

An On-Chip High-Efficiency DC-DC Converter with a Compact Timing Edge Control Circuit

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Abstract

We developed an on-chip DC-DC converter with a compact timing edge control circuit operating at high clock frequency. The circuit generates four states to control nearly ideal switchings of output transistors depending on the voltages sensed at two terminals across an off-chip output inductor. High efficiency can be achieved due to nearly exact timing edge control with the aid of a high frequency clock by eliminating the conventional dead time control circuit.

The DC-DC converter is fabricated in 0.25 μ m CMOS process with single polysilicon and triple metal. The experimental results at 2.5V output show efficiency over 90% with a off-chip filter consisting of an inductor of 220 μ H and a ceramic capacitor of 47 μ F. The converter has maximum efficiency of 93.3% with 29mV ripple at 37mA load current.

Introduction

In recent years, the number of portable personal communication systems such as mobile telephones, pagers and laptop computers has grown explosively. Such portable systems demands the use of a compact on-chip DC-DC converter with high efficiency for low-power LSIs.

High-efficiency DC-DC converters based on zero-voltage switching (ZVS) architecture have been implemented into a Si chip with the use of either a complex controller to generate accurate switching timings [1] or a large delay block [2] to achieve low-noise operation.

The aim of this paper is to describe an on-chip DC-DC converter with a compact timing control circuit, for which both an additional auxiliary feedback loop and a high frequency clock are used to keep the output voltage constant. The auxiliary feedback loop provides a signal in such a way that the control circuit triggers turning ON timings of the output MOS transistors to achieve nearly ideal ZVS.

Architecture

Fig. 1 depicts the block diagram of the architecture with two feedback loops. The feedback (A) is a conventional output monitoring path used in PWM self-resonance type buck converters, while the feedback (B) is used to control switching timings of the output power transistors in DC-DC converter to achieve ZVS. The control logic circuit of the DC-DC converter monitors V_z through the feedback (B) so that the power MOS transistors can be switched at ideal timings, when V_z , PWM output voltage, equals to either the supply voltage or ground.

Circuit Implementation

Fig. 2 shows the schematic of the timing edge control circuit. The timing chart of the DC-DC converter is shown in Fig. 3. Switches SW1 and SW2 are connected to node B, when V_{CI} ="high", otherwise connected to A.

The operation of the circuit is repeated through the following four states. At STATE1 where V_{out} is higher than a desired output voltage, the power NMOS transistor is ON, shorting V_z to GND and decreasing V_{out} . Once V_{out} crosses below the desired output voltage (V_{ref}), the Comparator 1 detects the timing and then the power NMOS is switched OFF at the subsequent rising edge of CLK (Fig. 3 (a)). At STATE2, both power transistors are OFF. The external inductor acts as a current source, increasing V_z . In order to achieve a lossless low-to-high transition, the power PMOS

transistor should be turned ON exactly when $V_z = V_{DD}$ which can be sensed with the Comparator 2 (Fig. 3 (b)). At STATE3, the negative to positive voltage transition across the inductor increases the charging current until V_{out} exceeds the desired output voltage. After the Comparator 1 detects the timing when V_{out} crosses above the desired output voltage (V_{ref}), the power PMOS is switched OFF at the subsequent rising edge of CLK (Fig. 3 (c)). Then, NMOS transistor is switched ON exactly when $V_z = GND$ (Fig. 3 (d)). Note that VC2 and VC3 control the exact turning ON timings of each transistor without reference to CLK. This operation achieves highly accurate control of ZVS, resulting in a high-efficiency DC-DC buck converter. Excessively fast transition of V_z causes timing error of ZVS, because of the delay in the control signal path. To avoid this, a capacitor C_z is integrated on a chip at the output. Turning OFF timings of each transistor are synchronized with CLK, which provides none ideal SW timings, causing the power losses in the output transistors. To reduce the power losses, we used a high frequency CLK at the cost of the increase of capacitive switching loss, thus avoiding the use of a delay generator consisting of complex control circuits.

Experimental Results

A test chip is fabricated in 0.25 μ m CMOS process with single polysilicon and triple metal. As shown in Fig. 4, the DC-DC converter with active area of 1.0mm \times 0.5mm is laid out very close to the I/O area to reduce metal wiring resistance. Thick oxide transistor is used for 3.3V input voltage. The external filter consists of a 220nH inductor with 550m Ω parasitic resistance, and a 47 μ F capacitor. Fig. 5 shows the measured output waveform at 2.5 output voltage from 3.3V supply with 20MHz clock.

Fig. 6 shows the measured efficiency of the DC-DC converter as a function of the load current for 2.0V and 2.5V output. Maximum peak efficiency of 93.28% is measured at 2.5V output and 37mA load current with 29mV ripple.

Table 1 shows the measured performance summary of the DC-DC converter.

Conclusion

We proposed an on-chip high-efficiency DC-DC converter with a newly developed compact ZVS control circuit operating at high clock frequency. The compact control block provides accurate turning On timings of the output transistors. Also, the power losses in turning OFF timings of each transistor is significantly reduced by using a high frequency CLK at the cost of the increase of capacitive switching loss, thus avoiding the use of a delay generator consisting of complex control circuits. The measured results show the power efficiency of over 90% at 2.5V output in the range of load current from 25mA to 93mA. The maximum efficiency of 93.3% is measured at 37mA load current.

References

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- [2] Shiro Sakiyama, Jun Kajiwara, Masayoshi Kinoshita, Katsuji Satomi, Katsuhiro Ohtani, and Akira Matsuzawa, "An On-Chip High-Efficiency and Low-Noise DC/DC Converter Using Divided Switches with Current Control Technique," in *IEEE ISSCC Dig. Tech. Papers*, 1999, pp. 156–157.

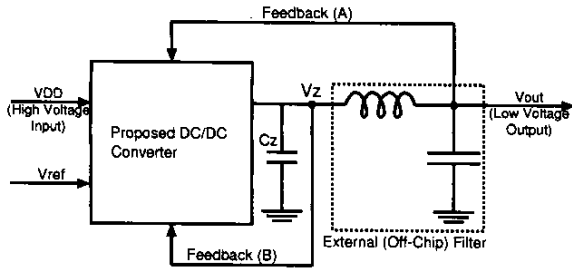


Fig. 1. Block diagram of the architecture.

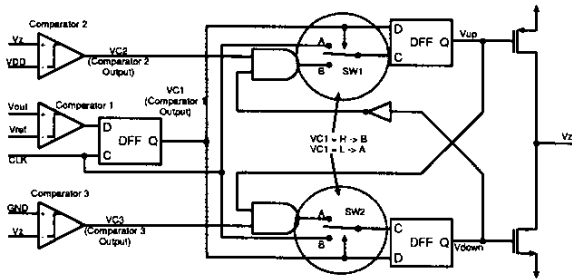


Fig. 2. Timing edge control circuit with power MOS transistors.

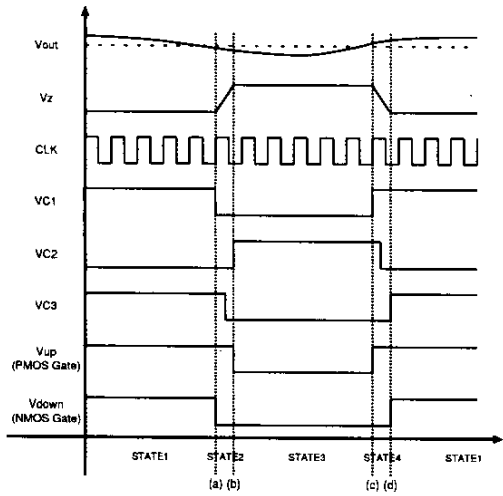


Fig. 3. Ideal timing chart of operation.

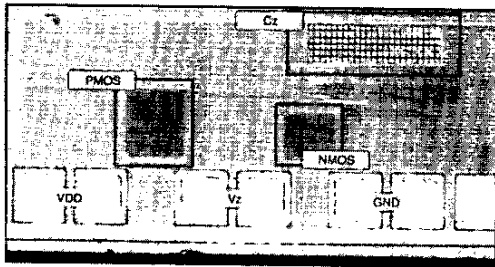


Fig. 4. Chip photography.

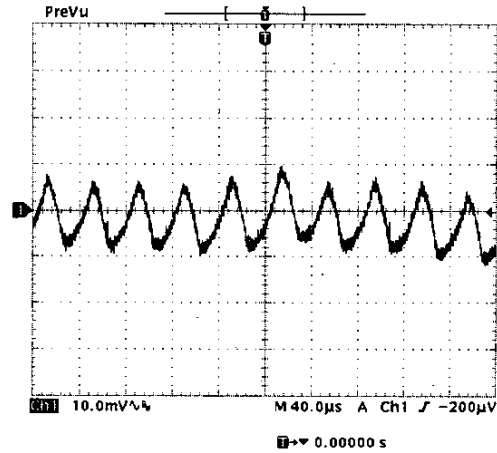


Fig. 5. Output waveform of DC-DC converter at 2.0V output with 20mA load current.

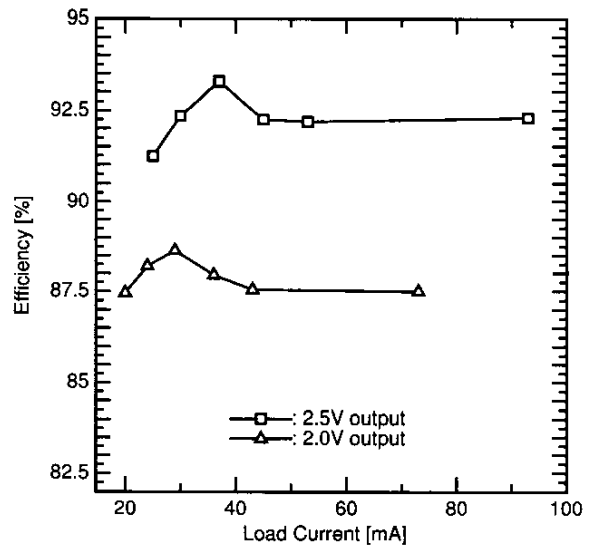


Fig. 6. Measured DC-DC converter efficiency vs. current load.

Table 1. Performance summary.

Process	0.25µm 1 poly 3 metal CMOS
Active area	Thick oxide transistor
Supply voltage	1.0mm × 0.5mm
Clock frequency	3.3V
Switching frequency	20MHz
Inductor (off-chip)	≅ 20KHz
Capacitor (off-chip)	220µH (with 550mΩ parasitic resistance)
Efficiency	47µF
Output ripple	93.28% @37mA current load, 3.3V→2.5V
Output voltage range	29mV @37mA current load, 3.3V→2.5V
Output current range	2.0V ~ 2.5V
	< 100mA