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A DYNAMIC LATCHED COMPARATOR WITH BUILT-IN OFFSET CALIBRATION

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Abstract

This paper presents a novel dynamic latched comparator that uses a built-in offset-cancellation technique. The proposed offset-cancellation scheme does not require any extra amplifiers or digital-assistant cancellation. Combining a conventional dynamic latched comparator with a one-stage amplifier benefits from not only an enhancement in comparator gain but also a reduction in power consumption. The Monte-Carlo simulation results, which were derived by using a 130-nm CMOS process, show that the comparator achieved a 3.8 mV equivalent input-referred offset voltage at a 10 MHz clock rate while dissipating 2.7 μW from a 1.2V supply.

1. Introduction

Comparators are the basic elements used for analog-to-digital converters, memory circuits, and so forth. They can have a significant impact on the

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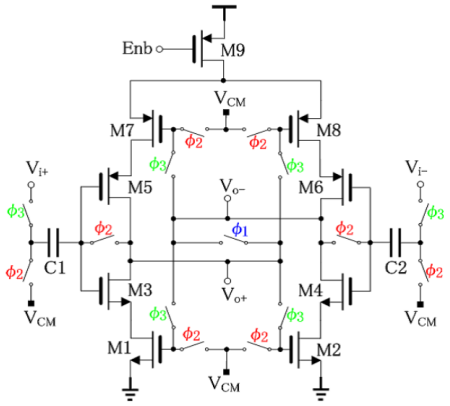
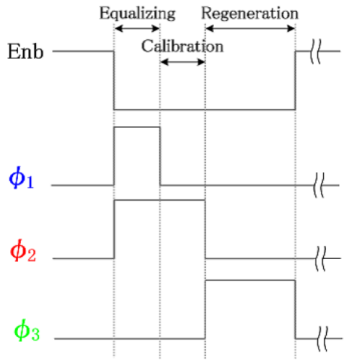
performance of their target applications in terms of accuracy, speed, and power consumption. In order to amplify a small input voltage to a fully logic voltage, comparators require very high gain. For dynamic latched comparators, a high voltage gain can be more easily achieved by adopting a positive feedback load. These comparators consume no static power. Therefore, such a comparator is widely utilized. However, dynamic latched comparators suffer from large input-offset voltages, which cannot be self eliminated. In conventional processes, a scheme that utilizes pre-amplifiers is used to reduce the offset voltage at the cost of an increase in power dissipation and delay [1]. Moreover, the continuing trend of technology scaling leads to a larger mismatch in MOS transistors and a lower voltage supply. As a result, it is difficult to design a high-performance pre-amplifier without increasing the power consumption. On the other hand, instead of using a pre-amplifier, a calibration technique based on a digital-assistant circuit becomes more attractive since it is likely to benefit from technology scaling [2, 3]. This technique generally reduces the offset voltage by feeding back an error signal during the output of the comparator. This method is an efficient approach, but increases in complexity and power consumption are inevitable.

In this paper, a dynamic latched comparator that utilizes a built-in offset-cancellation technique is proposed. The proposed topology of the comparator combines a conventional dynamic latched comparator with a one-stage amplifier, which is embedded in the same current path. Therefore, the comparator does not require any pre-amplifiers or digital-assistant circuits and also benefits from low power consumption.

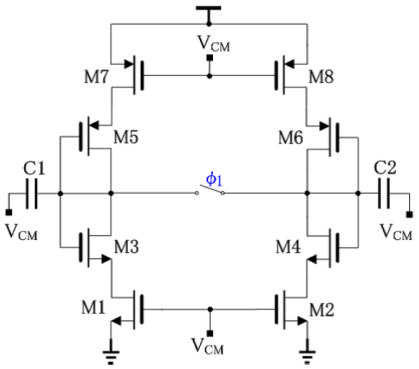
In Section 2, a detailed analysis is carried out to verify the proposed technique for the offset voltage cancellation. The simulations of this analysis are described in Section 3. The conclusions of this study are given in Section 4.



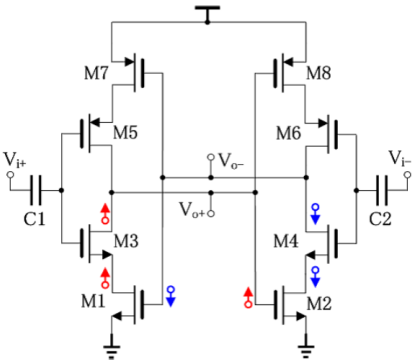
(a) Circuit configuration



(b) Timing diagram



(c) Equivalent circuit in equalization and calibration modes



(d) Equivalent circuit in regeneration mode

Figure 1. Proposed dynamic latched comparator.

2. Proposed Dynamic Latched Comparator

The circuit configuration of the proposed comparator is shown in Figure 1(a), and is mainly comprised of two modified latch stages and capacitors that are used for storing input-offset voltage. The stored offset voltage can be subtracted from the input signal to determine the offset-cancellation by using auto-zeroing techniques [4]. The proposed comparator is operated at equalization, calibration, and regeneration modes that are switched by using

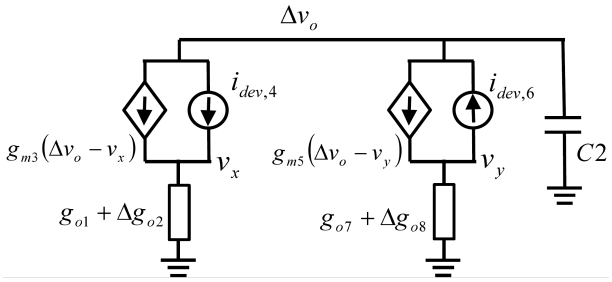
a clock, as shown in Figure 1(b). The operation of the comparator is described as follows. When the clock signals ϕ_1 and ϕ_2 increase, the comparator operates in the equalization mode illustrated in Figure 1(c), in which the switch is closed. The objective is to make the voltages of C1 and C2 equal so that the error resulting from the unbalance of the initial voltage can be compressed as much as possible. When the clock signal ϕ_1 decreases and ϕ_2 remains high, the comparator operates in the calibration mode illustrated in Figure 1(c), in which the switch is open. In this mode, the offset voltage resulting from M1-M8 is stored in the capacitors C1 and C2. Additionally, M3-M6 perform as a unity-gain amplifier. Thus, the proposed offset-cancellation technique can be considered to be based on the input-offset storage [1]. However, when ϕ_3 increases, the circuit is switched to the regeneration mode shown in Figure 1(d). The offset voltage generated by M1-M8 is the same as that caused during the calibration mode, and they consequently are mutually canceled by the subtraction of the offset voltage from the input signal.

In Figure 1(d), the M3-M6 transistors serve as a one-stage pre-amplifier as well as a part of the latch stage and are constructed in the current-reused configuration. Thus, its power consumption is significantly lower than the conventional dynamic latched comparator, which utilizes the pre-amplifiers and latch stages separately. The principle operation of the modified latch stage is described as follows. The up arrows and down arrows represent the voltage rises and drops, respectively. Assuming that the initial state of the output is $V_{o+} > V_{o-}$, V_{o+} tends to increase and V_{o-} tends to decrease at the start of operation. This mechanism apparently results from positive feedback. In the latch circuit, the gain of the latch stage can be generally defined as one-half the loop gain in decibels. For the modified latch stage, the gain of latch A_{latch} is given by

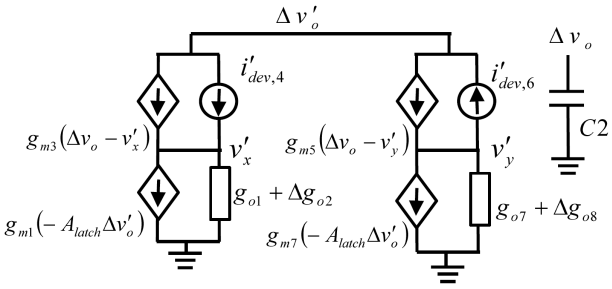
$$A_{latch} = (g_{m1} + g_{m7})\left[\left(\frac{g_{m3}}{g_{o3}g_{o1}} + \frac{1}{g_{o1}} + \frac{1}{g_{o3}}\right)//\left(\frac{g_{m5}}{g_{o5}g_{o7}} + \frac{1}{g_{o5}} + \frac{1}{g_{o7}}\right)\right], \quad (1)$$

where g_{mi} and g_{oi} are the transconductance and small-signal drain conductance of Mi, respectively. The above gain expression contains the term g_{m1}/g_{o1}, which indicates the gain of M1 that operates as a common-source amplifier, and the term g_{m3}/g_{o3} that is attributed to M3, which can be viewed as a common-gate amplifier. Consequently, the gain of the modified latch is significantly reinforced compared with a common-source amplifier. The enhancement of gain is expected to improve the voltage transition.

Next, the operation of the offset voltage cancellation is explained in detail with a small-signal analytical expression. It is worth noting that M9 is operated as a current source and it is not taken into account because of its limited effect on the performance of the entire circuit.



(a) Calibration mode



(b) Regeneration mode

Figure 2. Half small-signal equivalent circuit of proposed dynamic latched comparator.

In the calibration mode, most of the supply voltage is occupied by M3-M6, since they are operated in a saturation region. Therefore, the voltages between the drains and sources of M1-M2 and M7-M8 decrease to smaller values compared to their overdrive voltages determined by using the gate voltage V_{CM}. For this reason, M1-M2 and M7-M8 are operated in a linear region. For simplicity, the drain conductances of M3-M4 and M5-M6 that are operated in the saturation region are neglected. In this case, the offset voltage originates from the mismatch of the threshold voltage V_{TH} and transconductance parameter β (depending on carrier mobility, gate oxide thickness, and gate width/length) of the MOS transistor [5]. To evaluate this, a half equivalent circuit (M2, M4, M6, and M8) that focuses on the deviations from the other half of the circuit (M1, M3, M5, and M7) in the comparator is utilized as illustrated in Figure 2(a). The deviations of the drain conductance and currents originating from the threshold voltage and transconductance parameter β of the MOS transistors in Figure 2(a) are calculated as follows:

$$\Delta g_{o2} = \frac{\Delta\beta_2}{\beta_1} g_{o1} - \beta_1 \Delta V_{TH,2}, \quad \Delta g_{o8} = \frac{\Delta\beta_8}{\beta_7} g_{o7} + \beta_7 \Delta V_{TH,8}, \tag{2}$$

$$i_{dev,4} = \frac{\Delta\beta_4}{\beta_3} I_{D3} - g_{m3} \Delta V_{TH,4}, \quad i_{dev,6} = \frac{\Delta\beta_6}{\beta_5} I_{D5} + g_{m5} \Delta V_{TH,6}, \tag{3}$$

where $\Delta\beta_i = \beta_i - \beta_{i-1}$, $\Delta V_{TH,i} = V_{TH,i} - V_{TH,i-1}$, and I_{Di} are the drain bias current of Mi. By solving the half circuit shown in Figure 2(a), the deviation of the output voltage in the calibration mode is given by

$$\Delta v_o = -\frac{(g_{m4,eff}/g_{m3}) i_{dev,4} - (g_{m6,eff}/g_{m5}) i_{dev,6}}{g_{m4,eff} + g_{m6,eff}}, \tag{4}$$

$$g_{m4,eff} = \frac{g_{m3}(g_{o1} + \Delta g_{o2})}{g_{m3} + g_{o1} + \Delta g_{o2}} \approx \frac{g_{m3} g_{o1}}{g_{m3} + g_{o1}} \left[1 + \frac{g_{m3} \Delta g_{o2}}{g_{o1}(g_{m3} + g_{o1})}\right], \tag{5}$$

$$g_{m6,eff} = \frac{g_{m5}(g_{o7} + \Delta g_{o8})}{g_{m5} + g_{o7} + \Delta g_{o8}} \approx \frac{g_{m5} g_{o7}}{g_{m5} + g_{o7}} \left[1 + \frac{g_{m5} \Delta g_{o8}}{g_{o7}(g_{m5} + g_{o7})}\right]. \tag{6}$$

The input-referred offset voltage corresponds to Δv_o, and is primarily dominated by the mismatches of the channel resistances of M1-M2, M7-M8, and the threshold voltages of M3-M4 and M5-M6.

In the regeneration mode, the comparator amplifies the small input voltage to a detectable logic level. The equivalent input-referred offset voltage Δv_o can be stored with the Gaussian-distributed values located on the gate node of each differential pair in series [6]. To evaluate the output-referred offset voltage, the differential input voltage is set to zero. It should be noted that the initial output voltages of the regeneration mode are assumed to be nearly equal to V_{CM}, which is defined as one-half the supply voltage. To evaluate the output-referred offset voltage $\Delta v_o'$ in the regeneration mode, a similar half equivalent circuit (M2, M4, M6 and M8) that focuses on the deviations from the other half circuit (M1, M3, M5 and M7) in the comparator is utilized as illustrated in Figure 2(b). Owing to the existence of the positive feedback paths, the deviations of the drain currents $i'_{dev,4}$ and $i'_{dev,6}$ differ slightly from those in the calibration mode ($i_{dev,4}$ and $i_{dev,6}$). By solving the half circuit shown in Figure 2(b), the deviation of the output voltage in the regeneration mode is given as

$$\Delta v_o' = \frac{1}{A_{latch}} \frac{g_{m4,eff}(\Delta v_o + i'_{dev,4}/g_{m3}) + g_{m6,eff}(\Delta v_o - i'_{dev,6}/g_{m5})}{g_{m4,eff}\, g_{m1}/(g_{o1} + \Delta g_{o2}) + g_{m6,eff}\, g_{m7}/(g_{o7} + \Delta g_{o8})}. \quad (7)$$

Substituting Equation (4) into Equation (7) gives the following:

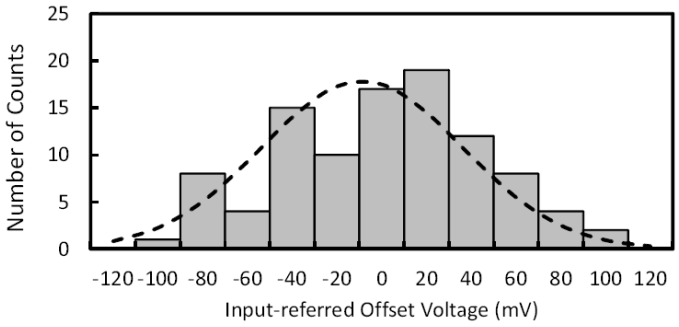
$$\Delta v_o' = \frac{1}{A_{latch}} \cdot \frac{(g_{m4,eff}/g_{m3})(i'_{dev,4} - i_{dev,4}) - (g_{m6,eff}/g_{m5})(i'_{dev,6} - i_{dev,6})}{g_{m4,eff}\, g_{m1}/(g_{o1} + \Delta g_{o2}) + g_{m6,eff}\, g_{m7}/(g_{o7} + \Delta g_{o8})}. \quad (8)$$

If the values of $i'_{dev,4} - i_{dev,4}$ and $i'_{dev,6} - i_{dev,6}$ are small and the value of A_{latch} is large, $\Delta v_o'$ gets very small. This shows that the offset voltage caused during the calibration mode can be canceled during the regeneration mode.

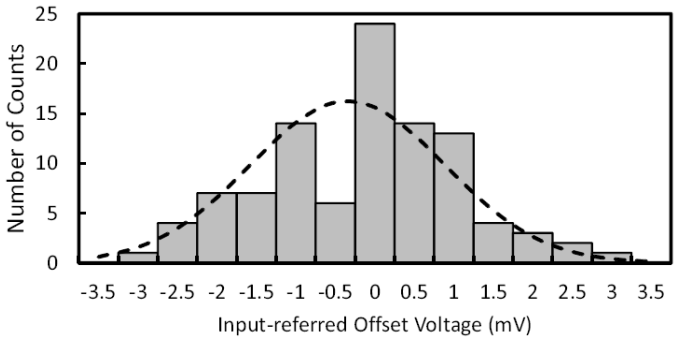
3. Simulation Results

The proposed dynamic latched comparator was designed and simulated by using a 130-nm CMOS process. The gate width and length of M1-M4 are 24μm and 0.3μm, and those of M5-M8 are 60μm and 0.3μm. To maintain the current consumption, the gate width and length of M9 are 0.16μm and 1μm. All of the switches are CMOS transmission gate with a small size (PMOS gate width: 4μm, NMOS gate width: 1.6μm, gate length: 0.12μm) so as to reduce the effect of charge injection. Each of all MOS devices has connection between its source and body with triple-well process to avoid body effect. The capacitors C1 and C2 are 88 fF.

In order to verify the usefulness of the proposed offset-cancellation method, a proposed comparator without any input storage capacitors was introduced for comparison. Except for the offset-cancellation function, the performance of the comparator was expected to be identical to the proposed latched comparator. The equivalent input-referred offset voltage was observed by applying a ramp signal to the comparator input. Both comparators were operated with a 10MHz clock frequency and 1.2V supply. The results were obtained by carrying out 100 Monte-Carlo transient simulations. Distributions of the equivalent input-referred offset voltage of the comparator without and with calibration are illustrated as histograms in Figures 3(a) and 3(b). For the comparator without the offset-cancellation function, the maximum equivalent input-referred offset extension is up to 134mV at $\pm 3\sigma$. In contrast, the maximum offset voltage of the proposed comparator is reduced to 3.8mV. It should be noted that larger capacitors C1 and C2 can be beneficial to the offset-cancellation at the cost of a decrease in operating speed.



(a)



(b)

Figure 3. Monte-Carlo simulation results of the equivalent input-referred offset voltage distribution (a) without and (b) with the offset-cancellation function (100 trials).

The proposed comparator consumes less than 2.7μW of dynamic power with a clock frequency of 10MHz and a 1.2V supply. In this study, the ratio of period between ϕ_1, ϕ_2 and ϕ_3 is set as 1:2:2 approximately. Current dissipation can be scaled down by decreasing the pulse width of ϕ_2 during the calibration mode. Furthermore, Table 1 compares the performances of our design to that of other studies.

In practical case, there are some timing variations of ϕ_1, ϕ_2 and ϕ_3 through clock buffers. Even considering the clock buffer delay variation for each of CMOS switches, the simulation result shows that the maximum offset voltage of the proposed comparator is only 4.1mV.

Table 1. Performance summary and comparisons

Performance	Ref. [7]	Ref. [8]	This work
Offset voltage [mV]	2	4	3.8 [$\pm 3\sigma$]
Power consumption [μW]	3.5	43	2.7
Sampling frequency [MHz]	20	10	10
Supply voltage [V]	1.2	3	1.2
Process [nm]	180	600	130

4. Conclusions

A low-offset dynamic latched comparator with a built-in offset calibration that does not require extra amplifiers or digital cancellation was proposed. This structure contributes to the compact size of the comparator circuit and lower power consumption. The proposed comparator was verified by using analytical method and simulation. The simulation results show that the equivalent input-referred offset voltage can be reduced to 3.8mV at $\pm 3\sigma$ when using a 10MHz clock frequency and 1.2V supply.

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References

[1] B. Razavi and B. A. Wooley, Design techniques for high-speed, high-resolution comparators, IEEE J. Solid-State Circuits 27(12) (1992), 1916-1926.

[2] M. Miyahara, Y. Asada, D. Paik and A. Matsuzawa, A low-noise self-calibrating dynamic comparator for high-speed ADCs, IEEE Asian Solid-State Circuits Conference, Nov. 2008, pp. 269-272.

[3] C.-H. Chan, Y. Zhu, U.-F. Chio, S.-W. Sin, S.-P. U and R. P. Martins, A voltage-controlled capacitance offset calibration technique for high resolution dynamic comparator, IEEE International SoC Design Conference, 22-24 Nov. 2009, pp. 392-395.

[4] A. Bakker, K. Thiele and J. H. Huijsing, A CMOS nested-chopper instrumentation amplifier with 100-nV offset, IEEE J. Solid-State Circuits 35(12) (2000), 1877-1883.

[5] K. Uyttenhove and M. S. J. Steyaert, Speed-power-accuracy tradeoff in high-speed CMOS ADCs, IEEE Trans. Circuits and Systems II 49(4) (2002), 280-287.

[6] B. Razavi, Principles of Data Conversion System Design, IEEE Press, New York, 1995.

[7] S. Kwon and H. Lee, A 1.2V, 3.5μW, 20MS/s, 8-bit comparator with dynamic-biasing preamplifier, Proc. 2006 IEEE International Symposium on Circuits and Systems, 21-24 May 2006, pp. 4767-4770.

[8] K. Kotani, T. Shibata and T. Ohmi, CMOS charge-transfer preamplifier for offset-fluctuation cancellation in low-power A/D converters, IEEE J. Solid-State Circuits 33(5) (1998), 762-769.