A Novel Transient Thermal Characterization System for Power Modules

Shuhei Fukunaga, *Member, IEEE,* and Tsuyoshi Funaki, *Senior Member, IEEE*

***Abstract*—Thermal design of power modules has been required to ensure long-term reliability for industrial applications. The static test method utilizes the temperature dependency of I-V characteristics on power devices to characterize the transient thermal resistance of power module packages. With modern power modules achieving high heat dissipation performance, accurate transient thermal characterization demands precise measurement of the fast and small voltage responses associated with their enhanced thermal performance. This paper develops an advanced transient thermal characterization system to capture the fast and small electrical response of power modules for their appropriate thermal characterization. The performance of the developed system is evaluated based on the experiment compared with the conventional characterization system and is validated with numerical simulation.**

***Index Terms*—Semiconductor device packaging, SiC MOSFET, thermal design**

I. Introduction

WIDE bandgap (WBG) power devices such as silicon carbide (SiC) and gallium nitride (GaN) are attracting attention for energy savings in industrial applications. The superior characteristics of SiC power devices, which promise low on-state resistance and high-speed switching capability, allow for the miniaturization of power conversion systems, especially in high-voltage industrial applications [1]–[3]. Additionally, they are expected to operate at higher temperatures compared to silicon (Si) power devices, exceeding 200 °C [4]. While this capability enables the miniaturization of power conversion systems without the need for large cooling systems, the heat dissipated per unit area/volume increases, which leads to reliability issues in power module packages [5]. Therefore, the thermal design of power modules is crucial to fully utilizing the potential of SiC power devices [6].

Heat generated at the junction of the power device flows to the heatsink through the power module. The heat flow path is modeled as a transient thermal network by the static test method [7]. This method utilizes the temperature dependency in the I-V characteristics of power devices to estimate the junction temperature (T_J). The time response of T_J, estimated by the electrical test method [8], provides the parameters of the thermal network model through deconvolution. Accurate thermal modeling of power module packages relies on the thermal response of the power device itself, which is used as both a heater and a sensor for the measurement. Typically, the thermal diffusivity of SiC power devices is more than twice that of Si power devices. In addition, the thickness of bare dies is expected to decrease to reduce the conduction loss of power devices. These factors result in a faster change in the initial time response of T_J when switched from the heating to cooling operation [9], [10]. Several literatures discussed and developed methods for estimating the initial T_J, i.e., the virtual T_J estimation, by adopting the post-processing algorithm or simulation tools [11]–[13]. For further improvements to enhance the accuracy of obtained transient thermal networks, a novel measurement system is required to directly capture the fast thermal response resulting from small time constants of power modules.

The electrical performance of the measurement system should be improved as it directly affects the accuracy and validity of obtained transient thermal networks estimated from the electrical response of the power device. The authors studied a high-speed and high-resolution data logging unit and a high-speed current switch box to capture the fast and small electrical response of power modules, which is suitable for their superior thermal performance [14], [15]. The advanced analysis algorithm was also developed to take advantage of the measured time response of T_J [16]. This paper establishes a novel transient thermal characterization system for power modules by integrating each developed hardware and software. The developed system is validated by comparing it with a conventional system for a SiC power module with a direct bonding copper (DBC) substrate. The measured time response of T_J is compared with the numerical simulation result to demonstrate the validity of the developed system. Moreover, we evaluate thermal resistance for several types of commercial Si and SiC power modules by using the developed characterization system.

II. Thermal Network Model Related to Power Module Package

This section outlines the measurement and evaluation procedure for transient thermal characterization of power module packages. The requirement for a measurement system in characterizing the thermal performance of modern power module packages is also introduced considering the material properties and the recent progress of manufacturing power devices.

A. Transient Thermal Characterization of Power Modules

The transient thermal network model is derived from the heat conduction equation [17], [18]. Fig. 1 illustrates a typical structure of a power module package with a direct bonded

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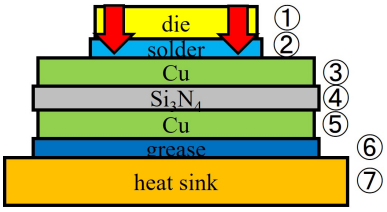
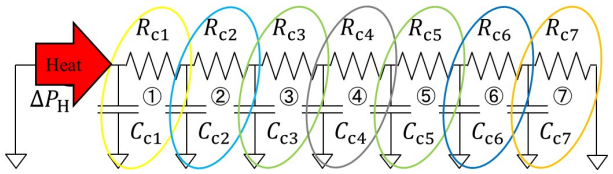
Manuscript received September xx, 2024; revised XX xx, 2024.



(a) Cross section structure of power module.



(b) Cauer thermal network model.

Fig. 1. An example of power module package with DBC substrate and related Cauer thermal network model.

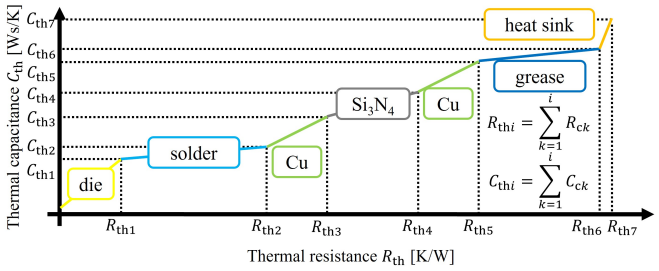


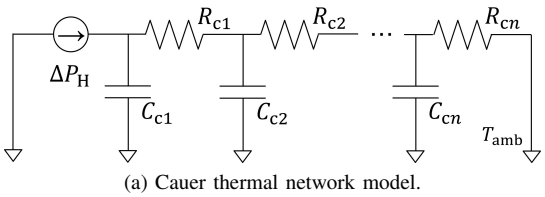
Fig. 2. An example of structure function related to Fig. 1.

copper (DBC) substrate. We assume a semi-infinite one-dimensional heat path, i.e., the heat generated at the junction of power devices primarily flows to the heat sink through each layer of the power module package in one direction. This heat flow path can be modeled by a Cauer thermal network model, which represents a series of cascaded pairs of thermal resistances and thermal capacitances, assuming uniformity in each layer of the power module package. The Protonotarios-Wing function [19], or the structure function [18], expresses the cumulative thermal capacitance as a function of the cumulative thermal resistance, as illustrated in Fig. 2. In other words, the structure function represents the transient thermal behavior of the respective components within the power module packages.

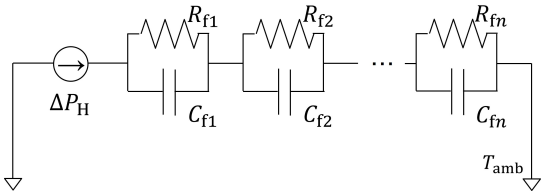
The thermal impedance of an n-th order Cauer thermal network model $Z_{\mathrm{C}}(s)$ in the Laplace (s-) domain is given by the following equation with the parameters in Fig. 3(a):

$$Z_{\mathrm{C}}(s) = \cfrac{1}{sC_{\mathrm{c1}} + \cfrac{1}{R_{\mathrm{c1}} + \cfrac{1}{sC_{\mathrm{c2}} + \cfrac{1}{R_{\mathrm{c2}} + \cdots + \cfrac{1}{sC_{cn} + \cfrac{1}{R_{\mathrm{cn}}}}}}}}. \tag{1}$$

The Cauer thermal network model corresponds to the physical parameters and structure of power module packages. However, it is difficult to extract their model parameters



(a) Cauer thermal network model.



(b) Foster thermal network model.

Fig. 3. Transient thermal network model.

directly from the measured results. Instead, we consider a numerical equivalent Foster thermal network model (Fig. 3(b)), whose parameters do not have a physical correspondence to the actual power module package. The thermal impedance of an n-th order Foster thermal network model $Z_{\mathrm{F}}(s)$ in the s-domain is given by the summation of fractional impedances using the parameters shown in Fig. 3(b):

$$\begin{aligned} Z_{\mathrm{F}}(s) &= \frac{R_{\mathrm{f1}}}{1 + sR_{\mathrm{f1}}C_{\mathrm{f1}}} + \cdots + \frac{R_{\mathrm{fn}}}{1 + sR_{\mathrm{fn}}C_{\mathrm{fn}}}, \\ &= \sum_{i=1}^{n} \frac{R_{\mathrm{fi}}}{1 + sR_{\mathrm{fi}}C_{\mathrm{fi}}}. \end{aligned} \tag{2}$$

By converting Eq. (2) from s-domain to time domain, the time response of junction temperature $T_{\mathrm{J}}(t)$ for ΔP_{H} power dissipation is calculated by the following equation:

$$T_{\mathrm{J}}(t) = \Delta P_{\mathrm{H}} \sum_{i=1}^{n} R_{\mathrm{fi}} \left[1 - \exp\left(-\frac{t}{\tau_{\mathrm{fi}}}\right)\right] + T_{\mathrm{amb}}, \tag{3}$$

where $\tau_{\mathrm{fi}} = R_{\mathrm{fi}}C_{\mathrm{fi}}$ denotes a thermal time constant. This equation implies that the measured time response of T_{J}, which is experimentally obtained from the power device in power modules, gives the parameters of the Foster thermal network model.

B. Static Test Method Standardized for Identifying Transient Thermal Network Model of Power Module Packages

Since power devices are fully molded to protect them from physical shocks and electrical insulation in the external environment, direct measurement of T_{J} by using such thermocouples or thermocameras is challenging. A unique feature of the static test method [7] is that utilizes the temperature dependence of the I-V characteristics in power devices as a heater and a sensor. The voltage drop for a fixed small current, whose self-heating is negligible, is proportional to the T_{J} of the power device. This is characterized as a TSEP, namely the K factor [8]. The K factor is obtained in advance under thermal equilibrium conditions using a temperature-controlled chamber for a constant small current. Thus, the time response of the terminal voltage (V_{T}) gives that of T_{J} via the K factor.

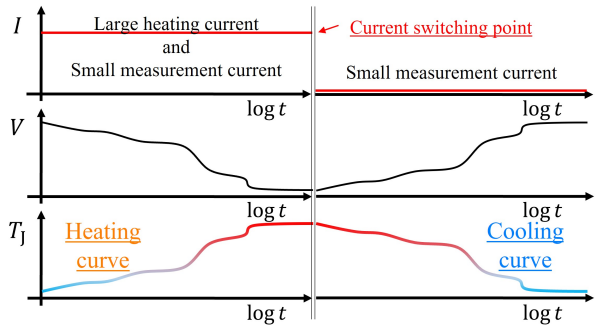


Fig. 4. Measurement procedure (show ideal response).

Figure 4 illustrates the procedure to obtain the time response of T_J. First, the device under test (DUT) is attached to a temperature-controlled cold plate. A large current, sufficient to induce self-heating, is applied to the DUT until it reaches thermal equilibrium. The heating current is then turned off, and the time response of V_T is measured during the cooling operation. The measured time response of V_T is then converted to that of T_J using the K factor. Note that although the ideal voltage and temperature time response are illustrated in Fig. 4, the overshoot voltage occurs in the experiment due to the current interruption from the heating to measurement, which will be discussed in detail in the next section.

The parameters of the Foster thermal network model are identified from the obtained time response of T_J. First, Eq. (3) is rewritten as a transfer function $a(t)$ for a unit power step.

$$a(t) = \frac{T_J(t) - T_{amb}}{\Delta P_H} = \sum_{i=1}^{n} R_{fi}\left[1 - \exp\left(-\frac{t}{\tau_i}\right)\right]. \quad (4)$$

Second, $a(t)$ is transformed to $a(z)$ by introducing the logarithmic time scale $z = \ln t$. Thermal time constant spectrum $R(z)$ is given as the following equation with the deconvolution integral $\otimes^{-1}$:

$$R(z) = \frac{d}{dz}a(z) \otimes^{-1} w(z), \quad (5)$$

where, $w(z) = \exp(z - \exp(z))$ is a known weighted function. Eq. (5) shows the relationship between the obtained time response of T_J and the Foster thermal network model. Finally, the Cauer thermal network model is derived from the identified Foster thermal network through a numerical equivalent transformation, specifically the Foster-Cauer transformation [20].

C. System Requirement for Transient Thermal Characterization Based on Electrical Method

Generally, it is difficult to directly measure the initial T_J at which switching from heating to cooling operation. It stems from the switching surge voltage across the DUT, induced by parasitics in the measurement system when interrupting the large heating current. To manage this, an extrapolation is used to estimate the initial T_J. The change in junction temperature, ΔT_{J0}, between $t = 0$ and t is derived from the one-dimensional heat conduction equation and given as follows [21].

$$\Delta T_{J0}(t) = \frac{\Delta P_H}{A} k_{therm}\sqrt{t}, \quad (6)$$

$$k_{therm} = \frac{2}{\sqrt{\pi c \rho \lambda}}. \quad (7)$$

Here, ΔP_H[W] denotes a heating power, A[m^2] denotes the heat dissipating area, and t[s] denotes the elapsed time from $t = 0$. c[J/(kg·K)], ρ[kg/m^3], and λ[W/(m·K)] denote a specific heat, density, and thermal conductivity of the material on the heat path, respectively. Eqs. (6) and (7) are used to estimate the initial T_J at $t = 0$ by the extrapolation. Note that users empirically determine the range for the extrapolation.

However, since the heat flows not only in the vertical direction but also in the horizontal direction, there is a limitation we can adopt the previous assumption, i.e., a semi-infinite one-dimensional heat path. Reference [9] defines a cut-off time t_b[s], which represents the propagation time from the junction on the top side to the bottom side of the bare die. Fourier's law for the bare die of the power device gives t_b as follows:

$$t_b = \frac{\delta^2}{12\alpha}, \quad (8)$$

where, δ[m] denotes the thickness of the bare die, and α[mm^2/s] denotes the thermal diffusivity. The extrapolation using Eq. (6) should be applied within the cut-off time to characterize the thermal property of the bare die. Table I shows the physical constants of major semiconductor materials at room temperature, and Table II shows an example of the cut-off time for Si and SiC power devices as a parameter of their thickness. The cut-off time of SiC power devices is lower than that of Si power devices because the thermal conductivity of SiC semiconductors is two to three times higher than that of Si semiconductors. Moreover, Eq. (8) indicates that thinner bare dies result in shorter cut-off times. As the trend moves toward thinner bare dies for reduced on-state and thermal resistance, for example, the latest Si IGBTs are less than 100 μm. Therefore, a precise thermal characterization system is essential for next-generation power devices and packages.

An integrated design with both hardware and software is necessary to capture the superior thermal performance of state-of-the-art power modules. A key challenge in capturing the fast thermal response of the bare die is a switching surge

TABLE I
THERMAL PARAMETERS OF MAJOR SEMICONDUCTOR MATERIALS AT ROOM TEMPERATURE [22], [23].

Material	λ[W/(m·K)]	c[J/(kg·K)]	ρ[kg/m^3]	α[mm^2/s]
Si	151	750	2300	87.5
SiC	490	690	3200	221.9
GaN	230	490	6150	76.3
Diamond	2000	510	3520	1114.1

TABLE II
AN EXAMPLE OF CUT-OFF TIMES FOR SI AND SIC BARE DIE.

Material	δ =377 μm	δ =300 μm	δ =200 μm	δ =100 μm
Si	135.3 μs	85.7 μs	38.1 μs	9.5 μs
SiC	53.4 μs	33.8 μs	15.0 μs	3.8 μs

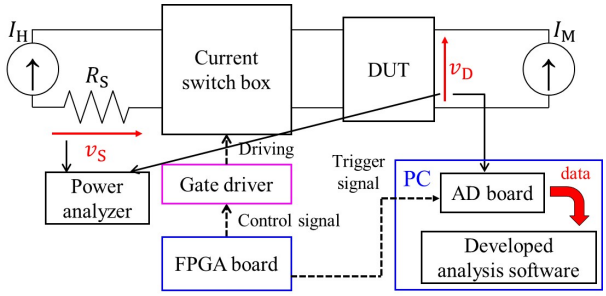


Fig. 5. Overview of the developed characterization system.

voltage elimination when interrupting the large current for self-heating. It stems from the parasitic inductance in the heating current path from the power supply to the DUT. The current switch box helps to reduce the shunt-off time of the large current by suppressing surge voltage, which enables the direct evaluation of the initial T_J related to the bare die immediately after current switching. Additionally, power modules are expected to reduce thermal resistance by applying promising materials with high thermal conductivity as well as the bare die. It results in a fast, small temperature change in the measurement. Therefore, a superior data logging unit with high-speed, high-resolution, and low-noise performance is required for the accurate thermal modeling of power modules with low thermal resistance.

In addition to the hardware design, dedicated analysis software is necessary in order to achieve higher noise reduction capability for identifying the accurate transient thermal network model from the obtained time response of T_J. Additional filtering or another signal-processing algorithm to gain a high signal-to-noise (S/N) ratio is also expected to maximize the obtained data from the developed hardware.

III. Developed Transient Thermal Characterization System

A. Overview of Developed Characterization System

Figure 5 illustrates the configuration of the developed transient thermal characterization system. The system consists of measuring and heating current source, a current switch box, a shunt resistor with R_S=10 mΩ for heating current measurement, an AD converter for logging the time response of junction voltage v_D on a DUT, and an FPGA board to control the system. A 6220 (Keithley) and a PU12.5-120 (TEXIO) are used as current sources for temperature estimation and self-heating, respectively. The heating power is calculated by the terminal voltages of the shunt resistance and DUT, which is measured by using a power analyzer WT-333E (Yokogawa). This paper uses an FPGA board Zybo Z7-20 (Digilent) to control the current switch box. The obtained time response of T_J is analyzed on the developed signal analysis software with the developed algorithm for identifying the transient thermal network model.

The rest of this section briefly explains the key components of the developed characterization system. Their details are addressed in our previous reports [14]–[16].

B. Sampling Unit for Measuring Time Response of Voltage

The time response of V_T on the DUT during the cooling operation is measured by using the AD converter. The sampling frequency and the bit length of the AD converter, which discretizes and quantizes the voltage response, affect the resolution and accuracy of the identified transient thermal network model. High-speed and high-resolution sampling capability successfully capture a fast and small temperature change in the time response of V_T, which stems from the superior thermal dissipation performance of power modules. High-speed sampling also contributes to increasing the effective vertical resolution based on oversampling [24]. Generally, the signal-to-noise ratio (SNR) of the quantization error to an ideal sinusoidal wave for full-scale input N_{bit} bit AD converter is given as follows [24]:

$$\text{SNR [dB]} = 6.02N_{\text{bit}} + 1.76 \tag{9}$$

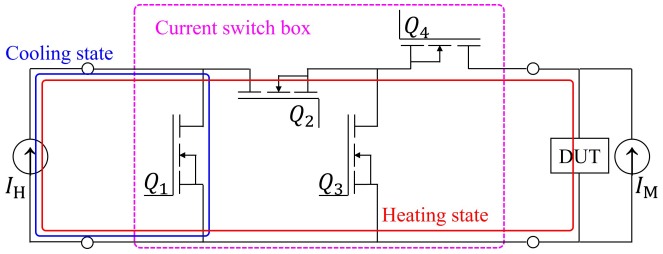
From Eq. (9), for example, the SNR of a 12-bit AD converter is 74 dB. Oversampling is the general method for suppressing the quantization error for the same bit length AD converter [24]–[26]. The improved SNR for oversampled signal ratio (OSR) is redefined after low-pass filtering and decimation as given by Eq. (10) [24].

$$\text{SNR [dB]} = 6.02N_{bit} + 1.76 + 10\log_{10}(OSR) \tag{10}$$

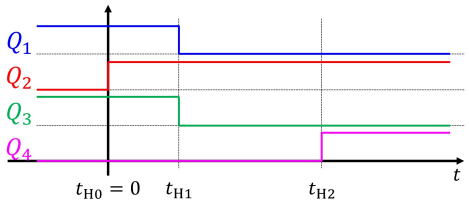
Since the post-processing of oversampling utilizes a low-pass filter, further reduction of noise superimposed on the measured data can be expected. The developed characterization system installs a high-speed and high-resolution AD board M2p.5933-x4 (Spectrum) on the PC [14]. This AD board can sample the voltage up to 40 MS/s with 16-bit resolution, which has a superior specification than the conventional measurement system with 1 MS/s, 12-bit resolution.

C. Current Switch Box

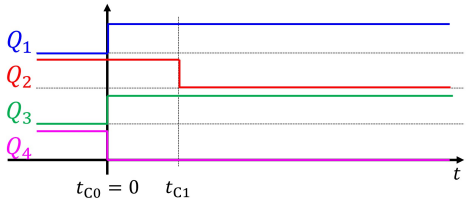
The current switch box is utilized to interrupt the large heating current within several microseconds. Fig. 6(a) illustrates a circuit diagram of a high-speed current switch box to achieve a fast cut-off of the large heating current [15]. The developed switch box is composed of four power switches, which are sequentially controlled by gate drivers and a controller FPGA. There are two current paths; the red line in Fig. 6(a) is the heating state, and the blue line is the measurement or cooling state. The heating current to a device under test (DUT) flows through MOSFETs Q2 and Q4 while it goes back to a power supply through Q1 in the cooling state of DUT. The parasitic diode of MOSFET Q3 works as the free-wheeling diode to commutate the residual current flowing through the DUT. In addition, MOSFETs Q2 and Q4 are connected in series in the opposite direction so that the measurement current does not flow to the current switch box in the cooling state of the DUT. The current path is switched in accordance with the ON/OFF state of each device for the sequential control signal shown in Figs. 6(b) and (c). Note that the time t_{H1} =1 μs, t_{H2} =2 μs, and t_{C1} =5 μs are determined by trial and error by considering the turn-on/off time of four switches and the shunt-off time of the heating current. Fig. 6(d) shows the photograph of the



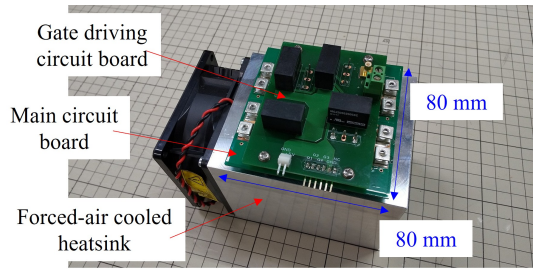
(a) Circuit diagram.



(b) Control sequence at heating operation.



(c) Control sequence at measurement operation.



(d) Photograph of current switch box.

Fig. 6. Circuit diagram and its control sequence of the current switch box.

implemented current switch box. The thick Cu wiring PCB circuit board and ϕ2 mm Cu via are adopted to flow large currents. This switch box is highly integrated to reduce the parasitic inductance in the circuit wiring.

In general, the relationship between the voltage difference of the DUT ΔV and the current change rate di/dt is given as the following equation, assuming a linear time-invariant circuit:

$$\Delta V = L_S \frac{di}{dt}. \tag{11}$$

Here, L_S represents the total parasitic inductance in the current path in the wiring of the circuit board and the cable from the output of the current switch box to the DUT. After the heating current is interrupted, the current value goes from the heating current for the self-heating of the DUT I_H to the measurement current I_M. The difference in the voltage drop for the heating and measurement current ΔV_{HC} is then given as follows with the current interrupting time Δt_i:

$$|\Delta V_{HC}| = \left| L_S \frac{di}{dt} \right| \approx \left| L_S \frac{\Delta i}{\Delta t_i} \right| = \left| L_S \frac{I_M - I_H}{\Delta t_i} \right|. \tag{12}$$

By transforming the Eq. (12) and assuming $I_M << I_H$, Δt_i can be given as follows:

$$\Delta t_i = L_S \frac{I_H}{\Delta V_{HC}}. \tag{13}$$

If we assume ΔV_{HC} to be constant regardless of the heating current, the current interrupting time is almost proportional to the total parasitic inductance and the heating current. Additionally, excess electromagnetic energy E_S is stored in the current path due to the parasitic inductance and the heating current given as $E_S = L_S {I_H}^2/2$. This excess energy induces the switching surge voltage across the DUT at the current interruption, which delays the evaluation time for the extrapolation. The developed switch box is designed to minimize parasitic inductance in the wiring on the circuit board and to dissipate the excess energy by utilizing the on-state resistance of the switches. It achieved a fast cut-off of the large current within 5 μs [16]. The current switch box in this paper is rated for a maximum current of 50 A and uses SiC MOSFETs SCT3017AL (Rohm) as switches. Note that the cable length from the current switch box to the DUT varies depending on the experimental setup, and it changes L_S in Eq. (13). The cable length should be as short as possible to minimize Δt_i.

D. Algorithm Improvement for Identifying Transient Thermal Network Model

The conventional algorithm described in [7] applies a moving average filter in the linear time domain to reduce noise in the measured signal. However, this method cannot effectively eliminate measurement noise, and the residual noise is emphasized during the numerical differentiation of $a(z)$ in Eq. (5), which degrades the accuracy of the identified transient thermal network model. Furthermore, the transformation from the linear to logarithmic time domain complicates the assumption of an equivalent sampling interval. Therefore, we developed an advanced signal processing algorithm for identifying the transient thermal network model. This algorithm employs a weighted discrete Fourier transformation (DFT) to eliminate measurement noise in the logarithmic frequency domain. Here is a brief description of the contents of [16].

Fourier transformation of a given function $x(z)$, and its inverse Fourier transformation are given by the following equations:

$$X(\Phi) = \int_{-\infty}^{\infty} x(z) e^{-j2\pi\Phi z} dz, \tag{14}$$

$$x(z) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(\Phi) e^{j2\pi\Phi z} d\Phi. \tag{15}$$

where, $j^2 = -1$. Note that Φ denotes logarithmic frequency corresponding to logarithmic time domain z. Assuming that $x(z)$ is periodic over $z = [a, b]$, the function is discretized with a non-uniform time step for N total data points. At this time, the fundamental frequency Φ_0 in the logarithmic frequency domain is given as follows:

$$\Phi_0 = \frac{1}{\Delta z_{max}}. \tag{16}$$

where, $\Delta z_{\max} = \max\{z_{i+1} - z_i\}$ for $0 \le i \le N-1$. Eq. (14) is discretized as follows with $\Phi_k = k\Phi_0$:

$$X(\Phi_k) = \int_a^b x(z) e^{-j2\pi \left(\frac{k}{z_{N-1} - z_0} \right) z} dz. \tag{17}$$

To apply Eq. (14) for non-uniform interval sampled data, $X(\Phi_k)$ is rewritten by adopting the trapezoidal formula as follows:

$$X(\Phi_k) \simeq \sum_{n=0}^{N-2} \left(x_{n+1} e^{-j2\pi \frac{k}{z_{N-1} - z_0} (z_{n+1} - z_0)} + x_n e^{-j2\pi \frac{k}{z_{N-1} - z_0} (z_n - z_0)} \right) \frac{(z_{n+1} - z_n)}{2}. \tag{18}$$

Eq. (18) is taken as a weighted discrete Fourier transformation. In order to suppress the influence of noise in the measured signal, a low-pass filter is adopted in the frequency domain. In practice, the Fermi-Dirac function F_{fd} [7] is used as the low-pass filter.

$$F_{\text{fd}}(\Phi_k) = \left[\exp\left(\frac{|\Phi_k| - \Phi_0}{\sigma} \right) \right]^{-1} \tag{19}$$

The shape of the Fermi-Dirac function is determined by two parameters: the bandwidth Φ_0 and the edge steepness σ. The parameter is adjusted for the best compromise between resolution and noise enhancement. $\Phi_0 = 0.45$ and $\sigma = 0.05$ are good values as given in [7].

Inverse discrete Fourier transformation (IDFT) is processed for the noise-eliminated signal in the logarithmic time domain. The non-uniform time step of the measured signal in the logarithmic time domain is transformed to the uniform time step by IDFT, i.e. the resynthesized signal is resampled. The conventional algorithm sets the output data to become 20-point samples per octave.

Practical deconvolution algorithms, such as Bayesian deconvolution [27] [28] and Fourier domain inverse filtering [29], have been applied for the transient thermal characterization of power modules. This paper performs Bayesian deconvolution for the low-pass filtered signal in the logarithmic time domain.

$$R_i^{(m+1)} = R_i^{(m)} \sum_k \frac{w_{ki} \left(\frac{da}{dz}\Big|_i \right)}{\sum_j w_{kj} R_i^{(m)}} \tag{20}$$

where, R_i is the discretized time constant spectrum, $R_i^{(m)}$ is the estimated R_i after m iterations, and $w_{ki} = \exp(z_k - z_i - \exp(z_k - z_i))$. Convolution and correlation sums in Eq. (20) have to be recalculated for each iteration step. The iteration number m seems to be sufficient to the order of 1000 in [27].

IV. Assesment of the Developed Transient Thermal Characterization System

The performance of the developed characterization system is evaluated with the obtained transient thermal network model in comparison to a conventional characterization system Simcenter T3STER (Siemens). The numerical simulation is also performed to discuss the validity of the time response of T_{J} obtained by the developed measurement system.

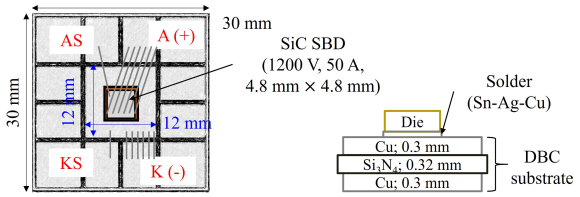


Fig. 7. Studied DBC substrate with SiC SBD.

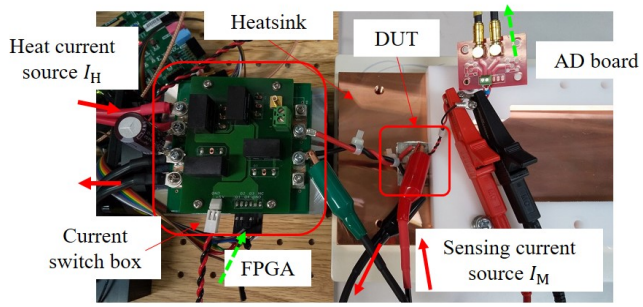


Fig. 8. Photograph of the measurement setup with the developed system.

A. Studied Sample and Experimental Setup

Figure 7 illustrates the schematic diagram of a studied sample, which is fabricated in the laboratory. A SiC Schottky barrier diode (SBD) S6305 (1200 V, 50 A, 4.8 mm × 4.8 mm) is attached to a DBC substrate with a Pb-free solder M705 (Sn-Ag-Cu, SMIC). The ϕ 300 μm aluminum wires are used for the electrical connection so as to flow the rated current. The insulation layer is composed of silicon nitride (Si_3N_4) with 320 μm thickness. The thick Cu pattern of 300 μm is bonded to both sides of the insulation layer.

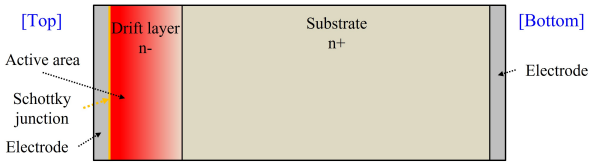
Figure 8 shows the measurement setup for the developed characterization system. The time response of V_{T} to the fixed small current 100 mA is sampled with 10 MS/s with a differential input. The time response of T_{J} is converted from voltage drop for a fixed measurement current and K factor. K factor is obtained by using a temperature-controlled chamber SH-661 (ESPEC) in advance based on the electrical test method [8], whose slope is -1.577 mV/K. The studied sample is mounted on a water-cooled copper heatsink with Si thermal grease. The coolant temperature is set at 25 °C.

B. Numerical Simulation Model for Validity Discussion

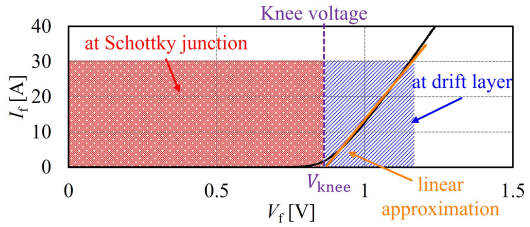
This paper performs a numerical simulation to validate the measured time response of T_{J} by the developed measurement system. This paper uses the simulation software FloEFD (Siemens), which is based on a finite volume method (FVM), and calculates the time response of T_{J} in the transient analysis. The physical parameters of materials used in the DUT are listed in Table III. The model emulates the experimental setup in Fig. 8 except for the heatsink. A simple rectangle block

TABLE III
PHYSICAL PARAMETERS OF MODULE PACKAGE MATERIALS.

	λ[W/(m·K)]	c[J/(kg·K)]	ρ[kg/m^3]
Sn-Ag-Cu	54	231	7400
Cu	402	385	8960
SiN	58	630	3500
grease	0.84	800	2340



(a) Cross section structure of studied SBD.



(b) Heat dissipating sharing based on the $I-V$ curve.

Fig. 9. Heat generation model of SBD.

TABLE IV
COMPARISON OF OBTAINED INITIAL T_J.

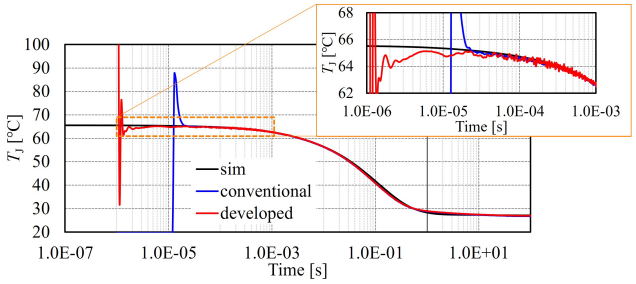
	simulation	conventional	developed
Time window for extrapolation	-	38-132 μs	7-31 μs
Obtained initial T_J	65.55 °C	63.64 °C	65.81 °C

is set as a heatsink instead of the water-cooled heatsink to make it easy to perform the simulation. The fixed ambient temperature is given uniformly across the opposite side of a heatsink to the sample mounted, and other model surfaces are thermally insulated.

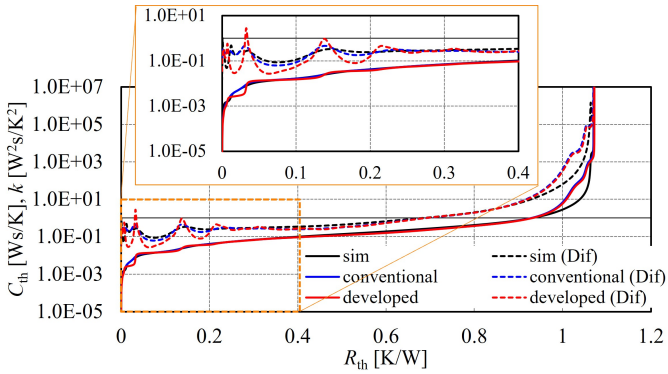
Figure 9(a) shows a detailed heat generation model of SBD bare die. Generally, the heat is generated in the Schottky junction and the drift layer of SBDs. The share of heat generation is identified by their I-V characteristics, whose boundary is determined as the intercept of the linear approximation for a large current region shown in Fig. 9(b). The heat generations at the junction and drift layer are 18.4 W and 17.0 W for I_H =30 A, respectively from the measured I-V characteristics of the DUT by using a semiconductor curve tracer. The drift layer is modeled as an active area (3.9 mm × 3.9 mm × 20 μm) in the bare die, and the heat generations are set as the surface and volume of the active area in the simulation.

C. Transient Thermal Characterization of SiC Power Module

Figure 10(a) shows the time response of T_J for DUT. The heating current is set by I_H =30 A and then the heating power P_H is about 36 W. The heating and cooling times are the same 100 s. The black, blue, and red lines are obtained from the simulation, the conventional characterization system T3Ster, and the developed characterization system, respectively. The



(a) Time response of T_J.



(b) Structure function.

Fig. 10. Obtained transient thermal network model.

red line coincides with the blue line well. Moreover, the result shows a faster convergence of voltage oscillation within 10 μs at the terminal voltage of DUT in the developed system than in the conventional system, which is close to the simulated time response of T_J. In other words, the developed system can directly measure the initial time response of T_J corresponding to the bare die and apply the extrapolation within the reasonable cut-off time. It stems from the fast cut-off of the heating current within several microseconds by the developed switch box. Table IV lists the values of the time window to extrapolate the initial T_J and the obtained initial T_J. The extrapolation from 7 μs to 31 μs in Fig. 10(a) is acceptable for the developed system. The estimated initial T_J of the developed system is closer to the simulation value than that of the conventional system.

Figure 10(b) shows the structure function of the DUT calculated from the obtained time response of T_J shown in Fig. 10(a). "Dif" denotes a differential structure function, which is a numerically differentiated structure function and its infection point indicates the boundary in the heat flow path of the power module packages. In calculating the structure function, the conventional analysis software T3SterMaster (Siemens) is applied to the simulated and measured results by T3Ster, and the developed software [16] is applied to the measured result by the developed system. In this work, 1000 Bayesian iterations and a resolution of 20 points/decade are used, which are default values of T3SterMaster. The same settings are applied for all the following structure function extractions. The developed system can successfully emphasize the inflection point related to the boundary between components in the actual structure of the power module package. This

TABLE V
STUDIED COMMERCIAL SI AND SIC POWER MODULES.

Name	CAS300M12BM2	WAB300M12BM3	FF3MR12KM1HHPSA1	FF300R12KT4P
Company	Wolfspeed	Wolfspeed	Infineon Technologies	Infineon Technologies
Generation	Gen 2 SiC MOS + Diodes	Gen 3 SiC MOS	CoolSiC™ Trench MOSFET	TRENCHSTOP™ IGBT4 + Emitter Controlled diode
Rated voltage	1200 V	1200 V	1200 V	1200 V
Rated current	300 A	300 A	280 A	300 A
$R_{\text{th(JC)}}$	0.070 K/W (S), 0.073 K/W (D)	0.16 K/W (S)	0.168 K/W (S)	0.121 K/W (S), 0.167 K/W (D)
Insulation plate	AlN	Si_3N_4	Al_2O_3	Al_2O_3

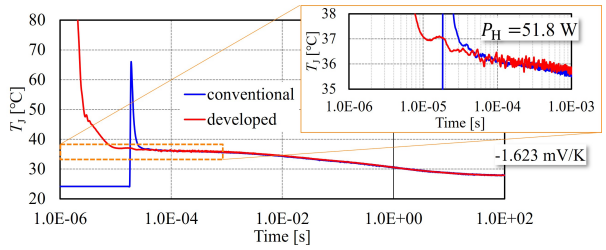
makes it easy to identify the internal structure of the module package from the transient thermal network model. The developed transient thermal characterization system contributes to accurate thermal design evaluation of SiC power modules by both hardware and software development.

V. TRANSIENT THERMAL CHARACTERIZATION OF SI AND SIC POWER MODULES WITH DEVELOPED SYSTEM

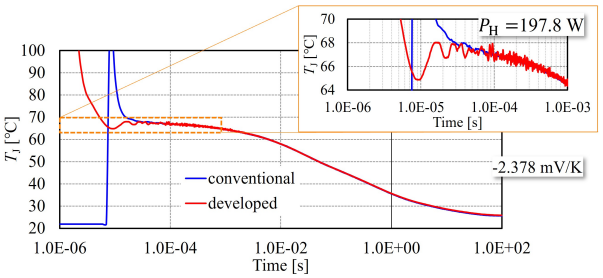
For further discussion about the validity of the developed characterization system, the transient thermal resistances of several commercial power modules are compared by using the conventional and developed characterization systems. Table V lists the studied commercial SiC and Si power modules. The rated voltage, current, and package type are almost the same. The generation of the implemented power devices and the insulation materials are referred from their datasheets. The junction-to-case thermal resistance $R_{\text{th(JC)}}$ is also referred from their datasheets, which would be determined from the finite element method (FEM) simulation. Here, "S" and "D" denote switches (MOSFET or IGBT) and anti-paralleled diodes for free-wheeling, respectively.

The transient thermal resistance of SiC power modules with SBD can be characterized by utilizing the SBD. The heating and measurement currents flow through the source to drain terminals, and then most of the current flows through the anti-paralleled SBD. SiC SBDs have theoretically no reverse recovery time, enabling the relatively fast transition from heating to cooling operation. The transient thermal resistance of SiC power modules without SBDs can be characterized by using the body diode of MOSFET, which is formed at the pn junction of MOSFET from the source-to-drain terminal. Note that SiC MOSFETs still have difficulty in their transient thermal characterization due to electrical characteristic fluctuations, especially the dynamic gate threshold voltage shift. Clamping the gate-to-source voltage with a fixed negative gate bias voltage is required to avoid the influence of the dynamic gate threshold voltage shift and achieve the transient thermal characterization of SiC MOSFETs [30], [31]. This paper applies $V_{\text{GS}} = -9$ V with a battery to the gate-to-source terminal, whose value is determined from the $I_{\text{D}} - V_{\text{DS}}$ characteristics in reverse conduction with V_{GS}. For the characterization of Si IGBT module, a constant $V_{\text{GE}} = +9$ V with a battery is applied to the gate-to-emitter terminals, and the heating and measurement currents flow to the collector-to-emitter terminals. This method is called SAT mode by the supplier of the conventional system.

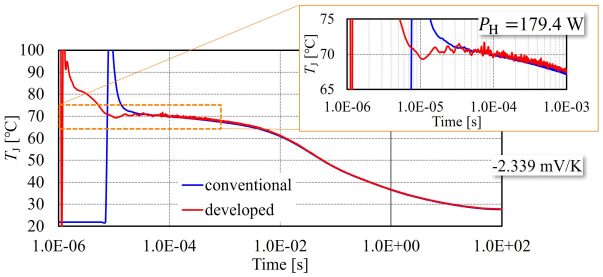
Figure 11 shows the time response of T_{J} for the studied power modules. The heating current is set at the same I_{H} =50 A and the heating power P_{H} is indicated in each figure. The heating power varies among sample modules due to differences in their $I - V$ characteristics. The measurement current



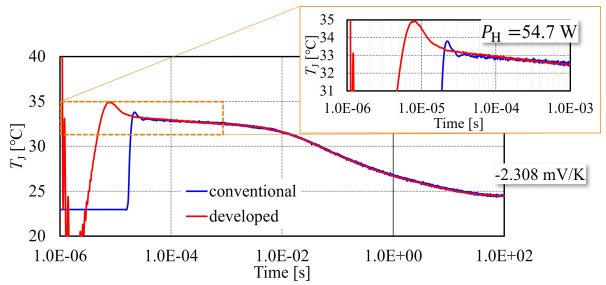
(a) CAS300M12BM2.



(b) WAB300M12BM3.



(c) FF3MR12KM1HHPSA1.



(d) FF300R12KT4P.

Fig. 11. Time responses of T_{J} for commercial power modules.

TABLE VI
COMPARISON OF OBTAINED INITIAL T_J FOR COMMERCIAL MODULES.

	CAS300M12BM2		WAB300M12BM3		FF3MR12KM1HHPSA1		FF300R12KT4P	
	conv.	dev.	conv.	dev.	conv.	dev.	conv.	dev.
Time window for extrapolation	189-376 μs	7-31 μs	99-189 μs	17-43 μs	127-215 μs	17-43 μs	135-375 μs	27-44 μs
Obtained initial T_J	33.32 °C	36.65 °C	67.08 °C	69.17 °C	68.00 °C	68.45 °C	33.59 °C	34.16 °C

is 100 mA, and both heating and cooling times are set to 100 s. The time response of T_J is converted from that of the voltage drop for the measurement current by using individual K factor, which is also indicated in each figure. The sample is mounted on a water-cooled copper heatsink with a Si thermal grease and the coolant temperature is set at 25 °C. The obtained time response of T_J with the developed system closely matches that of the conventional system well. The developed system shows faster convergence of voltage oscillations compared to the conventional system for all modules regardless of device type. Modules with SBDs exhibit faster oscillation convergence than those without SBDs, which is attributed to differences in turn-off times related to the reverse recovery phenomenon of FWDs. The measurement delay is larger for Si IGBT modules than for SiC power modules. This is because the injected minority carrier in the drift region of Si IGBTs takes time for recombination though the collector current does not flow by shunting off current externally. Table VI lists the values of the time window to extrapolate the initial T_J and the obtained initial T_J. Here, "conv." and "dev." denote the results obtained by the conventional and developed systems. The extrapolations to estimate the initial T_J for modules with and without SBDs, and Si IGBT are applied from 7 μs to 31 μs, from 17 μs to 43 μs, and from 27 μs to 44 μs, respectively. The developed system successfully captures the fast temperature changes inside the power devices, which results in avoiding the underestimation of the initial T_J.

Figure 12 shows the structure function of the DUT calculated from the obtained time response of T_J shown in Fig. 11. The developed system emphasizes the inflection points that correspond to the boundaries between components in power modules, regardless of the device type used for characterization. The identified package components based on inflection points from the developed system are also shown in Fig. 12. The identified thermal resistances $R_{\text{th(JC)}}$ from the structure-function coincide with those from the datasheet in Table V. This system successfully reveals the detailed package structure and provides quantitative thermal resistance such as the chip area and insulation materials. The developed transient thermal characterization system enhances the accuracy of thermal design evaluations for power modules with low thermal resistance through both hardware and software improvements.

VI. CONCLUSION

This paper developed a novel transient thermal characterization system to evaluate the superior thermal performance of state-of-the-art module packages and their materials. The main features of the developed characterization system are as follows; a high-speed and high-resolution sampling unit, a high-speed current interrupting circuit within several microseconds, and an advanced signal processing algorithm to obtain a high S/N ratio. Transient thermal characteristics of power modules were evaluated using the developed characterization system, and its results showed the validity and usefulness of the developed system for identifying the package structure of the Si and SiC power modules more precisely than the conventional system, regardless of SiC SBDs, SiC MOSFETs, and Si IGBTs. The developed system enables us to evaluate the thermal performance of the bare die itself in power modules, which are expected to have high heat dissipation capability, as well as power modules with even higher heat dissipation performance.

ACKNOWLEDGMENTS

The authors wish to acknowledge the partial support received under Grant 22K14239 (Kakenhi Young Scientists) of the Japanese Society for the Promotion of Science (JSPS), the Nagamori Foundation, and the MEXT-Program for Creation of Innovative Core Technology for Power Electronics Grant Number JPJ009777.

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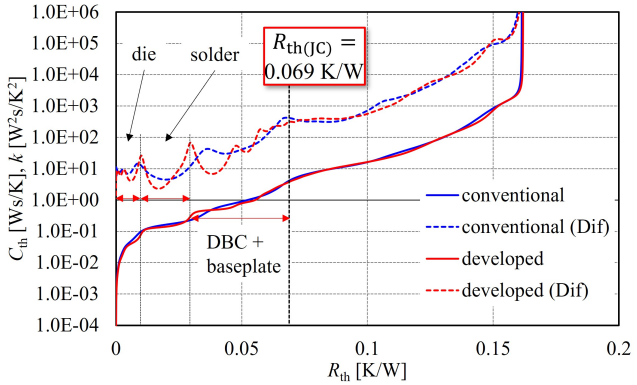
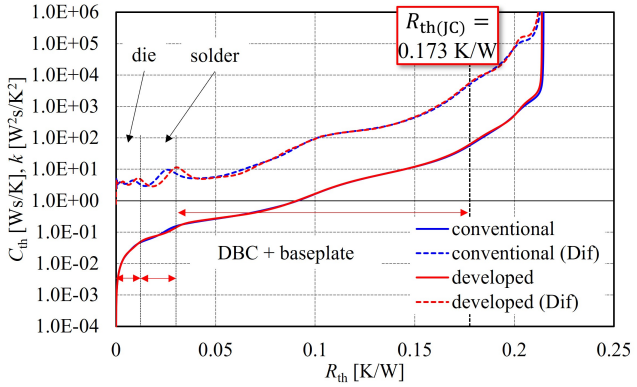
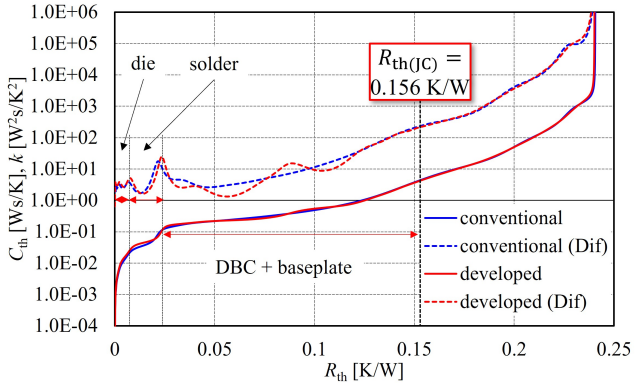


(a) CAS300M12BM2.



(b) WAB300M12BM3.



(c) FF3MR12KM1HHPSA1.

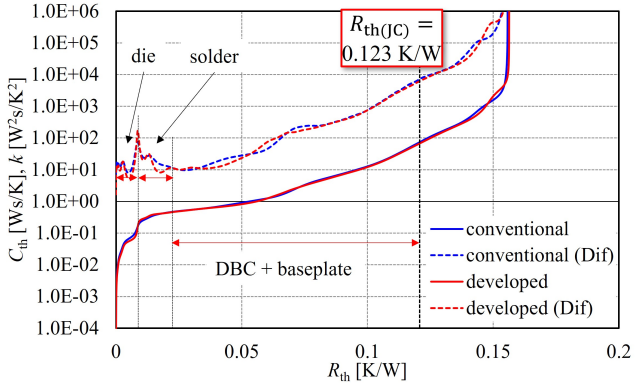


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Fig. 12. Structure functions of commercial power modules.

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