Letter

Room-temperature spin transport through band-to-band tunneling at semiconductor *p*-*n* junctions

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We report electrical spin injection, transport, and detection at room temperature through band-to-band tunneling (BTBT) at semiconductor *p*-*n* junctions. Using germanium-based lateral spin-valve devices with *p*-*n*-junction electrodes, we experimentally observe pure spin-current transport through BTBT at room temperature. Asymmetric bias-current dependence of the spin signals is evidently found, which originates from the spin injection via BTBT through *p*-*n* junctions or the spin extraction via localized states near *p*-*n* junctions. Notably, even for the use of a thin *p*-type semiconductor layer at the spin injector and detector, we find clear spin-transport properties at room temperature. This study will open a path for the room-temperature operation of a spin-based tunnel field-effect transistor with a *p*-*n* junction.

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Spin transport at room temperature in semiconductors (SCs) is a key requirement for achieving nonvolatility, reconstructibility, and ultralow power consumption for SC-based electronic devices [1–5]. Because of the space-inversion symmetry, group-IV SCs, such as carbon (C), silicon (Si), and germanium (Ge) have been explored for the room-temperature spintronic technologies [6–11]. Furthermore, Ge is not only a next-generation channel material for CMOS transistors [12] but is also compatible with spin-based photonics [11,13,14] and quantum computing devices [15,16].

Thus far, we have developed a highly efficient spin injection and detection technique with Co-based ferromagnetic Heusler alloy, $Co_2FeAl_{0.5}Si_{0.5}$ (CFAS) [17,18], and Co_2MnSi (CMS) [19], as spin injectors and detectors for Ge-based lateral spin-valve (LSV) devices. Also, a Schottky-tunnel contact consisting of the Co-based ferromagnetic Heusler alloy and a phosphorus (P) δ-doped Ge layer has been utilized to promote the tunneling conduction of spins without using insulator tunnel barriers [11,19–21]. These techniques are well established for exploring the spin injection and detection efficiency [22] and the spin-relaxation mechanism in group-IV SCs [11,17,23].

Recently, Ge-based metal-oxide-semiconductor field-effect transistors (MOSFETs) with top-gate stacks and the Co-based ferromagnetic Heusler alloy electrodes were fabricated [24,25]. Although we observed a relatively high field-effect electron mobility of approximately 350 cm^2/Vs [25] compared to those in a Si-based back-gate spin-MOSFET reported previously [26], the ON:OFF ratio of the source-drain (S-D) current flows is still low for the application level. Since this is attributed to the small built-in potential and the barrier height between the *p*-*n* junction in the S-D region, it is indicated that the OFF-state leakage current of the MOSFET, corresponding to the junction leakage current, became relatively high because of the presence of the defects in Ge spin-transport layers [25]. To overcome the above issue, we should explore the other approaches to demonstrate a great current modulation in a transistor structure other than the MOSFET.

For spintronic applications, we here draw inspiration from a tunnel FET (TFET) structure [27–33]. In general, TFETs utilize quantum-mechanical band-to-band tunneling (BTBT) from *p*-type SC layer to *n*-type SC one through the *p*-*n* junction for the current modulation with low power

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consumption [27–33]. Even for Ge, the BTBT was discussed for a TFET [28–30,33]. As a first step for an application of the TFET to spintronics, one should explore the spin transport through BTBT at Ge p-n junctions, considered for the spin TFET applications. Although there are several studies on the spin transport through BTBT at p-n junctions having ferromagnetic semiconductors [34–37], all the data were limited to the low-temperature demonstrations less than room temperature unfortunately.

In this letter, we show pure spin-current transport through BTBT at Ge p-n junctions even at room temperature because of the use of highly spin injection and detection techniques [22]. Asymmetric bias-current dependence of the spin signals is evidently found, which originates from the spin injection via BTBT through p-n junctions or the spin extraction via localized states near p-n junctions. Even for the use of a 7-nm-thick p-Ge layer at the spin injector and detector, we find clear spin-transport properties at room temperature. This study will open a path for designing spin-TFET structures with a Ge p-n junction at room temperature.

To demonstrate spin transport through BTBT at Ge p-n junctions, we grew CFAS/p-Ge/n-Ge/Ge-buffer layer/Si(111) heterostructures. The schematic of the heterostructure is shown in Fig. 1(a). In the following, we explain the growth procedure and fabricated LSV devices. Using molecular beam epitaxy (MBE), we first formed an undoped Ge(111) layer (approximately 40 nm) grown at 350 °C [low-temperature (LT) Ge layer] on an undoped Si(111) substrate ($\rho \sim 1000$ Ωcm) and then formed an undoped Ge(111) layer (approximately 500 nm) grown at 700 °C [high-temperature (HT) Ge layer] [38,39]. Then, we grew a 140-nm-thick P-doped n-Ge layer with a concentration of approximately 10^{19} cm^{-3} by MBE at 350 °C on the HT Ge layer. Subsequently, we grew a 7-nm-thick gallium (Ga)-doped p-Ge layer with a concentration of approximately 10^{19} cm^{-3} by MBE at 350 °C on the n-Ge layer. Here, to promote BTBT at the p-n junction, we grew a P δ-doped Ge layer with an ultrathin Si layer on the bottom of the p-Ge layer [20], as described by the red dashed line shown at the bottom of the p-Ge layer [Fig. 1(a)]. Finally, as a spin injector and detector, we grew a CFAS layer, which is a highly spin-polarized Heusler alloy [22,40–43] on the p-Ge layer. Here, a 0.7-nm-thick Fe layer was inserted between the CFAS layer and the p-Ge layer to suppress the interdiffusion between Co and Ge and to obtain large spin signals [18,19,44].

After the film growth, we measured the magnetization curves of the CFAS layer by using a vibrating sample magnetometer. The saturation magnetization of the CFAS layer was estimated to be approximately 1000 emu/cm^3, close to that of our previous report [17]. Finally, we fabricated LSV devices [2,45–47], as shown in Fig. 1(b), using electron-beam lithography and Ar ion milling. Details and top views of similar LSV devices have been reported

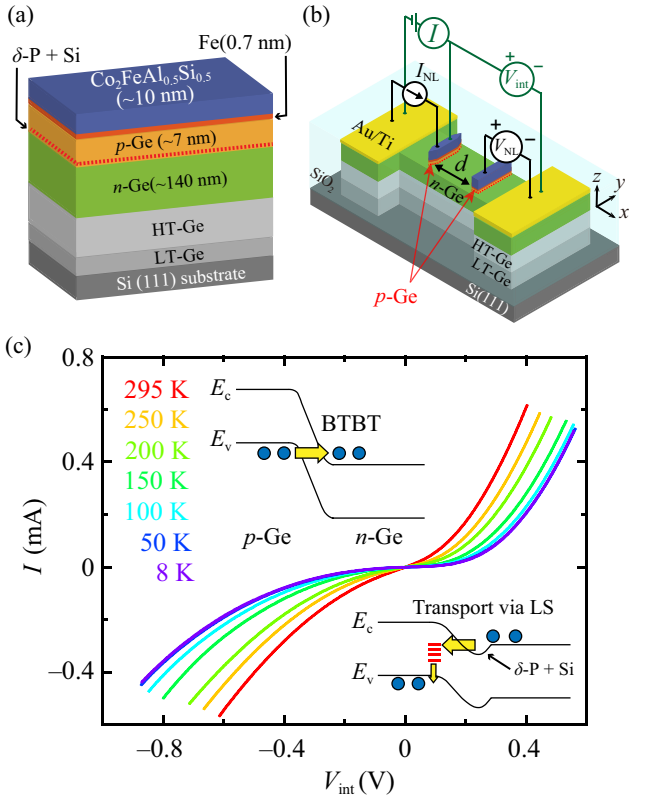

FIG. 1. Schematics of (a) a grown $Co_2FeAl_{0.5}Si_{0.5}$/p-Ge/n-Ge/Ge-buffer/Si(111) heterostructure and (b) a fabricated lateral spin-valve (LSV) device with the Ge p-n junctions. The black and green terminal configurations represent the four-terminal and three-terminal nonlocal voltage measurements, respectively. (c) $I - V_{\rm int}$ characteristics recorded by the three-terminal nonlocal voltage measurement at various temperatures. The insets show possible band diagrams in $V_{\rm int} < 0$ (left) and $V_{\rm int} > 0$ (right).

elsewhere [11,48]. As needed, we varied the edge-to-edge distance (d) between the spin injector and the detector, and the size of the spin injector (detector) contact is 0.4 × 5.0 μm^2 (1.0 × 5.0 μm^2). Finally, to obtain the value of carrier concentration in the n-Ge layer, we also fabricated Hall-bar devices next to the LSV devices on the same heterostructure. As a result, the carrier concentration at room temperature is estimated to be $2.0 \sim 3.0 \times 10^{18}$ cm^{-3}.

First, we perform current (I)− voltage characteristic measurements in an LSV device to confirm BTBT through the Ge p-n junction. Figure 1(c) shows $I - V_{\rm int}$ characteristics from 8 to 295 K, measured by a three-terminal method shown in Fig. 1(b), where $V_{\rm int}$ means the voltage applied to the interface consisting of the CFAS/p-Ge/n-Ge junction [48,49]. In $V_{\rm int} > 0$ (forward-bias conditions), conventional features of forward-bias currents through the p-n junction are observed from 8 to 295 K. For analyzing the $I - V_{\rm int}$ features in $V_{\rm int} > 0$, we fit the data at 295 K using $I = I_0\{\exp(qV_{\rm int}/nkT) - 1\}$ in $V_{\rm int} > kT/q$, where I_0 is the saturation current, n is ideality factor, q is the elementary charge, k is the Boltzmann constant, and T is

the absolute temperature. As a result, the value of n can be obtained to be $1.3 \sim 1.8$ in $0.006\ \mathrm{V} < V_{\mathrm{int}} < 0.018\ \mathrm{V}$ at 295 K. In general, the n value between 1 and 2 is caused by the recombination of carriers at the localized states in p-n junction [50,51]. Therefore, we consider that a possible model of the forward currents through the p-n junction is illustrated in the right inset schematic in Fig. 1(c). In $V_{\mathrm{int}} < 0$ (reverse-bias conditions), on the other hand, we can see no strong rectifying behavior and clear tunnel conductions even for the reverse bias at the p-n junction. Note that almost the same features were detected even though the terminal configuration was switched. Since we have intentionally used a P δ-doped Ge layer at the pn junction, the quantum-mechanical BTBT is easily observed even in a small negative V_{int}. The feature in $V_{\mathrm{int}} < 0$ means the BTBT through the Ge p-n junction prepared here, as shown in the left inset schematic in Fig. 1(c). Although this is a demonstration of an ON state (normally ON) via BTBT in a TFET structure, we can explore the spin injection and detection properties in the LSV devices with the Ge p-n junctions using the CFAS/p-Ge/n-Ge junctions as a spin injector and a detector.

Figure 2(a) shows a representative nonlocal spin signal [$\Delta R_{\mathrm{NL}} = \Delta V_{\mathrm{NL}}/I_{\mathrm{NL}} = (V_{\mathrm{NL}}^{\uparrow\downarrow} - V_{\mathrm{NL}}^{\uparrow\uparrow})/I_{\mathrm{NL}}$] as a function of in-plane magnetic fields (B_y) at 297 K. Here, these signals were recorded in $I_{\mathrm{NL}} < 0$, indicating that the spin-polarized electrons are injected into the n-Ge from the CFAS/p-Ge contact via BTBT. By sweeping B_y [Fig. 2(a)], hysteretic behavior depending on the magnetization switching between the parallel and antiparallel states is clearly observed at 297 K. In these measurements, we did not detect the enhancement in R_{NL} in the high magnetic fields, observed in metallic spin-valve devices with some influences of the ferromagnetic impurities [52,53]. Temperature dependence of magnitude of ΔR_{NL} ($|\Delta R_{\mathrm{NL}}|$) is also shown in Fig. 2(b). Monotonic increase in $|\Delta R_{\mathrm{NL}}|$ is seen with decreasing temperature, indicating the absence of the impurity-induced reduction in $|\Delta R_{\mathrm{NL}}|$ in these measurements [53,54].

Also, by sweeping out-of-plane magnetic fields (B_z) [Fig. 2(c)], Hanle precession signals are clearly observed in both the parallel and antiparallel magnetization states of CFAS electrodes at room temperature. Here, in Hanle curve measurements, background curves originating from magnetoresistance effect and Hall effect in semiconductor channels are superimposed. In Fig. 2(c), the influence of the Hall effect was subtracted from the raw data for clarity [2,11]. Therefore, we did not conduct the detailed analyses with these Hanle curves. In any case, we note that these data mean that the spin transport through the pn junctions in the Ge-based LSV device is evidently observed at 297 K. Because the previous reports regarding the spin transport through the BTBT were limited to the low-temperature observation [34–37], the present results with room-temperature spin transport

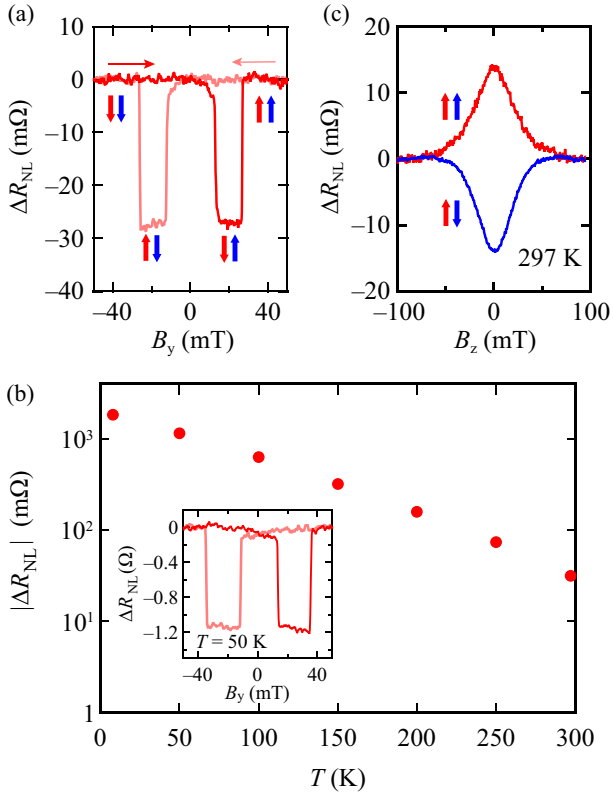

FIG. 2. (a) Nonlocal spin signals and (c) Hanle-effect curves measured at 297 K for an LSV device with $d = 0.5$ μm. (b) Temperature dependence of $|\Delta R_{\mathrm{NL}}|$. The inset shows a nonlocal spin signal at 50 K. For these measurements, the injection current I_{NL} of −0.1 mA is applied, inducing a BTBT condition.

are significant progress that can pave the way to demonstrate a spin TFET with room-temperature operation.

To further explore the spin injection and detection through the p-n junctions at room temperature, we investigate the bias-current (I_{NL}) dependence of $|\Delta V_{\mathrm{NL}}|$ (and $|\Delta R_{\mathrm{NL}}|$) in Fig. 3(a) (and in the inset) for an LSV device with $d = 1.0$ μm. When $I_{\mathrm{NL}} < 0$, the $|\Delta V_{\mathrm{NL}}|$ is enhanced linearly within $I_{\mathrm{NL}} = -0.3$ mA, meaning that spin accumulation in the n-Ge spin-transport channel is linearly increased. As illustrated in the left band diagram of Fig. 3(b), the spin injection through BTBT occurs to create the spin accumulation in n-Ge [35,36]. Here, a very small Schottky barrier height due to the strong Fermi-level pinning should be considered at the metal/p-Ge [55–57]. With decreasing I_{NL} (with increasing $|I_{\mathrm{NL}}|$ in $I_{\mathrm{NL}} < 0$), the spin accumulation created in n-Ge is efficiently increased. In this situation, the $|\Delta R_{\mathrm{NL}}|$ is also enhanced around $I_{\mathrm{NL}} = -0.2$ mA, and then, the ΔR_{NL} is decreased in $I_{\mathrm{NL}} < -0.2$ mA, giving rise to the influence of the Joule heating. When $I_{\mathrm{NL}} > 0$, on the other hand, the $|\Delta R_{\mathrm{NL}}|$ is decreased monotonically with increasing I_{NL}. This feature is inconsistent with the conventional spin extraction from semiconductor channels, discussed in the literature [58–62]. At this stage, we consider that the condition of

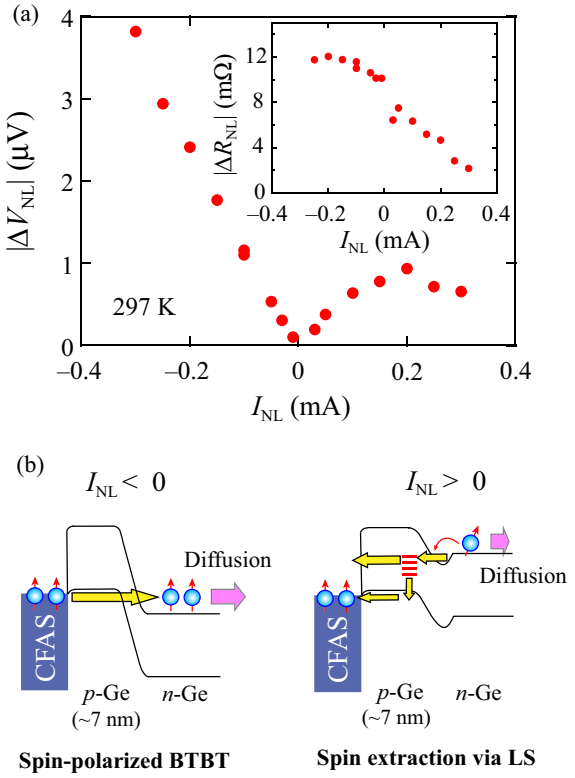

FIG. 3. (a) Bias-current (I_{NL}) dependence of $|\Delta V_{NL}|$ for the LSV with $d = 1.0$ μm at room temperature. The inset shows its I_{NL} dependence of $|\Delta R_{NL}|$. (b) Possible band diagrams of the spin injection via BTBT (left) and of the spin extraction via localized states (right) at a Ge p-n junction.

$I_{NL} > 0$ enables the creation of the spin accumulation in n-Ge via the spin extraction from the p-Ge or localized states (LS) in the p-n junction, as depicted in the right of Fig. 3(b). The details are discussed in the next paragraph.

Due to the strong influence of the spin-orbit interaction in the valence bands [1,63], it is generally difficult to observe hole spin transport at room temperature. Several reports on spin transport in p-Ge at room temperature have been published, including three-terminal Hanle measurements in lateral devices [64,65] or detection of spin transport in vertical spin-valve structures [66,67]. Since the present study uses an LSV device structure with a long spin transport layer of n-Ge, the decrease in the spin-generation efficiency due to the spin relaxation phenomena in p-Ge can affect the total value of ΔR_{NL} in the LSV devices in $I_{NL} > 0$. Furthermore, the LS in the p-n junction can also influence the spin transport and spin relaxation in the semiconductor devices, as previously argued in the literature [68]. Therefore, the presence of the spin extraction from the p-Ge or localized states in the p-n junction is a possible mechanism of the creation of the small spin accumulation in n-Ge in the present LSV devices in $I_{NL} > 0$.

We finally examine the spin-diffusion phenomena at room temperature after the spin injection in $I_{NL} < 0$.

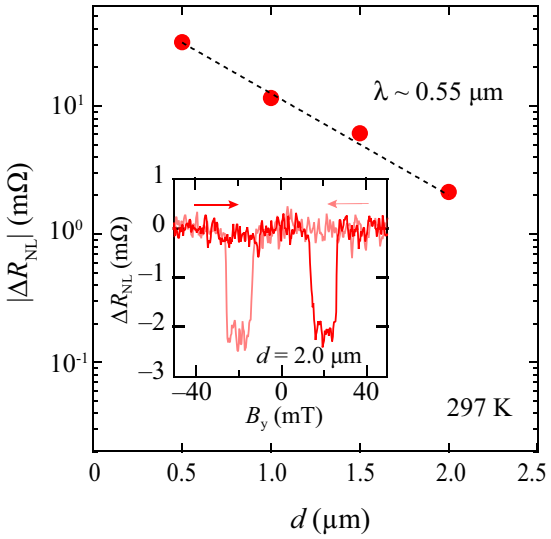

FIG. 4. The d dependence of $|\Delta R_{NL}|$ at room temperature for LSV devices with Ge p-n junctions. The linear fit to the data using Eq. (1) is represented as a dashed line. The inset shows a representative nonlocal spin signal for the LSV with $d = 2.0$ μm at room temperature.

Unlike the conventional spin injection and detection at the CFAS/n^+-Ge contact in our previous works [11,17,22,23], the LSV devices in this study have the p-n junctions at the contacts. As discussed in the previous paragraph, the p-n junction at the spin-injection side acts effectively as a tunnel barrier with BTBT. After the spin injection via BTBT, the spins can transfer in the n-Ge layer, and then reaches at the another p-Ge layer at the contact. Therefore, we should consider the spin transport in the n-Ge and p-Ge layers at room temperature. Figure 4 shows a d dependence of ΔR_{NL} at room temperature. Even for the LSV devices with p-n junctions, clear d dependence with exponentially decaying ΔR_{NL} is observed. The value of $|\Delta R_{NL}|$ in LSV devices with sufficiently large contact resistance can roughly be expressed by the equation [2,45–47],

$$|\Delta R_{NL}| = P^2 \frac{\rho\lambda}{S} \exp(-d/\lambda), \tag{1}$$

where P is the average of the spin-injection and detection efficiency, λ, S (approximately 0.98 μm^2), and ρ (approximately 3.5 mΩ cm) are the spin-diffusion length, the cross-section area, and the resistivity of the semiconductor channel, respectively. The λ value can be estimated by fitting the decay of $|\Delta R_{NL}|$, as shown in the dashed curve of Fig. 4. From these analyses, the λ in the present devices is estimated to be approximately 0.55 μm, roughly consistent with λ for n-Ge with a carrier concentration of 1.0×10^{18} cm^{-3} [69]. Also, the value of $P \sim 0.06$ is also obtained at room temperature. Here we roughly compare the value of P (approximately 0.06) at room temperature with those in other works. In the case of SC-based LSV devices without insulator tunnel barriers and with Heusler

alloys, there are some reports on higher values of P, 0.14 for CFAS/n-Ge, [18], 0.13 for Co_2MnSi/n-Ge, [19] 0.24 for CFAS/n-GaN, [70]. For Co_2FeSi/n-GaAs, however, the value of P is less than 0.01 at 300 K [71]. Considering these results, we judge that the spin injection and detection via p-n junctions is relatively useful above room temperature. Since LSV devices with p-n junctions have a relatively high contact resistance ($RA \sim 2\,\mathrm{k\Omega}\,\mu\mathrm{cm}^2$) unfortunately compared to those with Schottky tunnel junctions ($RA \leq 1\,\mathrm{k\Omega}\,\mu\mathrm{cm}^2$), it is a disadvantage with respect to the two-terminal magnetoresistance effect [18,72]. The actual value of the two-terminal magnetoresistance ratio at room temperature was limited to approximately 0.002% (not shown here), slightly larger than those in Ref. [72] but one order of magnitude smaller than those in Ref. [18]. Due to it being out of scope to explore this in detail in this paper, we will further explore the two-terminal magnetoresistance effect in the future. In addition to these, we find that although there is an approximately 7-nm-thick p-Ge relevant to the spin transport in the LSV devices, its influence on the room-temperature spin transport is weak. We understand that the thickness of the p-Ge layer in the LSV devices is thinner than the room-temperature spin-diffusion length of p-Ge(8.4 nm $\sim$ 30 nm) reported [63,67]. On the basis of the above experiments, we evidently see that spin-injection condition ($I_{\mathrm{NL}} < 0$) and a thin p-Ge layer at the p-n junction can be used for room-temperature spin transport in a device for spin-based tunnel field-effect transistors.

In summary, to integrate spintronic technologies into a tunnel field-effect transistor, we have explored electrical spin injection, transport, and detection at room temperature through BTBT at a semiconductor p-n junction. We experimentally observed pure spin-current transport through BTBT at p-n junctions using n-Ge based lateral spin-valve devices even at room temperature. Asymmetric bias-current dependence of the spin signals was evidently found, originating from the spin injection via BTBT or the spin extraction via LS at p-n junctions. Notably, even for the use of a thin p-type semiconductor at the spin injector and detector, we found clear spin-transport properties at room temperature. This study will open a path for the room-temperature operation of a spin-based tunnel field-effect transistor with a p-n junction.

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[1] I. Žutić, J. Fabian, and S. Das Sarma, Rev. Mod. Phys. **76**, 323 (2004).
[2] X. Lou, C. Adelmann, S. A. Crooker, E. S. Garlid, J. Zhang, K. S. M. Reddy, S. D. Flexner, C. J. Palmstrøm, and P. A. Crowell, Nat. Phys. **3**, 197 (2007).
[3] M. Tanaka and S. Sugahara, IEEE Trans. Electron Devices **54**, 961 (2007).
[4] S. Lee, H. Koike, M. Goto, S. Miwa, Y. Suzuki, N. Yamashita, R. Ohshima, E. Shigematsu, Y. Ando, and M. Shiraishi, Nat. Mater. **20**, 1228 (2021).
[5] M. Ciorga, J. Phys. D Appl. Phys. **58**, 012001 (2025).
[6] N. Tombros, C. Jozsa, M. Popinciuc, H. T. Jonkman, and B. J. van Wees, Nature **448**, 571 (2007).
[7] W. Han, R. K. Kawakami, M. Gmitra, and J. Fabian, Nat. Nanotechnol. **9**, 794 (2014).
[8] A. Spiesser, H. Saito, Y. Fujita, S. Yamada, K. Hamaya, S. Yuasa, and R. Jansen, Phys. Rev. Appl. **8**, 064023 (2017).
[9] T. Suzuki, T. Sasaki, T. Oikawa, M. Shiraishi, Y. Suzuki, and K. Noguchi, Appl. Phys. Express **4**, 023003 (2011).
[10] M. Yamada, M. Tsukahara, Y. Fujita, T. Naito, S. Yamada, K. Sawano, and K. Hamaya, Appl. Phys. Express **10**, 093001 (2017).
[11] K. Hamaya, Y. Fujita, M. Yamada, M. Kawano, S. Yamada, and K. Sawano, J. Phys. D Appl. Phys. **51**, 393001 (2018).
[12] A. Toriumi and T. Nishimura, Jpn. J. Appl. Phys. **57**, 010101 (2018).
[13] C. Zucchetti, F. Bottegoni, C. Vergnaud, F. Ciccacci, G. Isella, L. Ghirardini, M. Celebrano, F. Rortais, A. Ferrari, A. Marty, M. Finazzi, and M. Jamet, Phys. Rev. B **96**, 014403 (2017).
[14] S. De Cesari, R. Bergamaschini, E. Vitiello, A. Giorgioni, and F. Pezzoli, Sci. Rep. **8**, 11119 (2018).
[15] H. Watzinger, J. Kukučka, L. Vukušić, F. Gao, T. Wang, F. Schäffler, J.-J. Zhang, and G. Katsaros, Nat. Commun. **9**, 3902 (2018).
[16] F. N. M. Froning, L. C. Camenzind, O. A. H. van der Molen, A. Li, E. P. A. M. Bakkers, D. M. Zumbühl, and F. R. Braakman, Nat. Nanotechnol. **16**, 308 (2021).
[17] Y. Fujita, M. Yamada, M. Tsukahara, T. Oka, S. Yamada, T. Kanashima, K. Sawano, and K. Hamaya, Phys. Rev. Appl. **8**, 014007 (2017).
[18] M. Yamada, F. Kuroda, M. Tsukahara, S. Yamada, T. Fukushima, K. Sawano, T. Oguchi, and K. Hamaya, NPG Asia Mater. **12**, 47 (2020).
[19] K. Kudo, M. Yamada, S. Honda, Y. Wagatsuma, S. Yamada, K. Sawano, and K. Hamaya, Appl. Phys. Lett. **118**, 162404 (2021).
[20] M. Yamada, K. Sawano, M. Uematsu, and K. M. Itoh, Appl. Phys. Lett. **107**, 132101 (2015).
[21] M. Yamada, Y. Fujita, S. Yamada, T. Kanashima, K. Sawano, and K. Hamaya, Mater. Sci. Semicond. Process. **70**, 83 (2017).
[22] K. Hamaya and M. Yamada, MRS Bull. **47**, 584 (2022).
[23] T. Naito, M. Yamada, S. Yamada, K. Sawano, and K. Hamaya, Phys. Rev. Appl. **13**, 054025 (2020).
[24] Y. Fujita, M. Yamada, Y. Nagatomi, K. Yamamoto, S. Yamada, K. Sawano, T. Kanashima, H. Nakashima, and K. Hamaya, Jpn. J. Appl. Phys. **55**, 063001 (2016).
[25] K. Yamamoto, T. Matsuo, M. Yamada, Y. Wagatsuma, K. Sawano, and K. Hamaya, Mater. Sci. Semicond. Process. **167**, 107763 (2023).
[26] S. Sato, M. Tanaka, and R. Nakane, Phys. Rev. B **102**, 035305 (2020).

[27] K. Boucart and A. M. Ionescu, Solid-State Electron. **52**, 1318 (2008).
[28] T. Krishnamohan, D. Kim, S. Raghunathan, and K. C. Saraswat, IEDM Tech. Dig., 947 (2008).
[29] S. H. Kim, S. Agarwal, Z. A. Jacobson, P. Matheu, C. Hu, and T.-J. K. Liu, IEEE Electron Device Lett. **31**, 1107 (2010).
[30] K. H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Soree, G. Groeseneken, and K. D. Meyer, IEEE Trans. Electron Devices **59**, 292 (2012).
[31] A. M. Ionescu and H. Riel, Nature **479**, 329 (2011).
[32] K. Tomioka, M. Yoshimura, and T. Fukui, in *2012 Symposium on VLSI Technology (VLSIT)* (2012), p. 47.
[33] P. Jain, P. Rastogi, C. Yadav, A. Agarwal, and Y. S. Chauhan, J. Appl. Phys. **122**, 014502 (2017).
[34] M. Kohda, Y. Ohno, K. Takamura, F. Matsukura, and H. Ohno, Jpn. J. Appl. Phys. **40**, L1274 (2001).
[35] M. Oltscher, M. Ciorga, M. Utz, D. Schuh, D. Bougeard, and D. Weiss, Phys. Rev. Lett. **113**, 236602 (2014).
[36] M. Oltscher, F. Eberle, T. Kuczmik, A. Bayer, D. Schuh, D. Bougeard, M. Ciorga, and D. Weiss, Nat. Commun. **8**, 1807 (2017).
[37] N. Thanh Tu, T. Otsuka, Y. Arakawa, L. D. Anh, M. Tanaka, and P. N. Hai, J. Appl. Phys. **131**, 013902 (2022).
[38] K. Sawano, Y. Hoshi, S. Kubo, K. Arimoto, J. Yamanaka, K. Nakagawa, K. Hamaya, M. Miyao, and Y. Shiraki, Thin Solid Films **613**, 24 (2016).
[39] H.-C. Luan, D. R. Lim, K. K. Lee, K. M. Chen, J. G. Sandland, K. Wada, and L. C. Kimerling, Appl. Phys. Lett. **75**, 2909 (1999).
[40] R. Shan, H. Sukegawa, W. H. Wang, M. Kodzuka, T. Furubayashi, T. Ohkubo, S. Mitani, K. Inomata, and K. Hono, Phys. Rev. Lett. **102**, 246601 (2009).
[41] R. Farshchi and M. Ramsteiner, J. Appl. Phys. **113**, 191101 (2013).
[42] S. Yamada, M. Kato, S. Ichikawa, M. Yamada, T. Naito, Y. Fujiwara, and K. Hamaya, Adv. Electron. Mater. **9**, 2300045 (2023).
[43] Z. Nedelkoski, B. Kuerbanjiang, S. E. Glover, A. M. Sanchez, D. Kepaptsoglou, A. Ghasemi, C. W. Burrows, S. Yamada, K. Hamaya, Q. M. Ramasse, P. J. Hasnip, T. Hase, G. R. Bell, A. Hirohata, and V. K. Lazarov, Sci. Rep. **6**, 37282 (2016).
[44] T. Naito, R. Nishimura, M. Yamada, A. Masago, Y. Shiratsuchi, Y. Wagatsuma, K. Sawano, R. Nakatani, T. Oguchi, and K. Hamaya, Phys. Rev. B **105**, 195308 (2022).
[45] F. J. Jedema, H. B. Heersche, A. T. Filip, J. J. A. Baselmans, and B. J. van Wees, Nature **416**, 713 (2002).
[46] F. J. Jedema, N. S. Nijboer, A. T. Filip, and B. J. van Wees, Phys. Rev. B **67**, 085319 (2003).
[47] T. Kimura and Y. Otani, J. Phys. Condens. Matter. **19**, 165216 (2007).
[48] Y. Fujita, M. Yamada, M. Tsukahara, T. Naito, S. Yamada, K. Sawano, and K. Hamaya, Phys. Rev. B **100**, 024431 (2019).
[49] M. Honda, T. Shiihara, M. Yamada, S. Yamada, and K. Hamaya, Mater. Sci. Semicond. Process. **116**, 105066 (2020).
[50] S. T. Le, P. Jannaty, A. Zaslavsky, S. A. Dayeh, and S. T. Picraux, Appl. Phys. Lett. **96**, 262102 (2010).
[51] G. Thareja, S. L. Cheng, T. Kamins, K. Saraswat, and Y. Nishi, IEEE Electron Device Lett. **32**, 608 (2011).
[52] G. Mihajlović, S. I. Erlingsson, K. Výborný, J. E. Pearson, S. D. Bader, and A. Hoffmann, Phys. Rev. B **184**, 132407 (2011).
[53] A. J. Wright, M. J. Erickson, D. Bromley, P. A. Crowell, C. Leighton, and L. O'Brien, Phys. Rev. B **104**, 014423 (2021).
[54] K. Hamaya, T. Kurokawa, S. Oki, S. Yamada, T. Kanashima, and T. Taniyama, Phys. Rev. B **94**, 140401(R) (2016).
[55] A. Dimoulas, P. Tsipas, A. Sotiropoulos, and E. K. Evangelou, Appl. Phys. Lett. **89**, 252110 (2006).
[56] T. Nishimura, K. Kita, and A. Toriumi, Appl. Phys. Lett. **91**, 123123 (2007).
[57] K. Yamane, K. Hamaya, Y. Ando, Y. Enomoto, K. Yamamoto, T. Sadoh, and M. Miyao, Appl. Phys. Lett. **96**, 162104 (2010).
[58] S. A. Crooker, M. Furis, X. Lou, C. Adelmann, D. L. Smith, C. J. Palmstrøm, and P. A. Crowell, Science **309**, 2191 (2005).
[59] X. Lou, C. Adelmann, M. Furis, S. A. Crooker, C. J. Palmstrøm, and P. A. Crowell, Phys. Rev. Lett. **96**, 176603 (2006).
[60] H. Dery and L. J. Sham, Phys. Rev. Lett. **98**, 046602 (2007).
[61] K. Kasahara, Y. Baba, K. Yamane, Y. Ando, S. Yamada, Y. Hoshi, K. Sawano, M. Miyao, and K. Hamaya, J. Appl. Phys. **111**, 07C503 (2012).
[62] R. Jansen, A. Spiesser, H. Saito, Y. Fujita, S. Yamada, K. Hamaya, and S. Yuasa, Phys. Rev. Appl. **10**, 064050 (2018).
[63] C. Lange, G. Isella, D. Chrastina, F. Pezzoli, N. S. Köster, R. Woscholski, and S. Chatterjee, Phys. Rev. B **85**, 241303(R) (2012).
[64] S. Iba, H. Saito, A. Spiesser, S. Watanabe, R. Jansen, S. Yuasa, and K. Ando, Appl. Phys. Express **5**, 053004 (2012).
[65] F. Rortais, S. Oyarzún, F. Bottegoni, J. C. Rojas-Sánchez, P. Laczkowski, A. Ferrari, C. Vergnaud, C. Ducruet, C. Beigné, N. Reyren, A. Marty, J. P. Attané, L. Vila, S. Gambarelli, J. Widiez, F. Ciccacci, H. Jaffrès, J. M. George, and M. Jamet, J. Phys: Condens. Matter **28**, 165801 (2016).
[66] M. Kawano, M. Ikawa, K. Santo, S. Sakai, H. Sato, S. Yamada, and K. Hamaya, Phys. Rev. Mater. **1**, 034604 (2017).
[67] A. Yamada, M. Yamada, T. Shiihara, M. Ikawa, S. Yamada, and K. Hamaya, J. Appl. Phys. **129**, 013901 (2021).
[68] M. Tran, H. Jaffrès, C. Deranlot, J. M. George, A. Fert, A. Miard, and A. Lemaître, Phys. Rev. Lett. **102**, 036601 (2009).
[69] T. Naito, M. Yamada, Y. Wagatsuma, K. Sawano, and K. Hamaya, Phys. Rev. Appl. **18**, 024005 (2022).
[70] S. Yamada, M. Kato, S. Ichikawa, M. Yamada, T. Naito, Y. Fujiwara, and K. Hamaya, Adv. Electron. Mater. **9**, 2300045-1 (2023).
[71] T. A. Peterson, S. J. Patel, C. C. Geppert, K. D. Christie, A. Rath, D. Pennachio, M. E. Flatté, P. M. Voyles, C. J. Palmstrøm, and P. A. Crowell, Phys. Rev. B **94**, 235309 (2016).
[72] M. Tsukahara, M. Yamada, T. Naito, S. Yamada, K. Sawano, V. K. Lazarov, and K. Hamaya, Appl. Phys. Express **12**, 033002 (2019).