Technical Note—Slowdown in the Energy Efficiency of Analog-to-Digital Converters and a Compressed-Sensing-Based Solution

Daisuke Kanemoto
The University of Osaka
Email: dkanemoto@ieee.org; dkanemoto@eei.eng.osaka-u.ac.jp

***Abstract*—Power consumption remains a critical bottleneck in the design of sensor systems. To investigate power consumption problems in sensor circuits, we surveyed the latest developments in analog-to-digital converter (ADC) integrated circuits, which are indispensable components of sensor front ends. An evaluation based on the Walden figure-of-merit, using data from ADCs presented at the International Solid-State Circuits Conference, revealed a slowdown in the energy-efficiency improvement of state-of-the-art ADCs. To overcome this limitation, we are developing a compressed-sensing (CS)-based solution: a low-power sensing approach that combines random undersampling with CS reconstruction. A prototype wireless electroencephalogram system implemented on a general-purpose microcontroller reduces both sampling activity and radio duty cycle, achieving continuous operation at 72 μW while maintaining signal fidelity. These efforts are expected to pave the way for next-generation ultralow-power and energy-harvesting sensor networks.**

***Index Terms*—Analog-to-digital converter (ADC), compressed sensing (CS), energy efficiency, figure-of-merit (FoM)**

I. Introduction

The rapid expansion of the Internet of Things and digital transformation is driving the widespread deployment of wireless sensor systems that collect and transmit data to clouds or edge computers. Such sensor systems are now being applied to a wide range of fields. Examples include healthcare [1] and BrainTech [2], structural health monitoring [3] of roads, bridges, and buildings, fault detection [4] in industrial equipment, and early warning of natural disasters [5], all of which will be critical for sustaining modern society. However, every sensor requires a power source, and many rely on batteries or, ideally, energy harvesters that scavenge the ambient energy. In battery-powered sensor networks, increasing the number of sensors leads to higher costs for battery replacement and maintenance. Although energy harvesters offer a potential solution to these challenges, the energy they can provide is fundamentally constrained.

A fundamental solution is to reduce the power consumption of the sensor circuitry. Ultralow-power operation contributes not only to battery life and maintenance cost reduction, but also to the development of fully battery-free systems that operate solely with harvested energy. Achieving such an efficiency requires fundamental technological innovation across the entire sensing chain, from the analog front-end to the wireless transceiver.

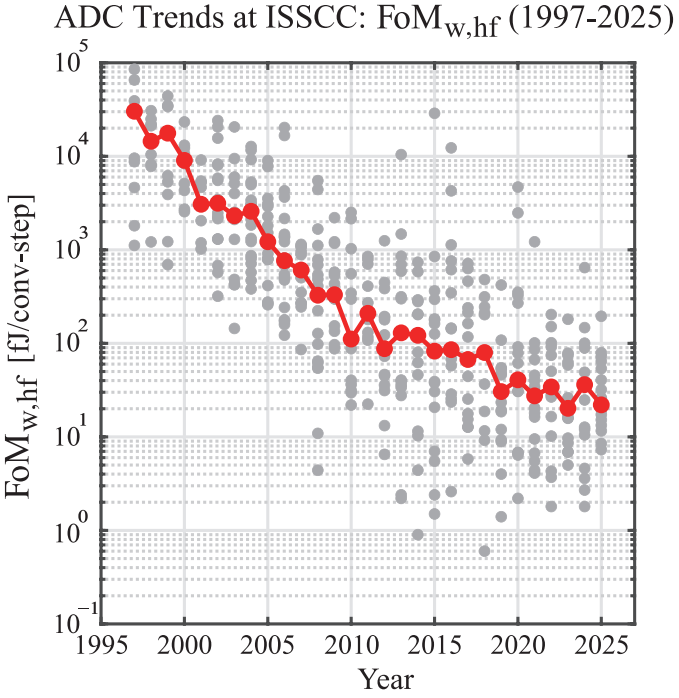

Fig. 1. Recent $\mathrm{FoM_{w,hf}}$ trend of state-of-the-art ADCs reported in ISSCC (1997–2025). The red circles indicate the yearly medians. The plot shows a steady year-on-year improvement up to roughly 2010. Between 2010 and 2020 the rate of improvement slows noticeably, and from 2020 onward the median $\mathrm{FoM_{w,hf}}$ appears to exhibit a pronounced slowdown.

This technical note briefly reviews the evolution of energy-efficiency improvements in analog-to-digital converters (ADCs), which are key circuits in analog front ends and represent one of the major bottlenecks in many sensing applications. It then introduces a novel sampling strategy, developed by the authors, that enables low-power sensing under severe energy constraints.

II. FoM Trend Analysis

An ADC is a core building block of any sensing system that translates analog sensor outputs into digital data for subsequent processing. Since an ADC handles both the analog and digital domains and often integrates circuitry from both, it serves as a useful proxy for analyzing broader trends in sensor-oriented integrated circuit designs.

Multiple ADC architectures are available, including the flash, successive-approximation register, and delta–sigma types. Their performance is typically analyzed in terms of power consumption P, effective number of bits (ENOB), and signal bandwidth BW. These parameters are interdependent and present inherent trade-offs for power efficiency.

Figure-of-merit (FoM) metrics are widely used to compare the energy efficiency across designs. Two well-known examples are the FoM proposed by Richard Schreier, denoted $\mathrm{FoM_s}$, and that proposed by Richard H. Walden, denoted $\mathrm{FoM_w}$. Because either metric leads to a similar conclusion in this technical note, we adopt $\mathrm{FoM_w}$ for our analysis, which is defined as

$$\mathrm{FoM_w} = \frac{P}{2^{\mathrm{ENOB}} \cdot 2\,BW}. \tag{1}$$

Because the ENOB depends on the input signal frequency, we adopt $\mathrm{FoM_{w,hf}}$, calculated based on the ENOB measured with a high-frequency sinusoidal input, for our analysis.

Figure 1 shows a graph based on a comprehensive table compiled by Prof. Boris Murmann [6], which summarizes $\mathrm{FoM_{w,hf}}$ data for ADCs presented at the International Solid-State Circuits Conference (ISSCC). Each gray dot represents the $\mathrm{FoM_{w,hf}}$ of an ADC reported in a given year, whereas the red circles denote the yearly medians, which are connected by a solid line to clarify the overall trend. The plot presents a steady year-on-year improvement up to approximately 2010. Between 2010 and 2020, the rate of improvement slowed down noticeably, and from 2020 onward, the improvement in the median $\mathrm{FoM_{w,hf}}$ showed signs of saturation. A possible reason for this slowdown is that further progress in analog circuitry is constrained by physical factors, such as thermal noise, jitter, and low supply voltages (for example, [7], [8]).

Uniform sampling, grounded in the sampling theorem, enables perfect signal reconstruction; therefore, it is regarded as a fundamental and universal approach. For applications requiring exact signal reconstruction, sampling based on the Nyquist criterion [9] is essential. However, in cases where a slight performance degradation is acceptable, alternative sampling strategies may be explored to achieve significant reductions in power consumption.

Given the pronounced slowdown in conventional circuit-level improvements, architecture-level innovation is required to continue enhancing energy efficiency. To address this, we are developing a compressed-sensing (CS)-based solution: a low-power sensing system that enables data acquisition with inherent compression and represents one of the promising approaches for next-generation energy-efficient sensing.

III. Energy-Efficient Sensing Systems Based on a CS Approach

Figure 2(a) depicts the sampling behavior and power consumption of a conventional uniform-sampling sensing system. In this system, data are sampled periodically at intervals of T_s, and each sampling action consumes a specific amount of energy. When a predetermined amount of data has been collected, it is transmitted through a wireless transceiver that consumes a significant amount of power. As described in the previous section, low-power circuit design is an effective approach to decrease the power consumption in such systems. However, because significant progress has already been made in energy-efficient integrated circuit designs, achieving further substantial reductions in circuit-level power consumption has become increasingly difficult.

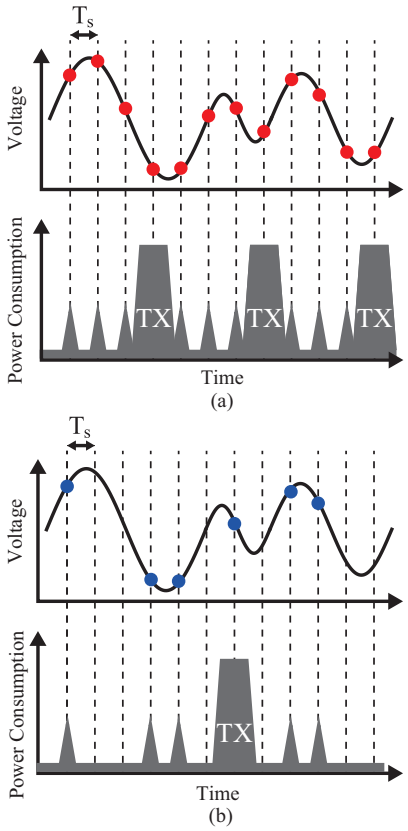

Fig. 2. Relationship between signal sampling (top) and power consumption (bottom). (a) shows conventional uniform sampling, and (b) shows random undersampling. "TX" denotes wireless transmission. Random undersampling reduces the number of activations of sampling circuits and decreases the frequency of wireless transmissions, thereby lowering overall power consumption.

To address this limitation, we propose a different approach: by employing random undersampling, the number of sampling operations can be reduced, thereby decreasing the volume of the acquired data (Fig. 2(b)). Consequently, the frequency of wireless transmission can also be significantly reduced. Although this method generates compressed signal representations, the original waveform can be reconstructed by leveraging the inherent sparsity of the signal in an appropriate transform basis and solving a suitable optimization problem on edge devices, personal computers, and cloud servers, where power constraints are less critical.

First, we developed a proof-of-concept wireless electroencephalogram (EEG) transmitter that applied random undersampling on a general-purpose microcontroller (Nordic Semiconductor nRF52840), which includes the path from the ADC

to the Bluetooth Low Energy transceiver, and consumed 97 μW [10]. The use of a generic frequency-domain basis limited both the compression ratio and reconstruction accuracy; however, it reduced the power by 72% relative to uniform sampling. A miniature thermoelectric generator driven by a $2\,^{\circ}\mathrm{C}$-gradient powered the system continuously, demonstrating battery-free operation.

Next, to increase sparsity and enable higher compression, we previously demonstrated that basis learning on archived EEG signals significantly improves reconstruction accuracy [11]. More recently, we proposed a novel approach that constructs a basis by aligning similar waveforms obtained in the past, leveraging signal similarity rather than relying on traditional learning algorithms. This method achieves higher-fidelity reconstruction, even under high compression ratios [12]. Finally, we integrated this latter method into a second prototype with high compression based on the nRF52840, which operates at 72 μW with a normalized mean-squared error (NMSE) of 0.116 [13]. Despite achieving higher fidelity, it consumes less power than a custom ASIC-based wireless EEG transmitter [14], which operates at 90 μW.

We have also addressed artifacts that reduce sparsity and degrade CS accuracy. In particular, we have published several papers on exploiting the properties of random undersampling for mitigation schemes based on independent component analysis and outlier detection (for example, [15]–[17]). Our technique has also been applied to integrated circuit designs (for example, [18]–[21]). Furthermore, we have investigated the feasibility of leveraging the intrinsic randomness of random undersampling in lightweight cryptography [22].

Collectively, these efforts are part of an ongoing program to redefine sensing using CS. When perfect reconstruction is essential, uniform Nyquist rate sampling is required. In contrast, if a certain level of signal degradation is acceptable, the deliberate undersampling enabled by our proposed CS-based approach can yield significant power savings and enable new directions in signal-processing-driven sensing systems.

IV. Conclusion

This study quantified the recent slowdown in ADC power efficiency by analyzing $\mathrm{FoM}_{\mathrm{w,hf}}$ data reported at ISSCC. To address this challenge, we are currently investigating a CS-based solution, which combines random undersampling with CS reconstruction. Experimental prototypes built using a general-purpose microcontroller have demonstrated that this approach reduces both the sampling activity and further lowers the wireless transmission duty cycle of an EEG transmitter, thereby enabling operation at 72 μW while maintaining signal fidelity (NMSE = 0.116). Future work will focus on developing dedicated CS-based sensing chips and extending this approach to lightweight cryptographic sensor nodes. These efforts show a viable path toward the advancement of next-generation ultralow-power and energy-harvesting sensor networks.

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Daisuke Kanemoto (Member, IEEE) received the B.S. degree in Electronics and Information Science from Kyoto Institute of Technology, Kyoto, Japan in 2004 and the M.S. and Ph.D. degrees in Electronic Engineering from The University of Osaka, Osaka, Japan in 2006 and 2011, respectively. From 2010 to 2013, he was an Assistant Professor in the Department of Electronics, Graduate School of Information Science and Electrical Engineering, Kyushu University, Fukuoka, Japan. From 2013 to 2019, he was an Assistant Professor in the Department of Research, Interdisciplinary Graduate School of Medicine and Engineering, University of Yamanashi, Yamanashi, Japan. From 2015 to 2017, he was a Visiting Assistant Professor in the Department of Electrical Engineering, Stanford University, Stanford, CA, USA. Since 2019, he has been an Associate Professor in the Division of Electrical, Electronic and Information Engineering, Graduate School of Engineering, The University of Osaka, Osaka, Japan. His research interests include analog circuits, mixed-signal integrated circuits, signal processing (including compressed sensing and machine learning), and next-generation sensing systems through hardware/software co-design.

Dr. Kanemoto is also a member of the Institute of Electronics, Information and Communication Engineers (IEICE). He served as the Technical Program Committee Chair and Vice-Chair of the International Conference on Solid-State Devices and Materials from 2020 to 2022; an Associate Editor for the IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences from 2013 to 2017; and an Associate Editor for the IEICE Transactions on Fundamentals of Electronics from 2019 to 2022. He has been a Chapter Secretary for the IEEE Solid-State Circuits Society (SSCS) Kansai Chapter since 2023. He received the IEICE Young Researcher's Award in 2013.