Reduction of hole traps in GaN MOS structures by high-pressure oxygen annealing

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The impact of annealing pressure on hole traps in SiO_2/p-type GaN MOS structures was investigated. The density of fast-response interface hole traps (N_{hump}) was characterized from a hump in capacitance–voltage (C–V) characteristics of the MOS capacitors. N_{hump} was below 2×10^{12} cm^{-2} and was almost unchanged at 200–800°C when annealed under 100 MPa, while atmospheric-pressure annealing at a higher temperature led to a higher N_{hump}, exceeding 1×10^{13} cm^{-2} at 800°C. When samples first annealed at 800°C under atmospheric pressure were additionally annealed under 100 MPa, N_{hump} was reduced to about 2×10^{12} cm^{-2} regardless of the temperature of high-pressure annealing. Consequently, high-pressure oxygen annealing turned out to not only suppress the generation of interface hole traps but also reduce the traps once generated in GaN MOS structures.

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The wide bandgap, high critical electric field, and high saturation drift velocity make gallium nitride (GaN) uniquely suitable for high-power and high-frequency electronic devices[1–3]. By utilizing a high-density two-dimensional electron gas (2DEG) induced by piezoelectric and spontaneous polarization[4,5], GaN-based heterojunction field-effect transistors (HFETs) have been important building blocks for high-frequency switching devices[6]. Recently, high-performance GaN metal-oxide-semiconductor field-effect transistor (MOSFETs) with a vertical structure have been demonstrated that have a high channel mobility and a low on-state resistance[7–11].

The most fundamental components in these switching devices are MOS gate structures. The major requirement in fabricating MOS structures to improve the performance and reliability of devices is to reduce defects near a dielectric/semiconductor interface. In GaN MOS structures, low-density interface electron traps near the conduction band minimum (E_C) can be obtained[12–18]. On the other hand, the hole trap density near the valence band maximum (E_V) is very high[19–21], causing a serious reliability issue of threshold voltage instability during switching operation of GaN MOS devices[22,23]. Thus, a gate dielectric formation process that can achieve sufficiently low hole trap density is desirable based on a physical understanding of hole traps.

A unique hump and a large hysteresis were observed in capacitance–voltage (C–V) curves of silicon dioxide (SiO_2)/p-type GaN MOS capacitors[24–26], which results from hole trapping by fast-response interface defects and slow-response oxide traps, respectively[24,27]. The voltage range of the hump increased when post-deposition annealing (PDA) was performed at a higher temperature and/or the MOS structure had a thicker gallium oxide (GaO_x) interlayer[24–26] that is induced during the dielectric formation process[13,14]. This result indicates that defects thermally generated in the GaO_x interlayer in SiO_2/GaN structures are one of the major origins of the interface hole trap. Although these hole traps were challenging to sufficiently reduce only by controlling the conditions of gate dielectric formation process (deposition, annealing, etc.), no hump and a small hysteresis were obtained in GaN MOS structures fabricated on heavily magnesium (Mg)-doped epitaxial layers, achieving an exceptionally low hole trap density[28,29].

Recent theoretical studies have discussed the origin of hole traps in GaN MOS structures[30,31]. Among various types of defects, oxygen vacancy (V_O) in a GaO_x layer is regarded as a possible candidate because V_O acts as a deep donor in bulk gallium oxides[32–35]. A first-principles calculation showed that heavily doped Mg atoms can form a complex with V_O in GaO_x and passivate a hole trap[31], supporting the experimental result of reduced hole trap density in heavily Mg doped GaN MOS structures[28,29].

Although high-density Mg doping is a way for reducing hole traps, the flexibility of the device design and fabrication process is severely limited, and mobility degradation by enhanced impurity scattering is a serious concern. Thus, another process should be developed for passivating V_O-related hole traps in a GaO_x interlayer, and the authors focused on high-pressure treatment for GaN MOS structures, motivated by the ultra-high-pressure annealing (UHPA) process adopted for Mg ion-implanted p-type GaN[36,37]. High-temperature annealing is usually required for activation of implanted dopant atoms. In Mg-implanted GaN, however, thermal decomposition of GaN due to nitrogen desorption (i.e., generation of nitrogen vacancies) easily occurs at a high temperature ($> 1000^\circ$C) under atmospheric pressure. It turned out that UHPA under 400–1000 MPa realized sufficient acceptor activation in Mg-implanted p-type GaN with effectively suppressing thermal decomposition of GaN. Therefore, high-pressure oxygen annealing is expected to be able to suppress generation of V_O in the GaO_x interlayer in MOS structures. Regarding the impact of high-pressure annealing (HPA) on electrical properties of GaN MOS structures, few studies have performed 400 MPa-annealing on n-type GaN MOS capacitors[38]. However, there exist no reports on p-type GaN MOS structures annealed under high pressure, and effects of HPA on hole traps are unclear. In this study, SiO_2/GaN MOS structures were fabricated by performing oxygen annealing under 100 MPa, and the impact of annealing pressure on hole traps was systematically investigated.

Figure 1 depicts a process flow for fabricating SiO_2/p-type GaN MOS structures. SiO_2/GaN MOS capacitors were fabricated using GaN substrates, having a stacking structure with $p^-/p^+/n^+$-GaN epitaxial layers (doping density: 1×10^{17}, 3×10^{18}, and 2×10^{18} cm^{-3}, respectively) grown on n-type GaN(0001) substrates. Although p-type GaN free-standing substrates are unavailable, backside contacts can be formed with a reduced parasitic capacitance at p-n junctions by introducing the heavily doped buffer layers ($\sim 10^{18}$ cm^{-3}). The samples were cleaned with acetone and 50% hydrogen fluoride (HF), followed by nitrogen (N_2) annealing at 800°C for 20 min to activate Mg acceptors. After cleaning the samples with 50% HF again, SiO_2 was deposited by plasma-enhanced chemical vapor deposition (PECVD) under the following process conditions: substrate temperature of 400°C, pressure of 79 Pa, radio frequency (RF) power of 30 W, and tetraethyl orthosilicate (TEOS) and oxygen (O_2) gas flows of 1 and 250 sccm, respectively. The SiO_2 film was determined to be 26–28 nm thick by spectroscopic ellipsometry. Then, PDA was conducted in various conditions. HPA was performed with Hot Isostatic Pressing (HIP) Equipment (O_2-Dr.HIP, Kobe Steel, Ltd.) under 100 MPa in O_2 diluted by argon (Ar) (O_2/Ar: 20%) by varying the temper-

ature from 200–800°C. Note that the O_2 partial pressure of 20% was the maximum value allowed for the equipment, while in principle higher O_2 content is desired for V_O compensation. For comparison, PDA in a diluted O_2 ambient (O_2/N_2: 20%) was performed under atmospheric pressure of 0.1 MPa (atmospheric-pressure annealing, APA). Additionally, to investigate whether HPA is also effective for reducing hole traps, some samples were annealed in a pure O_2 ambient at 800°C under atmospheric pressure, which generates a large amount of fast-response hole traps[24,25], before performing HPA (APA+HPA). Finally, nickel (Ni) gate electrodes and aluminum (Al) backside contacts were formed by vacuum evaporation.

Figure 2 shows bidirectional C–V characteristics of the SiO_2/p-type GaN MOS capacitors subjected to (a) HPA and (b) APA in a diluted O_2 ambient. The probe frequency of the measurement was 1 kHz, and the gate voltage was swept from depletion (positive bias) to accumulation (negative bias), and back to depletion again. We previously reported that the voltage range of the hump (ΔV_{hump}) resulting from hole capturing by interface hole traps gradually increased in 400°C-deposited SiO_2/p-type GaN MOS capacitors when O_2 or N_2 annealing under atmospheric pressure was performed at a higher temperature (200–800°C)[24,25], as an example of the O_2 annealing at 800°C shown in Fig. 2(a) (gray dashed line). In the case of 100 MPa-annealing, on the other hand, ΔV_{hump} (observed at $C \simeq 0.07$–$0.08\ \mu\mathrm{F/cm^2}$) was not much changed even at a higher annealing temperature, indicating that HPA suppressed thermal generation of interface hole traps. All the HPA-treated samples exhibited hole accumulation where the maximum capacitance (C_{max}) of 0.14–0.15 μFcm^2 was close to the oxide capacitance ($C_{\mathrm{ox}} \simeq 0.13\ \mu\mathrm{Fcm^2}$) estimated from the SiO_2 thickness determined by ellipsometry. To distinguish the impact of high pressure and low oxygen content on ΔV_{hump}, APA was performed with the same O_2 partial pressure of 20%. As shown in Fig. 2(b), an increase in ΔV_{hump} and a decrease in C_{max} were clearly observed when annealed at a higher temperature under atmospheric pressure. This result is consistent with our previous report in which an annealing temperature-dependent increase in ΔV_{hump} was observed regardless of the annealing ambient (pure O_2 or N_2)[24]. As a result, it was revealed that the critical factor suppressing hole trap generation was not low oxygen content but high pressure.

Then, ΔV_{hump} was extracted from the experimental C–V curves by a differential analysis described elsewhere[24], and the density of interface hole traps (N_{hump}) was characterized based on $N_{\mathrm{hump}} = C_{\mathrm{ox}}\Delta V_{\mathrm{hump}}/e$, where e is the elementary charge. Figure 3 shows the annealing temperature dependence of N_{hump} in the SiO_2/p-type GaN MOS capacitors. In the samples subjected to APA, N_{hump} significantly increased from 1.4×10^{12} cm^{-2} for the annealing temperature be-

low 200°C to over 1.0×10^{13} cm^{-2} ($\Delta V_{\mathrm{hump}} > 13.5$ V) for 800°C-annealing (indicated by the red dashed line in Fig. 3). When HPA was performed, on the other hand, ΔV_{hump} was in the range of 1.1–2.5 V for each sample, and N_{hump} stayed lower than 2.0×10^{12} cm^{-2} regardless of the annealing temperature. As a result, it turned out that HPA did not cause thermal generation of interface hole traps in p-type GaN MOS structures.

To further investigate the impact of HPA on interface hole traps, some samples were first annealed at 800°C in pure O_2 ambient under atmospheric pressure, and then HPA under 100 MPa was additionally performed. Figure 4 shows the *C*–*V* characteristics of the SiO_2/p-type GaN MOS capacitors subjected to combined annealing (APA+HPA). As reported in previous literature[24,25], APA in O_2 at 800°C generated a large amount of interface hole traps, resulting in a large hump of the *C*–*V* curves ($\Delta V_{\mathrm{hump}} > 13.9$ V). When subsequent HPA was performed at 200-800°C, ΔV_{hump} reduced to 2.1–2.5 V, and hole accumulation with $C_{\mathrm{max}} \simeq C_{\mathrm{ox}}$ was observed regardless of the HPA temperature. The density of interface hole traps for the APA+HPA samples was 1.7–2.0×10^{12} cm^{-2} almost independent of the HPA temperature (green square symbols in Fig. 3), while the density was above 1.1×10^{13} cm^{-2} without HPA (green dashed line in Fig. 3). Therefore, HPA was revealed to not only suppress the generation of interface hole traps but also passivate the traps once generated in GaN MOS structures. Besides, since hole traps were reduced by HPA at the lowest temperature of 200°C, the critical factor is considered to be not additional oxidation during HPA but a high-pressure treatment in an O_2 ambient.

The mechanism of the hole trap reduction by HPA is hypothesized to be related to the generation and reduction of V_{O} in the interfacial GaO_x layer. It is presumed that, under atmospheric pressure, oxygen removal from a GaO_x interlayer easily occurs and is enhanced at a higher temperature in SiO_2/GaN systems, even in an oxidant gas ambient, leading to a significant increase in the hole trap density. Based on the comparison between HPA and APA, on the other hand, V_{O} formation hardly occurs under 100 MPa, and V_{O} once generated by high-temperature APA is compensated for by high-pressure oxygen annealing. This suggests that the decomposition kinetics of a thin GaO_x interlayer in SiO_2/GaN structures would be dominated by annealing pressure: it is more energetically stable for oxygen atoms to be desorbed from the GaO_x layer under atmospheric pressure, while the GaOx interlayer is stable under high pressure. Scanning transmission electron microscope (STEM) and energy dispersive X-ray spectroscopy (EDX) analysis of the SiO_2/p-GaN MOS structures were performed, mainly focusing on the GaO_x interfacial layer. Figure 5 shows the cross-sectional high-angle annular dark field (HAADF)-STEM images and atomic percentage

mapping of Ga and O elements analyzed by EDX near the SiO_2/GaN interfaces subjected to (a) APA (pure O_2, 800°C) and (b) APA and subsequent HPA. Unfortunately, changes in the interface structures (e.g., increases in the thickness and/or atomic density of the GaO_x layer) were not clearly observed because an amorphous GaO_x interlayer was too thin to be identified. Despite this, it was found that oxygen annealing under 100 MPa did not cause the SiO_2 film, GaN bulk, and their interface to degrade. Since we found that N_{hump} could be reduced by about an order of magnitude by HPA, physical and chemical analyses that can monitor such a minor change in the V_{O} density, such as positron annihilation spectroscopy (PAS) technique[39], are needed to fully clarify the mechanism behind the hole trap reduction.

It should be emphasized that the advantage of HPA can be obtained with lower pressure ($\sim$ 100 MPa) than that of the UHPA process (400–1000 MPa) for acceptor activation in Mg-implanted p-type GaN. Thus, the proposed high-pressure treatment could more easily be applicable in the actual device fabrication process. From a technological point of view, investigating how low pressure can be accepted in terms of reducing the hole traps will be a future direction. Adopting the proposed process for actual MOSFET fabrication is also an important future work. Lastly, it should also be mentioned that large hysteresis due to slow-response oxide hole traps remained even after HPA was performed. Since the hysteresis was confirmed to monotonically increase with expanding the sweeping voltage range (maximum negative voltage: up to -15 V), it is challenging to quantitatively discuss the impact of HPA on oxide traps. Despite that, the presence of large hysteresis even after HPA suggests that the origin of oxide hole traps is different from interface traps that are passivated by HPA. For fully understanding the origins of different kinds of hole traps, further studies are necessary by controlling the annealing conditions (temperature and pressure) and depositing various dielectric materials (e.g., SiO_2, aluminum oxide, etc.) with various methods (PECVD, atomic layer deposition, etc.). This approach would help to establish the fabrication process of highly reliable GaN MOS-gate transistors.

In summary, the impact of high-pressure oxygen annealing on fast-response interface hole traps in SiO_2/p-type GaN MOS structures was systematically investigated. The density of the interface hole traps was kept lower than 2×10^{12} cm^{-2} and was negligibly dependent on the annealing temperature (200–800°C) for 100 MPa-annealing (O_2 partial pressure: 20%), while the density exceeded 1×10^{13} cm^{-2} at 800°C when annealed under atmospheric pressure with the same O_2 partial pressure. When HPA was subsequently performed on the MOS capacitors that first annealed at 800°C in a pure O_2 ambient under atmospheric pressure, the hole trap density was reduced by

about an order of magnitude. Consequently, high-pressure oxygen annealing turned out to be effective for not only suppressing thermal generation of interface hole traps but also reducing the hole traps, which would be ascribed to the passivation of oxygen vacancy in the GaO_x interlayer. The present results are useful for the physical understanding of the origin of hole traps in GaN MOS structures and for developing gate dielectric formation processes for highly reliable GaN devices.

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

CONFLICT OF INTEREST

The authors have no conflicts to disclose.

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- **lightly doped p-GaN epilayer** (~1×10^{17} cm^{-3})
- **wet cleaning** (acetone & 50% HF)
- **activation annealing** (N_2, 800°C, 20 min)
- **wet cleaning** (50% HF)
- **SiO_2 deposition by PECVD** (26–28 nm)
- **post-deposition annealing (PDA)**
  - **(1) 100 MPa, O_2/Ar: 20%, 200–800°C [HPA]**
  - **(2) 0.1 MPa, O_2/N_2: 20%, 200–800°C [APA]**
  - **(3) 0.1 MPa, pure O_2, 800°C**
    → **100 MPa, O_2/Ar: 20%, 200–800°C [APA+HPA]**
- **Ni gate electrode & Al back contacts**

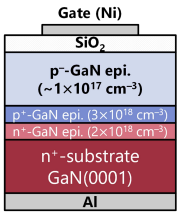

FIG. 1. Process flow for the fabrication of SiO_2/p-type GaN MOS capacitors.

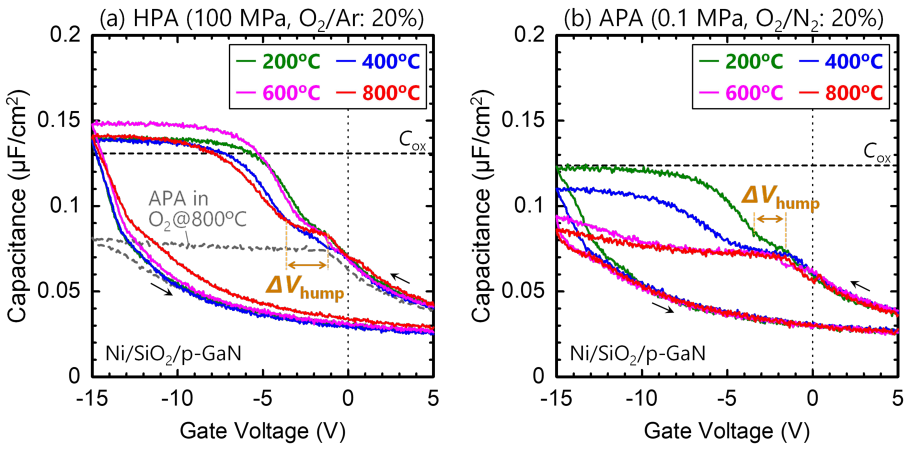

FIG. 2. *C–V* characteristics of the SiO_2/p-type GaN MOS structures annealed at various temperatures (200–800°C) under (a) a high pressure (HPA) or (b) atmospheric pressure (APA). Data obtained in an MOS capacitor underwent APA in O_2 ambient at 800°C are also shown by gray dashed line in (a). Oxide capacitance (C_{ox}) obtained from spectroscopic measurement of the SiO_2 thickness is indicated by horizontal dashed lines.

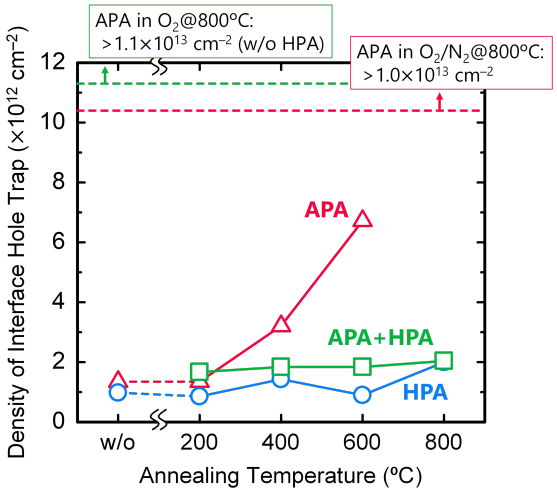

FIG. 3. Density of interface hole traps obtained using the voltage range of the hump (ΔV_{hump}) in *C–V* characteristics of the SiO_2/p-type GaN MOS structures subjected to high-pressure annealing (HPA), atmospheric-pressure annealing (APA), and combined annealing with APA (pure O_2, 800°C) and subsequent HPA (APA+HPA).

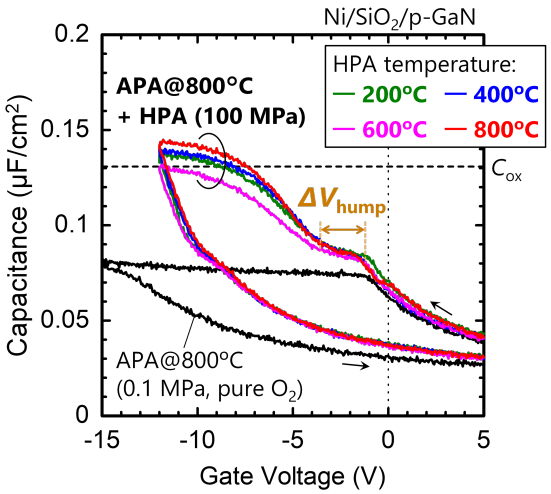

FIG. 4. *C*–*V* characteristics of the SiO_2/p-type GaN MOS structures subjected to annealing combined with APA in pure O_2 ambient at 800°C and subsequent HPA at 200–800°C (APA+HPA).

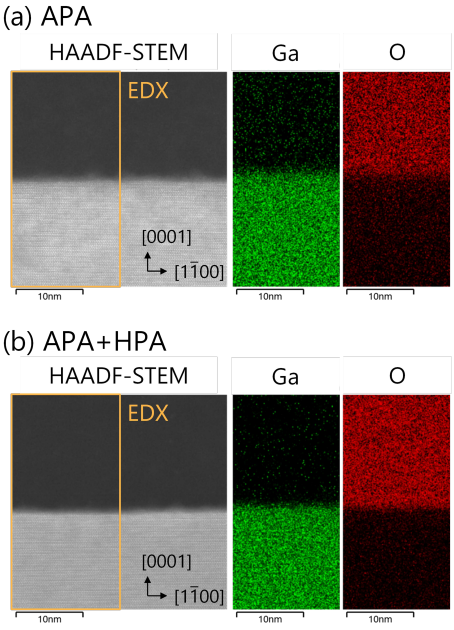

FIG. 5. Cross-sectional high-angle annular dark field scanning transmission electron microscope (HAADF-STEM) image and atomic percentage of Ga and O elements obtained by energy dispersive X-ray spectroscopy (EDX) near the SiO_2/p-type GaN interfaces subjected to (a) APA in pure O_2 at 800°C and (b) APA combined with subsequent HPA.