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Thermal Decouple Design of Multi-Chip SiC Power Module With Thermal Anisotropic Graphite

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Abstract—Thermal design of power modules is necessary to miniaturize and to secure the reliable operation of a high density power conversion system. Miniaturization of the power module reduces the heat conduction area and increases thermal interference among chips in the power module package, which increases the thermal resistance from the junction of chips to heatsink. This paper develops a multi-chip power module, which has the low thermal resistance using a high thermal conductive and anisotropic material graphite. The power module substrate using graphite as a heat spreader for the multi-chip power module is designed based on the numerical simulation of finite element method to reduce the thermal resistance and thermal interference effect of power devices on the power module substrate, and experimentally validated. The developed power module using graphite enables to reduce thermal interference by the use of its thermal anisotropy, and achieves the 8% lower thermal resistance than the conventional copper power module.

Index Terms—Semiconductor device packaging, Finite element method, Graphite

I. INTRODUCTION

POWER electronics plays an increasingly significant role in modern society such as industrial application, transportation, and home electrical appliance. The miniaturization and/or weight saving is a great concern for these applications. Recently, wide bandgap (WBG) semiconductors, such as silicon carbide (SiC) or gallium nitride (GaN), attract attentions as the next generation materials for power semiconductor devices as an alternative of the conventional silicon (Si) semiconductor. They can break through the limitation of operation temperature, voltage and switching frequency of a high density power conversion system, which cannot be achieved with the conventional Si power semiconductor devices [1]-[4]. Fast switching operation of SiC unipolar power devices reduces switching losses and allows high switching frequency operation, which enables to

miniaturize power modules and passive components. Miniaturization of power modules, however, increases heat dissipation per unit area/volume due to the reduction of the heat conduction area. In addition, the effect of thermal interference increases as the distance between components in the power module becomes close. These make thermal management of power modules difficult, which also raises concerns for the long-term reliability. Then, thermal design of power modules is the key factor for miniaturization and reliable operation of high density power conversion systems with SiC power semiconductor devices.

Thermal design of power modules aims at transferring and spreading heat generated in the junction of power semiconductor devices to heatsink. Thermal characteristics of a power module mainly depend on the structure and material property of power module constitution. Thus it is reasonable to increase the heat conduction area and thermal diffusivity by adopting high thermal conductive material for power module package. Copper and aluminum baseplate is often used for power modules as the heat spreader, whose heat conductivity is 401 W/m/K and 237 W/m/K, respectively at room temperature. The higher thermal conductive material is desired to obtain high thermal transferring and spreading capability of power modules.

The carbon based materials such as diamond, graphene, or graphite have the highest thermal conductivity [5], [6]. For example, the thermal conductivity of graphite is over 1500 W/m/K at room temperature. Graphene has been already used as thin heat spreading sheet for mobile applications, and has studied for the nanoelectronic applications [7]. Graphite, which consists of laminated graphene sheets, attracts attention as heat spreading material for power module packages. The density of graphite is less than that of copper and aluminum, which enables to make power module lighter. High thermal conductivity and light weighted heat spreader using graphite was developed in [8]. Reference [9] developed the graphite heat spreader and achieved the low thermal resistance from the power device to heatsink. The research team in [9] also

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developed SiC half bridge module using graphite core for wiring and heat spreader and reduced the thermal resistance and its weight [10]. Moreover, the coefficient of thermal expansion (CTE) for graphite -0.6 ppm/K is closer to CTE of power semiconductor devices than copper or aluminum. This exhibits the long-term reliability as studied in [11].

One feature of graphite is its thermal anisotropy. While the thermal conductivity is 1500 W/m/K for two dimensions, the residual is only 5 W/m/K, which stems from the crystal structure of graphite. Reference [11] developed the laminated graphite heat spreader by orthogonally stacking and bonding three graphite plate so as to uniformly spread heat in power modules. This thermal anisotropy is useful to design the effect of thermal interference among power semiconductor devices in the power module. For a multi-chip power module, thermal interference among chips is one of the concern in thermal design of power modules, and thus analyzed in [12] [13]. Thermally well designed multi-chip power modules using thermal anisotropic graphite contribute to miniaturize a high density power conversion system.

The authors' group developed a high thermal conductive heat spreader with graphite for power module substrates to reduce the junction-to-case thermal resistance and thermal interference effect among power semiconductor devices on the power module substrate. This paper develops a multi-chip SiC half bridge module using the developed graphite heat spreader. The effect of thermal anisotropy in graphite heat spreader is utilized in optimizing thermal design of the power module using the numerical simulation based on finite element method (FEM). The transient thermal resistance of the designed power module is experimentally validated for the implemented single chip and two parallel connected chip power module with the graphite and conventional copper heat spreader.

II. PHYSICAL PROPERTY OF GRAPHITE

The crystal structure of graphite is illustrated in Fig. 1. Graphite consists of stacked graphene sheets with van der Waals forces, which compose of six-membered ring with the covalent bond of carbon atoms. Table I shows the physical properties of typical heat spreading materials. The main features of graphite are the followings:

- 1) High thermal conductivity 1500 W/m/K for planer along graphene plane, where heat is carried by phonon. Low thermal conductivity 5 W/m/K on the stacked direction.
- 2) CTE is -0.6 ppm/K along graphene, which is close to power semiconductor devices. For example, Si is 2.4 ppm/K, and 4H-SiC is 4.2 ppm/K.
- 3) The density 2.22 g/cm³ is smaller than other metal heat spreader.

High thermal conductivity of graphite are expected to expand heat dissipating area and thermal anisotropy can be utilized for suppressing the effect of thermal interference among chips on the power module substrate. And since thermal stress on the die-attach will be small due to less difference of CTE, graphite is also expected to increase the long-term reliability. Moreover, graphite enables to reduce the weight of power module substrates.

TABLE I
PHYSICAL PROPERTIES OF HEAT SPREADER MATERIALS

Material	Heat conductivity λ [W/m/K]	Specific heat c [J/kg/K]	Density ρ [kg/m ³]	CTE [ppm/K]
Graphite	1500 (x, z) 5 (y)	777	2100	-0.6 (x, z) 25 (y)
Copper	401	384	8960	16.8
Aluminum	237	902	2689	23

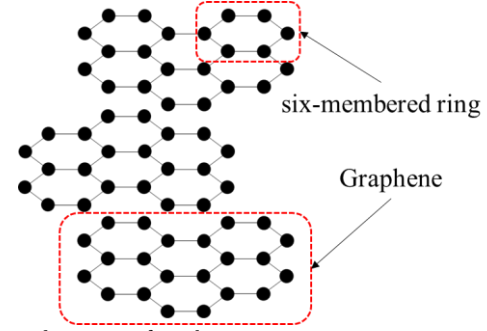


Fig. 1. Crystal structure of graphite

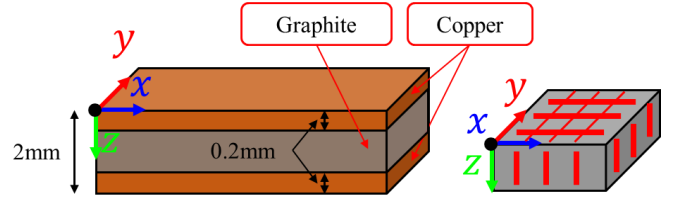


Fig. 2. Overview of the studied graphite substrate. The left hand is the cross-section of the substrate. Thick red line of the right hand indicates the high thermal conductivity.

Fig. 2 illustrates the structure of the developed graphite heat spreader by the authors' group with Kaneka Co. High thermal conductivity of graphite core is set to one horizontal and the vertical direction (for example x, z), and the low thermal conductivity is set to the other horizontal direction (y) as shown in Fig. 2. Graphite is difficult to directly bond a power semiconductor device with solder. Thus, 0.2 mm thin copper plate enclosed both side of the studied graphite core and bonded with 10 μ m thermal conductive adhesive as shown in Fig. 2.

III. POWER MODULE SUBSTRATE DESIGN

To maximize the material capability of graphite, it is necessary to use its thermal anisotropy in heat dissipation of a power module. This section analyzes and designs the thermal anisotropy of a power module substrate with graphite for a multi-chip SiC power module.

A. Specification of the Studied Power Module

Fig. 3 shows the basic structure of the studied two-chip SiC half bridge module. The dimension of the module substrate is 28 mm/15 mm/4.08 mm. The graphite substrate of Fig. 2 is used as a heat spreader and the wiring pattern (P, O) to mount chips. Other wiring patterns (N, G1, G2) are formed with copper since they do not contribute to the heat spreading from the junction of chips. 80 μ m plastic insulation sheet is thermally formed. Two parallel connected SiC MOSFETs CPM2-1200-0160B

TABLE II
DESIGN OF THE THERMAL ANISOTROPY.

Sample	Pattern (P)	Pattern (O)	Heat spreader
GrCu-A	XZ	XZ	XZ
GrCu-B	YZ	XZ	XZ
GrCu-C	XZ	YZ	XZ
GrCu-D	YZ	YZ	XZ
GrCu-E	XZ	XZ	YZ
GrCu-F	YZ	XZ	YZ
GrCu-G	XZ	YZ	YZ
GrCu-H	YZ	YZ	YZ

TABLE III
PHYSICAL PARAMETERS OF MATERIALS FOR SIMULATION

Material	λ [W/m/K]	c [J/kg/K]	ρ [kg/m ³]
SiC	495	680	3250
Sn-Ag-Cu	54	231	7400
Insulation sheet	2	860	2070
Si grease	0.84	800	2340
Al	237	902	2698
Air	0.027	1006	1.205

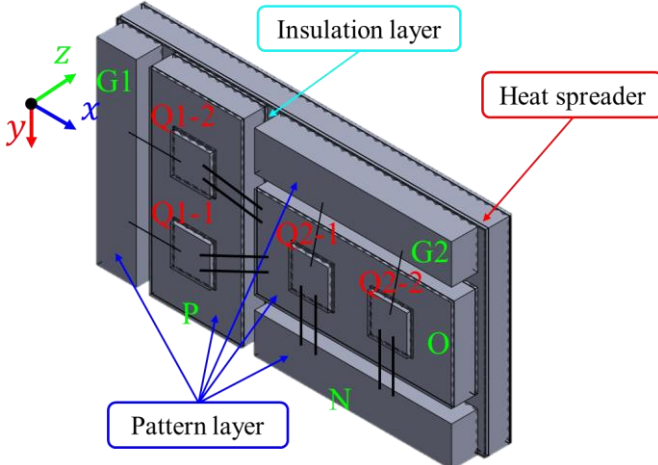


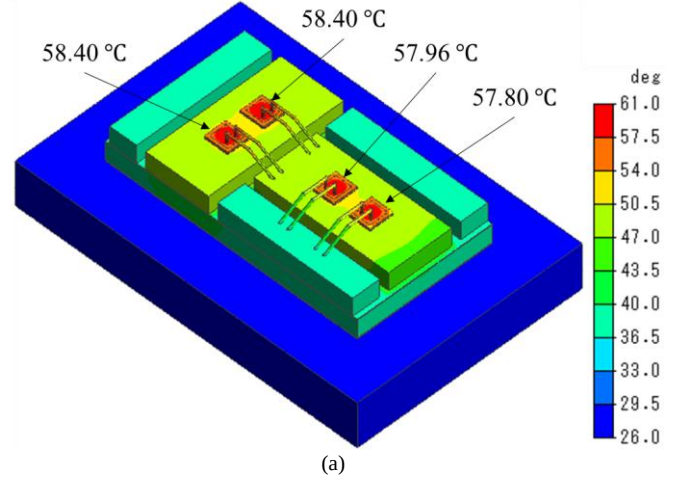
Fig. 3. Basic structure of the studied power module.

(1200 V/20 A, 2.39 mm/2.63 mm/0.18 mm, CREE) are mounted on both side arm of the power module with 120 μ m Sn-Ag-Cu solder (SMIC). The distance between center of chips on each arm is 4 mm. Gate and source of MOSFETs are wired with 100 μ m and 300 μ m Al wire, respectively.

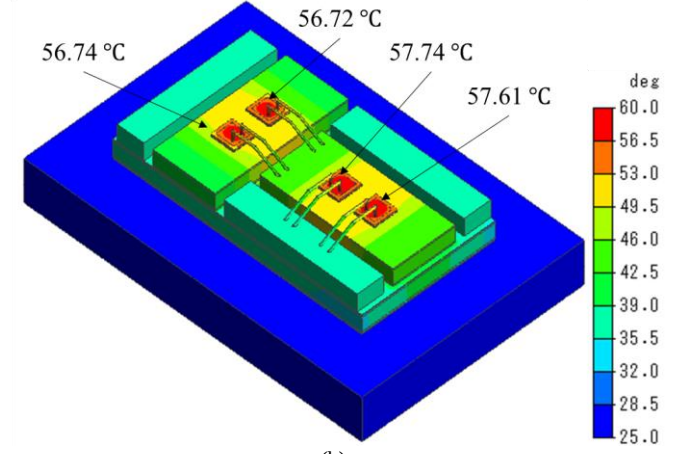
This paper designs the direction of thermal anisotropy for the power module substrate with graphite to reduce thermal interference among chips. The combination of thermal anisotropy on the power module substrates is listed in Table II. Here, “GrCu” denotes the graphite wiring power module substrate. “XZ” and “YZ” denote that (x, z) and (y, z) direction have the high thermal conductivity, respectively. All copper wiring power module substrate with same dimension is also prepared as a reference to compare thermal characteristics with graphite module substrate. The weight of the developed graphite and copper power module are 7.2 g and 14.0 g, respectively. The graphite enables to reduce the weight of power module in the same size. On the other hand, thermal capacitance of graphite wiring module is small, which may cause the fast temperature raise in over or fault current condition.

TABLE IV
JUNCTION TEMPERATURE OF EACH MOSFET INCREASED BY THERMAL INTERFERENCE.

Sample	High side	Low side
Cu	33.597	33.348
GrCu-A	31.149	33.562
GrCu-B	33.034	33.553
GrCu-C	31.177	31.865
GrCu-D	33.049	31.859
GrCu-E	33.492	33.968
GrCu-F	35.417	33.989
GrCu-G	33.589	32.369
GrCu-H	35.509	32.385



(a)



(b)

Fig. 4. Temperature distribution by FEM simulation. (a)Cu module substrate. (b)Graphite module substrate.

B. Design to Reduce Thermal Interference Effect

Thermal analysis of each studied power module is conducted using the numerical simulation model based on FEM with software Femtet (Murata Software) for steady-state heat conduction analysis. The uniform ambient temperature 25 °C is set at the backside of a heatsink and other surfaces of the model are thermally insulated. The heat dissipating active area of SiC MOSFET is given as 2.0 mm/1.8 mm/20 μ m at the surface of MOSFET to simulate the heat generation in the channel of an MOSFET. The physical parameter of materials for FEM simulation is listed in Table I and III.

The calculated junction temperature of each MOSFET on the

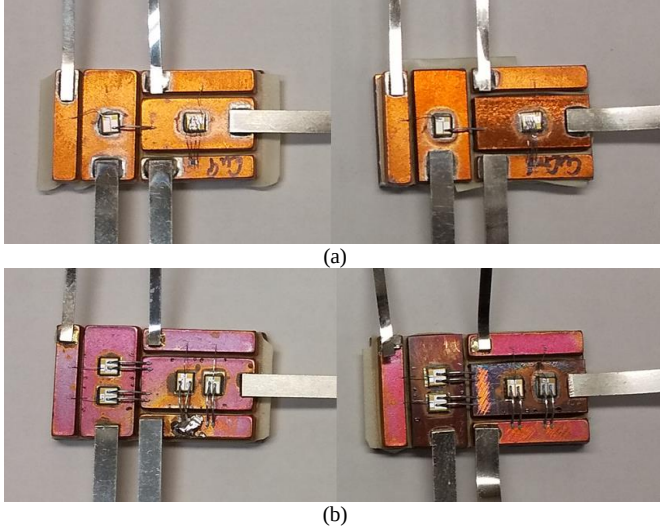


Fig. 5. The implemented power module. (a)Single chip power module. (b)Two chip power module. The left and right hand are Cu and graphite wiring power module, respectively.

studied module is listed in Table IV. In this simulation, Q1-1 or Q2-1 are set to dissipate heat at 10W, and the temperature of the companion die Q1-2 or Q2-2 are evaluated, respectively. Here, the averaged temperature on active area is used as the junction temperature. The temperature distribution for the copper wiring power module substrate is same at the high and low side arm. The temperature distribution for the graphite power module substrate is different for the combination of the high thermal conductivity direction. GrCu-B and F have the larger thermal interference effect, whose high thermal conductivity orientation transfers the heat to the companion chip. The design of orientation on thermal conductivity for the thermal anisotropic substrate is necessary for a multi-chip power module package to reduce the junction-to-case thermal resistance.

The sample GrCu-C gives the lowest thermal interference for both side arm as shown in Table IV. The temperature distribution in Cu and graphite power module obtained from FEM simulation is shown in Fig. 4. Here, all the MOSFETs dissipate heat at 10W. The temperature distribution shows that the graphite wiring power module substrate gives the higher heat spreading capability than the copper power module substrate.

IV. EXPERIMENTAL EVALUATION OF DESIGNED POWER MODULE

This paper experimentally evaluates the thermal interference reduction for power module substrate with graphite heat spreader, and validates its design using FEM simulation in section III. Single chip and two parallel connected chips are implemented in one arm of power modules for each substrate as shown in Fig. 5 to verify the thermal interference.

A. Transient Thermal Characteristics

The transient thermal network models called as structure function from junction to ambient for each side arm of the studied single chip power module are shown in Fig. 6. Structure function is identified from the time response of junction

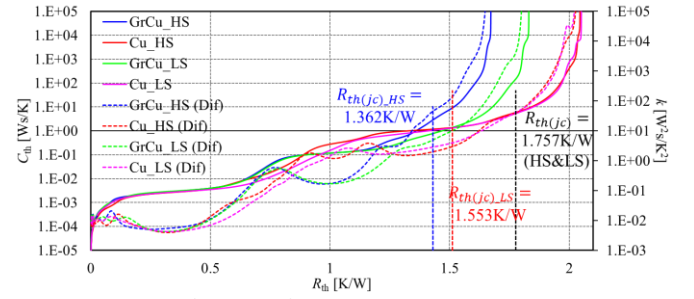


Fig. 6. The structure functions of the studied one chip power module.

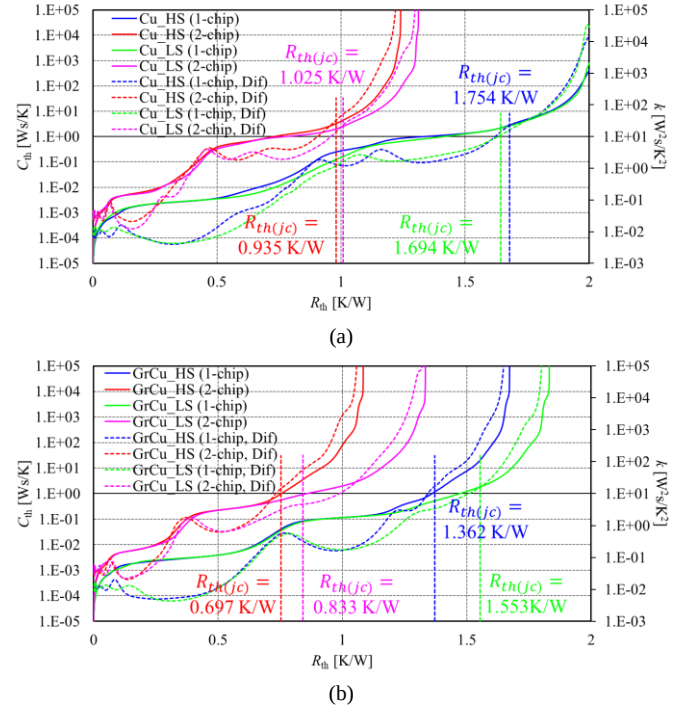


Fig. 7. The structure functions of the studied power module. (a)Copper power module. (b)Graphite power module.

temperature based on static test method [14] using T3Ster (MentorGraphics). Here, the time response of junction temperature is experimentally measured using the temperature dependency of body diode of MOSFET for a fixed small measurement current by applying $V_{gs} = -9$ V to gate and source terminal with battery during the measurement, which is proposed by the authors in Ref. [15] to avoid the dynamical threshold voltage shift in SiC MOSFET. “Dif” denotes the differential structure function, which is obtained by numerically differentiating the structure function to detect inflection points.

The junction-to-case thermal resistance is identified with thermal dual interface method in [14] and the inflection point of the differential structure function. The thermal resistances for the high and low side of the graphite power module with the single chip are 1.362 K/W and 1.553 K/W, respectively, while 1.757 K/W and 1.757 K/W for the copper power module. The thermal capacitance of the developed graphite power module is higher than the copper power module at the range from 0.5 K/W to 0.8 K/W, and copper power module gives higher value beyond this range. The density and specific heat of graphite are a quarter and two times of copper, respectively. The higher thermal conductivity of graphite spreads heat at the horizontal

direction, which leads to the higher thermal capacitance than copper power module at the first several micro seconds on the time response of junction temperature. Thus, the developed power module using graphite enables to mitigate the critical initial rise of junction temperature in over or fault current condition.

The structure functions of the studied two chip power module is shown in Fig. 7. The thermal resistance and thermal capacitance for two chips is a half and two times of one chip power module, respectively as shown in Fig. 7, since heat dissipating area of chip is almost two times larger. The thermal resistance from junction of MOSFET to the heatsink for each studied power module is shown in Table V. The thermal resistance of the studied two chips power module with copper will be ideally a half of the single chip power module, but it is higher than in actual due to thermal interference among chips, which is reflected in the thermal resistance. The studied power module with graphite enables to suppress the thermal resistance about 8% for both side arm. The thermal anisotropy of graphite enables to reduce thermal interference and to achieve the low thermal resistance for power modules.

B. Parasitic Inductance

The frequency characteristics of the parasitic inductance between terminal P and N of the developed graphite power module is shown in Fig. 8. The blue and red solid line are the measured and simulated result, respectively. The measured result is experimentally obtained by impedance analyzer 4294A (Agilent Technology) with conducting MOSFET by applying $V_{gs}=18$ V between the gate to source terminals for both arms. The measurement result under 1 MHz includes noticeable noise due to the detection limit of equipment. The simulated result is calculated by electromagnetic analysis of FEM simulation using Femtet between the terminal P and N in one port S parameter analysis. The simulated result of the inductance is good agreement with the measured result. The parasitic inductance of the developed module substrate is 2.26 nH at 10 MHz, which is smaller to the same size power module of 6.51 nH in Ref. [16]. In addition, the thermal resistance from the junction to case of the previous module [16], which mounted 3 mm square one SiC SBD as heat source, is 0.91 K/W. The larger heat conduction area decrease the thermal resistance. In general, miniaturization of power module enables to reduce the parasitic inductance, but it increases the thermal resistance. The developed power module using thermal anisotropy of graphite heat spreader will enable to reduce both the thermal resistance and the parasitic inductance.

V. CONCLUSION

This paper developed a low thermal resistance power module substrate using the high thermal conductivity with thermal anisotropic graphite to reduce thermal interference effect for a multi-chip SiC power module. The design of thermal anisotropy for a two chip power module based on FEM simulation enabled to reduce the thermal resistance offered by thermal interference. The experimental results showed the lower thermal resistance of the designed graphite power module than the conventional copper power module and validated the FEM simulation results.

TABLE V
JUNCTION TEMPERATURE OF EACH MOSFET INCREASED BY THERMAL INTERFERENCE.

Sample		One chip [K/W]	Two chip [K/W]	ΔR [%]	ΔR [K/W]
Copper	HS	1.694	0.935	10.42	0.088
	LS	1.754	1.025	16.86	0.148
Graphite	HS	1.362	0.697	2.37	0.016
	LS	1.553	0.833	7.25	0.056

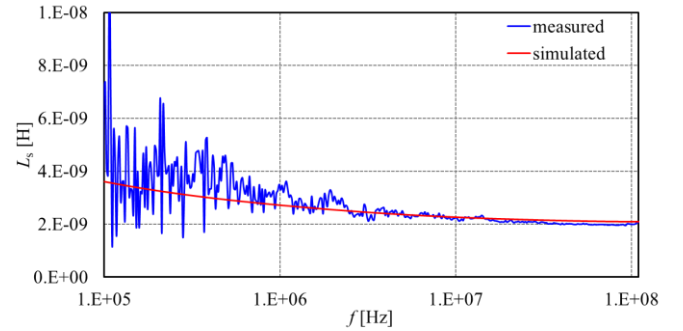


Fig. 8. Frequency characteristics of the impedance between the terminal P and N by conducting MOSFET.

The developed graphite power module enables to achieve high frequency switching operation and to realize a high density power conversion system.

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