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Doctoral Dissertation

**Characterization and Mitigation of Defects in
SiC MOS Structures for High-Performance
and High-Reliability MOSFETs**

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January 2026

**Graduate School of Engineering
The University of Osaka**

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Chapter 1

Introduction

1.1 Background

Semiconductors are now indispensable in a wide range of applications and form the backbone of modern society. In recent years, remarkable advances in artificial intelligence (AI), digital transformation (DX), and data centers, have been driven by the continuous evolution of semiconductor technologies. However, these advances have increased power consumption and carbon dioxide (CO₂) emissions, thereby accelerating global warming. To address this issue, it is essential to achieve a carbon-neutral society, which requires the development of high-efficiency power electronics. Power electronics is a technology that controls, transfers, and supplies electricity [1], and is applied in a wide range of fields, including electric vehicles, trains, smart grids, and renewable energy systems. The key to realizing high-efficiency power electronics depends on power devices, a primary component of power electronics.

Today, silicon (Si) is commonly used as the base semiconductor material for power devices. For a low breakdown-voltage application, metal-oxide-semiconductor field-effect transistors (MOSFETs) are often used due to their fast-switching capability. However, their on-resistance increases significantly with a higher breakdown voltage application, because a drift region must be thick to withstand the voltage [2]. This makes MOSFETs less suitable for high-voltage applications. In contrast, insulated-gate bipolar transistors (IGBTs) can achieve lower on-resistance even at high voltages through conductivity modulation, with which minority carriers are injected into the drift region, effectively reducing its resistance [3]. The drawback of IGBTs, however, is the high switching losses associated with the tail current [2]. Consequently, MOSFETs and IGBTs are used in different breakdown voltage ranges depending on the trade-off between on-resistance and switching characteristics. Currently, approximately 10% of the power is lost during power conversion [4]. Since they use large amounts of electricity, reducing the losses is a critical issue. However, the on-resistance of Si-based power devices has already reached the physical

limits of Si, and further improvements are difficult to achieve. Thus, wide-bandgap semiconductors such as silicon carbide (SiC), gallium nitride (GaN), gallium oxide (Ga_2O_3), and diamond are gaining attention as next generation power semiconductor materials. Among various wide bandgap semiconductors, SiC has advantages over controllable n- and p-type doping, formation of an insulating layer through thermal oxidation, and the commercial availability of large-diameter wafers [4–6].

1.2 Physical Properties of Silicon Carbide (SiC)

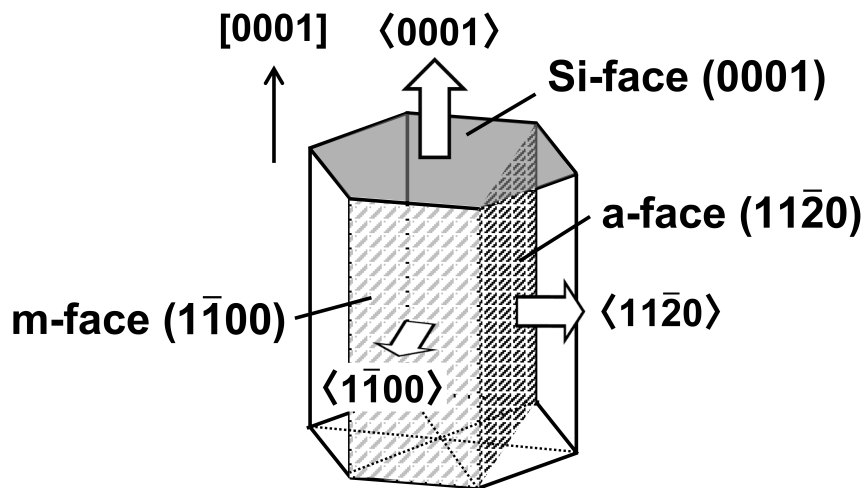
SiC is a group IV-IV compound semiconductor consisting of Si and carbon (C) bonded in a 1:1 ratio. A unique feature of SiC is the existence of numerous polytypes, with more than 200 reported to date [4]. The names of these polytypes are determined by their crystal structure and the number of Si-C layers within one unit cell according to Ramsdell's notation. When the structure is cubic, hexagonal, or rhombohedral, it is denoted as C, H, or R, respectively. Table 1.1 shows the main physical properties of Si, 3C-, 4H-, and 6H-SiC [4, 7]. SiC has a wider bandgap and a higher dielectric breakdown field than Si, which offers strong advantages in lowering the on-resistance of power devices. Furthermore, since the thermal conductivity of SiC is about three times higher than that of Si, the cooling systems for power modules can be simplified, enabling an increase in power density of devices. Among the polytypes, 4H-SiC is the most suitable for power devices due to its wide bandgap [4], high critical breakdown field [8], high electron mobility [9], and small anisotropy in electron mobility [9].

It is known that electron mobility and permittivity of 4H-SiC are dependent on crystal orientation. Figure 1.1 shows the crystal orientation axes of the hexagonal system and the typical crystal and surface orientations. The Si-face is the most used crystal face and corresponds to the (0001) orientation, which is referred to as the basal plane. In contrast, the a- and m-faces, which are perpendicular to the Si-face, are referred to non-basal planes and are typically used as channel faces in trench-type power devices, as will be explained in next section. The Si-face is terminated by Si atoms, whereas a- and m-faces are terminated by Si and C atoms, which leads to distinct interface properties and strongly affects the device performance [10].

For device applications, an epitaxial layer is grown on the SiC substrate using a chemical vapor deposition (CVD) method, which allows precise control over doping concentration and film thickness. However, when using an on-axis 4H-SiC substrate, 3C-SiC, which is stable at low temperatures, tends to grow [11, 12]. To overcome this issue, the substrates are intentionally tilted off-axis, creating atomic steps on the SiC surface and enabling the growth of high-quality 4H-SiC epilayers, a process known as step-controlled epitaxy [13].

Table 1.1. Major physical properties of Si, 3C-, 4H-, and 6H-SiC [4, 7]

	Si	3C-SiC	4H-SiC	6H-SiC
Bandgap (eV)	1.12	2.36	3.26	3.02
Relative Dielectric Constant	11.9	9.72	9.76 ($\perp c$) 10.3 ($\parallel c$)	9.66 ($\perp c$) 10.0 ($\parallel c$)
Critical Electric Field (MVcm $^{-1}$)	0.3	1.4	2.2	1.7
Electron Mobility (cm 2 V $^{-1}$ s $^{-1}$)	1450	1000	1000 ($\perp c$) 1200 ($\parallel c$)	450 ($\perp c$) 100 ($\parallel c$)
Thermal Conductivity (Wcm $^{-1}$ K $^{-1}$)	1.6	3.3–4.9	3.3–4.9	3.3–4.9
Hole Mobility (cm 2 V $^{-1}$ s $^{-1}$)	500	100	120	100

**Figure 1.1.** Schematic illustration of crystal orientations in a hexagonal structure.

1.3 Advantages of SiC Metal-Oxide-Semiconductor (MOS) Devices

1.3.1 On-Resistance

The theoretical limit of on-resistance (R_{on}) of unipolar devices, such as Schottky barrier diodes and MOSFETs, is essentially the resistance of the drift layer and is given by [2]

$$R_{\text{on}} = \frac{4V_{\text{B}}^2}{\varepsilon\mu E_{\text{B}}^3}, \quad (1.1)$$

where, V_{B} , ε , μ , and E_{B} are the breakdown voltage, permittivity, carrier mobility, and critical electric field strength of semiconductor, respectively. Figure 1.2 shows specific on-resistance as a function of breakdown voltage. The relationship between on-resistance and breakdown voltage of SiC is based on the latest updated data, assuming that E_{B} depends on the doping concentration and that the device has a non-punch-through structure [14]. Because SiC has a higher E_{B} than Si, the on-resistance of SiC MOSFETs can theoretically be about 600 times lower than that of Si-based power devices. This theoretical advantage has already been demonstrated in reported SiC MOSFETs [6, 15]. The adoption of SiC power devices in electric vehicles and railway applications is rapidly advancing, with substantial energy-saving benefits.

Figure 1.3 shows the schematic diagram of lateral, planar, and trench power MOSFETs. Power MOSFETs have a thick drift layer, through which the drain current flows vertically. This enables power MOSFETs to operate at high voltages, which distinguishes them from ordinary low-voltage MOSFETs (Fig. 1.3(a)).

The on-resistance of vertical MOSFETs is determined by the sum of the series resistances, including contact, channel, junction FET (JFET), drift, and substrate resistances in the planar power MOSFETs. In power devices, a thick drift layer is required to achieve a high breakdown voltage, which typically makes the drift resistance the dominant factor in determining the on-resistance. Indeed, Eq. (1.1) expresses the resistance of the drift layer. Replacing Si with SiC substantially reduces the drift resistance, owing to its wider bandgap and higher critical electric field. On the other hand, compared with the planar structure, the trench structure can increase current density by reducing the cell pitch, and the absence of a JFET region reduces the on-resistance. In the planar structure, the channel is formed on the basal plane, whereas non-basal planes (e.g., a- and m-faces) are used as the channel faces in the trench structure. The channel mobility at the SiC MOS interface on these non-basal planes is higher than that on the Si-face [10]. As a result, the trench structure has lower channel resistance compared with the planar structure. Because of these reasons, the common structure of current SiC MOSFETs is the trench type, which has already been commercialized [6].

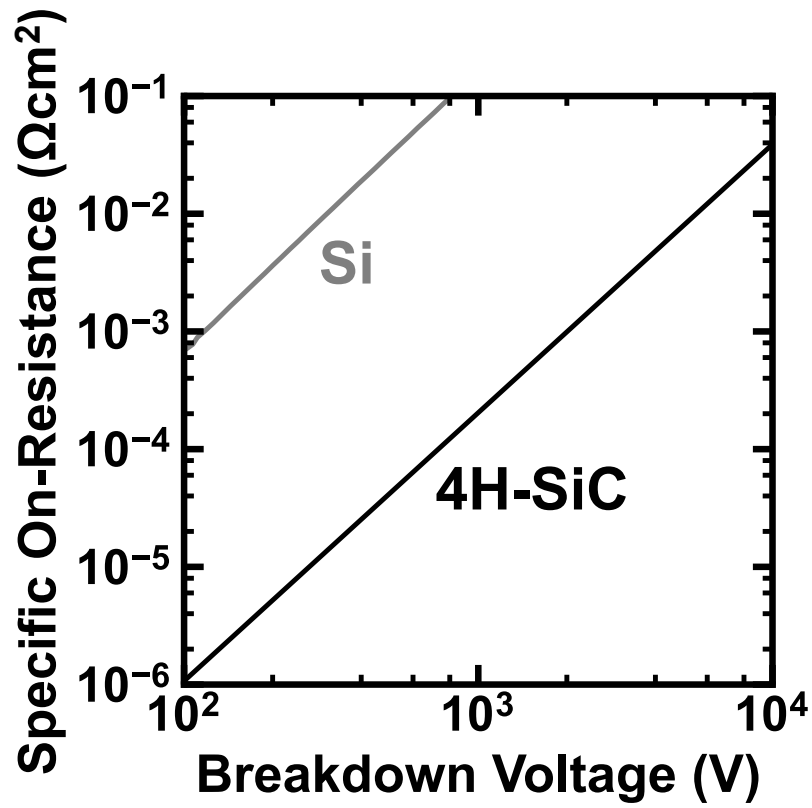


Figure 1.2. Specific on-resistance as a function of breakdown voltage for Si and 4H-SiC [14].

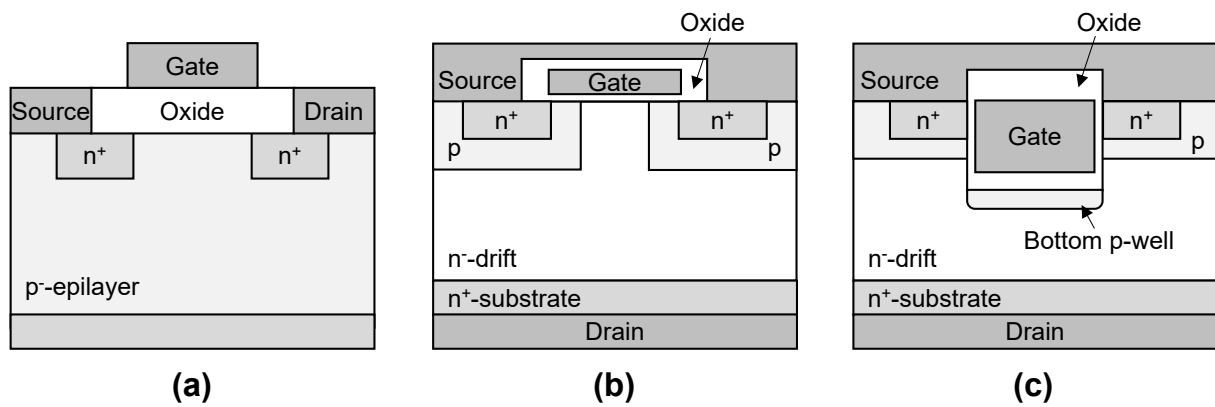


Figure 1.3. Schematic cross-sectional diagrams of lateral, planar, and trench MOSFETs.

1.3.2 Operation Under Harsh Environments

SiC semiconductor devices can be applied not only to power electronics but also to integrated circuits (ICs) operating in high-temperature environments [16]. At elevated temperatures, electrons in the valence band can gain sufficient thermal energy to be excited into the conduction band, which may cause the semiconductor to lose its n- or p-type conductivity and result in a p-n junction failure. In wide bandgap semiconductors, a large energy is required for this excitation. Figure 1.4 shows the intrinsic carrier density (n_i) of Si and SiC. n_i of Si is about 10^{10} cm^{-3} at room temperature, but it increases to 10^{14} cm^{-3} at 200°C . When the minority carrier density in Si becomes close to the majority carrier density, the reverse-bias leakage current increases, which is undesirable. In contrast, n_i of SiC is only about 10^{-9} cm^{-3} at room temperature and 10^{-3} cm^{-3} at 200°C , much lower than Si. This means that SiC devices can operate more stably than Si devices at high temperatures, and in fact, high-temperature operation of SiC MOSFETs has been demonstrated [17, 18].

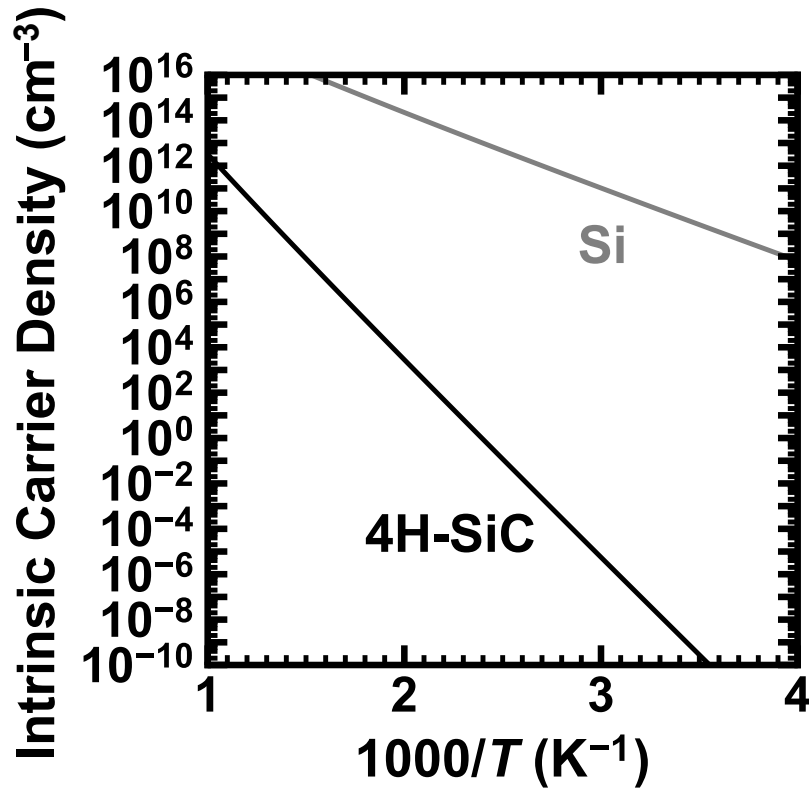


Figure 1.4. Temperature (T) dependence of the intrinsic carrier density of Si and 4H-SiC.

In addition, SiC devices can also be used in radiation-rich environments such as space or nuclear power plants, where they are exposed to high-energy particles (α -rays, heavy

ions), light particles (neutrons, electrons), and photons (X-rays, γ -rays, UV light). In such environments, their electrical properties can change due to interactions with high-energy particles [19, 20]. While Si devices are mainly used in those harsh environments, SiC has better physical properties than Si, which can lead to improved device reliability. Since SiC has a wider bandgap than Si, fewer electron-hole pairs are generated when the device is exposed to radiation. As a result, the leakage current under reverse bias is smaller in harsh environments [21], and SiC MOSFETs with high radiation tolerance have also been reported [22, 23].

1.4 Issues of SiC MOS Field-Effect Transistors (MOSFETs)

Although SiC MOSFETs exhibit excellent properties, a SiC MOS structure, the core of the MOSFET, contains a variety of defects that significantly impact device performance [4, 5, 24–27]. These defects lower the MOS channel mobility by scattering [28, 29] and trapping carriers [30] and also degrade the long-term reliability of the gate oxide [31]. Figure 1.5 schematically illustrates a cross-sectional view of a planar n-channel MOSFET and the silicon dioxide (SiO_2)/SiC interface, highlighting the presence of interface traps, fixed charges, near-interface traps, and oxide traps [31–36]. These defects are the main causes of the major challenges associated with SiC MOSFETs, which leads to low channel mobility and poor reliability.

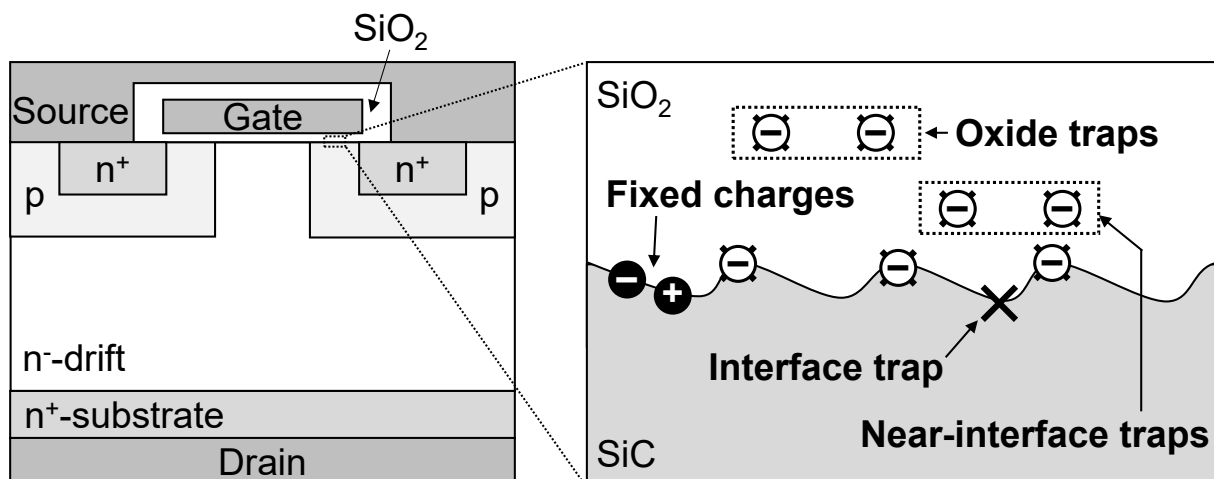


Figure 1.5. Schematic cross-sectional view of a planar MOSFET and schematic illustration of the MOS interface, the core region of the device, where various defects such as interface traps, fixed charges, near-interface traps, and oxide traps are present.

1.4.1 Low Channel Mobility

Low channel mobility, one of the major issues of SiC MOSFETs, increases channel resistance, resulting in an increase in the on-resistance. For devices with a breakdown voltage of 600–1200 V, the on-resistance is about ten times higher than the physical limit, mainly due to the high channel resistance. The channel resistance accounts for 66% of the total on-resistance in 600 V devices and 48% in 1200 V devices [6]. This high channel resistance has been a major obstacle to the widespread adoption of SiC MOSFETs and is attributed to the low channel mobility in the SiC MOS channel.

The channel mobility (μ_{channel}) can be expressed as follows [4]:

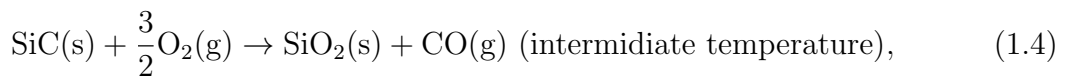
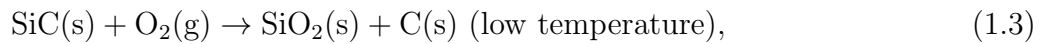
$$\mu_{\text{channel}} = \mu_{\text{free}} \times \frac{n_{\text{free}}}{n_{\text{free}} + n_{\text{trap}}}, \quad (1.2)$$

where μ_{free} , n_{free} , and n_{trap} are the mobility of mobile electrons, the density of mobile electrons, and the density of trapped electrons, respectively. In SiC MOS channels, both μ_{free} and n_{free} are low, resulting in significantly reduced μ_{channel} .

Low Density of Mobile Electrons

Low n_{free} is due to a high density of interface states. SiC is more suitable for MOSFET applications than other wide bandgap semiconductors because it can form a SiO₂ dielectric by thermal oxidation. However, the interface state density (D_{it}) near the conduction band edge (E_C) at the SiO₂/SiC interface is about $10^{13} \text{ eV}^{-1}\text{cm}^{-2}$, much higher than at SiO₂/Si interfaces [32, 37].

The origin of interface states has been discussed for many years. Theoretical and experimental studies have suggested that carbon-related defects are plausible candidates of D_{it} [38–40]. Various carbon-related defects, such as C-C bonds [40–43], C-O bonds [39, 42], C clusters [44, 45], and C dangling bonds [46, 47] have been proposed. This can be qualitatively explained by considering the thermal oxidation reactions of SiC, which are expressed as follows:



SiO₂ can be formed under passive oxidation conditions (Eq. (1.3) and (1.4)). On the other hand, under active oxidation conditions, volatile SiO is generated, preventing the formation of the oxide (Eq. (1.5)). Although the ideal oxidation reaction of SiC is represented by Eq. (1.4), the reaction deviates from this ideal in practice, resulting in formation of carbon-related defects, likely due to residual carbon at the SiO₂/SiC interface. When

thermally oxidized samples were annealed in an ultra-high-purity argon (Ar) atmosphere, ejection of carbon atoms from the SiO₂/SiC interface into the SiO₂ layer was observed by secondary ion mass spectrometry (SIMS) measurements, indicating the presence of excess carbon atoms at the SiO₂/SiC interface [48].

Figure 1.6 shows a schematic band diagram of the SiO₂/SiC interface. Interface states capture electrons in the SiC MOS channel, reducing n_{free} [30]. Since trapped carriers do not contribute to conduction, drain current density is reduced, leading to an increase in on-resistance. At the as-oxidized SiO₂/SiC interface, the mobile electron ratio is only a few percent, resulting in very low field-effect mobility (μ_{FE}). For as-oxidized n-channel SiC MOSFETs, μ_{FE} is 3–5 cm²V⁻¹s⁻¹ [49], which is significantly lower than the bulk mobility of SiC (~ 1000 cm²V⁻¹s⁻¹ [9, 50]).

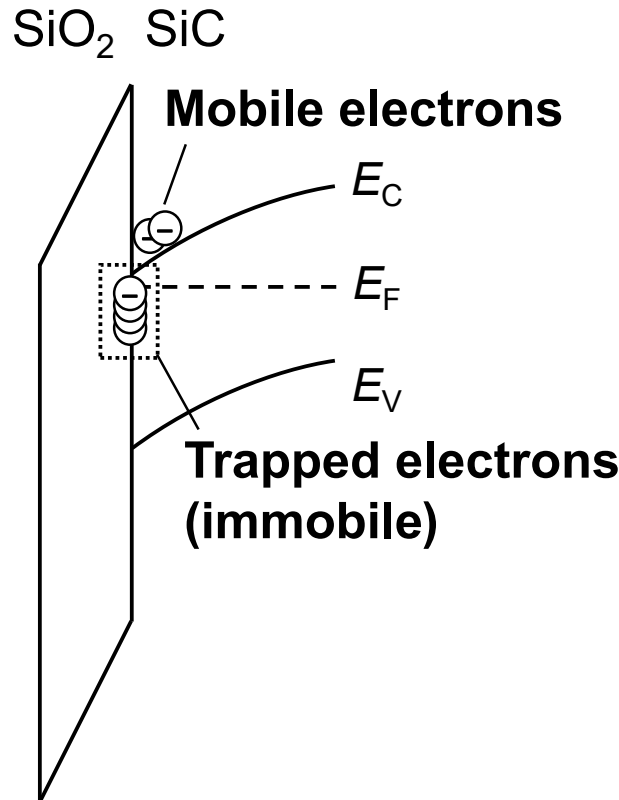


Figure 1.6. Schematic band diagram of the SiO₂/SiC interface. Interface states capture electrons in the SiC MOS channel, and the trapped electrons do not contribute to conduction.

Low Mobility of Mobile Electrons

Although the cause of low μ_{free} is still debated, Coulombic scattering is often considered the main factor. In SiC MOSFETs, conventional mobility evaluation metrics, such as μ_{FE} or effective mobility, cannot accurately measure μ_{free} . This is because an assumption

underlying these evaluations breaks down when D_{it} is extremely high. To accurately determine μ_{free} , MOS-Hall effect measurements have recently been used to study scattering mechanisms [30, 51, 52]. The Hall mobility (μ_{Hall}) obtained from the Hall effect measurement is assumed to μ_{free} because the measured Hall voltage reflects the contribution of free electrons. According to a previous study, while μ_{FE} of the thermally oxidized sample was 8–9 cm²V⁻¹s⁻¹, μ_{Hall} was about 160 cm²V⁻¹s⁻¹ [30]. This result shows that electron trapping due to D_{it} has a significant effect on the gate characteristics of SiC MOSFETs. By comparison, in Si MOSFETs, μ_{free} is about 1/3 of the bulk mobility [53, 54], but it is only about 1/10 in SiC MOSFETs. This suggests the presence of numerous scattering centers at the SiO₂/SiC interface. Several types of scattering factors have been proposed, including interface dipoles [55], potential fluctuations at the E_C [56], trapped charges [28, 57], fixed charges [57–59], and neutral defects [60], but their exact origins remain unclear.

Mobility Enhancement Techniques

For decades, many researchers have tried to improve $\mu_{channel}$. Currently, the standard method for improving $\mu_{channel}$ is annealing in a nitric oxide (NO) atmosphere [61–63]. During NO annealing, nitrogen atoms are introduced at the SiO₂/SiC interface, which reduces D_{it} to about 10¹¹–10¹² eV⁻¹cm⁻² [61, 64]. This increases the mobile electron ratio to about 30% and μ_{FE} to around 30–40 cm²V⁻¹s⁻¹ in SiC MOSFETs fabricated on the Si-face [30, 63]. It has also been revealed that such mobility improvement depends on the amount of nitrogen incorporated at the SiO₂/SiC interface [65]. However, during prolonged nitridation, the amount of nitrogen at the SiO₂/SiC interface saturates because nitrogen atoms are removed by O₂, a byproduct of NO decomposition [66]. While nitrogen incorporation is a dominant reaction in the early stage of NO nitridation, prolonged annealing leads to a balance between nitridation and nitrogen removal by O₂, resulting in saturation of the nitrogen amount.

Other approaches have also been reported, including the incorporation of phosphorus (P) [67], boron (B) [68], and sodium (Na) [69]. μ_{FE} can be increased to 89 cm²V⁻¹s⁻¹ by annealing in POCl₃ at 1000°C followed by nitrogen (N₂) annealing [67]. B diffusion in a thermally grown oxide has enabled reduction of D_{it} , resulting in high μ_{FE} peak values (102 cm²V⁻¹s⁻¹) [68]. Incorporation of Na accelerates SiC oxidation, leading to very high μ_{FE} (170 cm²V⁻¹s⁻¹) [69], however, practical use of Na is limited due to ion drift. Another approach is an ultra-high temperature oxidation process that does not introduce foreign atoms at the SiO₂/SiC interface [49]. In this method, the temperature and the O₂ partial pressure are optimized to achieve the ideal oxidation conditions represented by Eq. (1.4). Specifically, SiC is oxidized at 1600°C in a 0.3% O₂ atmosphere, which lies at a passive-active oxidation boundary. While the μ_{FE} value of thermally oxidized samples is around 3 cm²V⁻¹s⁻¹, this process increases it to about 10 cm²V⁻¹s⁻¹. High-temperature CO₂

annealing is also effective in improving the electrical properties of SiO₂/SiC interfaces [70]. The oxidation rate of SiC in CO₂ ambient follows an activation energy of approximately 7.5 eV, which is significantly higher than that of conventional O₂ oxidation (2.9 eV). Post-oxidation annealing (POA) in CO₂ at temperatures above 1400°C improves the SiO₂/SiC interface quality, resulting in an enhanced μ_{FE} ($\sim 11 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$).

The interface properties are also known to strongly depend on the crystal orientation. D_{it} of thermally oxidized samples is higher on the non-basal planes than on the Si-face [71, 72]. In contrast, NO nitridation improves the interface properties, and SiC MOSFETs fabricated on non-basal planes (a- and m-faces) exhibit μ_{FE} of 80–100 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ [10, 73], which is significantly higher than that on the Si-face. This feature provides a clear advantage in trench MOSFET applications.

As a new strategy, oxidation-minimizing processes have recently been proposed, and a dramatic improvement in μ_{FE} has been demonstrated [74–77]. In this method, hydrogen (H₂) annealing is first performed to remove surface defects on the SiC surface. Next, a deposited SiO₂ layer is used to suppress defect generation during oxidation of SiC, and finally, interface nitridation is performed. The oxidation-minimizing process reduces D_{it} to below $10^{11} \text{ eV}^{-1}\text{cm}^{-2}$ and increases μ_{FE} to $\sim 80 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ even for SiC MOSFETs fabricated on the Si-face [76]. Thus, it has been reported that a combination of surface etching by H₂, suppression of SiC oxidation, and interface nitridation is effective in forming a high-quality SiC MOS interface.

1.4.2 Reliability

Positive and Negative Bias Instability

In addition to low μ_{channel} , the threshold voltage (V_{th}) instability is another critical issue [31, 78, 79]. Figure 1.7 shows the schematic band diagrams and schematics of capacitance–voltage (C – V) characteristics of a p-type MOS capacitor and the drain current–gate voltage (I_{D} – V_{G}) characteristics of an inversion-type n-channel MOSFET under (a) positive and (b) negative gate bias stress. When a positive bias is applied, electrons are trapped in oxide defects, acting as negative fixed charges. This causes a positive drift in the flatband voltage (V_{FB}). Since V_{th} directly correlated to V_{FB} , it also drifts positively, making it difficult to uniquely determine the on-state gate voltage for device operation. In addition, the positive drift of V_{th} leads to a lower drain current at a given gate voltage, resulting in an increased on-resistance. In contrast, under negative bias stress, holes are trapped in oxide defects and behave as positive fixed charges. This results in a negative drift of the C – V and I_{D} – V_{G} characteristics. This negative drift can cause normally-on operation, leading to serious reliability issues. Furthermore, additional defects can be generated under a strong oxide electric field, which also causes drifts in the device characteristics [80, 81].

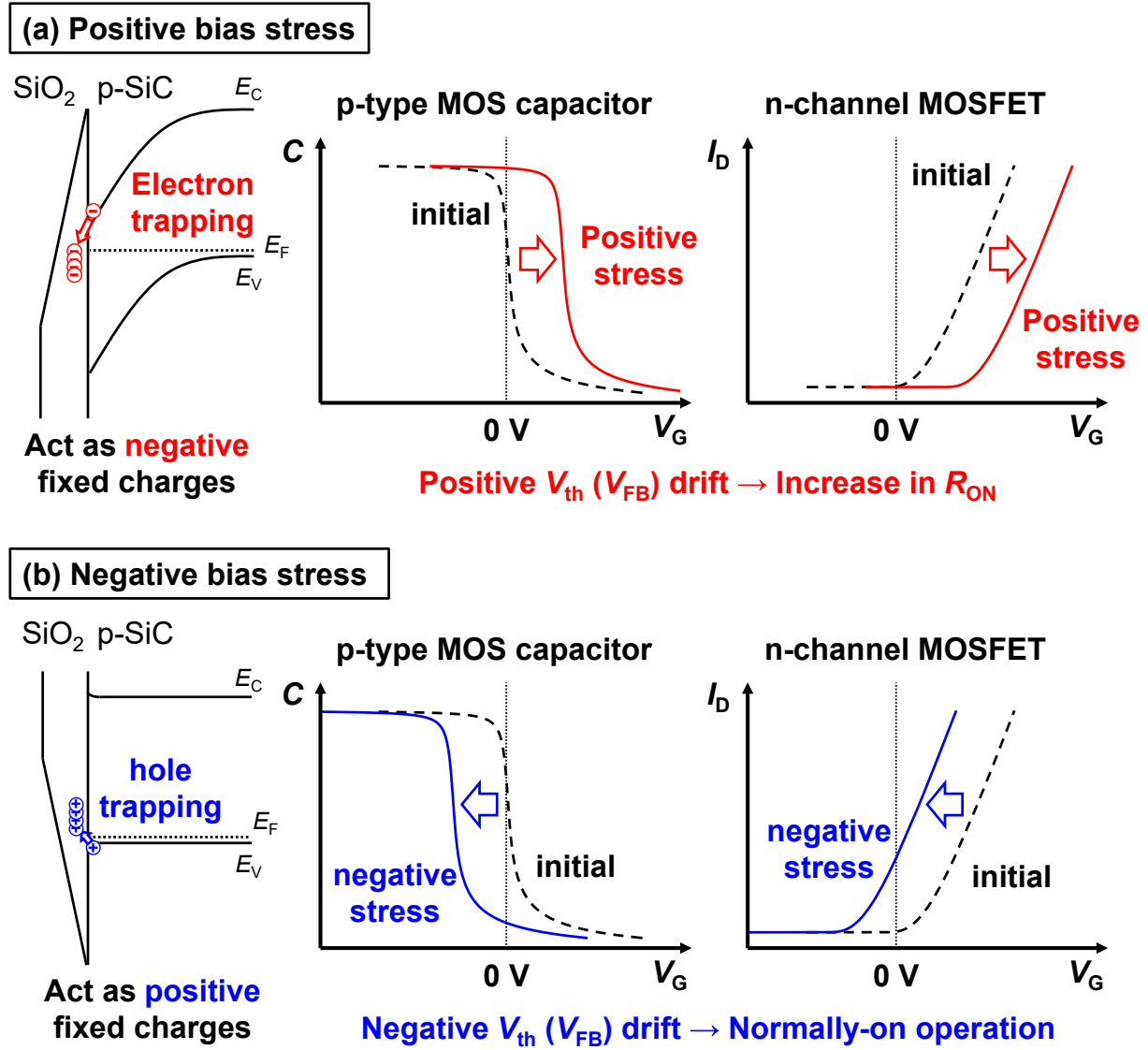


Figure 1.7. Schematic illustrations of the band diagrams of the SiO₂/SiC interface, the $C-V$ characteristics of a p-type MOS capacitor, and the I_D-V_G characteristics of an inversion-type n-channel MOSFET under (a) positive and (b) negative stress bias. Under positive bias, the $C-V$ and I_D-V_G characteristics moves to the positive direction, resulting in an increased on-resistance. In contrast, under negative bias, V_{FB} and V_{th} drift in the negative direction, leading to normally-on operation.

The thermally grown SiO_2/SiC structure is known to contain a high density of oxide traps [65], which enhances V_{th} drift under positive bias stress. By applying an oxide electric field of $\pm 3 \text{ MVcm}^{-1}$, the thermally oxidized SiC MOSFET exhibits a significant positive V_{th} drift [31]. Although the positive bias instability of the thermally oxidized sample can be improved by NO annealing, nitrided SiC MOS devices exhibit poor negative bias instability, showing a significantly large V_{FB} drift under negative gate bias [65, 82]. In addition, both positive and negative bias instabilities are pronounced in NO-nitrided SiC MOS devices fabricated on non-basal planes [72, 83], which are promising for trench-channel applications. As a result of poor reliability of NO-nitrided devices, the maximum oxide field that can be applied under positive or negative gate bias is considerably low [6]. Several studies have reported that the incorporation of P or B also degrades the reliability of SiC MOS devices. P- or B-incorporated SiC MOSFETs exhibit a significant V_{th} drift under gate bias stress especially at elevated temperatures [27, 78]. In contrast, ultra-high-temperature oxidation or CO_2 annealing can enhance the stability of SiC MOS structures [49, 70]. Therefore, although introducing foreign atoms into the SiO_2/SiC structure effectively improves μ_{FE} , it inevitably compromises the long-term reliability of SiC MOSFETs, posing a critical challenge for device applications.

Previous studies have suggested that reliability degradation in NO-nitrided SiC MOS devices is attributed to nitrogen atoms introduced near the SiO_2/SiC interface [83, 84]. X-ray photoelectron spectroscopy (XPS) measurements have confirmed that NO annealing incorporates nitrogen atoms on both the SiC and SiO_2 sides of the interface [84]. The reliability tests primarily investigate long-time-constant defects, corresponding to oxide defects rather than interface defects. This suggests that nitrogen on the SiO_2 side of the interface is likely responsible for the reliability, and a correlation between reliability degradation and the nitrogen amount in the oxide has indeed been observed [65, 84]. In Si MOSFETs, nitridation is known to degrade negative bias temperature instability [85, 86]. Despite the differences in band alignment, similar nitrogen-related defects in the SiO_2 layer of SiC MOSFETs may act as carrier traps, leading to the reliability degradation. Therefore, the introduction of nitrogen atoms into the oxide should be carefully controlled or avoided in terms of reliability.

Gate Leakage Characteristics

The gate leakage characteristic of MOS devices is an important reliability metric that determines the maximum voltage apply to the gate electrode. While the gate current does not flow at low gate voltages because an insulator exists between the metal and the semiconductor, leakage current is observed under high gate voltages. Figure 1.8 shows a schematic band diagram of the SiO_2/SiC interface under a high oxide electric field. Under such this condition, the energy bands in the oxide have a downward slope,

forming the triangular barrier that allows electrons to tunnel from the semiconductor to the metal. This conduction mechanism is known as Fowler-Nordheim (FN) tunneling [87]. The relationship between the FN current density (J_{FN}) and the oxide electric field (E_{OX}) is given by [87, 88]

$$J_{\text{FN}} = \frac{e^3 E_{\text{OX}}^2}{16\pi^2 \hbar \Delta E_C} \left(\frac{m_0}{m_e} \right) \exp \left[-\frac{4\sqrt{2m_e} \Delta E_C^3}{3e\hbar E_{\text{OX}}} \right], \quad (1.6)$$

where, e , $\hbar$, ΔE_C , m_0 , and m_e are the elementary charge, the Dirac's constant, the conduction band offset, the free electron mass, and the electron effective mass in the oxide, respectively.

The ΔE_C is the energy difference between the conduction band edges of SiO_2 and SiC as shown in Fig. 1.8, and it determines the onset electric field at which FN tunneling current begins to flow. The onset electric field is also known to depend on crystal orientation, being lower for SiO_2/SiC samples on the a- and m-faces than on the Si-face [72, 83]. This is attributed to the smaller ΔE_C , which leads to poorer reliability for the SiC MOS devices on non-basal-planes.

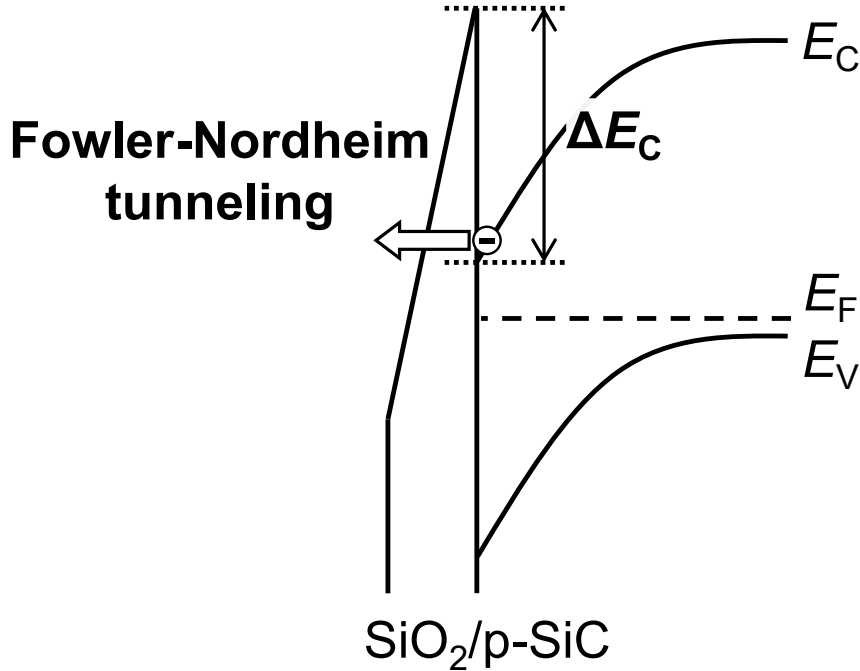


Figure 1.8. Band diagram of the SiO_2/SiC interface under a high oxide electric field. The Fowler-Nordheim (FN) tunneling current through the triangular potential barrier and the conduction band offset (ΔE_C) are shown.

1.5 Objective and Outline of This Thesis

The main objective of this study is to address the reliability issues associated with the conventional NO nitridation technique and to establish guidelines for realizing both high performance and high reliability in SiC MOSFETs. To this end, the following experiments and analyses are conducted.

Chapter 2 investigates the influence of excimer ultraviolet (UV) light irradiation on NO-nitrided and non-nitrided SiO₂/SiC structures fabricated on the Si- and a-faces. The correlation between the nitrogen amount in the SiO₂/SiC structures and the changes in electrical properties are investigated for different NO nitridation times. Based on the obtained results, the origin of reliability degradation in NO-nitrided SiC MOS devices is discussed.

Chapter 3 presents the gate oxide formation process, consisting of plasma nitridation, SiO₂ deposition, and post-deposition annealing (PDA) in CO₂. These processes are employed with the goal of simultaneously achieving low D_{it} and high reliability. SiC MOS capacitors are fabricated on the Si-face to evaluate the impact of the proposed method. D_{it} is evaluated by a high-low method, and the stability of SiO₂/SiC structures is investigated using excimer UV irradiation and electron injection tests. Furthermore, the impact of PDA conditions on interface properties and reliability of SiC MOS devices is systematically investigated.

Chapter 4 demonstrates the improvements in the performance and reliability of SiC MOS devices through two-step annealing in diluted H₂ annealing without interface nitridation. In this process, Ar-diluted H₂ annealing is performed both before and after oxide formation, aiming to remove surface defects and reduce interface defects. Using this approach, SiC MOS capacitors and MOSFETs are fabricated on the Si-face, and D_{it} , device reliability, and μ_{FE} are subsequently characterized. In addition, the concentrations of foreign elements in the SiO₂/SiC structures are evaluated using the SIMS analysis. The effect of the process conditions on device performance and reliability are comprehensively evaluated and analyzed.

Chapter 5 summarizes the major findings of this research.

Chapter 2

Degradation of NO-Nitrided SiC MOS Devices due to Excimer Ultraviolet Irradiation

2.1 Introduction

The current standard SiC MOSFET structure is the trench-type, which eliminates the JFET region and reduces the cell pitch, resulting in lower on-resistance and higher cell density [2]. In trench MOSFETs, the MOS channel is formed on non-basal planes (e.g., a- and m-faces). μ_{FE} of SiC MOSFETs strongly depends on crystal orientation, with a- and m-faces exhibiting higher μ_{FE} than the Si-face [10, 73], which further contributes to lower on-resistance.

However, the reliability of NO-nitrided SiC MOS devices on the a-face degraded with interface nitridation [83]. With a 10-min NO nitridation at 1250°C, SiC MOS devices show minimal V_{FB} drift under gate-bias stress. However, the drift becomes significant when the nitridation time exceeds 30 min. Although this reliability degradation is assumed to originate from nitrogen atoms near the SiO₂/SiC interface [84], a detailed physical model remains unclear.

Meanwhile, UV irradiation has been proposed as a method to have an insight into the origin of the interface defects [89]. In a previous study, SiC substrates were thermally oxidized, and subsequently irradiated with UV light with wavelengths of 193, 221, and 257 nm (corresponding to photon energies of 6.4, 5.6, and 4.8 eV, respectively). Electrical characterizations revealed that electrical degradation occurred when the photon energy exceeded 5–6 eV. Considering the bond breaking energy, double C-C bonds have been suggested to serve as defects activated by UV light. Although UV irradiation was shown to be a useful tool for defect evaluation in the previous study, the sample was fabricated under a limited condition.

Therefore, in this chapter, the reliability degradation induced by NO nitridation is examined by investigating changes in the electrical properties of NO-nitrided $\text{SiO}_2/\text{SiC}(11\bar{2}0)$ structures under excimer UV irradiation. Here, excimer UV light is employed to activate defects under the severe condition. It has a higher photon energy (wavelength of 172 nm) than that used in the previous study [89]. In addition, excimer UV irradiation is conducted on a NO-nitrided sample and an ultra-high-temperature oxidized sample fabricated on the Si-face, as references. Thermal oxidation is typically performed at 1200°C – 1300°C , which often leaves residual carbon at the interface, leading to formation of interface defects. To address this issue, a previous study has carried out oxidation at the higher temperature of 1600°C and reduced the O_2 partial pressure to 0.3% to control the oxidation rate. This approach resulted in a lower D_{it} compared with conventional thermal oxidation [49].

2.2 Experimental Details

The process flow of sample preparation is shown in Figs. 2.1(a) and (b). As shown in Fig. 2.1(a), SiC MOS capacitors were fabricated on n-type $\text{SiC}(11\bar{2}0)$ epilayers with a donor density (N_{D}) of $1.5 \times 10^{15} \text{ cm}^{-3}$. After wet cleaning, a 55-nm-thick gate oxide was formed by dry oxidation at 1200°C , followed by Ar annealing at 1200°C . Then, NO annealing was performed at 1250°C for 10, 30, 60, and 120 min. These samples are referred to as a-NO10, a-NO30, a-NO60, and a-NO120, according to the crystal face and the NO annealing time. Two reference samples were fabricated on n-type $\text{SiC}(0001)$ epilayers ($N_{\text{D}} = (0.8\text{--}1.0) \times 10^{16} \text{ cm}^{-3}$), as shown in Fig. 2.1(b). One is an NO-nitrided sample (Si-NO60), which was fabricated by dry oxidation, Ar annealing, and NO nitridation at 1250°C for 60 min. The other was a high-temperature oxidized sample (Si-HTO), in which dry oxidation was conducted at 1600°C for 3 min in a diluted O_2 atmosphere (0.3%- O_2/Ar). Then, the samples were irradiated with excimer UV light for 10 min at room temperature under vacuum (pressure: $\sim 1 \text{ Pa}$). Excimer UV light, generated from a xenon lamp by radio-frequency (RF) discharge, has a wavelength of 172 nm with a full width at half maximum of 17 nm. Finally, aluminum (Al) gate electrodes were formed to fabricate MOS capacitors.

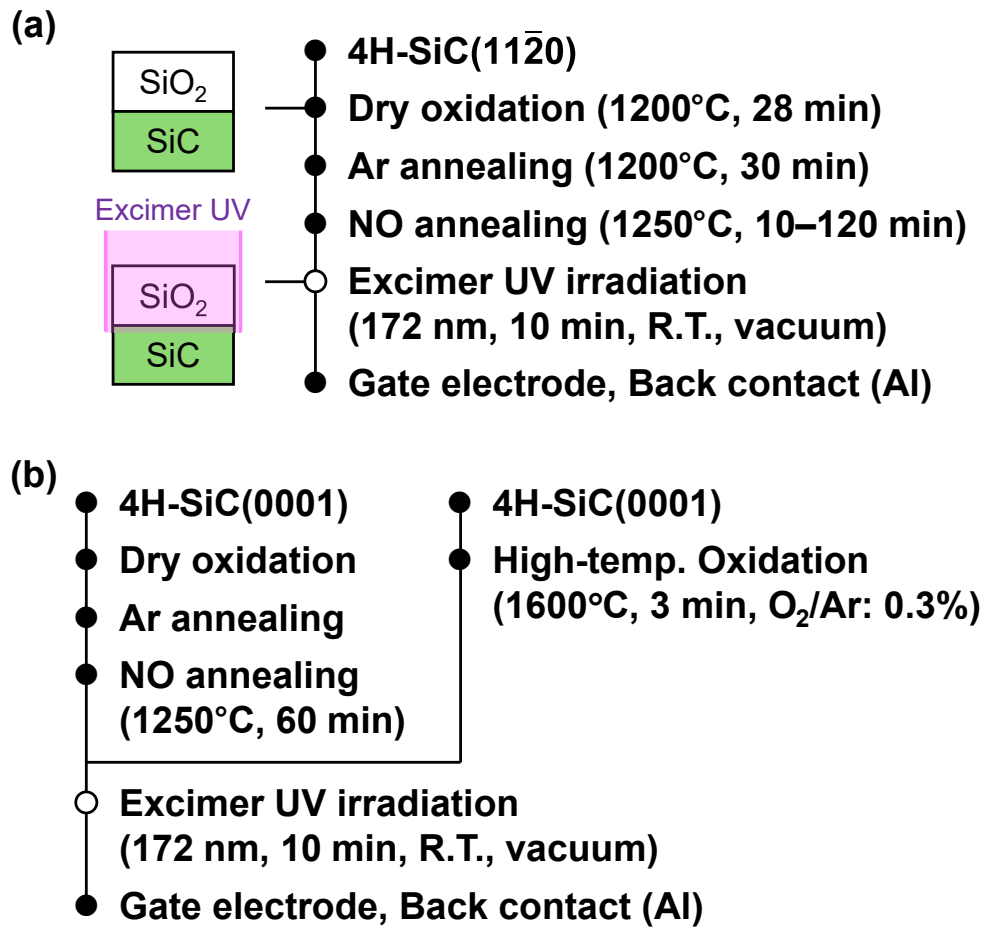


Figure 2.1. Fabrication process of SiC MOS capacitors: (a) a-face and (b) reference Si-face samples.

2.3 SiC MOS Interface Properties

2.3.1 Capacitance–Voltage (C – V) Characteristics

Figure 2.2 shows the bidirectional C – V characteristics of the a-NO60, Si-NO60, and Si-HTO samples. Here, the gate voltage was swept from depletion (negative) to accumulation (positive) and then back to depletion (negative). First, the results of the a-NO60 sample shown in Fig. 2.2(a) are described. Before excimer UV light was irradiated, a slight difference between the forward and backward C – V curves was observed, known as C – V hysteresis. This behavior is observed when electrons trapped at defect states are not released, acting as negative fixed charges and shifting the C – V curve in the positive direction. Focusing on the characteristics of the sample irradiated with excimer UV light, the C – V hysteresis was increased from 0.74 to 6.31 V. Additionally, a plateau appeared in the C – V curves, referred to as a hump. This occurs when electrons are captured by defect states during sweeping the gate voltage, which strongly pins the surface potential and results in constant capacitance. The increase in the C – V hysteresis and the hump indicates that excimer UV irradiation generates both slow and fast electron traps in SiO_2/SiC structures.

Similarly, the C – V hysteresis of the Si-NO60 sample was increased after excimer UV irradiation. In contrast, the Si-HTO sample showed little change in its C – V characteristics. The C – V hysteresis was increased due to excimer UV irradiation from 0.22 to 6.04 V for the Si-NO60 sample and from 0.54 to 0.67 V for the Si-HTO sample. The ultra-high-temperature oxidation process may help reduce carbon-related defects [46, 49], which is likely why no significant electrical degradation [89] was observed in the Si-HTO sample. Since the significant electrical degradation was observed only in the NO-nitrided samples, it seems to be caused by nitrogen atoms. Considering that the energy of excimer UV light is 7.2 eV, which is slightly lower than the SiO_2 band gap of 8.9 eV, UV light is likely to penetrate the SiO_2 layer and interact with the SiO_2/SiC interface. Consequently, the nitridation process would create nitrogen-related defects at or near the interface that can be activated by UV irradiation. It should be noted that, because the pressure was sufficiently low during UV irradiation, the observed electrical degradation is unlikely to result from oxygen (additional oxidation) generated by excimer UV light irradiation.

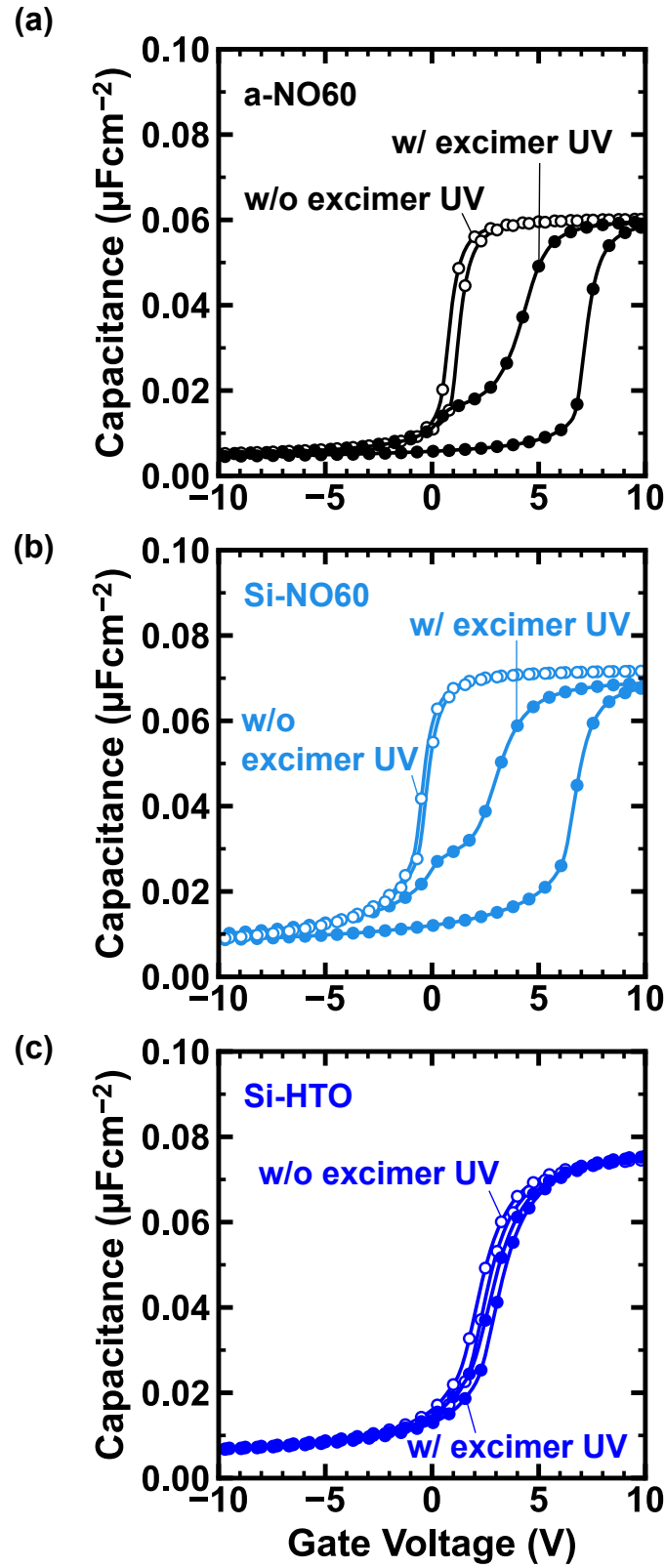


Figure 2.2. Bidirectional $C-V$ characteristics of the (a) a-NO60, (b) Si-NO60, and (c) Si-HTO samples. Open and closed symbols represent samples without and with excimer UV irradiation, respectively.

To investigate the increase in the C - V hysteresis caused by excimer UV irradiation in more detail, the C - V characteristics of the a-NO60 sample were measured twice. Figure 2.3 shows bidirectional C - V characteristics obtained in the first and second sweeps. The gate voltage was swept in a range of -25 to 25 V. The C - V hysteresis observed in the first sweep was 6.31 V, whereas it nearly disappeared (0.34 V) in the second sweep. This result suggests that once electrons are captured at defect states, they are not emitted even when negative gate bias is applied. Therefore, the defects responsible for the increase in C - V hysteresis are likely to have a long time constant (e.g., oxide traps).

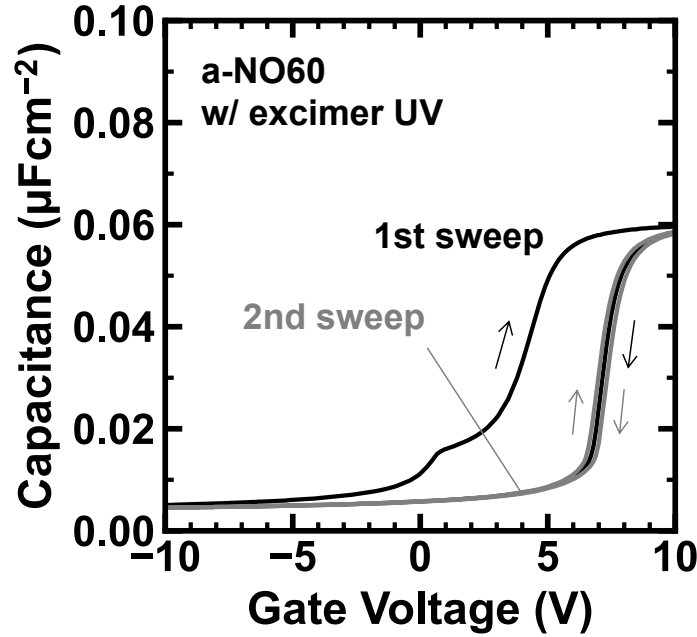


Figure 2.3. Bidirectional C - V characteristics obtained from the a-NO60 sample irradiated with excimer UV light for the first and second sweeps of gate voltages.

2.3.2 Energy Distributions of Interface State Density (D_{it})

To quantitatively characterize the interface properties, D_{it} was evaluated by a high (1 MHz)-low method. Figure 2.4 depicts energy distributions of D_{it} obtained from the a-NO60, Si-NO60, and Si-HTO samples. NO-nitrided samples (a-NO60 and Si-NO60) exhibited relatively low D_{it} compared to the non-nitrided sample (Si-HTO) when samples were not irradiated with excimer UV light. This indicates the effectiveness of nitridation in reducing interface states. In contrast, D_{it} was increased due to excimer UV irradiation only in the NO-nitrided samples, which means that excimer UV irradiation generates interface states near the E_C in NO-nitrided samples.

Figure 2.5 shows the NO annealing time dependence of D_{it} at $E_C - E = 0.5$ eV for samples fabricated on the a-face (a-NO10–120). Without excimer UV irradiation,

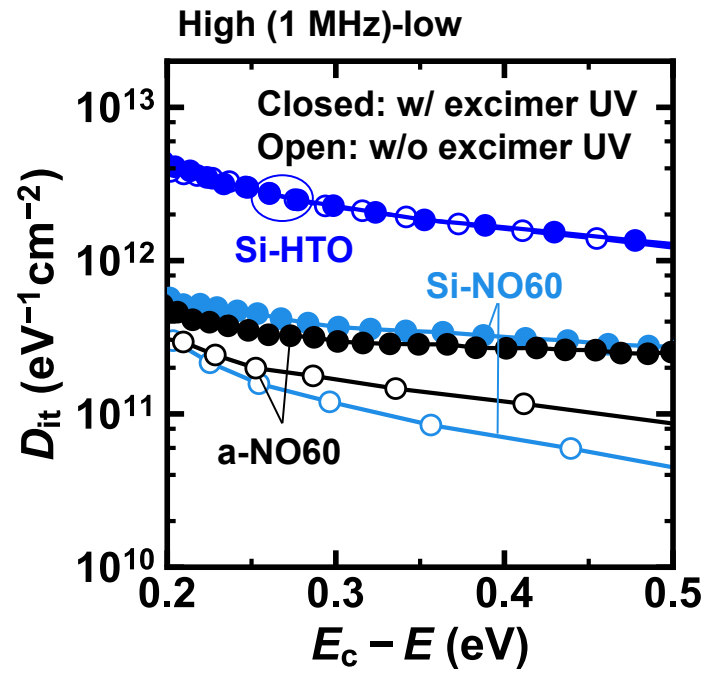


Figure 2.4. Energy distributions of D_{it} calculated using a high (1 MHz)-low method for the a-NO60, Si-NO60, and Si-HTO samples. Open and closed symbols correspond to the samples without and with excimer UV irradiation, respectively.

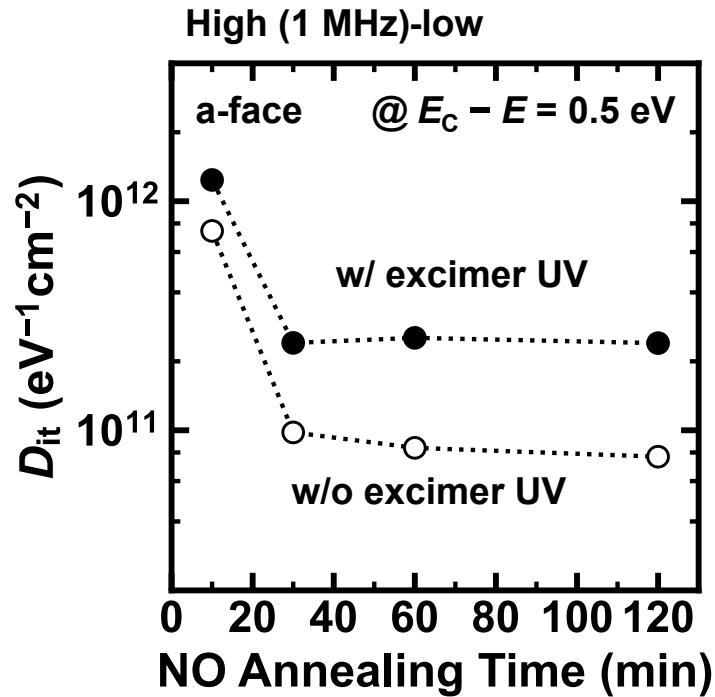


Figure 2.5. NO annealing time dependence of D_{it} at $E_c - E = 0.5$ eV, obtained from the a-NO10–120 samples.

D_{it} values decreased from 7.4×10^{11} to $9.8 \times 10^{10} \text{ eV}^{-1}\text{cm}^{-2}$ as the NO annealing time increased from 10 to 30 min, indicating that long NO annealing effectively passivates interface defects. However, the passivation effect saturated when the annealing time exceeds 30 min. This tendency is consistent with the amount of nitrogen [65], indicating that, although nitrogen incorporation is an effective way to passivate interface defects, the passivation effect saturates after the incorporated nitrogen reaches a certain amount. After excimer UV irradiation, in samples with low nitrogen content during the early stage of nitridation, the increase in D_{it} is small, while in samples with nearly saturated nitrogen content, the increase becomes constant. For example, the D_{it} value of the a-NO60 sample was increased from 8.4×10^{10} to $2.5 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$ due to excimer UV irradiation. These results indicate that excimer UV irradiation activates defects and that the activated defects create interface states near the E_C . That is, NO nitridation is likely to form precursors of nitrogen-related defects that can be easily activated by UV irradiation.

2.3.3 C – V Characteristics Under UV Illumination

Next, the author investigated the impact of excimer UV irradiation on characteristics near the E_V . Since 4H-SiC is a wide bandgap semiconductor, the hole density at room temperature is extremely low in n-type SiC. Therefore, when a negative gate bias is applied to an n-type SiC MOS capacitor, a depletion layer is formed. In a previous study, UV light (wavelengths: 250–450 nm) with energy exceeding the bandgap of SiC was irradiated onto n-type SiC MOS capacitors during C – V measurements to evaluate the characteristics near the E_V [82]. This UV illumination generates electron-hole pairs around gate electrodes, enabling the supply of holes at the MOS interface under negative gate bias and allowing the observation of hole accumulation. Since the SiO_2/SiC interface is covered with the Al gate electrode, additional degradation of the MOS interface [89] during the measurements is negligible. In this experiment, a Spot Cure SP-9 (USHIO Inc.) was used as a UV light source.

Figure 2.6 shows 1 kHz C – V characteristics under UV illumination obtained from the a-NO60 and Si-HTO samples. It should be noted that the energy of UV light used during C – V measurements differs from that of excimer UV light. Focusing on the C – V characteristics without excimer UV irradiation, both samples showed clear hole accumulation under negative gate bias. In addition, negligible C – V hysteresis was observed at the negative side of the gate voltage, indicating a low density of hole traps. With excimer UV irradiation, C – V hysteresis under negative gate voltages increased in the a-NO60 sample. In contrast, the change in C – V characteristics was little for the Si-HTO sample. These results suggest that excimer UV irradiation activates defects in the NO-nitrided SiO_2/SiC structure and creates interface states not only near the E_C , but also near the E_V .

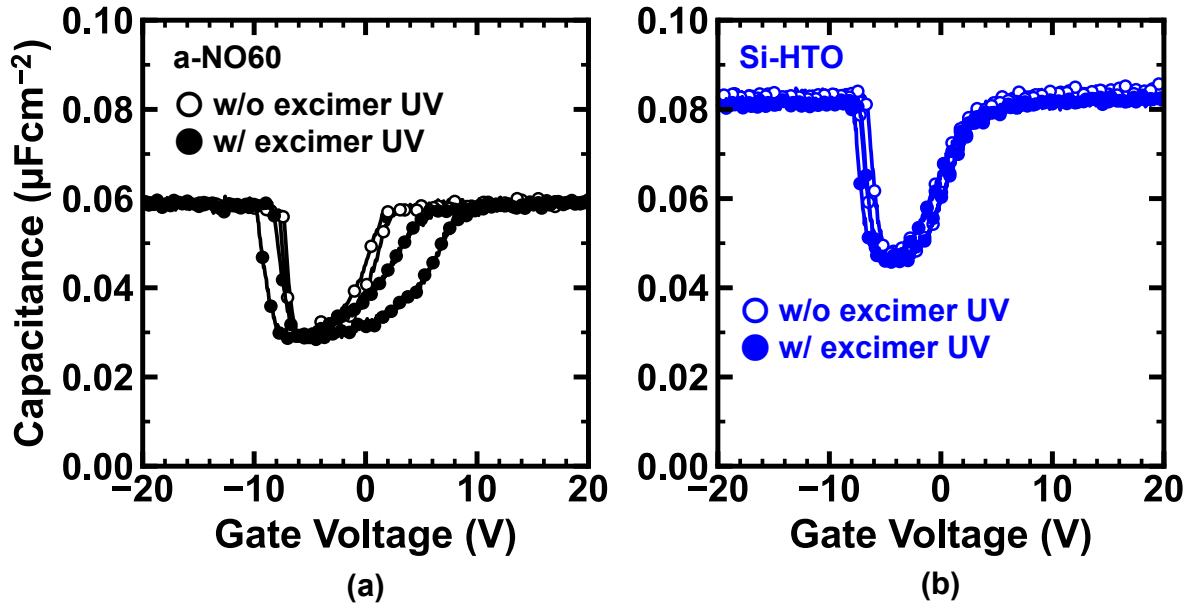


Figure 2.6. Bidirectional C - V characteristics measured at 1 kHz for (a) a-NO60 and (b) Si-HTO samples. During the measurement, UV light with wavelengths of 250–450 nm was irradiated onto the MOS capacitor to generate electron-hole pairs around the gate electrode. Under negative gate bias, hole accumulation can be observed using n-type SiC MOS capacitors.

2.4 Reliability

2.4.1 Procedure of Stress Test

In the following, the impact of excimer UV irradiation on the reliability of the MOS structures was investigated. To assess the reliability of SiC MOS structures, a positive bias stress test was conducted. Figure 2.7 schematically illustrates the procedure of the stress test. First, C - V characteristics were measured twice, and positive bias stress and C - V measurements were repeated. In these measurements, a constant voltage corresponding to a stress oxide field ($E_{\text{OX, stress}}$) of $+6 \text{ MVcm}^{-1}$ was applied to the gate electrode. $E_{\text{OX, stress}}$ was calculated as follows:

$$E_{\text{OX, stress}} = \frac{V_G - V_{\text{FB}}}{t_{\text{OX}}}, \quad (2.1)$$

where t_{OX} is the oxide thickness calculated from the oxide capacitance (C_{OX}). V_{FB} was determined from $1/C^2$ - V_G plots by extracting a intercept and a slope from the following equation:

$$\frac{1}{C^2} = \frac{1}{C_{\text{OX}}^2} + \frac{2(V_G - V_{\text{FB}})}{e\varepsilon_{\text{SiC}}N_D}. \quad (2.2)$$

Here, ε_{SiC} denotes the permittivity of SiC. The V_{FB} drift (ΔV_{FB}) was calculated from the change in V_{FB} before and after the bias stress. Typical results of the C - V characteristics

for the a-NO60 sample are shown in Fig. 2.7. Here, the gate bias stress was applied to the gate electrode for 1–2000 s, and the gate voltage was swept from accumulation to depletion. A positive drift of the C – V curves was observed, indicating electron trapping.

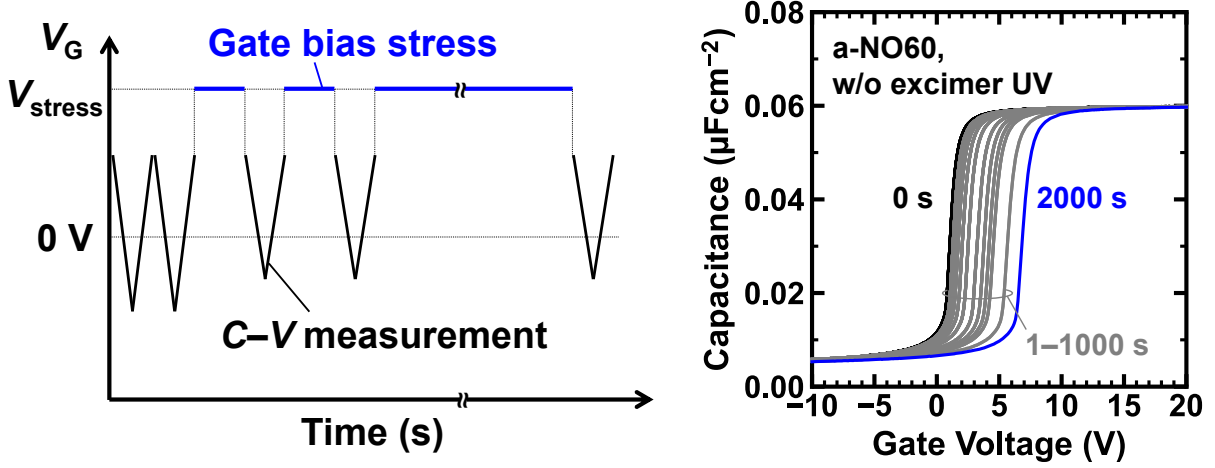


Figure 2.7. Measurement flow of the positive bias stress test and the typical result of the C – V characteristics obtained from the a-NO60 sample during the stress test.

2.4.2 Stress Time Dependence of Flatband Voltage Drift

Figure 2.8 shows the stress time dependence of ΔV_{FB} obtained from the fabricated SiC MOS capacitors. ΔV_{FB} was low in the a-NO10 sample, while it increased as the NO annealing time increased. Therefore, these results suggest that, for the a-face samples, prolonged nitridation forms oxide traps in the SiO_2/SiC structure. However, nitridation longer than 30 min is necessary to effectively reduce D_{it} (Fig. 2.5), and this trade-off remains a key challenge. Conversely, the Si-NO60 and Si-HTO samples showed relatively low ΔV_{FB} , in agreement with previous reports [49, 82].

Even with the same NO nitridation time of 60 min, the a-NO60 sample exhibits a larger ΔV_{FB} compared to the Si-NO60 sample, indicating the poor reliability of the non-basal plane samples [83]. Under excimer UV irradiation, ΔV_{FB} was significantly increased in NO-nitrided samples fabricated on both the a- and Si-faces. An increase in ΔV_{FB} was observed even with 1 s of stress, and it increased substantially with longer stress times for all NO-nitrided samples (a-NO10–120 and Si-NO60). For example, the ΔV_{FB} value of the a-NO60 sample after 2000 s of stress increased from 5.7 to 13.3 V by excimer UV irradiation. However, the Si-HTO sample showed only minimal changes (0.8 to 1.3 V), showing high stability against electron injection and excimer UV irradiation, which is likely due to the absence of nitrogen atoms. These results strongly suggest that defects activated by excimer UV irradiation are nitrogen-related.

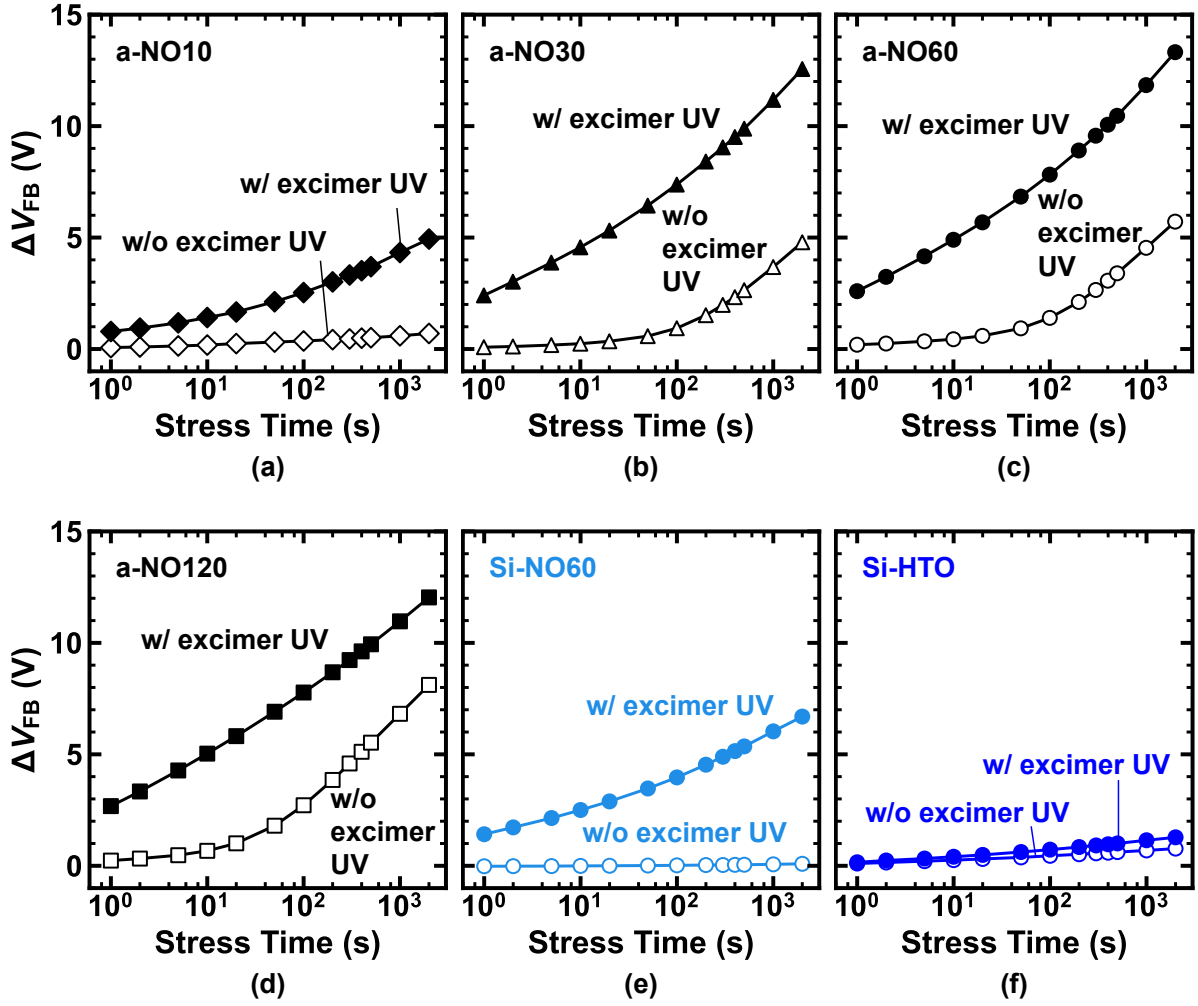


Figure 2.8. Stress time dependence of ΔV_{FB} for (a) a-NO10, (b) a-NO30, (c) a-NO60, (d) a-NO120, (e) Si-NO60, and (f) Si-HTO samples. The applied gate voltage corresponded to $E_{OX, stress}$ of $+6 \text{ MVcm}^{-1}$. Open and closed symbols represent the samples without and with excimer UV irradiation, respectively.

2.5 Discussion

This section explores the impact of excimer UV irradiation on reliability, considering its correlation with the nitrogen amount. Figure 2.9(a) shows NO annealing time dependence of ΔV_{FB} after 2000 s of stress and normalized XPS intensities (I_{N1s}/I_{Si2p}) for NO-nitrided SiO₂/SiC samples fabricated on the a-face. Here, XPS intensities on the SiC side of the interface (N_{SiC}) was obtained after SiO₂ was fully etched by hydrofluoric acid (HF) solutions, thus corresponds to the nitrogen content on the SiC surface. The corresponding value on the SiO₂ side of the interface (N_{SiO2}) was determined by subtracting N_{SiC} from the I_{N1s}/I_{Si2p} of the SiO₂/SiC sample with a SiO₂ layer of 1.5 nm, reflecting the amount of nitrogen incorporated on the SiO₂ side of the interface. ΔV_{FB} increased with increasing NO annealing time in the samples without excimer UV irradiation. In these samples, the ΔV_{FB} values after 2000 s of stress were 0.7, 4.8, 5.7, and 8.1 V for NO nitridation times of 10, 30, 60, and 120 min, respectively. When excimer UV light was irradiated, ΔV_{FB} was increased as the NO annealing time increased from 10 to 30 min, and saturated after annealing time of 30 min. The ΔV_{FB} values for NO nitridation times of 10, 30, 60, and 120 min were 4.9, 12.6, 13.3, and 12.0 V, respectively. Figure 2.9(b) depicts ΔV_{FB} as a function of N_{SiO2} . Here, reliability tests primarily evaluate oxide traps, and thus, ΔV_{FB} is compared with N_{SiO2} in this study. A clear correlation was observed between ΔV_{FB} and N_{SiO2} , including the Si-NO60 sample. This result indicates that excimer UV irradiation activates nitrogen-related defect precursors in SiO₂.

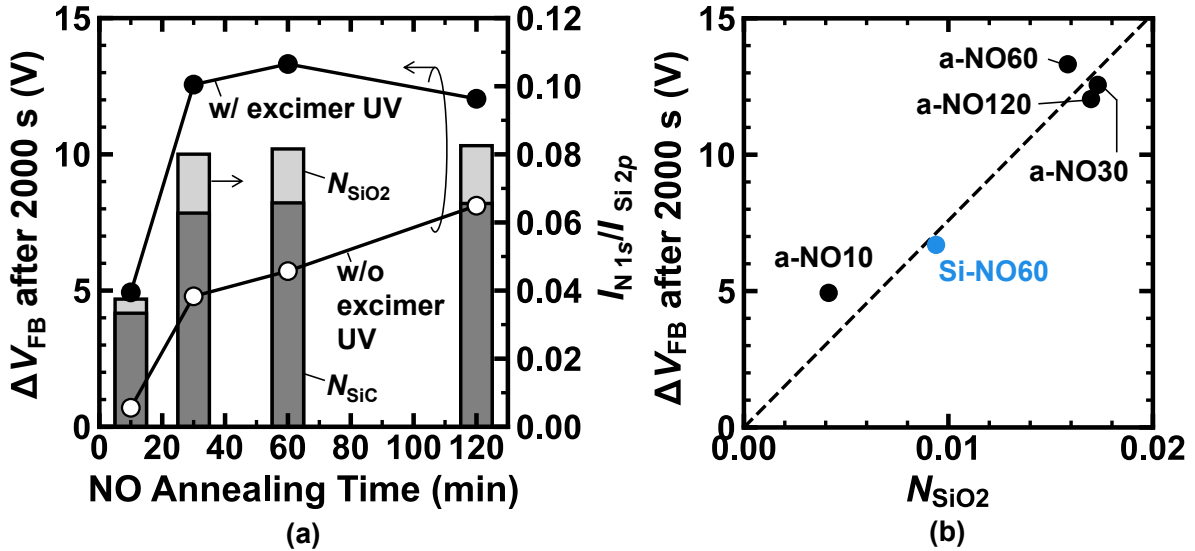


Figure 2.9. (a) NO annealing time dependence of ΔV_{FB} after 2000 s of stress and the XPS intensity (I_{N1s}/I_{Si2p}) corresponding to the nitrogen content on the SiC side (N_{SiC}) and the SiO₂ side (N_{SiO2}) of the interface [90]. (b) ΔV_{FB} after 2000 s of stress as a function of N_{SiO2} . The dashed line is provided as a visual guide.

2.6 Summary

In this chapter, the author investigated the impact of excimer UV irradiation on NO-nitrided SiC MOS devices fabricated on $(11\bar{2}0)$ face and (0001) face. C - V characteristics were dramatically degraded due to excimer UV irradiation for NO-nitrided samples (a-NO10-120 and Si-NO60). On the other hand, excimer UV irradiation had little effect on electrical properties for the non-nitrided sample (Si-HTO). Reliability of SiC MOS devices were also evaluated, and a significant increase in ΔV_{FB} was observed in NO-nitrided samples. The degradation in reliability was discussed based on the relationship between ΔV_{FB} and the amount of nitrogen measured by XPS. A clear correlation between ΔV_{FB} and the nitrogen amount in SiO_2 was confirmed, indicating that excimer UV irradiation activates nitrogen introduced on the SiO_2 side near the interface. These findings suggest that caution must be taken when using NO-nitrided SiC MOS devices in harsh radiation environments, and a novel defect passivation method, which avoids nitrogen incorporation in the oxide, is necessary to achieve high reliability.

Chapter 3

SiC MOS Interface Engineering via Nitrogen Profile Control With High-Density Nitrogen Plasma

3.1 Introduction

NO annealing is the standard method to reduce interface defects [61–63]. However, several challenges remain with the NO nitridation technique, as follows.

1. Limited nitrogen incorporation on the SiC surface

High-low measurements confirmed that D_{it} decreases with increasing NO annealing time [65]. However, while the amount of nitrogen increases from the NO nitridation time of 10 to 60 min, it saturates after 60 min [65, 84]. This saturation seems to be due to the balance between nitridation and nitrogen removal by O_2 , a byproduct of NO [66]. Since there is a correlation between D_{it} and the nitrogen amount at the interface [65], incorporating a high nitrogen density is considered an effective way for reducing D_{it} .

2. Incorporation of nitrogen in SiO_2 near the SiO_2/SiC interface

Scanning XPS measurements have revealed that nitrogen is incorporated both on the SiC surface and in SiO_2 near the interface [84]. The nitrogen content in SiO_2 increases with longer NO annealing times, which correlates with a degradation of device reliability [65]. Furthermore, as discussed in Chap. 2, a large number of electron traps exist in SiO_2/SiC structure after excimer UV irradiation, which is also likely to be related to nitrogen in SiO_2 .

Based on the above backgrounds, when interface nitridation is employed, precise control of the nitrogen profile is essential for forming a high-quality SiO_2/SiC interface. Specifically,

a high density of nitrogen atoms should be incorporated only on the SiC side of the interface to passivate interface defects and improve reliability of the SiC MOS structure. Additionally, according to recently proposed oxidation-minimizing processes [74–76], the gate oxide must be formed while suppressing the oxidation of SiC.

In this chapter, a method for forming a nitrated SiO_2/SiC interface, consisting of plasma nitridation of the SiC surface, SiO_2 deposition, and CO_2 -PDA is proposed and interface properties and reliability of the SiC MOS capacitor are compared with those of the conventional NO-nitrated sample. In addition, SiO_2/SiC structures are fabricated by changing the PDA temperature and atmosphere after plasma nitridation and SiO_2 deposition. The effect of PDA conditions on the electrical properties of SiC MOS devices is systematically investigated.

3.2 Gate Oxide Formation Process

Figure 3.1 shows a schematic flow of the gate oxide formation process. The first process is plasma nitridation of the SiC surface. In conventional NO nitridation, NO annealing is performed after SiO_2 formation. However, this approach limits the nitrogen content at the SiO_2/SiC interface [66] and allows some nitrogen to be incorporated on the SiO_2 side of the interface [84, 90]. In contrast, in the proposed method, nitridation is performed before SiO_2 formation. Plasma nitridation is carried out using a system in which the nitrogen plasma is generated with a porous carbon electrode [91, 92]. Although plasma nitridation has been employed in some previous studies [93–95], nitrogen plasma in these previous studies was generated under relatively low pressure. In contrast, nitrogen plasma is generated under 10.5 Torr in the present study, enabling generation of high-density nitrogen plasma, which may lead to incorporation of a high density of nitrogen atoms.

The second key process is the sputter deposition of SiO_2 . Since oxidation of SiC likely leads to the formation of carbon-related defects at the SiO_2/SiC interface [40, 41], recent studies have employed plasma enhanced CVD (PECVD) for SiO_2 deposition to suppress oxidation of SiC [75, 76]. While PECVD can deposit SiO_2 layers with favorable properties, sputtering in a pure Ar atmosphere is also an effective method for suppressing the oxidation of SiC.

The final key process is CO_2 -PDA. The deposited SiO_2 layer likely contains oxygen vacancies, which should be passivated by annealing in an oxidant. O_2 annealing is usually used to passivate those defects, but it simultaneously oxidizes the SiC surface, which may lead to unwanted carbon-related defects [40, 41]. Previous studies have shown that CO_2 annealing can reduce oxygen vacancies [70, 96] while suppressing the oxidation of SiC because CO_2 has a higher activation energy for SiC oxidation (7.5 eV) than O_2 (2.9 eV) [70]. Therefore, in this study, CO_2 -PDA is used to reduce oxide defects while

minimizing the oxidation of SiC. Furthermore, this chapter investigates whether a CO₂ atmosphere is necessary and how the annealing temperature affects the interface properties and reliability.

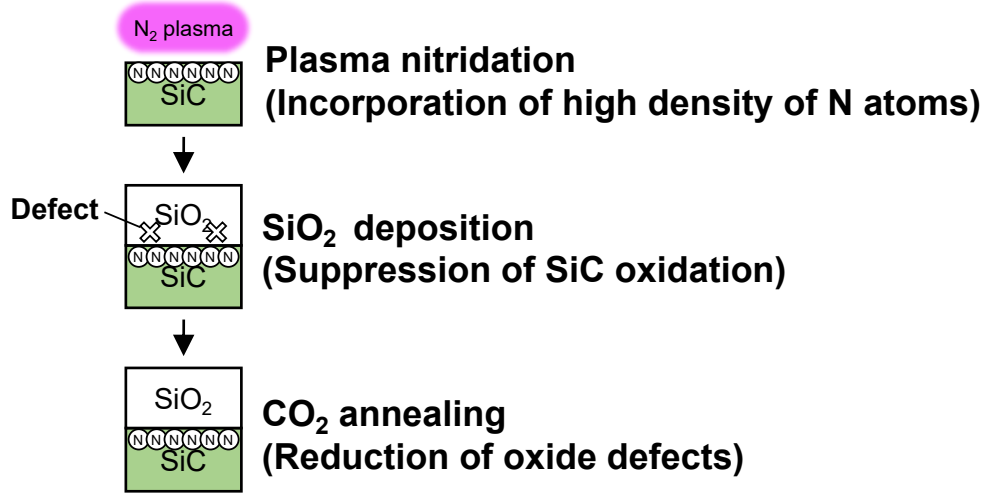


Figure 3.1. A schematic illustration of the gate oxide formation process consisting of plasma nitridation, SiO₂ deposition, and CO₂ annealing.

3.3 Experimental Procedure

Figure 3.2 shows the process flow for sample preparation. This study used n-type SiC(0001) epilayers with N_D of $1.0 \times 10^{16} \text{ cm}^{-3}$. First, the SiC surface was nitrided using high-density nitrogen plasma. The plasma nitridation conditions were set as follows: substrate temperature of 350°C, exposure time of 30 min, N₂ flow rate of 1.5 sccm, pressure of 10.5 Torr, RF power of 50 W, and the gap between the electrode and the substrate of 0.8 cm. Next, a 45-nm-thick SiO₂ dielectric layer was deposited using a sputtering method, using Ar as the sputter gas and SiO₂ as the target. The sputtering was performed under Ar pressure of 0.3 Pa, flow rate of 8 sccm, and RF power of 100 W. Then, PDA was performed in CO₂ atmosphere at 1250°C for 30 min. This sample is labeled as “Npla.-depo.-CO₂(1250°C).” In addition, samples without plasma nitridation (depo.-CO₂(1250°C)) and without CO₂-PDA (Npla.-depo.) were also fabricated. A reference sample fabricated by oxidation at 1200°C, followed by Ar annealing at 1200°C and NO annealing at 1250°C for 60 min (Ox.-NO), was also prepared. To evaluate the nitrogen amount incorporated on the SiC surface, SiO₂ was fully etched by 10% HF solutions, and XPS measurements were conducted. The excitation energy and the take-off-angle were 1486.6 eV and 90°, respectively. Meanwhile, to assess the reliability of SiO₂/SiC structures, excimer UV light with a wavelength of 172 nm was irradiated for 10 min at

PDA at 1050°C is labeled as “Npla.-depo.-CO₂(1050°C)”). To evaluate the effect of CO₂ ambient, a reference sample subjected to Ar-PDA at 1250°C for 30 min was also prepared (Npla.-depo.-Ar(1250°C)). Finally, Al gate electrodes were formed, and MOS capacitors were fabricated.

3.4 Nitrogen Content on a SiC Surface

Figure 3.4 shows the XPS spectra of (a) Si 2*p* and (b) N 1*s* core levels for Npla.-depo.-CO₂(1250°C) and Ox.-NO samples. Both Si 2*p* and N 1*s* signals were normalized using the Si 2*p* intensity, which corresponds to the Si-C component at 101.8 eV. Since the SiO₂ layer was completely removed by the HF solution, no Si-O related peaks were observed, and only signals from the SiC bulk remained. Consequently, the N 1*s* spectrum in Fig. 3.4(b) can be attributed exclusively to nitrogen atoms on the SiC surface.

Distinct N 1*s* peaks were observed for both the Npla.-depo.-CO₂(1250°C) and NO samples, indicating nitrogen incorporation on the SiC surface. The Npla.-depo.-CO₂(1250°C) sample exhibited about three times higher intensity than the Ox.-NO sample. It should be noted that CO₂ annealing reduces the amount of nitrogen [97]. Although CO₂-PDA was carried out in the Npla.-depo.-CO₂(1250°C) sample, the N 1*s* intensity remained high. This result indicates that plasma nitridation prior to SiO₂ deposition is more effective than NO annealing for introducing nitrogen atoms on the SiC surface.

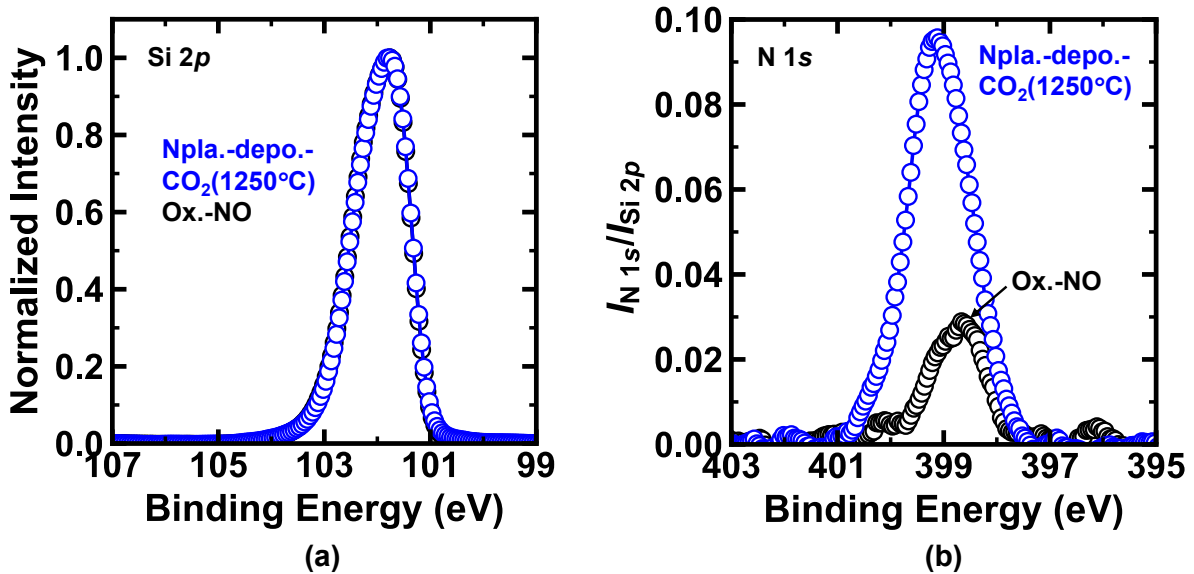


Figure 3.4. (a) Si 2*p* and (b) N 1*s* core level spectra obtained from the Npla.-depo.-CO₂(1250°C) and Ox.-NO samples. The intensities are normalized with the Si-C peak in the Si 2*p* spectrum. Before the XPS measurement, the SiO₂ layer was fully etched using 10%-HF.

3.5 SiC MOS Interface Properties

3.5.1 C – V Characteristics

3.5.1.1 Impact of Plasma Nitridation

Next, the electrical properties of the fabricated SiC MOS capacitors are described. Figure 3.5 shows bidirectional C – V characteristics of the Npla.-depo.-CO₂(1250°C), Npla.-depo., depo.-CO₂(1250°C), and Ox.-NO samples. Significant stretch-out and C – V hysteresis were observed in depo.-CO₂(1250°C) and Npla.-depo. samples. In the Npla.-depo. sample, the measured capacitance remained below the expected accumulation capacitance, indicating significant electron trapping. The fact that the Npla.-depo. sample exhibited degraded C – V characteristics indicates that either sputtered SiO₂ contains a high density of electron traps or traps are generated by plasma treatment. In contrast, the Npla.-depo.-CO₂(1250°C) and Ox.-NO samples exhibited steep C – V characteristics. Compared with the Ox.-NO sample, the C – V hysteresis was smaller in the Npla.-depo.-CO₂(1250°C) sample. The estimated charge densities associated with the C – V hysteresis was 1.3×10^{10} and $9.9 \times 10^{10} \text{ cm}^{-2}$ for the Npla.-depo.-CO₂(1250°C) and Ox.-NO samples, respectively. However, the C – V curves are shifted in the negative direction, which is likely due to positive fixed charges.

The C – V characteristic of the Npla.-depo.-CO₂(1250°C) sample is then compared with the ideal C – V curve. The ideal semiconductor capacitance is described by the following equation [98]:

$$C_{D, \text{theory}}(\psi_S) = \frac{eSN_D \left| \exp\left(\frac{e\psi_S}{kT}\right) - 1 \right|}{\sqrt{\frac{2kTN_D}{\varepsilon_{\text{SiC}}} \left[\exp\left(\frac{e\psi_S}{kT}\right) - \frac{e\psi_S}{kT} - 1 \right]}}, \quad (3.1)$$

where S , ψ_S , k , and T are the pad area, surface potential, Boltzmann constant, and absolute temperature, respectively.

Figure 3.5(b) presents 1 MHz C – V characteristics of the Npla.-depo.-CO₂(1250°C) sample in comparison with an ideal curve, which was calculated using N_D , thickness of SiO₂, and ideal V_{FB} values of $1.0 \times 10^{16} \text{ cm}^{-3}$, 45 nm, and 0.22 V, respectively. Additionally, the C – V curve shifted by -3.1 V from the ideal curve is also shown. The measured 1 MHz C – V curve agreed well with the shifted ideal curve, indicating that the proposed method effectively reduces the interface defects.

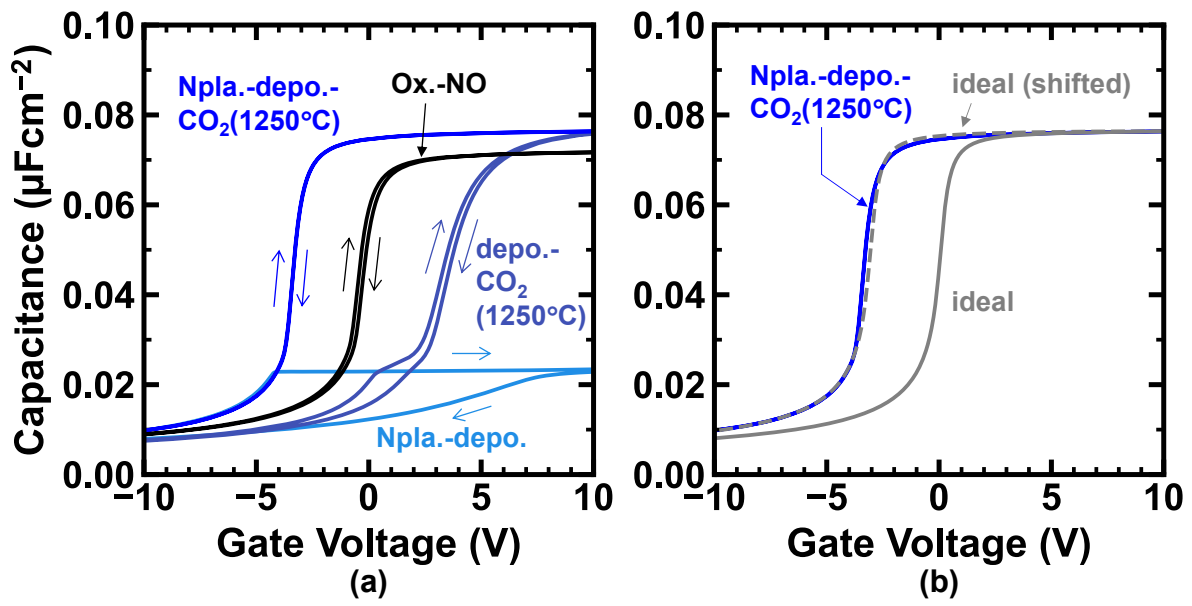


Figure 3.5. (a) Bidirectional 1 MHz $C-V$ characteristics of the Npla.-depo.-CO₂(1250°C), Npla.-depo., depo.-CO₂(1250°C), and Ox.-NO. samples. (b) $C-V$ characteristics of the Npla.-depo.-CO₂(1250°C) sample measured by sweeping the gate voltage from depletion to accumulation. The ideal curve and the curve shifted by -3.1 V are also shown.

3.5.1.2 Role of Post-Deposition Annealing Temperature and Atmosphere

Figure 3.6 shows the dependence of the PDA temperature and atmosphere on bidirectional 1 MHz C - V characteristics. As already shown in Fig. 3.5(a), a large hump due to electron injection into defects was observed in the Npla.-depo. sample. In contrast, Fig. 3.6(a) shows that Npla.-depo.-CO₂(1050°C) exhibited electron accumulation, indicating that CO₂-PDA effectively reduced the defects. As the CO₂-PDA temperature increased, hump and stretch-out were further reduced. C - V curves were negatively shifted with increasing CO₂-PDA temperatures, suggesting generation of positive fixed charges. The fixed charge densities, calculated from the differences between the measured and ideal V_{FB} of samples annealed in CO₂ at 1050°C, 1150°C, and 1250°C, were $4.8 \times 10^{10} \text{ cm}^{-2}$ (negative), $5.2 \times 10^{10} \text{ cm}^{-2}$ (positive), and $1.7 \times 10^{12} \text{ cm}^{-2}$ (positive), respectively. Figure 3.6(b) compares C - V characteristics of the Npla.-depo.-CO₂(1250°C), Npla.-depo.-Ar(1250°C), and Ox.-NO samples. Regardless of the PDA ambient, PDA at 1250°C effectively improved the C - V characteristics, indicating that thermal annealing plays an essential role in defect reduction.

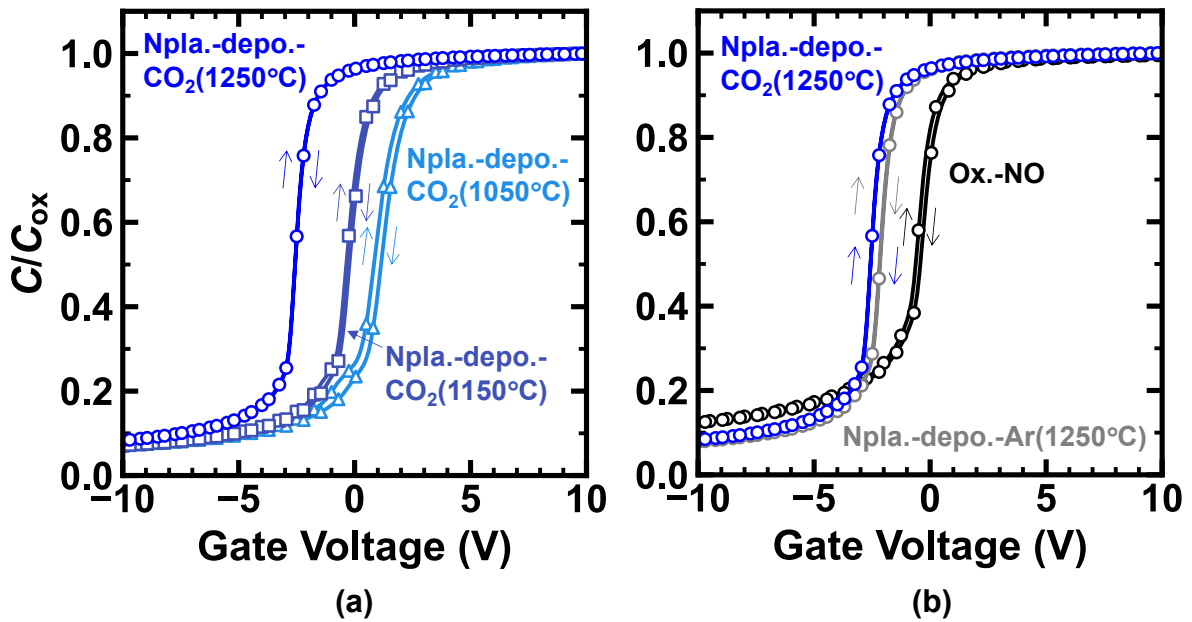


Figure 3.6. Bidirectional C - V characteristics measured at 1 MHz: (a) Npla.-depo.-CO₂(1050°C), Npla.-depo.-CO₂(1150°C), and Npla.-depo.-CO₂(1250°C) samples, and (b) Npla.-depo.-CO₂(1250°C), Npla.-depo.-Ar(1250°C), and Ox.-NO samples. The capacitance is normalized by the C_{ox} .

Next, the impact of PDA conditions on interface properties is quantitatively discussed. In this section, the charge density (Q_{hys}) corresponding to the C - V hysteresis (V_{hys}) was calculated using the following equation:

$$Q_{\text{hys}} = \frac{C_{\text{OX}} \times V_{\text{hys}}}{e}. \quad (3.2)$$

Figure 3.7 indicates Q_{hys} as a function of annealing temperature. C - V hysteresis was evaluated based on the difference in V_{FB} between forward and reverse sweeps. Considering the oxide thickness, the sweep range of gate voltage was set to -10 to 10 V for plasma nitrated samples (Npla.-depo.-CO₂ and Npla.-depo.-Ar) and -20 to 20 V for the Ox.-NO sample. Q_{hys} decreased with increasing CO₂-PDA temperature. The Q_{hys} values were 4.4×10^{11} , 2.4×10^{11} , and $1.4 \times 10^{10} \text{ cm}^{-2}$ for CO₂-PDA temperatures of 1050°C , 1150°C , and 1250°C , respectively. This indicates that high-temperature annealing is effective in passivating defects that contribute to the C - V hysteresis. As a result, Q_{hys} of the Npla.-depo.-CO₂(1250°C) sample was lower than that of the Ox.-NO sample ($9.9 \times 10^{10} \text{ cm}^{-2}$). By contrast, the Npla.-depo.-Ar(1250°C) sample showed insufficient reduction in Q_{hys} , with a value of $3.7 \times 10^{10} \text{ cm}^{-2}$. These results indicate that passivation by CO₂ molecules is necessary for effective defect reduction.

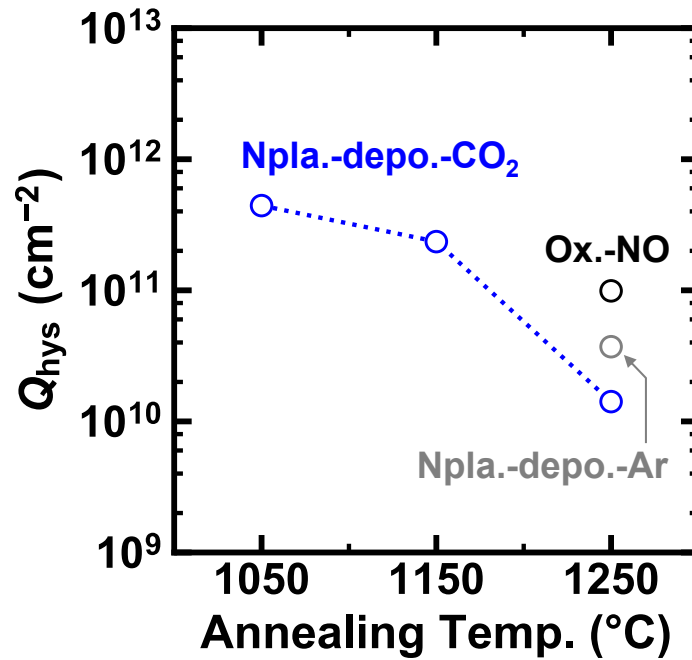


Figure 3.7. Q_{hys} calculated from C - V hysteresis as a function of annealing temperature.

3.5.1.3 Robustness Against Excimer UV Irradiation

Then, the stability of the MOS structures was investigated using excimer UV irradiation as described in Chap. 2. Figure 3.8 shows the bidirectional $C-V$ characteristics of Npla.-depo.-CO₂(1250°C) and Ox.-NO samples with and without excimer UV irradiation. Here, excimer UV light was irradiated prior to the formation of the Al gate electrode. As shown in Fig. 3.8, $C-V$ hysteresis of the Ox.-NO sample increased after excimer UV irradiation. The excimer UV irradiation increased the charge density corresponding to the $C-V$ hysteresis from 9.9×10^{10} to $2.6 \times 10^{12} \text{ cm}^{-2}$ for the Ox.-NO sample. As discussed in Chap. 2, this degradation is likely due to activation of nitrogen atoms by excimer UV irradiation. In contrast, only minor changes in the $C-V$ characteristics were observed for the Npla.-depo.-CO₂(1250°C) sample. The increase in charge density corresponding to the $C-V$ hysteresis was relatively small (from 1.3×10^{10} to $4.8 \times 10^{10} \text{ cm}^{-2}$). This indicates that defect activation due to excimer UV irradiation does not occur in the Npla.-depo.-CO₂(1250°C) sample, probably due to the absence of nitrogen in the SiO₂ layer. These findings indicate that the presented method effectively improves the stability of SiO₂/SiC structures under excimer UV irradiation.

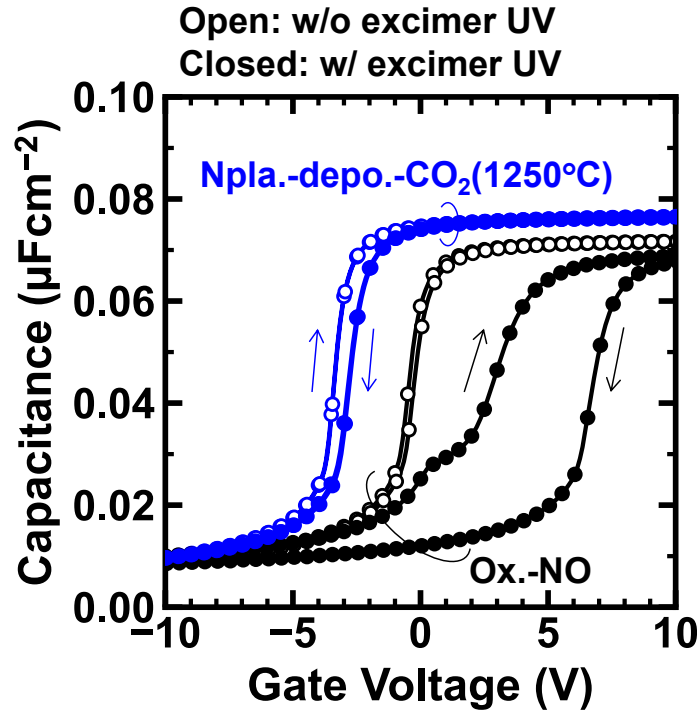


Figure 3.8. Bidirectional 1 MHz $C-V$ characteristics of the Npla.-depo.-CO₂(1250°C) and Ox.-NO samples. Open and closed symbols correspond to the samples without and with excimer UV irradiation, respectively. The excimer UV irradiation was conducted prior to gate electrode formation.

3.5.2 Energy distributions of D_{it}

Figure 3.9 presents D_{it} distributions evaluated by a high (1 MHz)-low method. While relatively high D_{it} values were obtained in the depo.-CO₂(1250°C) sample, a significant reduction in D_{it} was observed in the Npla.-depo.-CO₂(1250°C) sample. This suggests that interface nitridation is essential for the reduction in D_{it} . Notably, D_{it} at shallow energy levels ($E_C - E = 0.2$ – 0.3 eV) of the Npla.-depo.-CO₂(1250°C) sample were lower than those of the Ox.-NO sample. At $E_C - E = 0.2$ eV, the D_{it} values were 1.0×10^{11} and 3.0×10^{11} eV⁻¹cm⁻² for the Npla.-depo.-CO₂(1250°C) and Ox.-NO samples, respectively. This result is likely attributed to the incorporation of the high density of nitrogen atoms on the SiC surface (Fig. 3.4).

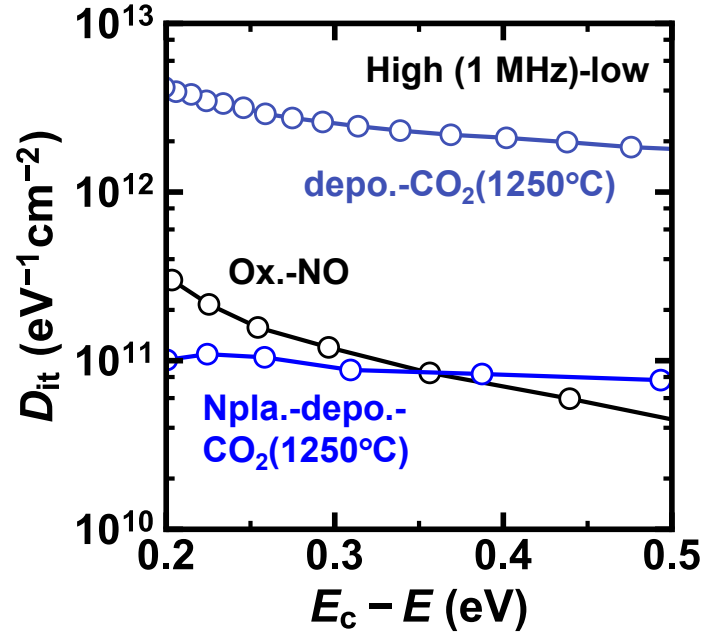


Figure 3.9. Energy distributions of D_{it} obtained from the Npla.-depo.-CO₂(1250°C), depo.-CO₂(1250°C), and Ox.-NO samples. D_{it} was extracted by a high (1 MHz)-low method.

Figure 3.10 compares the energy distributions of D_{it} for samples subjected to different PDA conditions. As the CO₂-PDA temperature increased, D_{it} was reduced. The D_{it} values at $E_C - E = 0.2$ eV were 1.6×10^{12} , 9.3×10^{11} , and 1.2×10^{11} eV⁻¹cm⁻² for the Npla.-depo.-CO₂(1050°C), Npla.-depo.-CO₂(1150°C), and Npla.-depo.-CO₂(1250°C) samples. Here, D_{it} of the Npla.-depo.-CO₂ samples was almost constant with respect to energy, which differs from the typical distribution observed in SiC MOS structures that D_{it} increases toward E_C (e.g., Ox.-NO). According to previous studies [70, 97], D_{it} of the samples subjected to NO and CO₂ annealing increases as the energy approaches E_C . Therefore, such a flat D_{it} distribution is considered to originate from the plasma

nitridation process.

As mentioned already, D_{it} became lower in Npla.-depo.-CO₂(1250°C) sample than in the Ox.-NO sample. In contrast, Ar-PDA had an insufficient impact on reducing D_{it} ($3.2 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$ at $E_C - E = 0.2 \text{ eV}$). Therefore, high-temperature CO₂-PDA is one of the key aspects for D_{it} reduction in the proposed method.

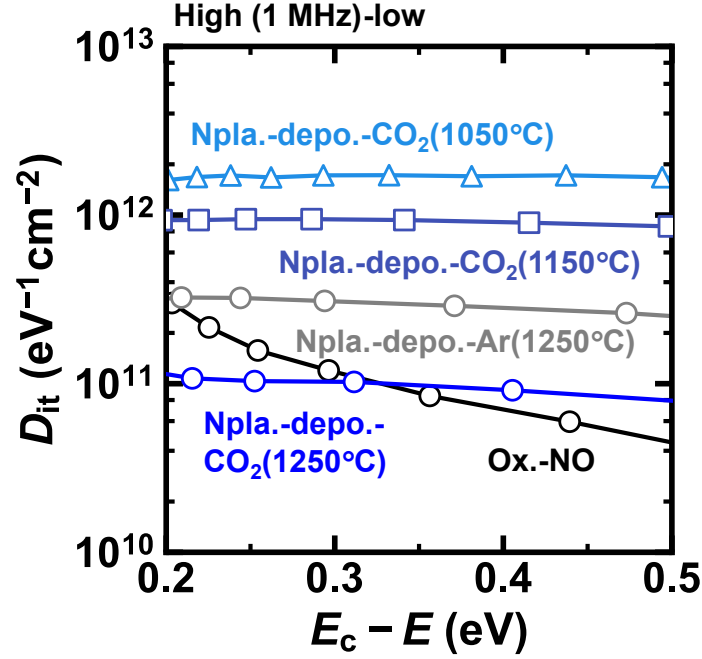


Figure 3.10. Comparison of the energy distributions of D_{it} for the fabricated SiC MOS capacitors.

3.6 Positive Bias Instability

3.6.1 Robustness Against Excimer UV Irradiation

Next, the positive bias instability of the fabricated SiC MOS structures was investigated. First, the effect of excimer UV irradiation on V_{FB} instability under electron injection was investigated. Here, a relatively high gate voltage stress corresponding to $E_{OX, stress}$ of $+7 \text{ MVcm}^{-1}$ was applied for 2000 s to examine the device reliability under severe conditions. During the stress test, $C-V$ curves were repeatedly measured after each stress. The detailed test procedure is described in section 2.4.1.

Figure 3.11 shows ΔV_{FB} as a function of stress time for the Ox.-NO and Npla.-depo.-CO₂(1250°C) samples. Results of the samples with the excimer UV irradiation are also shown. For the Ox.-NO sample, ΔV_{FB} increased with increasing stress time and it reached 2.8 V after 2000 s of stress before excimer UV irradiation. After excimer UV irradiation,

ΔV_{FB} was increased to 1.5 V after just 1 s of stress and even reached 8.4 V after 2000 s of stress. In contrast, ΔV_{FB} remained nearly constant throughout the stress time for the Npla.-depo.-CO₂(1250°C) sample, indicating a low density of electron traps in the oxide. Moreover, the excimer UV irradiation had minimal impact on the device stability. After applying 2000 s of positive bias stress, the ΔV_{FB} value changed only slightly, from 0.1 to 0.3 V. These results indicate that the method proposed in this chapter can form SiO₂/SiC structures with fewer oxide traps compared to NO-nitrided samples. In addition, the SiC MOS structures exhibit high stability against excimer UV irradiation, which is likely attributable to the controlled nitrogen concentration profile, characterized by reduced nitrogen content in the SiO₂ layer.

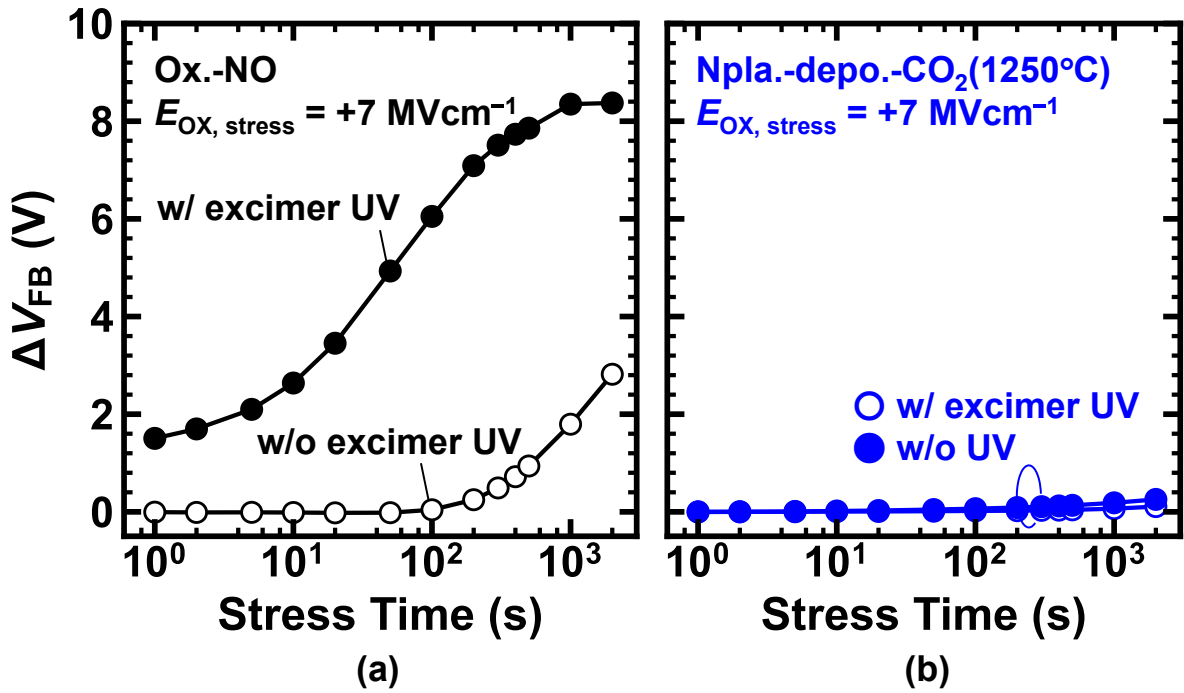


Figure 3.11. Stress time dependence of ΔV_{FB} for the (a) Ox.-NO and (b) Npla.-depo.-CO₂(1250°C) samples. A constant gate voltage corresponding to $E_{OX, stress}$ of +7 MVcm⁻¹ was applied for 2000 s. Open and closed symbols indicate the samples without and with excimer UV irradiation prior to gate electrode formation, respectively.

3.6.2 Measurement Temperature Dependence

The positive bias instability of the Npla.-depo.-CO₂(1250°C) and Ox.-NO samples was then evaluated at elevated temperatures. Here, the measured samples were not irradiated with excimer UV light. The stress tests were conducted at room temperature, 50°C, 100°C, and 150°C with $E_{OX, stress}$ of +7 MVcm⁻¹. Figure 3.12 shows the temperature dependence of ΔV_{FB} after 2000 s of stress. For the Ox.-NO sample, ΔV_{FB} increased from

2.8 V at room temperature to 5.2 V at 150°C. In contrast, the Npla.-depo.-CO₂(1250°C) sample exhibited ΔV_{FB} values of only 0.1 V at room temperature and 0.9 V at 150°C. These results indicate that the proposed method enables the formation of SiC MOS structures stable at high temperatures. In other words, the fabricated MOS devices can operate stably under high-temperature conditions.

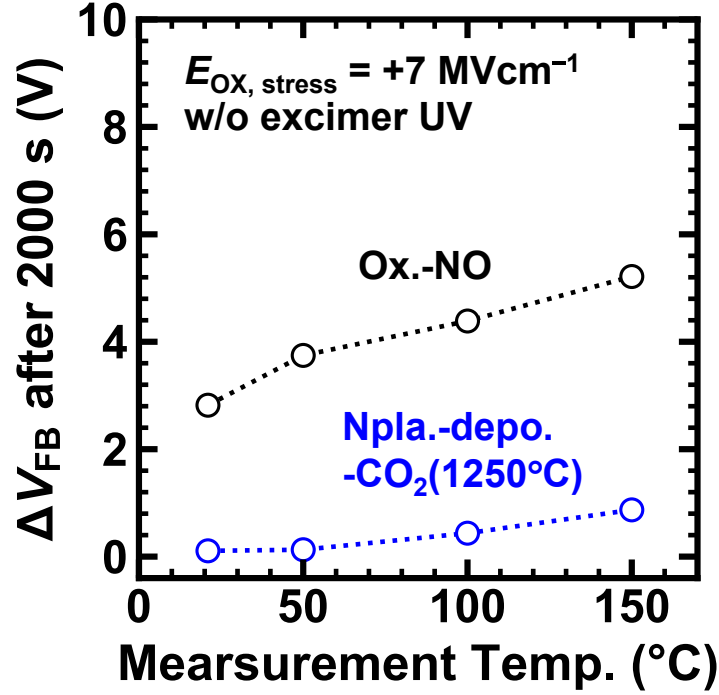


Figure 3.12. Measurement temperature dependence of ΔV_{FB} after 2000 s of gate bias stress for the Npla.-depo.-CO₂(1250°C) and Ox.-NO samples. The samples shown here were not irradiated with excimer UV light.

3.6.3 Role of Post-Deposition Annealing Temperature

The impact of CO₂-PDA temperatures on positive bias instability was then investigated. The applied gate bias corresponded to $E_{OX, stress}$ of +5, +7, and +8 MVcm⁻¹, which are relatively high and used to evaluate reliability under severe conditions. During the stress tests, the sweep range of the gate voltage in the $C-V$ measurements was 10—5 V for the Npla.-depo.-CO₂ samples and 20—10 V for the Ox.-NO sample. The difference in the sweep ranges was chosen to account for the oxide thickness. In this experiment, the injected charge density (ΔQ_{stress}) was calculated from ΔV_{FB} using the following equation:

$$\Delta Q_{stress} = \frac{C_{OX} \times \Delta V_{FB}}{e}. \quad (3.3)$$

Figure 3.13 shows ΔQ_{stress} as a function of stress time when $E_{OX, stress}$ was (a) +5 MVcm⁻¹ and (b) +7 MVcm⁻¹. ΔQ_{stress} was significantly reduced as the CO₂-PDA temperature

increased. When $E_{\text{OX, stress}}$ was $+5 \text{ MVcm}^{-1}$, the ΔQ_{stress} values after 2000 s of stress for the samples annealed in CO_2 at 1050°C , 1150°C , and 1250°C were 1.7×10^{11} , 3.9×10^{10} , and $6.6 \times 10^8 \text{ cm}^{-2}$, respectively. For $E_{\text{OX, stress}}$ of $+7 \text{ MVcm}^{-1}$, the ΔQ_{stress} values after 2000 s of stress decreased from 6.9×10^{11} to $1.4 \times 10^{10} \text{ cm}^{-2}$ as the CO_2 -PDA temperature increased from 1050°C to 1250°C .

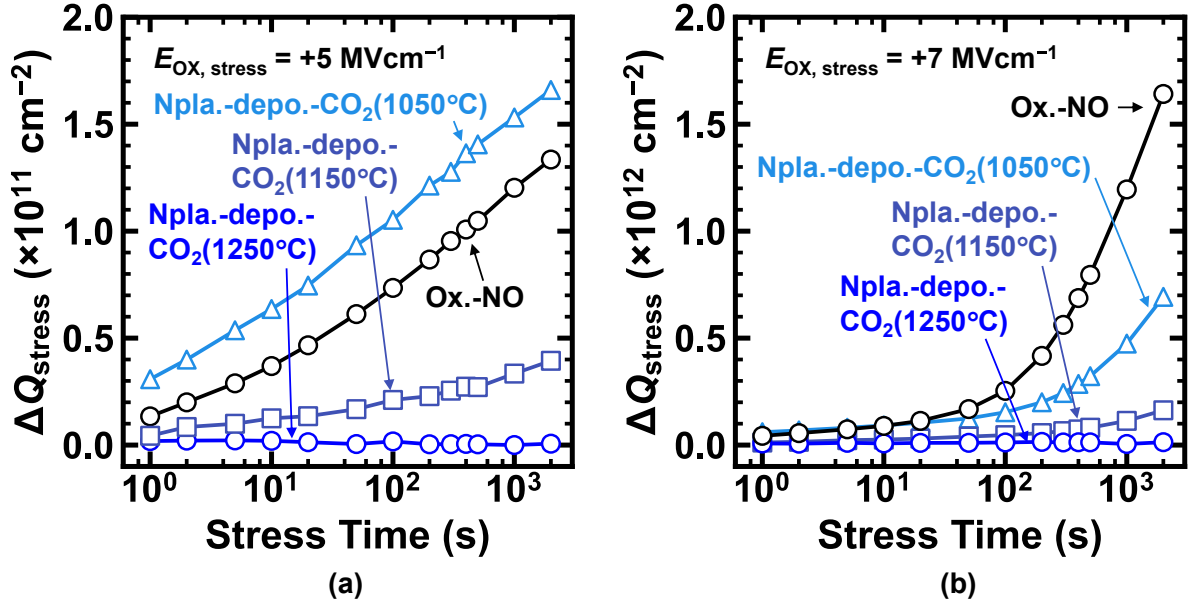


Figure 3.13. Stress time dependence of ΔQ_{stress} corresponding to the injected electron density. Constant voltages corresponding to $E_{\text{OX, stress}}$ of (a) $+5 \text{ MVcm}^{-1}$ and (b) $+7 \text{ MVcm}^{-1}$ were applied to the gate electrode.

To easily compare the results of stress tests, Fig. 3.14 represents $E_{\text{OX, stress}}$ dependence of ΔQ_{stress} after the gate bias stress was applied for 2000 s. ΔQ_{stress} was found to increase with increasing $E_{\text{OX, stress}}$. This is definitely because of the strong oxide field applied to the oxide, resulting in significant electron injection. In all stress conditions, ΔQ_{stress} decreased as the CO_2 -PDA temperature increased. Notably, ΔQ_{stress} of the Npla.-depo.- $\text{CO}_2(1250^\circ\text{C})$ sample was much lower than that of the Ox.-NO sample. When $E_{\text{OX, stress}}$ was $+5$, $+7$, and $+8 \text{ MVcm}^{-1}$, the ΔQ_{stress} values for the Ox.-NO sample were 1.3×10^{11} , 1.6×10^{12} , and $5.0 \times 10^{12} \text{ cm}^{-2}$, while those of the Npla.-depo.- $\text{CO}_2(1250^\circ\text{C})$ sample were 6.6×10^8 , 1.4×10^{10} , and $6.7 \times 10^{11} \text{ cm}^{-2}$, respectively. These results indicate that high-temperature CO_2 -PDA reduces not only interface defects (Fig. 3.10) but also oxide defects, leading to high stability to electron injection.

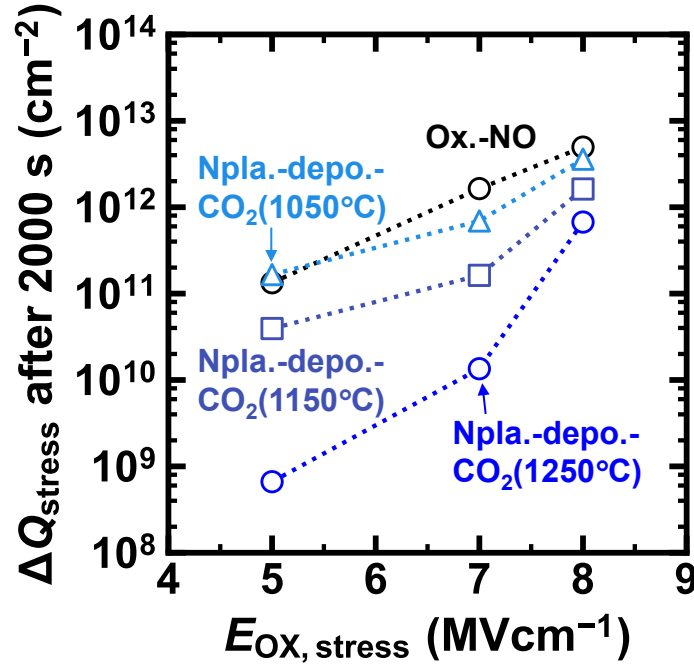


Figure 3.14. ΔQ_{stress} after applying gate bias stresses for 2000 s as a function of $E_{OX, stress}$.

3.7 Flatband Voltage Control Using Low-Temperature Oxygen Annealing

The results so far indicate that the combination of plasma nitridation, SiO₂ deposition, and CO₂-PDA can effectively reduce both interface and oxide defects. However, the C - V curves are shifted in the negative direction (Fig. 3.5(a)), which is undesirable for practical applications. Therefore, this section focuses on the attempt to control V_{FB} . It has been reported that N₂ nitridation causes a negative V_{FB} shift, whereas subsequent low-temperature O₂ annealing moves V_{FB} closer to its ideal position [99]. Here, particular attention must be paid to the O₂ annealing temperature, because high-temperature O₂ annealing oxidizes the SiC surface, which likely leads to the formation of carbon-related defects [38, 40]. Thus, it is favorable to use low-temperature O₂ annealing.

This section examines whether the above strategy is effective for SiO₂/SiC interfaces formed by plasma nitridation and SiO₂ deposition and discusses the origin of the V_{FB} shift based on the relationship between V_{FB} and the capacitance equivalent thickness (CET). From the V_{FB} -CET plot, information such as the fixed charge density, the polarity of the fixed charges, and the presence of dipoles can be obtained.

3.7.1 Experiment

The detailed process flow is shown in Fig. 3.15. The SiC surface was plasma nitrided at 350°C for 30 min. Next, a SiO₂ layer with a thickness of 50 nm was deposited by the sputtering method in a pure Ar ambient. The deposition conditions were the same as section 3.3. Subsequently, CO₂-PDA was performed at 1250°C, 30 min. Then, O₂ annealing was performed at 500°C–700°C for 30 min. After that, SiO₂ was etched with a 1%-HF solution to form a slope-shaped structure. Finally, MOS capacitors were fabricated by depositing Al gate electrodes. CET was calculated from C_{OX} obtained from C – V measurements.

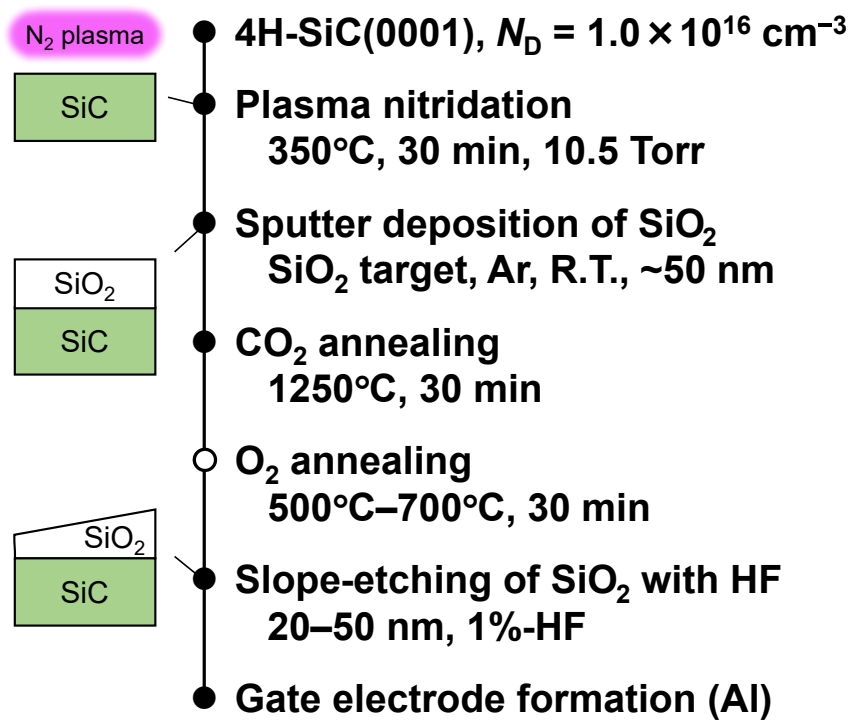


Figure 3.15. Fabrication flow of the SiC MOS capacitors in this section. After plasma nitridation of the SiC surface, SiO₂ was deposited, and CO₂-PDA was performed, followed by O₂ annealing. Subsequently, the SiO₂ layer was slope-etched using a 1%-HF solution.

3.7.2 C – V Characteristics

Figure 3.16 shows the C – V characteristics of samples without O₂ annealing and those annealed in O₂ at 500°C–700°C. Here, the gate voltage was swept from depletion to accumulation. While the sample without O₂ annealing showed a steep characteristic, V_{FB} was shifted in the negative voltage direction. By carrying out the subsequent O₂ annealing at 500°C, V_{FB} was positively shifted, approaching its ideal value. The positive shift even increased as the O₂ annealing temperature increased. The V_{FB} values of the

samples without O_2 annealing and those annealed in O_2 at 500°C , 600°C , and 700°C were -2.90 , -0.21 , 0.37 , and 0.93 V, respectively. The V_{FB} value after O_2 annealing at 600°C was particularly close to the ideal value of 0.23 V. Furthermore, no significant stretch-out was observed in the $C-V$ characteristic of the sample with O_2 annealing, indicating that O_2 annealing does not cause severe degradation in interface properties.

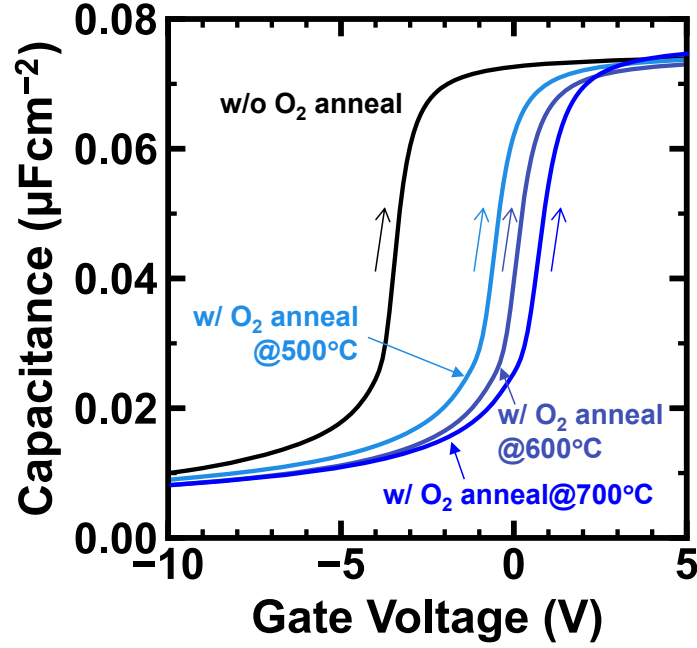


Figure 3.16. $C-V$ characteristics of the samples without O_2 annealing and with O_2 annealing at 500°C , 600°C , and 700°C . The gate voltage was swept from negative to positive.

3.7.3 Flatband Voltage as a Function of Capacitance Equivalent Thickness

This section discusses the origin of the negative shift of V_{FB} based on the V_{FB} -CET plot. V_{FB} was calculated from the $1/C^2-V_G$ plot obtained by sweeping the gate voltage from depletion to accumulation at 1 MHz. Figure 3.17 shows the V_{FB} -CET plot for samples without O_2 annealing and with O_2 annealing at 600°C , which gives V_{FB} closest to the ideal value. The ideal V_{FB} value is also shown in the figure. For the sample without O_2 annealing, V_{FB} was negatively shifted with increasing CET. The dashed line represents a linear fit and closely matches the data. This indicates that the fixed charges are not distributed in the oxide but rather localized near the SiO_2/SiC interface [100]. The fixed charge density calculated from the slope was $1.1 \times 10^{12} \text{ cm}^{-2}$, while the intercept was 0.16 V, close to the ideal V_{FB} (0.23 V). Thus, the influence of the dipole is considered

negligibly small. After O_2 annealing at 600°C , the slope remarkably decreased, indicating a reduction of positive fixed charges. The calculated fixed charge density was $9.2 \times 10^{10} \text{ cm}^{-2}$. The intercept remained nearly unchanged (0.23 V), suggesting no additional formation of interface dipoles. These results indicate that the negative V_{FB} shift observed in the Npla.-depo.- $\text{CO}_2(1250^\circ\text{C})$ sample is mainly caused by positive fixed charges. O_2 annealing can effectively remove these charges and, therefore, can be used for proper control of V_{FB} .

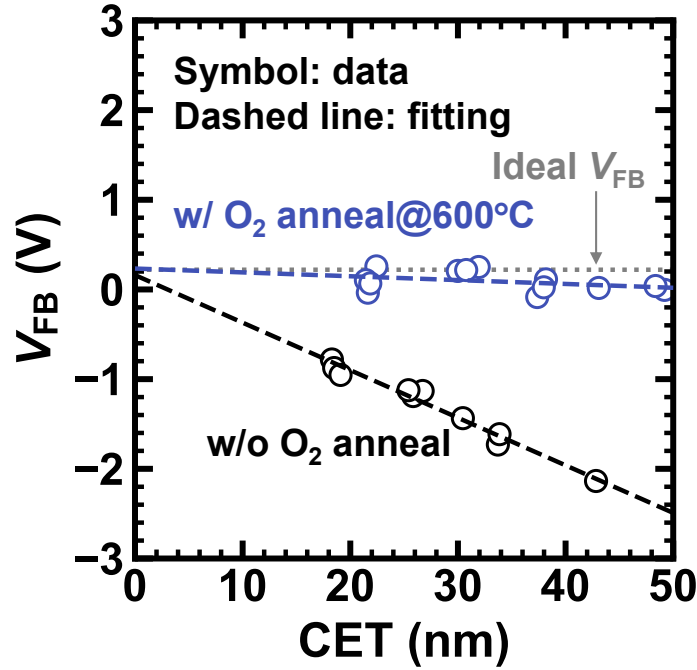


Figure 3.17. V_{FB} as a function of CET. V_{FB} was obtained from the C - V curves swept from depletion to accumulation. Symbols represent the experimental data, and the dashed lines indicate the linear fitting. The dotted line shows the ideal V_{FB} calculated from the work-function difference between Al and SiC.

3.8 Discussion

Finally, the author discusses key factors contributing to the improvement of interface properties and reliability via the proposed method. First is the incorporation of high density of nitrogen atoms by plasma nitridation. Conventional nitridation methods are conducted after formation of the gate oxide [61, 63]. However, this limits the nitrogen amount at the SiO_2/SiC interface [66] and would incorporate nitrogen atoms on the SiO_2 side of the interface [84]. In the proposed method, the SiC surface was directly nitrided, leading to selective incorporation of nitrogen atoms. Plasma nitridation enabled

effective incorporation of a high density of nitrogen atoms, which may contribute to better passivation of defects.

The second is the suppression of SiC surface oxidation. Since experimental and theoretical studies have shown that oxidation of SiC generates carbon-related defects at the SiO₂/SiC interface [38, 40, 101], sputter deposition was conducted in pure Ar gas to minimize oxidation. In addition, PDA was conducted in CO₂ atmosphere, which hardly oxidizes the SiC surface even at high temperatures [70].

Third is the reduction in oxide defects by CO₂-PDA. Since SiO₂ was formed by sputter deposition, the oxide likely contains a high density of oxygen vacancies [102–104]. Conventionally, O₂ annealing is usually employed to reduce oxygen vacancies [105–107]. However, it can oxidize the SiC surface, generating carbon-related defects. In contrast, CO₂ annealing effectively compensates oxygen vacancies [70, 96], while suppressing oxidation of SiC even under high-temperature annealing conditions. Another possible role of CO₂-PDA is the removal of nitrogen near the SiO₂/SiC interface. Nitrogen atoms near the interface can act as electron or hole trap [72, 86, 90]. In the process presented here, the SiC surface was nitrided prior to SiO₂ formation. Therefore, unlike NO annealing, introduction of nitrogen atoms on the SiO₂ side of the interface is negligible. Nevertheless, nitrogen on the SiC side of the interface may diffuse into the SiO₂ during PDA, but any diffused nitrogen is considered to be removed by CO₂ [97].

As a result of these factors, improved interface properties and reliability were achieved by the proposed method. Furthermore, positive fixed charges induced by the proposed method can be effectively eliminated via ultra-low-temperature O₂ annealing.

3.9 Summary

This chapter presents a technique for forming a high-quality nitrided SiO₂/SiC interface. The process consists of plasma nitridation of the SiC surface, sputter deposition of SiO₂, and CO₂-PDA. The XPS analysis confirmed that this approach introduces about three times higher amount of nitrogen on the SiC surface compared with NO annealing. *C*-*V* measurements revealed that this technique substantially reduces D_{it} at shallow energy levels relative to the Ox.-NO sample. The D_{it} value was effectively reduced by about one order of magnitude as the CO₂-PDA temperature increased from 1050°C to 1250°C. On the other hand, Ar-PDA at 1250°C had only a limited effect on defect passivation, suggesting a critical role of CO₂ atmosphere in mitigating defects. SiC MOS structures fabricated by the present method exhibited high stability under excimer UV irradiation and positive bias stress, demonstrating enhanced reliability. Key points of this approach can be summarized in three aspects: the incorporation of a high density of nitrogen on the SiC surface, suppression of oxidation, and reduction of oxide defects.

Chapter 4

Performance and Reliability Improvement in SiC MOS Devices via a Novel Hydrogen Annealing Process

4.1 Introduction

As described in Chap. 1, various defects exist in the SiO₂/SiC structure [4, 6], and these defects have negative impacts on the performance and reliability of SiC MOSFETs [30, 31]. Over the past several decades, many efforts have been made to reduce interface defects. The most effective approach is the introduction of foreign atoms. μ_{FE} can be increased by introducing N [61–63], P [67], B [68], or Na [69] at the SiO₂/SiC interface. However, as discussed in Chap. 2 and reported in previous studies [65, 82, 83], the introduction of N causes reliability degradation in SiC MOS devices. Similar reliability issues are pointed out for P or B atoms [27, 78]. Na has long been known as a factor in ion drift [88], which makes it unsuitable for practical use. Meanwhile, efforts have been made to reduce interface defects in SiO₂/SiC structures with H₂ annealing, a common technique in Si MOS technology. It has been reported that H₂-POA can reduce D_{it} near the E_C [108, 109] and improve μ_{FE} of n-channel SiC MOSFETs to about 7 cm²V⁻¹s⁻¹ [109] and that of p-channel SiC MOSFETs to about 13 cm²V⁻¹s⁻¹ [110]. However, significant μ_{FE} improvements comparable to those achieved by N, B, P, or Na incorporation have not yet been reported for H₂-POA.

Recently, oxidation-minimizing processes that can improve μ_{FE} have been reported [74–76]. A key point of the methods is to remove surface defects through H₂ annealing, followed by the deposition of the gate oxide while suppressing oxidation of the SiC surface. However, since interface nitridation was used in these previous studies, forming a high-

quality SiC MOS structure that eliminates the introduction of problematic impurities has yet to be achieved. In Chap. 3, it was found that precise control of the nitrogen profile can improve reliability. Nevertheless, the ideal SiO_2/SiC interface is considered to be one that excludes problematic impurities as much as possible.

In this chapter, a two-step annealing process in H_2/Ar mixtures is presented, and improvements in the performance and reliability of SiC MOS devices without nitridation are demonstrated.

4.2 Two-Step Annealing in Diluted Hydrogen Mixtures

Figure 4.1 shows gate oxide formation process using two-step annealing in H_2/Ar mixtures (2-step H_2/Ar process). N_2 -diluted H_2 annealing is widely employed in Si MOS technology [111]. In this study, however, Ar-diluted H_2 (3% H_2 in Ar) was used to exclude possible nitridation of the SiO_2/SiC interface. In the 2-step H_2/Ar process, pre-deposition H_2/Ar annealing (pre- H_2/Ar) was first performed on the SiC surface prior to SiO_2 deposition, aiming to remove surface defects. Next, the surface is cleaned with HF solutions, and a SiO_2 dielectric was deposited by PECVD to suppress oxidation of the SiC surface. Then, CO_2 annealing and post-deposition H_2/Ar annealing (post- H_2/Ar) were performed to reduce oxide and interface defects, respectively.

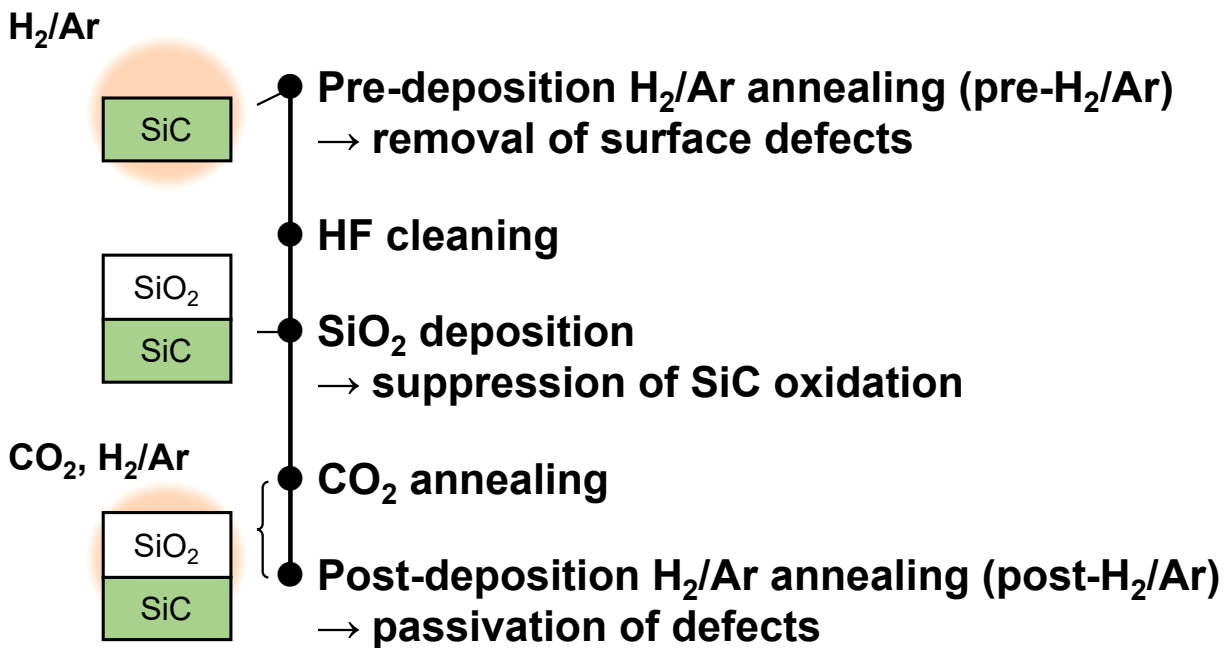


Figure 4.1. Gate oxide formation process of two-step annealing in H_2/Ar mixtures.

4.3 Experiment

Figure 4.2 shows the detailed process flow for fabricating SiC MOS capacitors and MOSFETs. N-type SiC(0001) epitaxial layers (N_D : $(0.5\text{--}2.0) \times 10^{16} \text{ cm}^{-3}$) and p-type SiC(0001) epitaxial layers (acceptor density (N_A): $5.0 \times 10^{15} \text{ cm}^{-3}$) were used in this study. The source and drain regions of the MOSFETs were formed by implantation of P^+ , whereas the body regions were formed by implantation of Al^+ . P^+ and Al^+ were implanted at 500°C with doses of $7.7 \times 10^{14} \text{ cm}^{-2}$ and $2.0 \times 10^{15} \text{ cm}^{-2}$ and energies of 10–270 keV and 10–140 keV, respectively. The ions were implanted through a $\sim 50\text{-nm}$ -thick SiO_2 capping layer. Subsequently, the cap SiO_2 was removed by HF solutions, and a carbon cap was deposited prior to an activation annealing [112]. Following activation annealing at 1700°C for 5 min in Ar, the carbon cap was removed by O_2 annealing at 800°C for 120 min.

After wet cleaning, the gate oxides were formed in a manner described in Fig. 4.1. Pre- H_2/Ar was performed on the SiC surface at 1300°C for 10 min in a diluted H_2 atmosphere (3% H_2/Ar), followed by 5%-HF cleaning for 30 s. Next, SiO_2 with a thickness of 40–50 nm was deposited by PECVD. During deposition, the tetraethyl orthosilicate (TEOS) and O_2 gas flow rates, RF power, chamber pressure, and substrate temperature were 1, 250 sccm, 30 W, 79 Pa, and 400°C , respectively. This was followed by CO_2 annealing at 1300°C for 30 min. Then, post- H_2/Ar was performed at 1200°C for 30 min in the 3% H_2/Ar atmosphere. This sample is hereafter referred to as the “2-step H_2/Ar ”.

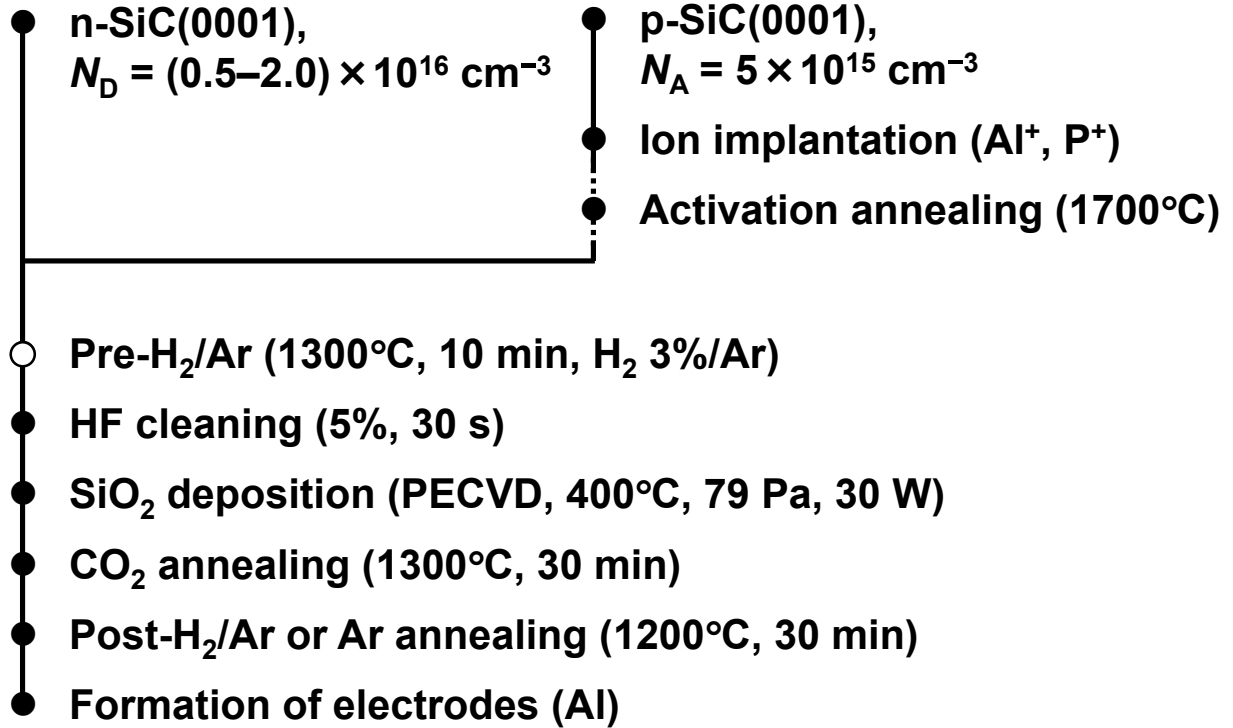


Figure 4.2. Fabrication process of SiC MOS capacitors and MOSFETs.

For comparison, samples without pre-H₂/Ar (w/o pre-H₂/Ar) and annealed in Ar instead of post-H₂/Ar (w/o post-H₂/Ar) were also prepared. In addition, samples fabricated by thermal oxidation at 1300°C (As-Ox.) and by thermal oxidation followed by NO annealing at 1250°C for 60 min (Ox.-NO) were prepared. For the fabrication of MOS capacitors and MOSFETs, Al was used as the electrodes. The channel length and channel width of the MOSFETs were 100 and 160 μm , respectively.

4.4 SiC MOS Interface Properties

4.4.1 High-Low $C-V$ Characteristics

Figure 4.3(a) shows the quasi-static and 1 MHz $C-V$ characteristics of the 2-step H₂/Ar, As-Ox., and Ox.-NO samples. Here, the gate voltage was swept from depletion to accumulation. For the As-Ox. sample, a large deviation was observed between the quasi-static and 1 MHz $C-V$ curves, indicating extremely high D_{it} values. In contrast, the 2-step H₂/Ar sample exhibited a significant reduction in frequency dispersion, and the two curves were in good agreement. Similarly, the Ox.-NO sample also showed small frequency dispersion, suggesting low D_{it} . It should be noted that the $C-V$ curve of the 2-step H₂/Ar sample was shifted in the negative direction. The V_{FB} value of the 2-step H₂/Ar sample was -4.2 V, and the fixed charge density corresponding to this V_{FB} shift was $2.0 \times 10^{12} \text{ cm}^{-2}$.

Next, the effects of pre-H₂/Ar and post-H₂/Ar steps were examined in detail. Figure 4.3(b) presents the quasi-static and 1 MHz $C-V$ curves measured for the 2-step H₂/Ar, w/o pre-H₂/Ar, and w/o post-H₂/Ar samples. Noticeable frequency dispersions appeared in the w/o pre-H₂/Ar, and w/o post-H₂/Ar samples, indicating D_{it} was not sufficiently reduced compared with the 2-step H₂/Ar sample. These findings indicate that both the pre- and post-H₂/Ar steps are essential for reducing D_{it} , highlighting the importance of eliminating surface defects and hydrogen passivation of interface defects. The V_{FB} values of the w/o pre-H₂/Ar, and w/o post-H₂/Ar samples were -0.8 and -3.1 V, respectively, exhibiting smaller negative shifts than that of the 2-step H₂/Ar sample. Notably, the V_{FB} shift in the w/o pre-H₂/Ar sample was relatively small, implying that the formation of positive fixed charges is attributed to the pre-H₂/Ar step.

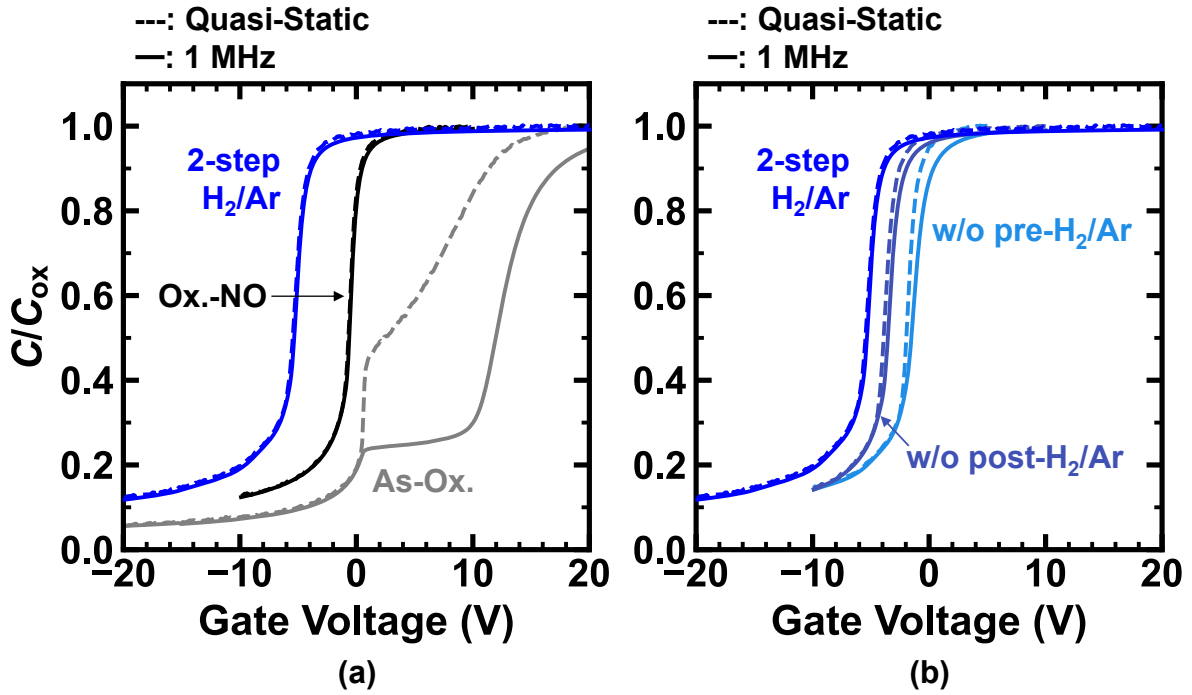


Figure 4.3. Quasi-static and 1 MHz C - V characteristics of (a) the 2-step H_2/Ar , As-Ox., and Ox.-NO samples and (b) the 2-step H_2/Ar , w/o pre- H_2/Ar , and w/o post- H_2/Ar samples. Dashed and solid lines represent the quasi-static and 1 MHz C - V curves, respectively. The capacitance is normalized by the C_{ox} .

4.4.2 Energy Distributions of D_{it}

Figure 4.4 shows the energy distributions of D_{it} evaluated by the high (1 MHz)-low method. As a result, D_{it} values at $E_C - E = 0.2$ eV were 9.0×10^{12} and 3.2×10^{11} eV⁻¹cm⁻² for the As-Ox. and 2-step H₂/Ar samples, respectively. Although a nitridation process was not involved in the 2-step H₂/Ar process, the D_{it} value at $E_C - E = 0.2$ eV of the 2-step H₂/Ar sample was comparable to that of the Ox.-NO sample. This indicates that the 2-step H₂/Ar process can effectively reduce interface defects without interface nitridation. In contrast, the D_{it} values at $E_C - E = 0.2$ eV for the w/o pre-H₂/Ar and w/o post-H₂/Ar samples were relatively high, i.e., 2.6×10^{12} and 1.4×10^{12} eV⁻¹cm⁻², respectively. Thus, the substantial reduction in D_{it} necessitates both the pre- and post-H₂/Ar treatments.

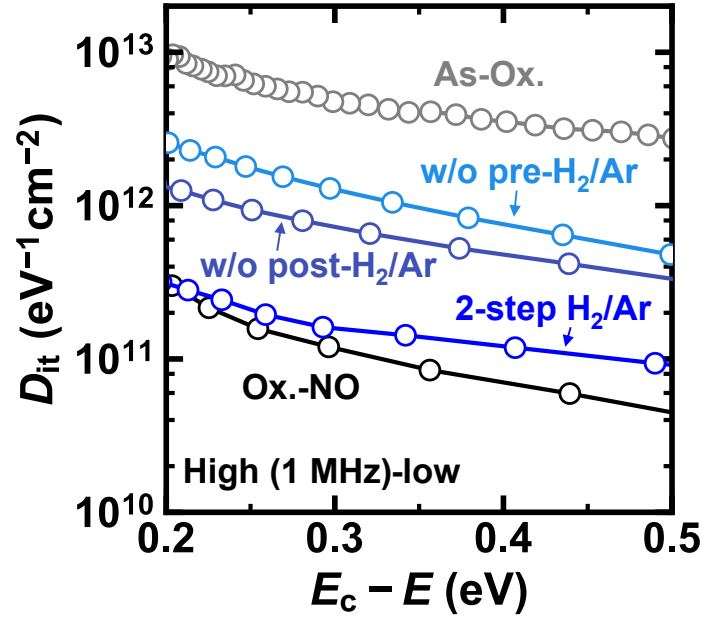


Figure 4.4. Comparison of the energy distributions of D_{it} for the 2-step H₂/Ar, w/o pre-H₂/Ar, w/o post-H₂/Ar, As-Ox., and Ox.-NO samples.

4.5 Depth Profiles of Foreign Atoms in Silicon Dioxide/SiC Structures

To confirm that the improvement in the electrical properties achieved by the 2-step H_2/Ar process was not due to the incorporation of problematic impurities, SIMS measurements were conducted. Concentrations of foreign elements were measured within the Ox.-NO and 2-step H_2/Ar samples. For the Ox.-NO sample, a N depth profile was evaluated, whereas for the 2-step H_2/Ar sample, depth profiles of N as well as H, B, P, and Na were obtained.

Figure 4.5(a) shows the depth profile of N concentration of the Ox.-NO sample, together with the raw count signals of O and C. The position of the SiO_2/SiC interface was defined as the depth where the C signal dropped to half of that in bulk SiC. In the Ox.-NO sample, the N concentration at the SiO_2/SiC interface reached the order of 10^{21} cm^{-3} . This result is consistent with previous studies [66, 113, 114] and indicates that a high concentration of N atoms is required for effective passivation of interface defects.

Figure 4.5(b) shows the depth profiles of N, H, B, P, and Na obtained from the 2-step H_2/Ar sample. The N concentration was about 10^{19} cm^{-3} at the interface, which was much lower than that of the Ox.-NO sample. In the 10-min nitrided sample, where defect reduction is still insufficient, the nitrogen concentration at the interface is $10^{20}\text{--}10^{21} \text{ cm}^{-3}$ [65, 115, 116], whereas the 2-step H_2/Ar sample exhibits roughly an order of magnitude lower nitrogen content. This indicates that the reduction in D_{it} by 2-step H_2/Ar process is not due to interface nitridation, but rather due to combining removal of surface defects, suppression of oxidation, and hydrogen passivation of interface defects. It was also confirmed that the introduction of B, P, and Na was almost negligible. Meanwhile, H concentration at the interface was about 10^{20} cm^{-3} , which is likely related to the post- H_2/Ar treatment. Thus, it seems that hydrogen passivation plays a critical role in the D_{it} reduction. However, as described in Fig. 4.4, the absence of the pre- H_2/Ar results in a high D_{it} (w/o pre- H_2/Ar sample). Therefore, simply introducing hydrogen is not effective, and sufficient D_{it} reduction can be achieved only when surface defects are removed by the pre- H_2/Ar treatment.

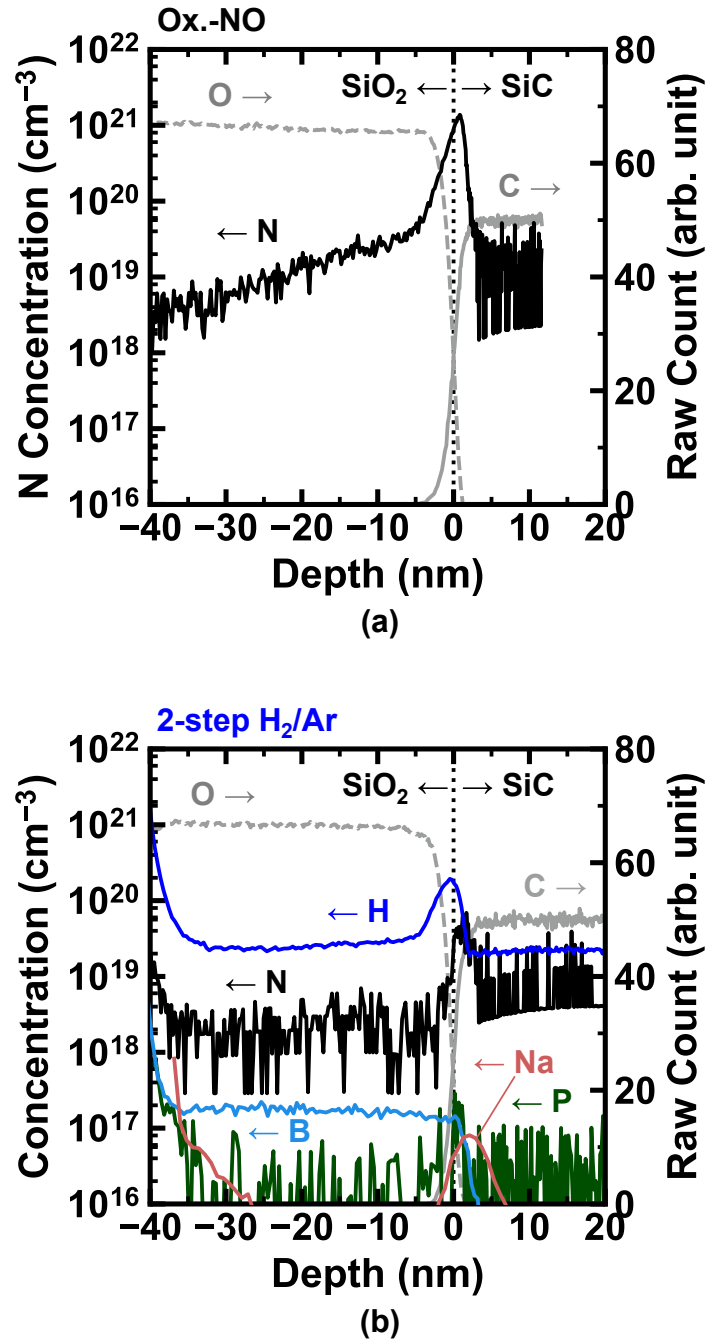


Figure 4.5. Depth profiles of foreign elements in SiO₂/SiC structures evaluated by SIMS. (a) N concentration in the Ox.-NO sample, and (b) N, H, B, P, and Na concentrations in the 2-step H₂/Ar sample. Raw counts of O and C are also shown. The SiO₂/SiC interface position was determined as the depth at which the C signal was half of its bulk level and was set to 0 nm.

4.6 Performance of SiC MOSFETs

In this section, the impact of the 2-step H₂/Ar process on the performance of the fabricated MOSFETs is described. Figure 4.6 shows the normalized drain current ($I_D \times L/W$) and μ_{FE} as a function of gate voltage for the 2-step H₂/Ar, and As-Ox. [49] samples. The gate voltage was swept from negative to positive and the drain voltage (V_D) was set to 0.1 V in this measurement. Although the $I_D \times L/W$ curve of the 2-step H₂/Ar sample shifted to the negative direction, its slope was steeper compared to that of the As-Ox. sample. The subthreshold slope (SS) was evaluated using the following equation [3]:

$$SS = \frac{dV_G}{d(\log_{10} I_D)} = \frac{kT}{e} \ln \frac{C_{OX} + C_D + e^2 D_{it}}{C_{OX}}, \quad (4.1)$$

where C_D is the semiconductor capacitance. The SS values extracted from the normalized drain current range from 10^{-9} to 10^{-8} A were 1.0 and 3.0 Vdec⁻¹ for the 2-step H₂/Ar and As-Ox. samples, respectively. These results indicate that the 2-step H₂/Ar process effectively reduces D_{it} , consistent with the results obtained for MOS capacitors (Fig. 4.4).

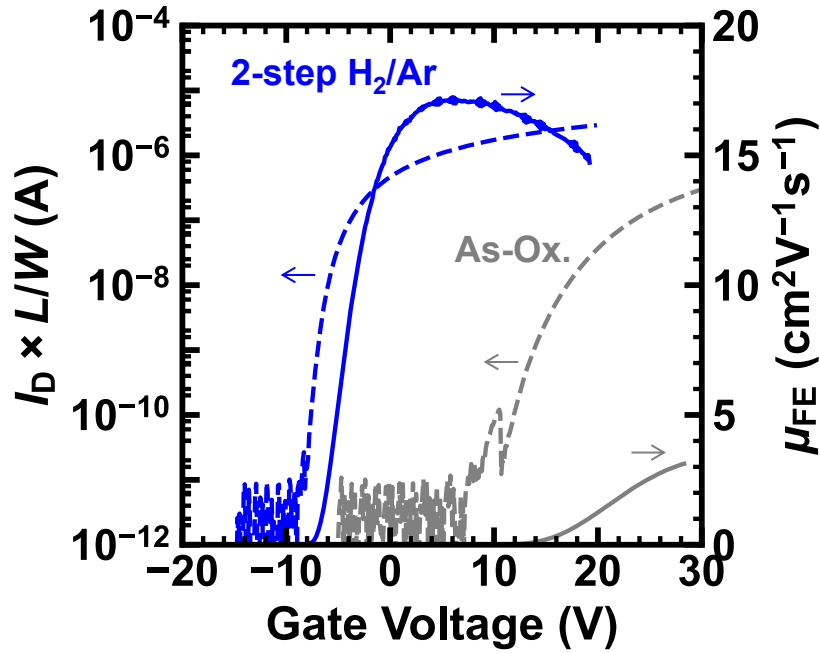


Figure 4.6. Normalized drain current ($I_D \times L/W$) and μ_{FE} as a function of gate voltage for the 2-step H₂/Ar and As.-Ox [49] samples. The drain voltage was set to 0.1 V.

μ_{FE} was calculated using the following equation:

$$\mu_{FE} = \frac{L}{WC_{OX}V_D} \times \frac{dI_D}{dV_G}. \quad (4.2)$$

The maximum μ_{FE} value of the As-Ox. sample was about 3 cm²V⁻¹s⁻¹, whereas the 2-step H₂/Ar process increased it to 17 cm²V⁻¹s⁻¹. As shown in the Eq. (4.2), μ_{FE} is

proportional to the slope of the gate characteristics. As mentioned in section 4.4.2, the D_{it} of the 2-step H₂/Ar sample was substantially lower than that of the As-Ox. sample. This would lead to an increase in n_{free} in the MOS channel for the 2-step H₂/Ar sample, which could lead to enhanced I_D and, consequently, the μ_{FE} . These results demonstrate that the 2-step H₂/Ar process improves the performance of SiC MOSFETs without introducing nitrogen at the interface.

4.7 Reliability of SiC MOS Devices

4.7.1 Gate Leakage Characteristics

The gate leakage current as a function of E_{OX} was evaluated. While E_{OX} is typically calculated using experimentally determined V_{FB} , here it was calculated using the ideal V_{FB} according to the following equation:

$$E_{OX} = \frac{V_G - \phi_{MS}}{t_{OX}}. \quad (4.3)$$

Here, ϕ_{MS} is the ideal V_{FB} (0.23 V). This approach was used because the SiO₂/SiC structure fabricated by the 2-step H₂/Ar process contains a high density of fixed charges, which makes the standard E_{OX} calculation inaccurate. Specifically, in the presence of a high density of fixed charges, E_{OX} is not zero even when V_G equals the experimentally determined V_{FB} .

Figure 4.7 shows the gate leakage current density (J_G) as a function of the E_{OX} obtained from the 2-step H₂/Ar and Ox.-NO samples. The onset field of the leakage current for the 2-step H₂/Ar sample was higher than that of the Ox.-NO sample.

In Fig. 4.7, the dashed lines represent the fitting results based on the FN model described in Eq. (1.6). Here, the effective mass of electrons in the oxide was assumed to be $0.42m_0$ [117]. Both the 2-step H₂/Ar and Ox.-NO samples roughly agreed with the theoretical characteristics, indicating that the leakage current is mainly governed by FN tunneling. The assumed ΔE_C was 3.26 and 2.95 eV for the 2-step H₂/Ar and Ox.-NO samples, respectively. This indicates that, the lower J_G observed in the 2-step H₂/Ar sample at a given E_{OX} is attributed to its higher ΔE_C compared with the Ox.-NO sample.

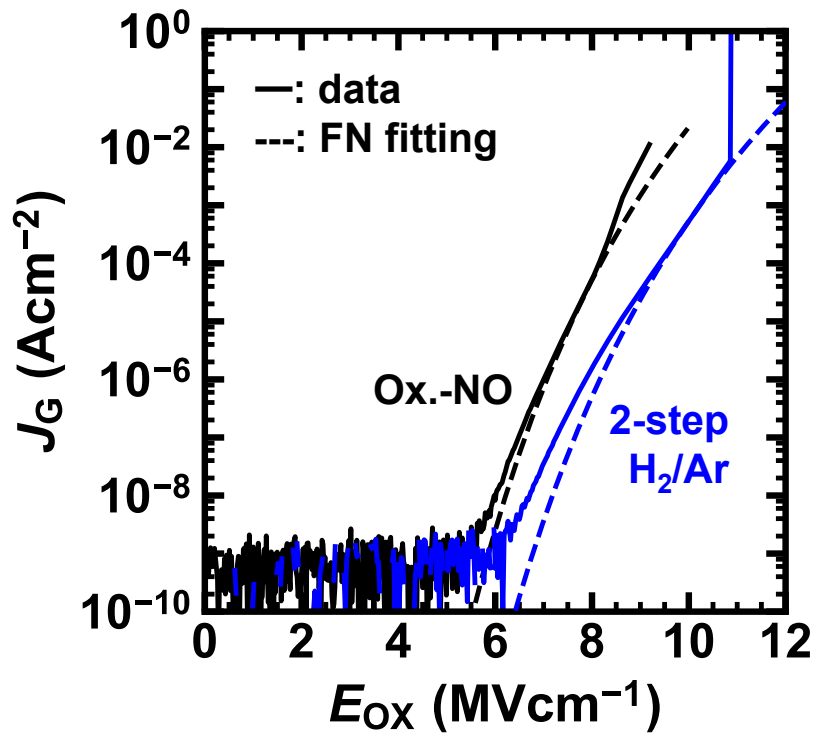


Figure 4.7. J_G - E_{OX} characteristics of the 2-step H_2/Ar and Ox.-NO samples. Solid lines represent the experimental data, while dashed lines indicate the fitting assuming the FN model.

4.7.2 Positive and Negative Bias Instability

Next, positive and negative bias instabilities of SiC MOS devices were investigated. Here, SiC MOS capacitors were used instead of MOSFETs to accurately evaluate the reliability. To evaluate the V_{th} of MOSFETs, the gate voltage must be swept over a wide range, including both positive and negative gate voltages. Depending on the voltage conditions, electrons or holes accumulate in the MOS channel. This leads to electron-hole recombination, resulting in an underestimation of V_{th} drift. By using MOS capacitors and appropriately limiting the gate voltage, positive and negative bias stress tests can be performed while minimizing carrier recombination. Specifically, during electron injection tests on n-type MOS capacitors, the gate voltage should not be swept to the negative side to avoid electron emission from the defect states. Similarly, when evaluating V_{FB} instability due to hole injection, the gate voltage should not be swept to the positive side to prevent recombination between trapped holes and electrons.

In this experiment, both positive and negative bias stress tests were performed as illustrated in Fig. 4.8. In the stress tests, the sweep ranges for the first two C - V measurements and for measurements during stress tests were set as follows: +15 V to -15 V and +15 V to -10 V for the positive bias test, and -15 V to +15 V and -15 V to -10 V for the negative bias test. $E_{\text{OX, stress}}$ was set to $\pm 6 \text{ MVcm}^{-1}$, which was determined using ϕ_{MS} instead of experimentally determined V_{FB} . During the application of the negative bias stress, holes were generated by illuminating the devices with UV light in the wavelength range of 250–450 nm [82].

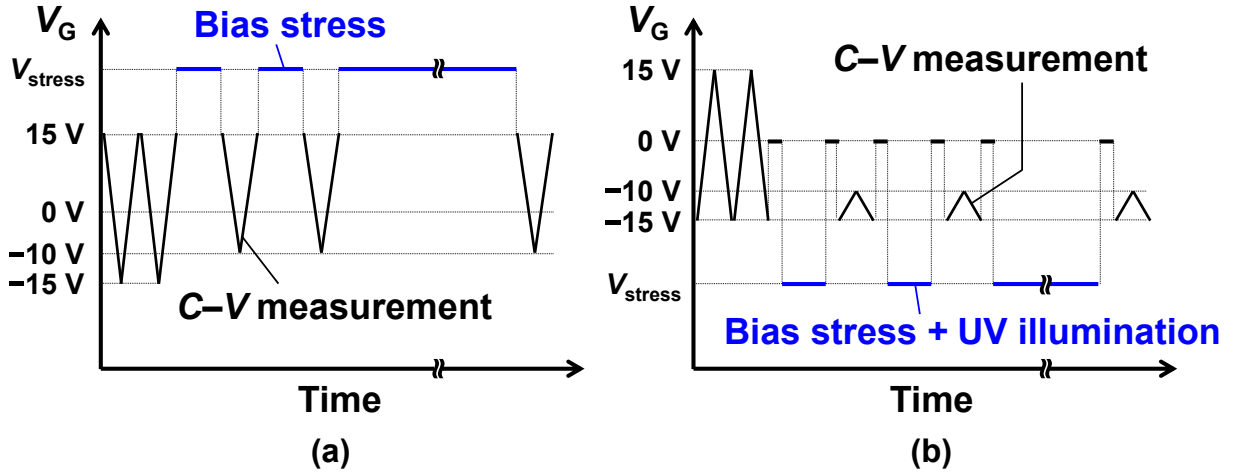


Figure 4.8. Measurement flow for (a) positive and (b) negative bias stress tests. During the application of negative bias stress, the MOS capacitor was illuminated with UV light (wavelengths: 250–450 nm) for hole accumulation at the MOS interface [82].

Figure 4.9 shows the ΔV_{FB} as a function of stress time of the 2-step H_2/Ar and Ox.-NO samples. In the Ox.-NO sample, applying the positive bias stress for 2000 s increased ΔV_{FB} up to 0.5 V, while ΔV_{FB} of the 2-step H_2/Ar sample remained near 0 V. This suggests that electron traps are nearly absent in the 2-step H_2/Ar sample. When the negative bias was applied, the ΔV_{FB} of the Ox.-NO sample increased significantly, reaching -4.0 V after 2000 s of stress. This is likely due to nitrogen atoms near the SiO_2/SiC interface [84]. In contrast, ΔV_{FB} of the 2-step H_2/Ar sample remained as small as -0.9 V. These results demonstrate that fabricating MOS structures without nitridation is an effective approach for improving reliability.

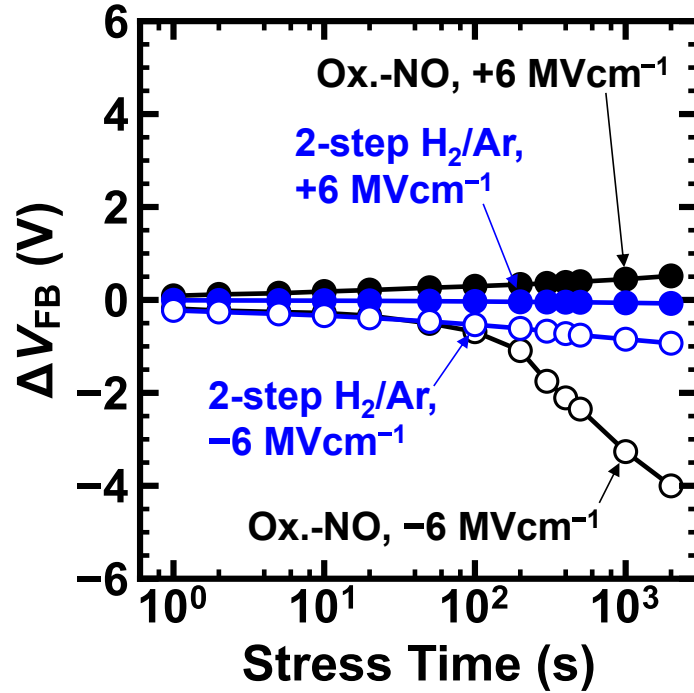


Figure 4.9. Stress time dependence of ΔV_{FB} for the 2-step H_2/Ar and Ox.-NO samples. Voltages corresponding to $E_{OX, stress}$ of $\pm 6 \text{ MVcm}^{-1}$ were applied to the gate electrode for 2000 s.

4.8 Discussion

The improvements in electrical properties of SiC MOS devices achieved by the 2-step H_2/Ar process are discussed in terms of the pre- H_2/Ar and post- H_2/Ar treatments. The pre- H_2/Ar step is performed prior to the formation of the gate oxide, aiming to remove surface defects. The presence of such defects has been recently suggested [76] and whether they exist should depend on the wafer vendors as well as the device fabrication process, including sacrificial oxidation [118]. In this study, care was taken to avoid unintended

oxidation of the SiC surface, and thus sacrificial oxidation was not performed even during MOSFET fabrication. Nevertheless, as the pre-H₂/Ar step remained necessary to realize any significant improvement in device properties, surface treatment is regarded as an essential process for optimizing device performance.

The post-H₂/Ar plays a crucial role in reducing defects in the SiO₂/SiC system. The most common effect of hydrogen introduction is the termination of dangling bonds. However, the termination temperatures for Si and C dangling bonds, about 450°C [111] and 900°C [119], respectively, are relatively low compared with the post-H₂/Ar temperature (1200°C) adopted in the present process. Therefore, the passivation of interface defects at the SiO₂/SiC interface observed in this study is unlikely to be explained solely by simple dangling bond termination. Although further studies are required, it is likely that defect passivation occurs only after bond-breaking reactions have taken place at elevated temperature.

In a previous study, H₂ annealing at 800°C–1000°C was performed on the thermally oxidized SiO₂/SiC structures, which led to a reduction in D_{it} values at relatively deep level ($E_C - E = 0.5\text{--}0.6$ eV) [108]. However, the shallow D_{it} values ($E_C - E = 0.2$ eV) remained above 10^{12} eV⁻¹cm⁻², which is higher than those observed in the 2-step H₂/Ar sample. This difference is likely due to the suppression of SiC oxidation and the pre-H₂/Ar step, both of which help to suppress defect formation. It should be noted that D_{it} of the samples without pre-H₂/Ar and post-H₂/Ar steps were relatively high (Fig. 4.4), indicating that the combination of both pre- and post-H₂/Ar is essential to achieve the observed improvement in device performance.

However, because μ_{FE} is still much lower than the bulk mobility, further improvements will be needed in future studies.

4.9 Summary

In this chapter, the 2-step H₂/Ar process was presented to enhance the performance and reliability of SiC MOS devices without interface nitridation. The 2-step H₂/Ar process consists of pre-H₂/Ar, SiO₂ deposition, CO₂ annealing, and post-H₂/Ar annealing. Pre-H₂/Ar aimed to remove surface defects prior to SiO₂ deposition, and post-H₂/Ar was performed for hydrogen passivation of defects after SiO₂ deposition. The D_{it} value was reduced to 3.2×10^{11} eV⁻¹cm⁻² at $E_C - E = 0.2$ eV by the 2-step H₂/Ar process, which is comparable with NO-nitrided samples. SIMS analysis confirmed that the observed improvements were achieved without incorporating problematic impurities such as N, P, B, or Na. MOSFETs fabricated using this method exhibited improved μ_{FE} of 17 cm²V⁻¹s⁻¹, which was significantly higher than that of the As-Ox. sample. Additionally, the 2-step H₂/Ar process achieved improved reliability under both positive and negative

bias stress.

Chapter 5

Conclusion

In this thesis, the author highlighted the drawback of conventional NO annealing on SiC MOS structures and reported novel process to improve both performance and reliability of SiC MOS devices.

Chapter 2 examined the effects of excimer UV irradiation on NO-nitrided SiC MOS devices fabricated on the (11 $\bar{2}$ 0) a-face and the (0001) Si-face. The C - V characteristics of NO-nitrided samples were degraded by excimer UV irradiation, whereas the non-nitrided sample exhibited little change in its electrical properties. For the NO-nitrided samples fabricated on the a-face with a 60 min nitridation, the C - V hysteresis was increased from 0.74 to 6.31 V, as a result of excimer UV irradiation. In contrast, the non-nitrided sample showed only a minor change in C - V hysteresis, increasing from 0.54 to 0.67 V. The reliability of these devices was also assessed, revealing a significant increase in ΔV_{FB} for the NO-nitrided devices. The ΔV_{FB} value of the 60 min-NO-nitrided sample fabricated on the a-face was increased from 5.7 to 13.3 V due to excimer UV irradiation, while that of the non-nitrided sample was increased from 0.8 to 1.3 V. A clear correlation was found between ΔV_{FB} and the nitrogen concentration in SiO₂, suggesting that UV irradiation activates nitrogen-related pre-existing defects on the SiO₂ side of the interface. These findings highlight the need for caution when using NO-nitrided SiC MOS devices under harsh environments and emphasize the importance of developing novel defect passivation techniques to achieve high reliability.

Chapter 3 described a method to control the nitrogen profile at the SiO₂/SiC interface. The proposed method aimed to introduce a high density of nitrogen only on the SiC side of the interface for improving the performance and reliability of SiC MOS devices. This specific process involved plasma nitridation of the SiC surface, sputter deposition of SiO₂, and CO₂-PDA. XPS analysis confirmed that this technique incorporates a higher nitrogen amount on the SiC surface than conventional NO annealing. C - V measurements revealed that the method effectively lowers D_{it} at shallow energy levels. Specifically, the D_{it} values at $E_C - E = 0.2$ eV were 1.0×10^{11} and 3.0×10^{11} eV⁻¹cm⁻² for the proposed method

and NO annealing, respectively. It was found that while high-temperature CO₂-PDA effectively reduces D_{it} , Ar-PDA showed a smaller improvement, indicating the importance of a CO₂ atmosphere for passivating interface defects. The SiO₂/SiC structure fabricated using this approach showed superior stability under excimer UV irradiation. Furthermore, their stability under positive bias stress was further enhanced with increasing CO₂-PDA temperature. These findings suggest that the proposed process effectively reduces the interface defects and improves reliability, with the nitrogen profile near the SiO₂/SiC interface playing a critical role in determining the reliability of SiC MOS devices.

Chapter 4 proposed a two-step annealing in H₂/Ar mixture process, designed to form a high-quality SiO₂/SiC structure without interface nitridation. In this process, pre-deposition annealing and post-deposition annealing were performed in Ar-diluted hydrogen (3% H₂ in Ar) to remove surface defects and passivate interface defects, respectively. D_{it} was significantly reduced by the proposed method compared to the as-oxidized sample. The D_{it} values at $E_C - E = 0.2$ eV were 3.2×10^{11} and 9.0×10^{12} eV⁻¹cm⁻² for the samples fabricated by the proposed method and conventional oxidation, respectively. SIMS measurements revealed that the incorporation of problematic impurities, such as N, P, B, Na, was negligible in the sample fabricated by the proposed method. The fabricated SiC MOSFETs exhibited a peak μ_{FE} value of 17 cm²V⁻¹s⁻¹, which was significantly higher than that of the as-oxidized sample (3 cm²V⁻¹s⁻¹). Positive and negative bias stress tests demonstrated improved device reliability. These results highlight the critical importance of removing surface defects and passivating interface defects for achieving high performance in SiC MOSFETs and of eliminating foreign atoms to enhance device reliability.

In summary, this study has provided insight into the mechanisms of degradation caused by conventional NO nitridation process and demonstrated effective approaches in improving device performance and reliability. These findings contribute to a deeper understanding of SiC MOS interface physics and provide useful guidelines for designing of the high-quality SiO₂/SiC interface. Further investigations on the effects of plasma nitridation and two-step annealing in H₂/Ar annealing processes are expected to lead to enhanced device stability and facilitate practical applications in power electronics.

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Publication List

Peer-reviewed journal articles

1. Hiroki Fujimoto, Takuma Kobayashi, Mitsuru Sometani, Mitsuo Okamoto, Takayoshi Shimura, and Heiji Watanabe,
“Degradation of NO-nitrided SiC MOS interfaces by excimer ultraviolet light irradiation”,
Applied Physics Express **15**, 104004 (2022).
2. Hiroki Fujimoto, Takuma Kobayashi, Takayoshi Shimura, and Heiji Watanabe,
“Improvement of interface properties in SiC(0001) MOS structures by plasma nitridation of SiC surface followed by SiO₂ deposition and CO₂ annealing”,
Applied Physics Express **16**, 074004 (2023).
3. Hiroki Fujimoto, Takuma Kobayashi, and Heiji Watanabe,
“Impact of post-deposition annealing on SiO₂/SiC interfaces formed by plasma nitridation of the SiC surface and SiO₂ deposition”,
Applied Physics Express **17**, 116503 (2024).
4. Takuma Kobayashi, Hiroki Fujimoto (equally contributed), Shinji Kamihata, Keiji Hachiken, Masahiro Hara, and Heiji Watanabe,
“Performance and reliability improvements in SiC(0001) MOS devices via two-step annealing in H₂/Ar gas mixture”,
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Conference presentations (first author)

1. Hiroki Fujimoto, Takuma Kobayashi, Mitsuru Sometani, Mitsuo Okamoto, Takayoshi Shimura, and Heiji Watanabe,
“Degradation of NO-nitrided SiC MOS devices due to excimer ultraviolet light illumination”,
International Conference on Silicon Carbide and Related Materials (ICSCRM2022),
September (2022), Davos, Switzerland, We-4-A-3, Oral.

2. Hiroki Fujimoto, Takuma Kobayashi, Yu Iwakata, Takayoshi Shimura, and Heiji Watanabe,
“Improved interface properties in SiC(0001) MOS structures by plasma nitridation of SiC surface prior to SiO₂ deposition”,
International Conference on Silicon Carbide and Related Materials (ICSCRM2023),
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3. Hiroki Fujimoto, Takuma Kobayashi, and Heiji Watanabe,
“Impact of post deposition annealing on SiO₂/SiC structures formed by plasma nitridation of the SiC surface”,
International Conference on Silicon Carbide and Related Materials (ICSCRM2024),
September (2024), Raleigh, USA, Mo-30, Poster.
4. Hiroki Fujimoto, Takuma Kobayashi, Shinji Kamihata, Keiji Hachiken, Masahiro Hara, and Heiji Watanabe,
“Fabrication of high-performance SiC MOSFETs via 2-step annealing in H₂/Ar gas mixtures: A novel method without interface nitridation”,
International Conference on Silicon Carbide and Related Materials (ICSCRM2025),
September (2025), Busan, South Korea, MO-P43, Poster.

Conference presentations (co-author)

1. Shinji Kamihata, Hiroki Fujimoto, Takuma Kobayashi, and Heiji Watanabe,
“Impacts of thermal oxidation and forming gas annealing on surface morphology of SiC(0001)”,
International Conference on Silicon Carbide and Related Materials (ICSCRM2024),
September (2024), Raleigh, USA, Tu-17, Poster.
2. Keiji Hachiken, Takuma Kobayashi, Hiroki Fujimoto, Masahiro Hara, and Heiji Watanabe,
“Critical role of post-deposition annealing on the improvements in SiC MOS structures formed by 2-step H₂/Ar annealing process”,
International Conference on Silicon Carbide and Related Materials (ICSCRM2025),
September (2025), Busan, South Korea, 16B-5, Oral.