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Doctoral Dissertation

High-Frequency Conducted Emissions Modeling in SiC MOSFET based Full-Bridge Power Modules

DEEPANKAR

December 2025

Division of Electrical, Electronic
and Infocommunications Engineering

Graduate School of Engineering

The University of Osaka

Abstract

Wide-bandgap semiconductor devices, such as silicon carbide (SiC) MOSFET, are increasingly preferred in high-voltage power converter applications due to their lower on-state resistance and higher switching frequency compared to silicon-based power devices. However, their operation at high dv/dt and di/dt, coupled with high parasitic oscillation frequency due to low device parasitic capacitances, can increase electromagnetic interference (EMI) noise in the high-frequency region. For both commercial and industrial applications, switching power converters must comply with emission limits set by regulatory bodies such as CISPR and FCC, making EMI analysis during the design phase critical. EMI modeling serves as an essential tool, with approaches typically based on equivalent circuits with noise sources characterized through behavioral or analytical methods. These require experimental measurements of voltage and current waveforms on prototypes and exhibit reduced accuracy at higher frequencies. Circuit simulation tools offer an alternative for emission prediction, though their reliability depends on the accuracy of manufacturer provided power device SPICE models.

This study aims to develop an analytical time-domain model for circuit voltage and current waveforms to predict the conducted emissions spectrum over the 150 kHz–30 MHz frequency range for a single-phase inverter implemented with an SiC MOSFET based full-bridge power module (FBPM). The circuit behavior is primarily determined by power module parasitics and device characteristics. First, empirical models of SiC MOSFET capacitances and output characteristics are presented. Next, a lumped-element FBPM circuit model incorporating wiring inductances and parasitic capacitances is introduced. Although several methods based on S-parameter measurements have been proposed to characterize the parasitics of half-bridge power modules, no equivalent method exists for FBPM due to the complexity of circuit analysis. An

S-parameter based method for FBPM parasitic inductance characterization and an experimental approach for parasitic capacitance estimation are proposed in this study. A non-linear analytical model is then developed to predict switching transients and overall circuit response. The predicted circuit voltage and current waveforms, as well as the conducted emissions spectrum obtained using the proposed model, are validated against experimental measurements.

Chapter 1 discusses EMI noise in switching power converters, focusing on regulatory limits and measurement techniques for conducted emissions.

Chapter 2 introduces a simplified lumped-element circuit model of the FBPM, including empirical modeling of power device characteristics and parasitic capacitances. The chapter also discusses FBPM operation as a single-phase inverter using phase-shift modulation.

Chapter 3 develops a time-domain analytical model and presents a common-mode equivalent circuit for the single-phase full-bridge inverter.

Chapter 4 proposes a method for characterizing FBPM wiring parasitic inductances using S-parameter measurements.

Chapter 5 describes a non-destructive approach for characterizing FBPM parasitic capacitances through time-domain measurements on the inverter circuit.

Chapter 6 simulates the voltage and current waveforms of the full-bridge circuit using the presented analytical model and subsequently analyzes the conducted emissions spectrum.

Chapter 7 concludes the thesis by summarizing key contributions.

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Osaka, December 2025

Contents

Abstract i

Acknowledgement iii

Contents iv

1 Introduction 1

1.1 EMC Standards . . . 2

1.2 Conducted Emissions Measurement . . . 5

1.3 Literature Review . . . 8

1.4 Thesis Outline . . . 12

2 SiC Full-Bridge Power Module 14

2.1 SiC MOSFET . . . 15

2.1.1 Equivalent Circuit Model . . . 16

2.1.2 Parasitic Capacitances: C_{gs}, C_{ds} and C_{dg} . . . 18

2.1.3 Transfer Characteristics, i_{ch}−v_{gs} . . . 19

2.2 Single-Phase Inverter Operation . . . 20

2.3 Lumped Element Model . . . 24

2.4 Summary . . . 26

3 Non-linear Analytical Model for Circuit Response Analysis 28

3.1 Displacement Current Model . . . 28

3.1.1 Common-Mode Equivalent Circuit . . . 32

3.2 Analytical Model of Single-Phase Inverter Circuit . . . 32

3.2.1 Circuit Response Analysis for t_{dly}=0 . . . 33

3.2.2 Circuit Response Analysis for t_{dly}>0 . . . 36
3.3 Summary . . . 37

4 Parasitic Inductance Characterization 39
4.1 Full-Bridge Power Module . . . 40
4.1.1 4-Port Network . . . 40
4.1.2 Network Analysis . . . 42
4.2 S-parameter Measurement . . . 45
4.3 Power Module Wiring Parasitic Inductance Calculation . . . 47
4.3.1 4-Port Test Fixture Parasitics . . . 47
4.3.2 Parasitic Inductance Calculation . . . 48
4.4 Summary . . . 50

5 Parasitic Capacitance Characterization 52
5.1 Common-Mode Equivalent Circut analysis . . . 52
5.1.1 Circut analysis for V_{xn} . . . 53
5.1.2 Circut analysis for V_{yn} . . . 54
5.1.3 Circut analysis for V_{pn} . . . 54
5.2 Power Module to Baseplate Parasitic Capacitance Calculation . . . 57
5.2.1 Step 1: C_{bp} measurement . . . 57
5.2.2 Step 2: V_{xn}, V_{yn}, V_{pn}, v_p and v_n measurement and i_{gnd} calculation 59
5.2.3 Step 3: Parasitic Capacitance Calculation . . . 59
5.3 Summary . . . 62

6 Differential-Mode Conducted Emissions Modeling 63
6.1 Introduction . . . 63
6.2 Differential-Mode Conducted Emissions (DM-CE) Model . . . 63
6.2.1 DM-CE Measurement . . . 63
6.2.2 DM-CE Equivalent Circuit . . . 64
6.3 Simulated Full-Bridge Inverter Circuit Waveforms . . . 65
6.3.1 Line Current (i_p) Waveform . . . 65
6.4 Simulated Differential-Mode Voltage . . . 70

6.5 Summary 76

7 Conclusion **77**

7.1 Key Contributions 78

Publications **80**

References **82**

Chapter 1

Introduction

Switching power converters are fundamental building blocks in modern electronic and energy systems. They allow for efficient power conversion between alternating current (AC) and direct current (DC), adapt voltage levels to meet load requirements, and enable frequency transformation in AC systems for applications such as motor drives and grid interconnection. However, their operation introduces significant electromagnetic challenges that must be addressed to ensure system reliability and regulatory compliance. Electromagnetic Interference (EMI) noise refers to unwanted emissions in switching power converters, primarily generated due to the high switching frequency and fast turn-on and turn-off times of power devices (MOSFETs, IGBTs). This results in rapid changes in power device current and voltage, as well as high-frequency parasitic oscillations or ringing between device parasitic capacitance and circuit wiring parasitic inductance.

Electromagnetic compatibility (EMC) addresses the performance degradation of electrical and electronic equipment caused by the disturbances in the electromagnetic environment in which the equipment operates. Achieving EMC essentially involves two key requirements. First, the electromagnetic disturbances should be maintained below a level that would cause unacceptable degradation in performance of the concerned equipment. Also, all the equipment operating in the electromagnetic environment should have sufficient immunity from the disturbances present at levels considered normal for standard operating conditions. The greater an equipment's immunity to disturbances, the less stringent are the emission requirements. Conversely, the more

effectively emissions are controlled, the less restrictive the immunity requirements need to be. So, emission control and immunity performance are functionally correlated in electromagnetic compatibility design. However, it is possible that multiple disturbance phenomena may coexist within the environment, and certain combinations of these disturbances could degrade equipment performance, even when each individual disturbance remains below the permissible threshold for compatibility. In such instances, these disturbance combinations must be identified to ensure compliance with immunity requirements.

EMI noise emissions can propagate through conductive and radiative paths, adversely affecting the performance of nearby electronic equipment. In regulatory standards, EMI emissions are categorized in conducted emissions and radiated emissions. Radiated emissions refer to EMI that is directly emitted as electromagnetic waves from the power electronic equipment due to high frequency noise current in circuit generated by power device switching transients. The current loop in the circuit with parasitic inductance act as an antenna to radiate these high frequency noise. Radiated interference propagates through the air and can couple with nearby equipment via electromagnetic fields, potentially affecting their performance. Whereas, conducted emissions are unwanted electromagnetic disturbances that propagate along physical electrical conductors, such as power lines, signal cables or ground connections directly attached to the equipment, rather than through free space. In switching power converters, these emissions are primarily generated by rapid changes in current and voltage during switching transitions, which introduce high frequency components into the supply lines. Conducted interference can affect other devices connected to the same power network, either directly or due to fluctuations on common ground or return lines, which then propagate as noise along those conductors to other devices. In this study, our focus is on conducted disturbances.

1.1 EMC Standards

The International Electrotechnical Commission (IEC) publish many EMC standards, with the aim of standardization and international cooperation in the field of electrical

and electronic. CISPR and IEC Technical Committee 77 are the two IEC committees dedicated to EMC standardization. The mandatory IEC Guide 107 instructs all other IEC committees on how to incorporate these results into their work. Within CISPR, there are six largely independent subcommittees. CISPR/A focuses on test methods, while CISPR/H addresses generic limits and the models used to calculate them. CISPR/B, CISPR/D, CISPR/F, and CISPR/I concentrate on specific product groups or environments, building their work on the foundations established by CISPR/A and CISPR/H [1].

In addition to those published by CISPR, there are specific standards published by regional EMC agencies that an electrical or electronic equipment must comply with. In Japan, Electrical Appliances and Material Safety Act, also referred to as DENA, requires compliance and marking for specified and non-specified appliances, aligned with IEC standards [2]. The EMC Directive in the EU limits electromagnetic emissions from equipment to ensure that, when used as intended, it does not interfere with radio, telecommunication, or other devices. It also governs immunity, requiring equipment to resist disturbance from radio emissions[3].The Federal Communications Commission (FCC) in United States issues CFR Title 47, which provides technical regulations for radio frequency equipment and components. CFR Title 47 includes several parts, with key EMC-related sections: Part 15 for radio frequency equipment, Part 18 for ISM equipment and Part 2 for general RF equipment regulations. Each part contains sub-parts for specific equipment types. FCC rules incorporate measurement standards by reference to demonstrate compliance. These standards are typically developed by the ANSI Accredited Standards Committee C63, a leading U.S. EMC standards body focused on emission and immunity measurements, instrumentation, and test lab quality control. EMC standards can be divided into three categories: Basic Standards, Generic Standards and Product Standards [4].

1. Basic EMC Standards define the fundamental principles for assessing electromagnetic compatibility (EMC) and related performance across all products, systems, and installations. They serve as reference documents for Generic and Product Standards, focusing on general concepts, interference phenomena, and measurement techniques. These standards do not specify limits or product-specific per-

formance requirements but provide guidance for establishing limits to protect radio reception.

- CISPR 16-1-1 and 16-1-2 specify the characteristics and performance of measurement apparatus and coupling devices for conducted disturbance measurements in the frequency range $9\,\text{kHz} - 18\,\text{GHz}$, respectively. [5]
- CISPR 16-2-1 and CISPR 16-2-4 specify the method for emissions measurement and immunity measurements in the frequency range $9\,\text{kHz} - 18\,\text{GHz}$, respectively. For conducted emissions measurement, the focus is on $9\,\text{kHz} - 30\,\text{MHz}$ frequency range. [6]
- CISPR 16-4-2 focus on measurement instrumentation uncertainty

2. Generic EMC Standards define essential EMC requirements and test procedures for all products or systems operating in a given environment when no specific EMC standard exists. They include limits and reference relevant Basic Standards for test methods.

   - IEC 61000-6-3: Emission standard for residential environments
   - IEC 61000-6-4: Emission standard for industrial environments
   - IEC 61000-6-8: Emission standard for professional equipment in commercial and light-industrial locations

3. Product Family Standards outline the EMC requirements, including applicable test procedures and performance limits, for specific products, systems, or installations.

   - CISPR 11 covers the limits and method of measurement related to radio-frequency disturbances for Industrial, scientific and medical equipment in the frequency range of $9\,\text{kHz} - 400\,\text{GHz}$. [7]
   - CISPR 12 provides the limits to protect off-board receivers from radio-frequency disturbances originating from vehicles, boats and devices with internal combustion engines or traction batteries in the frequency range of $30\,\text{MHz} - 1\,\text{GHz}$. [8]

- CISPR 14-1 and CISPR 14-2 specify the emissions and immunity requirement in the frequency range $9\,\text{kHz} - 400\,\text{GHz}$ for household appliances, electric tools and similar apparatus powered by AC or DC.[9][10]
- CISPR 15 applies to conducted and radiated emissions from electrical lighting and similar equipment. [11]
- CISPR 25 applies to vehicles, boats, internal combustion engines, trailers, devices and any electronic/electrical component intended for use in vehicles, boats, trailers and devices. This document contains both limits and procedure for disturbance measurement in the frequency range of $150\,\text{kHz} - 5.925\,\text{GHz}$. [12]
- CISPR 32 and CISPR 35 define the emissions and immunity requirement for multimedia equipment with rated rms AC or DC supply voltage not exceeding 600 V.[13]
- CISPR 36 defines limits and method of measurement of radio-frequency disturbances for 3 meter distance in the frequency range of $150\,\text{kHz} - 30\,\text{MHz}$ and applies to electric and hybrid electric road vehicles for protection of off-board receivers within 10 meter distance in residential environment.[14]

1.2 Conducted Emissions Measurement

There are three types of conducted disturbances or emissions [6]:

1. Common-Mode (CM) or asymmetrical mode, which is a vector sum of voltage or current in a group of wires in relation to the reference ground.
2. Differential-Mode (DM) or symmetrical mode.
3. Unsymmetric-Mode (UM), which is the voltage between port terminal under test and reference ground.

There are two methods for measuring conducted emissions along the leads when testing an equipment for compliance with limits defined in regulatory specifications,

either voltage measurement or current measurement. Although both methods can be used to measure all three types of conducted emissions, voltage is generally preferred for CISPR compliance testing. The characteristics of detectors required to measure emissions frequency spectrum are defined in CISPR 16-1-1 [5]. These specifications usually require peak, quasi-peak or average detector for emissions measurement. Due to very long time-constant of quasi-peak and average detectors, measurements are time consuming. So, peak detectors with shorter time-constants are usually used for initial measurements. If the emission levels recorded during these initial measurements exceed the permissible limits, the process is followed by measurements using quasi-peak and average detectors.

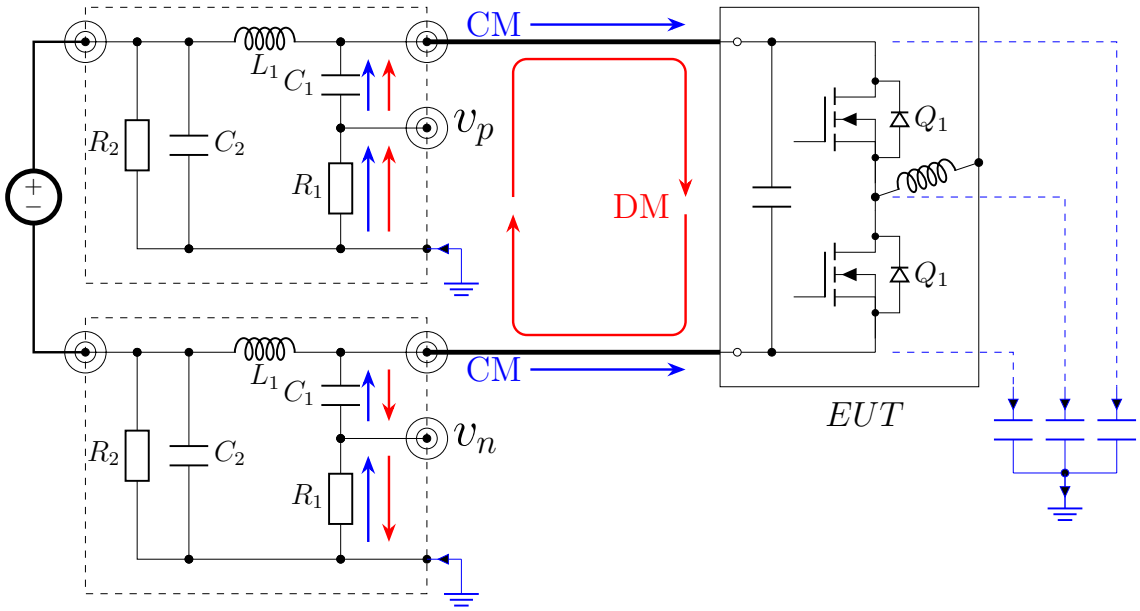


Figure 1.1 An electronic circuit with LISN inserted between DC source and EUT for conducted emissions measurement.

The CM, DM and UM network impedance are usually location dependent. Therefore, standardized testing require a known impedance, referred to as artificial network (AN) or line-impedance stabilization network (LISN), inserted between the equipment under test (EUT) and input source. The LISN simulates a long transmission line network while simultaneously decoupling the laboratory AC mains powering the input AC or DC power source. The high-voltage DC LISN schematic, as defined in CISPR 25 [12], is shown in Figure 1.2, where L_1=5 µH, C_1=0.1 µF, C_2=0.1 µF, R_1=1 kΩ and R_2=1 MΩ. The port I is connected to the input of the DC source and port O is con-

nected to the input of EUT. A measurement instrument with 50 Ω input impedance, usually a spectrum analyzer or EMI receiver is connected to RF measurement port M for emissions measurement. A large resistance across C_2 is required to discharge the capacitor in case of open-circuit. The characteristic impedance between port O and ground with a 50 Ω load on port M and port I short-circuited to ground, Z_{OG} should be with ±20% of nominal value as specified in CISPR 25 and shown in Figure 1.3.

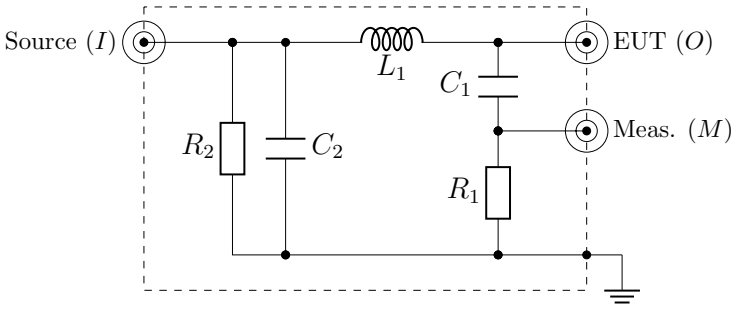


Figure 1.2 Schematic of high-voltage LISN as specified in CISPR 25.

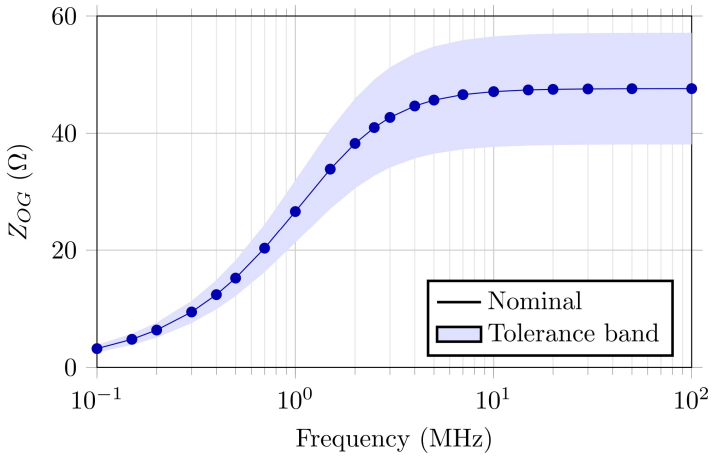


Figure 1.3 Impedance Z_{OG} between port for EUT connection and reference ground.

For conducted emissions measurement in a DC to AC power converter, LISN are connected in series with both positive and negative DC input lines, between the DC source and the EUT, as shown in Figure 1.1. The displacement current induced in the parasitic capacitances between the voltage bus of the EUT and ground due to rapid change in voltage (dv/dt) is the primary cause of common-mode noise. In an electronic circuit with switching power devices, ringing between stray circuit inductance and parasitic device capacitance results in high-frequency noise superimposed on input line current and constitutes the differential-mode current. EMC standards specify

disturbance limits for voltage method in terms of frequency-domain magnitude in dBµV of the voltage measured at the LISN RF port. In CISPR 25, focus is on protecting on-board RF receivers from disturbances originating from components or module on the vehicle. The conducted disturbance limits are listed for frequency bands of Analogue broadcast services and Mobile services, as shown in Figure 1.4

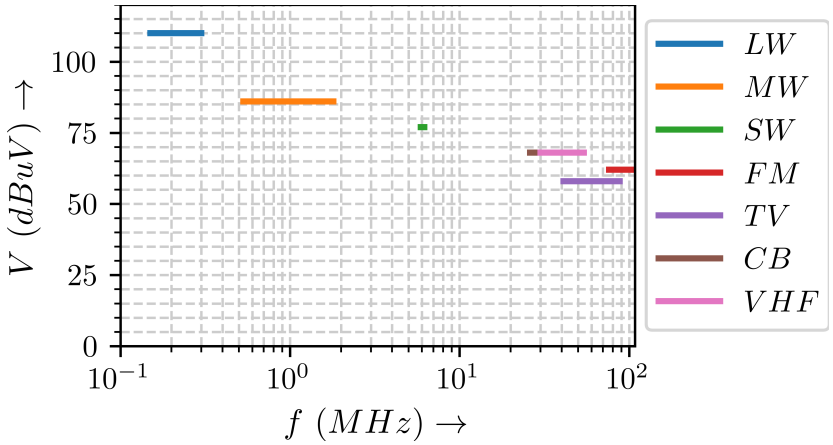


Figure 1.4 Conducted emissions limits for Class 1 devices as specified in CISPR 25.

1.3 Literature Review

The fast switching transients of SiC MOSFET and their higher parasitic oscillation frequency can increase EMI noise in the high-frequency region [15] and high frequency characteristics of power conversion circuit is an important concern. The latest generation of Silicon Carbide (SiC) MOSFET exhibit 50% lower switching losses compared to previous generation due to reduced parasitic capacitance of device [16]. In a converter circuit, circuit layout inductance and device capacitance will form an LC resonance circuit which will result in parasitic oscillations or ringing during switching transient period. An SiC MOSFET based power module will have these parasitic oscillations at higher frequency, which will shift electromagnetic interference (EMI) noise towards the high frequency region [17] [18].

Several EMI spectrum prediction techniques have been proposed in the literature [19, 20, 21, 22, 23, 24, 25, 26]. The behavioral models use Norton equivalents [19, 20, 21] and Thevenin equivalents [22] to model equivalent circuit, where current and voltage

noise sources are measured experimentally. The frequency domain model proposed in [23] uses FEM simulation to model circuit impedance and noise source waveform are modeled using multiple-slope approximation [27]. In [24], the model includes a simplified noise model derived from a 2^{nd} order circuit, where switching devices are approximated as an ideal switch during switching process. The mathematical model of EMI spectrum presented in [25] includes a time-domain expression of device drain-source voltage, however voltage dependency of device parasitic capacitance is not considered. In [26], switching voltages are mathematically modeled from their graphical representation. The behavioral model can accurately model EMI spectrum in high-frequency region as shown in literature [21]. A drawback is its reliance on experimental circuit realization and switching waveform measurements. An analytical conducted emissions model mitigates these requirements, but requires modeling of time-domain voltage and current switching transients which are influenced by device characteristics and circuit parasitics [28, 29, 33]. To analytically model conducted emissions, we have to first measure circuit layout inductances and parasitic capacitances to ground.

Several analytical models for switching transients of SiC MOSFET have been proposed, but most of them focus on device loss modeling for double-pulse test (DPT) circuit topology. The analytical modeling of switching transients requires circuit parasitics and device model. Several studies [29, 31, 30], have presented analytical model of switching transients for devices in a half-bridge circuit. In [29], constant device parasitic capacitance are used, but this can lead to inaccuracies due to the non-linearity of the parasitic capacitance. A nonlinear parasitic capacitance model was considered in [31, 30], although [31] uses a linear channel current model, whereas [30] uses a nonlinear channel current model. A semi-empirical SiC MOSFET model is described in [32] and model parameters were obtained using datasheet parameters.

Power Modules offer more power dense solution and better scalability with lower layout parasitic inductance compared to equivalent power converter design using discrete power devices, which is preferred. Full-Bridge resonant DC-DC converter topology such as phase-shifted full-bridge and single active bridge are used for power delivery applications in data centers because of their fast response time and efficiency [34], where as LLC and CLLC are used for battery charging applications in electric vehicles

[35]. For aforesaid applications, full-bridge power modules offer higher power density and lower wiring parasitics compared to using two half-bridge modules. To accurately model circuit behavior, precise measurement of power module wiring inductance and parasitic capacitance is required. However, complete parasitics model of power modules is seldom available from manufacturers. Although parasitics can be extracted using simulation tools, this requires knowledge of the layout geometry or 3D model of the power module. We can categorize the power module (PM) wiring parasitics characterization approach into calculation-based and measurement-based. The calculation-based approach uses methods such as partial element equivalent circuit (PEEC) and finite element analysis (FEA) for parasitics calculation. Software tools like FastHenry for PEEC [36], and Ansys Q3D and COMSOL for FEA [37, 38, 39] are commonly used. However, the drawback of this approach is the requirement of layout geometry or 3D Model of PM, which is not always available from the manufacturer.

For power module parasitic inductance characterization, measurement-based approach can be divided into indirect and direct measurements. The indirect approach characterizes circuit parasitic inductances using switching transients. In [40], power loop inductance of a half-bridge power module was treated as the device under test in a switching circuit consisting of a MOSFET-diode pair. The unknown parasitic inductances were then calculated using the parasitic oscillation frequency during device turn-off transient period. Accuracy of these methods depends on the precision of device transient voltage waveform measurements. The direct measurement based approach can be categorized into time-domain and frequency-domain measurement methods. The time-domain method uses time domain reflectometry (TDR) based on transmission line theory. In the literature, [41] proposes a model to profile impedance of a half-bridge power module using TDR. The frequency-domain method uses a vector network analyzer (VNA) to measure network scattering (S) parameters which are then converted to impedance (Z) parameters for network analysis.

A 2-port S-parameter measurement based method to characterize the package parasitics of a three terminal power device is presented in [42, 43, 44]. The gate terminal of discrete MOSFET is shorted to ground and 2-port measurement is performed across the drain-gate and source-gate ports as shown in Figure 1.5a. A half-bridge power mod-

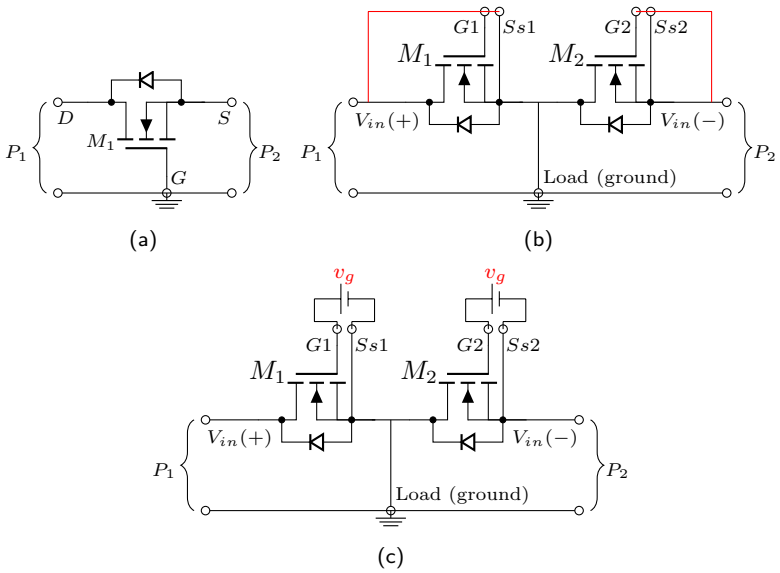


Figure 1.5 Circuit configuration for 2-port S-parameter measurement of (a) three-terminal discrete MOSFET and (b) HB-PM [44] and (c) HB-PM [47]

ule (HB-PM) parasitics characterization based on 1-port and 2-port measurements is studied in [45, 46, 47, 48, 49]. In [45, 46], 1-port measurement was performed between two terminals of the HB-PM using an impedance analyzer while the other terminals were floating, which can cause measurement errors as shown in [44]. A parasitic inductance characterization model of the HB-PM, modeled as a 3-port network, based on 2-port S-parameter measurement is presented in [47, 48, 49]. Since the HB-PM has seven terminals, there are multiple circuit configurations possible to model it as a 3-port network. In [44], five different 3-port network circuit configurations were used for five 2-port measurements to characterize the HB-PM parasitics. One of the five HB-PM circuit configurations is shown in Figure 1.5b. In [47], the load connection was shorted to ground and a positive voltage across the gate-source terminals was applied so that both MOSFET are operating in on-state, as shown in Figure 1.5c. However, no model has been proposed for either full-bridge or three-phase power modules due to the complexity of circuit analysis and S-parameter measurement.

The common-mode (CM) conducted emissions is caused by displacement current flowing through the parasitic capacitance between the switching nodes and ground, and its magnitude is proportional to dv/dt across the capacitance [50]. In power modules, direct bonded copper (DBC) substrates which consist of copper bonded on both

sides of a AlN or Silicon Nitride based ceramic plate (insulation layer) are used. The parasitic capacitances between conductive traces on top-layer of power module and baseplate which is typically grounded for safety reasons, is dependent on area of trace and thickness and permittivity of insulation material [51]. In literature, there has been several methods presented to characterize parasitic capacitances of power modules based on finite element analysis (FEA) simulation, direct impedance measurement and time-domain waveform analysis. The FEA simulation requires knowledge of geometry and materials of power module [52], which is generally not available. The direct measurement requires deconstruction of power module including cutting off bonding wires. The parasitic capacitances can then be measured between power module terminals and baseplate using impedance analyzer [53]. However, this destructive method is not desirable especially for expensive modules. In [54], a half-bridge power module parasitic capacitance extraction model based on common-mode current ringing frequency is presented. A similar model for three-level NPC power module parasitic capacitance estimation is presented in [55]. The ringing frequency is dependent on both parasitic inductances and parasitic capacitances. A test setup with additional inductance much larger than wiring parasitics in power module, connected in series with both positive and negative input dc terminals is required for measurement. A method to measure parasitic capacitances of a full-bridge power module using a combination of time-domain measurements on conducted emissions test setup and a frequency domain measurement using an Impedance Analyzer is proposed in this paper.

1.4 Thesis Outline

Chapter 2 discusses the advantages of silicon carbide MOSFETs compared to silicon-based switching power devices and presents empirical models for the capacitances and output characteristics of the power device used in this study. We then analyze the operation of a full-bridge power module (FBPM) configured as a single-phase inverter and describe the power device transient and steady states over one switching cycle. Finally, we present a simplified lumped-element equivalent circuit model of the FBPM incorporating wiring parasitic inductances and parasitic capacitances of the power module.

Chapter 3 presents an analytical model of a single-phase full-bridge inverter circuit variables such as voltage and current across passive circuit elements and power device state-variables such as drain-source voltage and drain current during transient-state. We will also present a common-mode equivalent circuit model for the full-bridge inverter circuit.

Chapter 4 introduce a method to characterize the wiring parasitic inductances of a FBPM using S-parameter measurements. We first study a lumped-element circuit model of the FBPM as a 4-port network and model the parasitic inductances in terms of network's Z-parameters. Then, we discuss the experimental measurement of FBPM S-parameters and subsequent conversion from S-parameters to Z-parameters. Finally, we compare the parasitic inductances obtained from measurements with finite element method (FEM) simulation results for validation.

Chapter 5 presents a non-destructive method to characterize parasitic capacitances in the FBPM using experimental measurement data. The parasitic capacitances between the conductive traces on top-layer and baseplate of the power module are characterized in terms of voltages between power circuit switching nodes modeled as noise sources in the common-mode equivalent circuit and voltages measured at LISN output ports on positive and negative input dc line. Then we calculate the parasitic capacitance values using the experimental data and validate them by comparing with FEM simulation results.

Chapter 6 builds upon the work presented in Chapter 2 to 5 by analytically modeling the voltage and current waveforms of the full-bridge circuit using the non-linear differential equations introduced in Chapter 3, incorporating the empirical SiC MOSFET characteristics discussed in Chapter 2, the measured parasitic inductances of the power module from Chapter 4, and the parasitic capacitances identified in Chapter 5. Subsequently, a frequency-domain equivalent circuit is presented to predict the differential-mode conducted emission noise of the full-bridge circuit.

Chapter 7 concludes the work presented in this thesis and presents an outline of the key contributions.

Chapter 2

SiC Full-Bridge Power Module

Power modules provide a more power dense, scalable solution with lower layout parasitic inductances compared to equivalent power converter designs using discrete power devices, which is preferred. For design of full-bridge power converter topologies, a full-bridge power module (FBPM) will offer higher power density and lower wiring parasitics compared to using two half-bridge modules. In this research we will be using a FBPM for analysis and its 3D model is shown in Figure 2.1. In this chapter, we first present an equivalent circuit model of a silicon carbide (SiC) based MOSFET and empirically model the transfer-characteristics and capacitances of the device used in this research work, which is required for power device switching transients modeling. Then we will discuss the single-phase inverter operation of the power module using phase-shift modulation and present a simplified lumped-element model of full-bridge

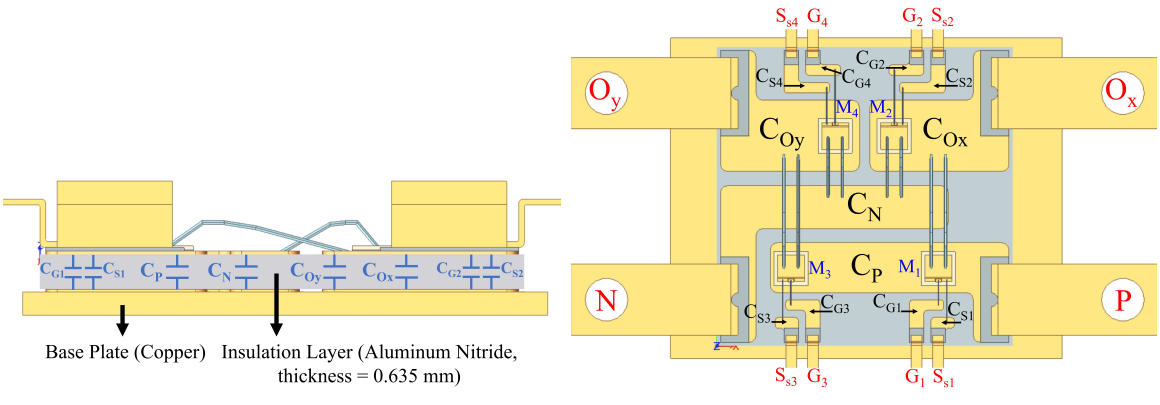


Figure 2.1 Full-Bridge Power Module (a) side-view (no-to-scale) and (b) top-view

power module consisting of wiring parasitic inductances and parasitic capacitances.

2.1 SiC MOSFET

In power electronics applications, vertical n-channel MOSFET are generally used, and their typical structure is shown in Figure 2.2a. An n^- drift layer is grown on n substrate and n^+ and p regions are formed on the top of drift layer [56]. An oxide layer is grown on the top, overlapping drift region and p region to form the gate dielectric. Metal contacts are deposited on the n^+ substrate to form the drain terminal, on the gate-oxide to form the gate terminal and on the top overlapping $p - n^+$ region to form the source terminal. When a positive voltage higher than a threshold is applied between gate-source terminals, a channel is formed below the gate-oxide in p region. When drain-source is positive biased, a current will flow from drain to source terminal through the channel. The p and n^- regions will also form a pn junction diode and when drain-source is reverse biased, a current could also flow from source to drain terminal even if inversion channel is not formed.

For the design of switching power converters, breakdown voltage and operation losses of power devices such as MOSFET are critical considerations. During on-state, conduction losses mainly depend on the drift region resistance r_{drift} and inversion channel resistance r_{ch} [57]. The breakdown voltage (V_B) of the device increases with an increase in n^- drift region thickness and a decrease in its doping concentration [58]. However, this will also increase r_{drift} which is detrimental to conduction loss of device. The r_{drift} is proportional to V_B^2 while total on-state device resistance is proportional to $V_B^{2.3-2.5}$ [59, 60, 61]. In case of silicon (Si) based MOSFET, r_{drift} increases considerably when V_B is increased beyond 1 kV [56, 61].

For wide-bandgap semiconductor materials such as silicon-carbide (SiC), drift region can be made much thinner for same breakdown voltage due to its much higher breakdown electric field compared to Si [62]. For power device application, 4H-SiC polytype is now preferred due to higher electron mobility and bandgap compared to 3C-SiC and 6H-SiC polytypes [59, 63, 64]. A comparison of physical properties of 4H-SiC and Si is given in Table 2.1 [65]. However, due to interface defect between oxide

layer and 4H-SiC layer, inversion channel mobility is typically $10-70\,\mathrm{cm}^2/\mathrm{Vs}$, which is very low compared to bulk electron mobility of 4H-SiC material [59, 66, 67, 68, 69]. This will result in much higher r_{ch} for SiC-MOSFET compared to Si-MOSFET with typical channel mobility of $420-550\,\mathrm{cm}^2/\mathrm{Vs}$ [57]. However, r_{drift} of SiC device is 500 times lower than Si device resulting in much lower total on-state resistance [70]. Another advantage of SiC power devices is their ability to operate at very high temperature [71][72]. This is due to much lower intrinsic carrier concentration in SiC material compared to Si because of higher bandgap energy [73]. This results in much lower leakage current in SiC devices which improves reliability of device operation at high temperature. SiC MOSFET are preferred for application with required voltage rating of $800\,\mathrm{V} - 6.5\,\mathrm{kV}$ due to comparatively low on-state resistance and high switching frequency [74, 75, 76]. However, for ultra-high voltage applications, bipolar devices such as Si-IGBT are preferred due to lower on-state voltage drop at rated current compared to SiC MOSFET [57, 77].

Table 2.1 Physical properties of 4H-SiC and Si at room temperature[65].

	SiC	**Si**
Bandgap (eV)	3.26	1.12
Electron mobility ($\mathrm{cm^2V^{-1}s^{-1}}$)	1200	1350
Breakdown electric field (MV/cm)	2.8	0.3
Thermal conductivity (W $\mathrm{cm^{-1}}$ $\mathrm{K^{-1}}$)	3.3–4.9	1.3–1.5
Relative dielectric constant	9.8	11.9

Planar type vertical SiC-MOSFET were first introduced in the 1990's [78, 79, 80] and have been superseded by trench-gate type SiC-MOSFET due to much lower r-on and parasitic capacitances resulting in lower conduction and switching losses [81, 82, 83]. In this research work, we will be using a SiC-MOSFET with double-trench gate structure from ROHM Inc., as shown in Figure 2.2b.

2.1.1 Equivalent Circuit Model

In transient-state, power device is operating in saturation region and its equivalent circuit is give by Figure 2.3a. The device impedance Z_M in this state can be modeled

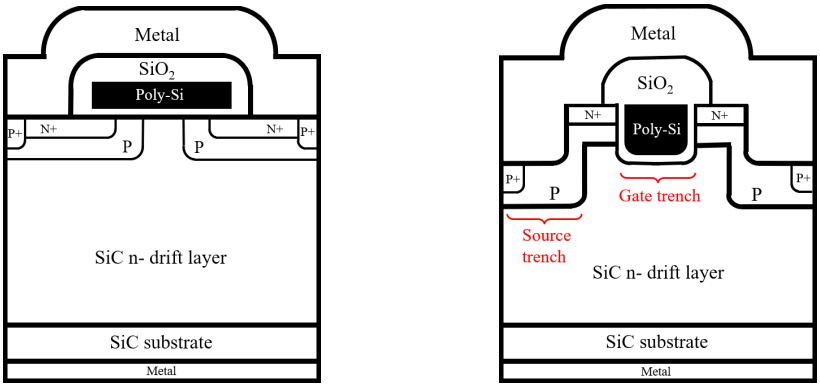


Figure 2.2 Comparison of SiC MOSFET with (a) planar-type structure and (b) double-trench structure from ROHM Inc.

as Eq.(2.1), where Z_i is given by Eq.(2.2), r_{ds} is the channel resistance and C_{ds}, C_{dg} and C_{gs} are voltage dependent device parasitic capacitances. During on-state, as shown in Figure 2.3b, device is operating in ohmic region, $r_{ds} \ll Z_i$ and its impedance can be approximated as $Z_M \approx r_{ds} = v_{ds}/i_{ch}$. In off-state, as shown in Figure 2.3c, device is operating in cut-off region where $r_{ds} \gg Z_i$ and $Z_M \approx Z_i$.

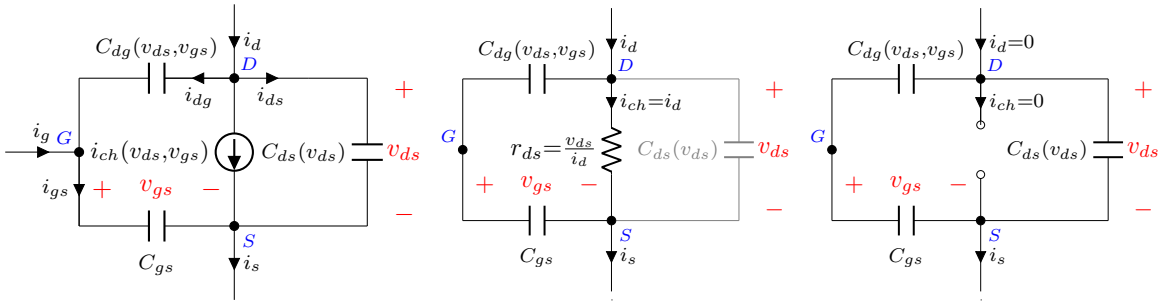


Figure 2.3 SiC MOSFET equivalent circuit during (a) transient-state, (b) on-state and (c) off-state.

$$Z_M = \left[{r_{ds}}^{-1} + {Z_i}^{-1}\right]^{-1} \tag{2.1}$$

$$Z_i = \left[j2\pi f \left(C_{ds}(v_{ds}) + \frac{C_{gs}C_{dg}(v_{ds},v_{gs})}{C_{gs}+C_{dg}(v_{ds},v_{gs})}\right)\right]^{-1} \tag{2.2}$$

2.1.2 Parasitic Capacitances: C_{gs}, C_{ds} and C_{dg}

The SiC MOSFET drain-source capacitance C_{ds}, drain-gate capacitance C_{dg} and gate-source capacitance C_{gs} have bias voltage dependency. In literature [31, 84] , C_{ds} and C_{dg} are modeled using non-linear equations with model parameter in power of bias voltage (V_{ds}^{x}, V_{dg}^{x}). It is difficult to curve-fit power law as initial value of model parameters automatically generated by programs (such as MATLAB, Python, *R*, etc.) may not be helpful. It may require multiple trial and error approach to get the desired result.

To derive the proposed empirical model for C_{ds}, first tangents l_1 and l_2 are drawn to the measured C_{ds}−V_{ds} curve at second and second last data point, as shown in Figure 2.4a. The line l_h bisects l_1-l_2 and intersects the measured C_{ds} at points (x, y). Now we rotate C_{ds} around the points (x, y) by an angle θ such that l_h is perpendicular to the y-axis. The C_{ds} in new co-ordinate system is denoted by $C_{ds\text{-}\theta}$ and V_{ds} by $V_{ds\text{-}\theta}$. The measured C_{ds}−V_{ds} is transformed to $C_{ds\text{-}\theta}$−$V_{ds\text{-}\theta}$ by Eqs. (2.3)-(2.4). The rotated $C_{ds\text{-}\theta}$−$V_{ds\text{-}\theta}$ resembles a hyperbolic-curve and is modeled by Eq. (2.5). The model parameters x, y and θ can be easily calculated using linear mathematics and geometry, and z_1, z_2, z_3 and z_4 were obtained from curve fitting $C_{ds\text{-}\theta}$ to Eq. (2.5) using *R* (programming language). Finally, modeled $C_{ds\text{-}\theta}$ is transformed back to the initial co-ordinate system by Eq. (2.6). A simplified equation (2.7) can be obtained from Eqs. (2.3)-(2.6) to model C_{ds}−V_{ds}.

The device capacitance C_{dg} for V_{dg} was also modeled by Eq. (2.7), and C_{gs} is assumed to be constant. To improve accuracy at low bias voltage, C_{dg} for $V_{dg} \leq 10\,\mathrm{V}$ was modeled as a trigonometric fourier series given by Eq. (2.8), where model parameters w, p, q_i and r_i were obtained using *R*. The model parameters for C_{ds} and C_{dg} are given in Table 2.2. In literature[31], C_{ds} and C_{dg} are modeled using non-linear equations. The measured C_{ds}−V_{ds} and C_{dg}−V_{dg} are compared with device capacitances modeled using the proposed empirical model and non-linear model in literature[31], as shown in Figure 2.4b and Figure 2.4c.

$$V_{ds\text{-}\theta} = (V_{ds} - x)\cos\theta - (C_{ds} - y)\sin\theta + x \tag{2.3}$$

$$C_{ds\text{-}\theta} = (V_{ds} - x)\sin\theta + (C_{ds} - y)\cos\theta + y \tag{2.4}$$

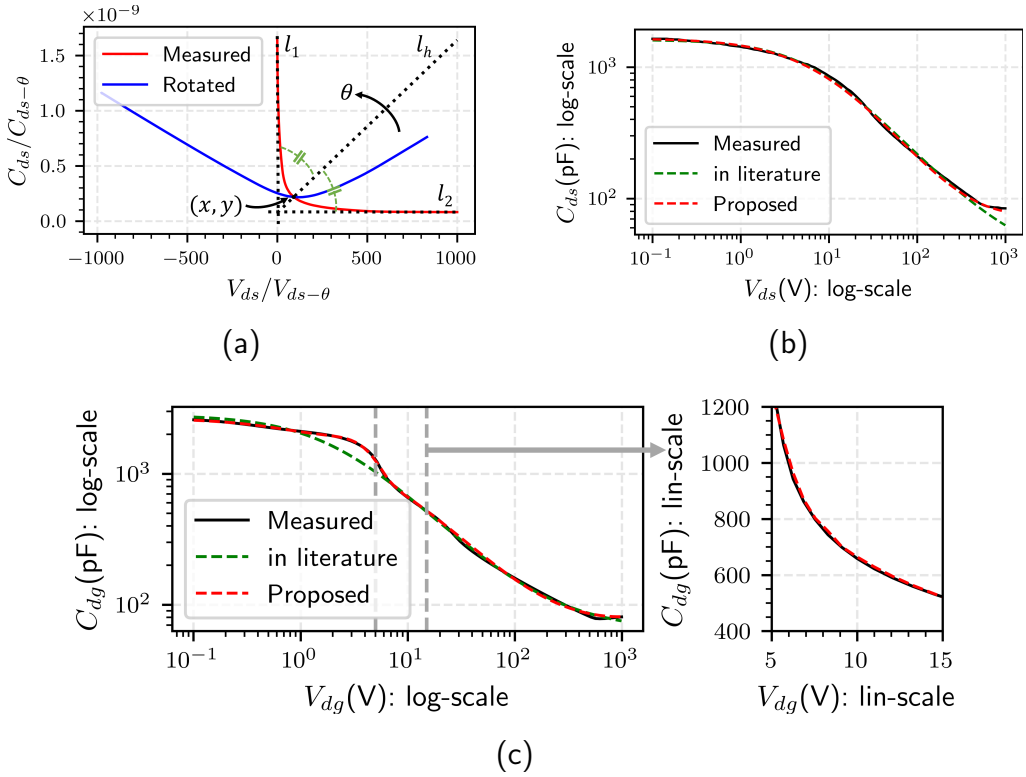


Figure 2.4 SiC MOSFET (a) $C_{ds}-V_{ds}$ in rotated co-ordinated system, and (b) C_{ds} vs. V_{ds} and (c) C_{dg} vs. V_{dg} comparison for modeled and measured data.

$$C_{ds\text{-}\theta} = z_1\sqrt{(V_{ds\text{-}\theta} + z_2)^2 + z_3^2} + z_4 \tag{2.5}$$

$$C_{ds} = \frac{C_{ds\text{-}\theta} - y - (V_{ds} - x)\sin\theta}{\cos\theta} + y \tag{2.6}$$

$$\begin{aligned} C_{ds} \;=\; & c\left\{d + \left[e + fV_{ds} - \left(-g - hV_{ds} + (1 + kV_{ds})^2\right)^{\frac{1}{2}}\right]^2\right\}^{\frac{1}{2}} \\ & + a - bV_{ds} \end{aligned} \tag{2.7}$$

$$C_{dg} = p + \sum_{i=1}^{3} q_i \cos(wV_b) + r_i \sin(wV_b) \tag{2.8}$$

2.1.3 Transfer Characteristics, $i_{ch}-v_{gs}$

The SiC MOSFET $i_{ch}-v_{gs}$ transfer characteristics were modeled as a Gaussian function by Eq. (2.9) and model parameters are given in Table 2.2. The measured and modeled transfer characteristics for low and high current values are shown in Figure 2.5.

Table 2.2 SiC MOSFET parasitic capacitance model parameters in Eq. (2.7) and Eq. (2.8) and transfer characteristics model parameters in Eq. (2.9).

	C_{ds}	C_{dg}		$C_{dg}(V_b \leq 10\,\mathrm{V})$		i_{ch}–v_{gs}
a	40.4867	33.5421	p	$3.747{\cdot}10^{11}$	a_1	3.048
b	0.99578	-1	q_1	$-5.608{\cdot}10^{11}$	b_1	7.399
c	24634	89614	q_2	$2.227{\cdot}10^{11}$	c_1	-0.824
d	0.000116	$4.375{\cdot}10^{-6}$	q_3	$-3.668{\cdot}10^{10}$	a_2	382.928
e	0.117675	0.014745	r_1	$4.018{\cdot}10^{10}$	b_2	12.108
f	0.007779	0.000932	r_2	$-3.208{\cdot}10^{10}$	c_2	1.264
g	0.997171	0.999962	r_3	$7.995{\cdot}10^{9}$		
h	0.01379	0.001858	w	-0.0120		
k	0.00782	0.000943				

$$i_{ch} = \begin{cases} \sum_{n=1}^{2} a_n \exp\left(-\frac{(v_{gs}-b_n)^2}{c_n^2}\right), & v_{gs} > v_{th} \\ 0, & v_{gs} \leq v_{th} \end{cases} \tag{2.9}$$

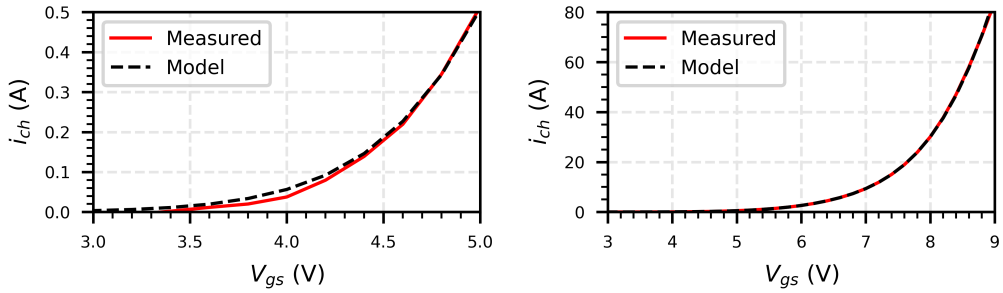


Figure 2.5 SiC MOSFET Transfer Characteristics.

2.2 Single-Phase Inverter Operation

The single-phase full-bridge inverter circuit under consideration is shown in Figure 2.6. It consists of two half-bridge or legs, Leg-A with devices M_1 and M_2 and Leg-B with devices M_3 and M_4. A phase-shift modulation scheme with dead-time t_d is used for inverter operation, as shown in Figure 2.7 where v_{gi} is gate signal corresponding to

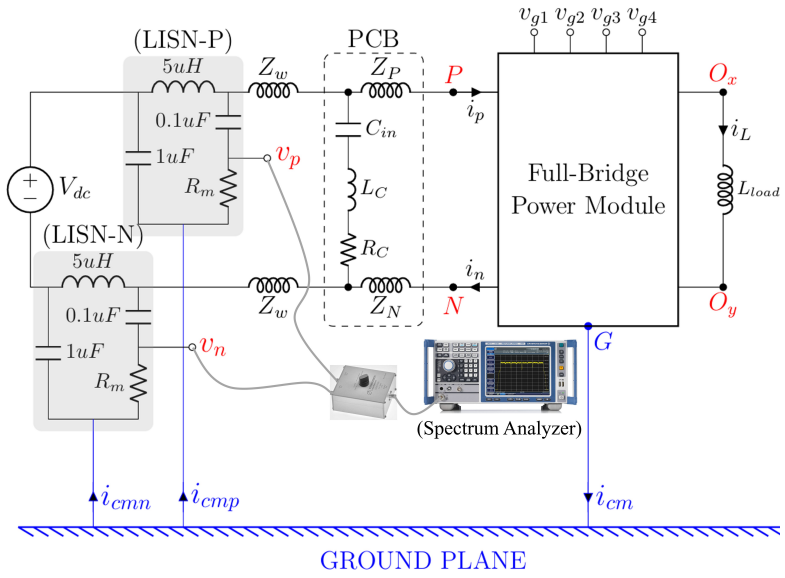


Figure 2.6 Conducted emissions (CE) test circuit for FBPM operating as single-phase inverter.

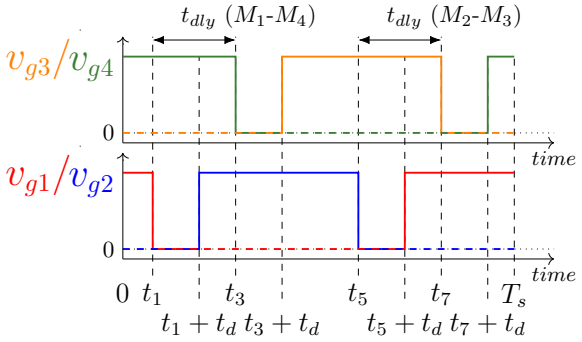


Figure 2.7 Phase-shift modulation gate signals,

device M_i for $i \in \{1, 2, 3, 4\}$. The phase-shift corresponds to the delay of time t_{dly} for switching between leg-A and leg-B. The devices on same leg switch at half-cycle shift . For one switching time-period T_s, single-phase inverter operation waveform for $t_{dly} > t_d$ are shown in Figure 2.8, where i_{di}, v_{dsi} and v_{gsi} are drain current, drain-source voltage and gate-source voltage of device M_i for $i \in \{1, 2, 3, 4\}$ in FBPM. The operation can be divided into 8 modes, detailed as follows:

1. S_{tr1} $(t_1 \rightarrow t_2)$: This mode starts when v_{g1} is pulled to low-state, i_{d1} starts decreasing, and the difference $i_L - i_{d1}$ starts flowing through M_2. This mode ends when the load current commutates from M_1 to body-diode of M_2.

2. S_1 $(t_2 \rightarrow t_3)$: Both low-side devices, M_2 and M_4 are in on-state and voltage across

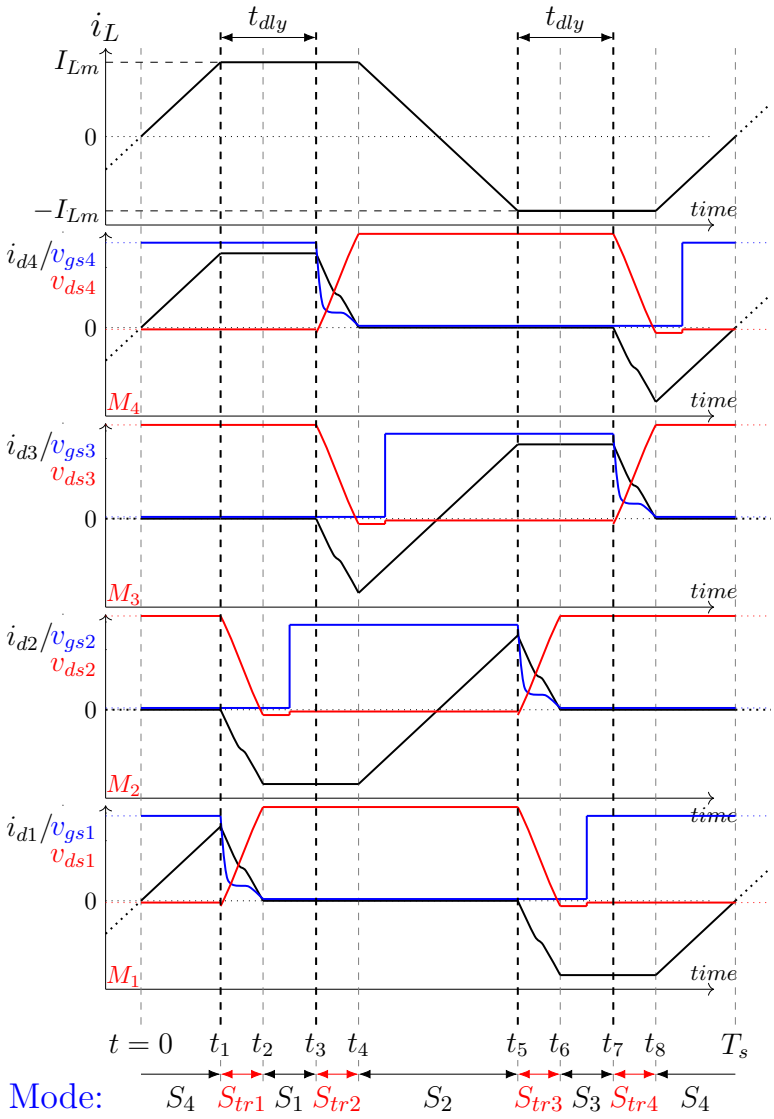


Figure 2.8 Single-Phase inverter operation waveform of switching devices for one switching cycle (not showing the parasitic oscillations) for $t_{dly} > t_d$.

load is zero. Initially the body-diode of M_2 is conducting. At $t = t_2 + t_d$, v_{g2} is pulled to high-state and channel of M_2 starts conducting.

3. S_{tr2} ($t_3 \rightarrow t_4$): This mode starts when v_{g4} is pulled to low-state, id_4 starts decreasing, and the difference $i_L - i_{d4}$ starts flowing through M_3. This mode ends when the load current commutates from M_4 to body-diode of M_3.

4. S_2 ($t_4 \rightarrow t_5$): M_2-M_3 are in on-state and M_1-M_4 are in off-state. Initially the body-diode of M_3 is conducting. At $t = t_4 + t_d$, v_{g3} is pulled to high-state and channel of M_3 starts conducting.

Table 2.3 Single-Phase Inverter Mode of Operation - Time Model

time	$t_{dly} > 0$	$t_{dly} = 0$
t_0	0	0
t_1	$t_0 + [(T_s/2) - (t_{M2-off} + t_{dly} + t_{M3-off})]/2$	$t_0 + [(T_s/2) - (t_{M2-off}]/2$
t_2	$t_1 + t_{M1-off}$	$t_1 + t_{M1-off}$
t_3	$t_2 + t_{dly}$	$t_2 + 0$
t_4	$t_3 + t_{M4-off}$	$t_3 + 0$
t_5	$t_4 + (T_s/2) - (t_4 - t_1)$	$t_4 + (T_s/2) - t_{M1-off}$
t_6	$t_5 + t_{M2-off}$	$t_5 + t_{M2-off}$
t_7	$t_6 + t_{dly}$	$t_6 + 0$
t_8	$t_7 + t_{M3-off}$	$t_7 + 0$
t_9	T_s	T_s

5. S_{tr3} ($t_5 \rightarrow t_6$): This mode starts when v_{g2} is pulled to low-state, i_{d2} starts decreasing, and the difference $i_L - i_{d2}$ starts flowing through M_1. This mode ends when the load current commutates from M_2 to body-diode of M_1.

6. S_3 ($t_6 \rightarrow t_7$): Both high-side devices, M_1 and M_3 are in on-state and voltage across load is zero. Initially the body-diode of M_1 is conducting. At $t = t_6 + t_d$, v_{g1} is pulled to high-state and channel of M_1 starts conducting.

7. S_{tr4} ($t_7 \rightarrow t_8$): This mode starts when v_{g3} is pulled to low-state, id_3 starts decreasing, and the difference $i_L - i_{d3}$ starts flowing through M_4. This mode ends when the load current commutates from M_3 to body-diode of M_4.

8. S_4 ($t_8 \rightarrow t_1$): M_1-M_4 are in on-state and M_2-M_3 are in off-state. Initially the body-diode of M_4 is conducting. At $t = t_8 + t_d$, v_{g4} is pulled to high-state and channel of M_4 starts conducting.

The load current i_L will rise and fall with a constant slope of $\approx V_i/L_{out}$ during mode S_2 and S_4 and peak load current I_{Lm} given by Eq. (2.10), where V_i is the input DC voltage and L_{out} is the load inductance. When $t_{dly} = 0$, t_1 is equal to t_3 and t_5 is equal to t_7 and model can be simplified to 4 modes of operation. The time instances shown in Figure 2.8 can be calculated by Table 2.3, where t_{Mi-off} is the turn-off time of power devices.

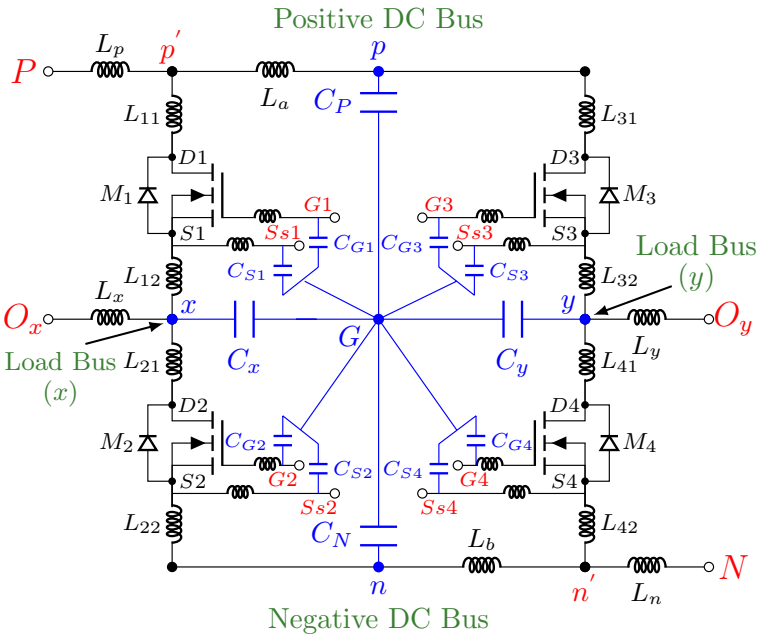


Figure 2.9 Full-Bridge Power Module lumped-element model.

$$I_{Lm} = \frac{V_i}{4L_{out}}\left(T_s - 2t_{dly}\right) \tag{2.10}$$

2.3 Lumped Element Model

The full-bridge power module (FBPM) consist of two half-bridge or legs, leg-A with devices M_1 and M_2 and leg-B with devices M_3 and M_4. A 3D wiring model of a FBPM under evaluation in this paper is shown in Figure 2.1. The FBPM has four power bus on the top-layer of DBC: P, N, O_x and O_y, and each bus and baseplate will have parasitic capacitances: C_P, C_N, C_{Ox} and C_{Oy}. Additionally, copper traces on the top-layer connected to gate terminal G_i and kelvin-source terminal S_{si} of each MOSFET and baseplate will have parasitic capacitances C_{Gi} and C_{Si} for $i \in \{1, 2, 3, 4\}$. A FBPM lumped-element model is shown in Figure 2.9 with wiring parasitic inductances and parasitic capacitances, where G is the fictitious uniform reference potential on the baseplate of module.

The equivalent-circuit of FBPM between nodes p' and x for all operation modes discussed in Section 2.2, is shown in Figure 2.10. The device M_1 is in off-state and on-state for modes $S_1 - S_{tr2} - S_2$ and $S_3 - S_{tr4} - S_4$, respectively. For modes S_{tr1} and

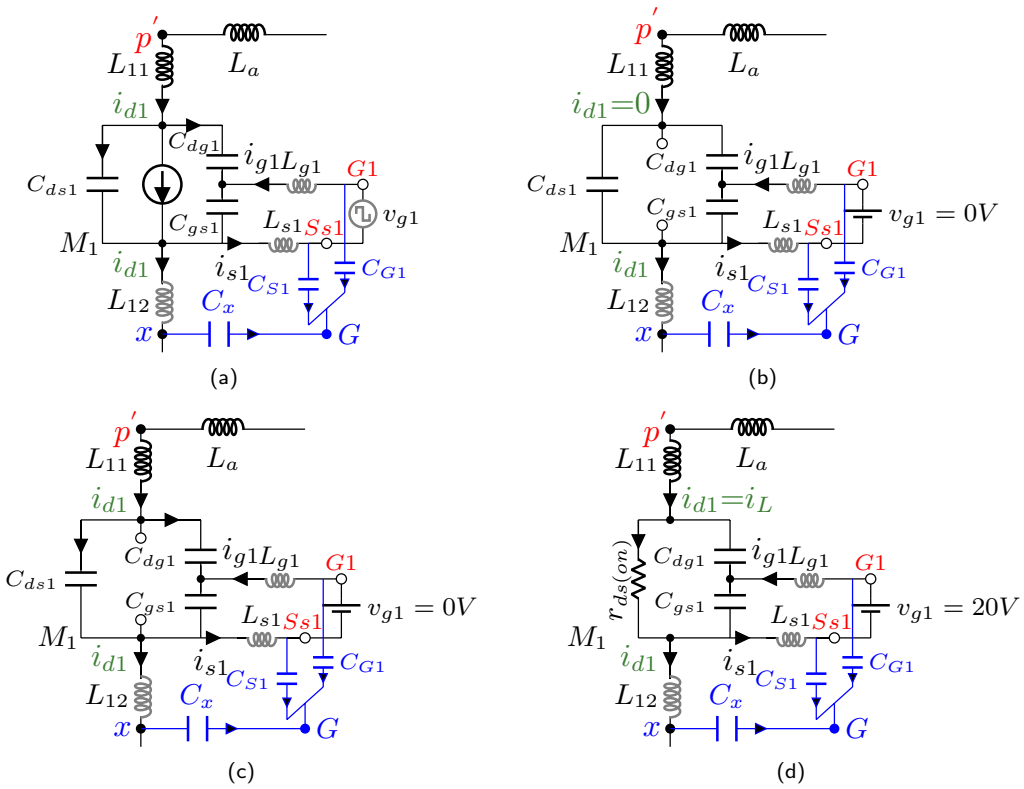


Figure 2.10 Equivalent circuit across nodes $p^{'}$ and x during mode (a) S_{tr1}, (b) $S_1 - S_{tr2} - S_2$, (c) S_{tr3} and (d) $S_3 - S_{tr4} - S_4$.

S_{tr3}, M_1 is operating in transient-state. KVL for loop $G - x - S_{s1}$ can be differentiated as Eq. (2.11), where V_{Cx} and V_{CS1} are voltages across C_x and C_{S1}, respectively. As L_{12} and L_{s1} are negligibly small, Eq. (2.11) can be approximated for all modes. Similarly, KVL for loop $G - x - G_1$ can be differentiated as Eq. (2.12), where V_{Cgs1} and V_{CG1} are voltages across C_{gs1} and C_{G1}, respectively. Here, L_{12} and L_{g1} are also negligibly small and v_{g1} is constant during modes $S_1 - S_{tr2} - S_2$, S_{tr3} and $S_3 - S_{tr4} - S_4$. Although, v_{g1} is transitioning from high to low in mode S_{tr1}, dv_{g1}/dt is negligible compared to the power loop dv/dt which appears across C_x. Then dv_{g1}/dt can be assumed to be 0 for all modes and with neglecting L_{12} and L_{g1}, Eq. (2.12) can be approximated. The Eq. (2.11) and Eq. (2.12) result in $dV_{Cx}/dt \approx dV_{CS1}/dt \approx dV_{CG1}/dt$ and total displacement current flowing from x to G can be calculated with combined capacitance $C_x^{'} = C_x + C_{G1} + C_{S1}$.

$$\frac{dV_{Cx}}{dt} = -L_{12}\frac{d^2 i_{d1}}{dt^2} + L_{s1}\frac{d^2 i_s}{dt^2} + \frac{dV_{CS1}}{dt} \approx \frac{dV_{CS1}}{dt} \tag{2.11}$$

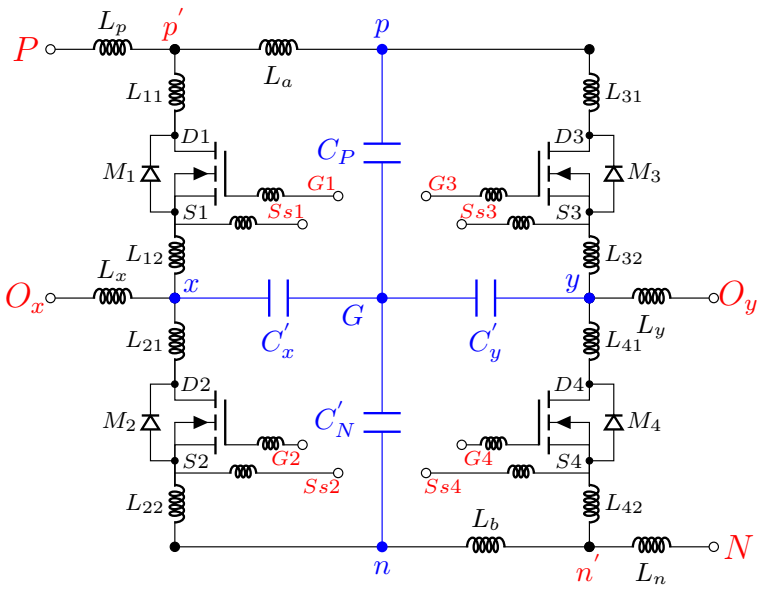


Figure 2.11 Simplified FBPM lumped-element model with combined parasitic capacitance.

$$\begin{aligned} \frac{dV_{Cx}}{dt} &= -L_{12}\frac{d^2 i_{d1}}{dt^2} - \frac{dV_{Cgs1}}{dt} - L_{g1}\frac{d^2 i_g}{dt^2} + \frac{dV_{CG1}}{dt} \\ &\approx -\frac{dv_{g1}}{dt} + \frac{dV_{CG1}}{dt} \approx \frac{dV_{CG1}}{dt} \end{aligned} \tag{2.12}$$

Similar approximation can be made across nodes y and G, where L_{32}, L_{g3} and L_{s3} are neglected and C_y, C_{G3} and C_{S3} are combined as $C'_y = C_y + C_{G3} + C_{S3}$ to obtain displacement current flowing from y to G. For branch between nodes n and G, L_{22}, L_{g2}, L_{s2}, L_{42}, L_b, L_{g4} and L_{s4} are neglected and C_{G2}, C_{S2}, C_{G4} and C_{S4} are combined with C_N as $C'_N = C_N + C_{G2} + C_{S2} + C_{G4} + C_{S4}$ to obtain displacement current flowing from n to G. The total parasitic capacitance of FBPM is hereafter referred as $C_{bp} = C_P + C'_x + C'_x + C'_N$. The simplified lumped element circuit model of FBPM is Figure 2.11.

2.4 Summary

We first discussed the advantages of silicon carbide (SiC) MOSFETs compared to silicon-based power devices. Next, we presented a new empirical model for the capacitances of S4103 1200V/95A bare-die SiC MOSFET used in this research work and compared its accuracy with models proposed in the literature. Subsequently, we ana-

lyzed the operation of a full-bridge power module (FBPM) configured as a single-phase inverter driving an inductive load using phase-shift modulation. Finally, we presented a simplified lumped-element circuit model of the FBPM with combined parasitic capacitances.

Chapter 3

Non-linear Analytical Model for Circuit Response Analysis

As discussed in the literature review in Chapter 1, modeling of power device switching transients has primarily focused on half-bridge circuits with discrete devices. In this chapter, we will present an analytical time-domain model of single-phase inverter circuit variables such as voltage and current across passive circuit elements and power device state-variables such as drain-source voltage and drain current during transient-state. We will also present a common-mode equivalent circuit model for the single-phase inverter circuit.

3.1 Displacement Current Model

The circuit diagram of conducted emissions measurement test circuit is shown in Figure 3.1, where i_{cp}, i_{cx}, i_{cy} and i_{cn} are the displacement currents induced by voltages v_{cp}, v_{cx}, v_{cy} and v_{cn} across FBPM parasitic capacitances C_P, C'_x, C'_y and C_N, respectively. The relationship between voltage across parasitic capacitances and induced displacement current is given by Eq. (3.1). The currents in power module positive and negative line, i_p and i_n are given by Eqs. (3.2)-(3.3). Also, the voltage v_{fb} across power module input terminals P and N is given by Eq. (3.4). The capacitor at the input terminal of power module is modeled as series $C_{in} - L_C - R_C$.

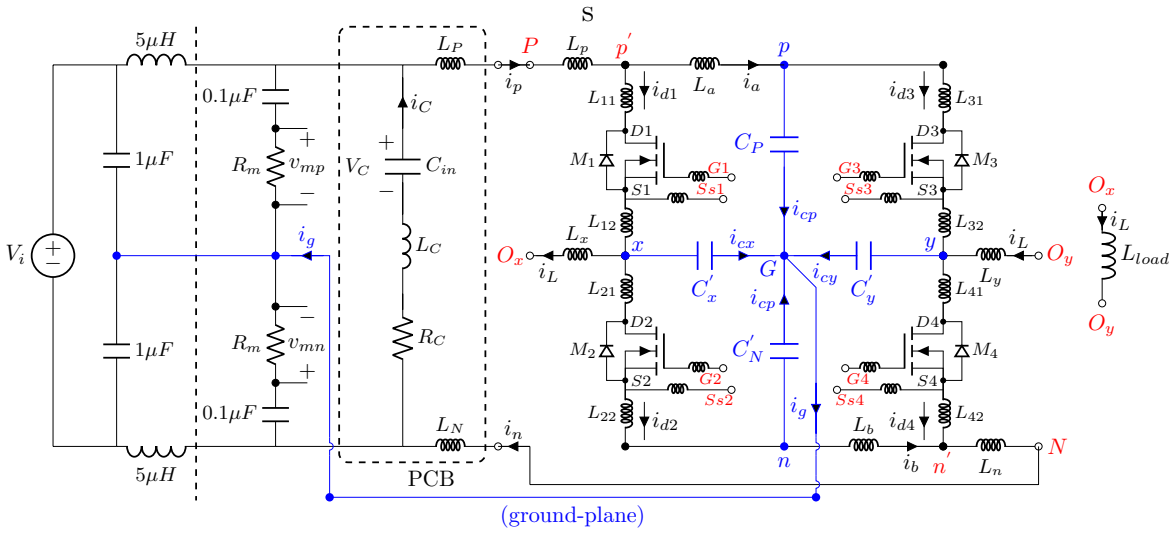


Figure 3.1 Conducted emissions measurement lumped circuit model including LISN, input capacitor and power module.

$$i_{cp} = C_P \frac{dv_{cp}}{dt},\ i_{cx} = C'_x \frac{dv_{cx}}{dt},\ i_{cy} = C'_y \frac{dv_{cy}}{dt},\ i_{cn} = C'_N \frac{dv_{cn}}{dt} \tag{3.1}$$

$$i_p = i_{d1} + i_a = i_{d1} + (i_{d3} + i_{cp}) \tag{3.2}$$

$$i_n = i_{d4} + i_b = i_{d4} + (i_{d2} - i_{cn}) \tag{3.3}$$

$$v_{fb} = V_C - L_P \frac{di_p}{dt} - L_N \frac{di_n}{dt} - L_C \frac{di_C}{dt} \tag{3.4}$$

The voltages v_{mp} and v_{mn} across LISN measurement resistance are due to differential-mode current i_{dm} and ground or common-current i_g. The i_{dm} is common to both positive and negative side LISN measurement resistances, while i_g is split into i_{gp} and i_{gn}.

$$v_{mp} = R_m(-i_{gp} - i_{dm}) \tag{3.5}$$

$$v_{mp} = R_m(-i_{gp} + i_{dm}) \tag{3.6}$$

Using KVL, we can write Eqs. (3.7)-(3.9), where voltage $v_k = v_{ds\text{-}k} + L_k(di_{d\text{-}k}/dt)$ for $k \in \{1, 2, 3, 4\}$, where $L_k = L_{k1} + L_{k2}$, $v_{ds\text{-}k}$ is voltage across drain-source terminals of power device M_k and $i_{d\text{-}k}$ is the drain current. The ground current i_g is summation of displacement currents induced in parasitic capacitances and is given by Eq. (3.10).

$$v_{fb} - v_a - v_{cp} + v_{cx} - v_2 - v_b = 0 \tag{3.7}$$

$$v_2 - v_{cx} + v_{cn} = 0 \tag{3.8}$$

$$v_4 - v_{cy} + v_{cn} = 0 \tag{3.9}$$

$$i_g = i_{cp} + i_{cx} + i_{cy} + i_{cn} \tag{3.10}$$

Now differentiating Eqs. (3.7)-(3.10) and solving those equations, we can write i_{cp}, i_{cx}, i_{cy} and i_{cn} in terms of voltages across circuit parasitic components and power devices, given by Eqs. (3.11)-(3.14).

$$i_{cp}=\frac{C_P}{C_b}\left[i_g+(C_b-C_P)\left(\frac{dv_{fb}}{dt}-\frac{dv_a}{dt}-\frac{dv_b}{dt}\right)-C_y^{'}\left(\frac{dv_4}{dt}-\frac{dv_b}{dt}\right)-C_x^{'}\frac{dv_2}{dt}\right] \tag{3.11}$$

$$i_{cx}=\frac{C_x^{'}}{C_b}\left[i_g-C_P\left(\frac{dv_{fb}}{dt}-\frac{dv_a}{dt}-\frac{dv_b}{dt}\right)-C_{y'}\left(\frac{dv_4}{dt}-\frac{dv_b}{dt}\right)+\left(C_b-C_x^{'}\right)\frac{dv_2}{dt}\right] \tag{3.12}$$

$$i_{cy}=\frac{C_y^{'}}{C_b}\left[i_g-C_P\left(\frac{dv_{fb}}{dt}-\frac{dv_a}{dt}-\frac{dv_b}{dt}\right)-\left(C_b-C_y^{'}\right)\left(\frac{dv_4}{dt}-\frac{dv_b}{dt}\right)+C_x^{'}\frac{dv_2}{dt}\right] \tag{3.13}$$

$$i_{cn}=\frac{C_N^{'}}{C_b}\left[i_g-C_P\left(\frac{dv_{fb}}{dt}-\frac{dv_a}{dt}-\frac{dv_b}{dt}\right)-C_y^{'}\left(\frac{dv_4}{dt}-\frac{dv_b}{dt}\right)-C_x^{'}\frac{dv_2}{dt}\right] \tag{3.14}$$

We can simplify Eqs. (3.11)-(3.14) to Eqs. (3.15)-(3.18), where voltages v_{xn}, v_{yn} and v_{pn} are given by Eqs. (3.19)-(3.21) and written in terms of positive and negative line current and power device drain current and voltage. The v_{xn} is voltage between nodes x and n, v_{yn} between nodes y and n and v_{pn} between p and n, as marked in Figure 3.1.

$$i_{cp} = \frac{C_P}{C_b}\left[i_g + (C_b - C_P)\frac{dv_{pn}}{dt} - C_y^{'}\frac{dv_{yn}}{dt} - C_x^{'}\frac{dv_{xn}}{dt}\right] \tag{3.15}$$

$$i_{cx} = \frac{C_x^{'}}{C_b}\left[i_g - C_P\frac{dv_{pn}}{dt} - C_y^{'}\frac{dv_{yn}}{dt} + \left(C_b - C_x^{'}\right)\frac{dv_{xn}}{dt}\right] \tag{3.16}$$

$$i_{cy} = \frac{C_y^{'}}{C_b}\left[i_g - C_P\frac{dv_{pn}}{dt} + \left(C_b - C_y^{'}\right)\frac{dv_{yn}}{dt} - C_x^{'}\frac{dv_{xn}}{dt}\right] \tag{3.17}$$

$$i_{cn} = \frac{C_N^{'}}{C_b}\left[i_g - C_P\frac{dv_{pn}}{dt} - C_y^{'}\frac{dv_{yn}}{dt} - C_x^{'}\frac{dv_{xn}}{dt}\right] \tag{3.18}$$

$$v_{xn} = v_2 = v_{ds2} + L_2\frac{di_{d2}}{dt} \tag{3.19}$$

$$v_{yn} = v_4 - v_b = v_4 - L_b\frac{di_b}{dt} = v_{ds4} + L_4\frac{di_{d4}}{dt} - L_b\frac{d(i_n - i_{d4})}{dt} \tag{3.20}$$

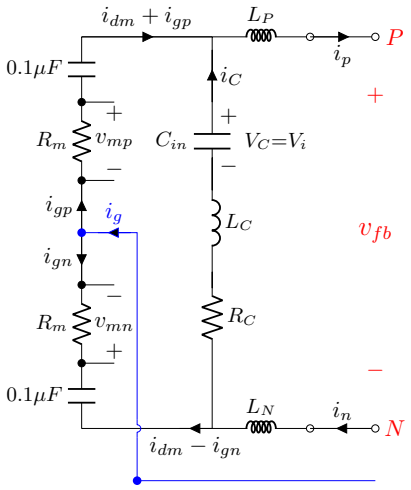


Figure 3.2 Simplified power module input-side circuit for analysis.

$$\begin{aligned} v_{pn} &= v_{fb} - v_a - v_b \\ &= v_{ds1} + v_{ds2} + (L_p - L_a)\frac{di_p}{dt} + (L_n - L_b)\frac{di_n}{dt} + (L_1 + L_a)\frac{di_{d1}}{dt} \\ &+ L_2\frac{di_{d2}}{dt} + L_b\frac{di_{d4}}{dt} \end{aligned} \tag{3.21}$$

The LISN on positive and negative input dc line will provide large impedance to the high-frequency ripple in line current and can be assumed to be open-circuit at its input for high-frequency analysis. Now, the input-side 5 µH inductor and 1 µF capacitor will appear to be connected in series and in parallel with measurement side series connected 0.1 µF capacitor and R_m. The measurement side impedance will be much lower than input side impedance at high-frequencies and LISN lumped-element circuit can be approximated as 0.1 µF capacitor in series with R_m. For a large input capacitor, it can be assumed that voltage across C_{in} is constant and equal to input dc source V_i. The simplified power module input-side circuit is shown in Figure 3.2. The positive and negative line currents, i_p and i_n can be written as Eqs. (3.22)-(3.23), where common-mode current $i_g = i_{gp} + i_{gn}$. Subtracting Eq. (3.22) and Eq. (3.23), we will model i_g by Eq. (3.24). Now, using KVL we can write Eq. (3.25) to model i_C.

$$i_p = i_C + (i_{dm} + i_{gp}) \tag{3.22}$$

$$i_n = i_C + (i_{dm} - i_{gn}) \tag{3.23}$$

$$i_g = i_p - i_n \tag{3.24}$$

$$\frac{di_C}{dt} = \frac{1}{L_C}\left(V_i - v_{fb} - L_p\frac{di_p}{dt} - L_n\frac{di_n}{dt}\right) \tag{3.25}$$

3.1.1 Common-Mode Equivalent Circuit

The common-mode equivalent circuit model for FBPM can be derived using Eqs. (3.15)-(3.18) and is shown in Figure 3.3, where noise sources v_{xn}, v_{yn} and v_{pn} can either be analytically modeled by Eqs. (3.19)-(3.21) or experimentally measured.

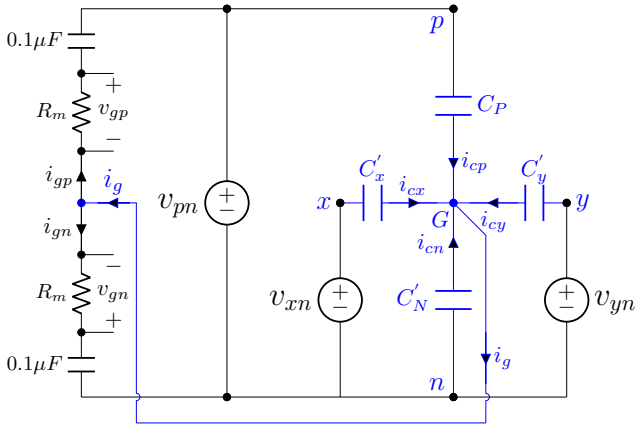


Figure 3.3 Common-Mode equivalent circuit model of a full-bridge power module.

3.2 Analytical Model of Single-Phase Inverter Circuit

The displacement current induced in parasitic capacitances of power module given by Eqs. (3.15)-(3.18) can be modeled using current and voltage response of power devices in the full-bridge circuit. In this section, a non-linear model for circuit voltage and current waveforms during mode S_{tr1} and S_1 is discussed. The nomenclature used to describe the SiC MOSFET device parameters are as follows: channel current $i_{ch\text{-}k}$, drain current $i_{d\text{-}k}$, gate current $i_{gr\text{-}k}$, drain-gate voltage $v_{dg\text{-}k}$, drain-source voltage $v_{ds\text{-}k}$, gate-source voltage $v_{gs\text{-}k}$ and gate driver voltage $v_{g\text{-}k}$, for $k \in \{1, 2, 3, 4\}$ corresponding to devices M_1, M_2, M_3 and M_4. The i_p and i_n are the positive and negative line currents and v_L is voltage across and i_L is current into load with parameters L_{load} and R_{load}. The device capacitance, C_{ds}, C_{dg} and C_{gs} are voltage dependent and are calculated from the capacitance model presented in Section 2.1.

For phase-shift modulation discussed in Section 2.2, analytical model of switching transients can be divided into two categories: $t_{dly} = 0$ and $t_{dly} > 0$. At $t < t_1$, device M_1 and M_4 are operating in on-state and M_2 and M_3 are operating in off-state. The initial conditions of the switching device state-variables are given by Eqs. (3.26)-(3.32).

$$i_{gr1} = 0,\ i_{gr2} = 0,\ i_{gr3} = 0,\ i_{gr4} = 0 \tag{3.26}$$

$$v_{gs1} = V_H,\ v_{gs2} = V_L,\ v_{gs3} = V_L,\ v_{gs4} = V_H \tag{3.27}$$

$$i_{d1} = i_{ch1} = i_L,\ i_{d2} = i_{ch2} = 0,\ i_{d3} = i_{ch3} = 0,\ i_{d4} = i_{ch4} = i_L \tag{3.28}$$

$$v_{ds1} = r_{ds1} i_L,\ v_{ds2} = v_{fb} - v_{ds1} - (L_p + L_1 + L_n)\frac{di_L}{dt} \tag{3.29}$$

$$v_{ds4} = r_{ds4} i_L,\ v_{ds3} = v_{fb} - v_{ds4} - (L_p + L_4 + L_n)\frac{di_L}{dt} \tag{3.30}$$

where,

$$\frac{di_L}{dt} = \frac{v_L}{L_{load}} - \frac{R_{load}}{L_{load}} i_L \tag{3.31}$$

$$v_L = v_{fb} - v_{ds1} - v_{ds4} - (L_p + L_1 + L_x + + L_y + L_4 + L_n)\frac{di_L}{dt} \tag{3.32}$$

3.2.1 Circuit Response Analysis for t_{dly}=0

When $t_{dly} = 0$, there is no time-delay for switching between devices in leg-A and leg-B, and both v_{g1} and v_{g4} are pulled down to low-state V_L at $t = t_1$. The non-linear model equations of circuit response during transient-state S_{tr1} are described as follows:

Mode-1 $(t_1 - t_x)$

This mode starts when v_{gs1} and v_{gs4} starts decreasing and the equivalent circuit is shown in Figure 3.4. It will take time T_f for gate-drive voltage to fall from V_H to V_L as given by Eq. (3.33). In this mode $dv_{gs\text{-}j}/dt \gg dv_{ds\text{-}j}/dt$ and model equations for $v_{gs\text{-}j}$ and $i_{gr\text{-}j}$ are given by Eqs. (3.34) and (3.35), for $j \in \{1, 4\}$.

$$v_{g\text{-}j} = \begin{cases} V_H + \frac{V_L - V_H}{T_f} t, & 0 < t < T_f \\ V_L, & t \geq T_f \end{cases} \tag{3.33}$$

$$v_{gs\text{-}j} = v_{g\text{-}j} - R_g^{'} i_{gr\text{-}j} - L_g \frac{di_{gr\text{-}j}}{dt} \tag{3.34}$$

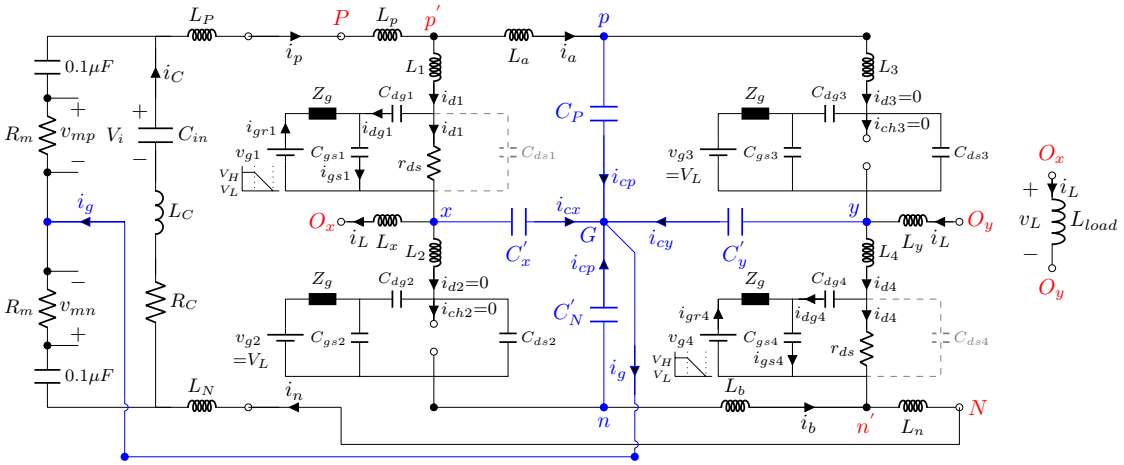


Figure 3.4 Full-bridge inverter equivalent circuit when device M1 and M4 are operating in linear region and M2 and M3 are in cut-off region at $t < t_1$.

$$i_{gr\text{-}j} = C_{gs\text{-}j}\frac{dv_{gs\text{-}j}}{dt} - C_{dg\text{-}j}\frac{dv_{dg\text{-}j}}{dt} \approx (C_{gs\text{-}j}+C_{dg\text{-}j})\frac{dv_{gs\text{-}j}}{dt} \tag{3.35}$$

where, $R_g^{'}$ and L_g are total loop resistance and parasitic inductance, respectively. The resistance $R_g^{'}$ is a combination of gate and source terminal resistance, and external gate resistance R_g. As $v_{gs\text{-}j}$ decreases, $r_{ds\text{-}j}$ also increases. Since the change in $r_{ds\text{-}j}$ is small, $v_{ds\text{-}j}$ is assumed to be constant in this mode. This mode ends when $v_{gs\text{-}j}$ is reduced to miller voltage v_{mil} [31].

Mode-2 $(t_x - t_y)$

In this mode, $i_{ch\text{-}j}$ starts decreasing, and the difference between $i_{ch\text{-}j}$ and $i_{d\text{-}j}$ charges $C_{ds\text{-}j}$ and $C_{dg\text{-}j}$. This causes $v_{ds\text{-}j}$ to start increasing. Since $v_{ds\text{-}j} < v_{gs\text{-}j}$, $v_{dg\text{-}j} < 0$ and $C_{dg\text{-}j}$ is equal to gate oxide capacitance [32]. The equivalent circuit for this mode is shown in Figure 3.5 and the model equations are given by Eqs. (3.36)-(3.38), for $j \in \{1, 4\}$.

$$i_{gr\text{-}j} \approx v_{gs\text{-}j}/R_g^{'} \tag{3.36}$$

$$\frac{dv_{gs\text{-}j}}{dt} = \frac{(C_{gs\text{-}j}+C_{dg\text{-}j})\, i_{gr\text{-}j} + C_{dg\text{-}j}\,(i_{d\text{-}j} - i_{ch\text{-}j})}{(C_{gs\text{-}j}+C_{dg\text{-}j})\,(C_{ds\text{-}j}+C_{dg\text{-}j}) - C_{dg\text{-}j}^2} \tag{3.37}$$

$$\frac{dv_{ds\text{-}j}}{dt} = \frac{C_{dg\text{-}j} i_{gr\text{-}j} + (C_{gs\text{-}j}+C_{dg\text{-}j})\,(i_{d\text{-}j} - i_{ch\text{-}j})}{(C_{gs\text{-}j}+C_{dg\text{-}j})\,(C_{ds\text{-}j}+C_{dg\text{-}j}) - C_{dg\text{-}j}^2} \tag{3.38}$$

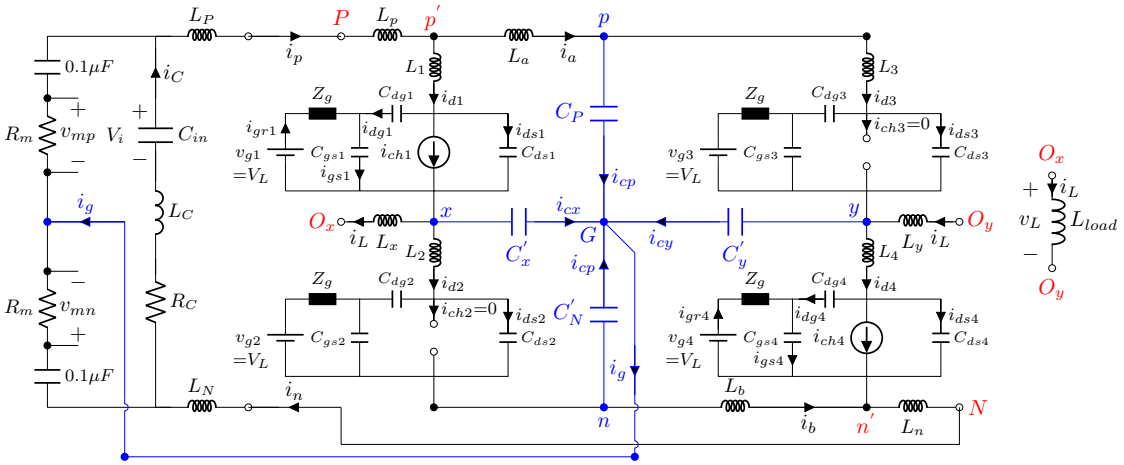


Figure 3.5 Full-bridge inverter equivalent circuit when M_1 -M_4 are turning off and M_2-M_3 are turning on.

Mode-3 $(t_y - t_2)$

At the start of this mode, i_{d1} starts decreasing. There is a delay of switching between M_1 and M_2 due to the dead-time t_d incorporated in the switching scheme. As v_{ds2} is positive and v_{g2} is held low, the body-diode of M_2 is reverse biased and the device is operating in blocking state. Since load current i_L cannot change instantaneously, the difference between i_L and i_{d1} is supplied by the discharge of C_{ds2} and C_{dg2}. The equivalent circuit is shown in Figure 3.5 and the model equations are given by Eqs. (3.39)-(3.44), where $L_{pn} = L_p + L_n$ and $L_v = L_{pn} + L_1 + L_2 + L_b$. The power module parasitic i_{cp}, i_{cx}, i_{cy} and i_{cn} can be calculated using Eqs. (3.15)-(3.18) and voltage across input terminals of power module, v_{fb} can be calculated using Eqs. (3.2)-(3.4).

$$i_{g41} \approx v_{gs1}/R'_g \tag{3.39}$$

$$\frac{dv_{gs1}}{dt} = \frac{i_{gr1}}{(C_{gs1}+C_{dg1})} + \frac{C_{dg1}}{(C_{gs1}+C_{dg1})}\frac{dv_{ds1}}{dt} \tag{3.40}$$

$$\frac{dv_{ds1}}{dt} = \frac{i_{d1} - i_{ch1}}{(C_{ds1}+C_{dg1})} \tag{3.41}$$

$$\frac{dv_{ds2}}{dt} = \frac{i_{d1} - i_L - i_{cx}}{(C_{ds2}+C_{dg2})} \tag{3.42}$$

$$\begin{aligned}\frac{di_{d1}}{dt} &= \frac{v_{fb}-v_{ds1}-v_{ds2}}{L_v} - \frac{L_{pn}}{L_v}\frac{di_{d3}}{dt} + \frac{(L_2+L_b)}{L_v}\frac{di_L}{dt} + \frac{(L_2+L_b+L_n)}{L_v}\frac{di_{cx}}{dt} \\ &+ \frac{L_n}{L_v}\frac{di_{cy}}{dt} + \frac{(L_b+L_n)}{L_v}\frac{di_{cn}}{dt} - \frac{L_p}{L_v}\frac{di_{cp}}{dt}\end{aligned} \tag{3.43}$$

$$i_{d2} = i_{d1} - i_L - i_{cx} \tag{3.44}$$

Similarly, i_{d4} will also start decreasing and the difference is load current will be supplied by the discharge of C_{ds3} and C_{dg3}. The model equations for M_3 and M_4 are given by Eqs. (3.45)-(3.50), where $L_{pn} = L_p + L_n$ and $L_w = L_{pn} + L_1 + L_2 + L_b$.

$$i_{gr4} \approx v_{gs4}/R_g^{'} \tag{3.45}$$

$$\frac{dv_{gs4}}{dt} = \frac{i_{gr4}}{(C_{gs4}+C_{dg4})} + \frac{C_{dg4}}{(C_{gs4}+C_{dg4})}\frac{dv_{ds4}}{dt} \tag{3.46}$$

$$\frac{dv_{ds4}}{dt} = \frac{i_{d4} - i_{ch4}}{(C_{ds4}+C_{dg4})} \tag{3.47}$$

$$\frac{dv_{ds3}}{dt} = \frac{i_{d4} - i_L - i_{cy}}{(C_{ds3}+C_{dg3})} \tag{3.48}$$

$$\begin{aligned}\frac{di_{d3}}{dt} &= \frac{v_{fb}-v_{ds3}-v_{ds4}}{L_w} - \frac{L_{pn}}{L_w}\frac{di_{d1}}{dt} - \frac{L_4}{L_w}\frac{di_L}{dt} + \frac{L_n}{L_w}\frac{di_{cx}}{dt} + \frac{(L_4+L_n)}{L_w}\frac{di_{cy}}{dt} \\ &+ \frac{L_n}{L_w}\frac{di_{cn}}{dt} - \frac{(L_p+L_a)}{L_w}\frac{di_{cp}}{dt}\end{aligned} \tag{3.49}$$

$$i_{d3} = i_{d4} - i_L - i_{cy} \tag{3.50}$$

3.2.2 Circuit Response Analysis for t_{dly}>0

When t_{dly}>0, there is a delay in switching between devices in leg-A and leg-B equal to t_{dly}. At $t = t_1$, v_{g1} is pulled down to low-state while v_{g4} remains pulled high. The circuit behaviour for Mode-1 and Mode-2 is similar to what we discussed in Section 3.2.1 for t_{dly}=0 and same non-linear model equations can be used to simulate circuit response. The non-linear model equations for Mode-3 during transient-state S_{tr1} are described as follows:

Mode-3 ($t_y - t_2$)

At the start of this mode, i_{d1} starts decreasing while M_3 and M_4 are operating in steady state with i_{d3}=0 and i_{d4}=i_L. There is a delay of switching between M_1 and M_2 due to the dead-time t_d incorporated in the switching scheme. As v_{ds2} is positive and v_{g2} is held low, the body-diode of M_2 is reverse biased and the device is operating in blocking state. Since load current i_L cannot change instantaneously, the difference is supplied

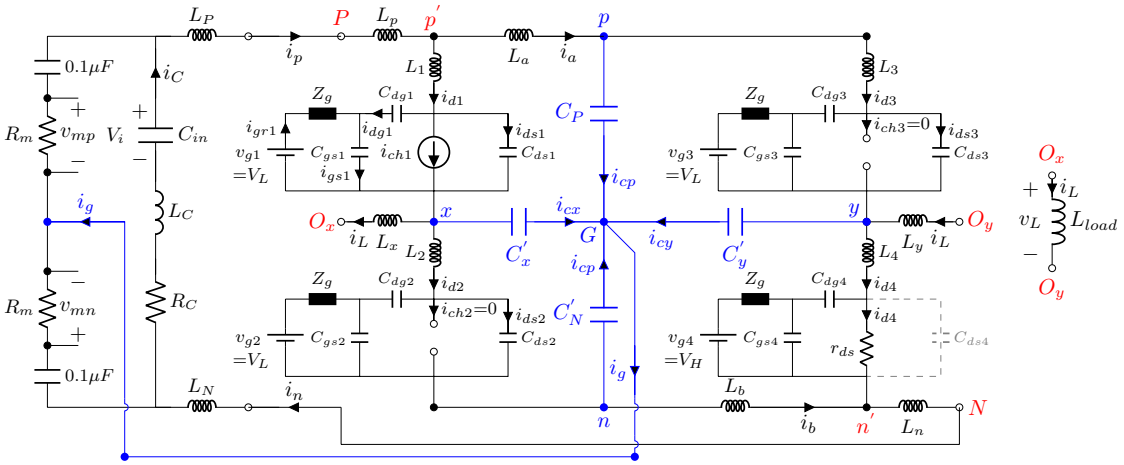


Figure 3.6 Full-bridge inverter equivalent circuit when M_1 is turning off and M_2 is turning on, and M_3 and M_4 are operating in off-state and on-state, respectively.

by the discharge of C_{ds2} and C_{dg2}. However, parasitic oscillations in line current due to M_1 and M_2 switching transients will cause voltage variation across M_3 and current will be induced in C_{ds3} and C_{dg3} proportional to dv/dt. The equivalent circuit for this mode is shown in Figure 3.6.The model equations for M_1 and M_2 are similar to what we discussed for t_{dly}=0, given by Eqs. (3.45)-(3.50). Additionally, model equations for M_3 and M_4 are given by (3.51)-(3.54).

$$\frac{dv_{ds3}}{dt} = \frac{i_{d3}}{(C_{ds3}+C_{dg3})} \tag{3.51}$$

$$v_{ds4} = (i_L + i_{d3} - i_{cy})r_{ds4} \tag{3.52}$$

$$\begin{aligned}\frac{di_{d3}}{dt} &= \frac{v_{fb}-v_{ds3}-v_{ds4}}{L_w} - \frac{L_{pn}}{L_w}\frac{di_{d1}}{dt} - \frac{L_4}{L_w}\frac{di_L}{dt} + \frac{L_n}{L_w}\frac{di_{cx}}{dt} + \frac{(L_4+L_n)}{L_w}\frac{di_{cy}}{dt} \\ &+ \frac{L_n}{L_w}\frac{di_{cn}}{dt} - \frac{(L_p+L_a)}{L_w}\frac{di_{cp}}{dt}\end{aligned} \tag{3.53}$$

$$i_{d4} = i_{d3} + i_L - i_{cx} \tag{3.54}$$

3.3 Summary

In this chapter, we first modeled circuit variables such as displacement current in parasitic capacitances, current in the input capacitor, differential-mode current, and common-mode (ground) current based on the drain-source voltage and drain current

of power devices in the full-bridge circuit. Next, we developed an analytical model for the power device state variables during one transient state, which can be generalized to other states in a switching cycle. The model was then extended to include the time delay introduced by phase-shift modulation. Because these state variables depend on parasitic capacitances, which vary with the bias voltage across device terminals, the resulting analytical model is non-linear.

Chapter 4

Parasitic Inductance Characterization

This chapter is based on the paper *'Parasitic Inductance Characterization of Full-Bridge Power Module Based on S-Parameter Measurements'* published in IEEJ Journal of Industry Applications.

The non-linear circuit response model presented in Chapter 3 relies on the parasitic inductances of the power module wiring. Previous studies have proposed several methods to characterize the parasitic inductances of half-bridge modules using S-parameter measurements. However, similar methods for full-bridge power modules (FBPM) have not been reported, likely due to the complexity of circuit analysis and S-parameter measurement. In this chapter, we first study the lumped-element circuit model of an FBPM as a 4-port network and parasitic inductances of the power module wiring are modeled in terms of network Z-parameters.Then, we will discuss the experimental measurement of FBPM S-parameters and the subsequent conversion from S-parameters to Z-parameters. Finally, we compare the parasitic inductances obtained from measurements with finite element method (FEM) simulation results for validation.

4.1 Full-Bridge Power Module

4.1.1 4-Port Network

The lumped element model of parasitics in full-bridge power module (FB-PM), modeled as a 4-port network, is shown in Figure 4.1a. The model consists of eight unknown wiring parasitic impedances modeled as inductances: Z_a, Z_b, Z_c, Z_d, Z_{ac}, Z_{ad}, Z_{bc} and Z_{bd}, and four SiC MOSFET impedance: Z_{M1}, Z_{M2}, Z_{M3} and Z_{M4}. The four ports of the network are labeled as P_1, P_2, P_3 and P_4. Further, the FB-PM lumped element model can be simplified by combining device impedance and wiring inductance, as shown in Figure 4.1b.

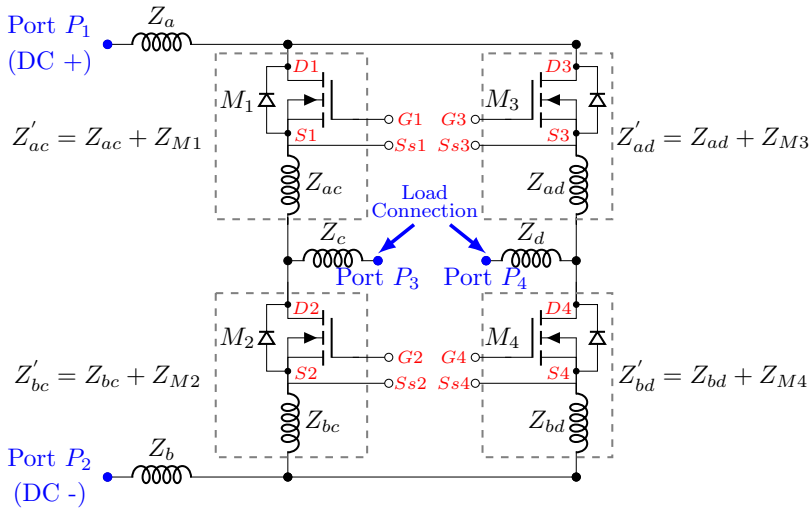
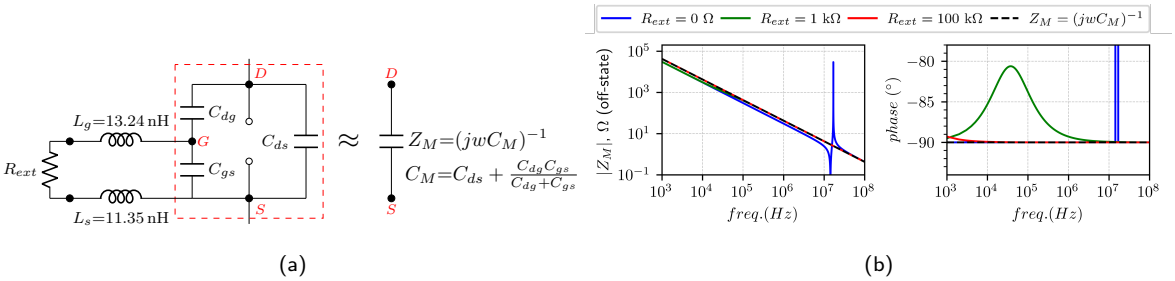


Figure 4.1 Full-Bridge Power Module (FB-PM) (a) lumped element model with wiring and device parasitics and (b) simplified lumped-element model.

There are 12 terminals in the FB-PM, as shown in Figure 4.1a. As per [44], the presence of floating terminals can lead to inaccuracies in S-parameter measurement. An

external impedance R_{ext} for termination is connected across the gate-source terminal of the device(s) in off-state. The SiC MOSFET equivalent circuit in off-state [85] with external gate-source loop inductances L_g and L_s is shown in Figure 4.2a. The impedance Z_M across Drain(D)-Source(S) terminals of power device in off-state is given by Eq. (4.1), where $Z_e = R_{ext}+jw(L_g+L_s)$ is approximated as $(1/Z_e) \approx 0$ for $R_{ext} \gg 1$. The equivalent circuit in off-state can then be modeled as a capacitance C_M. As we increase R_{ext} from $0\,\Omega$ to $100\,\mathrm{k}\Omega$, the impedance magnitude and phase gets close to the approximation (dotted line), as shown in Figure 4.2b. For $R_{ext} = 100\,\mathrm{k}\Omega$, Z_M magnitude and phase matches closely with the approximation.

$$\begin{aligned} Z_M &= \frac{jw\,(C_{dg}+C_{gs})+(1/Z_e)}{(jw)^2\,C_{ds}C_{dg}+jw\,(C_{ds}+C_{dg})\,(jwC_{gs}+(1/Z_e))} \\ &\approx \left(\frac{jwC_{dg}C_{gs}}{C_{dg}+C_{gs}}+jwC_{ds}\right)^{-1} = (jwC_M)^{-1} \end{aligned} \tag{4.1}$$



(a) (b)

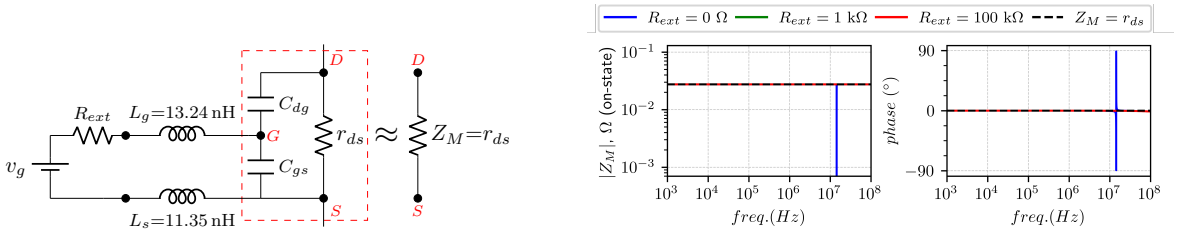
Figure 4.2 SiC MOSFET equivalent circuit (a) in off-state and (b) impedance Z_M magnitude and phase plot for different R_{ext}.

Similarly, SiC MOSFET equivalent circuit in on-state [85] is shown in Figure 4.3a and impedance Z_M across Drain(D)-Source(S) terminals of power device in on-state is given by Eq. (4.2), where $(1/Z_e) \approx 0$ for $R_{ext} \gg 1$. Approximation in Eq. (4.3) can be made for $f < 100\,\mathrm{MHz}$ and $Z_M \approx r_{ds}$ can be modeled as resistance. For R_{ext}=100 kΩ, Z_M magnitude and phase matches closely with the approximation (dotted line) as shown in Figure 4.3b. The values of C_{ds}, C_{dg}, C_{gs} and r_{ds} were obtained from power device data-sheet [86] and L_g and L_s were extracted from FEM simulation of power

module 3D model.

$$\begin{aligned} Z_M &= \frac{r_{ds}\left[jw\left(C_{dg}+C_{gs}\right)+\left(1/Z_e\right)\right]}{jw\left(C_{dg}+C_{gs}\right)+jwr_{ds}C_{dg}\left[jwC_{gs}+\left(1/Z_e\right)\right]+\left(1/Z_e\right)} \\ &\approx r_{ds}\left[1+r_{ds}\left(\frac{jwC_{dg}C_{gs}}{C_{dg}+C_{gs}}\right)\right]^{-1} \end{aligned} \tag{4.2}$$

$$\left|1+r_{ds}\left(\frac{jwC_{dg}C_{gs}}{C_{dg}+C_{gs}}\right)\right| = \sqrt[2]{1+0.75\cdot 10^{-21}w^2} \approx 1 \tag{4.3}$$



(a) (b)

Figure 4.3 SiC MOSFET equivalent circuit (a) in on-state and (b) impedance Z_M magnitude and phase plot for different R_{ext}.

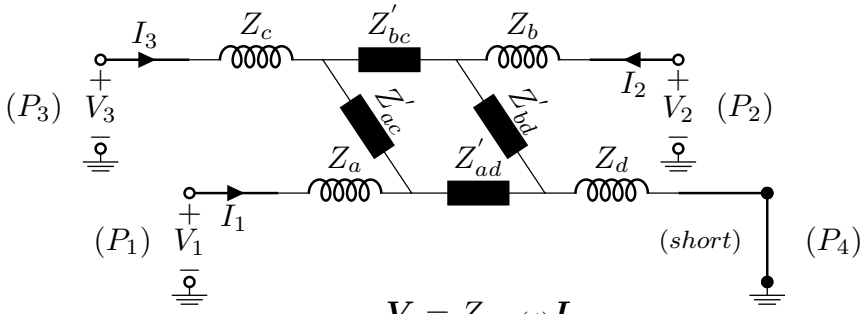
4.1.2 Network Analysis

In this section, a numerical model is derived to solve for FB-PM unknown impedances using network Z-parameters. In [44, 47, 48, 49], half-bridge power module (modeled as a 3-port network) is treated as a 2-port network with one port shorted to ground for network analysis, as shown in Figure 1.5. Since FB-PM is modeled as a 4-port network, for network analysis, it is treated as a 3-port network with one port shorted to ground. The Z-parameters of the 4-port network when port P_i is shorted to ground are defined by Eq. (4.4), where $m, n, i \in \{1, 2, 3, 4\}$ and $m, n \neq i$.

$$Z_{mn(i)} = \left.\frac{V_m}{I_n}\right|_{I_k=0, k\neq n, i} \tag{4.4}$$

The equivalent FB-PM network when port P_4 is shorted to ground is shown in Figure 4.4 and the Z-parameters $Z_{mn(4)}$ are given by Eqs. (4.5)-(4.10), where, $x = Z'_{ac} + Z'_{ad} + Z'_{bc} + Z'_{bd}$. Similarly, we will get 18 more equations from $Z_{mn(1)}$, $Z_{mn(2)}$ and $Z_{mn(3)}$, for a total of 24 equations.

$$Z_{11(4)} = Z_a + Z_d + \frac{Z'_{ad}(Z'_{ac} + Z'_{bc} + Z'_{bd})}{x} \tag{4.5}$$



$$\boldsymbol{V} = Z_{mn(4)}\boldsymbol{I}$$

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} Z_{11(4)} & Z_{12(4)} & Z_{13(4)} \\ Z_{21(4)} & Z_{22(4)} & Z_{23(4)} \\ Z_{31(4)} & Z_{32(4)} & Z_{33(4)} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix}$$

Figure 4.4 Equivalent lumped-element network and Z-matrix when port P_4 is shorted to ground.

$$Z_{22(4)} = Z_b + Z_d + \frac{Z'_{bd}(Z'_{ac} + Z'_{ad} + Z'_{bc})}{x} \tag{4.6}$$

$$Z_{33(4)} = Z_c + Z_d + \frac{(Z'_{ac} + Z'_{ad})(Z'_{bc} + Z_{bd})}{x} \tag{4.7}$$

$$Z_{21(4)} = Z_{12(4)} = Z_d + \frac{Z'_{ad}Z'_{bd}}{x} \tag{4.8}$$

$$Z_{31(4)} = Z_{13(4)} = Z_d + \frac{Z'_{ad}(Z'_{bc} + Z'_{bd})}{x} \tag{4.9}$$

$$Z_{32(4)} = Z_{23(4)} = Z_d + \frac{Z'_{bd}(Z'_{ac} + Z'_{ad})}{x} \tag{4.10}$$

When M_1 is in on-state and $Z_{M1} = r_{ds1}$ which is in $m\Omega$ range, the approximation in Eq. (4.11) can be made at high frequency when the inductive reactance of wiring parasitics will dominate over r_{ds1}. Similar approximations can be made for Z'_{bc}, Z'_{ad} and Z'_{bd} when M_2, M_3 and M_4 are in on-state.

$$Z'_{ac} = Z_{ac} + Z_{M1} = Z_{ac} + r_{ds1} \approx Z_{ac} \tag{4.11}$$

Using the Z-parameters measured when all devices were in on-state, $Z_{mn(i)on}$ for $i \in \{1, 2, 3, 4\}$, and simplifying the 24 equations, Z_a, Z_b, Z_d, Z_{ad}, Z_{bc} and Z_{bd} can be expressed in terms Z_c and Z_{ac} given by Eqs. (4.12)-(4.17).

$$Z_{ad} = \frac{Z_{12(3)on} - Z_{24(3)on}}{Z_{12(3)on} - Z_c} Z_{ac} = f\,(Z_c, Z_{ac}) \tag{4.12}$$

$$Z_{bc} = \frac{Z_c - Z_{24(3)on}}{Z_{14(3)on} - Z_c - Z_{ac}} Z_{ac} = f\,(Z_c, Z_{ac}) \tag{4.13}$$

Table 4.1 FB-PM circuit configurations and corresponding 3-port or 4-port S-Parameter (S-p) measurement for required Z-parameters (Z-p) to solve for unknown parasitic impedances

No.	Z-p	Device Operation				3-port S-p		4-port S-p
		M_1	M_2	M_3	M_4	Short	Measurement	Measurement
1.	$[Z_{mn(1)}]_{on}$	on	on	on	on	P_1	$P_2 - P_3 - P_4$	$P_1 - P_2 - P_3 - P_4$
2.	$[Z_{mn(2)}]_{on}$					P_2	$P_1 - P_3 - P_4$	
3.	$[Z_{mn(3)}]_{on}$					P_3	$P_1 - P_2 - P_4$	
4.	$[Z_{mn(4)}]_{on}$					P_4	$P_1 - P_2 - P_3$	
5.	$[Z_{12(3)}]_{M1}$	on	off	off	off	P_3	$P_1 - P_2 - P_4$	$P_1 - P_2 - P_3 - P_4$
6.	$[Z_{12(3)}]_{off}$	off	off	off	off	P_3	$P_1 - P_2 - P_4$	$P_1 - P_2 - P_3 - P_4$

$$Z_{bd} = \frac{\left(Z_{14(3)on} - Z_{12(3)on}\right)\left(Z_{24(3)on} - Z_c\right)}{\left(Z_{12(3)on} - Z_c\right)\left(-Z_{14(3)on} + Z_c + Z_{ac}\right)} Z_{ac} = f\left(Z_c, Z_{ac}\right) \tag{4.14}$$

$$Z_d = \frac{\left(Z_{12(3)on} - Z_{24(3)on}\right)\left(Z_{23(4)on} - Z_{12(4)on}\right)}{Z_{12(3)on} - Z_c} + Z_{12(4)on} = f\left(Z_c\right) \tag{4.15}$$

$$Z_b = \frac{\left(Z_{34(2)on} - Z_{14(2)on}\right)\left(Z_{24(1)on} - Z_{34(1)on}\right)}{Z_{34(1)on} - Z_a} + Z_{34(2)on} = f\left(Z_c, Z_{ac}\right) \tag{4.16}$$

$$Z_a = Z_{34(1)on} - \frac{Z_{ac}Z_{ad}}{Z_{ac} + Z_{ad} + Z_{bc} + Z_{bd}} = f\left(Z_c, Z_{ac}\right) \tag{4.17}$$

The unknown impedance Z_c and Z_{ac} are determined by solving Eq. (4.18) and Eq. (4.19). In Eq. (4.18), $Z_{12(3)M1}$ was measured when only device M_1 was in on-state. In Eq. (4.19), $Z_{12(3)off}$ was measured when all devices were in off-state. After substituting Z_{ad}, Z_{bc} and Z_{bd} from Eqs. (4.12)-(4.14), both Eq. (4.18) and Eq. (4.19) can be written in terms of Z_c and Z_{ac} and can be numerically solved.

$$Z_{12(3)M1} = \frac{Z'_{ac}Z'_{bc}}{Z_{ac}+Z'_{ad}+Z'_{bc}+Z'_{bd}} + Z_c = \frac{Z_{ac}(Z_{bc}+\frac{1}{jwC_M})}{Z_{ac}+Z_{ad}+Z_{bc}+Z_{bd}+\frac{3}{jwC_M}} + Z_c \tag{4.18}$$

$$Z_{12(3)off} = \frac{Z'_{ac}Z'_{bc}}{Z'_{ac}+Z'_{ad}+Z'_{bc}+Z'_{bd}} + Z_c = \frac{(Z_{ac}+\frac{1}{jwC_M})(Z_{bc}+\frac{1}{jwC_M})}{Z_{ac}+Z_{ad}+Z_{bc}+Z_{bd}+\frac{4}{jwC_M}} + Z_c \tag{4.19}$$

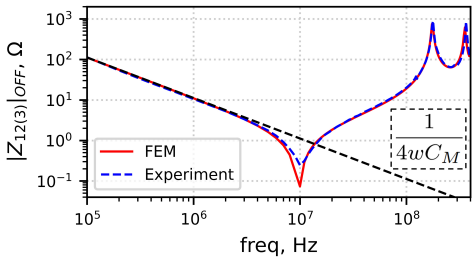


Figure 4.5 Measured $Z_{12(3)off}$ when all devices were in off-state.

To solve Eq. (4.18) and Eq. (4.19), the value of C_M is required. When M_1 is in off-state, the approximation for Z'_{ac} in Eq. (4.20) can be made at low frequency since L_{ac} and C_M are in nH/nF range. A similar approximation can be made for Z'_{bc}, Z'_{ad} and Z'_{bd} when M_2, M_3 and M_4 are in off-state. Since Z_c is also in nH range, Eq. (4.19) can be reduced to Eq. (4.21). The device capacitance $C_M = 3.613\,\text{nF}$ was calculated from measured $Z_{12(3)off} = 110.183\,\Omega$ at $f = 100\,\text{kHz}$, as shown in Figure 4.5.

$$Z'_{ac} = Z_{ac} + Z_{M1} = jwL_{ac} + \frac{1}{jwC_M} \approx \frac{1}{jwC_M} \tag{4.20}$$

$$Z_{12(3)off} \approx \frac{1}{4jwC_M} \tag{4.21}$$

4.2 S-parameter Measurement

To solve for the unknown FB-PM parasitic impedance using the model presented in the previous section, the Z-parameters for six different circuit configurations, as listed in Table 4.1, are required. The S-parameters of the FB-PM are measured and then converted to Z-parameters [87]. The S-parameter measurement experiment setup includes a test fixture with four SMA connectors, each representing one port. For 3-port S-parameter measurement, a short-circuit connector can be used to short the signal pin of SMA connector to ground. However, this will introduce error in measurement due to the inductance of short-circuit connector. Alternatively, we can experimentally measure the 4-port S-parameters and then mathematically convert them to the required 3-port S-parameters with one port shorted. This approach will also reduce the number of required S-parameter measurements from six to three, as listed in Table 4.1.

The FB-PM 4-port network and S-parameter matrix is shown in Figure 4.6a, where a_i and b_i are the incident wave and reflected wave respectively at port P_i and S_{mn}

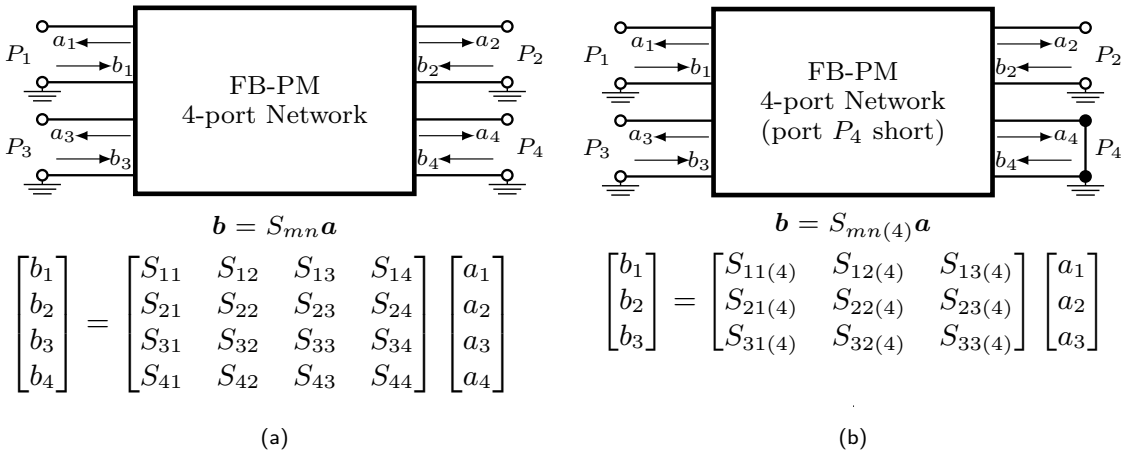


Figure 4.6 S-parameter matrix (a) for 4-Port network and (b) when port P_4 is shorted to ground.

denotes the measured network S-parameters. When port P_i is shorted to ground, $b_i = -a_i$ and the 3-port S-parameter matrix denoted by $S_{mn(i)}$ can be written in terms of S_{mn}. For P_4 shorted to ground, the 3-port network and S-parameter matrix $S_{mn(4)}$ is shown in Figure 4.6b. The relationship between S_{mn} and $S_{mn(4)}$ is given by Eq. (4.22), where $S_a = (1 + S_{44})$. Similarly, the relationships between the measured S_{mn} and the required $S_{mn(1)}$, $S_{mn(2)}$ and $S_{mn(3)}$ can be defined.

$$\begin{bmatrix} S_{11(4)} & S_{12(4)} & S_{13(4)} \\ S_{21(4)} & S_{22(4)} & S_{23(4)} \\ S_{31(4)} & S_{32(4)} & S_{33(4)} \end{bmatrix} = \begin{bmatrix} \frac{S_{11}S_a - S_{14}S_{41}}{S_a} & \frac{S_{12}S_a - S_{14}S_{42}}{S_a} & \frac{S_{13}S_a - S_{14}S_{43}}{S_a} \\ \frac{S_{21}S_a - S_{24}S_{41}}{S_a} & \frac{S_{22}S_a - S_{24}S_{42}}{S_a} & \frac{S_{23}S_a - S_{24}S_{43}}{S_a} \\ \frac{S_{31}S_a - S_{34}S_{41}}{S_a} & \frac{S_{32}S_a - S_{34}S_{42}}{S_a} & \frac{S_{33}S_a - S_{34}S_{43}}{S_a} \end{bmatrix} \tag{4.22}$$

The 4-port S-parameter measurement experiment setup is shown in Figure 4.7. An R&S ZNBT vector network analyzer (VNA) was used to measure the 4-port S-parameters of the 4-port FB-PM network for the following circuit configurations:

1. All devices are operating in on-state. Apply v_g with 18 V batteries across the gate-source terminals of M_1, M_2, M_3 and M_4.

2. All devices are operating in off-state. Connect R_{ext} across the gate-source terminals of M_1, M_2, M_3 and M_4.

3. Device M_1 is operating in on-state and M_2, M_3 and M_4 are operating in off-state. Apply v_g with 18 V battery across the gate-source terminal of M_1 and connect R_{ext} across the gate-source terminals of M_2, M_3 and M_4.

The voltage v_g across gate-source terminals of device is supplied using two NiMH 9V batteries connected in series. The batteries are floating with small parasitic capacitance to ground. The circuit traces in power module are isolated from any external signal path that could compromise the S-parameter measurements.

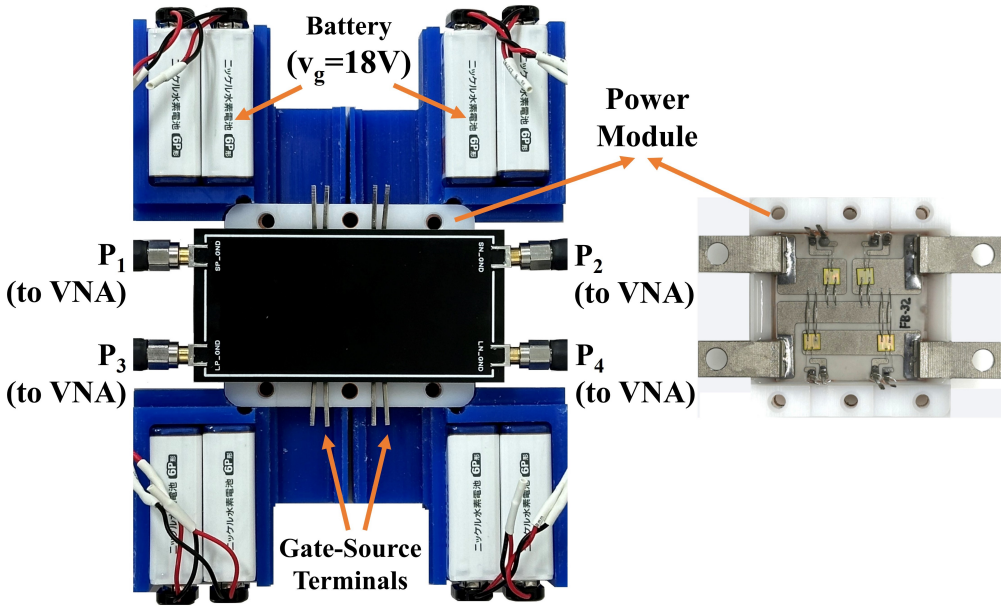


Figure 4.7 SiC MOSFET Full-Bridge Power Module 4-Port S-parameter measurement setup.

4.3 Power Module Wiring Parasitic Inductance Calculation

4.3.1 4-Port Test Fixture Parasitics

The FB-PM experimentally measured data includes fixture parasitics. The fixture 3D model is shown in Figure 4.8a, and it consists of SMA connectors, copper pads for power module connection and a reference plane. The impedance of the test fixture cannot be experimentally measured because of geometric limitations. The S-parameters of test

fixture were obtained from FEM simulation between ports P_{m1}, P_{m2}, P_{m3} and P_{m4} as shown in Figure 4.8a. To remove test fixture parasitics, S-parameter de-embedding was performed on experimentally measured data using a built-in function in PathWave ADS software.

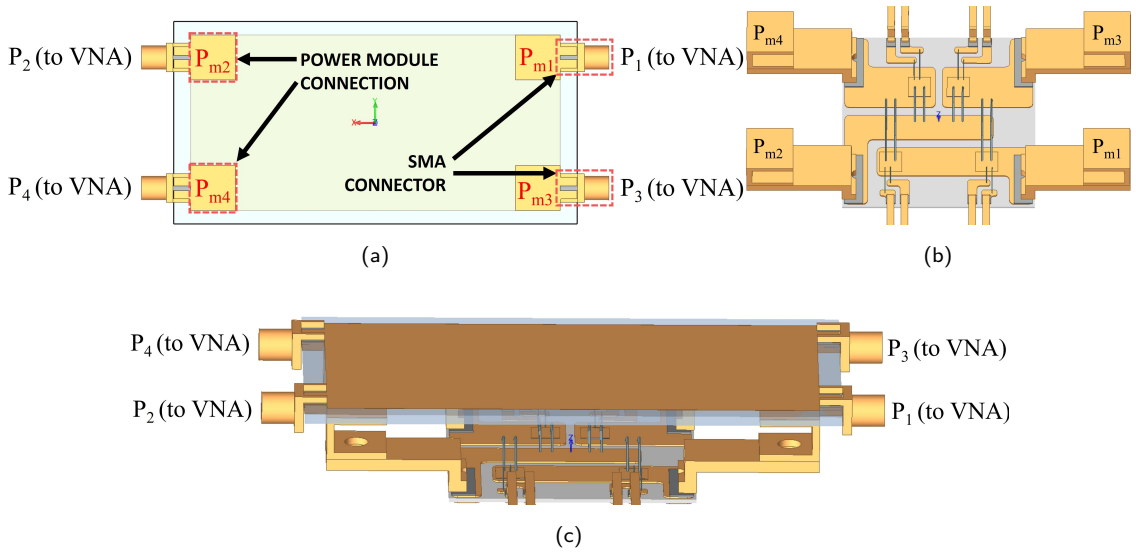


Figure 4.8 FEM simulation model of (a) 4-port test fixture, (b) full-bridge power module (FB-PM) and (c) S-Parameter experiment measurement setup.

4.3.2 Parasitic Inductance Calculation

The experimentally measured 4-port S-parameters after de-embedding are transformed to 3-port S-parameters for the circuit configurations listed in Table 4.1. Then, the 3-port S-parameters are converted to 3-port Z-parameters to solve for FB-PM wiring parasitics.

For parasitic inductance extraction, the unknown impedances are assumed to be purely inductive. First Eq. (4.18) and Eq. (4.19) are solved for Z_c and Z_{ac} using the measured Z-parameters. After numerically solving the equations, we get four distinct solutions. Of the four solutions, two for which Z_{ac} was negative are discarded. Then, the remaining two solutions are used to solve Eqs. (4.12)-(4.17). The solution which gives positive values of parasitic inductances is then selected. The FB-PM parasitic inductances calculated at f=10 MHz (Experiment.) and values obtained from FEM simulation (FEM.) are compared in Table 4.2. The largest difference between

the experimentally calculated and simulated values is 0.965 nH (4.585 %) for L_{ad}, and the smallest is 0.009 nH (0.058 %) for L_b. The difference between the experimentally calculated and simulated values can be attributed to the discrepancy between the experimental prototype of the power module and test fixture, and its 3D model used for simulation.

Table 4.2 FB-PM wiring parasitic inductance comparison.

Inductance	Experiment	FEM	|Difference|	
L_a	11.398 nH	11.426 nH	0.028 nH	0.245 %
L_b	15.461 nH	15.452 nH	0.009 nH	0.058 %
L_c	12.466 nH	12.287 nH	0.179 nH	1.436 %
L_d	12.103 nH	12.287 nH	0.184 nH	1.520 %
L_{ac}	9.391 nH	9.675 nH	0.284 nH	3.024 %
L_{ad}	21.045 nH	20.08 nH	0.965 nH	4.585 %
L_{bc}	11.328 nH	11.751 nH	0.423 nH	3.734 %
L_{bd}	5.630 nH	5.409 nH	0.221 nH	3.925 %

The FEM simulation of the FB-PM was performed both without a test fixture, as shown in Figure 4.8b, and with a test fixture, as shown in Figure 4.8c. In Figure 4.9(a), the experimentally measured (FB-PM Experiment) and simulated (FB-PM FEM) Z-parameters with test fixture are compared for port P_4 shorted to ground in the frequency range of 1 MHz−500 MHz. The large deviation between the measured and simulated results at frequency less than 5 MHz stems from the limitations of the measurement instrument. In Figure 4.9(b), the experimentally measured Z-parameters after de-embedding and the simulated Z-parameters without the test fixture are compared. The Z-parameters of the lumped-element model (FB-PM LUM), computed from equations (4.5)-(4.10) using the calculated parasitic inductance values given in Table 4.2, match closely with the measured and simulated results, as shown in Figure 4.9(b).

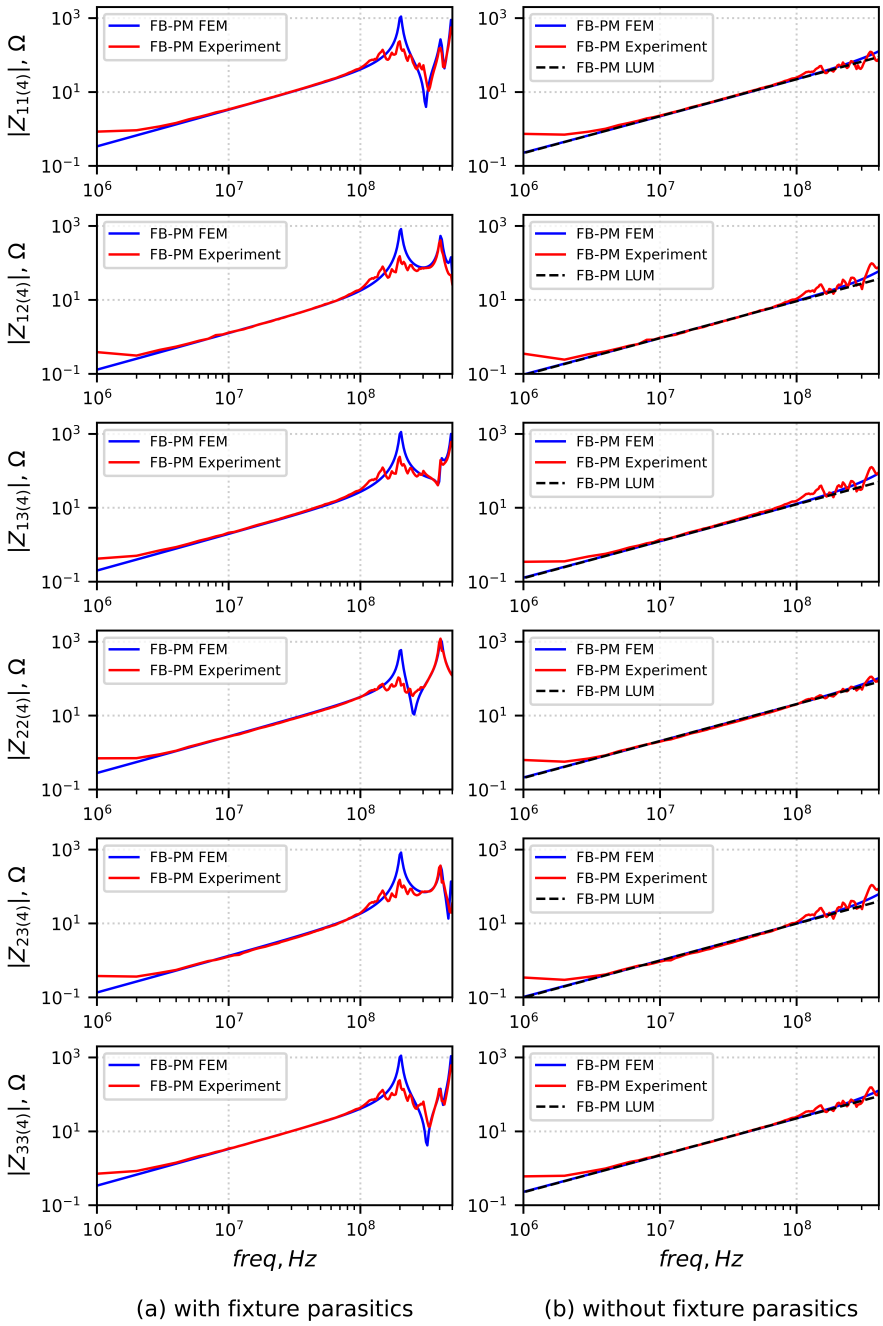


Figure 4.9 FB-PM Z-parameter comparison for port P_4 short.

4.4 Summary

In this chapter, we presented a procedure for calculating the wiring parasitic inductances of a full-bridge power module (FBPM). The FBPM was modeled as a 4-port lumped-element network with eight unknown impedances. To characterize these impedances, we developed a numerical model based on network Z-parameters. The 4-

port S-parameters of the FBPM were measured using a 4-port vector network analyzer and converted to Z-parameters. These Z-parameters were used to solve for the unknown network impedances. Additionally, the parasitic inductance of the power module were obtained through finite element method simulation. The simulated inductance values show good agreement with the calculated values. The simulated inductance values show good agreement with the calculated results. The largest difference was 4.585 %, the smallest was 0.058 %, and the average was 2.316 %.

Chapter 5

Parasitic Capacitance Characterization

This chapter is based on the paper *Non-destructive Characterization of Parasitic Capacitances in Full-Bridge Power Module'* published in IEEJ Journal of Industry Applications.

The common-mode conducted emissions are caused by displacement current flowing through the parasitic capacitance between the switching nodes and ground of the power module. Several techniques have been proposed in the literature to characterize parasitic capacitances in power modules. These include finite element analysis, which requires detailed geometric and material data that are generally not available, and direct impedance measurement, which necessitates destructive disassembly of the module. In this chapter, we propose a non-destructive method to measure parasitic capacitances between the conductive traces on top-layer and baseplate of a FBPM. The parasitic capacitances are characterized in terms of voltages between power circuit switching nodes modeled as noise sources in the common-mode equivalent circuit and voltages measured at LISN output ports on positive and negative input dc line.

5.1 Common-Mode Equivalent Circut analysis

The common-mode (CM) equivalent circuit introduced in Section 3.1.1 is based on a simplified LISN lumped-element model. This model assumes that a $50\,\Omega$ load is con-

nected across the LISN measurement resistance, simulating the input of a frequency spectrum measurement device, typically a spectrum analyzer or an EMI receiver. However, the method presented in this chapter relies on direct voltage measurement at the LISN port using a differential probe with input impedance of $\sim 10\,\mathrm{M\Omega}$. Therefore, we will use a detailed lumped-element model of the LISN in the CM equivalent circuit to characterize the parasitic capacitances of the full-bridge power module (FBPM) under analysis in this study., as shown in Figure 5.1.

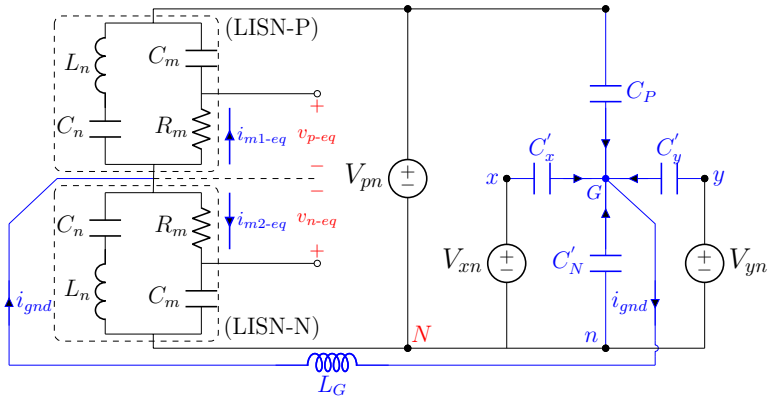


Figure 5.1 Simplified CM equivalent circuit model of CE measurement circuit.

5.1.1 Circut analysis for V_{xn}

The equivalent circuit for V_{xn} is shown in Figure 5.2, where $C_i = C_{bp} - C'_x$ and C_{bp} is the total parasitic capacitance of FBPM given by Eq. (5.1). The V_{xn} induces current $(i_{gnd})_x$ in the circuit and current $(i_{m1-eq})_x$ and $(i_{m2-eq})_x$ is flowing through LISN(s) measurement resistance R_m. KVL for $(i_{gnd})_x$ loop is differentiated as Eq. (5.2).

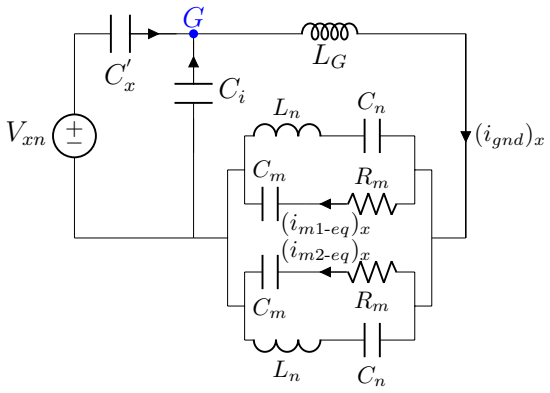


Figure 5.2 Equivalent circuit for V_{xn}.

$$C_{bp} = \sum_{i=1}^{4} (C_{Gi} + C_{Si}) + C_P + C_x + C_y + C_N \tag{5.1}$$

$$\begin{aligned} \frac{C_x'}{C_{bp}} \frac{dV_{xn}}{dt} &= \frac{R_m}{2} \frac{d\left(i_{m1\text{-}eq}\right)_x + \left(i_{m2\text{-}eq}\right)_x}{dt} + L_G \frac{d^2\left(i_{gnd}\right)_x}{dt^2} \\ &+ \frac{\left(i_{m1\text{-}eq}\right)_x + \left(i_{m2\text{-}eq}\right)_x}{2C_m} + \frac{\left(i_{gnd}\right)_x}{C_{bp}} \end{aligned} \tag{5.2}$$

5.1.2 Circut analysis for V_{yn}

The equivalent circuit for V_{yn} is shown in Figure 5.3, where $C_j = C_{bp} - C_y'$. The V_{yn} induces current $(i_{gnd})_y$ in the circuit and $(i_{m1-eq})_y$ and $(i_{m2-eq})_y$ is flowing through R_m. KVL for $(i_{gnd})_y$ loop is differentiated as Eq. (5.3).

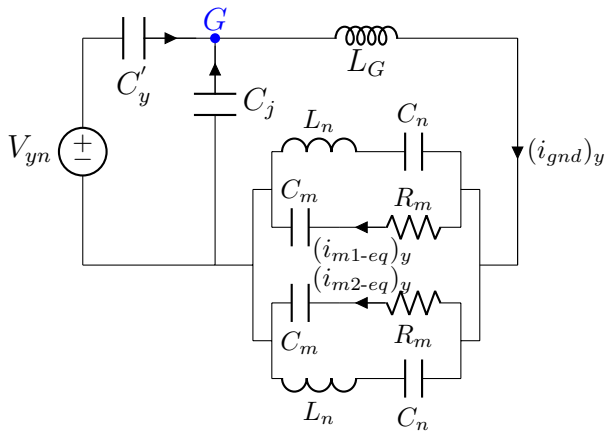


Figure 5.3 Equivalent circuit for V_{yn}.

$$\begin{aligned} \frac{C_y'}{C_{bp}} \frac{dV_{yn}}{dt} &= \frac{R_m}{2} \frac{d\left(i_{m1\text{-}eq}\right)_y + \left(i_{m2\text{-}eq}\right)_y}{dt} + L_G \frac{d^2\left(i_{gnd}\right)_y}{dt^2} \\ &+ \frac{\left(i_{m1\text{-}eq}\right)_y + \left(i_{m2\text{-}eq}\right)_y}{2C_m} + \frac{\left(i_{gnd}\right)_y}{C_{bp}} \end{aligned} \tag{5.3}$$

5.1.3 Circut analysis for V_{pn}

The equivalent circuit for V_{pn} is shown in Figure 5.4, where $C_k = C_{bp} - C_P$. The V_{pn} induces current $(i_{gnd})_z$ in the circuit and $(i_{m1-eq})_z$ and $(i_{m2-eq})_z$ is flowing through R_m. KVL for $(i_{gnd})_z$ loop is differentiated as Eq. (5.4).

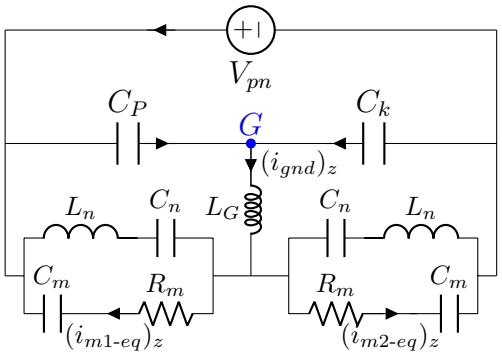


Figure 5.4 Equivalent circuit for V_{pn}.

$$\left[\frac{C_P}{C_{bp}}-\frac{1}{2}\right]\frac{dV_{pn}}{dt} = \frac{R_m}{2}\frac{d\left(i_{m1\text{-}eq}\right)_z+\left(i_{m2\text{-}eq}\right)_z}{dt}+\frac{\left(i_{m1\text{-}eq}\right)_z+\left(i_{m2\text{-}eq}\right)_z}{2C_m}+\frac{\left(i_{gnd}\right)_z}{C_{bp}} + L_G\frac{d^2\left(i_{gnd}\right)_z}{dt^2} \tag{5.4}$$

The total current flowing through the ground plane in the circuit is summation of current induced by individual voltage sources V_{xn}, V_{yn} and V_{pn}, and is given by Eq. (5.5). Similarly, current flowing through LISN(s) measurement resistance are given by Eqs. (5.6)-(5.7).

$$i_{gnd} = \left(i_{gnd}\right)_x + \left(i_{gnd}\right)_y + \left(i_{gnd}\right)_z \tag{5.5}$$

$$i_{m1\text{-}eq} = \left(i_{m1\text{-}eq}\right)_x + \left(i_{m1\text{-}eq}\right)_y + \left(i_{m1\text{-}eq}\right)_z \tag{5.6}$$

$$i_{m2\text{-}eq} = \left(i_{m2\text{-}eq}\right)_x + \left(i_{m2\text{-}eq}\right)_y + \left(i_{m2\text{-}eq}\right)_z \tag{5.7}$$

The $i_{m1\text{-}eq}$ and $i_{m2\text{-}eq}$ are the current flowing through measurement resistance R_m of LISN(s) in CM equivalent circuit (Figure 5.1). However in experiment circuit, it is measured as combination of line current (i_{dm}) and ground plane current (i_{m1-eq} and i_{m2-eq}) given by Eqs. (5.8)-(5.9), as shown in Figure 5.5. Adding Eq. (5.8) and Eq. (5.9), we can write $i_{m1\text{-}eq} + i_{m2\text{-}eq}$ in terms of voltages v_p and v_n measured at LISN output ports and is given by Eq. (5.10). The ground plane current i_{gnd} can be modeled in terms of v_p and v_n by Eq. (5.11), where circuit elements R_m, C_m, L_n and C_n are known LISN parameters.

$$v_p = -\left(i_{dm} + i_{m1\text{-}eq}\right)R_m \tag{5.8}$$

$$v_n = \left(i_{dm} - i_{m2\text{-}eq}\right)R_m \tag{5.9}$$

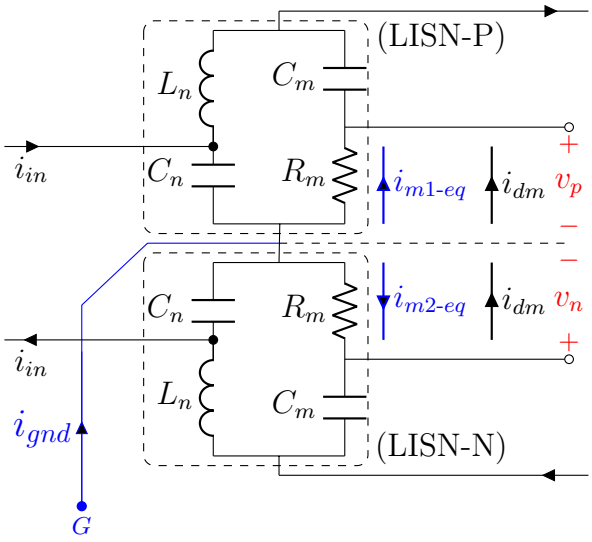


Figure 5.5 Current through LISN during experiment.

$$i_{m1\text{-}eq} + i_{m2\text{-}eq} = -\left(v_p + v_n\right)/R_m \tag{5.10}$$

$$\begin{aligned} i_{gnd} &= -\frac{L_n C_n}{R_m}\frac{d^2\left(v_p+v_n\right)}{dt^2} - C_n\frac{d\left(v_p+v_n\right)}{dt} \\ &- \frac{C_n}{R_m}\left[\frac{1}{C_m}+\frac{1}{C_n}\right]\left(v_p+v_n\right) - L_n C_n\frac{d^2 i_{gnd}}{dt^2} \end{aligned} \tag{5.11}$$

Using Eqs. (5.2)-(5.10), we can derive the relationship between parasitic capacitance, branch voltages: dV_{xn}/dt, dV_{yn}/dt and dV_{pn}/dt and LISN output voltages: dv_p/dt and dv_n/dt, given by Eq. (5.12).

$$\begin{aligned} &\frac{C_x'}{C_{bp}}\frac{dV_{xn}}{dt} + \frac{C_y'}{C_{bp}}\frac{dV_{yn}}{dt} + \left[\frac{C_P}{C_{bp}} - \frac{1}{2}\right]\frac{dV_{pn}}{dt} = \\ &L_G\frac{d^2 i_{gnd}}{dt^2} + \frac{i_{gnd}}{C_{bp}} - \frac{1}{2}\frac{d\left(v_p+v_n\right)}{dt} - \frac{\left(v_p+v_n\right)}{2R_m C_m} \end{aligned} \tag{5.12}$$

5.2 Power Module to Baseplate Parasitic Capacitance Calculation

5.2.1 Step 1: C_{bp} measurement

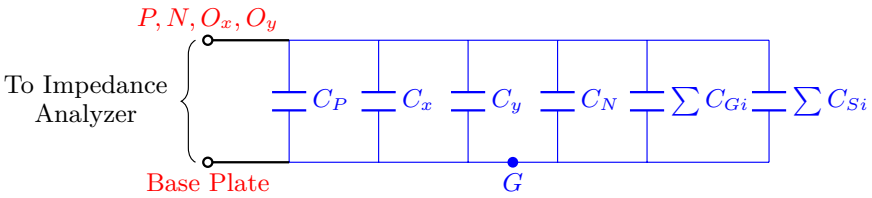
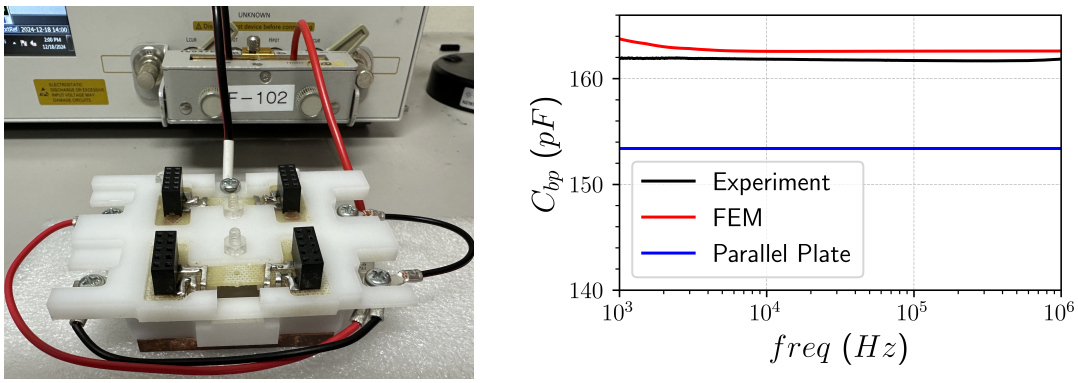


Figure 5.6 Low-frequency equivalent circuit model of FBPM.

The capacitance C_{bp} in Eqs. (5.2)-(5.4) is the total parasitic capacitance of power module. When measuring impedance between power terminals and baseplate of FBPM, the parasitic inductance exists in series with parasitic capacitance. At low-frequency ($f < 1\,\text{MHz}$), impedance of parasitic inductance is much lower than parasitic capacitance and can be neglected. If we short-circuit all the power terminals P, N, O_x and O_y, gate terminal G_i and kelvin-source terminal S_{si} for $i \in \{1, 2, 3, 4\}$, the lumped element model of FBPM shown in Figure 2.9 can be approximated as Figure 5.6 at low-frequency. The total parasitic capacitance of power module can then be measured using an impedance analyzer between power terminals and baseplate. The parasitic capacitance between terminal P and baseplate was measured using Keysight E4990A impedance analyzer and is shown in Figure 5.7a. For comparison, C_{bp} was also obtained from FEM simulation of detailed 3D CAE model of studied FBPM shown in Figure 5.8a and compared with measured result, as shown in Figure 5.7b. The FEM simulation was performed using EMPro software with the Target Mesh Size set to 'Automatic' and Delta Error set to 0.0009 for 3 consecutive passes. Here, Delta Error is the maximum allowable change in vector difference magnitude of all S-parameters, as defined in Keysight EMPro software documentation. A smaller Delta Error leads to more accurate results but requires a finer mesh to achieve convergence, which in turn increases the memory (RAM) usage, computation cost, and time. A Delta Error value of 0.0009 was selected to achieve the maximum simulation accuracy within

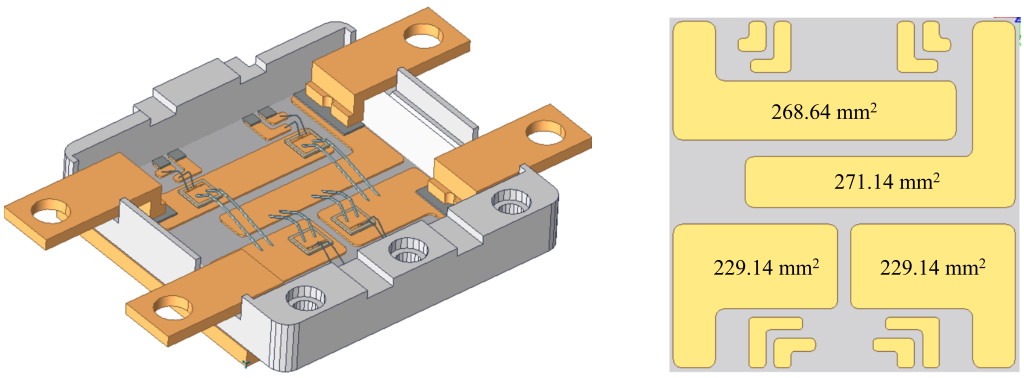
the computational limitations of the available hardware. At $f = 10\,\text{kHz}$, measured $C_{bp} = 161.8\,\text{pF}$ shows good agreement with simulated $C_{bp} = 162.5\,\text{pF}$.



(a) (b)

Figure 5.7 (a) FBPM parasitic capacitance measurement between terminal P and baseplate using Keysight E4990A and (b) comparison between FEM and Measured results.

The parallel plate capacitance formula $C = \varepsilon_\circ \varepsilon A/d$ can be used to calculate capacitance between trace on the top and bottom layer of power module DBC substrate, where A is the area of trace, d is thickness and ε is dielectric constant of insulation material and $\varepsilon_\circ$ is permittivity of free space. However this does not takes into account the fringing effect. The calculated parallel-plate capacitance C_{bp}= 153.4 pF is 5.22 % less than measured C_{bp} and is comparable to error reported in literature.



(a) (b)

Figure 5.8 Power Module (a) 3D CAE model and (b) DBC substrate.

5.2.2 Step 2: V_{xn}, V_{yn}, V_{pn}, v_p and v_n measurement and i_{gnd} calculation

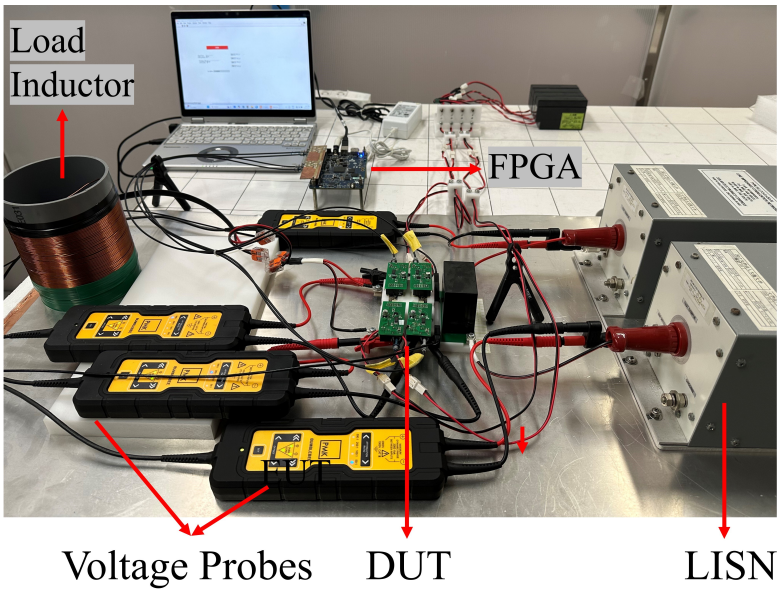


Figure 5.9 CE measurement experiment setup.

The CE measurement setup, which consist of two LISNs and a ground plane is shown in Figure 5.9 and experiment was conducted in a 'Faraday cage' test chamber (room) with temperature maintained at $\approx 20°C$. The test parameters are described in Table 6.1. A 1 GHz, 20 GSa/s Keysight DSOS104A Oscilloscope with 400 MHz PMK BumbleBee differential probe was used for measurement. The measured V_{xn}, V_{yn}, V_{pn}, and LISN output voltages v_p and v_n for $ps_d = 45°$ are shown in Figure 5.10. Since five voltages are required and we used a 4-channel oscilloscope, two experiment measurements were recorded: (V_{xn}, V_{yn}, v_p, v_n) and (V_{xn}, V_{pn}) with rising edge of V_{xn} as reference.

5.2.3 Step 3: Parasitic Capacitance Calculation

During transient state S_{tr1} (as discussed in Section 2.2), derivative of experimentally measured voltages with respect to time is shown in Figure 5.11a. The Eq. (5.12) consists of four unknown values: C_x', C_y', C_P and L_G and will be reduced to two unknowns C_x' and L_G for $dV_{yn}/dt = dV_{pn}/dt = 0$. At $t = t_w$ and $t = t_x$, $dV_{yn}/dt \approx dV_{pn}/dt \approx 0$ and we will get two equations from Eq. (5.12) with two unknowns C_x' and L_G for which we

Table 5.1 Experiment Parameters

Parameter	Value/Part No.	Remarks
V_{dc}	600 V	Input DC Voltage
L_{out}	326 ⁻H	Load Inductor
f_s, T_s	50 kHz, 20 ⁻s	Switching Frequency, Time-Period
t_{dly}	2.5 ⁻s	phase-shift time
SiC MOSFET	ROHM S4103	

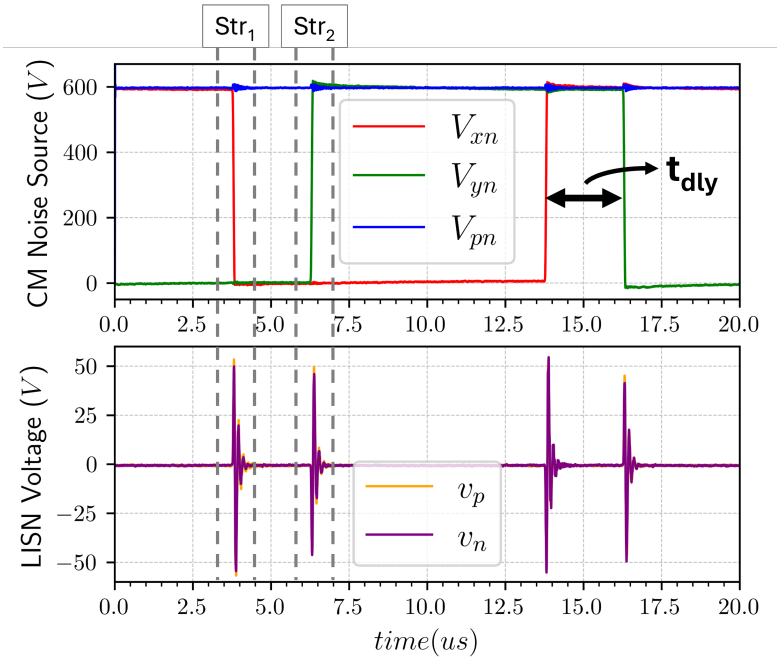
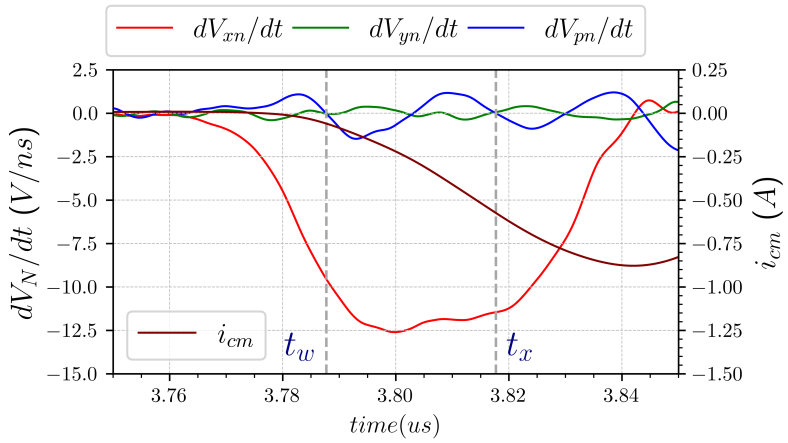


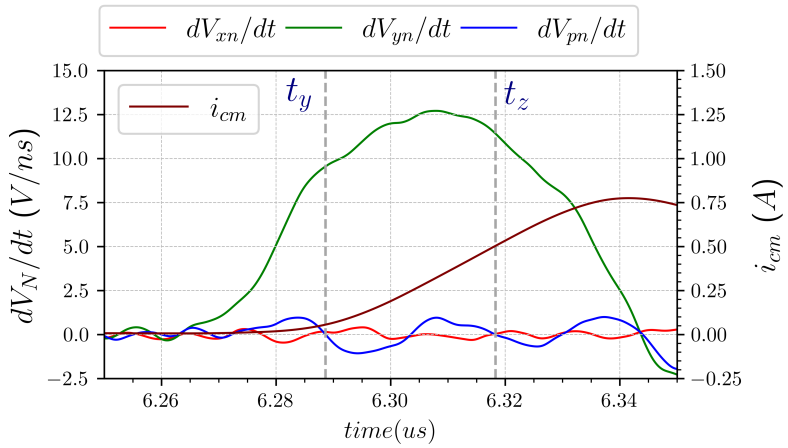
Figure 5.10 Measured circuit voltages and LISN ouput voltages over one switching cycle T_s=20 ⁻s for t_{dly}=2.5 ⁻s.

can solve for. The derivative of experimentally measured voltages with respect to time during transient state S_{tr2} is shown in Figure 5.11b. At $t = t_y$ and $t = t_z$, $dV_{xn}/dt \approx dV_{pn}/dt \approx 0$ and we will get two equations from Eq. (5.12) with two unknowns C_y' and L_G for which we can solve for. Now using the estimated values of C_x', C_y' and L_G, C_P can be calculated from Eq. (5.12) and $C_N' = C_{bp} - C_P - C_x' - C_y'$.

The experimentally estimated parasitic capacitances and ground plane parasitic are given in Table 5.2. The difference between estimated values of parasitic capacitances using the presented model and parallel-plate analytical formula is between +2.5 % and



(a)



(b)

Figure 5.11 Derivative of measured circuit voltages with respect to time during transient state (a) S_{tr1} and (b) S_{tr2}.

+8.9 %. However, when compared with values obtained from FEM simulation of detailed 3D CAE model of FBPM, this difference is reduced to between −2.1 % and +2.6 %. The comparison between estimated values, FEM simulation values and those obtained from parallel-plate capacitance analytical formula is shown in Figure 5.12. Although identified value of parasitic capacitances matches closely with the simulated values, difference could arise due to inaccuracy in time-domain experiment measurements.

Table 5.2 Experimentally estimated power module parasitic capacitance.

Experiment estimation	C'_x	C'_y	L_G	C_P	C'_N
S_{tr1}	36.3 pF	-	528 nH	39.3 pF	49.9 pF
S_{tr2}	-	36.4 pF	525 nH		

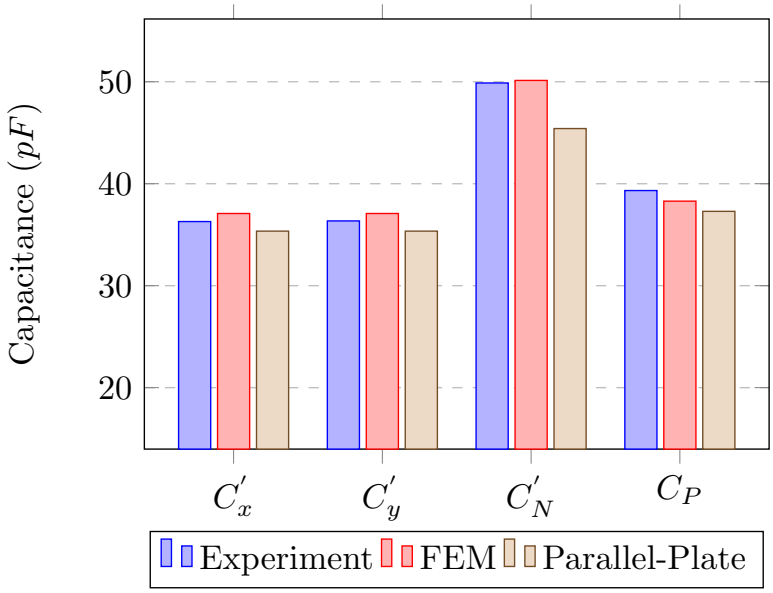


Figure 5.12 Experimentally estimated power module parasitic capacitance compared with values obtained from FEM simulation and parallel-plate capacitance formula.

5.3 Summary

In this chapter, we presented a non-destructive technique for identifying parasitic capacitances in a full-bridge power module (FBPM). Using the common-mode equivalent circuit model introduced in Chapter 3, we first characterized these parasitic capacitances in terms of noise source voltages and LISN output voltages. We then measured the noise-source voltages across the power-module terminals, along with the voltages at the LISN outputs, and calculated the parasitic capacitances. The calculated values matched closely with values obtained from the finite element method simulation of the detailed 3D model of power module.

Chapter 6

Differential-Mode Conducted Emissions Modeling

6.1 Introduction

This chapter concludes the work presented in this thesis by analytically modeling the voltage and current waveforms of the full-bridge circuit using the non-linear differential equations introduced in Chapter 3, incorporating the experimental SiC MOSFET characteristics discussed in Chapter 2, the measured parasitic inductance of the power module from Chapter 4, and the baseplate parasitic capacitance identified in Chapter 5. Subsequently, a frequency-domain equivalent circuit is presented to predict the differential-mode conducted emission (DM-CE) noise of the full-bridge circuit.

6.2 Differential-Mode Conducted Emissions (DM-CE) Model

6.2.1 DM-CE Measurement

This paper discusses DM-CE on the input-side of a single-phase inverter. For Conducted Emissions measurement, Line Impedance Stabilization Network V-LISN is used as shown in Figure 6.1. Here, v_p and v_n are voltages between measurement ports of V-LISN connected at positive and negative line to the reference ground plane, and

differential-mode voltage is given by $v_{dm} = v_p - v_n$.

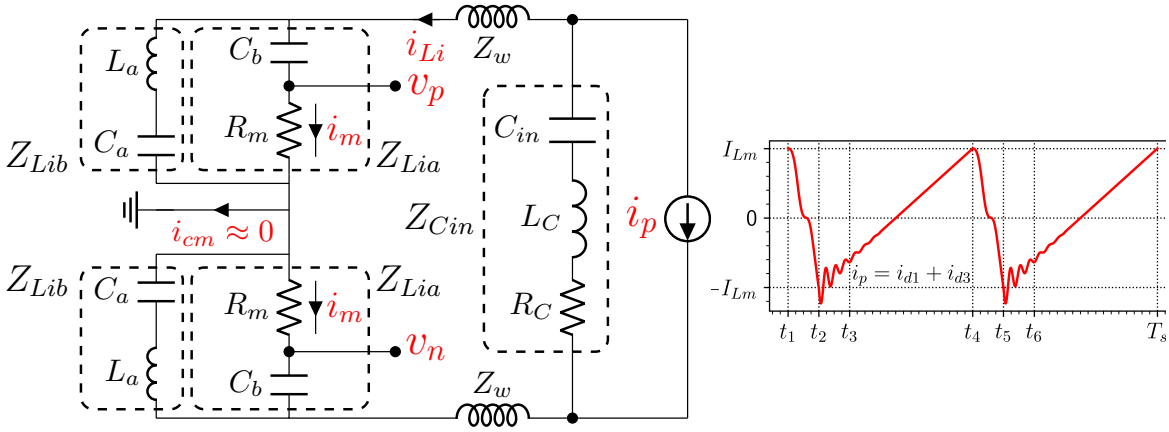


Figure 6.1 Differential-Mode equivalent circuit with noise current source.

6.2.2 DM-CE Equivalent Circuit

The input voltage V_{dc} and switching of power devices will induce line current i_p and i_n in the circuit. Assuming negligible common-mode current, positive line current i_p is equal to the negative line current i_n. Using substitution theorem [88], V_{dc} and full-bridge power module can then be substituted with a current source equal to i_p. The differential-mode equivalent circuit for single-phase inverter with noise current-source is shown in Figure 6.1. The positive line current, $i_p = i_{d1} + i_{d3}$ and device current i_{d1} and i_{d3} can be calculated using the model presented in previous section. However, the model differential equations are nonlinear and have no analytical solution. The Euler method is used to numerically solve the non-linear differential equations over one switching time period $T_s = 20\,\mu s$ and time-step $\Delta t = 0.01ns$. The k^{th} sample of line current is denoted by $i_p\,[k]$, where $k = \{0, 1, \cdots, N-1\}$ and total number of samples $N = T_s/\Delta t = 2 \cdot 10^6$.

In time-domain, current i_m flowing through the LISN measurement resistance R_m can be calculated by solving the circuit equations given by Eqs. (6.1)-(6.2) and differential-mode voltage is given by Eq. (6.3).

$$\frac{di_{Li}}{dt} = \frac{L_C \frac{di_p}{dt} - 2i_m R_m + (V_{Cin} - 2V_{Cb})}{2L_w + L_C} \tag{6.1}$$

$$\frac{di_m}{dt} = \frac{L_a \frac{di_{Li}}{dt} - i_m R_m + (V_{Ca} - V_{Cb})}{2L_a} \tag{6.2}$$

$$v_{dm}[k] = 2R_m i_m[k] \tag{6.3}$$

In frequency-domain, i_m can be written in terms of noise current-source i_p given by Eq. (6.4), where $G(s)$ is the transfer-function and $s = j2\pi f_n$. The current source i_p can then be transformed from discrete time-domain to frequency-domain using Discrete Fourier Transform (DFT) and is denoted by $I_p(f_n)$. The DM-CE spectrum at frequency f_n is given by Eq. (6.6).

$$I_m(s) = G(s) I_p(s) \tag{6.4}$$

$$G(s) = \frac{Z_{Cin} Z_{Lib}}{2Z_{Lia} Z_{Lib} + (Z_{Cin} + 2Z_w)(Z_{Lia} + Z_{Lib})} \tag{6.5}$$

$$\begin{aligned} V_{dm}(f_n) &= [2R_m G(j2\pi f_n)] I_p(f_n) \\ &= Z_{dm}(f_n) I_p(f_n) \end{aligned} \tag{6.6}$$

6.3 Simulated Full-Bridge Inverter Circuit Waveforms

6.3.1 Line Current (i_p) Waveform

The single-phase inverter experiment setup used a Full-Bridge SiC Power Module as shown in Figure 6.2 and the experiment parameters are described in Table 6.1. A 1GHz, 20GSa/s Keysight DSOS104A Oscilloscope was used for measurements. The drain-source voltage was measured using 500 MHz PMK BumbleBee differential probe and line current was measured using 100 MHz SS-683 Iwatsu current probe.

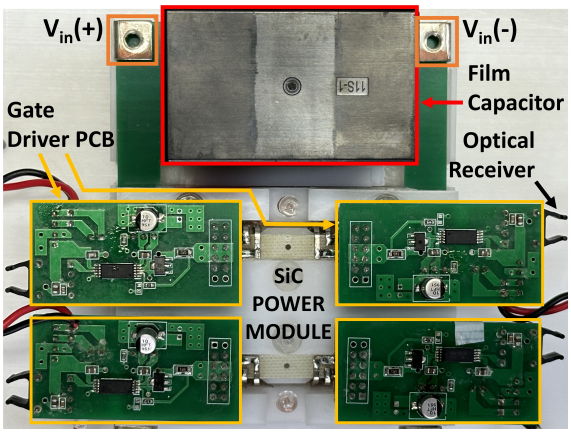


Figure 6.2 Experiment setup of single-phase inverter for switching transients measurement.

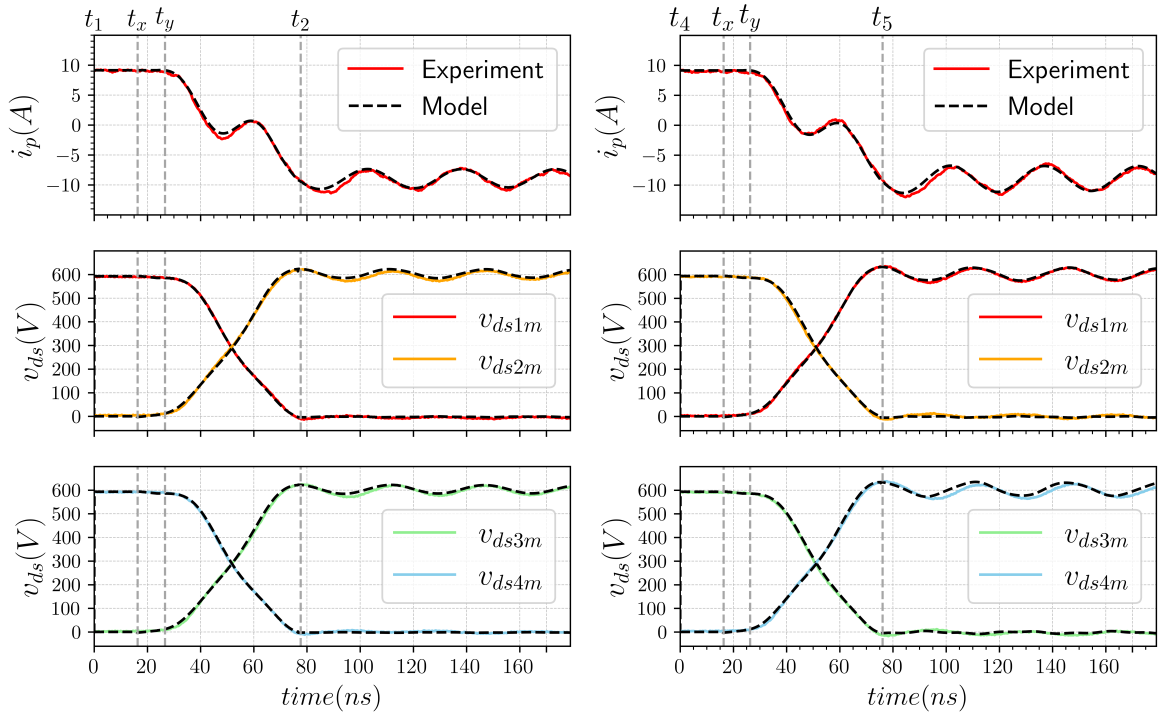
Table 6.1 Experiment Parameters

Parameter	Value/Part No.	Remarks
V_{dc}	500 V, 600 V	Input DC Voltage
L_{out}	326 µH	Load Inductor
f_s, T_s	50 kHz, 20 µs	Switching Frequency, Time-Period
I_{Lm}	7.67 A_{pk}, 9.20 A_{pk}	$= V_{dc}/(4L_{out}f_s)$, Peak Load Current
R_g	1 Ω, 2.5 Ω	External Gate Resistance
SiC MOSFET	ROHM S4103	

The line current (i_p) and device voltages obtained from switching transients model simulation are compared with experimentally measured waveforms at three operating conditions for different input dc voltage V_{dc} and external gate resistance R_g. The rate of change of voltage across the switching device during the turn-off transient, $(dv_{ds}/dt)_{off}$ is calculated for the change of v_{ds} from 10 % to 90 % of its final value $\approx V_{dc}$. During the turn-on transient, $(dv_{ds}/dt)_{on}$ is calculated for the change of v_{ds} from 90 % to 10 % of its initial value $\approx V_{dc}$. The rate of change of line current, di_p/dt was calculate for change of i_p from I_{Lm} to $-I_{Lm}$.

For V_{dc}=600 V and R_g=1 Ω, switching waveforms are shown in Figure 6.3 and, dv_{ds}/dt and di_p/dt are given in Table 6.2. As we increase R_g from 1 Ω to 2.5 Ω, dv_{ds}/dt decreases from an average of ∼15.42 V/ns to ∼14.19 V/ns for measured and

$\sim$15.44 V/ns to $\sim$14.22 V/ns for simulated device voltage waveforms. The average value is arithmetic mean of dv_{ds}/dt of all four devices during S_1 and S_3 mode of operation (as discussed in Section 3.1). Similarly, di_p/dt decreases from an average of $\sim$0.376 A/ns to $\sim$0.328 A/ns for measured and $\sim$0.381 A/ns to $\sim$0.332 A/ns for simulated line current waveforms. Here, the average value is arithmetic mean of di_p/dt during S_1 and S_3 mode of operation. The waveforms for V_{dc}=600 V and R_g=2.5 Ω are shown in Figure 6.4 and, dv_{ds}/dt and di_p/dt are given in Table 6.3.



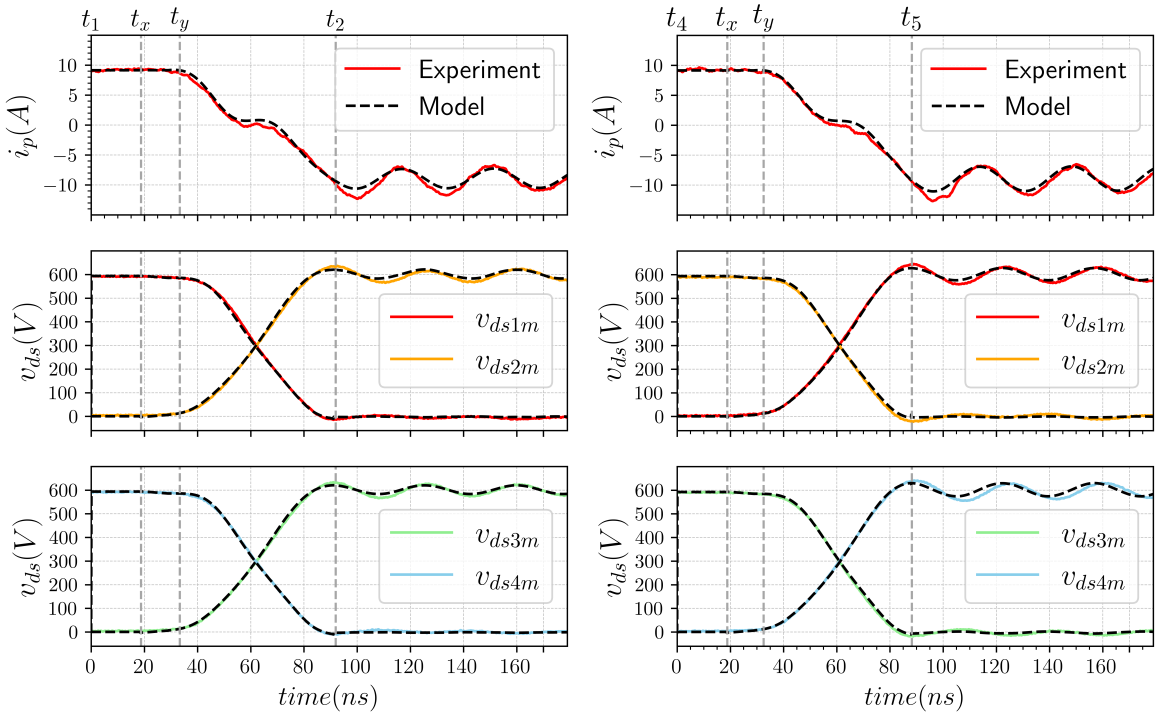
(a) M_2-M_3 are turning off (b) M_1-M_4 are turning off

Figure 6.3 Simulation and Experiment waveform for V_{dc}=600 V and R_g=1 Ω.

For R_g=1 Ω, decreasing V_{dc} from 600 V to 500 V causes dv_{ds}/dt to decrease from an average $\sim$15.42 V/ns to $\sim$11.79 V/ns for measured and $\sim$15.44 V/ns to $\sim$11.98 V/ns for simulated device voltage waveforms. The di_p/dt decreases from an average $\sim$0.376 A/ns to $\sim$0.284 A/ns for measured and $\sim$0.381 A/ns to $\sim$0.291 A/ns for simulated line current waveforms. The waveforms for V_{dc}=500 V and R_g=1 Ω are shown in Figure 6.5 and, dv_{ds}/dt and di_p/dt are given in Table 6.4. Although simulated switching waveform matches closely with experimentally measured waveforms for all operating conditions presented, the error between simulated and measured dv_{ds}/dt can be attributed to the discrepency between parasitics of experimental prototype and the corresponding

Table 6.2 dv_{ds}/dt and di_p/dt comparison for V_{dc}=600 V and R_g=1 Ω

Device	Parameter	M_2-M_3 are turning off (S_1)		M_1-M_4 are turning off (S_3)	
		Exp.	Sim.	Exp.	Sim.
M_1	dv_{ds1}/dt	-15.22 V/ns	-15.42 V/ns	15.60 V/ns	15.36 V/ns
M_2	dv_{ds2}/dt	15.05 V/ns	15.08 V/ns	-15.68 V/ns	-15.87 V/ns
M_3	dv_{ds3}/dt	15.24 V/ns	15.11 V/ns	-15.76 V/ns	-15.86 V/ns
M_4	dv_{ds4}/dt	-15.27 V/ns	-15.46 V/ns	15.52 V/ns	15.34 V/ns
–	di_p/dt	-0.367 A/ns	-0.373 A/ns	-0.384 A/ns	-0.389 A/ns



(a) M_2-M_3 are turning off (b) M_1-M_4 are turning off

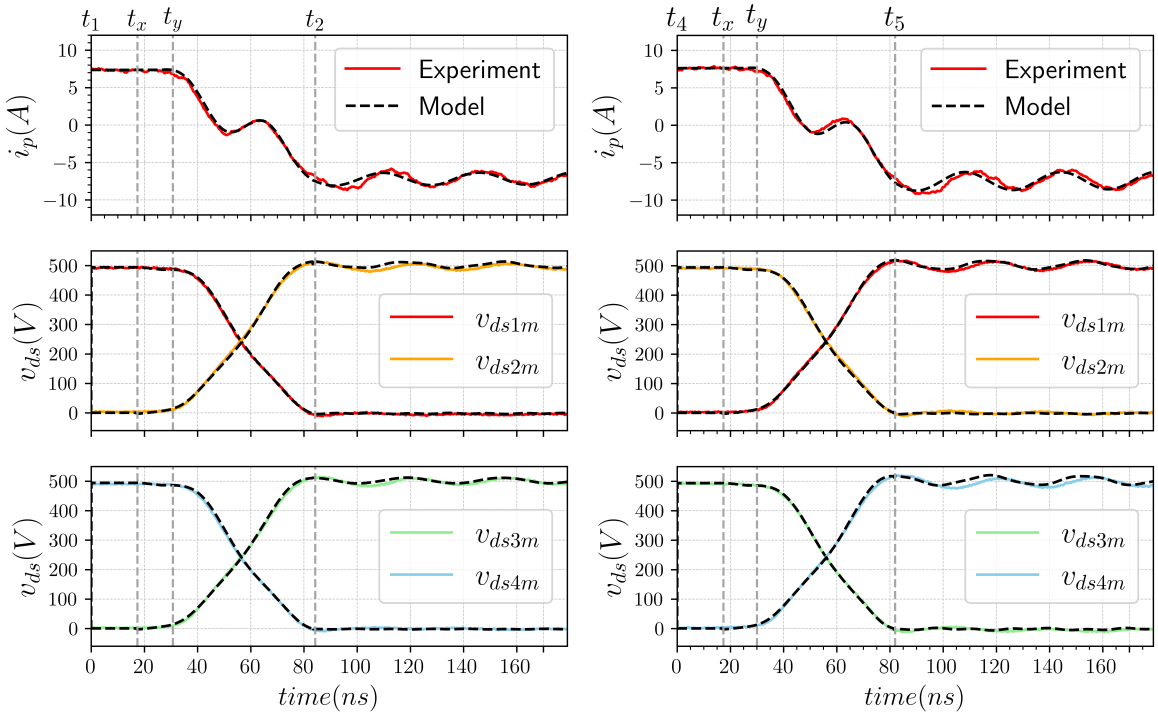
Figure 6.4 Simulation and Experiment waveform for V_{dc}=600 V and R_g=2.5 Ω.

parameters used in non-linear model.

The simulated line current i_p over one switching cycle T_s for V_{dc}=600 V and R_g=1 Ω is shown in Figure 6.6. For analysis, i_p can be divided into three components: linear, transient and oscillation. The time-domain i_p and its components separately were transformed to frequency domain using DFT and their magnitude in dB and phase in ° (degree) are as shown in Figure 6.7. For $f < 8$ MHz, linear component of I_p will

Table 6.3 dv_{ds}/dt and di_p/dt comparison for V_{dc}=600 V and R_g=2.5 Ω

Device	Parameter	M_2-M_3 are turning off (S_1)		M_1-M_4 are turning off (S_3)	
		Exp.	Sim.	Exp.	Sim.
M_1	dv_{ds1}/dt	-14.14 V/ns	-14.15 V/ns	14.33 V/ns	14.25 V/ns
M_2	dv_{ds2}/dt	13.82 V/ns	13.75 V/ns	-14.76 V/ns	-14.63 V/ns
M_3	dv_{ds3}/dt	13.62 V/ns	13.82 V/ns	-14.74 V/ns	-14.66 V/ns
M_4	dv_{ds4}/dt	-13.89 V/ns	-14.21 V/ns	14.20 V/ns	14.27 V/ns
–	di_p/dt	-0.313 A/ns	-0.318 A/ns	-0.343 A/ns	-0.346 A/ns



(a) M_2-M_3 are turning off (b) M_1-M_4 are turning off

Figure 6.5 Simulation and Experiment waveform for V_{dc}=500 V and R_g=1 Ω.

dominate with a slope of −20 dB/decade. For $f > 10$ MHz, phase of transient component becomes negative and causes a sudden drop in I_p magnitude. The accuracy of spectrum model for $f > 8$ MHz is contingent on accurate switching transient modeling. The oscillation component will dominate I_p near the parasitic oscillation frequency.

Table 6.4 dv_{ds}/dt and di_p/dt comparison for V_{dc}=500 V and R_g=1 Ω

Device	Parameter	M_2-M_3 are turning off (S_1)		M_1-M_4 are turning off (S_3)	
		Exp.	Sim.	Exp.	Sim.
M_1	dv_{ds1}/dt	-11.67 V/ns	-11.96 V/ns	11.87 V/ns	11.95 V/ns
M_2	dv_{ds2}/dt	11.73 V/ns	11.75 V/ns	-11.91 V/ns	-12.23 V/ns
M_3	dv_{ds3}/dt	11.64 V/ns	11.77 V/ns	-11.93 V/ns	-12.25 V/ns
M_4	dv_{ds4}/dt	-11.69 V/ns	-11.99 V/ns	11.85 V/ns	11.93 V/ns
–	di_p/dt	-0.273 A/ns	-0.280 A/ns	-0.295 A/ns	-0.301 A/ns

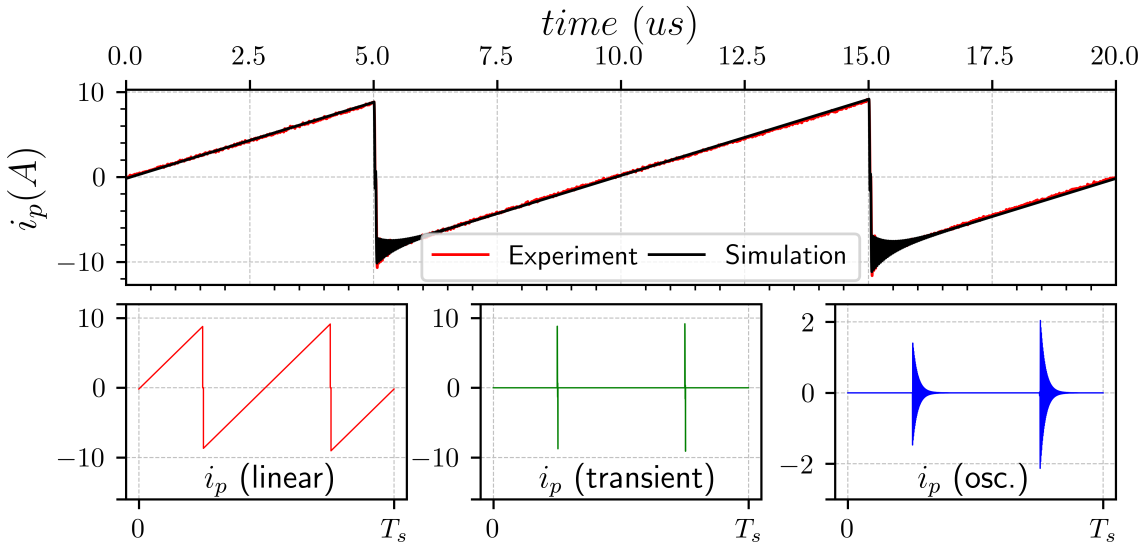


Figure 6.6 Simulated line current i_p over one switching cycle T_s = 20 µs in time-domain for V_{dc}=600 V and R_g=1 Ω.

6.4 Simulated Differential-Mode Voltage

The DM-CE measurement setup is shown in Figure 6.8 . The the measurement ports of LISN-A and LISN-B (Solar Electronics 9117-5-PJ-50-N) are connected to mode-splitter switch (Schwarzbeck CMDM 8700 B) using co-axial cables with BNC connector to measure differential-mode voltage. The spectrum analyzer (R&S FSV) measures the frequency spectrum of DM-CE. The equipment under test, single-phase inverter was floating 5cm above the ground plane.

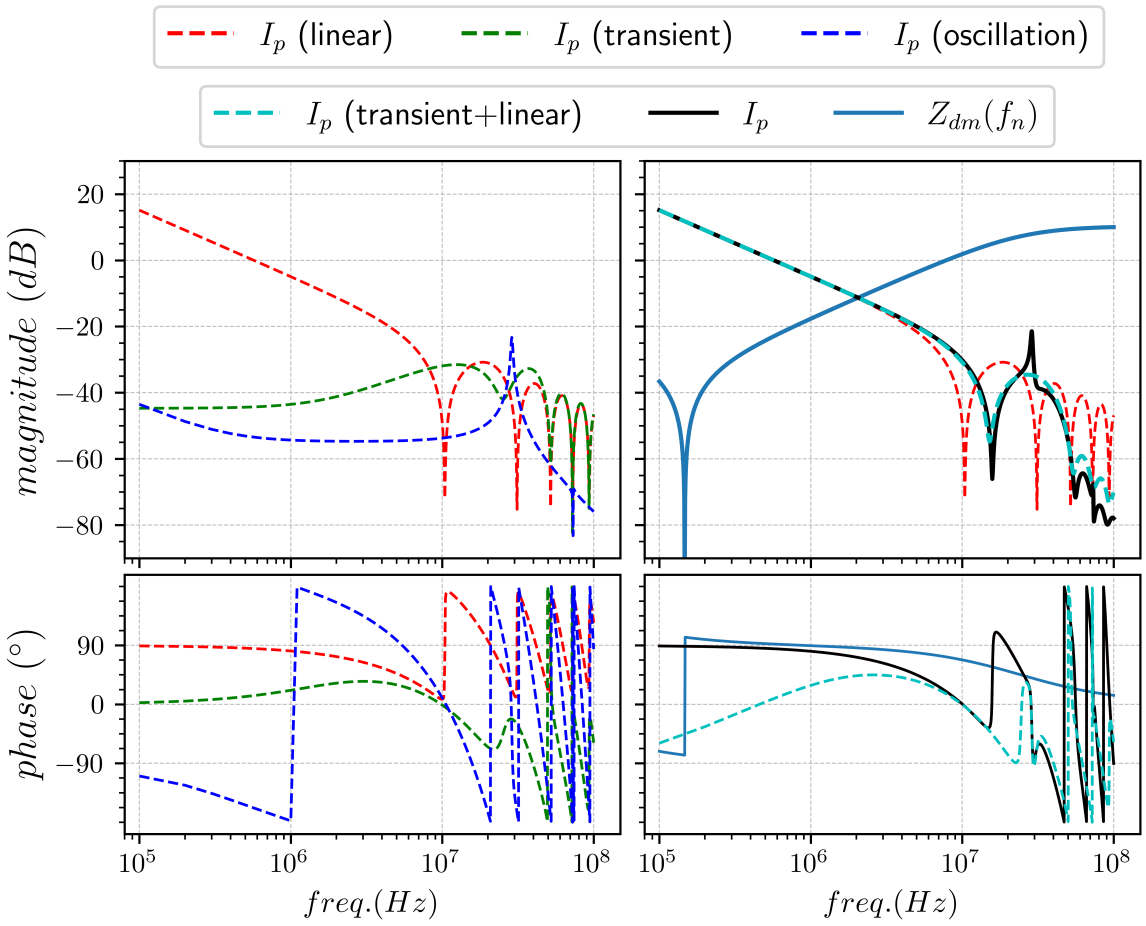
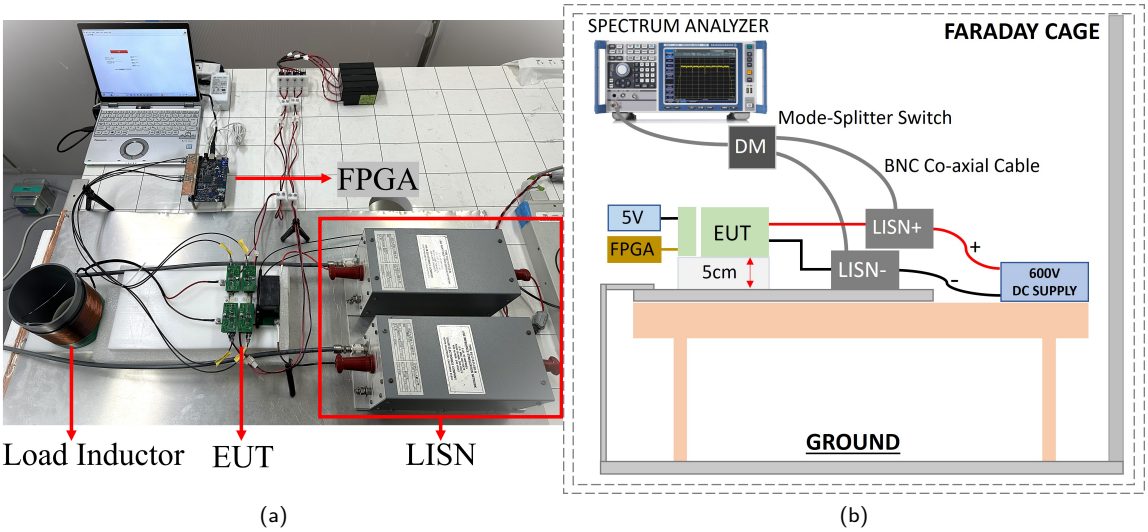


Figure 6.7 Simulated line current i_p over one switching cycle $T_s = 20\,\mu s$ in frequency–domain for V_{dc}=600 V and R_g=1 Ω.



(a) (b)

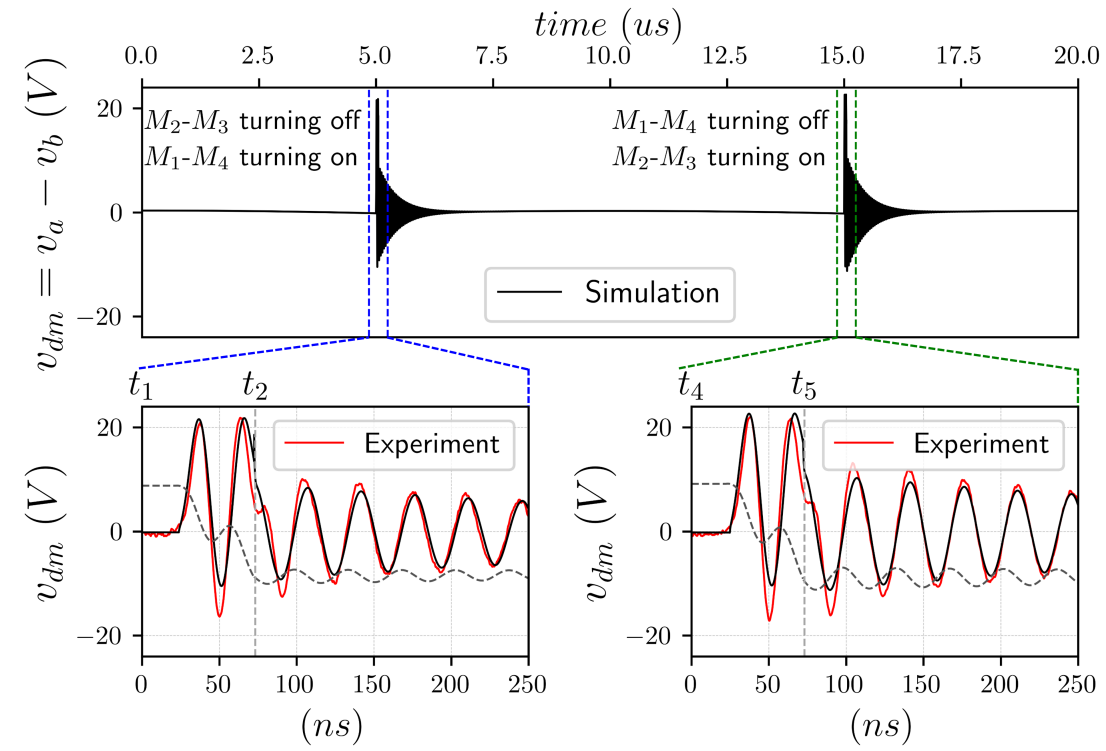
Figure 6.8 DM-CE measurement (a) experiment setup and (b) setup block diagram.

Time-domain

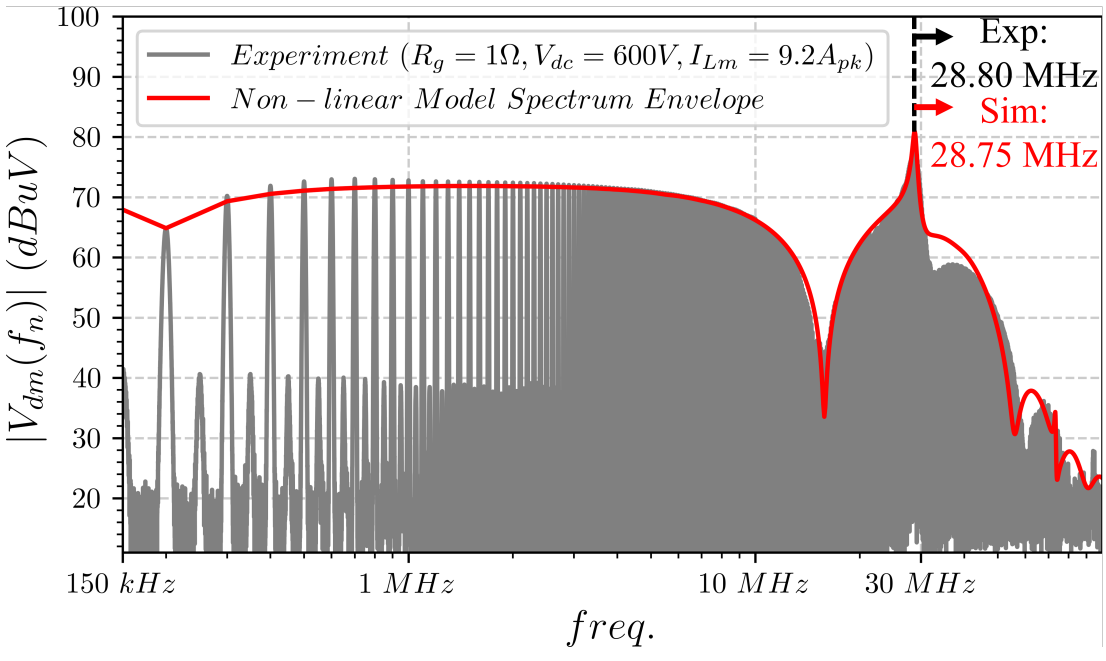
The differential-mode noise voltage (v_{dm}) was measured experimentally across the LISN measurement ports v_a and v_b. The simulated differential-mode voltage in time-domain by Eq. (6.3) is compared with measured result in Figure 6.9a for V_{dc}=600 V and R_g=1 Ω, Figure 6.10a for V_{dc}=600 V and R_g=2.5 Ω and Figure 6.11a for V_{dc}=500 V and R_g=1 Ω. The first two peaks in the expanded view correspond to the fall of i_p from I_{Lm} to $-I_{Lm}$ between $t_1 < t < t_2$ (S_1) and $t_4 < t < t_5$ (S_3). Beyond t_2 (and t_5), switching oscillations dominate and calculated values closely agrees with the simulated values. The non-linear model used for noise current source (i_p) calculation depends on SiC MOSFET device characteristics. Also, circuit parasitics were obtained from FEM simulation of an equivalent 3D model of experiment prototype. The error between calculated and measured v_{dm} can be attributed to the discrepency between parasitics of experimental prototype and the corresponding parameters used in non-linear model.

Frequency-domain

The DM-CE in frequency-domain was calculated by Eq. (6.6) and compared with experimentally measured spectrum. For V_{dc}=600 V and R_g=1 Ω, as shown in Figure 6.9b, simulated DM-CE spectrum follows experiment result with a difference of ±1 dB from 200 kHz to 30.80 MHz. The simulated noise spectrum peaks at 28.75 MHz with a magnitude of 80.28 dBµV compared 28.80 MHz at 79.29 dBµV for experimental observation. The peak frequency corresponds to the parasitic oscillation frequency of devices during switching transients. Similarly for V_{dc}=600 V and R_g=1 Ω, simulated spectrum closely follows measured result from 200 kHz to 29.25 MHz with peak of 80.95 dBµV at 28.79 MHz compared to 80.18 dBµV at 28.90 MHz for measured value, as shown in Figure 6.9b. As V_{dc} is decreased from 600 V to 500 V, the C_{oss} of device in off-state increases and parasitic oscillation frequency decreases. The spectrum for V_{dc}=500 V and R_g=1 Ω is shown in Figure 6.11b. The simulated spectrum peaks at 27.59 MHz compared to 27.80 MHz for experimental observation. The presented model accurately predicts DM-CE spectrum in the frequency range of 150 kHz-30 MHz, which is the common frequency range defined in regulatory standards such as CISPR 32 for conducted



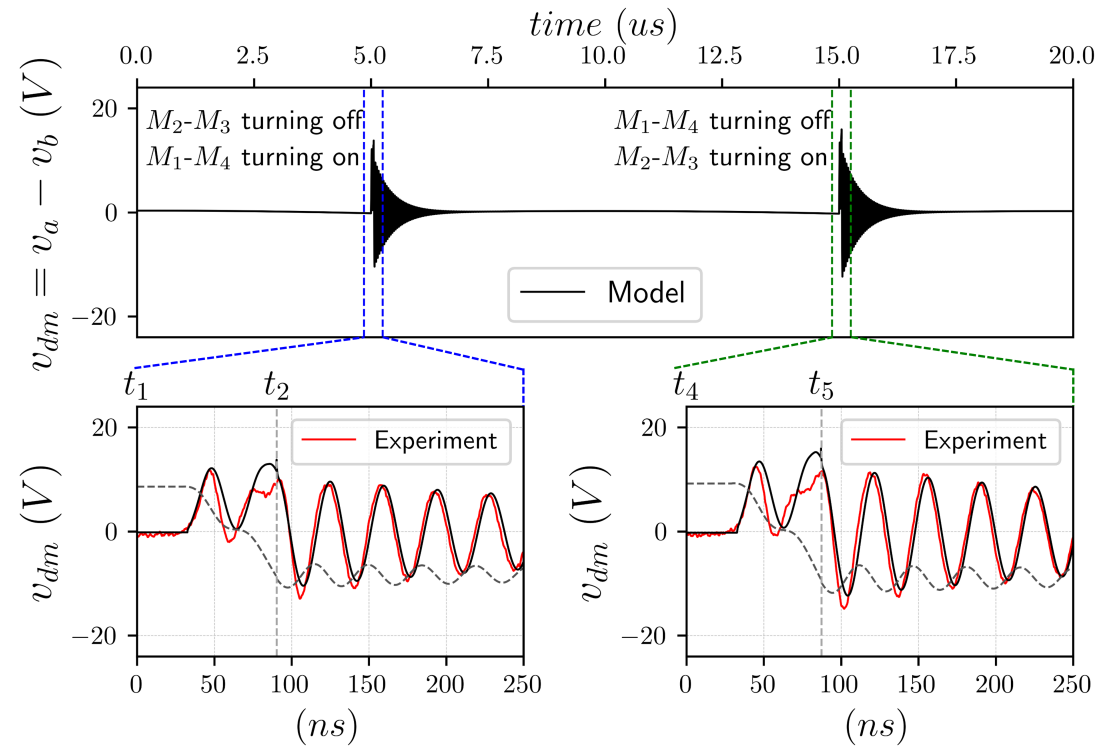
(a)



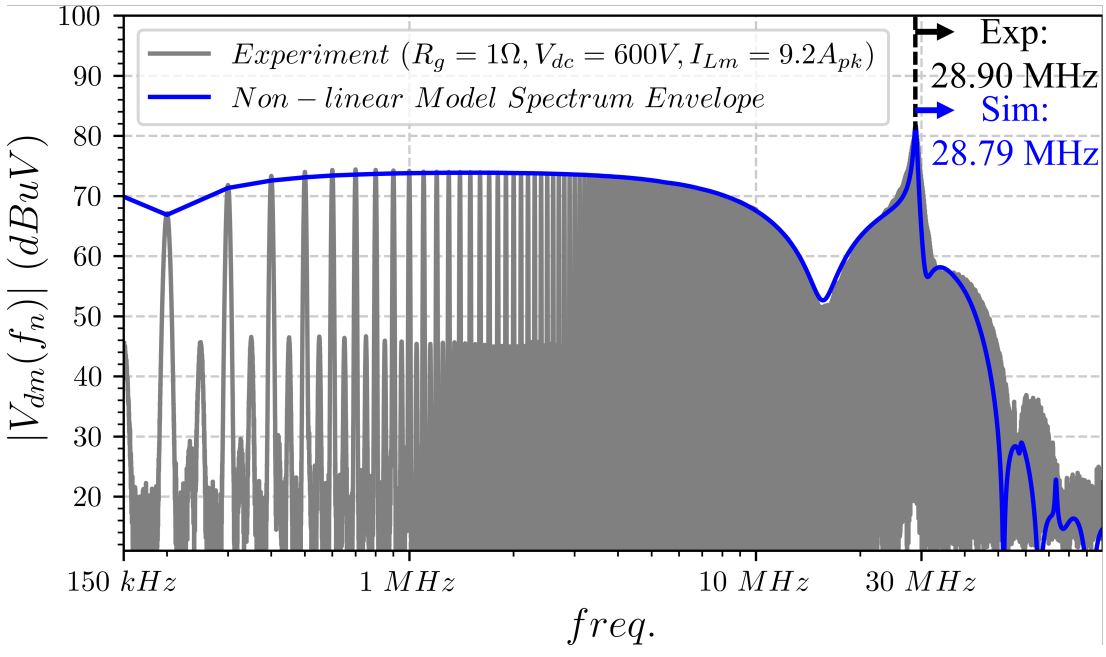
(b)

Figure 6.9 Comparison of simulated and measured differential-mode voltage v_{dm} in (a) time-domain and (b) frequency-domain over one switching cycle $T_s = 20\,\mu s$ for V_{dc}=600 V and R_g=1 Ω.

emissions limits.

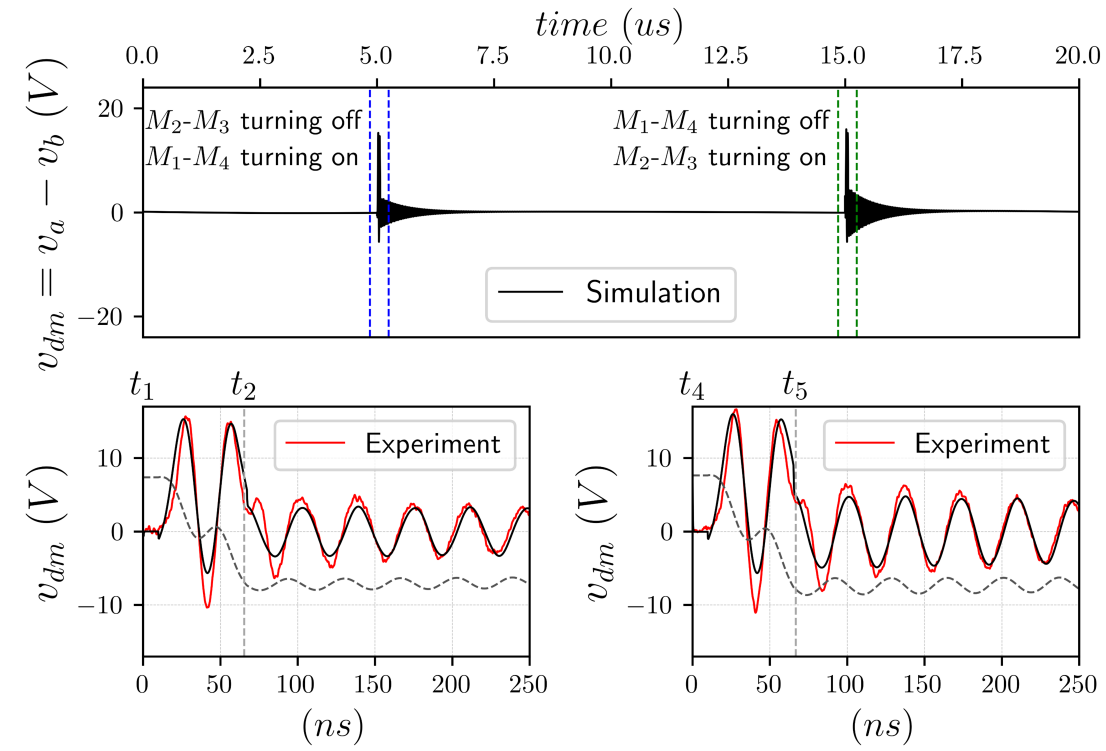


(a)

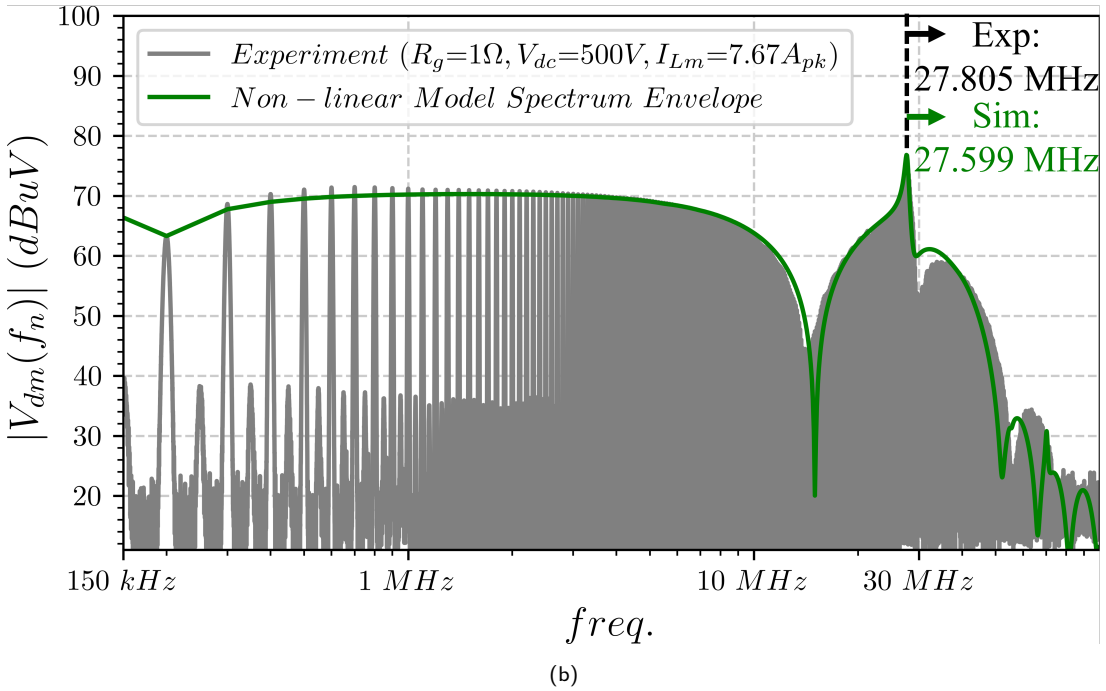


(b)

Figure 6.10 Comparison of simulated and measured differential-mode voltage v_{dm} in (a) time-domain and (b) frequency-domain over one switching cycle $T_s = 20\,\mu s$ for V_{dc}=600 V and R_g=2.5 Ω.



(a)



(b)

Figure 6.11 Comparison of simulated and measured differential-mode voltage v_{dm} in (a) time-domain and (b) frequency-domain over one switching cycle $T_s = 20\,\mu s$ for V_{dc}=500 V and R_g=1 Ω.

6.5 Summary

In this chapter, we numerically solve the non-linear differential equations presented in Chapter 3 to model power device state variables and full-bridge circuit current and voltage waveforms using Euler method in Python. Then, differential-mode conducted emission (DM-CE) were modeled in the frequency domain using the equivalent circuit model. The presented model accurately predicts DM-CE spectrum in the frequency range of $150\,\mathrm{kHz} - 30\,\mathrm{MHz}$, with an error of less than $\pm 1\,\mathrm{dB}$ compared to experimental measurements. This method provides a model with fast calculation times and fairly accurate predictions, eliminating the need for time-domain circuit measurements.

Chapter 7

Conclusion

In this thesis, we presented an analytical modeling approach to predict the conducted emissions noise spectrum in a single-phase inverter circuit implemented using a full-bridge power module.

First, in Chapter 2, we discussed the advantages of silicon carbide (SiC) MOSFETs compared to silicon-based power devices. Next, we presented a new empirical model for the capacitances of S4103 1200V/95A bare-die SiC MOSFET used in this research work and compared its accuracy with models proposed in the literature. Subsequently, we analyzed the operation of a full-bridge power module (FBPM) configured as a single-phase inverter driving an inductive load using phase-shift modulation. Finally, we presented a simplified lumped-element circuit model of the FBPM with combined parasitic capacitances.

In Chapter 3, we first modeled circuit variables such as displacement current in parasitic capacitances, current in the input capacitor, differential-mode current, and common-mode (ground) current based on the drain-source voltage and drain current of power devices in the full-bridge circuit. Next, we developed an analytical model for the power device state variables during one transient state, which can be generalized to other states in a switching cycle. The model was then extended to include the time delay introduced by phase-shift modulation. Because these state variables depend on parasitic capacitances, which vary with the bias voltage across device terminals, the resulting analytical model is non-linear.

Chapter 4 presents a procedure for calculating the wiring parasitic inductance of

a FBPM, which is modeled as a 4-port lumped-element network with eight unknown impedance. To characterize these impedance, a numerical model is developed based on network Z-parameters. The 4-port S-parameters of the FBPM are experimentally measured using a 4-port vector network analyzer and then converted into Z-parameters. These Z-parameters are used to solve for the unknown network impedance, which represent the wiring parasitic inductance. Additionally, the parasitic inductance of the power module is obtained through finite element method (FEM) simulation. The simulated inductance values show good agreement with the calculated results. The largest difference was 4.585 %, the smallest was 0.058 %, and the average was 2.316 %.

Chapter 5 introduces a non-destructive technique for identifying parasitic capacitances in an FBPM. Using the common-mode equivalent circuit model presented in Chapter 3, we first characterized the parasitic capacitance in terms of noise source voltages and LISN output voltages. We then measured the noise-source voltages across the power-module terminals, along with the voltages at the LISN outputs, and calculated the parasitic capacitances. The calculated values matched closely with values obtained from the FEM simulation of the detailed 3D model of power module.

Then in Chapter 6, we numerically solve the non-linear differential equations presented in Chapter 3 to model power device state variables and full-bridge circuit current and voltage waveforms using Euler method in Python. Then, differential-mode conducted emission (DM-CE) were modeled in the frequency domain using the equivalent circuit model. The presented model accurately predicts DM-CE spectrum in the frequency range of 150 kHz − 30 MHz, with an error of less than ±1 dB compared to experimental measurements. This method provides a model with fast calculation times and fairly accurate predictions, eliminating the need for time-domain circuit measurements.

7.1 Key Contributions

1. Introduces a new method to characterize parasitic inductances in a full-bridge power module using 4-port S-parameter measurements.

2. Proposes a non-destructive technique for identifying parasitic capacitances in a

full-bridge power module.

3. Presents an analytical model of full-bridge circuit voltage and current waveforms including power device state-variables considering parasitic capacitance in the full-bridge power module. Then accurately predicts differential-mode conducted emissions noise spectrum within $\pm 1\,\mathrm{dB}$ over $150\,\mathrm{kHz} - 30\,\mathrm{MHz}$ frequency range.

Publications

[Published papers]

1. Deepankar, Takaaki Ibuchi, Tsuyoshi Funaki, Parasitic Inductance Characterization of Full-Bridge Power Module Based on S-Parameter Measurements, IEEJ Journal of Industry Applications, 2025, Volume 14, Issue 3, Pages 477-483.

2. Deepankar, Takaaki Ibuchi, Tsuyoshi Funaki, Non-destructive Characterization of Parasitic Capacitances in Full-Bridge Power Module, IEEJ Journal of Industry Applications. [Advance online publication]

3. Deepankar, Takaaki Ibuchi, Tsuyoshi Funaki, Non-linear Modeling of High-Frequency Differential-Mode Conducted EMI Emissions in Single-Phase Inverter, IEEJ Journal of Industry Applications, 2025, Volume 14, Issue 4, Pages 575-582.

[International conference proceeding]

1. Deepankar, T. Ibuchi , T. Funaki , H. Sakai, T. Miyazaki, Y. Okawachi, "Analysis of DM EMI Noise Frequency Spectrum in Full-Bridge Inverter for Phase-Shift PWM," 2024 IEEE Joint International Symposium on Electromagnetic Compatibility, Signal & Power Integrity: EMC Japan/Asia-Pacific International Symposium on Electromagnetic Compatibility (EMC Japan/APEMC Okinawa), May 20-24, 2024. (Oral)

2. Deepankar, Takaaki Ibuchi, Tsuyoshi Funaki, Hiroto Sakai, Tatsuya Miyazaki, and Yuta Okawachi, "Comparison between Experimental and FEM Simulation Results of Differential-Mode Noise in SiC MOSFET based Full-Bridge Power

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