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1 **Controlled trap formation in SiC metal-oxide-semiconductor**
2 **structures via gate bias stress and its impact on the performance**
3 **of metal-oxide-semiconductor field-effect transistors**

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12 We regulated trap formation in silicon carbide (SiC) metal-oxide-semiconductor (MOS) structures
13 by applying gate bias stress and evaluated how traps at different energy levels degrade the
14 performance of SiC MOS field-effect transistors (MOSFETs). Specifically, samples with
15 systematically varied nitridation conditions were prepared, and the impact of interface traps
16 generated under negative-bias stress at an elevated temperature of 300°C was investigated. Carrier
17 trapping behavior and mobility degradation trends were examined using the transfer characteristics
18 together with Hall-effect measurements. In samples without nitridation, the interface states in the
19 shallow energy region ($E_C - E_T = 0 - 0.10$ eV) increased under stress, and they were found to act as
20 carrier traps. In nitrated samples, the interface states in relatively deep energy regions ($E_C - E_T =$
21 $0.15 - 0.35$ eV) increased and functioned as Coulomb scattering centers, thereby reducing the free
22 electron mobility.

I. INTRODUCTION

Silicon carbide (SiC) is a wide-bandgap semiconductor that is well suited for power electronics applications¹. Among SiC-based devices, metal-oxide-semiconductor field-effect transistors (MOSFETs) are especially promising as power switches. However, the performance of SiC MOSFETs has been limited by their high on-resistance, which is primarily attributable to the channel component. Indeed, estimates indicate that 48–66% of the total on-resistance is governed by the channel resistance for 600–1200 V-class SiC MOSFETs². The high channel resistance arises from carrier trapping caused by the high interface state density (D_{it}) in the MOS structure^{3–7}, as well as from degradation in free carrier mobility induced by carrier scattering^{5,8–14}. In general, the field-effect mobility (μ_{FE}), which is evaluated from the drain current–gate voltage (I_D – V_G) characteristics of a transistor, reflects both the free carrier density and free carrier mobility. To separate and evaluate these contributions, it is effective to examine the Hall mobility (μ_{Hall}), which represents the free carrier mobility and can be obtained from MOS Hall-effect measurements. Indeed, previous studies have evaluated μ_{Hall} and discussed the influence of interface states, fixed charges, dipole scattering, surface roughness, and other factors^{8–11}. However, elucidating the scattering mechanisms in SiC MOSFETs is not straightforward. For example, to investigate the effect of interface states on carrier mobility, it is necessary to prepare a set of samples in which D_{it} is systematically varied. Over the course of MOSFET research and development, intensive efforts have been devoted to understanding the origin of the interface states^{2,15–20}. Accordingly, several interface-state-reduction techniques, such as nitric oxide (NO) annealing^{21–23}, ultra-high-temperature oxidation²⁴, and oxidation with rapid cooling²⁵, have been devised. Recent studies have pointed out that minimization of SiC oxidation, combined with interface nitridation^{26–29} or hydrogen annealing³⁰, is a key factor to forming a high-quality SiC MOS interface. Nevertheless, variations in the process tend to alter characteristics other than D_{it} , such as fixed charges and dipoles, making it difficult to isolate their individual effects on carrier mobility. As an example illustrating this difficulty, a previous study has shown that when D_{it} is reduced by NO annealing, μ_{Hall} instead decreases⁵, which cannot be straightforwardly understood.

To address this issue, we proposed an approach in which gate bias stress is applied to the MOS structure to selectively generate fixed charges and interface states³¹. In practice, when a negative bias stress is applied at room temperature to an NO-annealed n -channel MOSFET, holes are captured in the oxide, allowing the influence of fixed charges to be examined. Furthermore, applying stress at an elevated temperature of 300°C additionally generates interface states, enabling evaluation of their effect. It was clarified that oxide fixed charges formed by stress have only a minor impact on μ_{Hall} , whereas the interface states generated by stress significantly degrade it. However, whether nitridation-introduced nitrogen atoms are associated with stress-induced strong scattering centers is still not well understood. Moreover, a systematic understanding is still lacking regarding how the stress-induced interface states, depending on their energy levels, contribute to carrier trapping or act as scattering centers.

Given this background, in this study we prepared samples under systematically varied NO annealing conditions to control the nitrogen concentration at the interface, and evaluated the traps generated by applying gate stress to these samples. This allowed us to distinguish whether the stress-induced interface states originate from nitrogen. Additionally, by evaluating both μ_{FE} and μ_{Hall} in the stressed samples, we distinguished the effects of the generated interface states on carrier trapping and scattering. Through this investigation, we aim to obtain insights into the nature of traps that can become killer defects in MOS devices and strategies for their mitigation.

II. EXPERIMENTAL PROCEDURE

P-type SiC(0001) epilayers with an acceptor density of $8 \times 10^{15} \text{ cm}^{-3}$ were used in this study. After cleaning the samples' surface, oxides were formed by dry oxidation and Ar annealing at 1200°C , followed by NO annealing for 30, 60, or 120 min. These samples are denoted as “NO30”, “NO60”, and “NO120”, depending on the NO annealing time. A sample that was not annealed in NO was also prepared for comparison (sample “w/o NO”). The capacitance-equivalent oxide thicknesses of the samples were about 50 nm. MOSFETs and MOS Hall bars were fabricated using these gate oxides. The gate electrode was made of polycrystalline silicon. For the MOSFETs, the channel length (L) and width (W) were $5 \mu\text{m}$ and $200 \mu\text{m}$, respectively; for the MOS Hall bars, they were $300 \mu\text{m}$ and $40 \mu\text{m}$. A negative gate bias stress corresponding to an oxide field of -8 MVcm^{-1} was applied to the samples for up to 2000 s at 300°C . The stress was temporarily interrupted at discrete stress times to perform intermediate measurements, allowing us to monitor the evolution of interface states in MOS structures. Measurements on the MOSFETs and on the MOS Hall bars were repeatedly performed to monitor the change in μ_{FE} and μ_{Hall} due to bias stress. While the $I_{\text{D}}-V_{\text{G}}$ measurements on MOSFETs were performed at 300°C , measurements on MOS Hall bars were performed at room temperature. Hall-effect measurements were performed under a magnetic field of 0.2 T.

III. RESULTS & DISCUSSION

Figures 1(a)–(d) show the normalized $I_{\text{D}}-V_{\text{G}}$ characteristics measured at 300°C for the fabricated MOSFETs. The changes induced by the negative bias stress are shown for each sample condition. For the sample w/o NO, the V_{G} value at a typical reference current level of $I_{\text{D}} \cdot L/W = 10^{-8} \text{ A}$ drifted toward the positive direction under bias stress, accompanied by a stretch-out of the $I_{\text{D}}-V_{\text{G}}$ characteristics, indicating the generation of interface states. In contrast, for the nitrided samples, the V_{G} value initially drifted in the negative direction upon the application of stress, and then drifted in the positive direction as the stress continued to be applied. The initial negative drift is attributed to hole trapping in the oxide, whereas the subsequent positive drift is caused by the increase in D_{it} , as described above. The negative voltage drift became more pronounced for longer NO annealing times, indicating that the nitridation process induced hole traps in the oxide, consistent with previous studies^{32,33}. The absence of a negative voltage drift in the sample w/o NO can be attributed to the lack

of nitridation-induced hole-trap generation, which allows the effect of the increased D_{it} to dominate.

Figures 2(a)–(d) plot μ_{FE} as a function of V_G evaluated at 300°C for the fabricated MOSFETs. Again, the changes induced by the negative bias stress are shown for each sample condition. Comparing the maximum μ_{FE} ($\mu_{FE,max}$) values before applying stress, annealing in NO for more than 30 min significantly increased the $\mu_{FE,max}$ from about 16 cm²V⁻¹s⁻¹ for the sample w/o NO to above 30 cm²V⁻¹s⁻¹. This is clearly due to trap passivation by interface nitridation^{21–23}, which increases the number of mobile electrons that contribute to conduction⁵. When the stress was applied, all the samples exhibited significant decrease in μ_{FE} . While the degradation in μ_{FE} with respect to the no-stress value (zero-second stress plots) seems to be similar across the samples, a quantitative discussion will be provided in the following paragraph. Considering the findings up to this point, both stress-induced interface defects and fixed charges (trapped holes) in the oxide can be considered as possible causes of the μ_{FE} degradation. Nevertheless, we clarified that the stress-induced positive fixed charge in the oxide has a limited impact on mobility in a previous study³¹. Since the fixed charges arise from holes trapped in the SiO₂ layer under high electric field, they are located far enough from the interface, and their influence on carrier scattering is therefore expected to be minimal. We thus will focus on the effect of stress-induced interface states in what follows.

Figure 3 shows the ratio of the maximum μ_{FE} to the no-stress value, as well as the change in the subthreshold swing (SS) as a function of stress time. Here, the SS value was evaluated within the current range of $I_D \cdot L/W = 10^{-11} - 10^{-10}$ A, reflecting the contribution from D_{it} at certain energy levels below the conduction band edge (E_C) of SiC. The energy-level range of the interface states will be discussed in detail later. As expected, the rate of decrease in the maximum μ_{FE} due to stress was similar among the samples, regardless of process conditions. In contrast, the degradation in SS was more pronounced for samples subjected to nitridation. For example, while the SS degradation with 2000 s stress in the sample w/o NO was 0.23 Vdec⁻¹, the sample NO120 reached 0.42 Vdec⁻¹, nearly twice as large. This suggests that the mechanism of μ_{FE} degradation differs depending on whether the sample was subjected to nitridation.

Next, let us examine the origins of the μ_{FE} degradation as revealed by the MOS Hall-effect measurements. Figures 4(a)–(d) show the free electron density (n_{free}) as a function of overdrive voltage ($V_G - V_{th}$) evaluated from MOS Hall-effect measurements at room temperature. To eliminate the influence of the negative voltage drift caused by hole trapping in oxide traps and to focus solely on the effect of the increased D_{it} , the horizontal axis is expressed in terms of the overdrive voltage. The threshold voltage V_{th} denotes the turn-on voltage and was determined as the V_G at which $I_D \cdot L/W = 10^{-9}$ A. The data before and after the 2000 s stress are shown for each sample. First, before applying stress (0 s), n_{free} is at most on the order of 10¹¹ cm⁻² in the sample w/o NO. In contrast, the nitrided samples show an order-of-magnitude increase, indicating that electron traps are reduced by the nitridation process. Next, examining the effect of stress (2000 s), the samples w/o NO or with relatively short nitridation times (i.e., NO30 and NO60) show a significant decrease in n_{free} under

stress, whereas sample NO120 exhibits only negligible degradation. Consequently, the trend is opposite to that inferred from the SS evaluation of the MOSFET (Fig. 3). Note that because the devices were heated to 300°C during stress application and then cooled down to room temperature before the Hall measurements were performed, the observed behavior appears to reflect effects that persist over long timescales rather than short-term relaxation occurring immediately after stress interruption.

Now, let us turn to the effect of stress on μ_{Hall} , which reflects the free electron mobility. Figures 5(a)–(d) show the μ_{Hall} as a function of n_{free} for each sample condition at room temperature. The data before and after the 2000 s stress are shown in each figure. While measurements on μ_{Hall} were carried out for n_{free} below 10^{11} cm^{-2} , the corresponding data are not shown because noise becomes dominant in that regime. The value of μ_{Hall} before stress application was approximately $70 - 80 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for all sample conditions and showed little variation. When comparing the mobility before and after stress, no significant degradation was observed in the samples w/o NO and NO30, whereas a clear degradation appeared in the samples nitrided for more than 60 minutes (i.e., NO60 and NO120). To quantitatively examine this trend, Fig. 6 summarizes the change in μ_{Hall} before and after stress as a function of NO annealing time, evaluated at $n_{\text{free}} = 10^{11} \text{ cm}^{-2}$. The stress-induced degradation becomes more pronounced as the nitridation proceeds. This indicates that the traps which formed under stress and caused the μ_{Hall} degradation originate from nitrogen atoms at the interface. The degradation is particularly pronounced when n_{free} is relatively low, while the μ_{Hall} measured after stress increases with n_{free} (Fig. 5). This behavior corresponds to the typical Coulomb-scattering trend^{8,34}, where increasing n_{free} enhances carrier screening and thereby leads to higher mobility. Since the stress-induced traps that increased with nitridation are detected as SS degradation (Fig. 3), the traps responsible for the SS degradation likely acted as Coulomb-scattering centers.

Here, we will proceed with a more detailed examination focusing on the energy levels of interface states. Figures 7(a)–(d) summarize the D_{it} distributions evaluated from the MOS Hall-effect measurements and from the room-temperature SS values of MOS Hall bars for each sample condition. In the case of the MOS Hall-effect measurement, the energy level at which D_{it} is monitored can be directly obtained from n_{free} , which corresponds to the surface Fermi level⁵. D_{it} was obtained by subtracting n_{free} from the total electron density determined from the split $C-V$ measurements. An evaluation based on the SS requires the free carrier mobility in the subthreshold region to determine the energy level of interface states⁴. Here, although the mobility generally depends on the current (or n_{free}) range used for extraction, we assume that the free-carrier mobility is equal to the Hall mobility evaluated at $n_{\text{free}} = 10^{11} \text{ cm}^{-2}$ for each sample condition. Based on this assumption, D_{it} at different energy levels was determined by varying the current range used for the SS evaluation from $I_D \cdot L/W = 10^{-12} - 10^{-11} \text{ A}$ to $10^{-9} - 10^{-8} \text{ A}$. Focusing on D_{it} in the shallow-energy region determined from the MOS Hall-effect measurement, the figures show that the sample w/o NO exhibited a high initial D_{it} and an even larger increase than those of the nitrided samples under stress. In contrast, the sufficiently

1 nitrided sample NO120 had a smaller initial D_{it} that exhibited a negligible stress-induced increase.
 2 Next, focusing on D_{it} in the deeper energy region determined from the SS , the sample w/o NO had a
 3 high initial value but exhibited almost no increase under stress, whereas the sample NO120 had a
 4 smaller initial value but a pronounced stress-induced increase. Thus, the shallow and deep energy
 5 regions exhibited clearly different trends.

6 A brief consideration is given to the origin of the scattering centers that are characteristic of the
 7 nitrided samples. Although stress-induced deeper-energy states have a lower density than shallow
 8 ones, they seem to function as strong Coulomb scattering centers. This suggests that the scatterers
 9 are generated on the SiC side of the interface, where channel electrons are localized, thereby exerting
 10 a stronger influence. This interpretation is further supported by MOS Hall-effect measurements
 11 performed under substrate-biased conditions, in which the average distance of electrons from the
 12 interface was varied³¹. The results of the present study strongly suggest that the stress-induced
 13 deeper-energy states originate from nitrogen atoms. Considering the previous XPS results^{21,35} and
 14 the fact that the extremely fast-responding traps are generated by NO annealing³⁶, it is highly likely
 15 that nitrogen is introduced on the SiC side of the interface during the nitridation process. Past
 16 theoretical studies have also investigated incorporation of nitrogen at the SiC surface due to
 17 nitridation³⁷⁻³⁹. Although the amount of nitrogen incorporated at the SiO₂/SiC interface during
 18 nitridation is typically on the order of 10^{14} cm^{-2} ³⁶, the density of stress-induced defects observed in
 19 this study is considerably smaller (Fig. 7). This suggests that, when strong voltage stress is applied
 20 at high temperature, a subset of the incorporated nitrogen-related defects undergo bond-breaking
 21 reactions, exposing dangling bonds that behave as electrically active traps.

23 IV. SUMMARY

24 We investigated traps generated in SiC MOS structures under gate bias stress and clarified that the
 25 trap-generation trends differ between the shallow and deep energy regions. (The key findings in this
 26 study are summarized in the SiO₂/SiC band diagram shown in Fig. 8.) The shallow-energy D_{it}
 27 increased under stress in the non-nitrided or short-time nitrided samples, whereas this increase was
 28 effectively suppressed in a sufficiently nitrided sample. Although the defects in this energy region
 29 had a large impact on n_{free} due to their high density, their influence on μ_{Hall} was minor. In contrast,
 30 for nitrided samples, D_{it} in the deeper energy region increased under stress, which had a limited
 31 impact on n_{free} because the density was comparably low, whereas it had a severe effect on μ_{Hall} by the
 32 corresponding defects acting as Coulomb scattering centers. Considering their impact on μ_{Hall} , it is
 33 presumed that the stress-induced interface states in the shallow energy region are located at the
 34 interface, whereas those in the deeper-energy region reside in SiC near the interface, closer to where
 35 the channel electrons are present. Because μ_{FE} , a key performance metric of MOSFETs, is influenced
 36 by both the carrier density and scattering, it inevitably deteriorates under stress regardless of the
 37 nitridation condition. Taken together, these results clarify that the impact of traps, whether acting as

1 carrier traps or scattering centers, depends strongly on their energy levels and location.

2

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6

7 **AUTHOR DECLARATIONS**

8 **Conflict of Interest**

9 The authors have no conflicts to disclose.

10

11 **DATA AVAILABILITY**

12 Data that support the findings of this study are available from the corresponding authors upon
13 reasonable request.

This is the author's peer reviewed, accepted manuscript. However, the online version of record will be different from this version once it has been copyedited and typeset.
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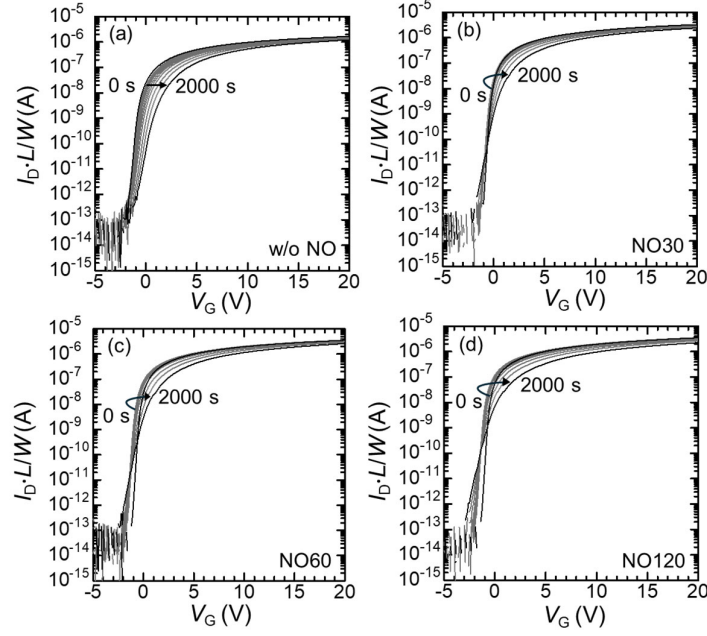


Fig. 1. Normalized drain current–gate voltage (I_D – V_G) characteristics measured at 300°C for SiC MOSFETs: (a) w/o NO, (b) NO30, (c) NO60, and (d) NO120. Time labels shown in figures represent duration of applied stress.

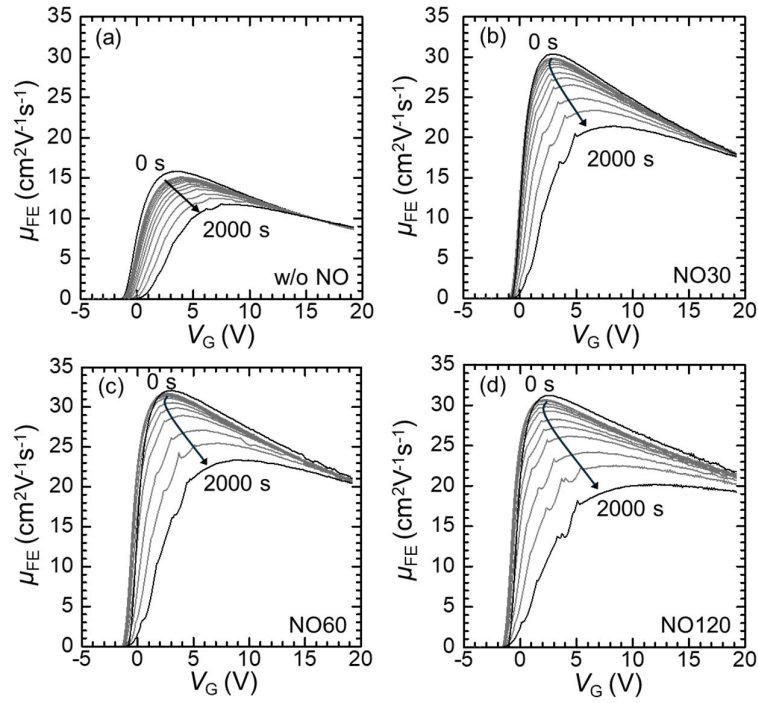


Fig. 2. Field-effect mobility (μ_{FE}) as a function of gate voltage (V_G) evaluated at 300°C for SiC MOSFETs: (a) w/o NO, (b) NO30, (c) NO60, and (d) NO120. Time labels shown in figures represent duration of applied stress.

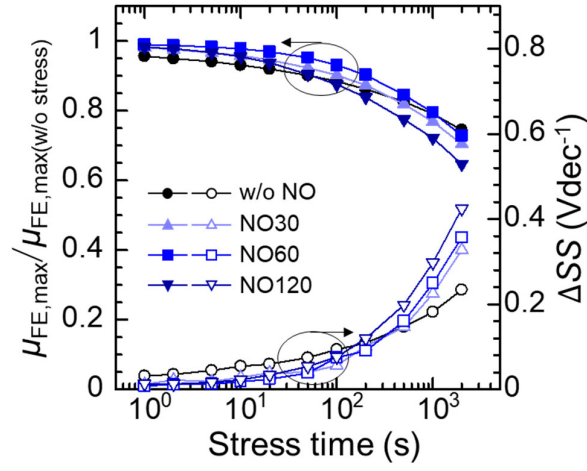


Fig. 3. Ratio of the maximum field-effect mobility (μ_{FE}) to no-stress value, and change in subthreshold swing (SS) as a function of stress time.

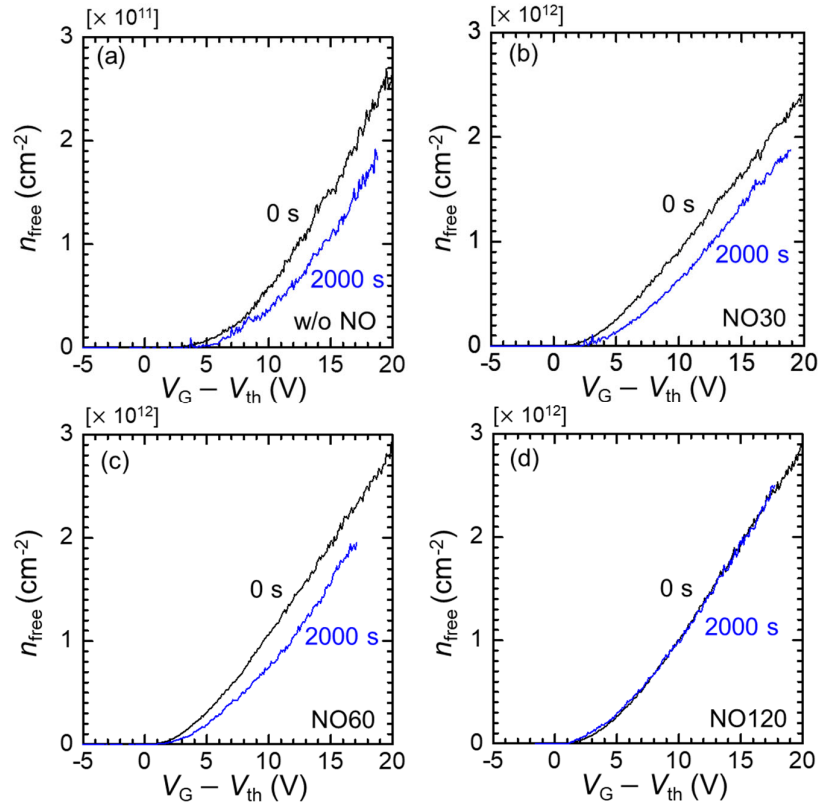


Fig. 4. Free electron density (n_{free}) as a function of overdrive voltage ($V_G - V_{th}$) evaluated from MOS Hall-effect measurements performed at room temperature: (a) w/o NO, (b) NO30, (c) NO60, and (d) NO120. The vertical axis in (a) is on the order of 10^{11} cm^{-2} , while the remaining panels use a 10^{12} cm^{-2} scale. Time labels shown in figures represent duration of applied stress.

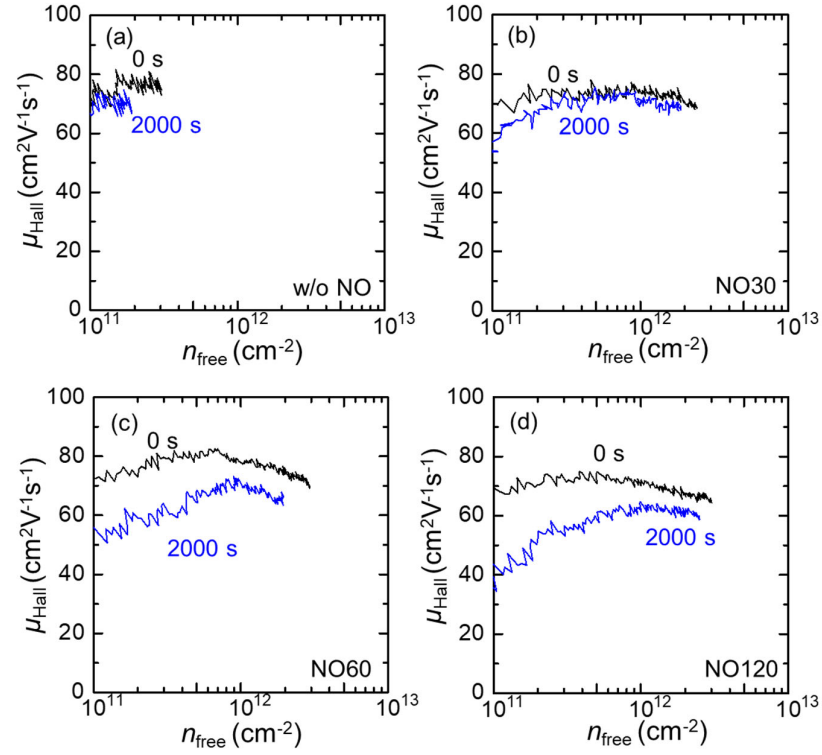


Fig. 5. Hall mobility (μ_{Hall}) as a function of free electron density (n_{free}) evaluated from MOS Hall-effect measurements at room temperature: (a) w/o NO, (b) NO30, (c) NO60, and (d) NO120. Time labels shown in figures represent duration of applied stress.

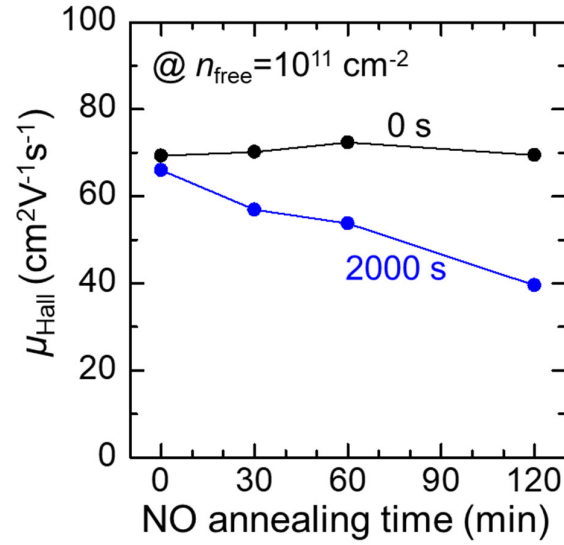


Fig. 6. Change in Hall mobility (μ_{Hall}) before and after stress as a function of NO annealing time. Time labels shown in figure represent duration of applied stress.

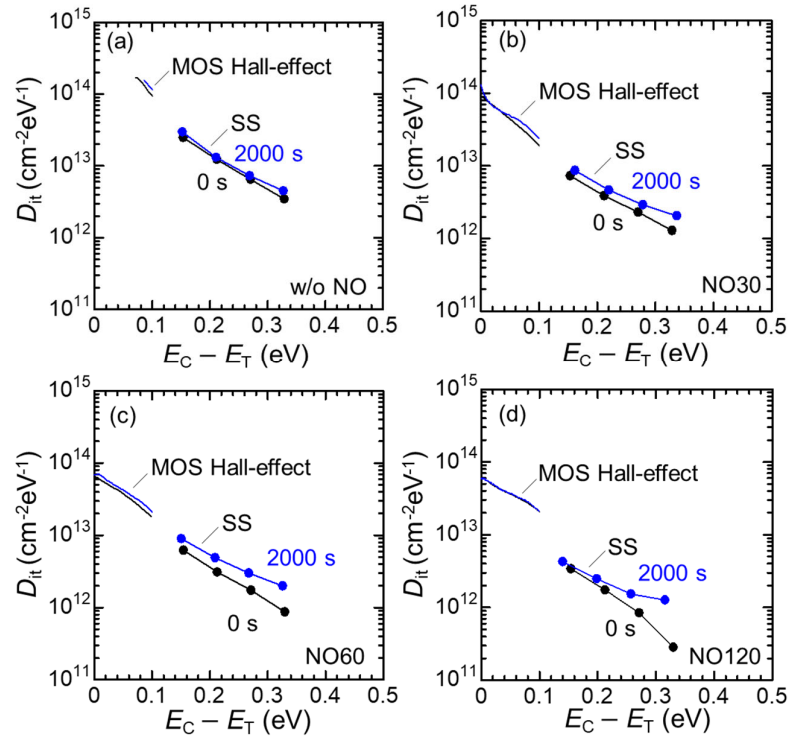


Fig. 7. Energy distribution of interface state density (D_{it}) evaluated from MOS Hall-effect measurements and from room-temperature subthreshold swing (SS) of MOS Hall bars: (a) w/o NO, (b) NO30, (c) NO60, and (d) NO120. Solid lines represent the D_{it} values determined from MOS Hall-effect measurements, whereas symbols connected lines represent the D_{it} values obtained from SS. Time labels shown in figures represent duration of applied stress.

Stress-induced interface traps

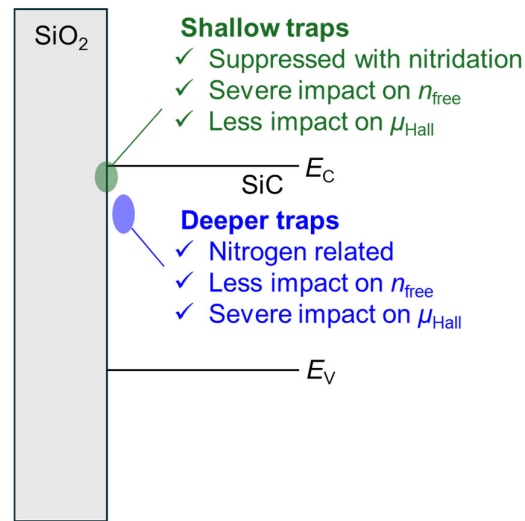


Fig. 8. Schematic band diagram of SiO_2/SiC structure summarizing key findings in this study.

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