WP 22.5 DS-CDMA Wired Bus with Simple Interconnection Topology for Parallel Processing System LSIs

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A new bus architecture is suitable for a parallel processing system without complexity of interconnection, and also drastically reduces the I/O pin count, which is highly desirable for future gigascale integrated systems. The architecture is based on the direct sequence code division multiple access (DS-CDMA) technique[1].

Unlike the DS-CDMA radio system, the DS-CDMA system uses wired buses as a communication medium and does not require upconversion to radio frequencies. The circuitry of DS-CDMA wired bus technique is shown in Figure 22.5.1. The local clock is distributed to all transmitter and receiver circuits to synchronously generate the PN codes. The interfaces use a differential signal as the modulated signal to help common-mode noise rejection. This architecture provides noise tolerance even for white noise on the bus, which is a key feature of the DS-CDMA technique.

The original digital signals, PN codes and modulated signals in Figure 22.5.2 are shown as examples. The DS-CDMA modulates the input bit data with the polarity of the PN code. Due to the random nature and high frequency of the PN code, the modulated data spectrum has a wider bandwidth than the original signal. One benefit to spreading the signal in the frequency domain is that a signal with a wider bandwidth is less susceptible to degradation from narrow-band noise. Another feature is the rejection of interfering signals by demodulation in the receiver. This enables multiple access with different PN codes, because each of them has a high correlation with itself and low correlation with the others. Therefore, assignment of the same PN code for the transmitter and the receivers corresponds to a virtual direct connection of their digital data streams. These connections do not require numerous interconnections, but they are flexible even during system operation. In addition, although the signal on the bus looks like analog with discrete voltage steps, the input of the transmitter and the output of the receiver are conventional digital signals, indicating compatibility with a conventional digital bus.

This system uses the M-sequence as the PN code, because it can be easily generated with a linear feedback shift register (LFSR)[2]. The M-sequence output synchronizes with a local clock which has the same frequency as the chip rate ($1/T_C$ in Figure 22.5.2). Therefore, using the local clock, the PN codes of the transmitters and receivers can match timing. This is useful for implementing the architecture with simple circuitry without code acquisition and tracking, which are important issues in CDMA cellular phone systems.

In the transmitter, the charge pump circuit injects positive or negative charge on the buses, as shown in Figure 22.5.3.The receiver circuit has a CMOS double-balanced mixer to demodulate the signal on the bus by PN code. The low-pass filter (LPF) in this receiver integrates the demodulated signal for about a bit cycle (T in Figure 22.5.2). If there are no transmitted signals on the bus which are modulated by the same PN code as the receiver, the output of the LPF stays in a limited range, because the mixer does not detect much correlation. The level detector of the receiver judges the transmitted bit data from the LPF output. As seen in Figure 22.5.4, it has two inverters which have logic threshold voltages of 1V and 2V, respectively. The "Valid" signal indicates whether data is being sent with the respective code. The output of this circuit changes at the last chip interval of the PN code because it comes from the integration of the demodulated signal. Therefore, the data transmission has time delay T.

The receiver has to wait for at most the bit interval to judge the received digital data. However, these interfaces can transfer multiple digital data streams concurrently, resulting in comparable data throughput. In addition, the architecture reduces power dissipation of the buses, because the voltage amplitude of the modulated signal for each transmitter can be small due to the noise tolerance. The multiplexed signal on the buses are between ground and the supply voltage. This bus architecture also has excellent dynamic flexibility, so that the architecture is suitable for parallel processing systems.

A longer PN code can realize more interconnectivity in the system, although the data transfer speed becomes slower than that for one-to-one communication. In the design, 63- and a 127-length PN codes are used (N in Figure 22.5.2). Figure 22.5.5 shows simulation results of whole circuit operation for two-to-two communication. Both the chip interval and the period of the local clock are 5ns. The operation period is 640ns consisting of 635ns bit data interval and 5ns reset period. These results show that the bus interface can transmit and receive digital data accurately with a small voltage step.

Acknowledgments:
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References:
[1] Yang, S. C., "CDMA RF System Engineering", ARTECH HOUSE INC., 1998.
[2] Sarwate, D. V. and M. B. Pursley, "Crosscorrelation properties of pseudorandum and related sequences", Proc. IEEE, 68, 5, pp.593-619, 1980.

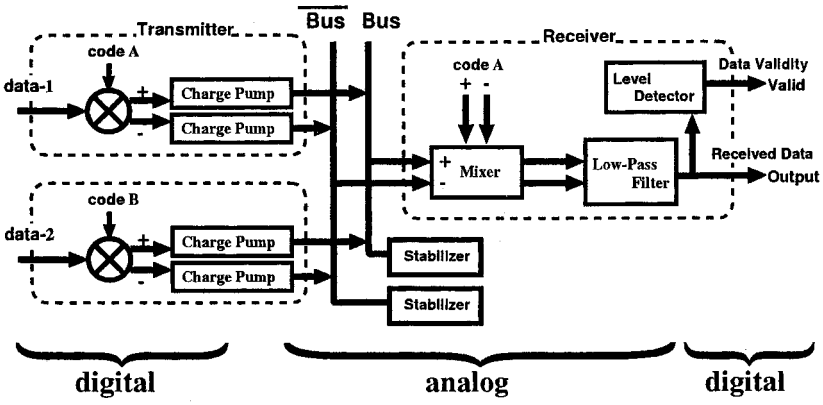

Figure 22.5.1: Interface block diagram.

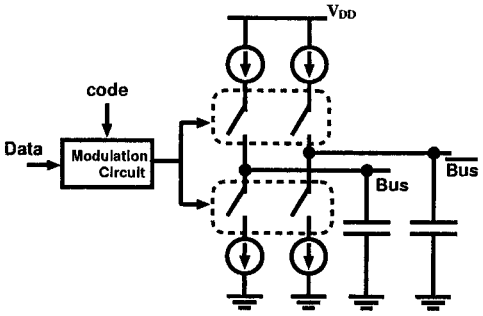

Figure 22.5.3: Charge pump circuit at transmitter. Input data given by digital logic.

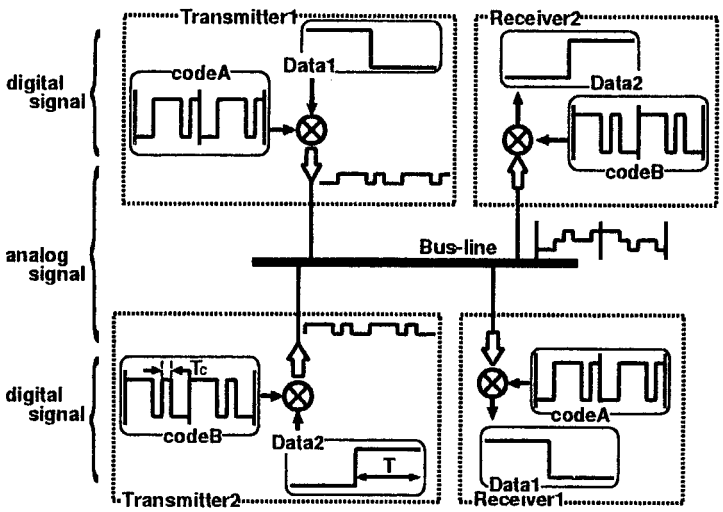

Figure 22.5.2: Basic schematic of DS-CDMA wired bus I/O interface and conceptual data signal at each point. T_C=T/N, N is length of PN code.

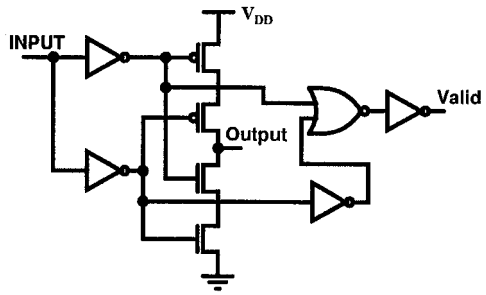

Figure 22.5.4: Level detector circuit. When voltage at INPUT stays in 1.5 ±0.5V range, Valid becomes 0, otherwise 1. Valid signal indicates whether it received a bit data.

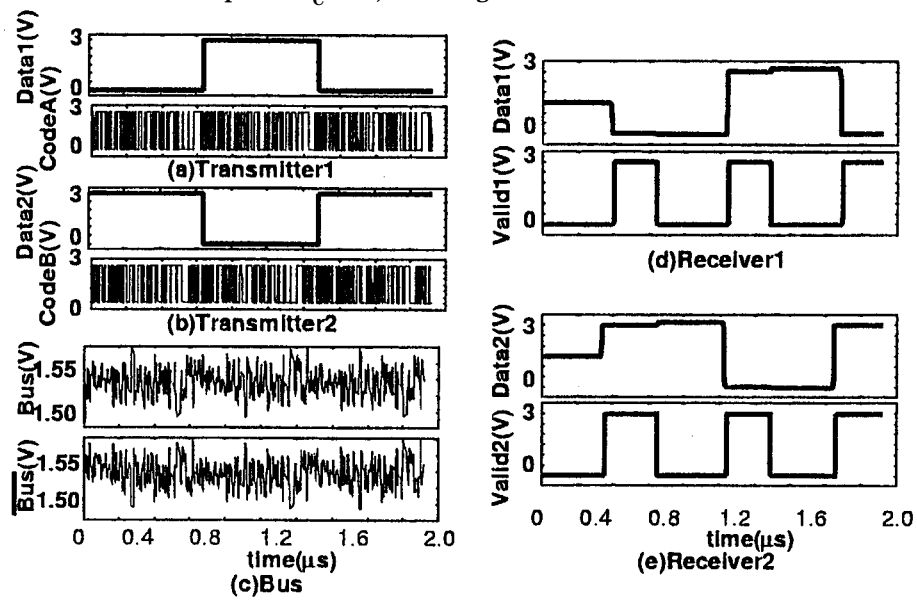

Figure 22.5.5: Simulation results of entire circuit for two-to-two communication. Figures show input data and PN code in transmitters (a) 1 and (b) 2, (c) signals on differential bus, and output data and valid signals in receivers (d) 1 and (e) 2.