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A New Analytical Inductance Extraction Technique of On-wafer Spiral Inductors

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Abstract - We derive a novel scalable self-inductance expression of interconnects connected to spiral inductors. With the use of the expression, intrinsic inductance of spiral inductors can be extracted from measured results without any special fixtures. The accuracy of proposed expression is proved by an electromagnetic simulator. In the comparison with the field solver, our calculated inductances match simulated results within 1.4%.

1. INTRODUCTION

On-chip planar spiral inductors are essential passive components in radio-frequency integrated circuits (RF IC's) [1]-[3]. The accurate extraction techniques of inductance from on-wafer measurements are highly required for circuit design and inductor modeling [4]-[6] because inductance is one of the most important physical quantity in RF IC's. One widely used on-wafer measurement calibration method is the open pad de-embedding technique (OPD) [7]. The technique does not, however, provide intrinsic measured inductance because interconnects between pads and device under test (DUT), are not well calibrated. The accurate extraction of inductance requires more precise calibration technique [7] regardless of its complication.

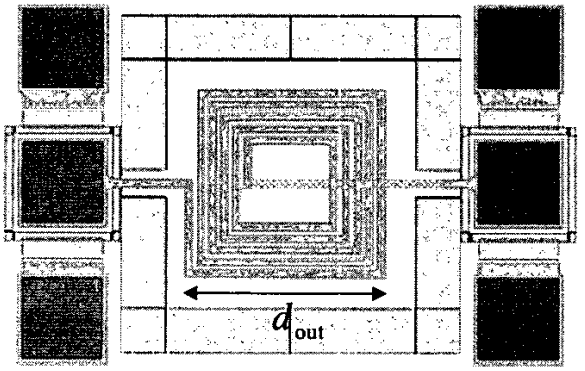
The aim of this paper is to propose a new and simple de-embedding method to extract intrinsic inductance of planar spiral inductors from their measured results. The method consists of two step processes. First, effective inductance including the effect of extended interconnects is extracted from measurements by using a conventional equivalent circuit. Second, the interconnects effect is de-embedded from the measured inductance using proposed analytical inductance formula. The analytical technique presented is quite useful and practical for extracting inductance from measurements without the use of any special measurement fixture.

2. DESIGN CONSIDERATIONS OF TEST STRUCTURE

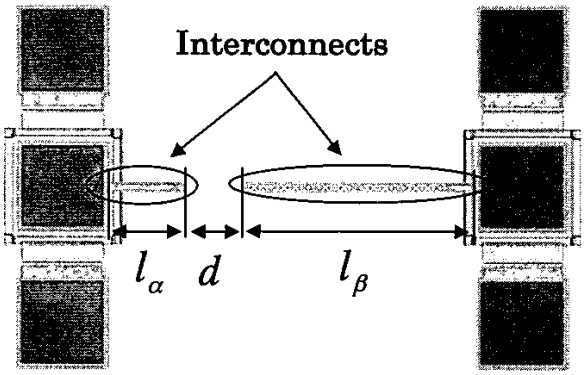
To extract accurate intrinsic inductance of spirals from measurement, special attention has to be paid to the layout of test structures to reduce magnetic interaction between a spiral and extended interconnects. The layout with reduced interaction allows us to analyze the components separately so that the excess inductance due to the interconnects can be simply subtracted from measured results.

Figure 1(a) show the layout to reduce the magnetic coupling for accurate de-embedding: the symmetric center-tapped inductor yields very weak magnetic coupling between the spiral and the extended interconnects (see Figure 1(b)). In this configuration, inductance extraction of the spiral can be achieved through the calculation of the self-inductance of the extended interconnects.

0-7803-8262-5/04/$17.00©2004 IEEE 04CH37516



(a)



(b)

Fig. 1. (a) A layout of center tapped square spiral inductor with measurement fixture. The outer diameter is d_{out}. (b) The measurement fixture, composed of pads and interconnects, used in Fig. 1(a) with geometric parameters of interconnects, two lengths and a gap of "d".

3. Self-Inductance Expression of Interconnects

We present a scalable analytical inductance formula of interconnects. Self-inductance expression of a wire with rectangular cross section [8],[9] is employed to derive the inductance formula, which is given by

$$L_{wire} = \frac{\mu_0 l}{2\pi}\left(\log\frac{2l}{GMD} - 1\right) \qquad (1)$$

where μ_0 is the magnetic permeability, l the length, and the GMD geometric mean distance of the rectangle. The GMD is given by

$$GMD = 0.223(w+t) \qquad (2)$$

where w is the width, t the thickness of the wire.

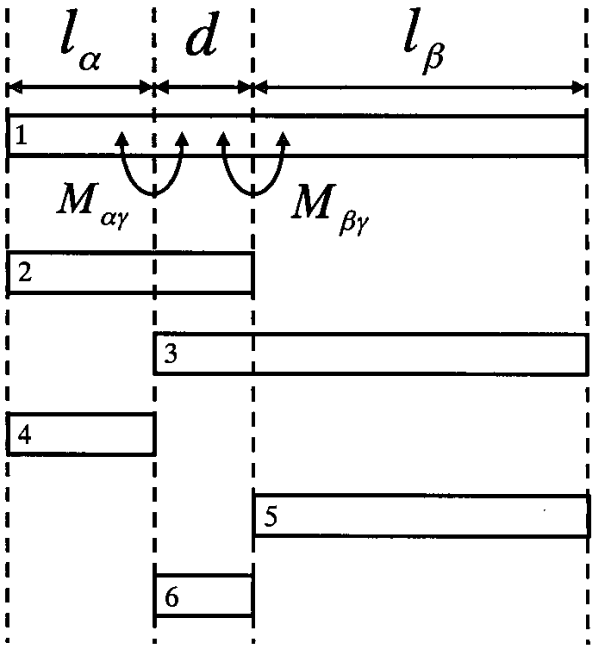


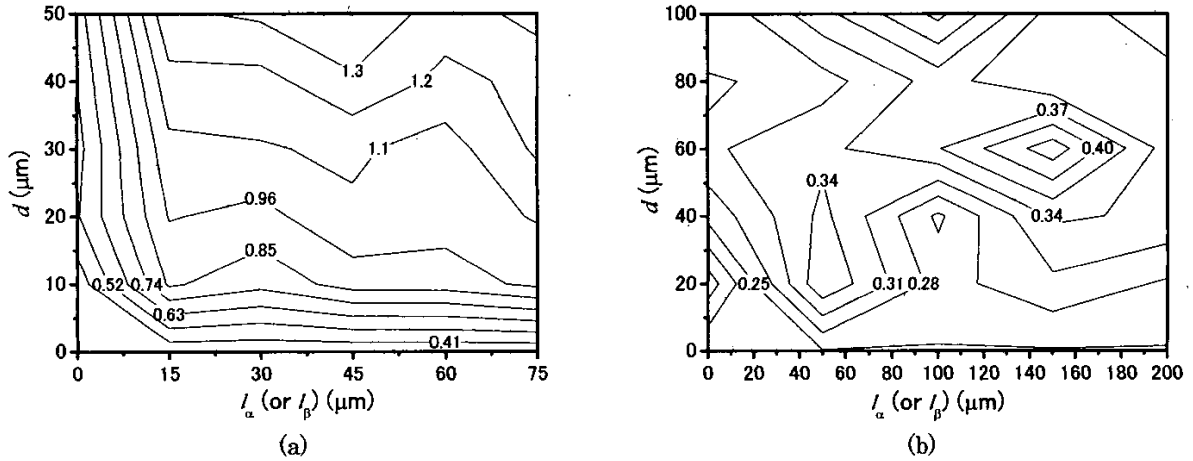
Fig. 2. Concept to derive self-inductance of interconnects composed of the single wires numbered from 1 to 6. An analytical expression of the self-inductance can be derived from a combination of the inductances described in the text.

Figure 2 denotes the concept of our technique to derive the self-inductance formula using equation (1). A special combination of the numbered single wires from 1 to 6 yields the expression as described below. The complete self-inductance, L, of interconnects can be obtained by

$$L = L_1 - \left(L_6 + M_{\alpha\gamma} + M_{\beta\gamma}\right) \qquad (3)$$

where

$$M_{\alpha\gamma} = L_2 - (L_4 + L_6) \qquad (4)$$



(a) (b)

Fig.3. Contours of error distribution in percentage. (a) $l_\alpha + l_\beta + d = 200\,\mu\text{m}$ and (b) $l_\alpha + l_\beta + d = 500\,\mu\text{m}$. The width w is $10\,\mu\text{m}$ and thickness t $1\,\mu\text{m}$ for both cases.

$$M_{\beta\gamma} = L_3 - (L_5 + L_6) \tag{5}$$

where L_i $(i = 1,2,\cdots,6)$ is self-inductance of the wire numbered i, $M_{\alpha\gamma}$ and $M_{\beta\gamma}$ mutual inductances as shown in Figure 2. Hence, the self-inductance L is

$$\begin{aligned} L = {} & \frac{\mu_0 l_\alpha}{2\pi}\left[\log\left\{\frac{2l_\alpha(l_\alpha + l_\beta + d)}{l_\alpha + d}\cdot\frac{1}{GMD}\right\} - 1\right] \\ & + \frac{\mu_0 l_\beta}{2\pi}\left[\log\left\{\frac{2l_\beta(l_\alpha + l_\beta + d)}{l_\beta + d}\cdot\frac{1}{GMD}\right\} - 1\right] \\ & + \frac{\mu_0 d}{2\pi}\log\left\{\frac{d(l_\alpha + l_\beta + d)}{(l_\alpha + d)(l_\beta + d)}\right\} \end{aligned} \tag{6}$$

where d is the gap between extended interconnects. It should be noted here that equation (6) is general self-inductance form of separated wires with the gap of d. This fully scalable equation has also geometric parameters including thickness of interconnects.

Figures 3(a) and (b) show the accuracy of our expression by comparing the results of our expression (L_{calc}) and those derived from a field solver (L_{sim}), Ansoft Q3D Extractor [10]. The contour plots show an absolute percentage error defined by $100\left|L_{\text{calc}} - L_{\text{sim}}\right| / L_{\text{sim}}$, while the x and y axes indicate the length of one of the wires and the gap respectively. These Figures show that the maximum error is less than 1.4%. Generally speaking, the overall length $l_\alpha + l_\beta + d$ in Figure 3(a) is minimum distance between pads used for measurement fixtures of spirals. This confirms the validity of our proposed formula which extracts accurate inductance of interconnects in test fixtures.

4. RESULTUS AND DISCUSSION

The new technique is applied to a set of spirals listed in Table I. We use a conventional spiral inductor model [11] to extract the effective inductance from measurements. The measured planar spiral inductors have been fabricated on both 0.20-μm SOI-CMOS and 0.35-μm CMOS processes. The metal thickness of SOI-CMOS process is thicker than the bulk process.

Table I. The layout parameters of inductors. n is the number of turn, d_{out} the outer diameter, w the metal width, s the turn spacing, l_α and l_β length of each interconnect, and d the gap between the interconnects. The inductors numbered 1-3, 7 and 11 have thicker metal.

Inductor #	n	$d_{out}[\mu m]$	$w[\mu m]$	$s[\mu m]$	$l_\alpha[\mu m]$	$l_\beta[\mu m]$	$d[\mu m]$
1	1	119	10	3	137	246	23
2	2	145	10	3	124	246	36
3	3	171	10	3	111	246	49
4	3	159.5	8.5	1	122.15	254.15	37
5	4	215.25	14.25	1	91.4	246.65	75.25
6	4	217	9	8	89.65	246.65	77
7	4	197	10	3	98	246	62
8	4	218.75	3.75	15	87.9	246.65	78.75
9	4	210.25	9.25	1	96.4	266.65	50.25
10	5	211.6	10.6	1	95.05	249.65	68.6
11	5	223	10	3	85	246	75
12	5	204.6	3.6	1	102.05	284.65	26.6

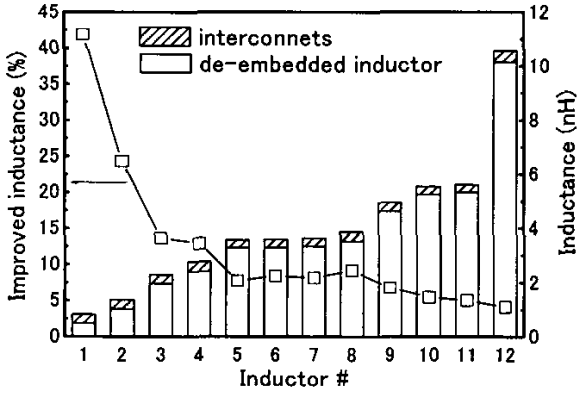


Fig.4. Improvement of measured results with our de-embedding technique. The open squares with solid line show the percentage of improved inductance, while the bar graphs indicate the measured inductance. The shaded regions are inductance due to interconnects.

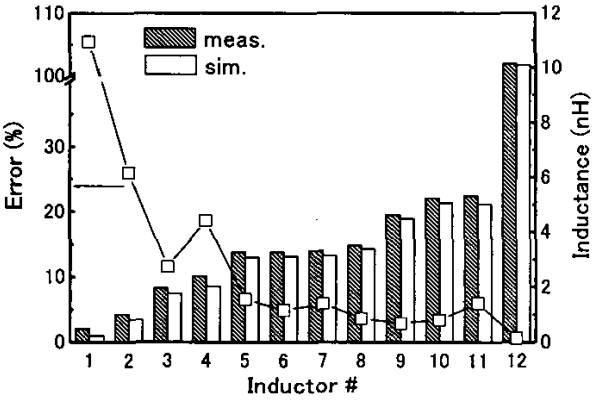


Fig.5. Comparison between extracted measured inductance and simulated one. The open squares with solid line are the error percentage from the simulated values, while the bar graphs show the inductances both measured and simulated results.

Figure 4 depicted the improvement of measured results using our expression. The vertical axis is defined by $100|L_{\text{no cal}} - L_{\text{cal}}|/L_{\text{no cal}}$, where $L_{\text{no cal}}$ is measured inductance of spirals without the de-embedding while L_{cal} the extracted intrinsic inductance from measurement. We find the technique significantly improve the measured results, particularly, in smaller inductance. This is due to the longer interconnect length because of the small inductor, when the size of test fixtures is constant for all inductors. Such small inductors are key components for state-of-the-art RF circuits in GHz bands. Therefore, de-embedding interconnects is fairly important to estimate the inductance of such inductors.

Figure 5 shows the comparison between the extracted inductances and the simulated results of spirals. The vertical axis, absolute percentage error level, is defined by $100|L_{\text{cal}} - L_{\text{sim}}|/L_{\text{sim}}$, where L_{sim} is the inductance calculated with the field

solver. The open squares show that the percentage error of inductors over 2nH are typically around 3−7%. These results would be acceptable, while the other results exceeding 10% are not good enough. However, the inductance error would originate from parameters extracted from inductor model and measurement system, as explained in [12]. Especially, for small inductance, the additive inherent inductances result in large relative error. The de-embedding technique is still useful except for such small inductors in spite of the existence of the additive inductances. Obviously, optimum choice of the model and good calibration of measurement system lead to further reduction of the error so that the de-embedding results will be acceptable in such cases.

5. CONCLUSION

We proposed a scalable expression of lead lines inductance for de-embedding inductors from test structures. The de-embedding technique requires no special fixtures by virtue of using the expression. The inductance of interconnects predicted with our formula matches that derived from the field solver, Ansoft Q3D Extractor, within 1.4% error in the conditions presented. With the use of the symmetric layout of inductor to reduce the magnetic coupling, the measured inductances calibrated are in good agreement with simulated results typically around 3−7%. The accuracy and simplicity of the technique offer practical usefulness to extract intrinsic inductance of spirals from test fixtures.

ACKNOWLEDGMENTS

This work was supported by Japan Society for the Promotion Science (JSPS) Research for the Future Program, and by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc.

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