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Test Structure for Precise Statistical Characteristics Measurement of MOSFETs

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ABSTRACT

A new test structure consisting of an MOSFET array and peripheral decoder circuits is proposed to study statistical variation (mismatch) in MOSFETs' characteristics. Kelvin technique was implemented in the structure to cancel parasitic resistance of metal wiring and transmission gates in such a way that any MOSFET in the array can be measured at the same bias condition. Accurate electrical measurements using the structure makes it possible to derive statistical variation of threshold voltage and transconductance of MOSFETs placed in small area.

INTRODUCTION

MOSFETs have statistical variation in device parameters such as threshold voltage (V_{th}) and transconductance (g_m)[1]. Therefore, the information of MOSFET matching for specific fabrication processes is highly required for analog circuit design because mismatch in device characteristics significantly affects the performance of MOSFET circuits, especially for high precision analog circuits. Matching evaluation requires statistical measurements using a large number of MOSFETs placed in short distance. However, a large number of MOSFETs together with measurement pads generally occupies large area. Note that both pad size and pad interval are not scaled with down-scaling because of the finite size of probing devices. For example, a 4mm×4mm chip with pad area of $100\mu m \times 100\mu m$ and pad interval of $150\mu m$ accommodates only 200 MOSFETs, which is not sufficient for statistical measurement.

MOSFET array structure with a decoder to select one of gate lines has been proposed to measure threshold voltage variation [2], in which the number of gate pads is significantly reduced but there still remains a large number of drain pads.

In order to further reduce the number of pads, we propose a new test structure for statistical measurement of MOSFET matching in which a decoder to select a drain line as well as a gate decoder is introduced. This drastically reduces the occupation area of an MOSFET array by cutting the number of drain pads. Key feature of the test structure is the use of Kelvin technique to avoid voltage drop in parasitic wiring and transmission gate resistance.

The test structure allows to derive statistics on MOSFET's parameters such as, V_{th} and g_m, by using an analog IC test system which measures all the characteristics of MOSFETs in the array one after another under the same bias condition.
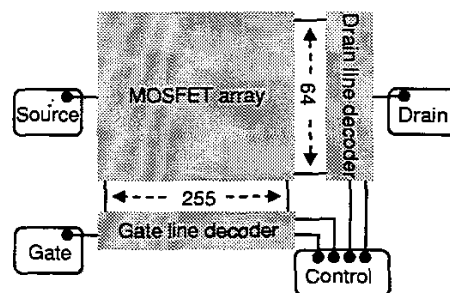

Figure 1: Block diagram of the statistical data acquisition circuit in which an array consisting of MOSFETs is included.
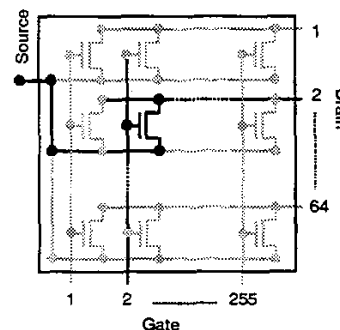

Figure 2: 255 × 64 MOSFETs array. Any one of MOSFETs in the array can be selected from a pair of the drain and gate lines

TEST STRUCTURE

Figure 1 shows the block diagram of the test structure for MOSFET matching measurement, which consists of an MOSFET array, gate and drain line decoders.

In the MOSFET array block shown in Fig.2, MOSFETs are placed at every nodes of a 255 × 64 array and they are connected with a common source line, where a given voltage is applied to the common gate of all the MOSFETs on a row and a given drain voltage to those on a column. Any one of the MOSFETs in the array can be selected with a pair of the gate and drain lines for the measurement at one's discretion. The gate and drain of any MOSFETs in the array are connected to their respective common pads to which external bias voltages are applied.
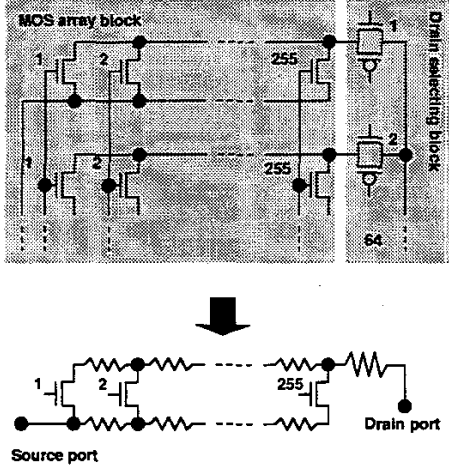
Figure 3: Parasitic resistance in the circuit. Actual source and drain voltages of a selected MOSFET slightly differ from those applied to the pads due to resistance of selector switches and metal wiring.

In the test structure, there are two factors whose parasitic resistance directly affect matching measurement. One is parasitic resistance of a common drain line connected with 255 MOSFETs because of the long connecting line, typically a few mm. The parasitic resistance depends on the location of MOSFETs measured in the array. Another is the resistance of transmission gates in the drain decoder (Figure 3).

Because of the existence of the parasitic resistance, actual drain voltage is lower than that at the external drain pad. Similarly, the source voltage of MOSFETs is higher than the external ground voltage. These parasitic effects cause significant error in mismatch measurement even at the same external bias condition.

For example, the drain current (I_D) in linear region is given by:

$$I_D = \beta[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2] \qquad (1)$$

where V_{DS} is the drain-source voltage, V_{GS} the gate-source voltage and β the current factor. Transconductance g_m, is also given by:

$$g_m = \frac{\delta I_D}{\delta V_{GS}} = \beta V_{DS}. \qquad (2)$$

In (2), g_m at a given V_{GS} directly depends on V_{DS}. Fig. 4(Conventional) shows the measured g_m as a function of the location of the MOSFETs which clearly reflects the effect of the voltage drop in the drain line. Since 255 MOSFETs are connected with a common drain pad through a metal wiring, the distance from the external drain bias pad increases with decreasing the number labeled to MOSFETs (255—1) so the effect of V_{DS}
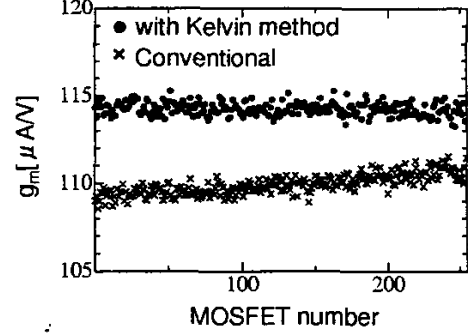

Figure 4: Systematic change of g_m ($\times$) due to parasitic resistance of the drain line connecting with MOSFETs with W/L=10.0μm/0.8μm measured at V_{DS}=0.05V. The systematic change of g_m can be avoided by using Kelvin method($\bullet$).
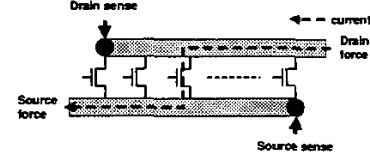

Figure 5: Technique to monitor actual drain and source voltages of a selected MOSFET. Solid circles represent the points where voltages applied to the MOSFET are monitored.

reduction due to wiring resistance is apparent: the measured g_m decreases with the distance from the external drain pad.

To avoid the voltage drop in the drain line, we use Kelvin technique[3] for which drain and source sense points are added at the end of each line as shown in Fig. 5. Drain and source voltages of a selected MOSFET can be accurately monitored through the drain and source sense points because there exists no voltage drop due to no current between the sense points and the drain/source of a selected MOSFET. Thus, any MOSFETs in array can be measured at the same bias condition.

Solid circles in Fig. 4 represent g_m measured by using the Kelvin method, in which there is no systematic g_m degradation due to parasitic resistance.

Figure 6 shows the test structure including transmission gates for the drain sense, source sense and drain force ports for a selected MOSFET. The source force is common for all MOSFETs. Thus, with only a few extra circuits, V_{th} and g_m can be evaluated accurately for all MOSFETs in the array at the same bias condition.

The parasitic resistance in the gate lines does not affect measured $V_{GS} - I_D$ characteristics because no DC current flows through the transmission gate connected with 64 MOSFETs' gate electrodes.
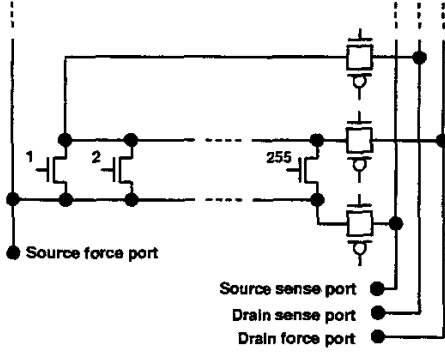
Figure 6: Auxiliary circuit to monitor actual drain and source terminal voltages by using Kelvin technique.
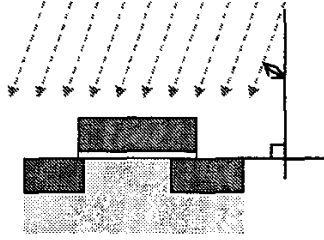

Figure 7: Asymmetric doping profile in the source and drain regions due to tilted angle ion implantation.

LAYOUT OF MOSFET ARRAY

On the physical layout of MOSFETs in the array block, the following phenomenon must be considered.

During doping process, dopant atoms are implanted into silicon substrate with an angle tilted from crystal axes to avoid ion channeling. This results in asymmetric diffusion profiles under gate electrode as show in Fig. 7: the area of drain overlap region differs from that of source so that the exchange of drain and source would end up with different MOSFET characteristics.

To avoid this phenomenon, we placed the MOSFETs in such a way that all the drain currents flow in the same direction as show in Fig. 8.

CALCULATION OF V_{th} AND g_m

LINEAR REGION

Figure 9 shows $V_{GS} - I_D$ characteristics of an MOSFET operating in linear region and g_m is derived from the maximum slope of this curve.

Threshold voltage, V_{th}, is derived from the intersection of the horizontal axis and the straight line with a point where g_m is derived.
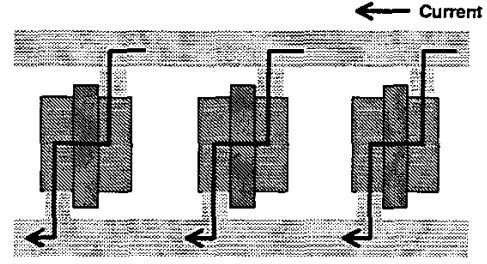

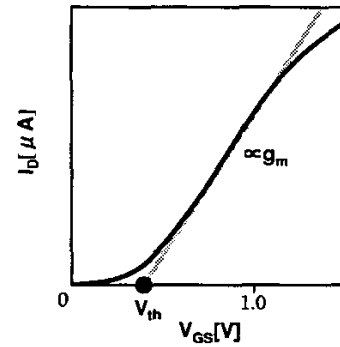Figure 8: Layout of MOSFETs in the array block.

Figure 9: Both V_{th} and g_m are derived using a line extrapolated from data measured in linear region.

SATURATION REGION

The drain current I_D in saturation region is expressed as follows:

$$I_D = \frac{\beta}{2}(V_{GS} - V_{th})^2. \tag{3}$$

A square root of this expression is given by:

$$\sqrt{I_D} = \sqrt{\frac{\beta}{2}}(V_{GS} - Vth). \tag{4}$$

We define V_{th} as the intersection of $\sqrt{I_D} = 0$ line and the tangent line of $V_{GS} - \sqrt{I_D}$ curve at the point where the slope of the curve is maximum.

The transconductance, g_m, is also extracted from the slope of $V_{GS} - \sqrt{I_D}$ curve, which differs from that in saturation region.

$$\frac{\delta\sqrt{I_D}}{\delta V_{GS}} = \sqrt{\frac{\beta}{2}}, \tag{5}$$

while g_m in saturation region is expressed as follows:

$$g_m = \frac{\delta I_D}{\delta V_{GS}} = \beta(V_{GS} - V_{th}). \tag{6}$$

Therefore, using (4), (5) and (6), g_m is given by:

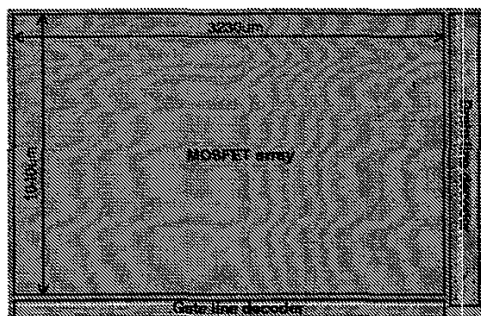$$g_m = 2\sqrt{I_D}\frac{\delta\sqrt{I_D}}{\delta V_{GS}}. \tag{7}$$

Figure 10: Photograph of the fabricated test chip.

The derivation of g_m using (7) is little affected by leakage current on the measurement instrument. The reproducibility of V_{th} and g_m measured was confirmed to be ± 0.1mV and $\pm 0.4\%$ ($=\sigma(g_m)/g_m$, $\sigma(g_m)$ is the standard deviation of g_m), respectively.

MEASUREMENT RESULT

Figure 10 shows a micro-photograph of the proposed test structure. In the array, we placed 16 types of MOS-FETs with different gate sizes and the number of MOS-FETs is 1,020 for each size. MOSFET device parameters such as V_{th} and g_m and their standard deviations are derived from the measured $V_{GS} - I_D$ characteristics of all the MOSFETs in the array. Matching characteristics of the MOSFETs in the array were measured with a mixed signal IC test system (Agilent 94000).

All the measured V_{th} and g_m of 1,020 MOSFETs with W/L=6.0μm/1.0μm are shown in Fig. 11. Both V_{th} and g_m randomly scatter around the average values. This indicates that V_{th} variation arises from a random event. Figure 12 shows the distributions of the measured data, which are well fitted with a Gaussian distribution[2].

Figure 13 shows the standard deviation of V_{th} as a function of the gate area. The slope of -0.51 in the log-log plot indicates that the standard deviation of V_{th} is inversely proportional to the square root of the gate area, meaning that the fluctuation of V_{th} originates from the statistical variation of the number of the channel dopant as reported in Ref. [2].

Figure 14 shows deviations of V_{th} and g_m from their averages for 1,020 MOSFETs with W/L=9.0μm/0.4μm measured at $V_{ds} = 1.00$V. Their distributions are shown in Fig. 15. Figure 16 shows the standard deviation of V_{th} measured at $V_{ds} = 1.00$V as a function of the gate area.

The measurement results shown above demonstrate that the new test structure eliminates the effect of parasitic resistance in wiring and transmission gates and the variation of V_{th} and g_m can be obtained from measurements in saturation as well as in linear regions.

CONCLUSION

We proposed a new test structure to study statistical fluctuation of MOSFETs' characteristics in a chip. This test structure consists of a MOSFET array accommodating a large number of MOSFETs in small area and peripheral decoder circuits to select one of the MOSFETS in the array which significantly reduces the number of the drain and gate pads. The test structure with 64 × 255 MOSFETs subject to measurement are placed in the area of 2mm × 4mm.

The use of Kelvin technique cancels parasitic resistance in wires and transmission gates so that we accurately measure any MOSFETs in the array at the same bias condition. We demonstrated that the new test structure allows one to derive V_{th} and g_m of any MOSFETs in the array and to analyze those variations statistically.

ACKNOWLEDGMENTS

References

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[2] T. Mizuno, J. Okamura and A. Toriumi, "Experimental Study of Threshold Voltage Fluctuation Due to Statistical Variation of Channel Dopant Number in MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, no. 11, 1994.

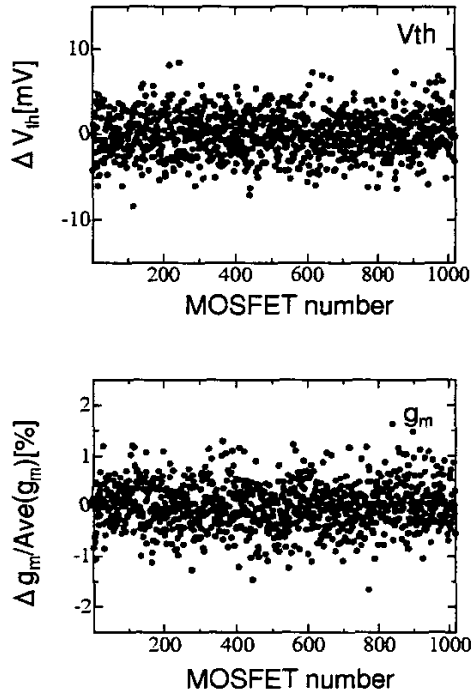[3] A. Hastings, "The Art of Analog Layout" (Prentice Hall, 2001), p.177.

Figure 12: Frequency distribution of V_{th} and g_m show in Fig.11.

Figure 11: Fluctuation of V_{th} and g_m from their averages derived from the data measured in linear region. The measurements were performed for 1,020 MOSFETs with W/L=6.0μm/1.0μm at V_{DS}=0.05V.

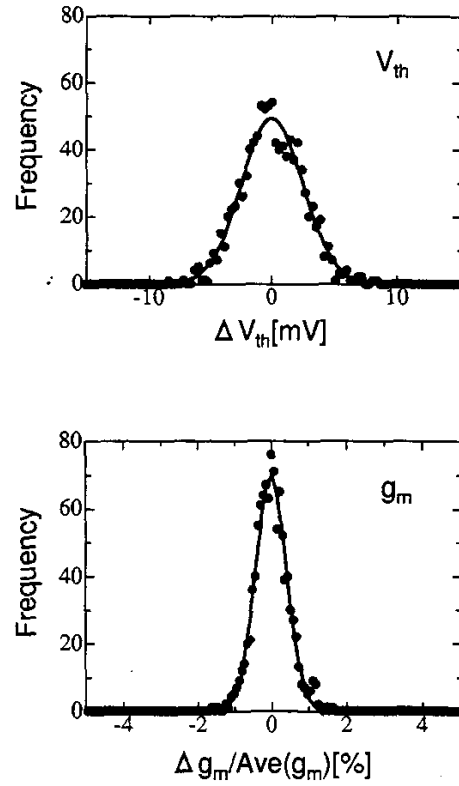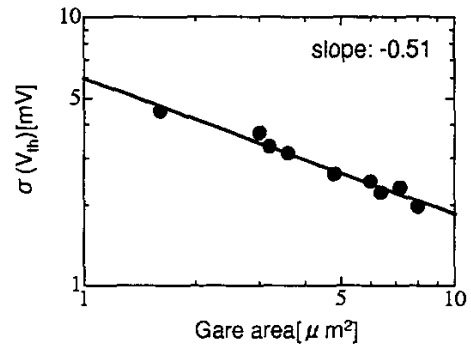Figure 13: Standard deviation of V_{th} as a function of gate area, which were measured in the linear region.
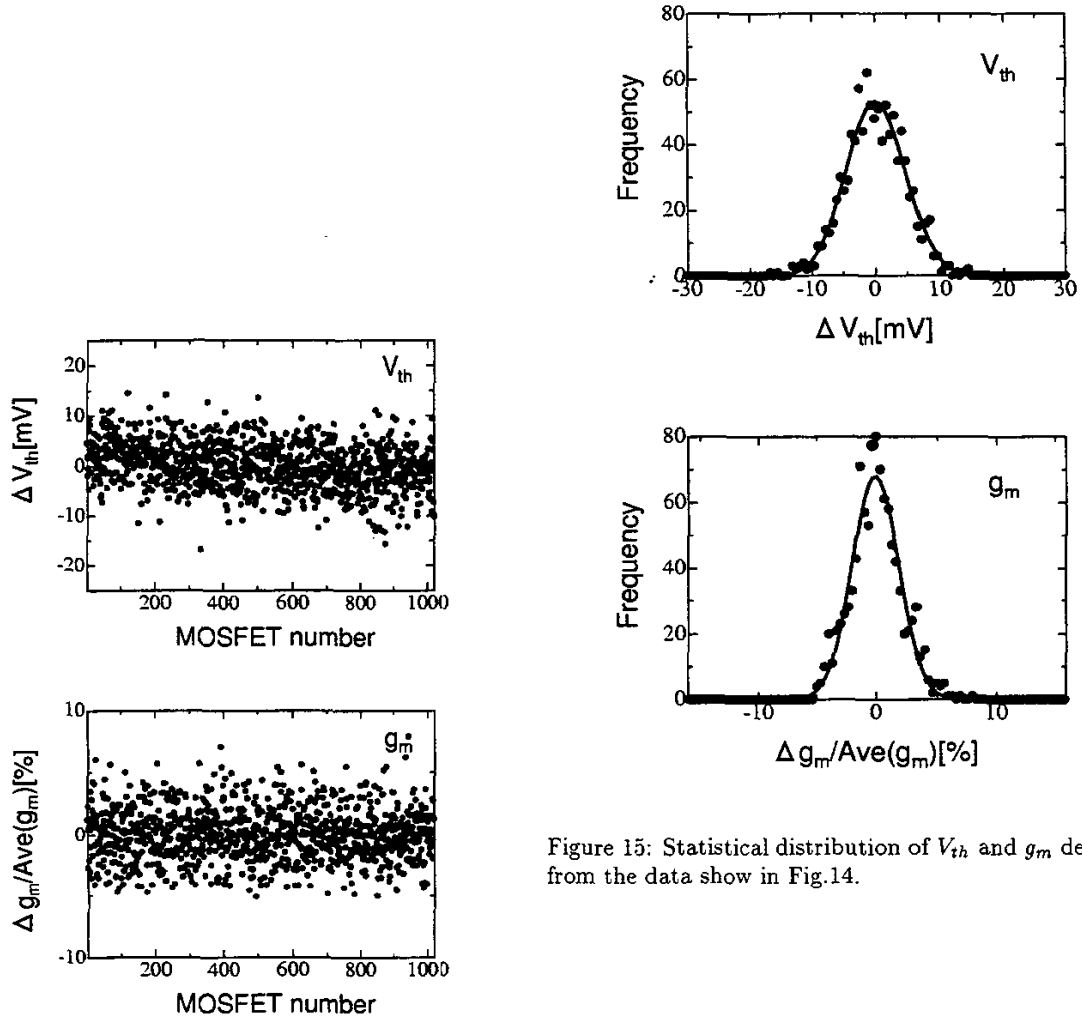
Figure 15: Statistical distribution of V_{th} and g_m derived from the data show in Fig.14.

Figure 14: Fluctuation of V_{th} and g_m in saturation region from their averages. The measurements were performed for 1,020 MOSFETs with W/L=9.0μm/0.4μm at V_{DS}=1.0V.
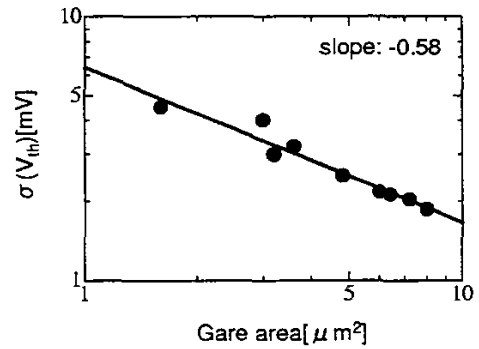

Figure 16: Standard deviation of V_{th} as a function of gate area, by measurement in saturation region.