Ultimate Scaling of High-κ Gate Dielectrics and Impact on Carrier Transport of Field-Effect Transistors

（高誘電率ゲート絶縁膜の薄膜化と電界効果
トランジスタのキャリア輸送への影響）

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2010

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To my parents, wife, and son

Contents

List of Abbreviations

Abbreviation	Description
a-HfO_2	Amorphous HfO_2
AR-XPS	Angle resolved X-ray photoelectron spectroscopy
ALD	Atomic layer deposition
BEOL	Back-end-of-line
C-V	Capacitance-voltage
CPU	Central processing unit
CMP	Chemical mechanical polishing
CVD	Chemical vapor deposition
CMOS	Complementary metal-oxide-semiconductor
CBM	Conduction band minimum
CP	Critical pressure
I-V	Current-voltage
DT	Deep trench
DOS	Density of states
DR	Deposition rate
DC	Direct current
DRAM	Dynamic random access memory
EWF	Effective work function
EELS	Electron energy loss spectroscopy
eDRAM	Embedded dynamic random access memory
EOT	Equivalent oxide thickness
FET	Field-effect-transistor
FGA	Forming gas anneal
HSG	Hemi-Spherical-Grain
HAADF	High angle annular dark field
HF	Hydrofluoric acid
I(F)L	Interfacial layer
ILD	Inter-layer dielectric
ITRS	International Technology Roadmap for Semiconductors
LSI	Large-scale integrated circuit

Abbreviation	Description
MEIS	Medium energy ion scattering
MIPS	Metal inserted poly-Si stack
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
m-HfO_2	Monoclinic-HfO_2
NSG	Non-doped silicate glass
NRA	Nuclear reaction analysis
PVD	Physical vapor deposition
poly-Si	Poly-crystalline Si
PF	Poole-Frenkel
PBTI	Positive bias temperature instability
PMN	Post metal nitridation
PDA	Post deposition anneal
RTA	Rapid thermal annealing
RIE	Reactive ion etching
RHEED	Reflection high-energy electron diffraction
RCS	Remote Coulomb scattering
RPS	Remote phonon scattering
r-SRS	Remote surface roughness scattering
RBS	Rutherford backscattering spectroscopy
STEM	Scanning transmission electron microscopy
SIMS	Secondary ion mass spectrometry
SHO	Sequential high-pressure ozone
STI	Shallow trench isolation
SCE	Short channel effect
NO	Silicon oxinitride
SRAM	Static random access memory
SS	Sub-threshold slope
SRS	Surface roughness scattering
SRPES	Synchrotron radiation photoemission spectroscopy
TEMAHf	Tetrakis(ethylmethylamino)hafnium
TEMASi	Tetrakis(ethylmethylamino)silicon

Abbreviation	Description
TDDB	Time dependent dielectric breakdown
TEM	Transmission electron microscopy
VBM	Valence band maximum

List of Symbols

Symbol	Unit	Description
C_{inv}	F/cm^2	Inversion oxide capacitance per unit area
C_O	F/cm^2	Gate oxide capacitance per unit area
d_{dipole}	m	Length of the unit dipole
$\Delta G°_{1000}$	cal/mol	Gibbs free energy change at 1000K
ΔT_{IL}	m	Average deviation of T_{IL}
E_c	eV	Si conduction band edge
E_{eff}	MV/cm	Effective field
E_g	eV	Band gap
E_{ox}	MV/cm	Oxide field
E_V	eV	Si valence band edge
G_m	A/V (=S)	Transconductance
I_d	A	Drain current
I_g	A	Gate current
I_{off}	A	Off-current
I_{on}	A	On-current
I_s	A	Source current
J_g	A/cm^2	Gate leakage current density
L_g	m	Gate length
L_{min}	m	L_g defined by off-state leakage current
N_A	cm^{-3}	Substrate doping concentration (acceptor)
N_{dipole}	cm^{-3}	Areal density of the unit dipole
N_{sub}	cm^{-3}	Substrate doping concentration
O_O		Oxygen atom at the oxygen site of HfO_2
q	C	Elementary charge (= 1.6×10^{-19} C)
Q_{fix}	C/cm^2	Areal density of fixed charge
Q_i	C/cm^2	Areal density of inversion layer charge
T_{IL}	m	Interfacial oxide thickness
T_{inv}	m	Inversion oxide thickness
T_{phys}	m	Physical thickness
v	m/s	Carrier velocity

Symbol	Unit	Description
V_{cc}	V	Supply voltage
V_{dd}	V	Supply voltage
V_{fb}	V	Flatband voltage
V_g	V	Gate voltage
V_O		Oxygen vacancy in HfO_2
V_t	V	Threshold voltage
W_{dep}	m	Depletion region width
W_g	m	Gate width
X_d	m	Depletion layer thickness
ε_{dipole}	F/cm	Permittivity of the dipole layer
ε_{Si}	F/cm	Permittivity of silicon (= 1.04×10^{-12} F/cm)
μ	cm^2/Vs	Carrier mobility
$\mu_{RPS+RCS}$	cm^2/Vs	Mobility limited by RPS and RCS
μ_{SRS}	cm^2/Vs	SRS limited mobility
μ_{total}	cm^2/Vs	Mobility measured at 300 K
φ_{bi}	V	Built-in potential of silicon
φ_M	V	Vacuum workfunction of metal electrode
φ_S	V	Fermi level of the Si substrate
ψ_B	V	Difference between the Fermi level of the doped Si substrate and the intrinsic Fermi level

CHAPTER 1 Introduction

1.1 CMOS device scaling

1.1.1 Constant-electric-field scaling

The rapid progress of complementary metal-oxide-semiconductor (CMOS) integrated circuit technology has been accomplished by a calculated reduction of the dimensions of the unit device in the circuit – a practice termed "scaling." Dennard et al. proposed constant-field scaling in 1974 [1]. In this theory, it was proposed that one can keep short-channel effects under control by scaling down the vertical dimensions of the entire metal-oxide-semiconductor field-effect transistor (MOSFET) structure along with the horizontal dimensions, while also proportionally decreasing the applied voltages and increasing the substrate doping concentration. Figure 1-1 schematically shows the concept of constant-field scaling. The principle of constant-field scaling lies in scaling the device voltages and the device dimensions by the same factor, α (>1), so that the electric fields applied to the device are unaffected. In this way, the requirements for the reliability of the device can be satisfied regardless of the device size shrinkage.

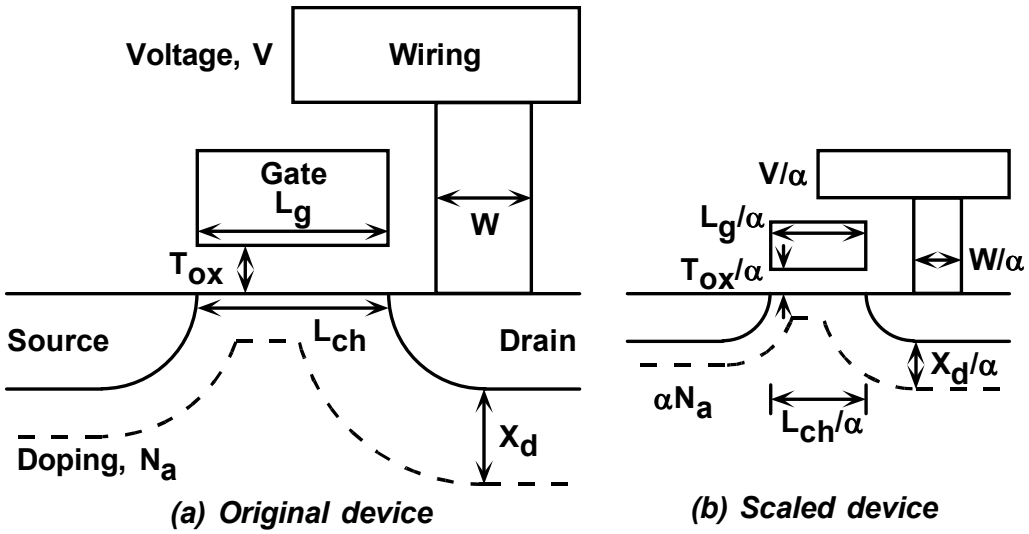


Fig. 1-1 Schematics of concept of MOSFET constant-electric-field scaling [1].

Table 1-1 summarizes the impact of constant-electric-field scaling on various device and circuit parameters. The depletion layer thickness (X_d) needs to scale by

the same factor as other device dimensions in order to suppress the potential change from the drain bias, which is known as short channel effects, and to control the inversion layer charge predominantly by gate bias. The maximum X_d is expressed by Equation (1.1).

$$X_d = \sqrt{\frac{2\varepsilon_{Si}(\varphi_{bi} + V)}{qN_{sub}}}, \tag{1.1}$$

where ε_{Si} is the permittivity of silicon (= 1.04×10^{-12} F/cm), φ_{bi} is the built-in potential of silicon, V is the supply voltage, q is the electronic charge (= 1.6×10^{-19} C), and N_{sub} is the substrate doping concentration. As seen in (1.1), the maximum X_d scales down by a factor of α, when V scales down by a factor of α and N_{sub} increases by a factor of α, thus enabling gate length scaling without losing short channel control.

Table 1-1 Scaling of MOSFET device and circuit parameters

	Device and Circuit Parameters	**Scaling factor**
MOSFET structure	Device dimensions (T_{ox}, L, W, X_j)	$1/\alpha$
	Doping concentration (N_a, N_d)	α
	Supply voltage (V)	$1/\alpha$
Scaling impact on device parameters	Electric field (ε)	1
	Carrier velocity (v)	1
	Depletion layer width (X_d)	$1/\alpha$
	Gate capacitance (C_g)	$1/\alpha$
	Inversion layer charge density (Q_i)	1
	Drive current (I_d)	$1/\alpha$
	Channel resistance (R_{ch})	1
Scaling impact on circuit parameters	Circuit delay time ($\tau \sim C_gV/I_d$)	$1/\alpha$
	Power dissipation per circuit ($P \sim VI_d$)	$1/\alpha^2$
	Power-delay product ($P\tau$)	$1/\alpha^3$
	Circuit density (~ 1/A)	α^2
	Power density (P/A)	1

All capacitances (including wiring load) scale down by a factor of α, since they are proportional to area and inversely proportional to thickness. The charge per device (~ C × V) scales down by a factor of α^2, while the inversion layer charge density (per unit gate area), Q_i, remains unchanged after scaling. Since the electric field at any given relative point of the device is maintained, the carrier velocity (v) is

also unchanged. One of the most important parameters for circuit delay is drain current (I_d), which is expressed by Equation (1.2).

$$\frac{I_d}{W} = Q_i v = Q_i \mu \varepsilon, \tag{1.2}$$

where W is the width of the gate, μ is the carrier mobility, and ε is the lateral electric field in the channel. As one can see from the equation, I_d scales down by a factor of α as a result of scaling.

With both the voltage and the current scale down by the same factor, it follows that the channel resistance at on-state of the scaled device remains unchanged. It is further assumed that parasitic resistance is either negligible or unchanged in scaling. The circuit delay, which is proportional to CV/I_d, then scales down by a factor of α. This is the most important conclusion of constant-field scaling: once the device dimensions and the supply voltage are scaled down, the circuit speeds up by the same factor. Moreover, power dissipation per circuit, which is proportional to VI_d, is reduced by a factor of α^2. Since the circuit density increases by a factor of α^2, the active power per chip area remains unchanged for the scaled-down device. The power-delay product of the scaled CMOS circuit shows a dramatic improvement by a factor of α^3. The simultaneous improvement in speed and power consumption of CMOS devices by scaling has propelled a dramatic expansion in technology and communications markets including the market associated with high performance microprocessors as well as low static-power applications, such as wireless systems.

1.1.2 Moore's law

Moore's law describes a long-term trend in the history of computing hardware, in which the number of transistors that can be placed on an integrated circuit has doubled approximately every two years. The law is named after Intel co-founder Gordon E. Moore, who introduced the concept in a 1965 paper [2]. It has since been used in the semiconductor industry to guide long-term planning and to set targets for research and development. Table 1-2 shows a historical trend of the number of transistors in Intel central processing unit (CPU) in the period between 1971 and 2005 [3].

The capabilities of many digital electronic devices are strongly linked to Moore's law: processing speed, memory capacity, sensors and even the number and size of pixels in digital cameras. All of these are improving at (roughly) exponential rates as well. This has dramatically increased the usefulness of digital electronics in nearly every segment of the world economy. Moore's law precisely describes a driving force of technological and social change in the late 20th and early 21st centuries. The trend has continued for more than half a century and is not expected to stop until 2015 or later.

Table 1-2 Historical trend of number of transistors in Intel CPU (1971-2005) [3]

Microprocessor	Year of Introduction	Transistors
4004	1971	2,300
8008	1972	2,500
8080	1974	4,500
8086	1978	29,000
Intel286	1982	134,000
Intel386™ processor	1985	275,000
Intel486™ processor	1989	1,200,000
Intel® Pentium® processor	1993	3,100,000
Intel® Pentium® II processor	1997	7,500,000
Intel® Pentium® III processor	1999	9,500,000
Intel® Pentium® 4 processor	2000	42,000,000
Intel® Itanium® processor	2001	25,000,000
Intel® Itanium® 2 processor	2003	220,000,000
Intel® Itanium® 2 processor (9MB cache)	2004	592,000,000

1.2 Requirements for high-κ dielectrics

1.2.1 MOSFET gate dielectrics

As CMOS devices have been scaled down according to Moore's law, the conventional SiO_xN_y/poly-crystalline Si (poly-Si) gate structure reached its physical limit to further reduce equivalent oxide thickness (EOT) for exponentially increasing gate leakage current. As an alternative to SiO_xN_y gate dielectrics, much work has been done on the research of high-κ materials that enable physically thicker gate dielectrics and hence lower gate leakage current while reducing the electrical thickness. Among all the candidates, Hf-based oxides, such as HfO_2 or $HfSi_xO_y$, have shown the most promise [4]. Recent studies on Hf-based oxide/poly-Si stacks have revealed, however, that an anomalous threshold voltage (V_t) increase, which is termed

Fermi-level pinning, is unavoidable with this material system [5], [6]. Although the physical models explaining this phenomenon differ in some details, they attribute the uncontrollable V_t to the intrinsic reaction at the Hf-based oxides/poly-Si interfaces in common. This fundamental issue necessitates the introduction of metal gate in conjunction with Hf-based high-κ dielectrics. Figure 1-2 schematically shows the benefit of high-κ dielectrics and metal gates in terms of inversion oxide thickness (T_{inv}). The improvement by replacing SiO_xN_y/poly-Si stacks with high-κ metal gate stacks is two-folds. One is EOT scaling from the high permittivity of the gate dielectric portion. The other is the elimination of the depletion layer at the dielectric/poly-Si interface, which amounts to approximately 0.4 nm at an inversion bias state. Both of them contribute to T_{inv} scaling.

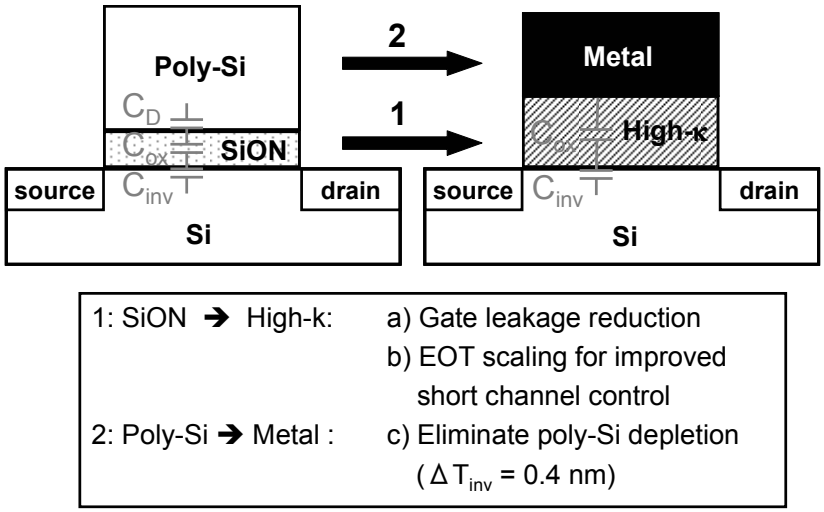


Fig. 1-2 Comparison of SiO_xN_y/Poly-Si and high-κ metal gate in inversion state. C_D, C_{ox}, and C_{inv} correspond to capacitance of depletion layer, oxide layer, and inversion layer, respectively.

Figure 1-3 shows the requirements for physical gate length (L_g) and EOT of a bulk high-performance device from the International Technology Roadmap for Semiconductors (ITRS) 2008 [7]. As seen in Fig. 1-3, continued L_g scaling below 25 nm is expected beyond 2010. Electrostatic control will be challenging in such a short L_g regime due to increasing impact from the drain bias on the potential in the channel region. Aggressive EOT scaling is one of the key enablers to maintain sufficient control of the channel potential by the gate bias. The EOT of the first generation high-κ metal gate stack was 1.0 nm [8]. The 22-nm-node and beyond requires EOT ≤ 0.6 nm for continued L_g scaling.

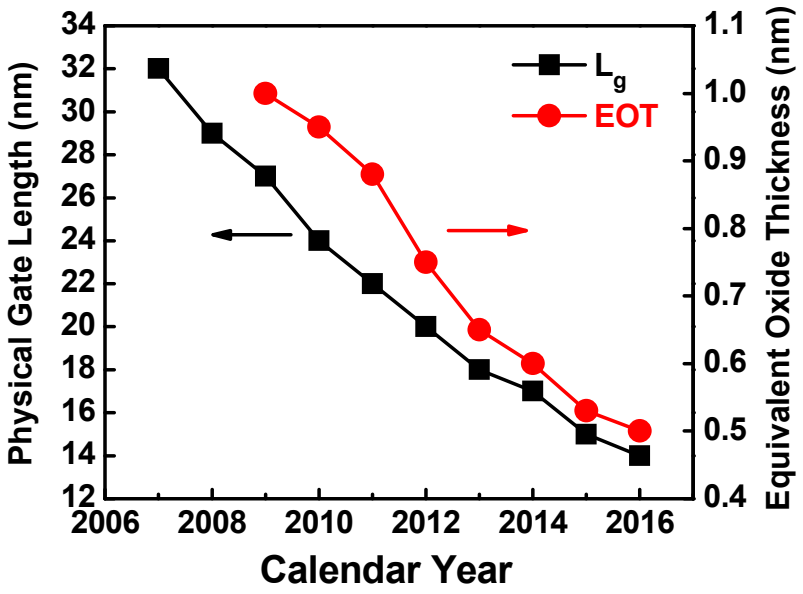


Fig. 1-3 ITRS requirements for L_g and EOT of bulk high-performance device.

In addition to EOT scaling, a high performance logic large-scale integrated circuit (LSI) requires the metal effective work functions (EWFs) to be within 0.2 eV of the conduction band edge (E_c) and valence band edge (E_V) of Si for n- and p-MOSFET, respectively [9]. Integration of CMOS devices having appropriate EWFs is one of the key challenges for the implementation of high-κ metal gate technology. After a brief introduction of two main approaches (i.e. gate-first and gate-last) of high-κ metal gate CMOS integration in Session 1.3, EWF controllability and EOT scalability will be discussed in detail in Chapter 3 (gate-last) and Chapter 4 (gate-first).

1.2.2 Embedded deep trench capacitors

Embedded dynamic random access memory (eDRAM) is a capacitor-based DRAM usually integrated on the same die as the main processor, as opposed to external DRAM modules and transistor-based static random access memory (SRAM) typically used for caches. Embedding permits much wider buses and higher operation speeds, and due to much higher density of DRAM in comparison to SRAM, larger amounts of memory can potentially be used. However, the difference in manufacturing processes make on-die integration difficult, so several dies have to be packaged in one chip, raising costs. The latest developments overcome this limitation by using standard CMOS process to manufacture eDRAM.

Fabricating deep trench (DT) capacitors prior to a standard CMOS process is one of the most promissing approaches to enable eDRAM with minimum changes to the integration flow [10, 11]. The typcial DT capacitor has a depth of several micro meters with a diemeter in the order of hundred nano meters. Thus, a large surface area per DT capacitor can be obtained with a limited footprint of a chip. This is important to keep the capacitance per DT sufficiently high to meet the requirements for operational margin. The historical migration of the shape of DT capacitors is shown in Fig. 1-4 together with the trend of capacitance per cell [12].

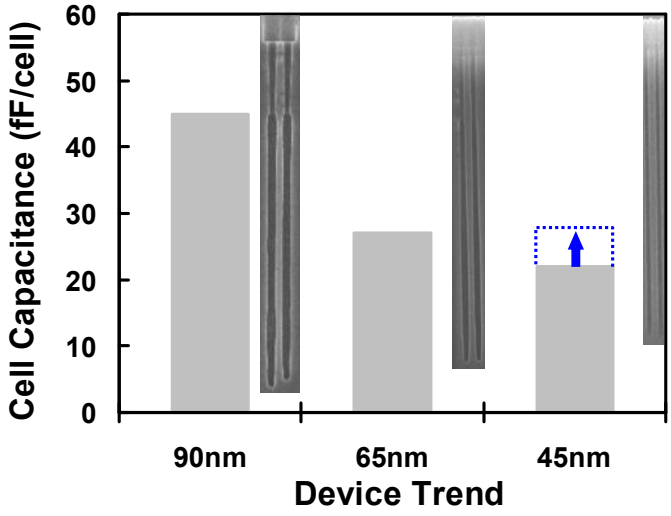


Fig. 1-4 Trend of DT capacitor configuration and capacitance per cell for 90, 65, and 45-nm-node eDRAM. The dotted collomn shows the requirement in the 45-nm-node.

Since reactive ion etching (RIE) technique has been used to form DT capacitors on a Si wafer, the depth of DT becomes shallower as the diameter becomes smaller in

accordance with CMOS scaling. This trend can be seen by comparing the cross sectional image of DT of each generation. As a result, the capacitance per cell is continuously reduced from generation to generation, provided that the conventional material (i.e. SiO_xN_y) is employed as a capacitor dielectric. As shown in Fig. 1-4, the capacitance will fall short of 25 fF/cell, which is the minimum requirement to sustain DRAM functionality, at the 45-nm-node eDRAM.

Over the last decade, a continuous trend in miniaturization of DT capacitors has required new technologies for maintaining a certain amount of capacitance per cell. Surface area enhancement techniques such as Hemi-Spherical-Grain (HSG) or the application of Al_2O_3 to the node dielectric has been investigated [13, 14]. As design rules edge into the sub-65nm region, however, geometrical options are exhausted because of physical limitations. Consequently, materials with permittivity higher than that of Al_2O_3 (~9) are required. In addition, high-κ materials for DT node dielectrics must have thermal stability of up to 1050°C and good step coverage at the same time. The potential material and process meeting these criteria will be discussed in detail in Chapter 2.

1.3 Integration of high-κ/metal gate MOSFET

Integration schemes for high-κ metal gate CMOS devices are categorized into gate-first and gate-last depending on the order of dopant activation anneal and high-κ metal gate formation. Each integration scheme is reviewed in the following sub-sections.

1.3.1 Gate-first integration

For integration of high-κ gate dielectrics into a CMOS process, a conventional integration scheme is generally favored. In gate-first process, formation of high-κ metal gate stack is completed prior to dopant activation to maximize the compatibility with the conventional CMOS process. In the state-of-the-art CMOS integration schemes, shallow trench isolation (STI) is employed for device isolation as shown in Fig. 1-5-1. After the isolation process, a pre-gate clean is performed using hydrofluoric (HF) acid followed by a pre-deposition treatment. Either a thermal treatment or a wet chemical process is used as surface preparation. Then the high-κ

film is deposited. As previously mentioned, direct contact of high-κ films and poly-Si electrodes causes undesired threshold voltage increases. Therefore, a metal film deposition follows the high-κ deposition as a workfunction setting layer. Then, the workfunction setting metal films are capped with either a poly-Si film or a low resistivity metal as shown in Fig. 1-5-2. The former stacked structure is termed metal inserted poly-Si stack (MIPS) [15]. For the latter approach, W is typically used for its thermal stability and low resistivity [16]. MIPS approach is widely accepted because of the compatibility with the conventional CMOS integration schemes. For gate patterning, photo resist is used in combination with RIE. The device structure after an ideal gate etch is shown in Fig. 1-5-3. Prior to source/drain ion implantation, a spacer is formed using a nitride layer. The activation of the junction and gate dopants is achieved by a 5 sec anneal at 1000 °C. The ideal device structure after spacer and junction formation is illustrated in Fig. 1-5-4. In order to minimize the junction and gate resistance the standard self-aligned silicide process is used, where Ni is deposited on the wafer first and then a thermal process step is applied to react the metal and the Si forming N-silicide. The unreacted Ni is selectively removed by a wet chemical process. The device structure after silicide formation is shown in Fig. 1-5-5. For device contact, an inter-layer dielectric (ILD) is deposited followed by a planarization step using chemical mechanical polishing (CMP). The contact hole process includes lithography, etch, clean and W deposition to obtain the structure described in Fig. 1-5-6. The metallization is achieved using Cu wiring in the state-of-the-art CMOS integration. A passivation anneal in forming gas completes the MOSFET fabrication.

The major advantage of gate-first process is the high compatibility with the conventional CMOS integration, but on the other hand, a high thermal budget poses more stringent requirements for the high-κ material. In the early days of high-κ research, the anomalous V_t behavior was attributed to the reaction at the Hf-based oxide/poly-Si interface. Recent studies, however, have revealed that this effect is present even in conjunction with thermally stable metal electrodes [17]. Therefore, V_t control for high-κ/metal gate stack still remains as one of the critical obstacles for implementation of gate-first integration. The technique to control V_t under the constraints of the high thermal budget of gate-first process will be discussed more in detail in Chapter 4.

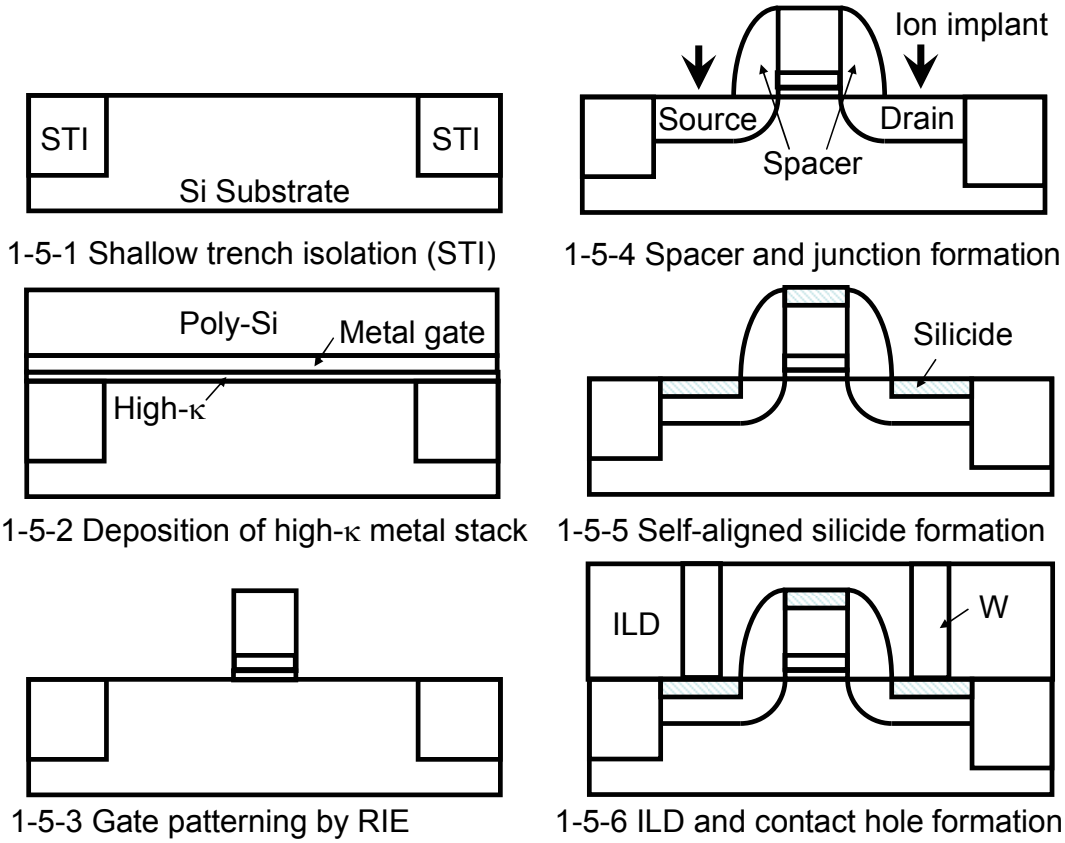


Fig. 1-5 Process flow of gate-first integration

1.3.2 Gate-last integration

Another way to obtain sufficiently low V_t is employing dual metal gates which have vacuum workfunctions corresponding to E_C and E_V of Si and limiting the thermal budget to below 500°C. This is achieved by forming the junctions prior to the high-κ/metal gate stack formation [18]. This approach is termed gate-last integration. The early process steps in gate-last process follow the conventional CMOS integration using SiO_2/poly-Si gate stacks. The SiO_2/poly-Si gate stacks serve the purpose as dummy gate structures. The source/drain junctions are formed by ion implantation using the dummy gate structure and a dopant activation anneal at 1000°C. Then the standard self-aligned silicide process is employed to form a low resistivity contact layer on the source/drain area as shown in Fig. 1-6-1. After ILD deposition, the poly-Si gate is exposed by CMP process, followed by poly-Si removal using either RIE process or wet etching process. Then the dummy SiO_2 layer is removed by HF acid to form a thinner interfacial layer as shown in Fig. 1-6-2. Prior to high-κ deposition, a pre-deposition treatment is carried out using wet-chemical treatments. As seen in Fig. 1-6-2, the high-κ layer must be grown uniformly at the bottom of the dummy gate whose aspect ratio becomes larger than 1:2 for the sub-50nm gate length MOSFETs. Therefore atomic layer deposition (ALD), which takes advantage of the surface adsorption rather than the gas phase reaction of the precursor, is the most suitable technique to form high-κ layer for gate-last process. The ALD process of Hf-based high-κ dielectrics will be discussed in Chapter 2. The high-κ deposition is followed by a post-deposition anneal (PDA). Then workfunction setting metal layers are deposited on the high-κ layer. For fabrication of CMOS devices, a metal layer for the n-type (p-type) MOSFETs needs to be removed from the p-type (n-type) MOSFET area selectively to the underlying high-κ layer, followed by a metal layer for the p-type (n-type) MOSFETs. The suitable materials for workfunction setting metals will be discussed in Chapter 3. Next, the rest of the trench is filled with a low resistivity metal such as Al or W as illustrated in Fig. 1-6-3. Then, the metal layers are removed by CMP to expose the ILD and to leave the metal layers only in the trench as shown in Fig. 1-6-4. Thus, the devices are isolated with each other in a self-aligned manner. After the metal CMP, the second ILD is deposited, followed by the

conventional contact hole and metallization process as discussed in gate-first integration to obtain the final structure as shown in Fig. 1-6-5.

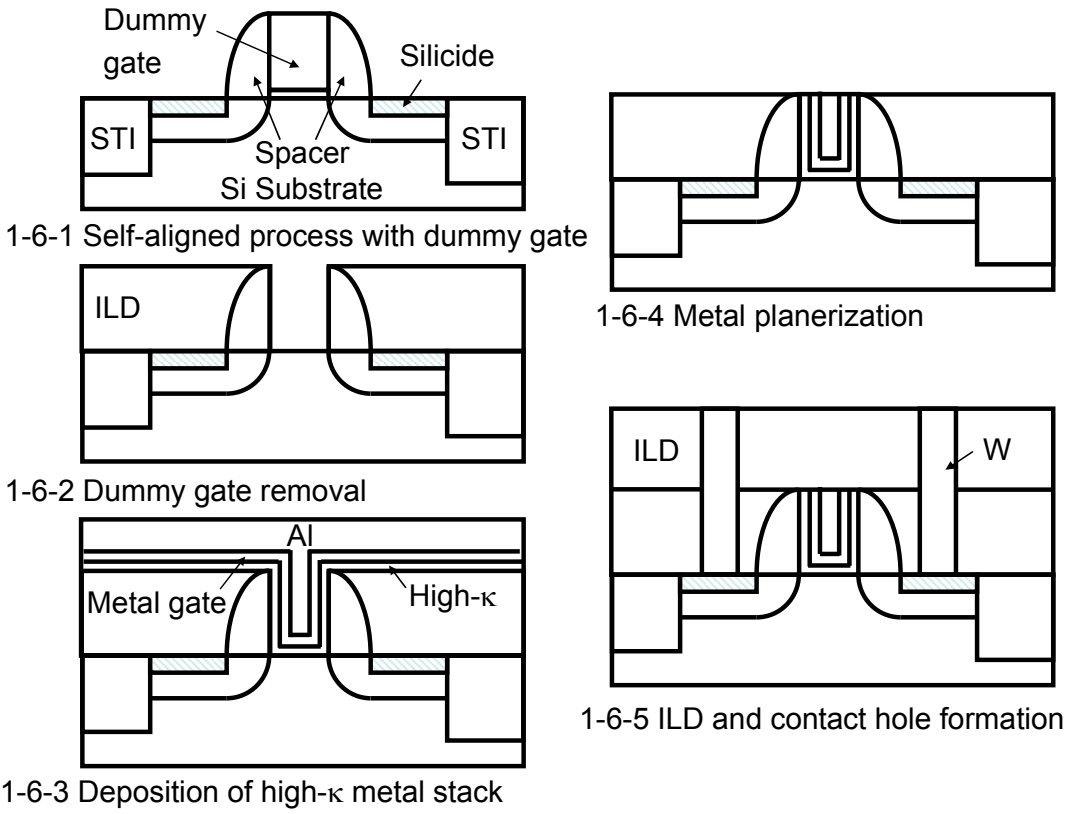


Fig. 1-6 Process flow of gate-last integration

1.3.3 Pros and cons of each scheme

The typical final structures obtained from gate-first and gate-last integration are shown in Fig. 1-7 [8, 19].

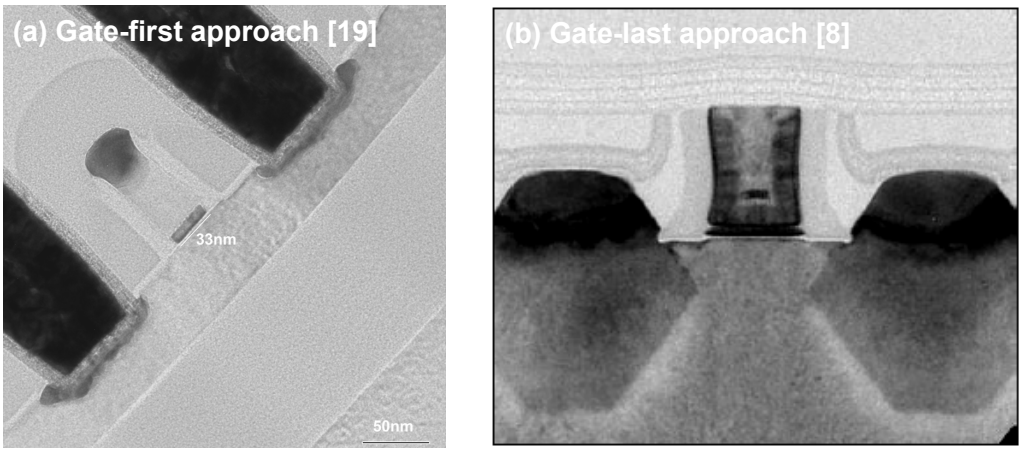


Fig. 1-7 Cross sectional TEM images of high-κ/metal gate devices fabricated by (a)gate-first process [19] and (b)gate-last process [8].

The semiconductor industry has not yet converged into one way for manufacturing. In this sub-section, generally known pros and cons of each scheme are summarized. As reviewed in Section 1.3.1, one of the most attractive characteristics of gate-first process is its simplicity. In the case of MIPS integration, depositions of high-κ and metal films are the only added steps to the conventional CMOS integration process. Therefore, the L_g can be scaled down in a similar way to the classic scaling, i.e. patterning gates with smaller dimensions using the state-of-the-art lithography tool and etching the gate structure using RIE process. It has been reported that gate-first process is a promising enabler of continued L_g scaling down to 25 nm when practiced with aggressive T_{inv} scaling [20]. In order to achieve such an aggressive device scaling, a lot of engineering effort is required in gate etching process for nearly straight vertical profiles. In addition, innovation in workfunction control is indispensable to achieve sufficiently low V_t values due to thermal instability of high-κ metal gate stacks. On the other hand, thermal budget on high-κ metal gate stacks is significantly reduced in gate-last process as reviewed in Section 1.3.2, which increases the options for gate electrode materials. Another benefit of gate-last process

is strain enhancement in the channel of MOSFETs. It has been reported that removal of dummy gate structure under the external stress element enhances the strain in the channel resulting in higher performance [21]. Since the modern CMOS technology relies on performance boost from strain engineering, gate-last process offers another attractive knob which has not been exploited in the previous CMOS generations. The biggest challenge of gate-last process is the metal fill into the trench and the subsequent metal CMP process. These steps add a lot of complexity to the CMOS integration flow. Also, the L_g scaling with gate-last process is limited by the gap fill capability, and thus requires continued innovation for future technology nodes. The pros and cons for gate-first and gate-last processes are summarized in Table 1-3.

Table 1-3 Summary of pros and cons

	Pros	Cons
Gate-first (MIPS)	Process simplicity L_g scalability	Workfunction instability Gate RIE
Gate-last	Material flexibility Strain enhancement	Process complexity (Gap fill, Metal CMP)

1.4 Purpose of this study

As reviewed in this Chapter, the Si-based CMOS technology is currently on the cusp of paradigm shift from the classic scaling rule to performance improvement by introduction of new materials. In this new era, the driving force of Moore's law is continued innovation in materials technology and the state-of-the-art lithography tool alone does not guarantee the future anymore. The primary purpose of this study is to establish methodologies of V_t control and EOT scaling of the high-κ metal gate stacks for the 22-nm-node and beyond and to obtain a general guideline for performance improvement in the material-driven scaling era by focusing on carrier mobility of MOSFETs.

Chapter 2 describes growth techniques of high-κ films and a leakage current conduction mechanism. Based on these understandings, materials and processes for

achieving EOT scaling and a low leakage current are discussed. Finally in this Chapter, feasibility of ALD HfSiON process as a node dielectric of DT capacitors is demonstrated. Chapter 3 discusses the suitable gate materials for gate-last high-κ metal gate MOSFETs. Hf-Si is proposed as a gate electrode for n-type MOSFETs. Through a systematic investigation of the HfO_2/Hf-Si stacks, key factors for V_t control and carrier mobility in gate-last process are clarified. On the other hand, V_t control and EOT scaling for gate-first high-κ metal gate MOSFETs are discussed in Chapter 4. The EOT scaling strategy for the 22-nm-node and beyond is shown in this Chapter. Chapter 3 and 4 provide new perspectives for comparing gate-first and gate-last processes in terms of EOT scaling and carrier mobility. Chapter 5 describes the impact of the extreme EOT scaling on carrier mobility based on the learning from both gate-last and gate-first processes. Physical models explaining mobility degradation from the EOT scaling and the V_t control techniques are proposed. Based on these models, a possible gate stack scaling scenario for MOSFETs in the future generation operating in a quasi-ballistic carrier transport regime is discussed. Finally, Chapter 6 provides general conclusions of this study.

Reference

[1] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc: J. IEEE **SC–9** (1974) 256 .

[2] G. E. Moore: Electronics **38** (1965) 8.

[3] Intel Corporation press kit; http://www.intel.com/pressroom/kits/events/moores_law_40th/index.htm?iid=tech_mooreslaw+body_presskit

[4] G. D. Wilk, R. M. Wallace, and J. M. Anthony: J. Appl. Phys. **89** (2001) 5243.

[5] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hedge, D. Gilmer, R. Garacia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin: Tech. Dig. VLSI Symp., 2003, p. 9.

[6] K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Kohno, T. Chikyo, H. Kitajima, and T. Arikada: Tech. Dig. VLSI Symp., 2004, p. 108.

[7] The International Technology Roadmap for Semiconductors; see http://www.itrs.net/Links/2008ITRS/Home2008.htm for the latest updates (2008).

[8] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M.Buehler, A. Cappelani, R. Chau, C. H. Choi, G. Ding, K. Fischer, T.Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, D. Huessner, D. Ingerley, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liy, B. McIntyre, P. Moon, J. Neiynck, C. Parker, D.Parsons, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L.Schifren, J. Sebastian, J. Seiple, D. Simon, S.Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vanderyoon, S. Williams, and K. Zawadzi: Tech. Dig. Int. Electron Devices Meet., 2007, p. 247.

[9] A. Kumar and P. M. Solomon: IEEE Trans. Electron Devices **53** (2006) 1208.

[10] L.Nesbir, J.Alsmeier, B.Chen, J.DeBrosse, P.Fahey, M.Gall, J.Gambino, S.Gernhardt, H.lshiuchi, R.Kleinhenz, J.Mandelrnan, T.Mii, M.Morikado, A.Nitayama, S.Parke, H.Wong, GBronner: Tech. Dig. Int. Electron Devices Meet., 1993, p. 627.

[11] G.Bronner, H.Aochi, M.Gall, J.Gambino, S.Gernhardt, E.Harnrner, H.Ho, J.lba, H.Ishiuchi, M.Jaso, R.Kleinhenz, T.Mii, M.Narita, L.Nesbit, W.Neumueller, A.Nitayama, T.Ohiwa, S.Parke, J.Ryan, T.Sato, H.Takato, S.Yoshikawa: Tech. Dig. VLSI Symp., 1995, p. 15.

[12] T. Ando, N. Sato, S.Hiyama, T.Hirano, K. Nagaoka, H.Abe, A.Okuyama, H. Ugajin, K. Tai, S. Fujita, K. Watanabe, R. Katsumata, J. Idebuchi, T. Suzuki, T. Hasegawa, H. Iwamoto, S. Kadomura: Extended Abstracts of SSDM, 2005, p. 186.

[13] H. Watanabe, T. Tatsumi, S. Ohnisihi, T. Hamada, I. Honma, and T. Kikkawa: Tech. Dig. Int. Electron Devices Meet., 1992, p.259.

[14] H. Seidl, M. Gutsche, U. Schroeder, A. Birner, T. Hecht, S. Jakschik, J. Luetzen, M. Kerber, S. Kudelka, T. Popp, A. Orth, H. Reisinger, A. Saenger, K. Schupke, B. Sell: Tech. Dig. Int. Electron Devices Meet., 2002, p.839.

[15] H.-S. Jung, J.-H. Lee, S.K. Han, Y.-S. Kim, H.J. Lim, M.J. Kim, S.J. Doh, M.Y. Yu, N.-I. Lee, H.-L. Lee, T.-S. Jeon, H.-J. Cho, S.B. Kang, S.Y. Kim, I.S. Park, D. Kim, H.S. Baik, Y.S. Chung: Tech. Dig. VLSI Symp., 2005, p. 232.

[16] F. Ootsuka, A. Katakami, K. Shirai, T. Watanabe, H. Nakata, M. Kitajima, T. Aoyama, T. Eimori, Y. Nara, Y. Ohji, M. Tanjyo: IEEE Trans. Electron Devices **55** (2008) 1042.

[17] Y. Akasaka, G. Nakamura, K. Shiraishi, N. Umezawa, K. Yamabe, O. Ogawa, M. Lee, T. Amiaka, T. Kasuya, H. Watabnabe, T. Chikyo, F. Ootsuka, Y. Nara, K. Nakamura: Jpn. J. Appl. Phys. **45** (2006) L1289.

[18] S. Yamaguchi, K. Tai, T. Hirano, T. Ando, S. Hiyama, J. Wang, Y. Hagimoto, Y. Nagahama, T. Kato, K. Nagano, M. Yamanaka, S. Terauchi, S. Kanda, R. Yamamoto, Y. Tateshita, Y. Tagawa, H. Iwamoto, M. Saito, N. Nagashima, and S. Kadomura: Tech. Dig. VLSI Symp., 2006, p. 192.

[19] M. Chudzik, B. Doris, R. Mo, J. Sleight, E. Cartier, and C. Dewan, D. Park, H. Bu, W. Natzle, W. Yan, C. Ouyang, K. Henson, D. Boyd, S. Callegari, R. Carter, D. Casarotto, M. Gribelyuk, M. Hargrove, W. He, Y. Kim, B. Linder, N. Moumen, V.K. Paruchuri, J. Stathis, M. Steen, A. Vayshenker, X. Wang, S. Zafar, T. Ando, R. Iijima, M. Takayanagi, V. Narayanan, R. Wise, Y. Zhang, R. Divakaruni, M.Khare, T.C. Chen: Tech. Dig. VLSI Symp., 2007, p. 194.

[20] K. Henson, H. Bu, M. H. Na, Y. Liang, U. Kwon, S. Krishnan, J. Schaeffer, R. Jha, N. Moumen, R. Carter, C. DeWan, R. Donation, D. Guo, M. Hargrove, W. He, R. Mo, R. Ramachandran, K. Ramani, K. Schonenberg, Y. Tsang, X. Wang, M. Gribelyuk, W. Yan, J. Shepard, E. Cartier, M. Frank, E. Harley, R. Arndt, R. Knarr, T. Bailey, B. Zhang, K. Wong, T. Graves-Abe, E. Luckowski, D-G. Park, V. Narayanan, M. Chudzik, M. Khare: Tech. Dig. Int. Electron Devices Meet., 2008, p. 645.

[21] J. Wang, Y. Tateshita, S. Yamakawa, K. Nagano, T. Hirano, Y. Kikuchi, Y. Miyanami, S. Yamaguchi, K. Tai, R. Yamamoto, S. Kanda, T. Kimura, K. Kugimiya, M. Tsukamoto, H. Wakabayashi, Y. Tagawa, H. Iwamoto, T. Ohno, M. Saito, S. Kadomura and N. Nagashima: Tech. Dig. VLSI Symp., 2007, p. 46.

CHAPTER 2 High-κ film growth and characterization

Growth of high-κ films with excellent insulating properties and thickness control of atomic precision is indispensable for the high-κ metal gate technology. In this Chapter, an ALD process for $Hf(Si)O_x$ is established with maturity enabling application to the state-of-the-art eDRAM. Importance of reduction of the residual carbon concentration is highlighted to realize a high-κ dielectric with extremely low leakage current. The ALD process established in this Chapter is the key building block throughout this study.

2.1 Introduction

As reviewed in Chapter 1, a node dielectric with a higher permittivity than that of Al_2O_3 (~9) is required for the DT capacitor in the 45-nm-node and beyond. In addition, application to DT capacitors necessitates thermal stability of up to 1050°C and good step coverage at the same time. The comparison of high-κ materials from these viewpoints is shown in Table 2-1. Although HfSiON, which has been widely investigated as gate dielectrics, shows both a high permittivity (~13) and thermal stability of up to 1000°C, it has never been considered as a candidate for the node dielectric of DT capacitors. This is due to the difficulty of depositing ternary materials into high aspect ratio structures with a uniform film composition.

Table 2-1 Comparison of high-κ materials for node dielectric for DT capacitor

Material	Permittivity	Thermal Stability	Deposition Method	Step Coverage
Si_3N_4	7	○	CVD	○
Al_2O_3	9	○	ALD	○
HfO_2	20	×	ALD	○
$HfAlO_x$	15-20	×	ALD	○
HfSiON	10-15	○	CVD	×
HfSiON	10-15	○	ALD	Unreported

2.2 Atomic Layer Deposition of $HfSiO_x$

In this study, feasibility of HfSiON as a node dielectric for DT capacitors was investigated by exploring ALD processes. Tetrakis(ethylmethylamino)hafnium (TEMAHf) and tetrakis(ethylmethylamino)silicon (TEMASi) were used as precursors. The chemical formulas of TEMAHf and TEMASi are shown in Fig. 2-1.

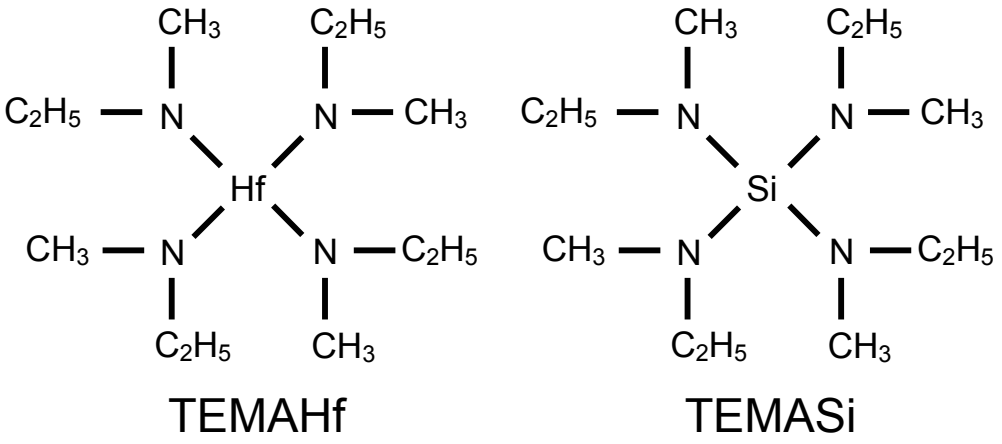


Fig. 2-1 Chemical formulas for TEMAHf and TEMASi.

Two ALD sequences were compared using these precursors. One is a laminate process in which HfO_2 and SiO_2 are deposited alternately. In this case, the Hf/Si ratio of the film is controlled by the cycle ratio. On the other hand, a coinjection process is a method of introducing multiple precursors into a chamber at the same time. TEMAHf and TEMASi is an ideal combination for the coinjection process because of close vapor pressures and absence of vapor phase reaction. In addition, having the same ligands (ethylmethylamino) enables exchange of the ligands between TEMAHf and TEMASi, resulting in a uniform chemical adsorption on the surface [1]. Figure 2-2 schematically shows the procedure of the coinjection process. The Hf ratio [Hf/(Hf+Si)%] of the film can be controlled over the range of 0~100% by varying the precursor gas flow rate. At step 1, TEMAHf and TEMASi molecules are chemically adsorbed to the substrate. At step 2, an Ar flow is introduced to the chamber to purge the unadsorbed molecules and to leave only a monolayer of molecules attached to the surface. At step 3, an O_3 flow is introduced to replace ethylmethylamino ligands with

oxygen atoms and to form a $HfSiO_x$ layer. At step 4, an Ar flow is introduced again to purge the O_3 gas in the chamber and to avoid the vapor phase reaction during the next TEMAHf and TEMASi flow. These steps are repeated until the $HfSiO_x$ layer reaches the target thickness. The deposition rates (DR) of the laminate and coinjection as a function of the Hf ratio are shown in Fig. 2-3. The Hf ratio was obtained by Rutherford backscattering spectroscopy (RBS).

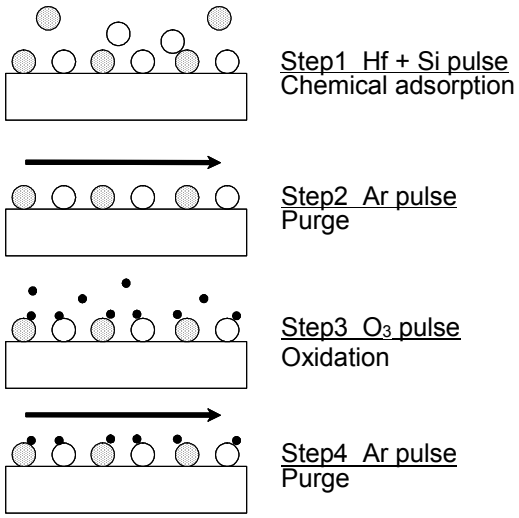


Fig. 2-2 Procedure of co-injection (1cycle).

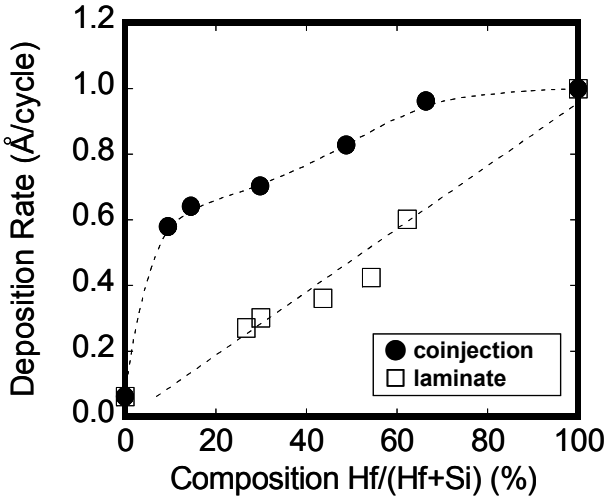


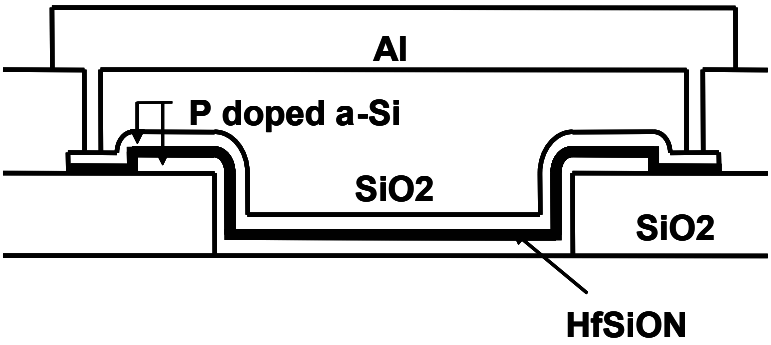
Fig. 2-3 Deposition rates of laminate and co-injection process as function of Hf ratio obtained by RBS.

The extremely low DR of SiO_2 (Hf/(Hf+Si)=0%, < 0.1 Å/cycle) compared with that of HfO_2 (Hf/(Hf+Si)=100%, ~1 Å/cycle) corresponds to the large disparity of sticking factors between TEMAHf and TEMASi. According to the simulation by Erben et al. [2], the difference in sticking factors leads to a gradation of Hf/Si ratio in

the depth direction of the DT structure. Since a uniform Hf/Si ratio is required to maintain a high permittivity and a high thermal stability in the entire DT structure, bridging the difference in sticking factors is of paramount importance. In the laminate process, DR increased in proportion to the Hf/(Hf+Si) ratio of the film. On the contrary, the coinjection process exhibited an increased DR from the proportional relationship. This phenomenon can be explained by the catalytic effect of TEMAHf in conjunction with TEMASi. It is speculated that the sticking factors for TEMAHf and TEMASi become closer due to this effect.

2.3 Experimental

First, the step coverage performance of each ALD process was evaluated using the DT of the 45 nm-node-eDRAM. Next, the mechanism underlying leakage current was analyzed on the basis of electrical properties of the planar capacitors whose cross-sectional structure is shown in Fig. 2-4. The thickness and stoichiometry of the HfSiON films are summarized in the table in Fig. 2-4.



Thickness	5 ~ 10nm
Hf/Si ratio	50%
N concentration	15atom%

Fig. 2-4 Schematics of planer capacitor fabricated in this study.

In this experiment, substrate temperature and chamber pressure during the ALD process were varied and their impact on the electrical properties was examined. For the film analysis, secondary ion mass spectrometry (SIMS) and synchrotron radiation photoemission spectroscopy (SRPES) were carried out. Finally, DT capacitors were fabricated using the 65 nm-node-eDRAM technology. Figure 2-5 shows the main part of the integration flow. The Hf/Si ratio of the film was adjusted

to 50% for all the samples. The nitridation of HfSiOx films was performed by NH_3 annealing.

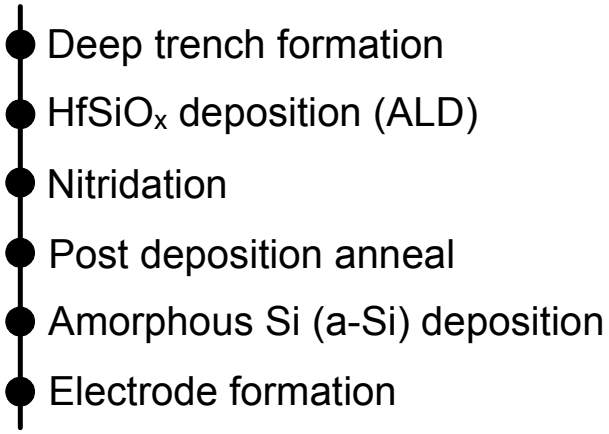


Fig. 2-5 Integration flow of DT capacitors.

2.4 Results and Discussions

2.4.1 Step coverage in DT (45-nm-node eDRAM)

In order to investigate the gradation of the stoichiometry of the HfSiON film in the depth direction of DT, SIMS analysis was performed while sputtering the Si substrate where DTs were formed with a known areal density. The SIMS intensity of Hf and N from that area were traced as a function of the sputtering time. The depth profiles of Hf and N for HfSiON films deposited by the laminate and coinjection processes were summarized as a function of normalized depth in the DT (full depth of DT = 1) as shown in Fig. 2-6. As seen in Fig. 2-6, Hf depletion occurred near the bottom of DT in the case of laminate, while the coinjection process showed uniform depth profiles of both Hf and N. This difference can be attributed to the catalytic effect of the coinjection process. In view of the flat distribution of each component of HfSiON in the depth direction, the coinjection process was chosen for DT applications in this study.

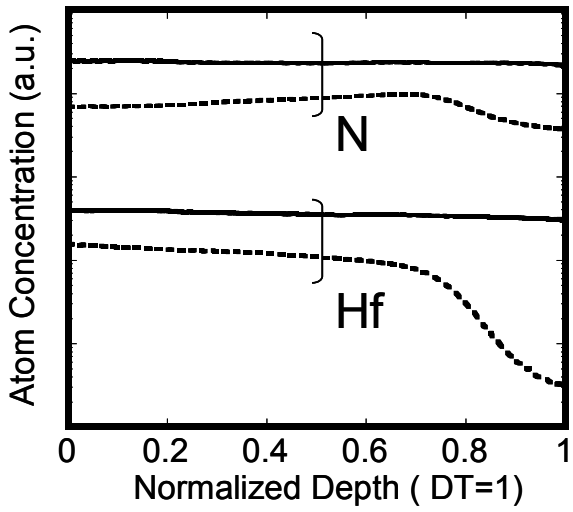


Fig. 2-6 Depth profiles of Hf and N obtained by SIMS (solid : coinjection, dashed : laminate). The x-axis is normalized by the total depth of the DT.

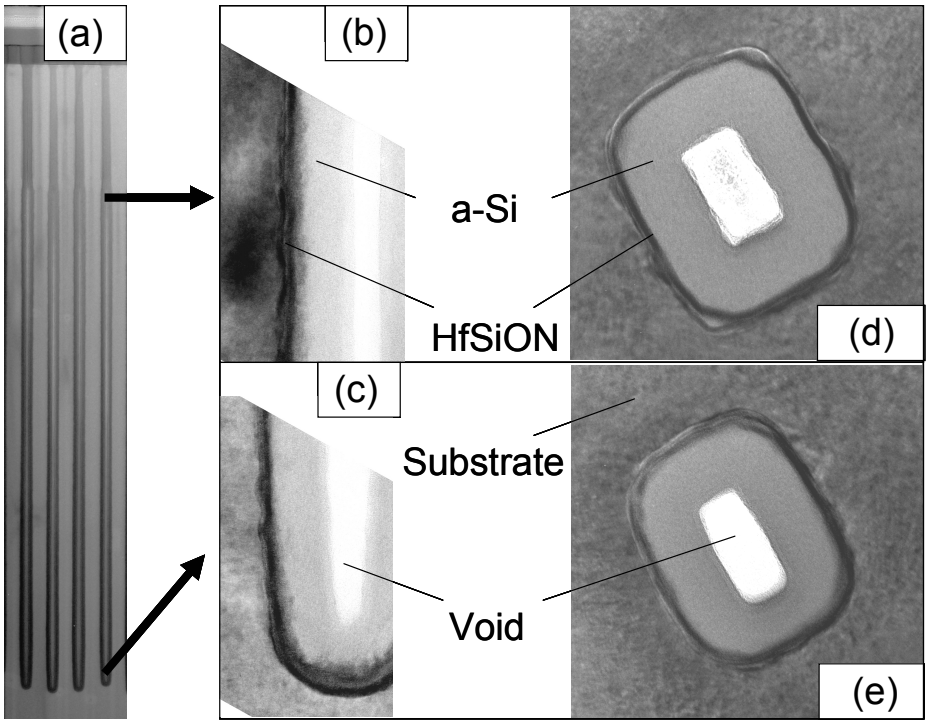


Fig. 2-7 (a) Cross-section image of entire DT structure.
Fig. 2-7 (b)-(c) Perpendicular images to wafer surface at same magnification.
Fig. 2-7 (d)-(e) Parallel images to wafer surface at same magnification.

Shown in Figs. 2-7 (a)-(e) are cross-sectional transmission electron microscopy (TEM) images of the coinjection sample. Almost identical physical thicknesses of HfSiON near the top and the bottom of DT were confirmed. On the basis of these results, it can be concluded that HfSiON obtained by the coinjection process has a sufficient step coverage performance for the 45-nm-node DT applications.

2.4.2 Mechanism underlying leakage current (planer)

The dependences of EOT-leakage current properties on the substrate temperature and chamber pressure during the ALD process are shown in Figs. 2-8 and 2-9, respectively. The leakage current was measured at a gate bias of 1V. As one can see in these figures, higher temperatures and higher pressures during the ALD process lead to a lower leakage current at a given EOT. These trends can be summarized as a function of carbon concentration in $HfSiO_x$, which was measured by SIMS as shown in Fig. 2-10.

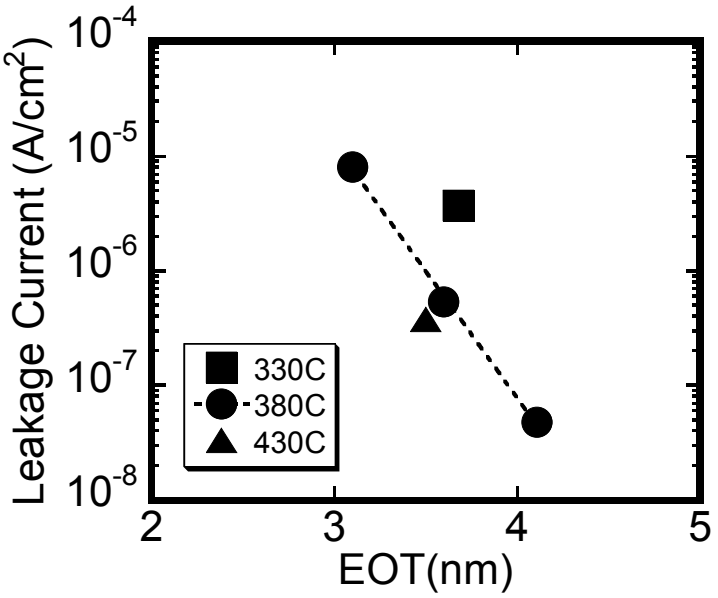


Fig. 2-8 Substrate temperature dependence (@ 2Torr) of EOT-Leak properties which were measured at gate bias of 1V.

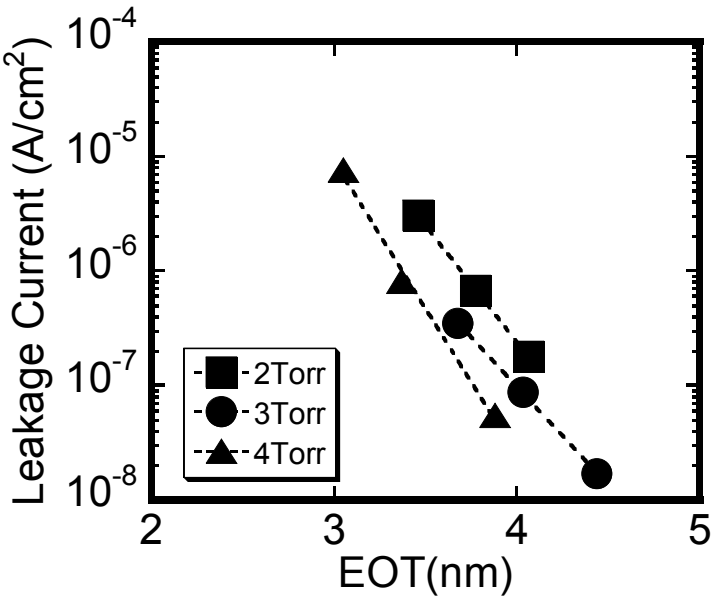


Fig. 2-9 Chamber pressure dependence (@ 380°C) of EOT-Leak properties which were measured at gate bias of 1V.

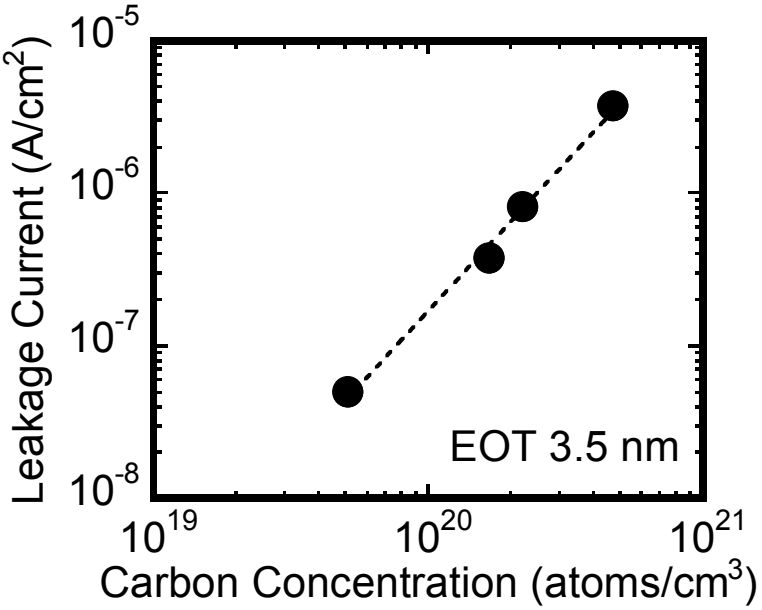


Fig. 2-10 Leakage current at gate bias of 1V as function of carbon concentration in $HfSiO_x$ measured by SIMS.

A strong correlation between leakage current and carbon concentration was observed. The concentration of residual carbon decreased as the temperature and pressure in the ALD process increased due to a stronger oxidative effect of O_3. Since there exits a strong correlation between leakage current and carbon concentration, it is extremely important to reduce the concentration of carbon.

The measurement temperature dependence of the leakage current was also examined and an Arrhenius plot was obtained as shown in Fig. 2-11. A good linearity of the Arrhenius plot indicates that the conduction mechanism is Poole-Frenkel (PF) type. It should be noted that the leakage current increased as carbon concentration increased while maintaining almost the same slope. This trend suggests the possible contribution of electron traps originating from residual carbon in HfSiON films to PF current. Then, trap depth was calculated to be 0.9 eV from the slope of the Arrhenius plot. Since both electrodes are n-type Si, it can be deduced that the dominant carrier is electron. Consequently the trap level locates below the conduction band minimum (CBM) of HfSiON. In order to elucidate the precise band alignment of HfSiON used in this study, SRPES was carried out. The valence band maximum (VBM) offset from that of Si was derived from the valence band spectrum of HfSiON by subtracting the spectrum of H-terminated Si(001) as a background [3]. On the other hand, the band gap (E_g) of HfSiON was extracted from the O 1s energy-loss spectrum, which reflects the interband transition from the valence band to the conduction band [4].

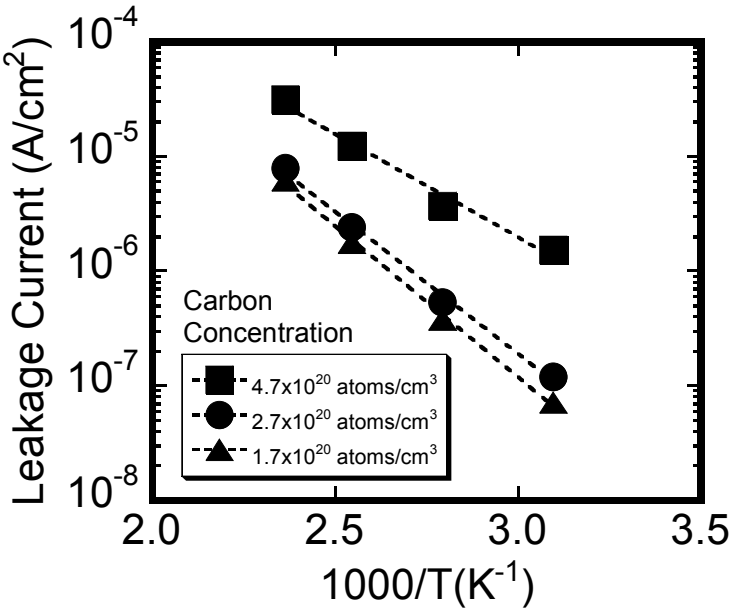


Fig. 2-11 Arrhenius plot of samples with varied carbon concentrations. The leakage current was measured in the temperature range between room temperature to 150°C.

Shown in Fig. 2-12 is the band diagram of HfSiON and the trap level, which was estimated from the Arrhenius plot. It was revealed that the trap level locates approximately 0.7 eV higher than the Fermi level of n-type Si, which is thought to be a reasonable path of electron current under the operating bias voltage.

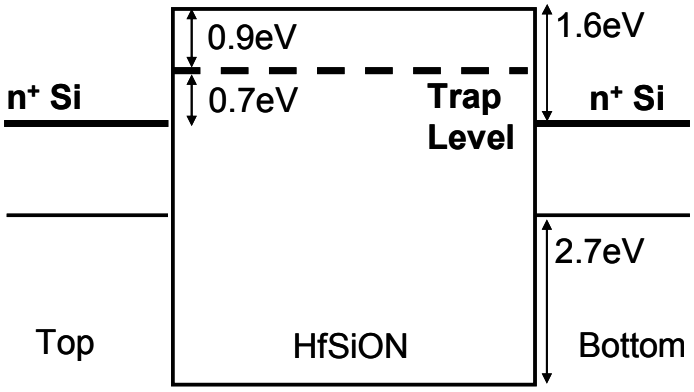


Fig. 2-12 Band diagram of n^+ Si/HfSiON/n^+ Si stack obtained by SRPES and trap level derived by Arrhenius plot.

The mechanism behind the link between the residual carbon and the trap level below the CBM of HfSiON requires further study. The possible model is that the residual carbon concentration is an indicator of oxygen vacancy concentration in the HfSiON film. It has been reported that oxygen vacancies in a Hf-based high-κ dielectric form a trap level 0.3-1.6 eV below the CBM of HfO_2 depending on charged status [5]. The residual carbon atoms in our ALD process originate from unreplaced ethylmethylamino-ligands. Three carbon atoms belong to one ligand as shown in Fig. 2-1. Since the bond between a Hf atom and an ethylmethylamino-ligand is weak enough to facilitate chemical adsorption, the unreplaced ethylmethylamino-ligand during the ALD process is most likely disconnected after the device fabrication process including a 1050°C anneal, leaving an oxygen vacancy in the oxygen site of HfO_2. Thus, a carbon concentration in a Hf-based high-κ dielectric can be an effective indicator of film quality. This model is extendible to any chemical reaction process of Hf-based high-κ film using a metal organic precursor. In the next sub-section, leakage current improvement using this metrics is demonstrated.

2.4.3 Reduction of leakage current

On the basis of the findings presented in the previous sub-section, we propose two solutions for low leakage current. One is sequential high-pressure ozone (SHO) treatment, which is a method for reducing carbon concentration in $HfSiO_x$ without causing any step coverage degradation. Although leakage current can be reduced

using a higher chamber pressure during the ALD process, the thermal decomposition of the precursors occurs at a certain point, which leads to a severe degradation of the step coverage. That is, there is a conflict between film quality and the step coverage performance of HfSiON in the conventional ALD process. The concept of SHO treatment is shown in Fig. 2-13. In this sequence, the coinjection process is carried out at lower than the critical pressure which separates the ALD mode and the chemical vapor deposition (CVD) mode (thermal decomposition of the precursors). In addition to the coinjection cycles, an O_3 step at the higher chamber pressure than the critical pressure is inserted every 5 to 10 cycles. In this additional O_3 step, residual carbons in the film are oxidized and removed without causing CVD reaction. Therefore, a reduced amount of residual carbons and excellent step coverage in the DT structure can be obtained at the same time.

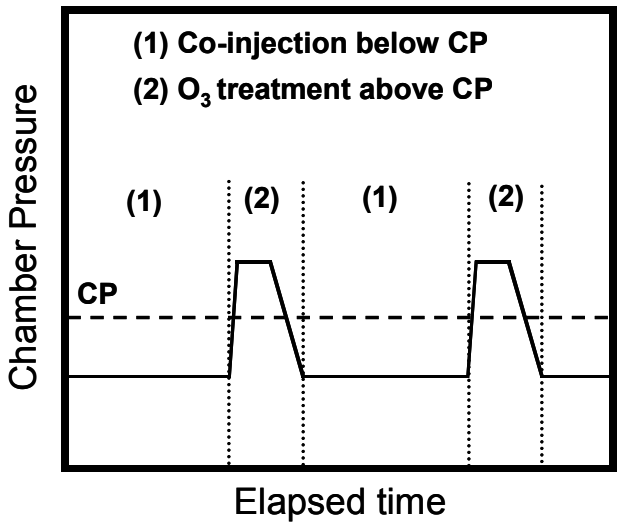


Fig. 2-13 Procedure of SHO treatment (CP: critical pressure that separates ALD and CVD).

Figure 2-14 shows the SIMS depth profiles of carbon in HfSiON with and without SHO treatment. It was confirmed that carbon concentration can be reduced by 60% with SHO treatment.

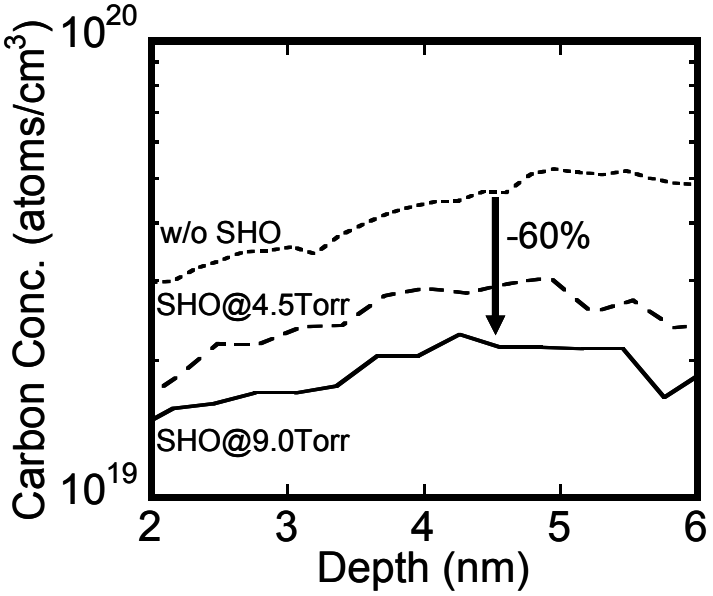


Fig. 2-14 Depth profiles of carbon concentration obtained by SIMS, with and without SHO.

The other solution is the sandwich structure (Si_3N_4/HfSiON/Al_2O_3 stack). To realize this structure, the prenitridation of the substrate is carried out before HfSiOx deposition by the coinjection process. After the postnitridation of $HfSiO_x$, the film is capped with ALD Al_2O_3. As a result, HfSiON is sandwiched between Si_3N_4 and Al_2O_3, both of which have larger CBM offsets than that of HfSiON, as shown in Fig. 2-15. The values for Al_2O_3 and Si_3N_4 are quoted from ref. [6]. Consequently, the trap-assisted electron current can be suppressed as compared with the single film of HfSiON. In addition, it should be noted that this combination of materials is thermally robust up to 1050°C, which means it is applicable to DT dielectrics. Since both HfSiON obtained by the coinjection process and ALD Al_2O_3 exhibit an excellent step coverage, the same effect as that of planar capacitors can be expected in high-aspect-ratio DT capacitors.

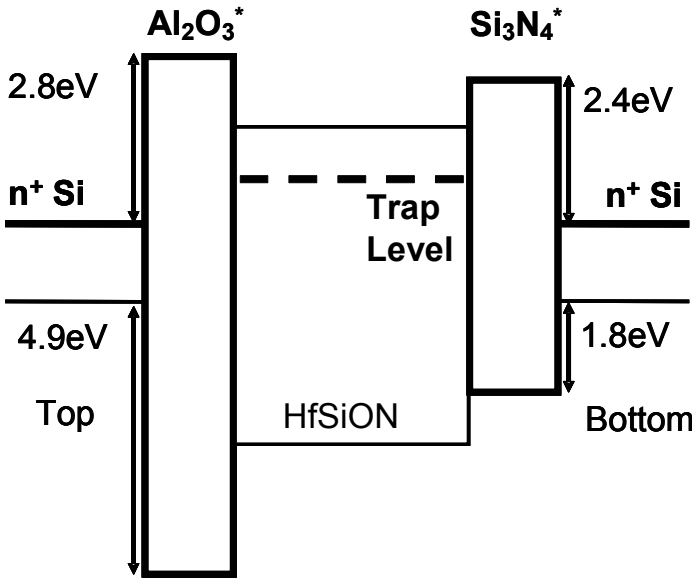


Fig. 2-15 Band diagram of sandwich structure (Si_3N_4/HfSiON/Al_2O_3 stack). The values for Al_2O_3* and Si_3N_4* are quoted from ref. [6].

2.4.4 Application to DT capacitors (65-nm-node eDRAM)

Finally, SHO treatment and the sandwich structure were applied to the fabrication of DT capacitors of the 65 nm-node-eDRAM. Shown in Fig. 2-16 is a capacitance versus leakage current plot, which was measured at the operating voltage ($V_{cc}/2$ = 0.6 V). The effect of SHO at a higher pressure was clearly observed and a capacitance enhancement of 30% as compared with the conventional dielectric (NO) was achieved at the leakage current of 0.1 fA/cell. Moreover, it was revealed that the sandwich structure more than compensated the EOT loss caused by a lower permittivity, and a capacitance enhancement of 50% was gained. Time dependent dielectric breakdown (TDDB) lifetime was also estimated as shown in Fig. 2-17. As a result, the product condition (memory size: 512 Mb, failure rate: 1ppm) demonstrated a 10-year lifetime at V_{node}=1.4 V.

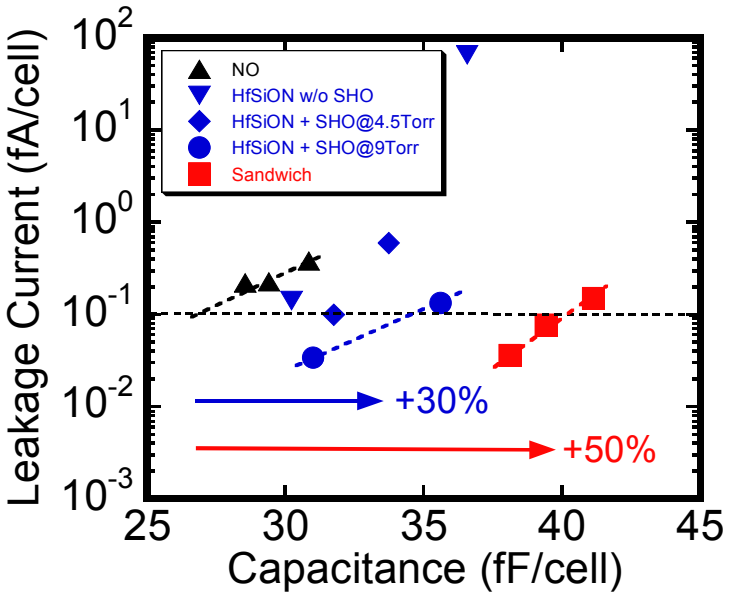


Fig. 2-16 Capacitance as function of leakage current (DT capacitors of 65-nm-node eDRAM, V_{node}=0.6V). Capacitance enhancement was measured at a leakage current of 0.1fA/cell.

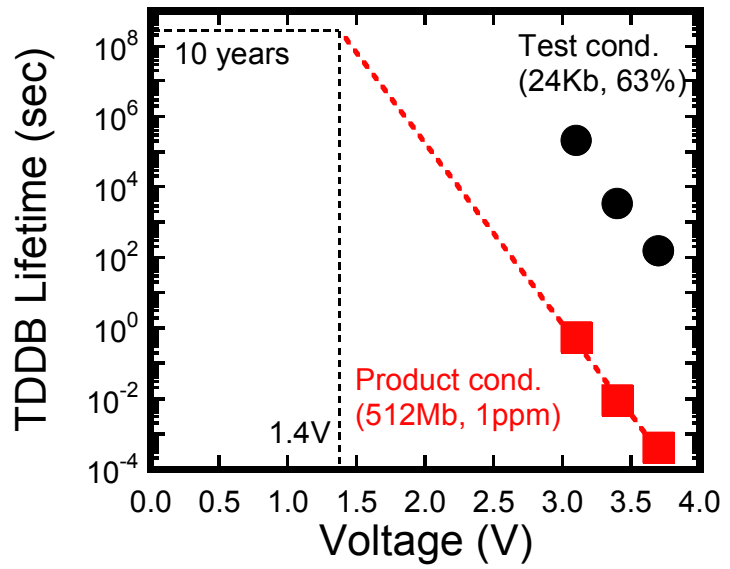


Fig. 2-17 TDDB life time as function of stress voltage. The test conditions were 85°C and constant voltage stress

2.5 Summary

In this Chapter, HfSiON was applied to the node dielectric of DT capacitors for the first time. The coinjection process of $HfSiO_x$ exhibited a sign of catalytic effect. By taking advantage of this effect, the conformal step coverage of HfSiON in the DT of the 45-nm-node eDRAM was achieved. In addition, the mechanism underlying leakage current was revealed to be PF current originating from residual carbon. This finding enables leakage current improvement of Hf-based high-κ films by using residual carbon concentration in the films as metrics. This method should be applicable to Hf-based high-κ films deposited from metal organic precursors in general. Then, SHO treatment and the sandwich structure (Si_3N_4/HfSiON/Al_2O_3 stack) were proposed in order to suppress the leakage current.

Finally, The DT capacitors of the 65 nm-node were fabricated and we demonstrated a capacitance enhancement of 50% as compared with the conventional SiON film. It can be concluded that the Si_3N_4/HfSiON/Al_2O_3 stack obtained by our newly developed ALD process is one of the promising candidates for the DT dielectric for the 45 nm-node-eDRAM and beyond.

Reference

[1] Y. Senzaki, S. Park, H. Chatham and L. Bartholomew: J. Vac. Sci. Tech. A **22** (2004) 1175.

[2] E. Erben, T. Hecht, S. Jakschik, W. Wiebauer, A. Kersch, G. Prechtl, U. Schroder, A. Link. T. Igel-Holtzendorff : ALD 2004 conference.

[3] S. Toyoda, J. Okabayashi, H. Kumigashira, M. Oshima, K. Ono, M. Niwa, K. Usuda, N. Hirashita : J. Electron Spectroscopy and Related Phenomena **137-140** (2004) 141.

[4] F. G. Bell and L. Ley : Phys. Rev. B **37** (1988) 8383.

[5] K. Torii, K. Shiraishi, S. Miyazaki, K. Yamabe, M. Boero, T. Chikyow, K. Yamada, H. Kitajima, and T. Arikado: Tech. Dig. Int. Electron Devices Meet., 2004, p. 129.

[6] J. Robertson : J. Vac. Sci & Technol. B **18** (2000) 1785.

CHAPTER 3 Gate-last high-κ metal gate MOSFET

It has been a consensus in the research community that high-κ dielectrics require a high temperature anneal to attain a high carrier mobility comparable to the ideal SiO_2/poly-Si case. In this Chapter, this belief is challenged and a record-high electron mobility is demonstrated by utilizing a low thermal budget of gate-last process. This is enabled by a novel Hf-Si electrode proposed in this study.

3.1 Introduction

One of the most attractive characteristics of gate-last process is low thermal budget on high-κ metal gate stacks. Less stringent thermal stability constraints of gate-last process allow dual metal gates which have vacuum work functions corresponding to E_c and E_v for n- and p-MOSFET, respectively [1-4]. Although a significant progress has been made on the control of EWF of high-κ/metal gate stacks, degradation of electron mobility for the high-κ/metal gate stacks still remains as one of the most serious issues [5]. The degradation is attributed to intrinsic properties of high-κ, such as remote-phonons [6] and fixed charges [7], and hence it seems difficult to circumvent this issue. Moreover, it has been reported that dipoles at the SiO_2/high-κ interface, which are useful to adjust EWF of n-MOSFET near E_c, can be an additional source of carrier scattering [8]. Thus, it is a formidable challenge to avoid the mobility degradation and to obtain EWF corresponding to the Si band edge simultaneously by using high-κ metal gate stacks.

After the launch of the first generation high-κ metal gate products [9], researchers in the community have been actively debating the suitable process (gate-first or gate-last) for high-κ metal gate manufacturing mainly from the viewpoint of economics. In this Chapter, the benefit of low thermal budget on high-κ/metal gate stacks in terms of electron mobility is discussed through a systematic study on HfO_2/Hf-Si stacks using gate-last process for the purpose of providing another perspective in the selection of process for the future generation high-κ/metal gate devices.

3.2 Workfunction control for gate-last process

3.2.1 Metal electrode for p-type MOSFET

As reviewed in Chapter 1, an anomalous V_t behavior for high-κ gate dielectrics is unavoidable with gate-first process even in conjunction with thermally stable metal electrodes. This behavior is more pronounced as the workfunction of the metal electrode increases. It is widely accepted to interpret this trend as thermo-dynamical energy gain for the electron transfer from the energy level of oxygen vacancies in a Hf-based high-κ film to a metal electrode, resulting in formation of dipoles at the high-κ metal gate interface, which shift the V_t toward the Si mid-gap. Therefore, a low temperature process should mitigate this effect by suppressing the oxygen vacancy formation. Figure 3-1 summarizes the reported workfunction values for Hf-based high-κ dielectrics with TiN and Ru electrodes as a function of process temperature [10-13].

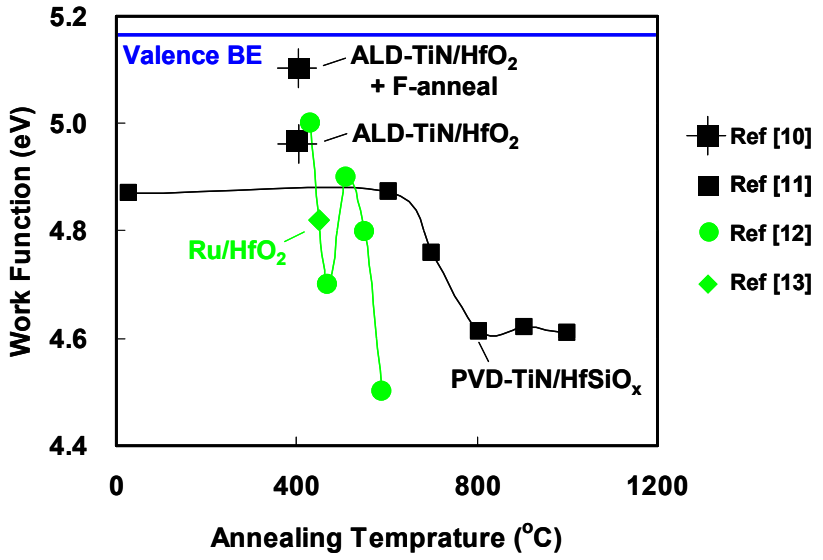


Fig. 3-1 Reported workfunction values for Hf-based high-κ dielectrics with TiN and Ru electrodes as function of process temperature [10-13].

As one can see in Fig. 3-1, reduction of effective workfunction occurs at different temperatures depending on the electrode material. The shift takes place at around 700°C for TiN electrodes, while the change happens at a much lower temperature for Ru electrodes. This trend is in agreement with the energy gain for the electron transfer

from the oxygen vacancies to the electrode [14]. Thus, it is indispensable to limit the post metal thermal budget to approximately 400°C when high workfunction metals such as Ru are employed. This means that care must be taken on thermal budget even with gate-last process. One encouraging trend in Fig. 3-1 is that TiN electrodes can exhibit sufficiently high workfunction for p-type MOSFET depending on deposition methods and post deposition treatments. Incorporation of electron negative species such as oxygen or fluorine may be the key to the high effective workfunction as discussed in [10]. TiN is a commonly used material in CMOS integration and favored in terms of manufacturability. Hence, TiN electrodes with appropriate deposition techniques and post treatments are attractive candidates for p-type MOSFET in gate-last process.

3.2.2 Metal electrode for n-type MOSFET

On the other hand, n-type MOSFETs require metal electrodes with workfunction close to the Si E_c (~ 4.10 eV). The candidates include pure metals such as Ti, Ta, Al, or Hf. However, the pure metals having low workfunction values are known to be highly reactive with the gate dielectrics [15]. The interface reactions between the pure metals and high-κ dielectrics are typically accompanied with severe degradation in insulating properties. One of the effective ways to suppress the interface reaction is to form binary metals by alloying with nitrogen or silicon. Binary metals such as Ti-N, Ta-N, and Ta-Si, have been widely studied for suppressing the reactivity [16-18], however, addition of such stabilizing elements result in increase of workfuction. Therefore, a workfunction value close to the Si E_c has never been reported with this approach.

In this study, we propose a Hf-Si alloy, considering the lower workfunction of Hf compared to previously investigated Ti and Ta. The workfunction setting mechanisms and impacts on electron mobility are discussed through systematic investigations on the HfO_2/Hf-Si stacks.

3.3 Experimental

HfO_2/Hf-Si n-MOSFETs were fabricated using the gate-last process as shown in Fig. 3-2. After a dummy gate removal and a pre-treatment, HfO_2 was deposited by ALD with the thickness ranging from 1.0 to 5.0 nm. The HfO_2 layer must be grown

uniformly at the bottom of the dummy gate whose aspect ratio becomes larger than 1:2 for the sub-50 nm gate length MOSFETs. Therefore ALD, which takes advantage of the surface adsorption rather than the gas phase reaction of the precursor, is the most suitable technique to form high-κ layer for the gate-last process. Then a PDA was performed at 700ºC in an N_2 ambient, followed by a deposition of the Hf-Si. The atomic ratio of the Hf-Si [defined as Si/(Hf+Si)%] was varied in the range between 20 and 80% by a co-sputter physical vapor deposition (PVD) method. The composition of the Hf-Si was analyzed by RBS. Next, the trench was filled with TiN/W for low gate resistivity, followed by CMP. The rest of the process followed a standard back-end-of-line (BEOL) integration flow using non-doped silicate glass (NSG) as inter layer dielectric. A reference n-MOSFET with a conventional SiO_2/n^+poly-Si gate stack was also prepared.

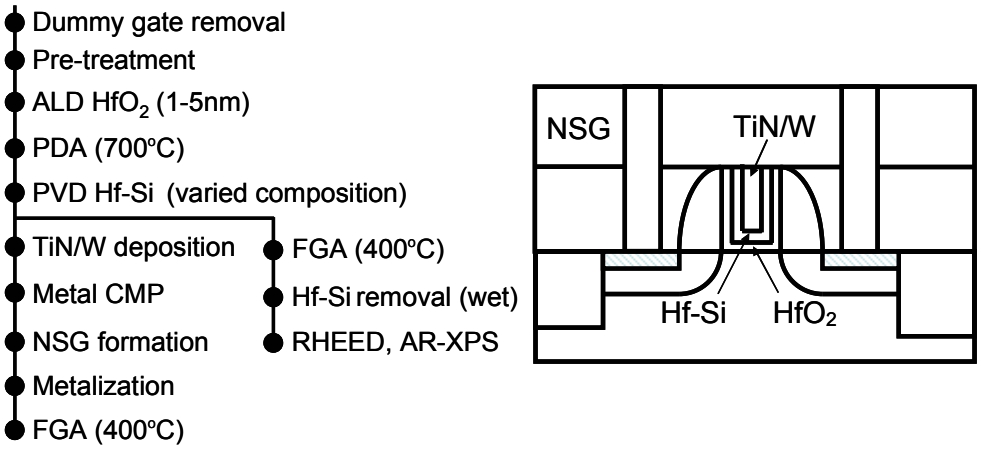


Fig. 3-2 Process flow of gate-last integration and film analysis samples used in this study. The schematics of the final device structure are shown on the right.

The basic gate stack properties were characterized with 10×10 μm^2 nMOSFETs with a substrate doping concentration of $1\times10^{17}/cm^3$, and then the short channel characteristics were obtained with a higher substrate doping concentration with a halo implantation. The samples for physical characterizations of the HfO_2/Hf-Si interface received a forming gas anneal (FGA) at 400ºC after the deposition of the Hf-Si, which simulates the actual thermal budget during the CMOS fabrication. Then, the Hf-Si electrode was removed by wet etching and angle resolved X-ray photoelectron spectroscopy (AR-XPS) was carried out to investigate the interface reactions. The

crystallinity of the HfO_2 was examined by reflection high-energy electron diffraction (RHEED). The depth profile of the crystallinity was studied by repeated RHEED analysis and HF wet etching.

3.4 Results and Discussions

3.4.1 Effective workfunction control of Hf-Si electrode

The composition of the Hf-Si was controlled by changing the ratio of the power applied to a Hf target and a Si target during the co-sputter process. The Si/(Hf+Si) ratio determined by RBS analysis was varied in a wide range (20-80%) with a negligible change in resistivity as shown in Fig. 3-3. The resistivity of the Hf-Si is approximately 2×10^{-4} ohm-cm, which is comparable to heavily doped (to the order of 10^{21} cm^{-3}) n^+poly-Si and p^+poly-Si and acceptable as a gate electrode.

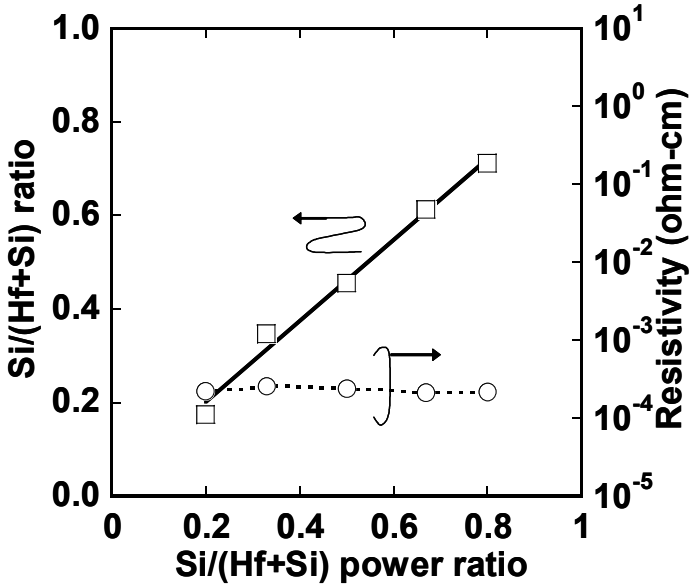


Fig. 3-3 Atomic content of silicon in Hf-Si (square) and resistivity (circle) as function of Si / (Hf + Si) power ratio.

Next, the impact of the composition of the Hf-Si on the V_t of n-MOSFETs was investigated using HfO_2 and SiO_2 as gate dielectrics. Note that the V_t for the heavily doped n^+poly-Si electrode was also obtained so that one can discuss the EWF of the Hf-Si electrode with respect to E_c. Figure 3-4 demonstrates that the V_t

of the Hf-Si electrode can be controlled in the range between the value corresponding to the n^+poly-Si control and the value 0.2 V higher than that.

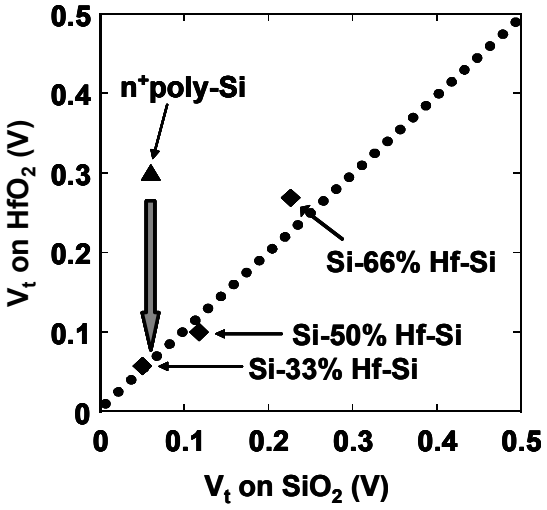


Fig. 3-4 V_t of n-MOSFETs using Hf-Si electrodes on SiO_2 and HfO_2 compared with n^+poly-Si gate.

The EWF of the HfO_2/Hf-Si stack was calculated from the V_t based on the following equations:

$$EWF = \phi_M + \Delta D + \Delta Q_{fix}, \tag{3.1}$$

$$V_t = EWF - \phi_S + 2\varphi_B + \frac{\sqrt{2\varepsilon_S q N_A (2\varphi_B)}}{C_O}, \tag{3.2}$$

where φ_M is the vacuum workfunction of the Hf-Si, ΔD is the contribution from the interface dipoles, ΔQ_{fix} is the contribution from the fixed charges in the gate dielectrics, φ_S is the Fermi level of the Si substrate, ψ_B is the energy difference between the Fermi of the doped Si substrate and the intrinsic Fermi level, ε_S is the permittivity of Si, q is elementary charge, N_A is the doping concentration of the Si substrate, and C_O is the gate oxide capacitance. The EWF was calibrated by adjusting the value of the n^+poly-Si control to 4.10 eV. The EWF values of Si-33% Hf-Si, Si-50% Hf-Si, and Si-66% Hf-Si were calculated to be 4.15, 4.21, and 4.36 eV, respectively. On the other hand, the φ_M values obtained by cutoff energy of X-ray excited secondary electron are 4.10, 4.20, and 4.35 eV, respectively [19]. The comparison between the EWF values derived from the V_t and the φ_M values indicates

that the sum of ΔD and ΔQ_{fix} is negligibly small and the V_t of the HfO_2/Hf-Si stack is controlled dominantly by the φ_M of the Hf-Si electrode. The linear relationship of the V_t for HfO_2 and that for SiO_2 as opposed to the deviated data point for the n^+poly-Si electrode also evidences the absence of the Fermi-level pinning effect for the HfO_2/Hf-Si stack fabricated by gate-last process.

3.4.2 Mobility trend for thick HfO_2 (T_{inv} > 1.6 nm)

Figure 3-5 shows the electron mobility at the effective field (E_{eff}) of 1.0 MV/cm and the hysteresis of the capacitance-voltage (C-V) measurement as a function of physical thickness (T_{phys}) of HfO_2 obtained with the Si-50% Hf-Si electrode. The hysteresis is defined as the flatband voltage (V_{fb}) difference between the up-sweep and the down-sweep of the C-V measurement. The voltage sweep range for each sample was adjusted to the oxide field (E_{ox}) of 5.0 MV/cm. The up-sweep is from the inversion bias (E_{ox} = + 5.0 MV/cm) to the accumulation bias (E_{ox} = - 5.0 MV/cm) and the down-sweep is vice versa. The hysteresis drastically decreased and the electron mobility improved as T_{phys} decreased below the critical value of 2.5 nm.

In order to further elucidate this phenomenon, HfO_2 of T_{phys} = 1.5 nm (Point A in Fig. 3-5), T_{phys} = 2.5 nm (Point B in Fig. 3-5), and T_{phys} = 5.0 nm were analyzed by RHEED as shown in Fig. 3-6. RHEED is sensitive to crystallinity of surface layers and suitable for the analysis of the depth profile of the crystal structure of HfO_2 when performed alternately with wet etching. The uppermost high-κ layers (top-IFL) exhibited halo patterns for all samples. After removing the top-IFL using HF etching, a ring pattern corresponding to a polycrystalline film was observed in Point B and the T_{phys} = 5.0 nm sample whereas Point A still showed a halo pattern. The higher HF etching rate for the bulk portion of Point A also indicates amorphous structure. The thickness of the top-IFL for Point B and the T_{phys} = 5.0 nm sample are approximately 1.0 nm. This portion may be originally crystalline after the PDA but transformed to amorphous by forming $HfSi_xO_y$ due the Si diffusion from the Hf-Si electrode as illustrated in Fig. 3-6. This effect can be accelerated by employing a Si-rich Hf-Si electrode as discussed later. The ring pattern for the bulk portion of Point B and the T_{phys} = 5.0 nm sample was assigned to the monoclinic-HfO_2 (m-HfO_2). The wet etching rate for this portion substantially decreased compared to the amorphous portion. The increase of hysteresis by crystallization [amorphous-HfO_2 (a-HfO_2)

(point A): 2.6 mV, m-HfO_2 (point B): 42.9 mV] is much larger than the expected difference from the T_{phys} values, which accounts for only 2.8× increase assuming uniform distribution of trapped charges in the bulk HfO_2. In addition, the V_t dependence of the HfO_2/Hf-Si n-MOSFETs on the T_{phys} of HfO_2 suggests generation of additional fixed charges localized at the SiO_2/HfO_2 interface upon crystallization (this trend will be discussed more in detail in Chapter 5). Both of these factors can explain the crystallization-induced mobility degradation. Our systematic study shows that both contributions can be dramatically reduced by reducing the HfO_2 thickness below the critical thickness for crystallization and hence extremely high electron mobility is attainable even with a direct current (DC) characterization method.

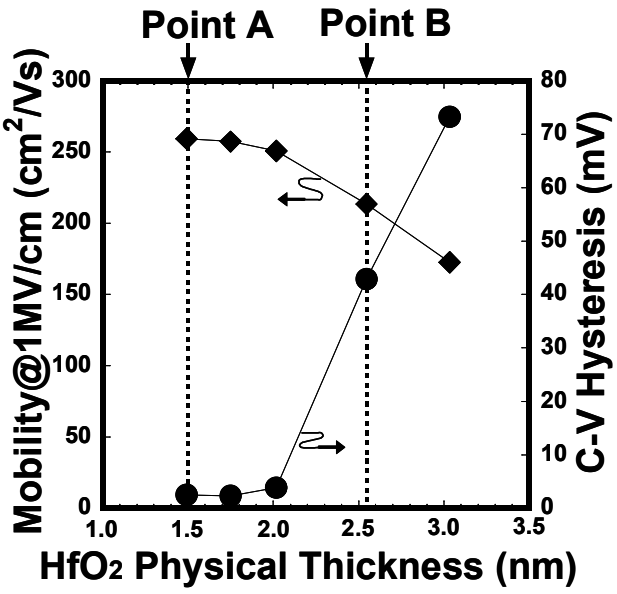


Fig. 3-5 Electron mobility at E_{eff} = 1 MV/cm and C-V hysteresis as function of HfO_2 thickness. Point A and B were analyzed by RHEED.

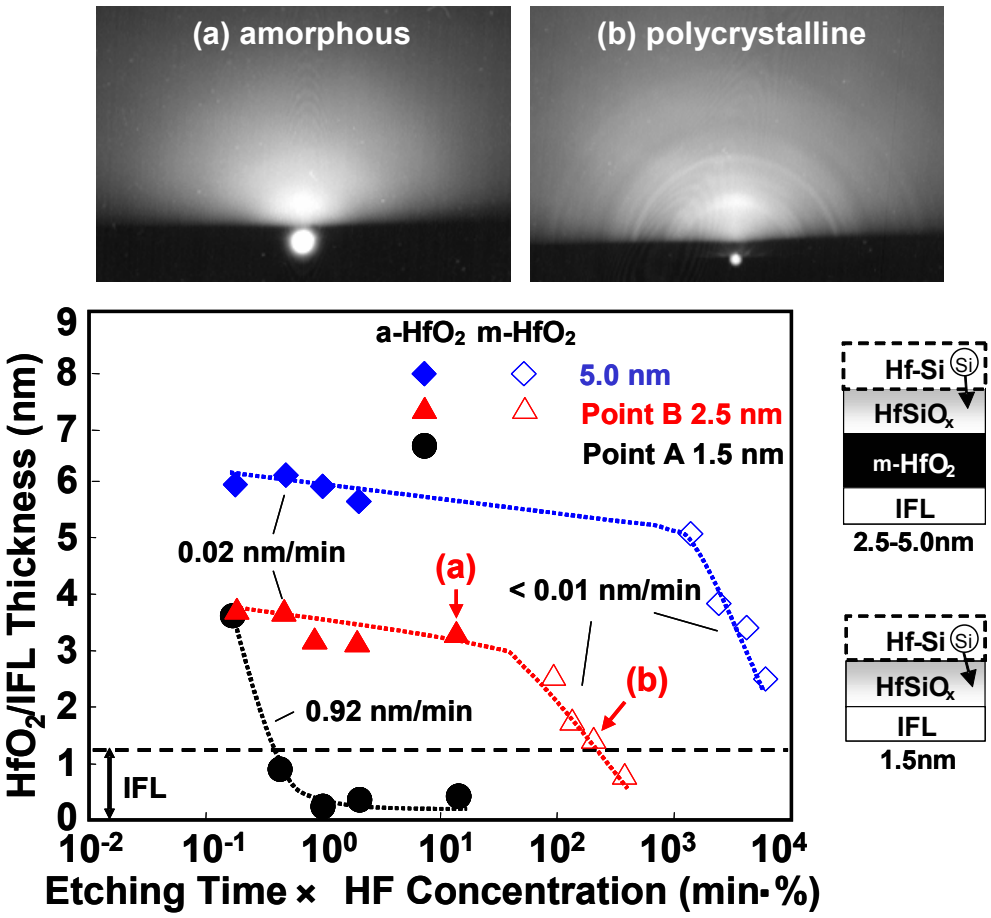


Fig. 3-6 Physical thickness of IFL/HfO_2 stacks obtained by elipsometer as function of product of etching time and HF concentration. The initial HfO_2 thicknesses are 1.5 nm (Point A), 2.5 nm (Point B), and 5.0 nm. The y-axis includes the IFL thickness in addition to the remaining HfO_2 thickness after the wet etching. The wet etching rates for 10% HF are shown in the figure. The RHEED patterns corresponding to data point (a) and (b) are shown on the top. The closed symbols correspond to a-HfO_2 and the open symbols correspond to m-HfO_2 based on RHEED.

3.4.3 Mobility trend for thin HfO_2 (T_{inv} < 1.6 nm)

Next, a further T_{inv} scaling was performed by changing the composition of the Hf-Si. Figure 3-7 compares the electron mobility for the Si-55%, Si-50%, and Si-33% Hf-Si as a function of E_{eff}. The drive current was calculated as the average of the source current (I_s) and the drain current (I_d) in order to exclude the measurement error caused by the gate current (I_g). For this comparison, the devices showing $I_g < 1\times10^{-6}$ A are chosen so that the I_s and I_d are at least one order of magnitude higher than the I_g. The mobility curve for the SiO_2/n^+poly-Si is also shown as a control.

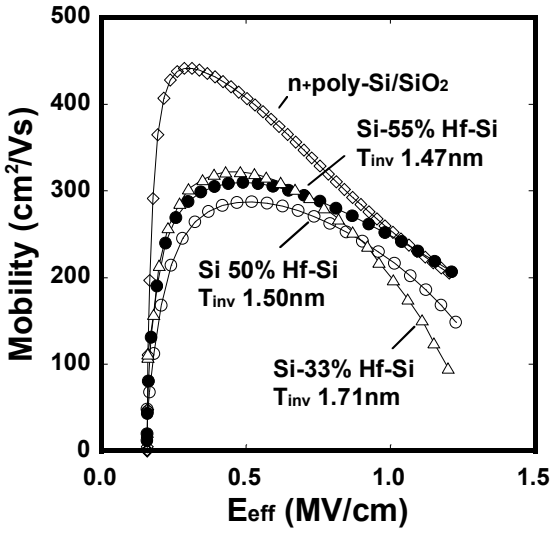


Fig. 3-7 Comparison of effective electron mobility of HfO_2/Si-33%, Si-50%, and Si-55% Hf-Si. The mobility curve for the SiO_2/n^+poly-Si is shown as a reference.

Another mobility degradation mode, which is highly sensitive to the metal composition, is clearly seen in the high E_{eff} regime. The mobility degradation in the middle E_{eff} (~ 0.5 MV/cm) compared to the SiO_2/n^+poly-Si control is attributable to the remote Coulomb and/or phonons scattering which is intrinsic to high-κ [5]. It should be noted that the HfO_2/Si-55% Hf-Si can be scaled down to T_{inv} = 1.47 nm with negligible mobility degradation in the high E_{eff} region. The improvement of the high E_{eff} mobility for the Si-55% Hf-Si indicates that carrier scattering mechanisms inherent to high-κ are not significant in the E_{eff} regime corresponding to the operating voltage (E_{eff} = 1 MV/cm corresponds to V_g = 1V) and it is indeed possible to avoid the mobility degradation from the ideal SiO_2/n^+poly-Si with the optimized metal gate high-κ process. Figure 3-8 shows the gate leakage current density (J_g) at E_{ox} = 4.5 MV/cm as a function of T_{inv}. The trend line for each Hf-Si composition was obtained by changing the thickness of HfO_2. The J_g should go up toward the point that corresponds to the bottom-IFL alone as HfO_2 thickness decreases. Therefore, the J_g at the extremely scaled T_{inv} is related to the thickness and quality of the bottom-IFL. The as-grown bottom-IFL thickness is shown as the vertical line in Fig. 3-8. The sharp increase of the J_g for the Si-33% Hf-Si indicates that the bottom-IFL is converted to $HfSi_xO_y$ due to the metal diffusion from the electrode as evidenced by the physical characterization data in the next section. The reduction of J_g from the

SiO_2/n^+poly-Si trend line is more than six orders of magnitude at T_{inv} = 1.47nm for the HfO_2/ Si-55% Hf-Si.

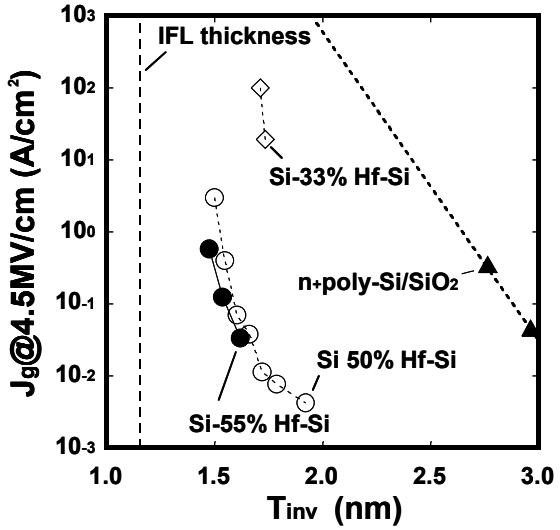


Fig. 3-8 J_g-T_{inv} characteristics of HfO_2/Hf-Si with varied electrode compositions. The J_g values were taken at E_{ox} = 4.5 MV/cm. The as-grown bottom-IFL thickness is shown as the vertical line.

3.4.4 Interface reactions of HfO_2/Hf-Si and electrical impacts

The impact of the composition of the Hf-Si on the film properties of the underlying HfO_2 was investigated in order to understand the trend of electrical characteristics described in the previous sub-section. The depth profiles of the Si 2p spectra from the high-κ layers were compared by AR-XPS after removing the Si-55% Hf-Si electrode as shown in Fig. 3-9. The chemical shift component corresponding to $HfSi_xO_y$ (the peak around 103 eV) increased for the surface-sensitive condition ($\theta = 30^o$), indicating $HfSi_xO_y$ formation at the HfO_2/Hf-Si interface induced by Si diffusion from the Si-55% Hf-Si. On the contrary, no clear sign of $HfSi_xO_y$ formation was observed for the Si-33% Hf-Si electrodes (not shown).

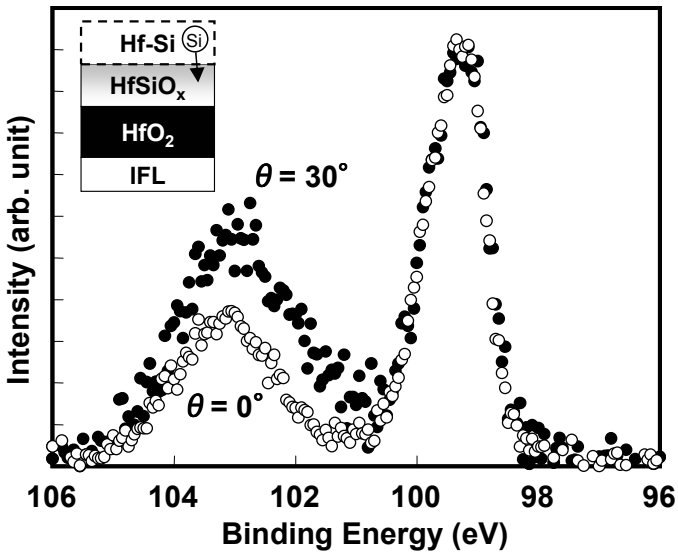


Fig. 3-9 Si 2p spectra of high-k film after removal of Si-55% Hf-Si electrode obtained by AR-XPS. The take off angles (θ) of the AR-XPS are 0 and 30^o.

Figure 3-10 shows the TEM images of the HfO_2/Si-33% and Si-55% Hf-Si. In the Si-33% Hf-Si case, the bottom-IFL completely disappeared, due to the Hf penetration from the electrode, whereas the bottom-IFL of the HfO_2/Si-55% Hf-Si was intact. In addition, lattice fringes were observed in the HfO_2 layer for the Si-33% Hf-Si case indicating a local crystallization. On the basis of these findings, the mobility degradation in the high E_{eff} region (Fig. 3-7) is attributable to the surface roughness scattering triggered by the local penetration of Hf atoms into the bottom-IFL and/or by the local crystallization of the HfO_2 induced by a higher Hf concentration for the Si-33% Hf-Si electrode. It should be noted that a smooth interface can be preserved by taking advantage of the Si diffusion effect from the Si-55% Hf-Si electrode, and therefore the high field mobility is maintained as high as that of SiO_2/n^+poly-Si even for a sub-1nm EOT device.

Figure 3-11 summarizes the impacts of the crystallization and the $HfSi_xO_y$ formation on the C-V hysteresis characteristics. Here, the C-V hysteresis is plotted as a function of the physical thickness of HfO_2 (T_{phys}) for the Si-50% and Si-55% Hf-Si electrode. The dotted arrow indicates the improvement of the C-V hysteresis by the transformation from the m-HfO_2 into the amorphous-HfO_2, which was confirmed by the RHEED analysis. In addition, the improvement from the formation of $HfSi_xO_y$ at the HfO_2/Hf-Si interface, which was detected by XPS, is highlighted by the solid

arrow. The reduction of the hysteresis by the Si diffusion effect is approximately 60%.

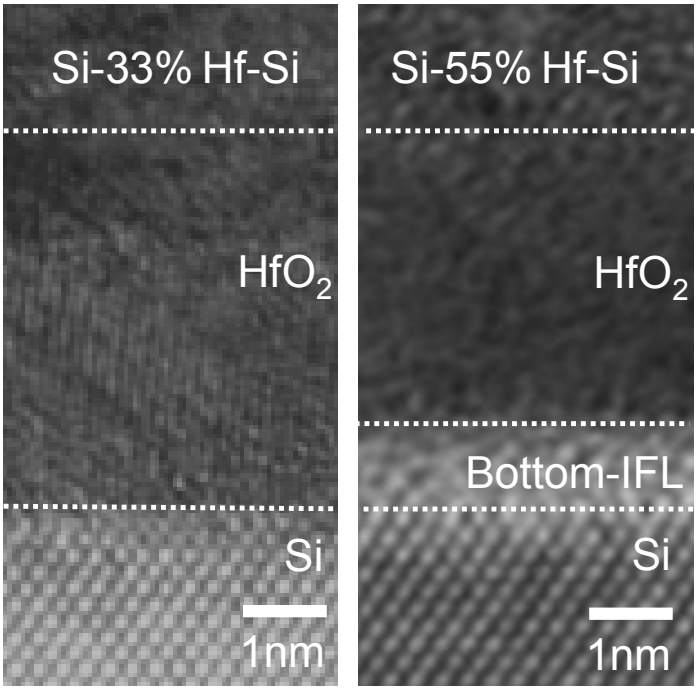


Fig. 3-10 TEM images of HfO_2/Si-33% Hf-Si (left) and HfO_2/Si-55% Hf-Si (right). The bottom-IFL disappeared in the Si-33% case. The estimated interface positions are shown with broken lines based on as-deposited elipsometer thickness.

These physical and electrical trends of the HfO_2/Hf-Si gate stacks can be consistently explained by assuming the contribution of oxygen vacancies. It was reported that an empty oxygen vacancy (V_o^{2+}) in HfO_2-based high-κ creates a gap state just below E_c, which is responsible for trap-assisted electron current as well as charge trapping [20]. It was also reported that the concentration of V_o^{2+} can be reduced by lowering the Hf concentration in the dielectric [21]. Thus, the suppression of J_g (Fig. 3-8) and the improvement of the hysteresis (Fig. 3-11) by the Si-55% Hf-Si can be understood as the reduction of the concentration of V_o^{2+} by means of the Si diffusion effect from the electrode. Also, the drastic increase of the hysteresis for the thick HfO_2 (Figs. 3-5 and 3-11) is attributable to the generation of V_o^{2+} promoted by the crystallization [22].

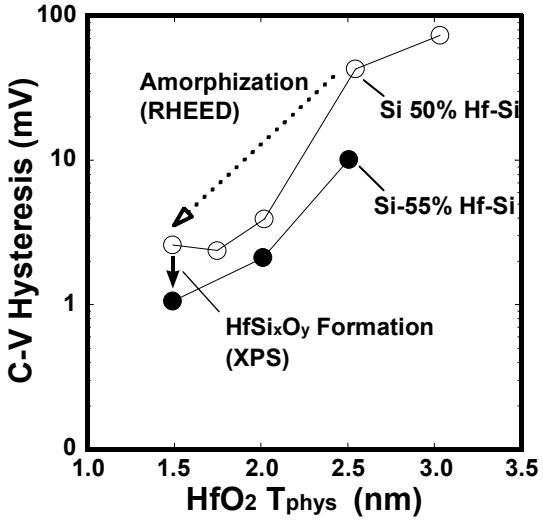


Fig. 3-11 C-V hysteresis as function of HfO_2 thickness (T_{phys}). The dotted arrow indicates the amorphization and the solid arrow indicates the $HfSi_xO_y$ formation.

These physical and electrical trends of the HfO_2/Hf-Si gate stacks can be consistently explained by assuming the contribution of oxygen vacancies. It was reported that an empty oxygen vacancy (V_o^{2+}) in HfO_2-based high-κ creates a gap state just below E_c, which is responsible for trap-assisted electron current as well as charge trapping [20]. It was also reported that the concentration of V_o^{2+} can be reduced by lowering the Hf concentration in the dielectric [21]. Thus, the suppression of J_g (Fig. 3-8) and the improvement of the hysteresis (Fig. 3-11) by the Si-55% Hf-Si can be understood as the reduction of the concentration of V_o^{2+} by means of the Si diffusion effect from the electrode. Also, the drastic increase of the hysteresis for the thick HfO_2 (Figs. 3-5 and 3-11) is attributable to the generation of V_o^{2+} promoted by the crystallization [22].

3.4.5 Application of Si-rich Hf-Si electrode to short channel device

Since the HfO_2/Hf-Si gate stack using the Si diffusion effect can prevent the mobility degradation at T_{inv} = 1.47 nm and also the steep increase of J_g, short channel devices were fabricated with this gate stack. The long channel V_t of the optimized HfO_2/Hf-Si for the substrate doping of 1×10^{17} cm^{-3} was 0.036 V compared to 0.050 V for the control SiO_2/n^+poly-Si, which corresponds to EWF of 4.14 eV based on the calculation discussed in §3.4.1. The V_t roll-off characteristics at V_{dd} = 1.0 V for two different dosages of channel ion implantation (I/I) are shown in Fig. 3-12. Low V_t

values, which are suitable for a high performance logic LSI, were maintained down to a 45nm gate length thanks to the near band-edge EWF of the Hf-Si.

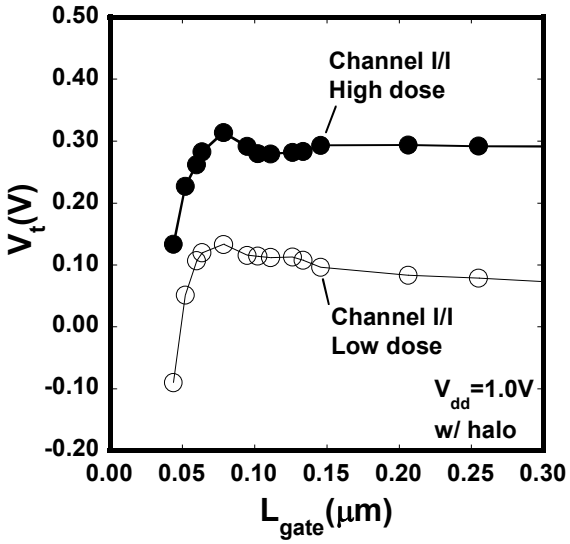


Fig. 3-12 V_t roll-off characteristics of n-MOSFET with HfO_2/Si-55% Hf-Si at V_{dd} = 1.0 V. High and low channel ion implantation (I/I) conditions are compared.

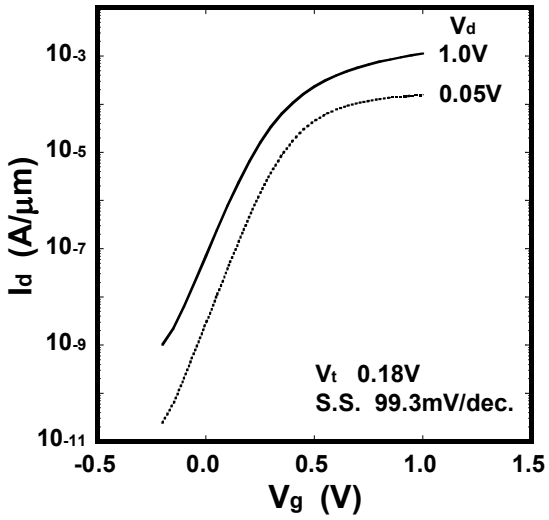


Fig. 3-13 I_d-V_g characteristics of 45nm gate n-MOSFET with HfO_2/Si-55% Hf-Si.

Figure 3-13 shows the I_d-V_g characteristics of the 45nm gate n-MOSFET. A low V_t of 0.18V and an excellent sub-threshold slope (SS) of 99.3 mV/decade was demonstrated by the optimization of the Hf-Si composition which preserves the high quality bottom-IFL. The on-current (I_{on}) vs off-current (I_{off}) characteristics obtained at supply voltage (V_{dd}) = 1.0 V are shown in Fig. 3-14.

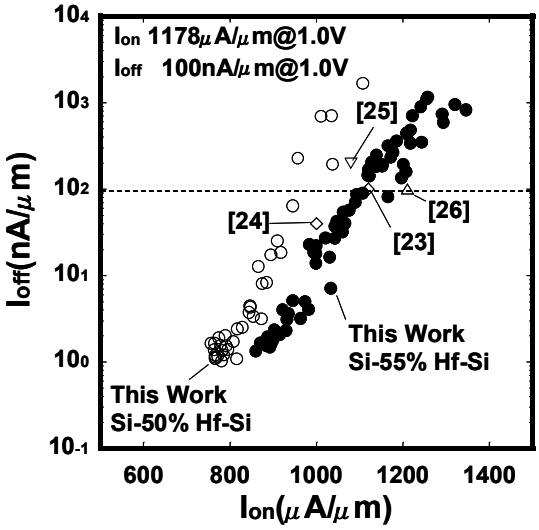


Fig. 3-14 I_{on}-I_{off} characteristics of HfO_2/Si-55% Hf-Si at V_{dd} = 1.0 V in comparison with other works [23-26].

The I_{on} was improved by 23% with the Si-55% Hf-Si compared to the Si-50% Hf-Si owing to additional T_{inv} scaling without mobility degradation. The I_{on} of 1178 uA/um (I_{off} 100 nA/um) is comparable to those of the 65nm-node high performance nMOSFETs with SiO_xN_y /poly-Si gate stacks [23-26] despite lack of strain enhanced technologies. The device performance compared with [23] and [26] is summarized in Table 3-1.

A further performance boost is expected when the Hf-Si/HfO_2 gate stack is combined with stress elements such as a tensile stress liner technology [27]. This is a clear demonstration of the performance advantage of metal gate/high-κ over conventional gate stacks when the EWF is controlled close to the Si band edge at no expense of the high field carrier mobility.

Table 3-1 Summary of device performance compared with 65-nm-node high performance n-MOSFETs.

	This work	Ref. 23	Ref. 26
L_g (nm)	45	37	35
T_{inv} (nm)	1.47	1.89	-
V_{dd} (V)	1.0	1.0	1.0
I_{on} (μA/μm)	1165	1120	1210
I_{off} (nA/μm)	81	100	100
Stressor effect (%)	Not used	+15	+40

3.5 Summary

The RHEED, AR-XPS, and TEM analyses revealed that the crystallization of HfO_2 and the metal diffusion into the bottom-IFL are the primary sources of mobility degradation. It was found that these degradation modes can be avoided by the careful optimization of the HfO_2 thickness below the critical value and by the Si-rich Hf-Si electrode. Moreover, the EWF of the optimized HfO_2/Hf-Si gate stack is located within 50 mV from the Si E_c. Based on these findings, we succeeded in scaling the T_{inv} of n-MOSFET down to 1.47 nm without degradation of the high field mobility. Finally, the performance advantage of the optimized HfO_2/Hf-Si gate stack over conventional SiO_xN_y/poly-Si gate stacks was demonstrated with the 45-nm-gate n-MOSFET.

The findings in this Chapter suggest that EWF can be controlled predominantly by the vacuum workfunction of the metal electrode in gate-last process if an appropriate material is employed. In addition, the low thermal budget of gate-last process enables us to keep the HfO_2 dielectrics amorphous after the whole integration process. The implication of these factors on the carrier mobility will be discussed in comparison with gate-first process in Chapter 5.

Reference

[1] T. Hirano, T. Ando, K. Tai, S. Yamaguchi, T. Kato, S. Hiyama, Y. Hagimoto, S. Takesako, N. Yamagishi, K. Watanabe, R. Yamamoto, S. Kanda, S. Terauchi, Y. Tateshita, Y. Tagawa, H. Iwamoto, M. Saito, S. Kadomura, N. Nagashima: Tech. Dig. Int. Electron Devices Meet., 2005, p. 911.

[2] T. Ando, T. Hirano, K. Tai, S. Yamaguchi, T. Kato, Y. Hagimoto, K. Watanabe, R. Yamamoto, S. Kanda, K. Nagano, S. Terauchi, Y. Tateshita, Y. Tagawa, M. Saito, H. Iwamoto, S. Yoshida, H. Watanabe, N. Nagashima, S. Kadomura: Tech. Dig. VLSI Symposium, 2006, p.208.

[3] S. Yamaguchi, K. Tai, T. Hirano, T. Ando, S. Hiyama, J. Wang, Y. Hagimoto, Y. Nagahama, T. Kato, K. Nagano, M. Yamanaka, S. Terauchi, S. Kanda, R. Yamamoto, Y. Tateshita, Y. Tagawa, H. Iwamoto, M. Saito, N. Nagashima, S. Kadomura: Tech. Dig. VLSI Symp., 2006, p. 192.

[4] K. Tai, T. Hirano, S. Yamaguchi, T. Ando, S. Hiyama, J. Wang, Y. Nagahama, T. Kato, M. Yamanaka, S. Terauchi, S. Kanda, R. Yamamoto, Y. Tateshita, Y. Tagawa, H. Iwamoto, M. Saito, N. Nagashima, S. Kadomura: Tech. Dig. ESSDERC, 2006, p. 121.

[5] S. Saito, D. Hisamoto, S. Kimura, M. Hiratani: Tech. Dig. Int. Electron Devices Meet., 2003, p. 797.

[6] M. Fischetti, D. Neumayer, E. Cartier: J. Appl. Phys. **90** (2001) 4587.

[7] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, H. Satake, N. Fukushima: Tech. Dig. Int. Electron Devices Meet., 2002, p. 621.

[8] H. Ota, A. Hirano, Y. Watanabe, N. Yasuda, K. Iwamoto, K. Akiyama, K. Okada, S. Migita, T. Nabatame, A. Toriumi: Tech. Dig. Int. Electron Devices Meet., 2007, p. 65.

[9] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M.Buehler, A. Cappelani, R. Chau, C. H. Choi, G. Ding, K. Fischer, T.Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, D. Huessner, D. Ingerley, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liy, B. McIntyre, P. Moon, J. Neiynck, C. Parker, D.Parsons, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L.Schifren, J. Sebastian, J. Seiple, D. Simon, S.Sivakumar, P. Smith, C.

Thomas, T. Troeger, P. Vanderyoon, S. Williams, and K. Zawadzi: Tech. Dig. Int. Electron Devices Meet., 2007, p. 247.

[10] K. Tai, S. Yamaguchi, K. Tanaka, T. Hirano, I. Oshiyama, S. Kazi, T. Ando, M. Nakata, M. Yamanaka, R. Yamamoto, S. Kanda, Y. Tateshita, H. Wakabayashi, Y. Tagawa, M. Tsukamoto, H. Iwamoto, M. Saito, N. Nagashima, S. Kadomura: Jpn. J. Appl. Phys. **47** (2008) 2345.

[11] K. Takahashi, K. Manabe, A. Morioka, T. Ikarashi, T. Yoshihara, H. Watanabe, T. Tatsumi: Jpn. J. Appl. Phys. **44** (2005) 2210.

[12] M. Tapajna, K. Cico, R. Luptak, K. Husekova, K. Frohlich, L. Harmmatha, J. C. Hooker, F. Roozeboom: Tech. Dig. ASDAM, 2004, p.167.

[13] H. C. Wen, K. Choi, P. Lysaght, P. Majhi, H. Alshareef, C. Huffman, R. Harris, H. Luan, B. H. Lee, N. Yamada, S. Wickramanayaka: Tech. Dig. VLSA-TSA, 2005, p.107.

[14] K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Kohno, T. Chikyo, H. Kitajima, T. Arikada: Tech. Dig. VLSI Symp., 2004, p. 108.

[15] Y. Akasaka, K. Miyagawa, A. Kariya, H. Shoji, T. Aoyama, S. Kume, M. Shigeta, O. Ogawa, K. Shiraishi, A. Uedono, K. Yamabe, T. Chikyow, K. Nakajima, M. Yashuhira, K. Yamada, and T. Arikado: Ext. Abst. SSDM, 2004, p.196.

[16] S. Datta, G. Dewey, M. Doczy, B.S. Doyle, B. Jin, J. Kavalieros, R. Kotlyar, M. Metz, N. Zelickand, R. Chau: Tech. Dig. Int. Electron Devices Meet., 2003, p.653.

[17] R. Choi, K. Onishi, C. S. Kang, S. Gopalan, R. Nieh, Y. H. Kim, J. H. Han, S. Krishnan, H. Cho, A. Shahriar, J. C. Lee: Tech. Dig. Int. Electron Devices Meet., 2002, p.613.

[18] Y. Akasaka, K. Miyagawa, T. Sasaki, K. Shiraishi, S. Kamiyama, O. Ogawa, F. Ootsuka, Y. Nara: Tech. Dig. VLSI, 2005, p.228.

[19] T. Ando, T. Shimura, H. Watanabe, T. Hirano, S. Yoshida, K. Tai, S. Yamaguchi, H. Iwamoto, S. Kadomura, S. Toyoda, H. Kumigashira, M. Oshima: Appl. Phys. Express **2** (2009) 071402.

[20] K. Torii, K. Shiraishi, S. Miyazaki, K. Yamabe, M. Boero, T. Chikyow, K. Yamada, H. Kitajima, T. Arikado: Tech. Dig. Int. Electron Devices Meet., 2004, p. 129.

[21] M. Sato, Y. Nakasaki, K. Watanabe, T. Aoyama, E. Hasegawa, M. Koyama, K. Sekine, K. Eguchi, M. Saito, T. Tsunashima: Tech. Dig. Int. Electron Devices Meet., 2006, p. 243.

[22] S. Migita, Y. Watanabe, H. Ota, H. Ito, Y. Kamimuta, T. Nabatame, A. Toriumi: Tech. Dig. VLSI Symp., 2008, p. 152.
[23] K. Goto, S. Satoh, H. Ohta, S. Fukuta, T. Yamamoto, T. Mori, Y. Tagawa, T. Sakuma, T. Saiki, Y. Shimamune, A. Katakami, A. Hatada, H. Morioka, Y. Hayami, S. Inagaki, K. Kawamura, Y. Kim, H. Kokura, N. Tamura, N. Horiguchi, M. Kojima, T. Sugii, K. Hashimoto: Tech. Dig. Int. Electron Devices Meet., 2004, p. 209.
[24] C. Sung, H. Yin, H. Ng, K. Saenger, V. Chan, S. Crowder, J. Li, J. Ott, R. Bendernagel, J. Kempisty, V. Ku, H. Lee, Z. Luo, A. Madan, R. Mo, P. Nguyen, G. Pfeiffer, M. Raccioppo, N. Rovedo, D. Sadana, J. Souza, R. Zhang, Z. Ren, C. Wann: Tech. Dig. Int. Electron Devices Meet., 2005, p. 243.
[25] M. Horstmann, A. Wei, T. Kammler, J. Höntschel, H. Bierstedt, T. Feudel, K. Frohberg, M. Gerhardt, A. Hellmich, K. Hempel, J. Hohage, P. Javorka, J. Klais, G. Koerner, M. Lenski, A. Neu, R. Otterbach, P. Press, C. Reichel, M.Trentsch, B. Trui, H. Salz, M. Schaller, H.-J. Engelmann, O. Herzog, H. Ruelke, P. Hübler, R. Stephan, D. Greenlaw, M. Raab, N. Kepler: Tech. Dig. Int. Electron Devices Meet., 2005, p. 233.
[26] S. Tyagi, C. Auth, P. Bai, G. Curello, H. Deshpande, S. Gannavaram, O. Golonzka, R. Heussner, R. James, C. Kenyon, S-H Lee, N. Lindert, M. Liu, R. Nagisetty, S. Natarajan, C. Parker, J. Sebastian, B. Sell, S. Sivakumar, A. St Amour, K. Tone: Tech. Dig. Int. Electron Devices Meet., 2005, p. 1070.
[27] S. Mayuzumi, J. Wang, S. Yamakawa, Y. Tateshita, T. Hirano, M. Nakata, S. Yamaguchi, Y. Yamamoto, Y. Miyanami, I. Oshiyama, K. Tanaka, K. Tai, K. Ogawa, K. Kugimiya, Y. Nagahama, Y. Hagimoto, R. Yamamoto, S. Kanda, K. Nagano, H. Wakabayashi, Y. Tagawa, M. Tsukamoto,H. Iwamoto, M. Saito, S. Kadomura, N. Nagashima: Tech. Dig. Int. Electron Devices Meet., 2007, p. 293.

CHAPTER 4 Gate-first high-κ metal gate MOSFET

Oxygen vacancies in a Hf-based high-κ dielectric have been considered as a source of all undesired electrical characteristics. This is the case especially among the researchers working on gate-first process. In this Chapter, a new oxygen transport phenomenon, which is closely related with the oxygen vacancies, is explored. By positively utilizing the presence of the oxygen vacancies, a powerful and practical EOT scaling technique is established. This technique opens up a pathway to EOT scaling toward the end of the CMOS roadmap.

4.1 Introduction

Improvement of CMOS performance by L_g scaling has been reported for a gate-first high-κ/metal gate process [1]. Continued L_g scaling beyond the 22 nm node requires EOT < 6Å to suppress short-channel effects. EOT scaling with a gate-first process is hampered by interfacial layer (IL) growth during high-temperature processes. Considering the maturity of Hf-based high-κ gate dielectrics, elimination of the low-κ IL in conjunction with the Hf-based high-κ appears to be the most practical approach to meet the requirements for the 22nm node and beyond.

Several techniques going in this direction have been reported [2-6]; however, they require direct modifications of high-κ dielectrics and the adverse effects are not fully understood. In this Chapter, we introduce a new concept of remote IL scavenging and its advantages over conventional IL scavenging schemes are discussed. The concept of the remote IL scavenging is illustrated in Fig. 4-1 in contrast with other published IL scavenging schemes. The prior publications on IL scavenging use direct doping of the scavenging metal into the high-κ dielectrics to promote the reaction with the IL. In this case, V_t shift due to additional charge generation and/or degradation of interface properties have been reported. Metal-gate-induced IL scavenging using a TaN-M alloy has been previously reported [6]. This scheme is still considered as direct scavenging because the scavenging element (M) diffuses into the high-κ dielectrics after the high temperature activation anneal. On the other hand, the remote IL scavenging is brought about by doping a TiN gate electrode with scavenging elements at a certain isolation from the high-κ/TiN interface. We shed light on the kinetics of this reaction.

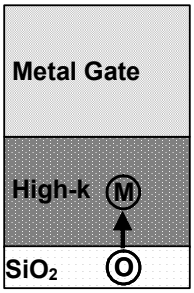
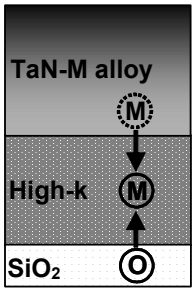
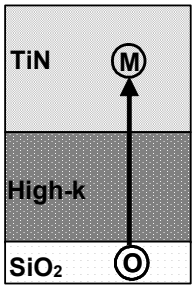
Type	Direct		Remote
Scavenging element (M)	Within or in contact with High-κ		Isolated from High-κ
Schematics			
Ref.	(2-5)	Previous work (6)	This work

Fig. 4-1 Schematics of direct and remote IL scavenging. The scavenging metal is isolated from high-κ in the remote case.

Another important aspect is the V_t control for CMOS compatibility. Previously, La and Al incorporation for the V_t adjustment of n- and p- field-effect-transistors (FETs) have been demonstrated with gate-first process [7, 8]. Yamamoto et al. found that the V_t change originates from dipole layers at the SiO_2/high-κ interface [9]. The high-κ metal gate stacks with multiple V_t values are attainable by employing different thicknesses of dipole layers, however, exposing high-κ to wet chemicals multiple times poses grave concerns in reliability and manufacturability. Therefore, a V_t control technique, which does not require exposure of high-κ, is highly anticipated. TaC is one of the promising candidates for metal gate and the EWF tuning capability via the film composition change using different deposition processes has been reported [10, 11]. Film transformation after the TaC deposition is preferred in terms of process simplicity, however, the feasibility has never been discussed with electrical data.

In this Chapter, we demonstrate modulation of La-induced V_{fb} shift by means of post metal anneal treatment on TaC electrodes, which opens up another knob for EWF control. In view of V_t control in the future node, we discuss the compatibility of the IL scaling and the La and Al induced dipoles.

4.2 Experimental

4.2.1 EWF control experiment

We fabricated MOS capacitors on n-type Si (100) as shown in Fig. 4-2. After IL preparation and HfO_2 deposition, a La cap layer was deposited. Next, TaC was deposited with various thicknesses (TaC1<TaC2) by reactive physical vapor deposition, followed by post metal nitridation (PMN) using rapid thermal anneal at 700-900°C under an NH_3 ambient. RBS shows that the Ta/(Ta+C) ratio of the as-deposited film is 0.512 and is barely affected by the PMN. On the other hand, it is found by nuclear reaction analysis (NRA) that N/(C+N) can be widely varied from 0.015 (as-deposited) to 0.569/0.612 (700/800°C) by the PMN. Then, a cap metal layer and a poly-Si film were deposited. The rest of the process flow simulates gate-first process. Finally, C-V measurement, TEM, electron energy loss spectroscopy (EELS), and SIMS were carried out.

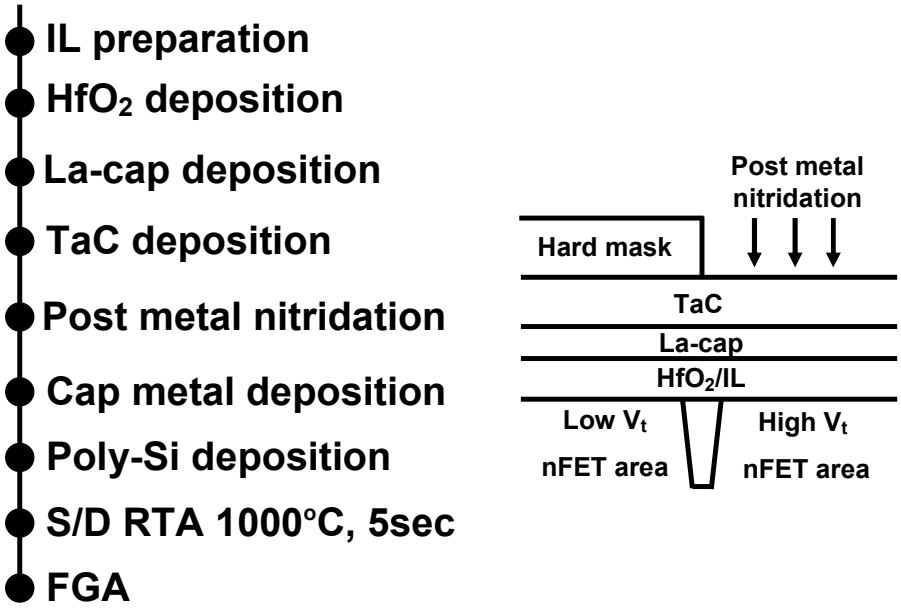


Fig. 4-2 Process flow and schematics for V_{fb} control experiment.

4.2.2 EOT scaling experiment

We fabricated 10×10 μm^2 FETs and MOS capacitors with high-κ/metal gate stacks using a gate-first process as shown in Fig. 4-3. After SiO_2 IL preparation and HfO_2 deposition, cap layers (La or Al) were employed for some samples for V_t adjustment. Next, TiN films were deposited as metal electrodes and then scavenging

elements (M1, M2, and M3) were doped in the TiN while maintaining an undoped high-κ/TiN interface. In the control samples, TiN-M3 and TaN-M3 alloy films were deposited to let M3 elements directly contact high-κ layers. The high-κ/metal gate stacks were capped with poly-Si followed by a conventional self-aligned CMOS process using a 1000°C rapid thermal annealing (RTA). The cap layers diffuse through the HfO_2 into the underlying SiO_2 during the high temperature annealing to form interface dipoles.

For the fabrication of MOS capacitors, after the poly-Si deposition, RTA treatments were performed at 600-1000℃ (N_2 ambient, 5 s) followed by Ni sputtering and a RTA at 500℃ (N_2 ambient, 30 s) in that order to form Ni silicide gates. In addition, electrical measurement was performed on the MOS capacitors with HfO_2/TiN stacks capped with 40-nm-thick TiN layers after 400℃ anneal (N_2 ambient, 30 min). Thus, the maximum process temperature was varied in the range between 400 and 1000℃.

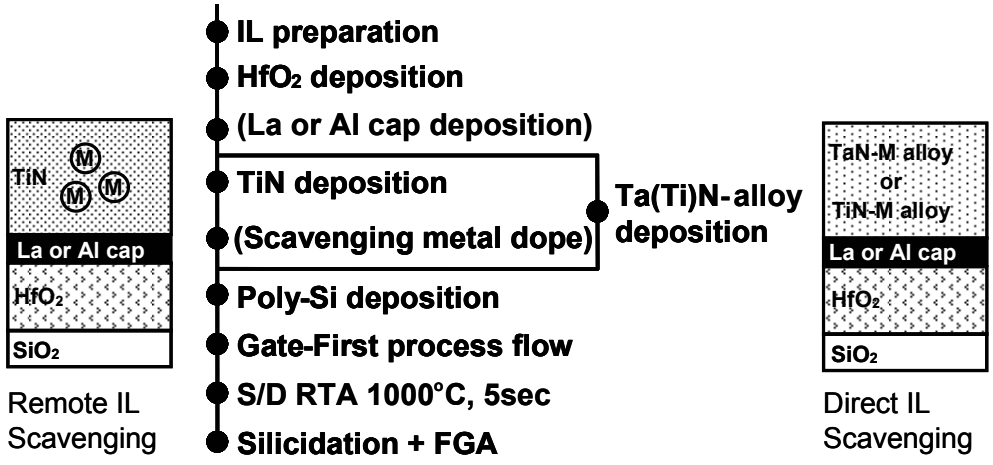


Fig. 4-3 Process flow for EOT scaling experiment. The schematics for the remote IL scavenging (left) and the direct IL scavenging (right) are shown.

TEM, EELS, and SIMS analyses were performed after the whole process. The EOT numbers were extracted from accumulation CV measurement on 10×10 μm^2 n-type and p-type MOS capacitors with an N_{sub} of 5×10^{15} cm^{-3} using Hauser's fitting model [12]. Mobility characterization was carried out on 10×10 μm^2 n-type and p-type FETs with an N_{sub} of 1×10^{17} cm^{-3} using current-voltage (I-V) and split-C-V method at a drain voltage bias of 50 mV.

4.3 EWF control via post metal anneal

Fig. 4-4 (a, b) show the TEM image of the high-κ/TaC stack and the EELS depth profiles for N, C, and O. The depth profiles of N demonstrate that the N/(C+N) ratio at the high-κ/TaC interface is successfully modulated by PMN 700°C.

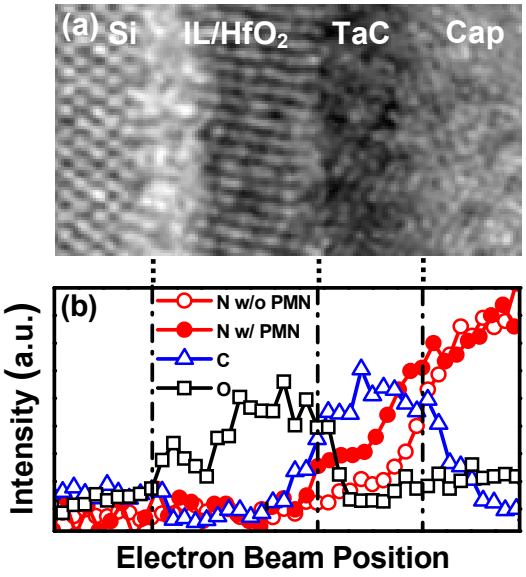


Fig. 4-4 (a) TEM image after full process (b) EELS of N (w/ and w/o PMN 700°C), C, and O.

Fig. 4-5 (a) compares C-V curves for different TaC thicknesses (TaC1 < TaC2) and PMN temperatures (700-800°C) using SiO_2 IL. The La cap provides -380mV shift resulting in an EWF close to the nFET band-edge (BE). When the PMN is performed on TaC1, +231mV shift is obtained independent of the PMN temperature. On the other hand, PMN 700°C on TaC2 provides only +134mV shift and PMN 800°C (additional +95mV) is required to attain the shift similar to TaC1. The +134mV shift by PMN 700°C is attributable to the EWF change by the transformation of TaC into TaCN [11]. It should be noted that the EWF of the high-κ/TaC can be controlled from the nFET BE to the quarter gap nFET at no expense of EOT using the PMN in conjunction with SiON IL as shown in Fig. 4-5(b).

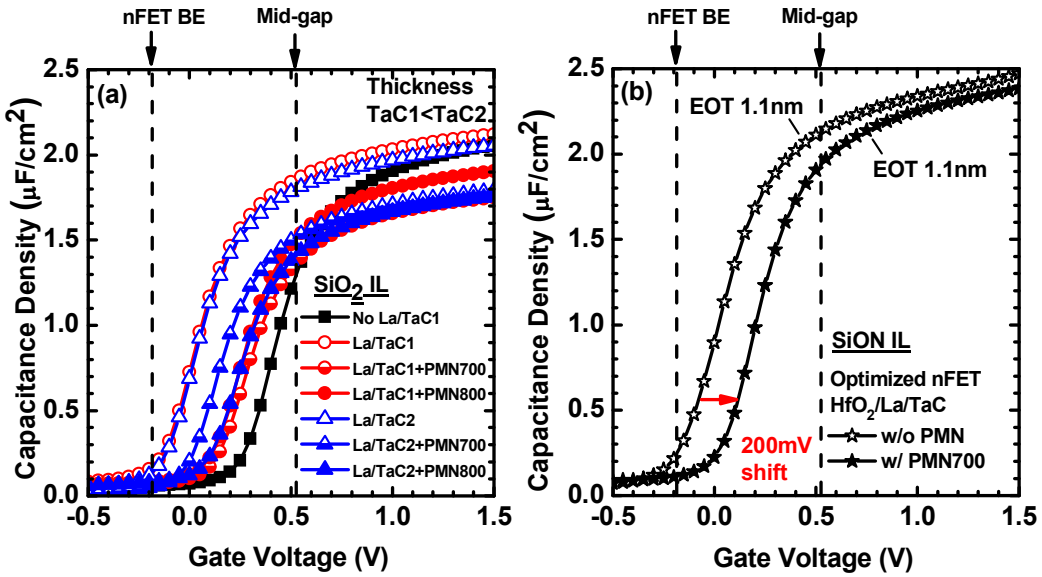


Fig. 4-5 (a) C-V curves for various TaC thicknesses (TaC1<TaC2) and PMN temperatures (700-900°C) with SiO_2 IL. (b) C-V curves for SiON IL/ HfO_2/La/TaC stack with and without PMN 700°C.

Next, the depth profiles of N and La were traced together by SIMS to understand the progressive EWF change for TaC2 (Fig. 4-6). The La depth profile starts to change as the N concentration increases at the the high-κ/TaC interface. Up-diffusion of La into TaCN as well as suppression of down-diffusion was observed with PMN 800°C. The decrease of La concentration at the IL/high-κ interface is 13%, which accounts for +31mV shift. Thus, the additional +95mV shift by PMN 800°C is not fully explained. There may be additional mechanisms induced by the up-diffusion of La, which counteract the dipole at the IL/high-κ interface. The two-step reaction and the impact on the EWF are summarized in Fig. 4-7. It is possible to control the two-step reaction (1: Transformation of the TaC into the TaCN, 2: Modification of the La depth profile) by means of the TaC thickness and the PMN temperature. These findings highlight the importance of precise control of depth profiles of V_t-tuning elements in gate-first process. Depth profile modification by means of post metal anneal opens up a new pathway for EWF control of high-κ/metal gate stacks.

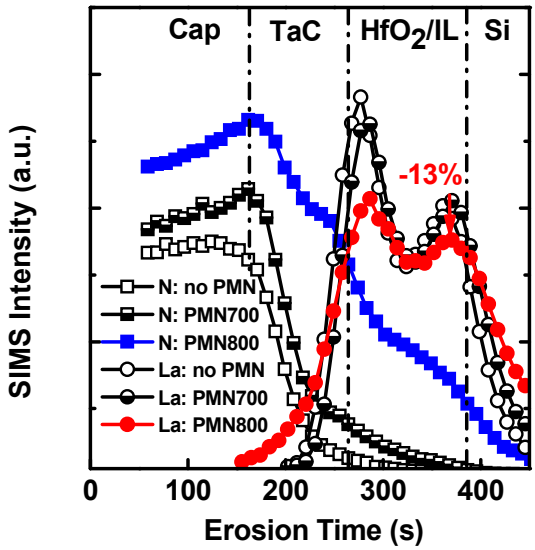


Fig. 4-6 SIMS depth profiles of N and La for PMN 700-900°C on high-κ /TaC2 stack.

	Step 1 Partial TaCN formation	Step 2 Complete TaCN formation	Step 3 Interaction with La-cap
MG/HK schematic	TaCN / TaC / La-cap / HfO_2, N	TaCN / La-cap / HfO_2, N	TaCN / La-cap / HfO_2, N
Metal EWF change	±0	+134mV	+134mV
La-induced EWF change	-380mV	-380mV	-285mV
Total EWF change	Control	+134mV	+229mV

Fig. 4-7 Reaction model for PMN on La-capped HfO_2/TaC stack and impacts on EWF.

4.4 EOT scaling toward the end of the roadmap

4.4.1 Direct and remote IL scavenging

Figure 4-8 demonstrates aggressive EOT scaling of HfO_2 down to 0.54 nm when the Gibbs free energy change at 1000K ($\Delta G°_{1000}$) of the following reaction (1) has a large positive value.

$$Si+\frac{2}{y}M_xO_y \rightarrow \frac{2x}{y}M+SiO_2 \qquad (4.1)$$

where M is the doped element in the TiN. The order of the $\Delta G°_{1000}$ (M1 < 0 < M2 << M3) is in agreement with the EOT scaling trend, indicating that oxidation of M3 is the driving force of the reaction.

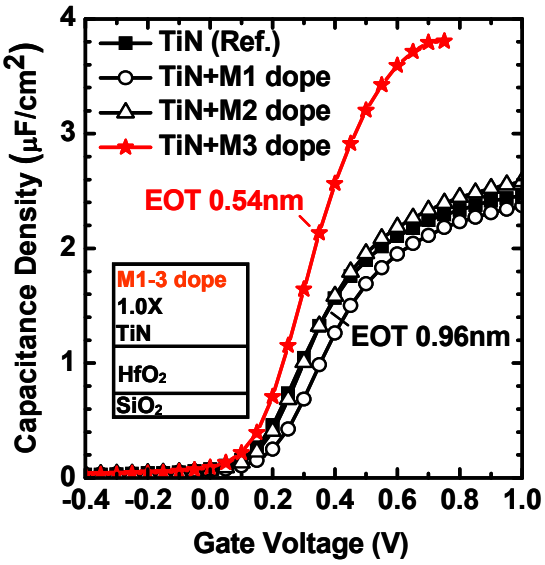


Fig. 4-8 Accumulation CV curves for TiN with various doping metals (M1, M2, M3). The order of $\Delta G°_{1000}$ of the reaction (4.1) is M1 < 0 < M2 << M3.

The EOT scaling can be controlled by changing the doped amount of M3 in the TiN gate as shown in Fig. 4-9. TEM reveals that the EOT change was brought about via IL scaling down to zero as shown in Fig. 4-10. The dose amount of M3 is varied by a factor of 2 between Fig. 4-10 (a) and (b). The difference of the IL thickness in the two TEM images indicates that the final IL thickness is controllable by changing the doped amount of M3.

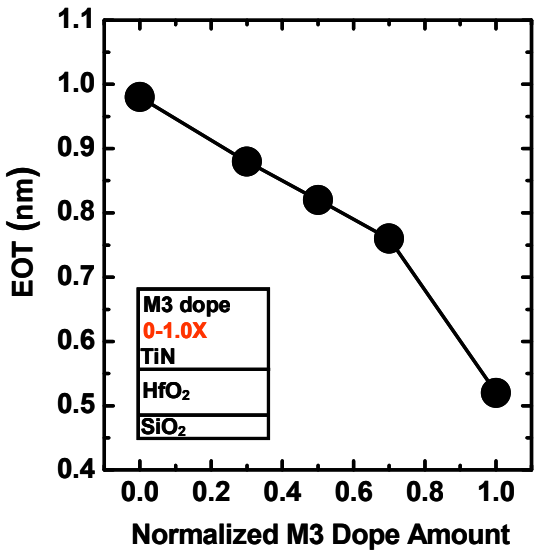


Fig. 4-9 EOT as function of normalized M3 dope amount in TiN.

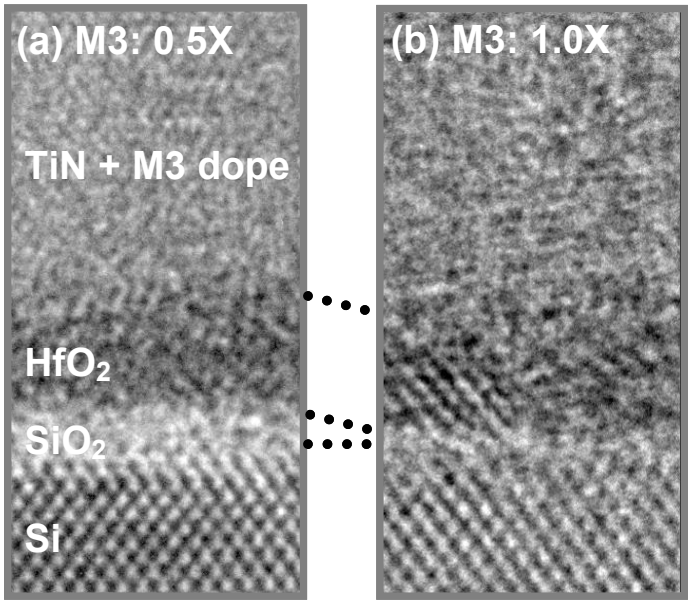


Fig. 4-10 TEM images of HfO_2/TiNstacks with M3 dope of (a)0.5X and (b)1.0X. The TEM was performed after the full process.

Figure 4-11 shows the EELS depth profile of Ti, Hf, and M3. The peak for M3 is isolated from the HfO_2/TiN interface and the intensity is below the detection limit in the HfO_2 layer. Note that the EELS was performed after the 1000°C activation anneal. The result evidences the remote IL scavenging mechanism.

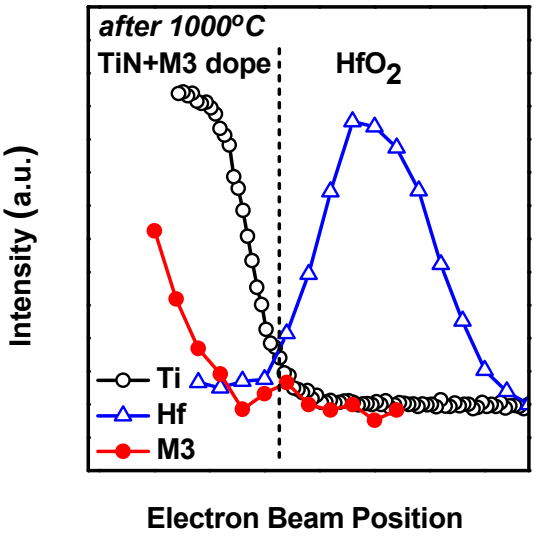


Fig. 4-11 EELS depth profiles for Ti, Hf, and M3 of HfO_2/M3-doped TiN. The EELS was performed after the full process.

Figure 4-12 compares the depth profiles of oxygen in the HfO_2/doped TiN stacks after the 1000°C activation anneal depending on the doped species and amount. Compared to the oxygen level for the M2 doping, increasing amount of oxygen was detected within the TiN electrode as the M3 doping amount increased. As a result, the total amount of oxygen in the IL/HfO_2 stack decreased accordingly. This result supports the theory of oxidation of M3 being the driving force of IL scavenging reaction.

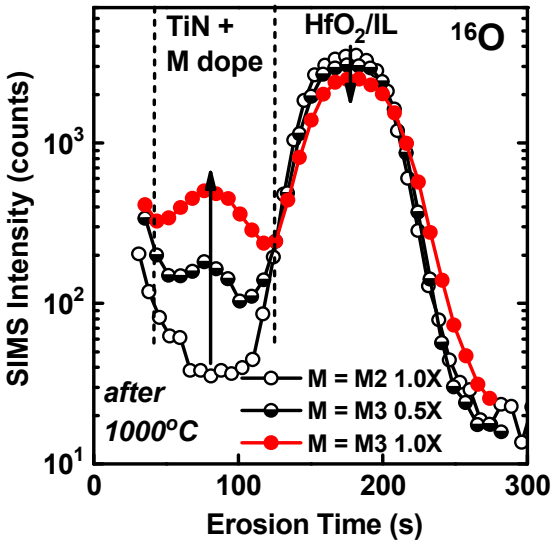


Fig. 4-12 ^{16}O SIMS profiles for TiN with various doping metals.

Figure 4-13 shows the EOT-J_g characteristics for the remote IL scavenging and the direct IL scavenging (i.e. TaN-M3 and TiN-M3 alloys). The trend line for SiO_2/poly-Si is also included. The J_g was measured at $V_g = V_{fb} - 1.0$ V. The trend line for the remote IL scavenging was obtained by varying the IL thickness by gradually changing the M3 doping amount. As one can see, the remote IL scavenging has 10× lower J_g compared to the direct IL scavenging. The improvement is attributable to the isolation of M3 from the HfO_2 layer, resulting in a lower defect density or more uniform IL scaling. As a result, a competitive EOT value (0.54 nm) meeting ITRS requirement [13] for the 15 nm node has been obtained while maintaining the J_g at 0.86 A/cm^2 by using the optimized HfO_2 condition. The slope for the remote IL scavenging is one order of magnitude increase of J_g per EOT 0.20 nm, which is identical to that of the SiO_2 scaling trend. This result also suggests a uniform IL scaling by the remote IL scavenging and no extrinsic J_g degradation from the IL thickness scaling.

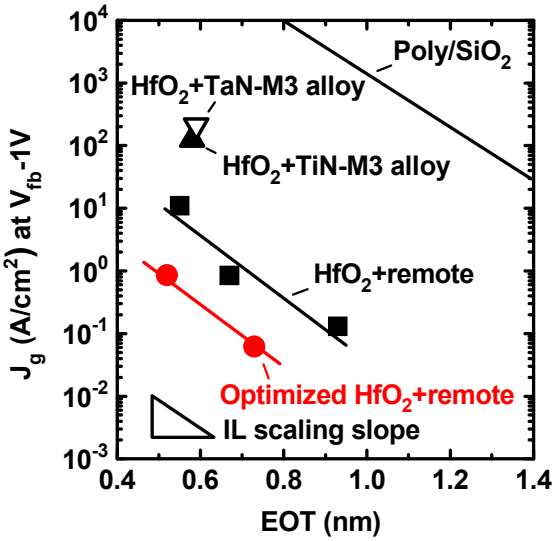


Fig. 4-13 EOT-J_g characteristics for remote IL scavenging and direct IL scavenging (i.e. TaN-M3 and TiN-M3 alloys). The trend line for the remote IL scavenging was obtained by changing the M3 doping amount.

Figure 4-14 shows the EOT-V_t plot for the HfO_2/TiN stacks with various amounts of M3 doping (0, 0.3X, 0.5X, 0.7X, and 1.0X). The EOT was continuously reduced as the M3 doping increased. The flat EOT-V_t trend indicates that no fixed charge/dipole is generated by the remote IL scavenging. This unique nature of the remote IL scavenging enables us to avoid additional scattering mechanisms and to explore an

intrinsic effect of scaling the IL thickness on the carrier mobility. The impact of intrinsic IL scaling on the carrier mobility will be discussed more in detail in Chapter 5.

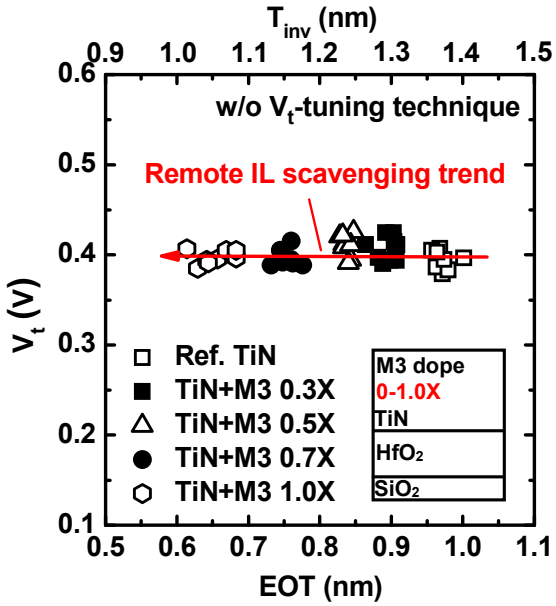


Fig. 4-14 EOT-V_t plot for HfO_2/TiN stacks with various amount of M3 doping (0, 0.3X, 0.5X, 0.7X, and 1.0X).

The electron and hole mobilities are compared for the remote and direct IL scavenging at matched T_{inv} values as shown in Fig. 4-15 (a) and (b), respectively. The electron mobility is compared at a T_{inv} of 1.20 nm and the hole mobility is compared at a T_{inv} of 1.10 nm as a function of E_{eff}. It should be noted that substantially higher mobilities are obtained for both electron and hole using the remote IL scavenging technique. This trend can be explained by the absence of additional fixed charge from the remote IL scavenging reaction. Therefore, no additional remote Coulomb scattering from fixed charges in the dielectric is accompanied. Thus, very strong advantages of the remote IL scavenging in J_g and carrier mobility (electron and hole) are demonstrated.

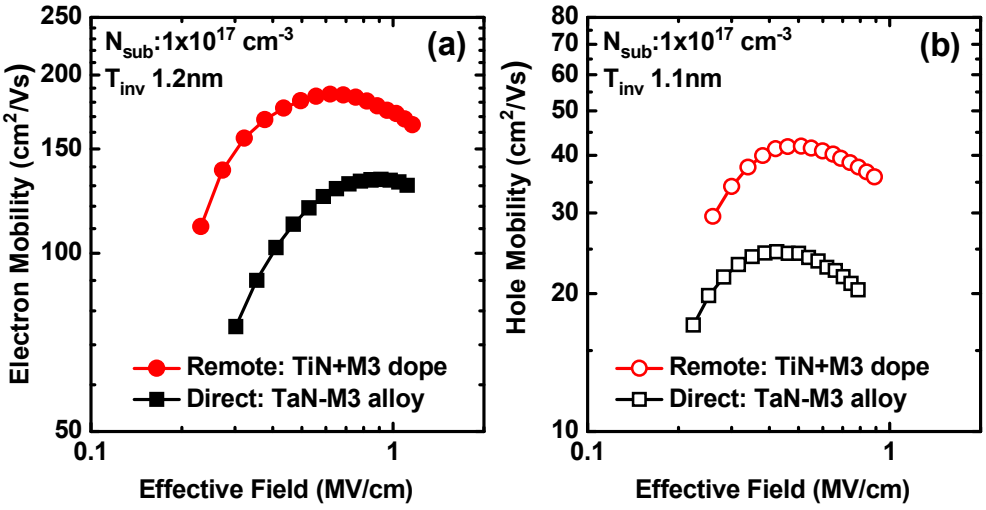


Fig. 4-15 Mobility comparison between remote IL scavenging and direct IL scavenging (TaN-M3 alloy) at matched T_{inv} for (a) electron and (b) hole.

4.4.2 Kinetics of remote IL scavenging reaction

In order to shed more light on the kinetics of the metal-gate-induced scavenging reaction, the impact of the post metal thermal budget was studied using the Ni silicide gate. As shown in Fig. 4-16 (a), most of the EOT scaling effect already took place at 600°C and little further change occurred with the 1000°C RTA. The EOT trend as a function of the maximum process temperature is summarized in Fig. 4-16 (b). In the case of reference TiN, a slight EOT increase was brought about by the 1000°C RTA due to IL regrowth. In contrast, the oxygen-scavenging TiN served two purposes. One is the substantial EOT scaling via IL scavenging in the temperature range between 400 and 600°C. The other is the suppression of IL regrowth at the higher temperature. The former reaction coincides with the reported temperature range in which oxygen vacancies in a HfO_2 layer become mobile and reach a steady state for oxygen transport [14]. We speculate that decomposition of the IL proceeds via the following reaction:

$$\frac{1}{2}SiO_2 + V_O \rightarrow \frac{1}{2}Si + O_O, \tag{4.2}$$

where V_o is the oxygen vacancy in the HfO_2 and O_o is the oxygen atom at the oxygen site of the HfO_2. The V_o acts as a mediator for oxygen transport from the IL to the TiN electrode, thus enabling oxygen scavenging in a remote way (See Fig. 4-10).

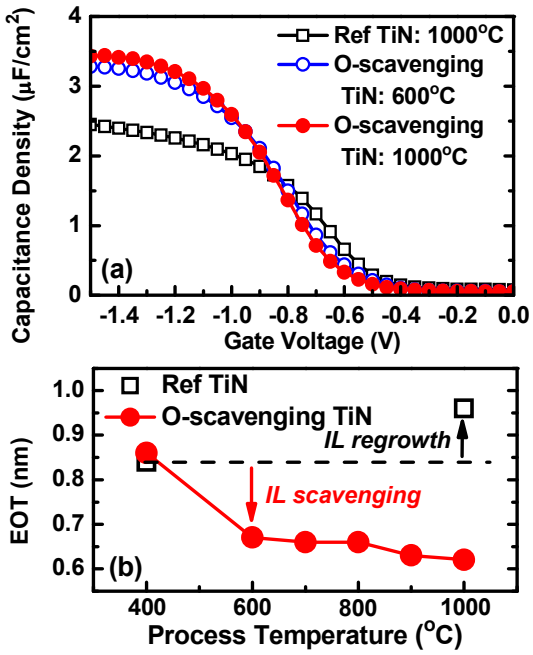


Fig. 4-16 (a) Accumulation CV curves for reference TiN with 1000°C RTA and oxygen scavenging TiN with 600 and 1000°C RTA using Ni silicide gate process. (b) EOT as function of post metal gate thermal budget for reference TiN and oxygen scavenging TiN. The data points for 400°C were obtained from the HfO_2/TiN gate stacks capped with 40-nm-thick TiN layers.

After the scavenging reaction, a small amount of Si was detected in the HfO_2 layer by medium energy ion scattering (MEIS). Based on the substantial EOT reduction, it is inferred that the impact of the Si incorporation on the permittivity of the HfO_2 should be limited and that a majority of the Si atoms in the original IL should be reincorporated into the underlying Si substrate as previously reported [15]. Once the oxygen transfer completes, the oxidized electrode acts as a barrier layer which limits the oxygen in-diffusion from the ambient during the high temperature RTA (> 600°C). The previously discussed reaction model is summarized in Fig. 4-17, in which oxygen vacancies (V_o) in HfO_2 act as mediators for a cascade reaction of oxygen transfer from the IL to the M3 atoms in the TiN and thus [V_o] in HfO_2 is maintained constant. Therefore, EOT scaling without V_t change is possible as far as oxygen is backfilled at

the SiO_2/HfO_2 interface during the remote IL scavenging reaction. In this model, the reaction proceeds until the M3 atoms in the TiN are completely oxidized, which means the final IL thickness is controllable by the amount of M3.

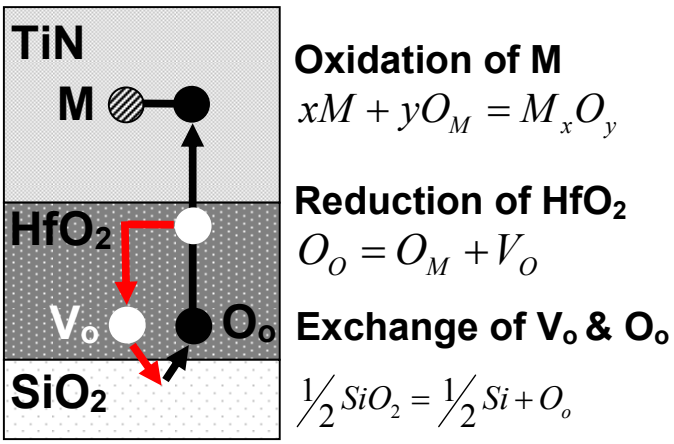


Fig. 4-17 Model: Cascade reactions of oxygen transfer from IL to the doped metal via V_o in HfO_2.

4.4.3 Compatibility of IL scaling and V_{fb}-tuning dipoles

Next, the compatibility of the remote IL scavenging and the V_{fb} tuning by the La and Al cap layers is investigated. Figure 4-18 shows the EOT-V_{fb} trends for the HfO_2/(La or Al cap)/TiN stacks with various amounts of M3 doping in the TiN layer. The magnitude of the V_{fb} shifts are approximately -300mV for the La-cap and +200mV for the Al-cap, which is consistent with the published data for nFET and pFET effective workfunction control, respectively. We found that the EOT scaling by the remote IL scavenging and the V_{fb} tuning by the La- and Al-dipole are additive, which makes this technique a viable option for CMOS integration. Figure 4-19 shows the accumulation CV curves for the extreme case of EOT scaling by combining the remote IL scavenging and the La-cap. It should be noted that EOT scaling down to 0.42 nm is obtained while maintaining a V_{fb} close to the Si E_c. This result demonstrates the potential of Hf-based high-κ for extension toward the 15-nm-node high performance logic device [13].

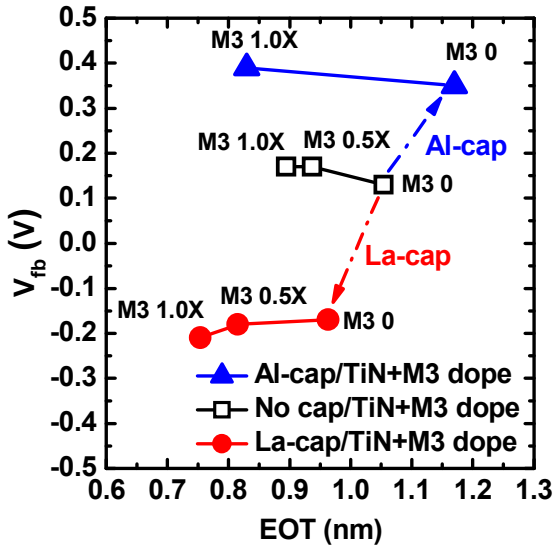


Fig. 4-18 EOT-V_{fb} trends for HfO_2/(La or Al cap)/TiN stacks with various amounts of M3 doping in TiN layer.

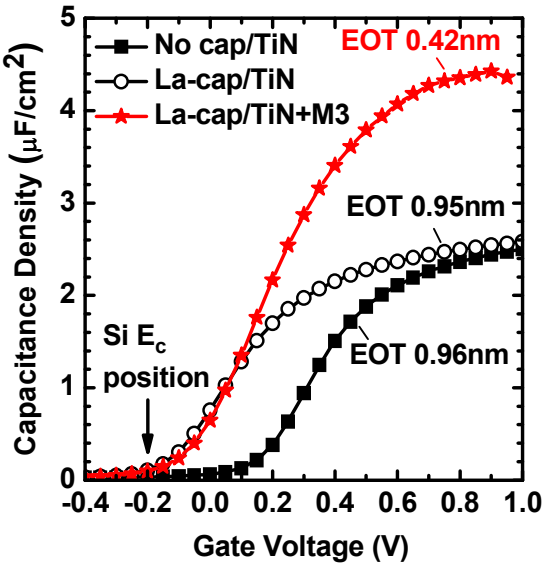


Fig. 4-19 Accumulation CV curves for extreme case of EOT scaling by combining remote IL scavenging (TiN+M3) and La-cap.

4.5 Summary

In this Chapter, EWF control and EOT scaling for gate-first process are discussed using novel process technologies. We demonstrated EWF control by means of the TaC electrode thickness and the PMN temperature in conjunction with La-cap layers. This finding highlights the importance of precise control of depth profiles of V_t-tuning elements in gate-first process. Depth profile modification by means of post metal anneal opens up a new pathway for EWF control of high-κ/metal gate stacks.

As for EOT scaling, a novel technique utilizing metal-gate-induced remote IL scaling is demonstrated and the kinetics underlying this process is clarified. The remote IL scavenging technique enables ultimate scaling of HfO_2 down to EOT 0.42 nm with a gate-first process. This technique shows advantages in carrier mobility and gate leakage current over conventional IL scaling schemes. Since this reaction takes advantage of transport of oxygen vacancies at 400-600°C, the compatibility is higher with gate-first process in which such thermal processes are automatically built in. We found that the EOT scaling by the remote IL scavenging and the V_{fb} tuning by the La- and Al-dipole are additive, which makes this technique a viable option for CMOS integration with gate-first process.

In Chapter 6, impacts of the remote IL scaling and the La- and Al-induced dipoles on carrier mobility are discussed more in detail.

Reference

[1] K. Henson, H. Bu, M. H. Na, Y. Liang, U. Kwon, S. Krishnan, J. Schaeffer, R. Jha, N. Moumen, R. Carter, C. DeWan, R. Donation, D. Guo, M. Hargrove, W. He, R. Mo, R. Ramachandran, K. Ramani, K. Schonenberg, Y. Tsang, X. Wang, M. Gribelyuk, W. Yan, J. Shepard, E. Cartier, M. Frank, E. Harley, R. Arndt, R. Knarr, T. Bailey, B. Zhang, K. Wong, T. Graves-Abe, E. Luckowski, D-G. Park, V. Narayanan, M. Chudzik, M. Khare: Tech. Dig. Int. Electron Devices Meet., 2008, p. 645.

[2] C. Choi, C-Y. Kang, S. J. Lee, M. S. Akbar, S. A. Krishnan, M. Zhang, H-S. Kim, T. Lee, I. Ok, F. Zhu, J. C. Lee, IEEE Electron Device Lett. **26** (2005) 7.

[3] M. Suzuki, M. Tomita, T. Yamaguchi, N. Fukushima: Tech. Dig. Int. Electron Devices Meet., 2005, p. 433.

[4] M. Takahashi, A. Ogawa, A. Hirano, Y. Kamimuta , Y. Watanabe, K. Iwamoto, S. Migita, N. Yasuda, H. Ota, T. Nabatame, A. Toriumi: Tech. Dig. Int. Electron Devices Meet., 2007, p. 523.

[5] J. Huang, D. Heh, P. Sivasubramani, P. D. Kirsch, G. Bersuker, D. C. Gilmer, M. A. Quevedo-Lopez, M. M. Hussain, P. Majhi, P. Lysaght, H. Park, N. Goel, C. Young, C. S. Park, C. Park, M. Cruz, V. Diaz, P. Y. Hung, J. Price, H.–H.Tseng, R. Jammy: Tech. Dig. VLSI Symp., 2009, p. 34.

[6] K. Choi, H. Jagannathan, C. Choi, L. Edge, T. Ando, M. Frank, P. Jamison, M. Wang, E. Cartier, S. Zafar, J. Bruley, A. Kerber**,** B. Linder, A. Callegari**,** Q. Yang, S. Brown, J. Stathis**,** J. Iacoponi, V. Paruchuri, V. Narayanan: Tech. Dig. VLSI Symp., 2009, p.138.

[7] H. S. Jung, J. H. Lee, S. K. Han, Y. S. Kim, H. J. Lim, M. J. Kim, S. J. Doh, M. Y. Yu, N. I. Lee, H. L. Lee, T. S. Jeon, H. J. Cho, S. B. Kang, S. Y. Kim, I. S. Park, D. Kim, H. S. Baik, Y. S. Chung: Tech. Dig. VLSI Symp., 2005, p. 232.

[8] V. Narayanan, V. K. Paruchuri, N. A. Bojarczuk, B. P. Linder, B.Doris, Y. H. Kim, S. Zafar, J. Stathis, S. Brown, J.Arnold, M. Copel, M. Steen, E. Cartier, A. Callegari, P. Jamison, J. -P. Locquet, D. L. Lacey, Y. Wang, P. E. Batson, P. Ronsheim, R. Jammy, M. P. Chudzik, M. Ieong, S. Guha, G. Shahidi, T. C. Chen: Tech. Dig. VLSI Symp., 2006, p. 224.

[9] Y. Yamamoto, K. Kita, K. Kyuno, A. Toriumi, Jpn. J. Appl. Phys. **46** (2007) 7251.

[10] J. K. Schaeffer, C. Capasso, R. Gregory, D. Gilmer, L. R. C. Fonseca, M. Raymond,
C. Happ, M. Kottke, S. B. Samavedam, P. J. Tobin, B. E. White, Jr.: J. Appl. Phys. **101** (2007) 014503.
[11] V. S. Chang, L.-A. Ragnarsson, G. Pourtois, R. O'Connor, C. Adelmann, S. Van Elshocht, A. Delabie, J. Swerts, N. Van der Heyden, T. Conard, H.-J. Cho, A. Akheyar, R. Mitsuhashi, T. Witters, B. J. O'Sullivan, L. Pantisano, E. Rohr, P. Lehnen, S. Kubicek, T. Schram, S. De Gendt, P. P. Absil, S. Biesemans: Tech. Dig. Int. Electron Devices Meet., 2007, p. 535.
[12] J. R. Hauser, IEEE Trans. Electron Devices **43** (1996) 1981.
[13] The International Technology Roadmap for Semiconductors; see http://www.itrs.net/Links/2008ITRS/Home2008.htm for the latest updates (2008)
[14] S. Guha and V. Narayanan, Phys. Rev. Lett. **98** (2007) 196101.
[15] H. Kim, P. C. McIntyre, C. O. Chui, K. C. Saraswat, and S. Stemmer, J. Appl. Phys. **96** (2004) 3467.

CHAPTER 5 EOT scaling and carrier mobility

The purpose of this Chapter is to unify the understanding on the EOT-mobility tradeoff for gate-last and gate-first processes. The difference in the crystallinity of HfO_2 and the oxygen transport tendency results in two different paths for device performance improvement, i.e. mobility improvement at a moderate EOT and aggressive EOT scaling at some expense of mobility. These findings provide a new perspective in selecting the integration scheme of high-κ metal gate devices in the future nodes. As for the aggressive EOT scaling path with gate-first process, the combination of the remote IL scavenging and the La-induced dipole shows a strong promise for device performance improvement in the 22-nm-node and beyond.

5.1 Introduction

As discussed in Chapter 3, crystallinity of high-κ films plays a significant role in electron mobility degradation. There have been previous reports discussing the correlation between the crystallization of high-κ films and the mobility degradation [1-3], however, the scattering mechanism induced by crystalline high-κ dielectrics is not fully understood. This is due to the difficulty in separating the contribution from the crystallization of high-κ from other mobility degradation factors, such as metal-gate-induced damage [4] or IL thickness [5]. Use of the Hf-Si electrode, as proposed in Chapter 3, enables us to solely focus on the impact of crystallization by eliminating other mobility degradation factors for the first time. In this Chapter, the effect of crystallization of HfO_2 on electron mobility is systematically investigated using a combination of high-κ PDA and the Hf-Si electrode in gate-last process. By employing high temperature PDA treatments, it is possible to bridge the learning from gate-last process to gate-first process, and thus obtain a universal understanding on the relationship between crystallinity of high-κ and carrier transport of MOSFET.

In Chapter 4, a unique capability of IL scaling toward zero IL is demonstrated using gate-first process. Many theoretical works predict mobility degradation as the IL thickness approaches zero due to remote carrier scattering mechanisms inherent to high-κ dielectric stacks [1, 6]. Experimental verification, however, has fallen behind for the sub-0.5-nm IL regime, since conventional IL scaling schemes are accompanied by additional fixed charge generation and/or interface degradation [7-10]. In this

Chapter, we shed light on the impact of intrinsic IL scaling on electron mobility by using a remote IL scavenging reaction as discussed in Chapter 4. Another important aspect is the impact of V_t control on mobility. Unlike gate-last process, gate-first process relies on V_t-setting dipole layers to overcome the Femi level pinning effect at high temperatures. Although many studies have been performed on the impact of La-induced dipoles [11, 12], interpretation of La-induced mobility degradation is still controversial. The understanding on the impact of V_t-setting dipole layers on carrier mobility when combined with IL scaling is of paramount importance for predicting the potential performance gain in the future technology nodes. In this Chapter, low temperature mobility analyses are performed for the intrinsic IL scaling and the La- and Al-induced dipoles to clarify the underlying physics behind the carrier transport.

Finally in this Chapter, physical models explaining all mobility data are presented and the potential scenario to improve the device performance via EOT scaling is discussed.

5.2 Experimental

5.2.1 High-κ crystallinity experiment (gate-last)

HfO_2 layers were deposited by ALD on Si(001) substrates with the thickness ranging from 1.0 to 3.0nm. Then, PDA were performed at 500 to 900^{o}C for 30 s in an N_2 atmosphere. In order to investigate the change of micro-structure of HfO_2 as functions of the film thickness and the PDA temperature, a valence-band photoemission spectroscopy was carried out on each sample. SRPES was performed at an undulator beam line BL-2C of the Photon Factory in High-Energy Accelerator Research Organization (KEK), where a high-performance photoelectron analyzer (Gammadata-Scienta SES100) was equipped. The base pressure in the chamber was kept at 10^{-10} Torr. The binding energies were calibrated by the peak position of Si 2p spectra from the Si substrates. The thicknesses of the HfO_2 layers and the IL between the HfO_2 layers and the Si substrates were estimated by cross-sectional TEM as well as by the intensity of Si-O bond normalized to the signal from the Si substrate.

Next, MOSFET with IL/HfO_2 gate dielectrics and Hf-Si electrodes were fabricated using the gate-last process as discussed in Section 3.3. The mobility analysis was carried out on 10×10 μm^2 nMOSFET with a substrate doping concentration of $1\times10^{17}/cm^3$. The channel sheet resistivity shows no dependence on the device size up

to 32×32 μm^2, which indicates that the external resistivity is sufficiently low and the impact on the mobility extraction is negligible.

5.2.2 Low temperature mobility analysis (gate-first)

In order to study the impact of intrinsic IL scaling on electron mobility, nMOSFETs with IL/HfO_2/M3-doped TiN stacks having different amounts of M3 were prepared using gate-first process as described in Section 4.2.2. The IL thickness was estimated by subtracting the EOT of the high-κ layer ($EOT_{high-\kappa}$) from the total EOT. The $EOT_{high-\kappa}$ was calculated from the physical thickness obtained by scanning transmission electron microscopy (STEM) and a κ-value of 20, which was estimated from the high-κ thickness dependence. The estimated IL thickness ranged from 0.12 to 0.54 nm depending on the doping amount of M3. In addition, nMOSFETs with IL/HfO_2/La- or Al-cap/TiN stacks were prepared without intentional IL scaling to evaluate the impact of V_t-setting dipoles alone on electron mobility. Finally, nMOSFETs with IL/HfO_2/La- or Al-cap/M3-doped TiN stacks were prepared to see the combined effect of IL scaling and V_t-setting dipoles. As discussed in Section 4.4.2, the remote IL scaling reaction occurs at the temperature between 400 and 600^oC. On the other hand, the V_t-setting cap layers require anneal temperature ≥ 600^oC to allow them to diffuse down to the bottom IL and to form dipole layers [13]. Thus, the chronological order of the reaction is as follows; 1) The remote IL scavenging happens during the poly-Si deposition, whose process temperature is 600^oC 2) Formation of La- and Al-induced dipole layers at the bottom IL during the activation anneal at 1000^oC. Therefore, we can investigate the case where Vt-tuning dipoles are formed on thinner ILs for these stacks.

Mobility characterization was carried out on 10×10 μm^2 nMOSFETs with a substrate doping concentration of 1×10^{17} cm^{-3} using I-V and split-C-V method at V_{ds} = 50 mV and f = 1 MHz in the wafer temperature range of 45-300K. Cs-corrected high angle annular dark field (HAADF) STEM and EELS were performed to obtain the La depth profile with a special resolution of 0.1-0.2 nm.

5.3 Impact of crystallinity of HfO_2

5.3.1 Phase diagram of HfO_2

Figure 5-1 shows valence-band spectra with various IL/HfO_2 thicknesses and PDA temperatures.

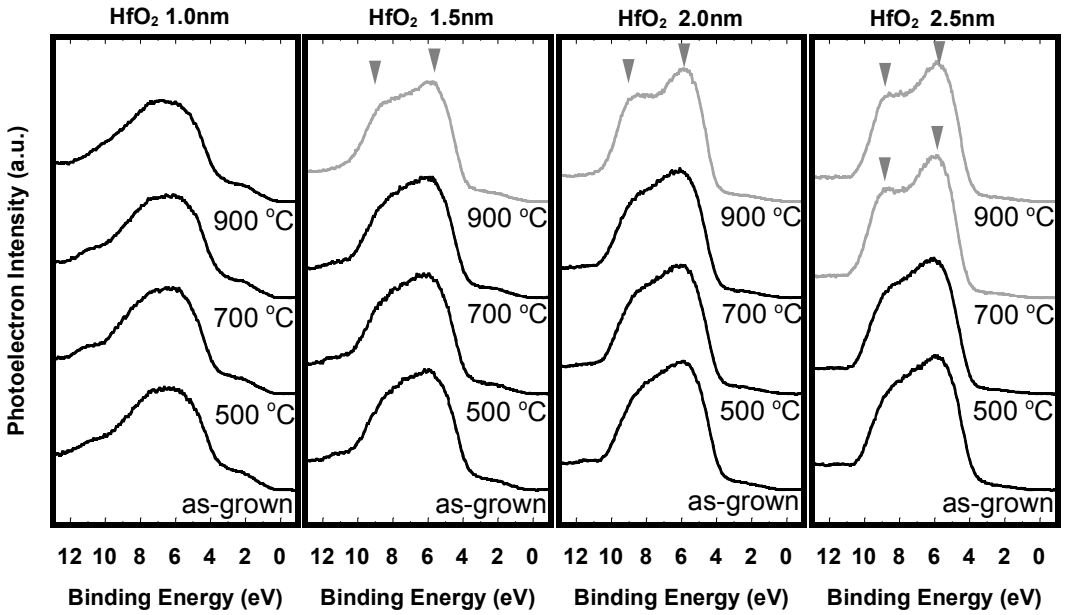


Fig. 5-1 Valence band spectra of HfO_2 (1.0-2.5 nm) with and without PDA 500-900 ^oC (N_2, 30s). The peak splits corresponding to monoclinic-phase HfO_2 are marked by gray triangles.

It has been reported that crystallization of HfO_2 is well related to the splitting in the valence-band spectra into the nonbonding state and the bonding state of O 2p [14]. The peak split was observed for the thickest HfO_2 sample (2.5 nm) with 700^{o}C PDA and for the intermediate thickness HfO_2 samples (1.5-2.0 nm) with 900^{o}C PDA whereas the thinnest HfO_2 sample (1.0 nm) maintained a single peak even after 900^{o}C PDA. The magnitude of the peak split was 2.9 eV, which agrees well with the density of states (DOS) calculation for monoclinic-HfO_2 (m-HfO_2) phase [15]. The result also indicates that HfO_2 in a commonly used thickness range (1.5-3.0nm) should exhibit a sign of crystallization with gate-first process, which includes thermal treatments higher than 900^{o}C.

Figure 5-2 (a) summarizes the trend of Si-O bond intensity from SRPES and IL thickness estimated from the bright portion of TEM images for sample A, B, C, and D

(details in Table 5-1). The good correlation of these parameters suggests that the increase of the bright portion of TEM images is caused by the oxidation of the Si substrate during the PDA treatment. In order to decouple the contribution of the oxygen supply from the ambient, 700°C PDA was performed to 1.5-nm-thick HfO_2 in two different atmosphere: 100% N_2 and N_2 with 0.1% O_2. The 700°C PDA under N_2 with 0.1% O_2 grows a 0.8-nm-thick SiO_2 film when performed directly on the Si(001) surface. After a full integration of MOSFETs with the Hf-Si electrode, the former yielded T_{inv} 1.62±0.01 nm whereas the latter yielded T_{inv} 1.63±0.01 nm. The weak dependence of T_{inv} on the PDA atmosphere suggests that the source of oxygen for the IL growth is within IL/HfO_2 stacks. An accelerated oxidation of Si due to the presence of HfO_2 as reported for ZrO_2 [16] may explain this phenomenon.

Table 5-1 Summary of HfO_2 samples

Sample	HfO_2 thickness (nm)	PDA temperature (°C)	EOT (nm)	HfO_2 phase by SRPES
A	1.5	500	0.9 nm	Amorphous
B	1.5	700	1.0 nm	Amorphous
C	2.5	700	1.1 nm	Monoclinic
D	1.5	900	1.5 nm	Monoclinic
E	1.0	900	1.4 nm	Amorphous

Figure 5-2 (b)-(d) show TEM images corresponding to sample B, C, and D, respectively. It should be noted that lattice fringes are visible in HfO_2 only for the samples showing peak splitting in Fig. 5-1. Thus, the validity of detecting the crystallization of HfO_2 by the splitting in the valence-band spectra was shown in the extremely thin thickness regime for gate dielectrics.

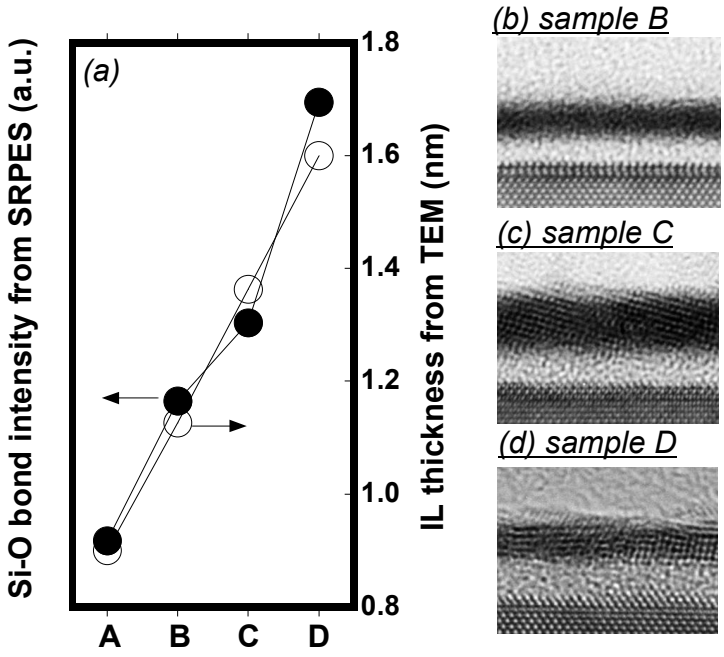


Fig. 5-2 (a) Si-O bond intensity relative to Si peak from substrate (left axis) and IL thickness estimated from TEM (right axis) for sample A-D. (b) Cross-section TEM of sample B. (c) Cross-section TEM of sample C. (d) Cross-section TEM of sample D.

5.3.2 Source of crystallization-induced mobility degradation

Figure 5-3 compares the electron mobility as a function of E_{eff} for sample B, C, D, and E. A distinctive mobility degradation was observed for m-HfO_2 by comparing sample B (amorphous HfO_2, hereinafter termed a-HfO_2) and sample C (m-HfO_2) especially near the peak at E_{eff} = 0.5 MV/cm. On the other hand, the same comparison between sample D (m-HfO_2) and sample E (a-HfO_2) showed only a small reduction of mobility. This trend is attributable to the difference of IL thickness (sample B: 1.36 nm, sample D: 1.60 nm by TEM). The strong dependence of crystallization-induced mobility degradation on the IL thickness indicates that the source of carrier scattering is remote from the channel. A remote surface roughness scattering induced by phase separation of high-κ dielectrics has been predicted [1], however, the weaker sensitivity at high E_{eff} rules out this possibility as a dominant mechanism. A recent study demonstrated that change in remote phonon scattering depending on the crystal phase of HfO_2 is neglibigle [17]. Therefore, we focused on remote scattering by fixed charges or dipoles in IL/HfO_2 and attempted to identify the physical origin behind the crystallization-induced mobility degradation.

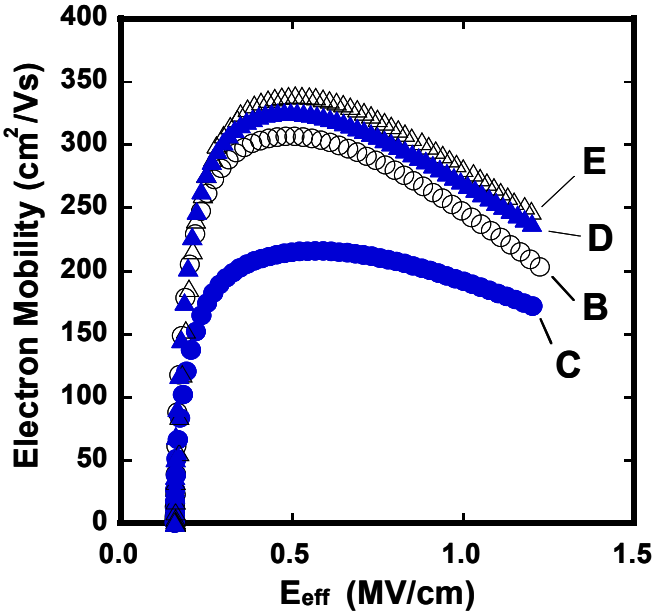


Fig. 5-3 Electron mobility as function of E_{eff} for sample B-E. The curves for the samples having m-HfO_2 (sample C and D) are shown in blue whereas the curves for the samples having a-HfO_2 (sample B and E) are shown in black.

We have experimentally investigated the following five locations as potential sources of mobility degradation: i) HfO_2/Hf-Si interface, ii) bulk portion of HfO_2, iii) bulk portion of IL, iv) Si/IL interface, and v) IL/HfO_2 interface.

i) HfO_2/Hf-Si interface: The vacuum work function of Hf-Si with various compositions was estimated from cutoff energy of X-ray excited secondary electron as shown in Fig. 5-4 (a). Figure 5-4 (b) shows the vacuum work function of Hf-Si as a function of Hf/(Hf+Si) ratio compared with the V_t of nMOSFETs having the corresponding Hf-Si electrodes on sample B (a-HfO_2) and sample C (m-HfO_2). The difference of the slope between the vacuum work function and the V_t in Fig. 5-4 (b) represents contributions of fixed charges or dipoles generated at the HfO_2/Hf-Si interface. In the case of a-HfO_2 (sample B), a disparity shows up for Si-rich Hf-Si, which may be attributable to the interface reaction of Hf-Si and HfO_2 and subsequent $HfSi_xO_y$ formation (see Fig. 3-9). On the other hand, the slopes are identical for m-HfO_2 (sample C) indicating immunity to the interface reaction with Hf-Si as opposed to a-HfO_2. Thus, metal gate induced fixed charges and dipoles are not responsible for the mobility reduction of m-HfO_2.

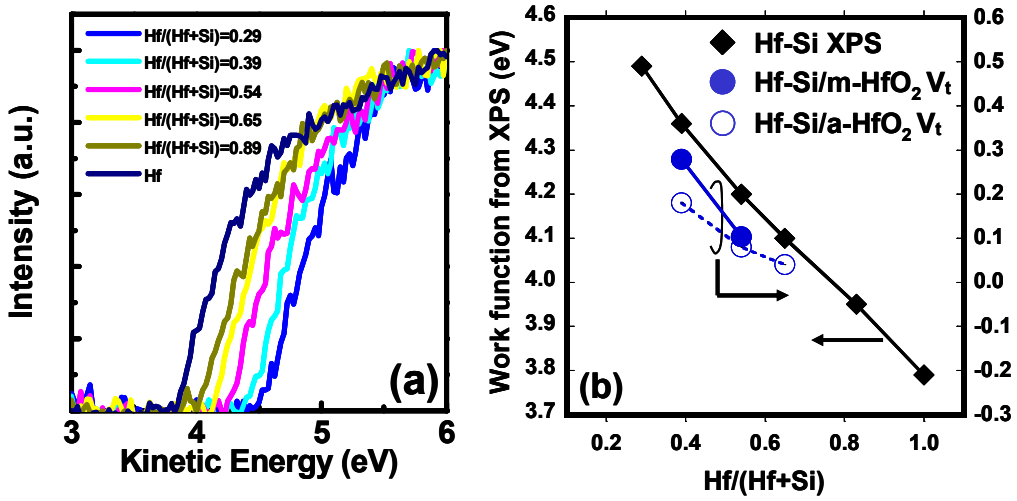


Fig. 5-4 (a) Cutoff energy of X-ray excited secondary electron from Hf-Si films with various compositions (b) Vacuum work function of Hf-Si obtained from XPS (left axis) and V_t of nMOSFETs with corresponding Hf-Si electrodes as function of Hf/(Hf+Si) ratio. The V_t for a-HfO_2 (sample B) and m-HfO_2 (sample C) are compared in the plot.

ii) Bulk portion of HfO_2: Since crystallization of HfO_2 accompanies a drastic increase of charge trapping (see Fig. 3-11), we have investigated the impact of trapped charges on carrier mobility via the change of transconductance (G_m) under a positive bias temperature instability (PBTI) stress condition. The PBTI measurement was performed on 10×10 μm^2 nMOSFET with m-HfO_2 (sample C) gate dielectric under the bias conditions of V_g = +1.6 V and at temperature 105°C. The peak value of G_m is a good indicator of a low field mobility which is sensitive to remote Coulomb scattering. The V_t shift after 1023s was 70mV which corresponds to a charge density of 8.4×10^{11} cm^{-2} at the IL/HfO_2 interface. The change of the peak value of G_m, however, was negligible (from 18.8 to 18.7 μS/μm). The result indicates that the trapped charges within the bulk portion of HfO_2 do not contribute much to the mobility degradation.

iii) Bulk portion of IL: The presence of oxygen vacancies in interfacial SiO_2 due to its interaction with the high-κ layer has been reported as the IL thickness decreases [18]. However, we have observed a growth of IL induced by the crystallization of HfO_2 (Fig. 5-2), and hence this model is not applicable. The other possibility is the fixed charge generation in the newly grown portion of IL as a result of the

crystallization of HfO_2. If this is the case, the mobility degradation should happen independent of the IL thickness as the source of scattering is just above the channel. The strong dependence of the mobility degradation on the IL thickness seen in Fig. 5-3 clearly disagrees with this model.

iv) Si/IL interface: A subthreshold slope of I_d-V_g characteristics is a good indicator of the quality of the Si/IL interface. Sample B (a-HfO_2) and sample C (m-HfO_2) yield almost identical subthreshold slope values (67 and 68 mV/dec, respectively). Thus, the Si/IL interface is not responsible for the crystallization-induced mobility degradation.

v) IL/ HfO_2 interface**:** The discussions so far lead us to conclude that the source of the mobility degradation induced by the crystallization of HfO_2 is localized at the IL/HfO_2 interface. Figure 5-5 compares the trend of V_t of nMOSFETs as a function of HfO_2 thickness for a-HfO_2 (1.0-2.0 nm) and m-HfO_2 (2.5-3.0 nm) with 700^{o}C PDA. Fittings on the experimental data by combinations of quadratic and linear components were performed in order to separate the effects from the fixed charges uniformly distributed within the bulk HfO_2 (which should show a quadratic dependence) and the ones localized at the IL/HfO_2 interface (which should show a linear dependence). A discontinuous change in the V_t is clearly seen as increasing the HfO_2 thickness beyond the critical thickness for the crystallization. If this is induced by formation of dipoles at the IL/HfO_2 interface, the change in the fitting curves should be a parallel downward shift because the V_t shift does not depend on the distance between the electrode and the dipoles. However, the difference between the two fitting curves is thickness dependent as seen in Fig. 5-5. A good fitting for m-HfO_2 data points was obtained by assuming generation of additional fixed charges localized at the IL/HfO_2 interface. The estimated amounts of the fixed charges at the IL/HfO_2 interface are 6.6×10^{12} cm^{-2} for a-HfO_2 and 1.1×10^{13} cm^{-2} for m-HfO_2. The degradation of the peak mobility in Fig. 3-3 (306 cm^2/Vs to 216 cm^2/Vs) and the increase of the amount of the fixed charges at the IL/HfO_2 are in a good quantitative agreement with the simulation for remote Coulomb scattering [1]. We believe that the oxygen transfer from the HfO_2 layer to the Si substrate is promoted upon the crystallization of HfO_2 as evidenced in Fig. 5-2 and fixed charges are generated at the IL/HfO_2 interface during the process.

This model explains the mobility degradation and the IL growth accompanied by the crystallization of HfO_2.

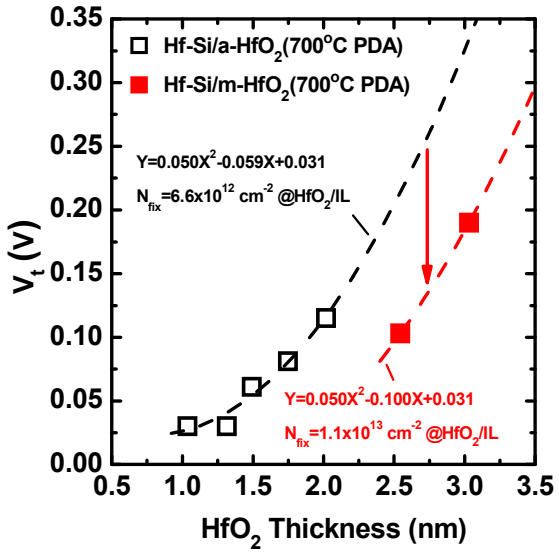


Fig. 5-5 V_t of nMOSFETs as function of physical thickness of HfO_2. The trends for a-HfO_2 (1.0-2.0 nm) and m-HfO_2 (2.5-3.0 nm) are compared with 700°C PDA. Fittings on the experimental data by combinations of quadratic and linear components were performed in order to separate the effects from the fixed charges within the bulk HfO_2 and the ones localized at the IL/HfO_2 interface.

In this sub-section, we have experimentally shown that the crystallization of HfO_2 and the subsequent formation of fixed charges localized the IL/HfO_2 interface are responsible for the degradation of electron mobility. The analysis of the valence band photoemission revealed that it is indeed possible to avoid the crystallization of HfO_2 by means of careful control of the HfO_2 thickness and the thermal budget of the subsequent processes and thereby the areal density of the fixed charges at the IL/HfO_2 interface can by reduced. The optimized gate stack (sample B) with a reduced amount of fixed charges at the IL/HfO_2 interface yielded a record high electron mobility of 248 cm^2/Vs (E_{eff} 1 MV/cm) at an EOT of 1.0 nm. These findings indicate a potential advantage of gate-last process, which enables use of amorphous HfO_2, in terms of carrier mobility.

5.4 Impact of IL scaling and interface dipoles

5.4.1 Intrinsic IL scaling effect

As discussed in Chapter 4, metal-gate-induced IL scavenging reaction opens up an attractive pathway to EOT scaling toward the 15nm-node. Since this reaction requires thermal treatment of 400-600^{o}C to trigger oxygen transport (see Fig. 4-16), the compatibility with gate-first process is higher. This means that IL scaling needs to be combined with V_t tuning by interface dipole layers. In this sub-section, we investigate the impacts of the intrinsic IL scaling and the La- and Al- induced dipoles on the electron mobility.

The I_d–V_g characteristics for the reference SiO_2/HfO_2 stack (Sample A), the IL scaling with M3-doped TiN (Sample B), the reference stack with the La-cap (Sample C), and the reference stack with the Al-cap (Sample D) are shown in Fig. 5-6. The EOT, V_t, and sub-threshold slope (S.S.) for Sample A, B, C, and D are summarized in Table 5-2. Sample B showed EOT scaling of 0.26 nm via IL thickness scaling with no V_t change. Sample C and D showed La-induced V_t shift of -460 mV and Al-induced V_t shift of +270 mV, respectively. Note that the S.S. values were barely changed for all samples, indicating that the degradation of interface trap density is limited and its impact on mobility should be negligible.

Table 5-2 Summary of MOSFET parameters

Sample	EOT (nm)	V_t shift (mV)	S.S. (mV/dec.)	Description
A	0.96	Ref.	64	SiO_2/HfO_2 (Ref.)
B	0.70	± 0	67	Intrinsic IL scaling
C	0.58	- 460	62	La-induced dipole
D	1.15	+ 270	67	Al-induced dipole

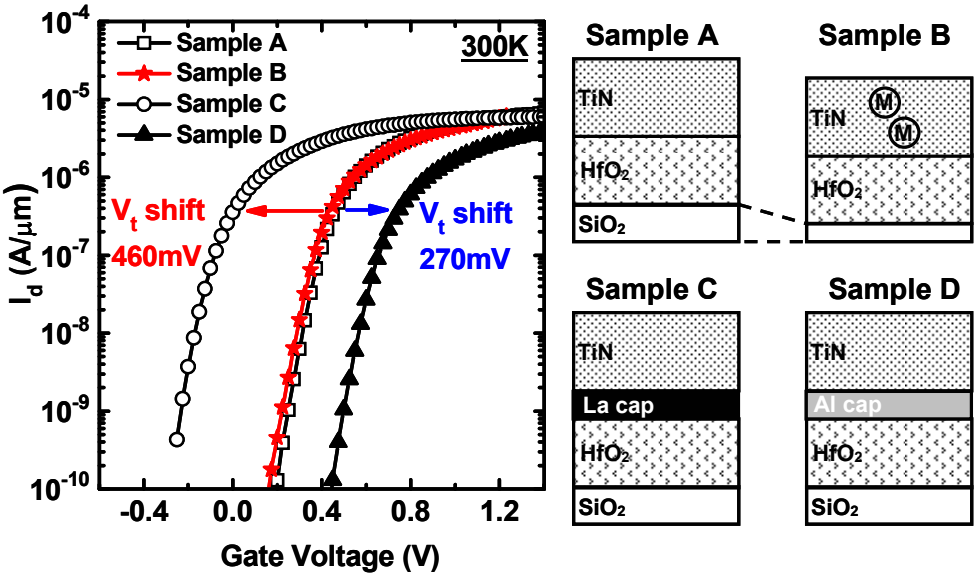


Fig. 5-6 I_d-V_g characteristics of Sample A, B, C, and D (see Table 5-2). The schematics of the gate stack structures are shown on the right.

Figure 5-7 shows the electron mobility as a function of EOT at E_{eff} of (a) 0.5 MV/cm and (b) 1.0 MV/cm. The mobility-EOT slopes for the intrinsic IL scaling are 30 cm^2/Vs and 20 cm^2/Vs per 0.1 nm, respectively. We have thus shown experimentally that the tradeoff between mobility and EOT is inevitable, even when employing intrinsic IL scaling without change in V_t and S.S. In this regard, Goto et al. demonstrated that aggressive EOT scaling at the expense of mobility to some extent yields a performance benefit in the quasi-ballistic carrier transport regime [19]. Thus, EOT scaling via IL scaling can improve the device performance when practiced with aggressive L_g scaling ($\leq$ 25 nm) and minimized extrinsic mobility degradation. It is interesting to note that the mobility-EOT slope for the La-capped samples is identical to that for the intrinsic IL scaling, whereas the Al-cap shows degradation in both E_{eff} regimes. We shed more light on this trend in the next sub-section.

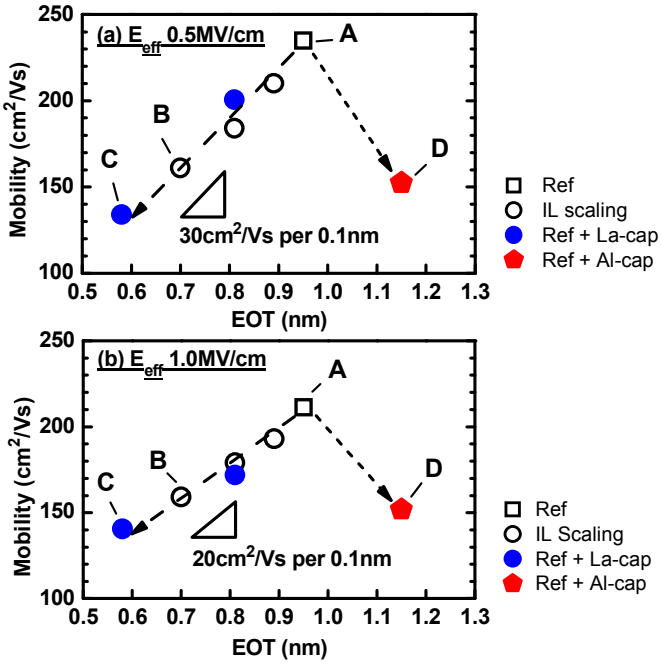


Fig. 5-7 Electron mobility as function of EOT at 300 K and E_{eff} of (a) 0.5 MV/cm and (b) 1.0 MV/cm.

5.4.2 Low temperature mobility analyses

The temperature dependence of mobility at 45-300 K was studied for sample A, B, C, and D in order to clarify the mechanisms behind the trend as shown in Fig. 5-8. The surface roughness scattering (SRS) limited mobility (μ_{SRS}) values were extracted to be $462\times E_{eff}^{-1.20}$, $270\times E_{eff}^{-0.72}$, $219\times E_{eff}^{-0.69}$, and $277\times E_{eff}^{-0.83}$ cm^2/Vs, respectively, by extrapolating the mobility at 45 K and E_{eff} 1MV/cm, where the temperature dependence disappeared. Then the mobility limited by remote phonon scattering (RPS) and remote Coulomb scattering (RCS) from the high-κ layer ($\mu_{RPS+RCS}$) was extracted using Matthiessen's rule as follows:

$$\mu_{RPS+RCS} = \left(\mu_{total}^{-1} - \mu_{SRS}^{-1}\right)^{-1}, \tag{5.1}$$

where μ_{total} is the total mobility measured at 300 K.

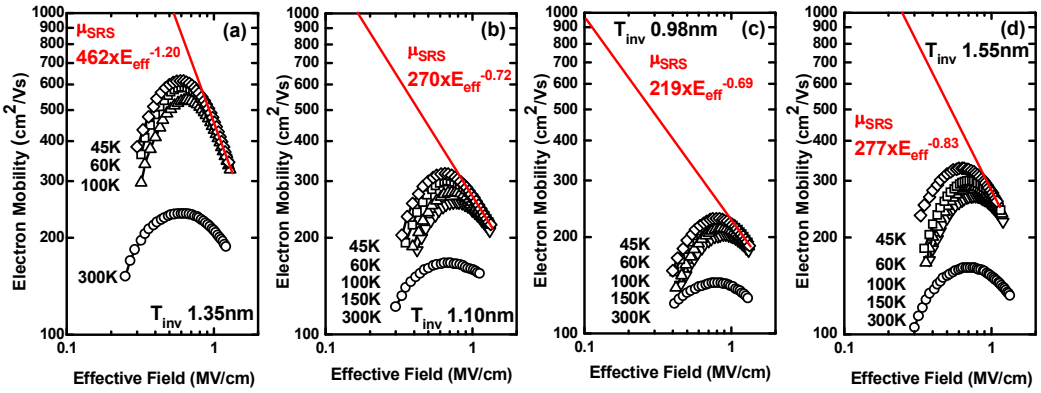


Fig. 5-8 Electron mobility as function of E_{eff} obtained at various wafer temperatures (45-300K) for (a) HfO_2/TiN (Sample A) (b) HfO_2/TiN+M3 dope (Sample B) (c) HfO_2/La-cap/TiN (Sample C), and (d) HfO_2/Al-cap/TiN (Sample D).

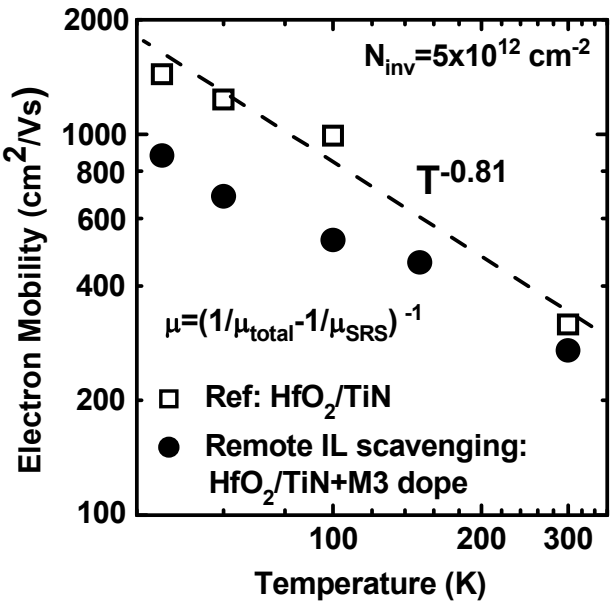


Fig. 5-9 Temperature dependence of $\mu_{RPS+RCS}$ at $N_{inv} = 5x10^{12}cm^{-2}$. The temperature dependence ($\sim T^{-0.81}$) indicates soft optical phonon response of HfO_2.

Next, the $\mu_{RPS+RCS}$ is plotted as a function of temperature to understand the middle E_{eff} mobility trend as shown in Fig 5-9. The temperature dependence ($T^{-0.81}$) for the HfO_2/TiN stack indicates soft optical phonon response of HfO_2 [20]. A slightly weaker sensitivity for the remote IL scavenging sample is explained by enhanced RPS. Since RPS and RCS are known to exhibit a strong dependence on the distance from the channel, the $\mu_{RPS+RCS}$ is summarized as a function of the estimated IL thickness in Fig. 5-10.

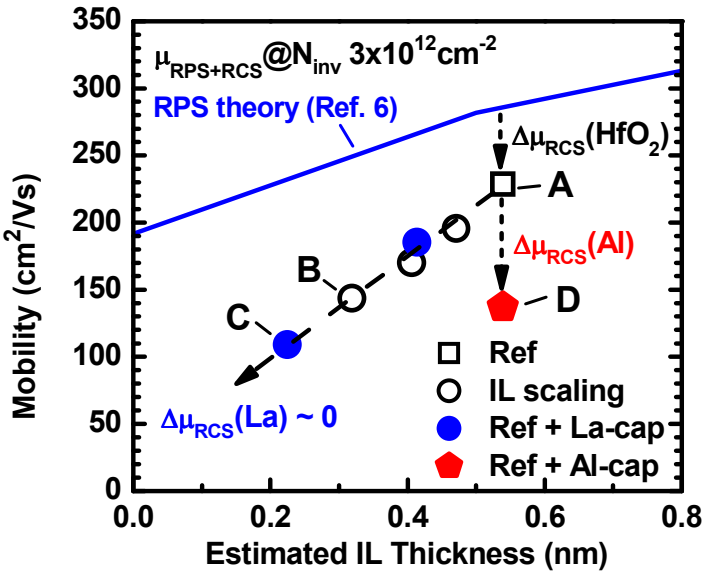


Fig. 5-10 Electron mobility limited by RPS and RCS ($\mu_{RPS+RCS}$) at 300 K as function of estimated IL thickness at N_{inv} of 3×10^{12} cm^{-3}. The simulated dependence from the RPS theory (Ref. 6) with ion impurity correction is also shown.

The plots for the intrinsic IL scaling delineate a straight tradeoff line, which is slightly steeper and shifted downward from the simulated trend from the RPS of HfO_2 alone [6]. The deviation is attributable to the additional RCS from the fixed charges localized at the SiO_2/HfO_2 interface as discussed in Section 5.3.2. More importantly, the trendline for the La-induced dipole is identical to that of the intrinsic IL scaling, indicating no additional RCS. In contrast, the Al-induced dipole brought about additional RCS at a fixed IL thickness. We attribute the difference to the silicate forming nature of La, as HAADF STEM on sample C detected a gradual La depth profile extending into the IL as shown in Fig. 5-11. It has been reported that La in SiO_2 forms a silicate layer with a saturation compound of $La_2Si_2O_7$ [21]. As a result, charges within the La-O-Si network are cancelled out and long-range and low-density net dipoles may be formed [22].

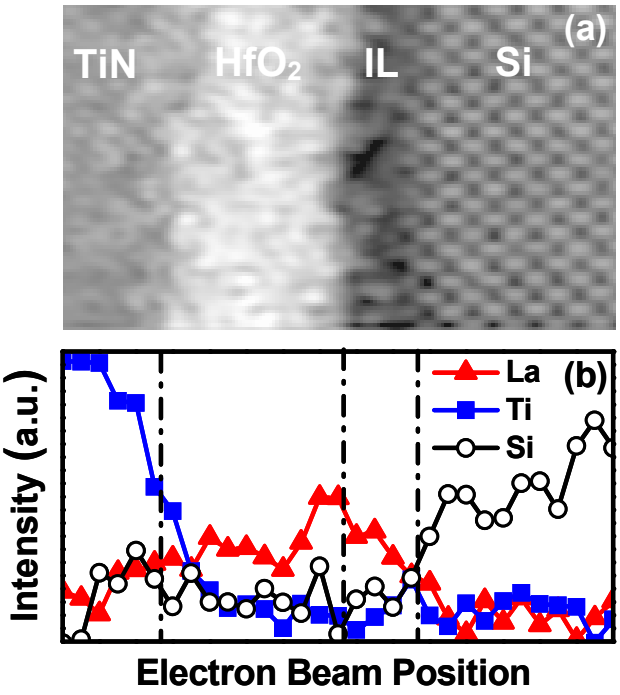


Fig. 5-11 (a) Z-contrast image obtained by HAADF STEM and (b) EELS depth profiles of La, Ti, and Si for La-capped sample (Sample C in Table 5-2).

The change in V_t by interface dipoles is expressed as follows:

$$\Delta V_t = \frac{Q \times d_{dipole} \times N_{dipole}}{\varepsilon_{dipole}}, \tag{5.2}$$

where Q is the charge amount at both ends of the unit dipole ($+Q$ and $-Q$), d_{dipole} is the distance between the charges, N_{dipole} is the areal density of the unit dipole, and ε_{dipole} is the permittivity of the dipole layer. Hence, a sufficient V_t shift can be maintained by compensating the reduction of N_{dipole} by the increase of d_{dipole}. The absence of additional mobility degradation indicates that the sum of RCS and RPS from the newly formed La-silicate layer is close to that of the HfO_2 owing to the low N_{dipole}.

Next, the $\mu_{RCS+RPS}$ values at E_{eff} 1.0 MV/cm were compared. The $\mu_{RCS+RPS}$ showed no degradation as the EOT decreased by the intrinsic IL scaling ($\mu_{RCS+RPS}$ 386 cm^2/Vs, EOT 0.70 nm) and the La-induced dipole ($\mu_{RCS+RPS}$ 392 cm^2/Vs, EOT 0.58 nm) compared to the reference SiO_2/HfO_2 ($\mu_{RCS+RPS}$ 389 cm^2/Vs, EOT 0.95 nm). Thus, the mobility degradation at E_{eff} 1.0 MV/cm is solely limited by SRS. Since the trend

of S.S. indicates no degradation at the Si/SiO_2 interface, we speculate that remote SRS (r-SRS) from the SiO_2/high-κ interface is the origin of the mobility degradation. Li and Ma predicted that roughness at the remote interface from the channel can degrade the carrier mobility depending on the oxide thickness (T_{IL}), the average deviation of T_{IL} (ΔT_{IL}) [23]. The mobility-EOT trend in Fig. 5-7 (b) indicates that the high E_{eff} mobility is degraded due to r-SRS driven by T_{IL} scaling in the case of intrinsic IL scaling and La-induced dipole. On the other hand, the mobility degradation without EOT scaling from the Al-induced dipole implies enhanced r-SRS by the increase of ΔT_{IL}. The addition of Al may degrade the morphology of the SiO_2/HfO_2 interface and cause additional r-SRS, whereas the front of the La-silicate reaction is maintained flat resulting in no additional r-SRS.

5.4.3 Physical model for mobility degradation

The previously discussed mechanisms in the middle and high E_{eff} are summarized in Fig. 5-12. In order to check the validity of our physical model, the electron mobility response is investigated by combining the La and Al cap layers and the M3-doped TiN electrode with gate-first process. As we previously discussed, the chronological order of the reaction is as follows; 1) The remote IL scavenging happens during the Poly-Si deposition, whose process temperature is 600^{o}C 2) Formation of La- and Al-induced dipole layers at the bottom IL during the activation anneal at 1000^{o}C. Thus, we can scale IL thickness and form La- and Al-induced dipole layers later at the SiO_2/HfO_2 interface. Figure 5-13 shows the electron mobility degradation from the reference HfO_2/non-doped TiN stack as a function of EOT. The intrinsic IL scaling (i.e. no cap/TiN+M3) degrades the electron mobility at the slope of 20 cm^2/Vs per 0.1 nm. It should be noted that the combination of the remote IL scavenging and the La-cap does not change the slope and only extends the EOT scaling. On the other hand, the combination of the remote IL scavenging and the Al-cap makes the slope steeper, indicating the additional carrier scattering source localized at the SiO_2/HfO_2 interface in the case of Al-induced dipole. These results are consistent with the proposed model in Fig. 5-12.

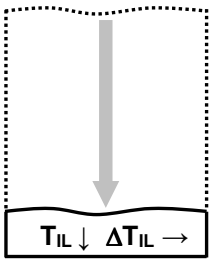
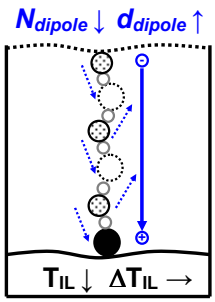
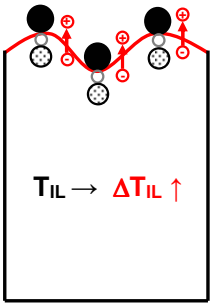
	Intrinsic IL scaling	La-induced dipole	Al-induced dipole
IL schematics Dipole element Oxygen Silicon			
Net dipole	No extrinsic dipole	Low N_{dipole} Long d_{dipole}	High N_{dipole} Short d_{dipole}
SiO_2/high-κ roughness	ΔT_{IL} unchanged	ΔT_{IL} unchanged	ΔT_{IL} degraded
Δμ at E_{eff} 0.5 MV/cm	RPS/RCS of HfO_2 by T_{IL} scaling	No additional RCS = Intrinsic IL scaling	Additional RCS by High N_{dipole}
Δμ at E_{eff} 1.0 MV/cm	Intrinsic r-SRS by T_{IL} scaling	No additional r-SRS = Intrinsic IL scaling	Additional r-SRS by ΔT_{IL} degradation

Fig. 5-12 Schematics of mobility degradation mechanisms from intrinsic IL scaling and La- and Al- induced dipoles at E_{eff} of 0.5 MV/cm and 1.0 MV/cm. T_{IL} is the thickness of the pure SiO_2 portion, ΔT_{IL} is the average deviation of T_{IL}, N_{dipole} is the areal density, and d_{dipole} is the length of the unit dipole.

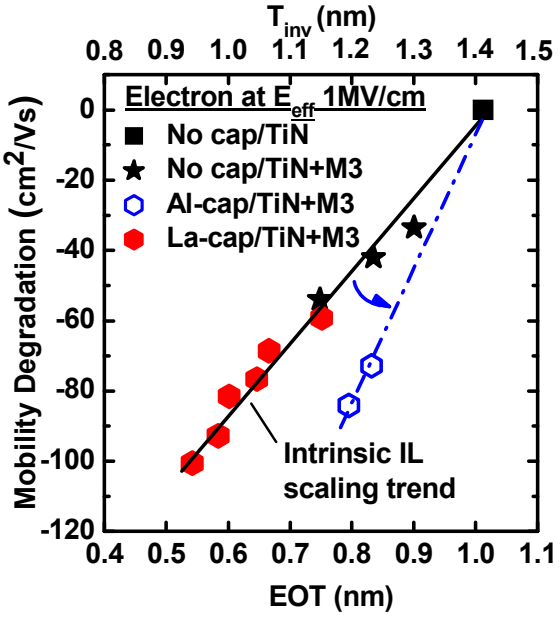


Fig. 5-13 Electron mobility degradation from reference HfO_2/non-doped TiN stack as function of EOT. The remote IL scavenging was performed on the non-capped, La-capped, and Al-capped HfO_2 samples.

5.4.4 EOT scaling strategy in quasi-ballistic transport era

Understanding of correlation between low-field mobility (μ) and high-field carrier velocity (*v*), which is more directly related to drive current, becomes more and more important in the state-of-the-art CMOS devices. The correlation depends on the L_g [24]. In long-channel MOSFETs, μ is the sole factor in determining *v*. As velocity saturation phenomenon begins to occur in short-channel MOSFETs, μ dependence of *v* becomes weaker [25]. As the L_g shrinks further, the carrier transport eventually reaches a full-ballistic regime where μ loses its meaning and *v* is determined solely by injection velocity [26]. Modern MOSFETs, however, are considered to operate in a quasi-ballistic transport regime [27] where μ still plays an important role via backscattering ratio for carriers injected from source to channel [28]. Therefore, a higher μ is still preferred at a given T_{inv} (EOT) for the near-term CMOS scaling until full-ballistic operation is realized.

In addition to the carrier transport mechanism, we need to consider the added benefits from T_{inv} scaling. It has been demonstrated that aggressive T_{inv} scaling enhances the control of channel potential by the gate and thus suppresses short channel effects (SCEs) [29]. Moreover, T_{inv} scaling (i.e. inversion oxide capacitance (C_{inv}) increase) is effective in suppressing variability of V_t due to random dopant fluctuation as the standard deviation of V_t (σV_t) is expressed as follows [30];

$$\sigma V_t = \frac{q}{C_{inv}} \sqrt{\frac{N_{sub} W_{dep}}{3 L_g W_g}}, \tag{5.3}$$

where q is electronic charge, N_{sub} is the substrate doping concentration, W_{dep} is the depletion region width, and W_g is the width of the gate.

Ideally, gate dielectric scaling should be achieved without carrier mobility degradation. As discussed in this Chapter, this is fundamentally not possible if we employ IL scaling strategy. The alternative is to maintain sufficiently thick IL and introduce higher-κ material exceeding Hf-based high-κ to scale EOT of the total stack. The mobility-EOT tradeoff may be mitigated this way, however, materials reaching the maturity of Hf-based high-κ have not been identified yet. Therefore, EOT scaling

with some compromise of carrier mobility is the only practical scaling approach. In this regard, Tatsumura et al. have predicted a mobility-T_{inv} relationship providing the same drive current at a given L_{min} (L_g defined by off-state leakage current) by considering both mobility degradation and SCE suppression from T_{inv} scaling [31]. The comparison between the experimental data from this study and the extracted contour lines from [31] is shown in Fig. 5-14. As seen in Fig. 5-14, the mobility-T_{inv} slope for the intrinsic IL scaling (~20 cm^2/Vs per 0.1 nm) is shallower than the breakeven relationship for $L_{min} \leq 30$ nm as predicted in Ref. [31] (~40 cm^2/Vs per 0.1 nm). This indicates that it is indeed possible to improve the short-channel device performance by employing IL scaling in conjunction with aggressive L_g scaling for the 22nm-node and beyond. One can also see that the performance gain rapidly diminishes if the IL scaling is accompanied by extrinsic mobility degradation factors such as Al-induced degradation. Thus, selecting IL scaling method and V_t-tuning dipole layers causing no extrinsic mobility degradation will be the key to EOT scaling in the quasi-ballistic carrier transport era. From this perspective, the remote IL scavenging and the La-induced dipole is the ideal combination which enables ultimate EOT scaling down to 0.42nm without extrinsic mobility degradation.

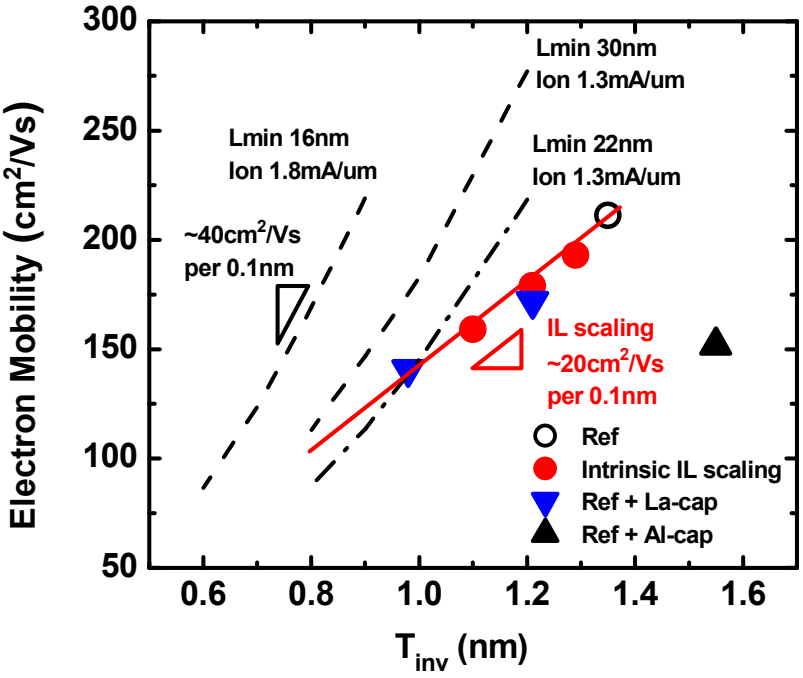


Fig. 5-14 Comparison of electron mobility at E_{eff} 1MV/cm as function of T_{inv} between experimental data in this study and extracted contour lines from Ref. 31. Contour lines providing the same drive current (I_{on}) at L_{min} 16nm, 22nm, and 30nm are shown.

5.5 Summary

We have experimentally clarified the mobility degradation mechanisms for intrinsic IL scaling and for La- and Al- induced dipoles. When IL scaling is employed to extend the EOT scaling using HfO_2 gate dielectrics, mobility degradation at a certain slope on a mobility vs EOT plot is inevitable due to the RPS effect from the HfO_2 layer. In addition, the RCS from the fixed charges localized at the SiO_2/HfO_2 interface is partially responsible for the mobility degradation. The former effect is intrinsic to high-κ and difficult to avoid. The latter effect can be mitigated by reducing the areal density of the fixed charges by keeping the high-κ film amorphous as discussed in Section 5.3.2. Gate-last process has an advantage in this regard. On the other hand, gate-first process renders a new pathway to EOT scaling down to 0.42nm by taking advantage of the automatically built-in thermal budget to trigger the oxygen transport from the IL to the scavenging metal electrode, albeit a potentially higher areal density of the fixed charges at the SiO_2 interface due to crystallization of HfO_2.

The difference in the crystallinity of HfO_2 and the oxygen transport tendency between gate-last and gate-first processes results in two different paths for device performance improvement, i.e. mobility improvement at a moderate EOT and aggressive EOT scaling at some expense of mobility. These findings provide a new perspective in selecting the integration scheme of high-κ metal gate devices. As for the aggressive EOT scaling path with gate-first process, we found that the La-induced dipoles do not degrade mobility from the intrinsic IL scaling baseline, while the Al-induced dipoles are accompanied with additional degradation mechanisms irrespective of the E_{eff} regime. Understanding of this difference is of paramount importance especially when these dipole layers are combined with IL scaling for the future nodes. We have demonstrated that when IL scaling and V_t-tuning are achieved without extrinsic mobility degradation, it is indeed possible to improve the short-channel device performance in the quasi-ballistic carrier transport era.

Reference

[1] S. Saito, D. Hisamoto, S. Kimura, and M. Hiratani: IEDM Tech. Dig., 2003, p. 797.

[2] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, H. Satake, N. Fukushima: Tech. Dig. Int. Electron Devices Meet., 2002, p. 621.

[3] M. A. Quevedo-Lopez, S. A. Krishnan, P. D. Kirsch, H. J. Li, J. H. Sim, C. Huffman, J. J. Peterson, B .H. Lee, G. Pant, B. E. Gnade, M. J. Kim, R. M. Wallace, D. Guo, H. Bu, T.P. Ma: Tech. Dig. Int. Electron Devices Meet., 2005, p.437.

[4] Y. Akasaka, K. Miyagawa, T. Sasaki, K. Shiraishi, S. Kamiyama, O. Ogawa, F. Ootsuka, Y. Nara: Tech. Dig. VLSI, 2005, p.228.

[5] A. Callegari, P. Jamison, E. Cartier, S. Zafar, E. Gusev, V. Narayanan, C. D'Emic, D. Lacey, F. R. McFeely, R. Jammy, M. Gribelyuk, J. Shepard, W. Andreoni, A. Curioni, C. Pignedolli: Tech. Dig. Int. Electron Devices Meet., 2004, p. 825.

[6] M. Fischetti, D. Neumayer, E. Cartier, J. Appl. Phys. **90** (2001) 4587.

[7] C. Choi, C-Y. Kang, S. J. Lee, M. S. Akbar, S. A. Krishnan, M. Zhang, H-S. Kim, T. Lee, I. Ok, F. Zhu, J. C. Lee: IEEE Electron Device Lett. **26** (2005) 7.

[8] M. Takahashi, A. Ogawa, A. Hirano, Y. Kamimuta , Y. Watanabe, K. Iwamoto, S. Migita, N. Yasuda, H. Ota, T. Nabatame, A. Toriumi: Tech. Dig. Int. Electron Devices Meet., 2007, p. 523.

[9] J. Huang, D. Heh, P. Sivasubramani, P. D. Kirsch, G. Bersuker, D. C. Gilmer, M. A. Quevedo-Lopez, M. M. Hussain, P. Majhi, P. Lysaght, H. Park, N. Goel, C. Young, C. S. Park, C. Park, M. Cruz, V. Diaz, P. Y. Hung, J. Price, H.–H.Tseng, R. Jammy: Tech. Dig. VLSI Symp., 2009, p. 34.

[10] K. Choi, H. Jagannathan, C. Choi, L. Edge, T. Ando, M. Frank, P. Jamison, M. Wang, E. Cartier, S. Zafar, J. Bruley, A. Kerber**,** B. Linder, A. Callegari**,** Q. Yang, S. Brown, J. Stathis**,** J. Iacoponi, V. Paruchuri, V. Narayanan: Tech. Dig. VLSI Symp., 2009, p.138.

[11] K. Tatsumura, T. Ishihara, S. Inumiya, K. Nakajima, A. Kaneko, M. Goto, S. Kawanaka, A. Kinoshita : Tech. Dig. Int. Electron Devices Meet., 2008, p. 25.

[12] J. Huang, P. D. Kirsch, D. Heh, C. Y. Kang, G. Bersuker, M. Hussain, P. Majhi, P. Sivasubramani, D. C. Gilmer, N. Goel, M. A. Quevedo-Lopez, C. Young, C. S. Park, C. Park, P. Y. Hung, J. Price, H. R. Harris, B. H. Lee, H.-H. Tseng, R. Jammy: Tech. Dig. Int. Electron Devices Meet., 2008, p. 45.

[13] M. Copel, S. Guha, N. Bojarczuk, E. Cartier, V. Narayanan, V. Paruchuri: Appl. Phys. Lett. **95** (2009) 212903.

[14] S. Toyoda, J. Okabayashi, H. Kumigashira, and M. Oshima, K. Yamashita, M. Niwa, K. Usuda, G. L. Liu: J. Appl. Phys. **97** (2005) 104507.

[15] A. S. Foster, F. Lopez Gejo, A. L. Shluger, R. M. Nieminen: Phys. Rev. B **65** (2002) 174117.

[16] H. Watanabe: Appl. Phys. Lett. **83**, 4175 (2003).

[17] H. Ota, A. Hirano, Y. Watanabe, N. Yasuda, K. Iwamoto, K. Akiyama, K. Okada, S. Migita, T. Nabatame, A. Toriumi: Tech. Dig. - Int. Electron Devices Meet. 2007, p. 65.

[18] G. Bersuker, C. S. Park, J. Barnett, P. S. Lysaght, P. D. Kirsch, C. D. Young, R. Choi, B. H. Lee, B. Foran, K. van Benthem, S. J. Pennycook: J. Appl. Phys. **100** (2006) 094108.

[19] M. Goto, S. Kawanaka, S. Inumiya, N. Kusunoki, M. Saitoh, K. Tatsumura, A. Kinoshita, S. Inaba, Y. Toyoshima: Tech. Dig. VLSI Symp., 2009, p. 214.

[20] K. Maitra, M. M. Frank, V. Narayanan, V. Misra, E. A. Cartier: J. Appl. Phys. **102** (2007) 114507.

[21] M. Copel, E. Cartier, F. M. Ross: Appl. Phys. Lett. **78** (2001) 1607.

[22] H. Arimura, R. Haight, S. L. Brown, A. Kellock, A. Callegari, M. Copel, H. Watanabe, V. Narayanan, T. Ando: Appl. Phys. Lett. **96** (2010) 132902.

[23] J. Li and T. P. Ma: J. Appl. Phys. **62** (1987) 10.

[24] S. Takagi, T. Irisawa, T. Tezuka, T. Numata, S. Nakaharai, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake, M. Shichijo, R. Nakane, S. Sugahara, M. Takenaka, N. Sugiyama: IEEE Trans. Electron Devices **55** (2008) 21.

[25] M. Saitoh and K. Uchida: Tech. Dig. Int. Electron Devices Meet., 2006, p. 261.

[26] K. Natori: J. Appl. Phys. **76** (1994) 4789.

[27] A. Lochtefeld and D. A. Antoniadis: IEEE Electron Device Lett. **22** (2001) 95.

[28] M. S. Lundstrom: IEEE Electron Device Lett. **22** (2001) 293.

[29] K. Henson, H. Bu, M. H. Na, Y. Liang, U. Kwon, S. Krishnan, J. Schaeffer, R. Jha, N. Moumen, R. Carter, C. DeWan, R. Donation, D. Guo, M. Hargrove, W. He, R. Mo, R. Ramachandran, K. Ramani, K. Schonenberg, Y. Tsang, X. Wang, M. Gribelyuk, W. Yan, J. Shepard, E. Cartier, M. Frank, E. Harley, R. Arndt, R. Knarr, T. Bailey, B. Zhang, K. Wong, T. Graves-Abe, E. Luckowski, D-G. Park, V. Narayanan, M. Chudzik, M. Khare: Tech. Dig. Int. Electron Devices Meet., 2008, p. 645.

[30] K. Takeuchi, T. Tatsumi, A. Furukawa: Tech. Dig. Int. Electron Devices Meet., 1997, p. 841.
[31] K. Tatsumura, M. Goto, S. Kawanaka, A. Kinoshita: Tech. Dig. Int. Electron Devices Meet., 2009, p. 465.

CHAPTER 6 General conclusions

The primary purpose of this study is to establish methodologies of V_t control and EOT scaling of the high-κ metal gate stacks for the 22-nm-node and beyond and to obtain a general guideline for performance improvement in the material-driven scaling era by focusing on carrier mobility of MOSFETs. The main achievements of this study are summarized below.

In Chapter 2, an ALD process for HfSiOx was established. The coinjection ALD process of $HfSiO_x$ exhibited a sign of catalytic effect. By taking advantage of this effect, the conformal step coverage of HfSiOx in the DT of the 45-nm-node eDRAM was achieved. In addition, the mechanism underlying leakage current was revealed to be PF current originating from residual carbon. This finding enables leakage current improvement of Hf-based high-κ films by using residual carbon concentration in the films as metrics. This method should be applicable to Hf-based high-κ films deposited from metal organic precursors in general. Finally in this Chapter, the DT capacitors of the 65 nm-node were fabricated and we demonstrated a capacitance enhancement of 50% as compared with the conventional SiON film. It can be concluded that the Al_2O_3/HfSiON/Si_3N_4 stack obtained by the newly developed ALD process is one of the promising candidates for the DT dielectric for the 45 nm-node-eDRAM and beyond.

In Chapter 3, a HfO_2/Hf-Si gate stack was proposed for n-MOSFETs using gate-last process. The RHEED, AR-XPS, and TEM analyses revealed that the crystallization of HfO_2 and the metal diffusion into the bottom-IL are the primary sources of mobility degradation. It was found that these degradation modes can be avoided by the careful optimization of the HfO_2 thickness below the critical value and by the Si-rich Hf-Si electrode. Moreover, the EWF of the optimized HfO_2/Hf-Si gate stack is located within 50 mV from the Si band edge (E_c). Based on these findings, we succeeded in scaling the T_{inv} of n-MOSFET down to 1.47 nm without degradation of the high field mobility for the first time. The findings in this Chapter suggest that EWF can be controlled predominantly by the vacuum workfunction of the metal

electrode in gate-last process if an appropriate material is employed. In addition, the low thermal budget of gate-last process enables us to keep the HfO_2 dielectrics amorphous, resulting in higher carrier mobilities.

In Chapter 4, EWF control and EOT scaling for gate-first process were discussed using novel process technologies. We demonstrated EWF control by means of the TaC electrode thickness and the PMN temperature in conjunction with La-cap layers. This finding highlights the importance of precise control of depth profiles of V_t-tuning elements in gate-first process. Depth profile modification by means of post metal anneal opens up a new pathway for EWF control of high-κ/metal gate stacks. As for EOT scaling, a novel technique utilizing metal-gate-induced remote IL scaling is demonstrated and the kinetics underlying this process is clarified. The remote IL scavenging technique enables ultimate scaling of HfO_2 down to EOT 0.42 nm with gate-first process. This technique shows advantages in carrier mobility and gate leakage current over conventional IL scaling schemes. We found that the EOT scaling by the remote IL scavenging and the V_{fb} tuning by the La- and Al-dipole are additive, which makes this technique a viable option for CMOS integration with gate-first process.

In Chapter 5, we experimentally clarified the mobility degradation mechanisms for intrinsic IL scaling and for La- and Al- induced dipoles. When IL scaling is employed to extend the EOT scaling using HfO_2 gate dielectrics, mobility degradation at a certain slope on a mobility vs EOT plot is inevitable due to the RPS effect from the HfO_2 layer. In addition, the RCS from the fixed charges localized at the SiO_2/HfO_2 interface is partially responsible for the mobility degradation. The former effect is intrinsic to high-κ and difficult to avoid. The latter effect can be mitigated by reducing the areal density of the fixed charges by keeping the high-κ film amorphous. Gate-last process has an advantage in this regard. On the other hand, gate-first process renders a new pathway to EOT scaling down to 0.42nm by taking advantage of the automatically built-in thermal budget to trigger the oxygen transport from the IL to the scavenging metal electrode, albeit a potentially higher areal density of the fixed charges at the SiO_2 interface due to crystallization of HfO_2. The difference in the

crystallinity of HfO_2 and the oxygen transport tendency between gate-last and gate-first processes results in two different paths for device performance improvement, i.e. mobility improvement at a moderate EOT and aggressive EOT scaling at some expense of mobility. These findings provide a new perspective in selecting the integration scheme of high-κ metal gate devices. As for the aggressive EOT scaling path with gate-first process, we found that the La-induced dipoles do not degrade mobility from the intrinsic IL scaling baseline, while the Al-induced dipoles are accompanied with additional degradation mechanisms irrespective of the E_{eff} regime.

In summary, the materials and processes for EWF control and EOT scaling of high-κ metal gate stacks using both gate-last and gate-first schemes were developed in this study. A universal physical model to explain the relationship between electron mobility and EOT was established by focusing on the effects of crystallinity of HfO_2 layer, IL scaling, and V_t-tuning dipole layers. This model provides a new perspective in selecting the integration schemes of high-κ metal gate devices. We demonstrated that the remote IL scavenging combined with EWF tuning by the La-induced dipole enables ultimate EOT scaling down to 0.42nm without extrinsic mobility degradation using gate-first process. Based on these understandings, IL scaling using HfO_2 gate dielectrics was proposed as the potential EOT scaling strategy in the quasi-ballistic carrier transport era. We demonstrated the feasibility of performance improvement using this approach toward the end of the CMOS roadmap.

Acknowledgements

I would like to express my very best gratitude to my supervisor, Prof. Heiji Watanabe, for his kind guidance, valuable suggestions, boundless energy, and continuous encouragement through out this study. I also deeply appreciate the valuable comments and helpful instructions from Prof. Kazuyoshi Itoh and Prof. Yoshizo Takai.

Part of this study was carried out through my work at Atsugi Technology Center of Sony Corporation and later at IBM T. J. Watson Research Center. First of all, I would like to thank my mentor, Mr. Tomoyuki Hirano, who introduced me to this exciting research topic when I joined Sony in 2003. Much gratitude is also due to Ms. Kaori Tai, Mr. Shinpei Yamaguchi, Mr. Koji Watanabe, Mr. Naoyuki Sato, Mr. Susumu Hiyama, Mr. Takayoshi Kato, Mr. Yoshiya Hagimoto, Mr. Shinichi Yoshida, Mr. Ryo Yamamoto, Mr. Yasushi Tateshita, Mr. Masaki Saito, Dr. Yukio Tagawa, and Dr. Hitoshi Wakabayashi for the valuable cooperation and discussions to bring the high-κ project to success. I also sincerely thank Mr. Hayato Iwamoto and Mr. Shingo Kadomura for their management support throughout my carrier at Sony. Dr. Masaki Yoshizawa, Mr. Yoshiaki Kikuchi, Mr. Atsunobu Isobayashi, Mr. Tsutomu Shimayama, Dr. Minoru Sugawara, Mr. Isao Mita, Dr. Junli Wang, and Mr. Tenko Yamashita deserve my special thanks for the friendship and teamwork during the assignment in the U.S. I also appreciate the management support from Mr. Masanori Tsukamoto and Mr. Toshiaki Hasegawa in this period.

I would like to appreciate the fruitful collaboration on the synchrotron radiation photoemissions spectroscopy with Dr. Satoshi Toyoda and Prof. Masaharu Oshima of the University of Tokyo, which gave a scientific backbone to this study.

My special thanks go to the members of the Laboratory of Applied Surface Science, Associate Prof. Takayoshi Shimura, Dr. Takuji Hosoi, Mr. Katsuhiro Kutsuki, Mr. Naomu Kitano, Mr. Takashi Yamamoto, and Ms. Mariko Suga for their help, suggestions, and friendship. I would like to especially thank Mr. Hiroaki Arimura for his dedicated summer intern work and the outstanding achievement.

I am deeply grateful to Dr. Vijay Narayanan for his kind guidance, valuable suggestions, and management support to complete this study. Special thanks to my colleagues at IBM T. J. Watson Research Center, Dr. Changhwan Choi, Dr. Martin M.

Frank, Dr. Richard Haight, Dr. Matthew Copel, Dr. Alessandro Callegari, Dr. Eduard Cartier, Dr. Young-Hee Kim, Dr. Sufi Zafar, Dr. John Bruley, Dr. Marinus Hopstaken, Dr. Barry Linder, Dr. Hemanth Jagannathan, Dr. Vamsi K. Paruchuri, Dr. Dechao Guo, Dr. Unoh Kwon, Dr. Siddarth Krishnan, Dr. Lisa F. Edge, Mr. Stephen L. Brown, Ms. Dianne Lacey, Mr. Gil Singco, and Mr. Yuri Ostrovski for the great teamwork, friendship and valuable discussions on my research. I would also like to thank my alliance partners, Dr. Kisik Choi, Dr. Andreas Kerber, and Dr. Jamie Schaeffer of GLOBALFOUNDRIES, Mr. Ryosuke Iijima, Dr. Takeshi Watanabe, Dr. Yoshinori Tsuchiya, and Mr. Hirohisa Kawasaki of Toshiba America Electronic Components for fruitful discussions, collaborations, and friendship. I would like to give my special thank to Dr. Tze-Chiang Chen for providing me a chance to work in IBM T. J. Watson Research Center and to continue my research on high-κ metal gate technology.

I would like to thank my parents for being an integral part of my quest and endeavor right from the word go. I am what I am today because of their constant encouragement and unflinching support throughout my early years. And last but not the least, a special word of thanks to my wife and son, Seiko and Koh, who stood beside me through the long journey across the Pacific Ocean and never let me lose sight of my goal.

May 2010

Tuckahoe, NY

Publication list

Original research reports: Journal papers (first author)

1. Takashi Ando, Naoyuki Sato, Susumu Hiyama, Tomoyuki Hirano, Kojiro Nagaoka, Hitoshi Abe, Atsushi Okuyama, Hajime Ugajin, Kaori Tai, Shigeru Fujita, Koji Watanabe, Ryota Katsumata, Jun Idebuchi, Takashi Suzuki, Toshiaki Hasegawa, Hayato Iwamoto, Shingo Kadomura, *Application of HfSiON to Deep-Trench Capacitors of Sub-45-nm-Node Embedded Dynamic Random-Access Memory*, Jpn. J. Appl. Phys. **45** (2006) 3165.

2. Takashi Ando, Takayoshi Shimura, Heiji Watanabe, Tomoyuki Hirano, Shinichi Yoshida, Kaori Tai, Shinpei Yamaguchi, Hayato Iwamoto, Shingo Kadomura, Satoshi Toyoda, Hiroshi Kumigashira, and Masaharu Oshima, *Mechanism of Carrier Mobility Degradation Induced by Crystallization of HfO_2 Gate Dielectrics*, Appl. Phys. Express **2** (2009) 071402.

3. Takashi Ando, Tomoyuki Hirano, Kaori Tai, Shinpei Yamaguchi, Shinichi Yoshida, Hayato Iwamoto, Shingo Kadomura, and Heiji Watanabe, *Band-Edge High-Performance Metal-Gate/High-k nMOSFET Using Hf-Si/HfO2 Stack*, IEEE Trans. Electron Devices **56** (2009) 3223.

4. Takashi Ando, Tomoyuki Hirano, Kaori Tai, Shinpei Yamaguchi, Shinichi Yoshida, Hayato Iwamoto, Shingo Kadomura, and Heiji Watanabe, *Low Threshold Voltage and High Mobility nMOSFET Using Hf-Si/HfO_2 Gate Stack Fabricated by Gate-Last Process*, Jpn. J. Appl. Phys. **49** (2010) 016502.

5. Takashi Ando, Matt Copel, John Bruley, Martin M. Frank, Heiji Watanabe, and Vijay Narayanan, *Physical Origins of Mobility Degradation in Extremely Scaled SiO_2/HfO_2 Gate Stacks with La and Al Induced Dipoles*, Appl. Phys. Lett. **96** (2010)132904.

6. Takashi Ando, Martin M. Frank, Kisik Choi, Changhwan Choi, Richard Haight, Matt Copel, Hiroaki Arimura, Heiji Watanabe, and Vijay Narayanan, *Ultimate EOT Scaling (< 5Å) Using Hf-based High-κ Gate Dielectrics and Impact on Carrier Mobility*, ECS Trans. **28** [1] (2010) 115.

Original research reports: Journal papers (co-author)

1. Satoshi Toyoda, Jun Okabayashi, Haruhiko Takahashi, Masaharu Oshima, Dong-Ick Lee, Shiyu Sun, Steven Sun, Piero A. Pianetta, Takashi Ando, and Seiichi Fukuda, *Nitrogen doping and thermal stability in HfSiOxNy studied by photoemission and x-ray absorption spectroscopy*, Appl. Phys. Lett. **87** (2005) 182908.

2. Alessandro Callegari, Katya Babich, Sufi Zafar, Takashi Ando, Paul Batson, and Vijay Narayanan, *Materials and Process Integration Issues in Metal Gate/high-k Stacks and Their Dependence on Device Performance*, ECS Trans. **11** [4] (2007) 265.

3. Kaori Tai, Shinpei Yamaguchi, Kazuki Tanaka, Tomoyuki Hirano, Itaru Oshiyama, Salam Kazi, Takashi Ando, Masashi Nakata, Mayumi Yamanaka, Ryo Yamamoto, Sayuri Kanda, Yasushi Tateshita, Hitoshi Wakabayashi, Yukio Tagawa, Masanori Tsukamoto, Hayato Iwamoto, Masaki Saito, Naoki Nagashima, and Shingo Kadomura, *PMOSFET Vth Modulation Technique using Fluorine Treatment through ALD-TiN Suitable for CMOS Devices,* Jpn. J. Appl. Phys. **47** (2008) 2345.

4. Itaru Oshiyama, Kaori Tai, Tomoyuki Hirano, Shinpei Yamaguchi, Kazuki Tanaka, Yoshiya Hagimoto, Takayuki Uemura, Takashi Ando, Koji Watanabe, Ryo Yamamoto, Sayuri Kanda, Junli Wang, Yasushi Tateshita, Hitoshi Wakabayashi, Yukio Tagawa, Masanori Tsukamoto, Hayato Iwamoto, Masaki Saito, Masaharu Oshima, Satoshi Toyoda, Naoki Nagashima, and Shingo Kadomura, *Tinv Scaling and Jg Reducing for nMOSFET with HfSix/HfO2 Gate Stack by Interfacial Layer Formation Using Ozone Water Treatment Process,* Jpn. J. Appl. Phys. **47** (2008) 2379.

5. Changhwan Choi, Takashi Ando, Eduard Cartier, Martin M. Frank, Ryosuke Iijima, and Vijay Narayanan, *Quasi-damascene metal gate/high-k CMOS using oxygenation through gate electrodes*, Microelectronic Engineering **86** (2009) 1737.

6. Hiroaki Arimura, Richard Haight, Stephen L. Brown, Andrew Kellock, Alessandro Callegari, Matthew Copel, Heiji Watanabe, Vijay Narayanan, and Takashi Ando, *Temperature-dependent La- and Al-induced dipole behavior monitored by femtosecond pump/probe photoelectron spectroscopy*, Appl. Phys. Lett. **96** (2010) 132902.

7. Marinus Hopstaken, John Bruley, Dirk Pfeiffer, Matt Copel, Martin M. Frank, Eduard Cartier, Takashi Ando, and Vijay Narayanan, *Oxygen Transport in High-κ Metal Gate Stacks and Physical Characterization by SIMS Using Isotopic Labeled Oxygen*, ECS Trans. **28** [1] (2010) 105.

Original research reports: Refereed conference proceedings (first author)

1. T. Ando, N. Sato, S. Hiyama, T. Hirano, K. Nagaoka, H. Abe, A. Okuyama, H. Ugajin, K. Tai, S. Fujita, K. Watanabe, R. Katsumata, J. Idebuchi, T. Suzuki, T. Hasegawa, H. Iwamoto, S. Kadomura, *Application of HfSiON to Deep Trench Capacitors of Sub-45nm Node Embedded DRAM*, Extended Abstracts of the International Conference on Solid State Devices and Materials, 2005, p. 186.

2. T. Ando, T.Hirano, K.Tai, S.Yamaguchi, T.Kato, Y.Hagimoto, K.Watanabe, R. Yamamoto, S. Kanda, K. Nagano, S.Terauchi, Y.Tateshita, Y.Tagawa, M.Saito, H. Iwamoto, S.Yoshida, H.Watanabe, N.Nagashima and S.Kadomura, *Sub-1nm EOT $HfSi_x/HfO_2$ Gate Stack Using Novel Si Extrusion Process for High Performance Application*, Tech. Dig. VLSI Symp., 2006, p.208.

3. T. Ando, T. Hirano, K. Tai, S. Yamaguchi, K. Tanaka, I. Oshiyama, M. Nakata, K. Watanabe, R. Yamamoto, S. Kanda, Y. Tateshita, H. Wakabayashi, Y. Tagawa, M. Tsukamoto, H. Iwamoto, M. Saito, S. Toyoda, H. Kumigashira, M. Oshima, N. Nagashima, S. Kadomura, *High Performance and High Reliability Dual Metal CMOS Gate Stacks Using Novel High-k Bi-layer Control Technique*, Tech. Dig. VLSI-TSA, 2007, p. 46.

4. Takashi Ando, Alessandro Callegari, Changhwan Choi, Marinus Hopstaken, John Bruley, Michael Gordon, Heiji Watanabe, and Vijay Narayanan, *Effective Work Function Control of TaC/High-κ Gate Stack by Post Metal Nitridation*, Abstracts of 40th IEEE Semiconductor Interface Specialists Conference, 2009, 9-2.

5. T. Ando, M. M. Frank, K. Choi, C. Choi, J. Bruley, M. Hopstaken, M. Copel, E. Cartier, A. Kerber, A. Callegari, D. Lacey, S. Brown, Q. Yang, and V. Narayanan, *Understanding Mobility Mechanisms in Extremely Scaled HfO_2 (EOT 0.42 nm) Using Remote Interfacial Layer Scavenging Technique and V_t-tuning Dipoles with Gate-First Process,* Tech. Dig. Int. Electron Devices Meet., 2009, p.423.

Invited presentations

6. *Sub-1nm EOT $HfSi_x/HfO_2$ Gate Stack Using Novel Si Extrusion Process for High Performance Application*, JSAP 12th Gate Stack Conference, Mishima, Japan, Feb 1, 2007.

7. *Opportunities and Challenges of ALD for CMOS Devices in 45-nm Generation and Beyond*, 7th International Conference on Atomic Layer Deposition, San Diego, USA, Jun 25, 2007.

8. *Ultimate EOT Scaling (< 5Å) Using Hf-based High-κ Gate Dielectrics and Impact on Carrier Mobility,* 217th ECS Meeting, Vancouver, Canada, Apr 25, 2010.

Original research reports: Refereed conference proceedings (co-author)

1. T. Hirano, T. Ando, K. Tai, S. Yamaguchi, T. Kato, S. Hiyama, Y. Hagimoto, S. Takesako, N. Yamagishi, K. Watanabe, R. Yamamoto, S. Kanda, S. Terauchi, Y. Tateshita, Y. Tagawa, H. Iwamoto, M. Saito, S. Kadomura and N. Nagashima, *High Performance nMOSFET with HfSix/HfO2 Gate Stack by Low Temperature Process,* Tech. Dig. Int. Electron Devices Meet., 2005, p.911.

2. S. Yamaguchi, K. Tai, T. Hirano, T. Ando, S. Hiyama, J. Wang, Y. Hagimoto, Y. Nagahama, T. Kato, K. Nagano, M. Yamanaka, S. Terauchi, S. Kanda, R. Yamamoto, Y. Tateshita, Y. Tagawa, H. Iwamoto, M. Saito, N. Nagashima and S. Kadomura, *High Performance Dual Metal Gate CMOS with High Mobility and Low Threshold Voltage Applicable to Bulk CMOS Technology*, Tech. Dig. VLSI Symp., 2006, p.192.

3. K. Tai, T. Hirano, S. Yamaguchi, T. Ando, S. Hiyama, J. Wang, Y. Nagahama, T. Kato, M. Yamanaka, S. Terauchi, S. Kanda, R. Yamamoto, Y. Tateshita, Y. Tagawa, H. Iwamoto, M. Saito, N. Nagashima and S. Kadomura, *High Performance pMOSFET with ALD-TiN/HfO2 Gate Stack on (110) Substrate by Low Temperature Process*, Tech. Dig. ESSDERC, 2006, p. 121.

4. A. Callegari, K. Babich, S. Zafar, T. Ando, P. Batson, and V. Narayanan, *Materials and Process Integration Issues in Metal Gate/high-k Stacks and Their Dependence on Device Performance*, 212th ECS Meeting, 2007.

5. S. Yoshida, Y. Kita, T. Ando, K. Tai, H. Iwamoto, T. Shimura, H. Watanabe and K. Yasutake, *Physical and Electrical Characterization of HfSix/HfO2 Gate Stacks for High-Performance nMOSFET Application*, Abstracts of 37th IEEE Semiconductor Interface Specialists Conference, 2006, 3-3.

6. Y. Tateshita, J. Wang, K. Nagano, T. Hirano, Y. Miyanami, T. Ikuta, T. Kataoka, Y. Kikuchi, S. Yamaguchi, T. Ando, K. Tai, R. Matsumoto, S. Fujita, C. Yamane, R. Yamamoto, S. Kanda, K. Kugimiya, T. Kimura, T. Ohchi, Y. Yamamoto, Y. Nagahama, Y. Hagimoto, H. Wakabayashi, Y. Tagawa, M. Tsukamoto, H. Iwamoto, M. Saito, S. Kadomura and N. Nagashima, *High-Performance and Low-Power CMOS Device Technologies Featuring Metal/High-k Gate Stacks with Uniaxial Strained Silicon Channels on (100) and (110) Substrates*, Tech. Dig. Int. Electron Devices Meet., 2006, p.63.

7. M. Chudzik, B. Doris, R. Mo, J. Sleight, E. Cartier, C. Dewan, D. Park, H. Bu, W. Natzle, W. Yan, C. Ouyang, K. Henson, D. Boyd, S. Callegari, R. Carter, D. Casarotto, M. Gribelyuk, M. Hargrove, W. He, Y. Kim, B. Linder, N. Moumen, V. K. Paruchuri, J. Stathis, M. Steen, A. Vayshenker, X. Wang, S. Zafar, T. Ando, R. Iijima, M. Takayanagi, V. Narayanan, R. Wise, Y. Zhang, R. Divakaruni, M. Khare, and T. C. Chen, *High-Performance High-k/Metal Gates for 45nm CMOS and Beyond with Gate-First Processing*, Tech. Dig. VLSI Symp., 2007, p.194.

8. K. Tai, S. Yamaguchi, K. Tanaka, T. Hirano, I. Oshiyama, S. Kazi, T. Ando, M. Nakata, M. Yamanaka, R. Yamamoto, S. Kanda, Y. Tateshita, H. Wakabayashi, Y. Tagawa, M. Tsukamoto, H. Iwamoto, M. Saito, N. Nagashima, and S. Kadomura, *PMOSFET Vth Modulation Technique using Fluorine Treatment through ALD-TiN*

Suitable for CMOS Devices, Extended Abstracts of the International Conference on Solid State Devices and Materials, 2007, p. 10.

9. I. Oshiyama, K. Tai, T. Hirano, S. Yamaguchi, K. Tanaka, Y. Hagimoto, T. Uemura,
T. Ando, K. Watanabe, R. Yamamoto, S. Kanda, J. Wang, Y. Tateshita, H. Wakabayashi, Y. Tagawa, M. Tsukamoto, H. Iwamoto, M. Saito, M. Oshima, S. Toyoda, N. Nagashima, and S. Kadomura, *Tinv Scaling and Jg Reducing for nMOSFET with HfSix/HfO2 Gate Stack by Interfacial Layer Formation Using Ozone Water Treatment Process*, Extended Abstracts of the International Conference on Solid State Devices and Materials, 2007, p. 848.

10. S. Mayuzumi, S. Yamakawa, D. Kosemura, M. Takei, J. Wang, T. Ando, Y. Tateshita, M. Tsukamoto, H. Wakabayashi, T. Ohno, A. Ogura, and N. Nagashima, *Channel-Stress Study on Gate-Size Effects for Damascene-Gate pMOSFETs with Top-Cut Compressive Stress Liner and eSiGe*, Tech. Dig. VLSI Symp., 2008, p.126.

11. C. Choi, T. Ando, Z. Karim, S. Ramanathan, and V. Narayanan, *Modulating Work Function for pFET with AVD Ru-based & TaN-based Gate Electrodes*, Abstracts of 39th IEEE Semiconductor Interface Specialists Conference, 2008, 8-4.

12. Changhwan Choi, Takashi Ando, Eduard Cartier, Martin M. Frank, Ryosuke Iijima, and Vijay Narayanan, *Quasi-damascene metal gate/high-k CMOS using oxygenation through gate electrodes*, INFOS, 2009.

13. K. Choi, H. Jagannathan, C. Choi, L. Edge, T. Ando, M. Frank, P. Jamison, M. Wang, E. Cartier, S. Zafar, J. Bruley, A. Kerber**,** B. Linder, A. Callegari**,** Q. Yang, S. Brown, J. Stathis**,** J. Iacoponi, V. Paruchuri, and V. Narayanan, *Extremely Scaled Gate-First High-k/Metal Gate Stack with EOT of 0.55 nm Using Novel Interfacial Layer Scavenging Techniques for 22nm Technology Node and Beyond*, Tech. Dig. VLSI Symp., 2009, p.138.

14. E. Cartier, M. Steen, B. P. Linder, T. Ando, R. Iijima, M. Frank, J. S. Newbury, Y. H. Kim, F. R. McFeely, M. Copel, R. Haight, C. Choi, A. Callegari, V. K. Paruchuri, and V. Narayanan, *pFET Vt control with HfO2/TiN/poly-Si gate stack using a lateral oxygenation process,* Tech. Dig. VLSI Symp., 2009, p.42.

15. Y. H. Kim, K. Schonenberg, T. Ando, D. Neumayer, R. Mo, H. Bu, J. Sleight, E. Cartier, N. Moumen, R. Jha, W. Yan, Y. Liang, V. Narayanan, M. P. Chudzik, and S. Guha, *Novel Single Metal Gate CMOS Integration with Effective Workfunction Modulation by a Differential Spacer:Manipulation of Oxygen Vacancy,* Extended Abstracts of the International Conference on Solid State Devices and Materials, 2009, C-6-3.
16. Martin M. Frank, Takashi Ando, Changhwan Choi, Kisik Choi1, and Vijay Narayanan, *Interfacial Layer Scaling Strategies for Metal Gate / High-k Stacks on Silicon,* MRS Spring Meeting, 2010.

17. H. Arimura, T. Ando, S. Brown, A. Kellock, A. Callegari, M. Copel, R. Haight, H. Watanabe, and V. Narayanan, *Optimization of composition ratio in La-Al-O gate dielectrics for advanced metal/higher-k devices,* MRS Spring Meeting, 2010.

18. M.J.P. Hopstaken, J. Bruley, D. Pfeiffer, M. Copel, M. M. Frank, E. Cartier, T. Ando, and V. Narayanan, *Oxygen Transport in High-κ Metal Gate Stacks and Physical Characterization by SIMS Using Isotopic Labeled Oxygen*, 217th ECS Meeting, 2010.

Curriculum vitae

Takashi Ando was born in Nagoya, Aichi, Japan, on October 30th, 1976, the son of Toshiya Ando and Yukiko Ando. After graduating from Eiko Gakuen High School, Tamanawa, Kanagawa, Japan, in 1995, he majored in Materials Science at the University of Tokyo, Tokyo, Japan, and graduated with the B.S. in 1999. He continued his study at the graduate school of the University of Tokyo and earned the M.E. degree in materials science in 2001. In April 2001, he joined Fujitsu Ltd., Isawa-gun, Iwate, Japan, where he engaged in the process integration of ferroelectric random access memory (FeRAM). In October 2003, He moved to Sony Corporation, Atsugi, Kanagawa, Japan, and initiated his research on high-κ and metal gate materials and the application to the advanced CMOS devices. He was assigned to IBM T. J. Watson Research Center, Yorktown Heights, New York, USA, to engage in the joint research project between IBM Corporation, Toshiba Corporation, and Sony Corporation in the period between July 2006 and December 2007. After the completion of the joint project, he has been a Research Staff Member at IBM T. J. Watson Research Center since March 2008. In addition, he has been pursuing the Ph.D. degree in advanced science and biotechnology at Osaka University, Osaka, Japan, since October 2008. His research interests include ultimate scaling of high-κ gate dielectrics, workfunction control of high-κ metal gate stacks, and understanding of carrier mobility degradation mechanisms, for continued CMOS device scaling toward the end of the roadmap.