# Micromachining of Si by Wet Processes Using Metal Catalysts: Boring, Cu Electrodeposition, Grooving, and Slicing

By

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**March 2010**

# Micromachining of Si by Wet Processes Using Metal Catalysts: Boring, Cu Electrodeposition, Grooving, and Slicing

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# *Contents*

# *Abstract*

By using metal catalysts, Si is oxidatively etched at the Si/metal interface in HF solution. As a result, nanometer sized pores can be formed in Si using nanometer-sized metal particles (Pt, Au, Ag, etc.). This phenomenon was studied in detail with the aim of developing new methods for machining Si devices and slicing Si ingots. The study consists of two parts. One is the formation of micrometer-sized pores in Si wafers using Au particles as catalysts and $H_2O_2$ as a chemical oxidant and filling the pores with Cu to make vertical interconnects through the Si wafer. The other is an electrochemical grooving of Si using catalyst wire electrodes, to which anodic potential is applied. After explaining the background of the study in Chapter 1, the two approaches are described in the following chapters.

(1) Formation of vertical pores in silicon by wet etching and Cu electrodeposition (Chapter 2 and Chapter 3)

In recent years, smaller, lighter portable electronic devices with higher performance are demanded by consumers. An approach to making these devices is application of 3D packaging, which uses through-wafer interconnects (TWIs), to electronic devices. However, TWIs are conventionally fabricated by such costly and complicated processes as deep reactive ion etching and physical vapor deposition.

To make pores in Si for interconnects, formation of pores with diameters of 5 - 20 μm in Si was studied by wet etching using Au particles as catalysts. Although it was difficult to make these pores using single Au particles with such large sizes, they were successfully formed using aggregates of 1-μm-sized Au particles. The aggregate structure was useful to enhance the diffusion of etching solution to the Si/Au interface and to control the direction of the pores. The concentrations of HF and $H_2O_2$ in the etching solution were also important to control the

morphology of the pores.

To make interconnects through a Si wafer, metal wires have to be inserted through the pores, which is a laborious process. Because the pores formed by the wet process have Au particles at the ends, the Au particles can be used as seeds for electrochemical deposition of Cu. By electroplating Cu from an aqueous solution of $CuSO_4$ on the Si wafer, in which pores had been made using Au aggregates, Cu was selectively deposited on the surface of the Au particles and Cu wires grew up toward the Si surface. The selective Cu deposition in the pores was achieved because the exchange current density for Cu electrodeposition was much higher on Au/Cu than on Si. To apply the Cu wires to the interconnects, a method for controlling the positions needs to be developed.

(2) Electrochemical grooving and slicing of Si wafers and blocks using catalytic wire electrodes in HF solution (Chapters 4-6)

Wafer slicing is an indispensable technique for the fabrication of Si wafers in semiconductor and photovoltaic industries. Currently, multi-wire slicing is the dominant slicing method because it can slice an ingot into hundreds of wafers at the same time. However, the kerf loss and mechanical damages on silicon crystal are unavoidably produced during the slicing process. The kerf loss resulted from multi-wire slicing is typically about 200 μm, which is almost the same as the thickness of Si wafers for devices and solar cells.

An entirely new method for slicing Si was studied by using the mechanism of pore formation by metal catalysts. For this purpose, catalytic wire electrodes, to which anodic potentials were applied, were used. In the experiments, two catalytic wires ($\varphi$=50 μm) were set on a Teflon holder and brought into contact with the Si sample. By applying 2 V vs Ag/AgCl to the catalytic wires in a HF solution, grooves with about 53 μm in width were formed in silicon. The width of the grooves was nearly the same as the diameter of the Pt

wires. Such a small kerf loss is advantageous to the process. Another advantage is that the process does not cause mechanical damage to Si wafers. By this electrochemical method, a 700-μm-thick sliced wafer was fabricated from a Si block. The pressure at the Si/Pt interface was critical to enhance the slicing speed.

# *CHAPTER 1*

*General Introduction*

# Chapter 1

# General Introduction

## Basic outline of silicon

Silicon (Si) is the second most abundant element in the crust after oxygen, making up about 25.7 % of the crust by mass. In the past five decades, silicon has significantly impacted the modern world's economy and lifestyle of human being because of the use of silicon wafers in the manufacture of discrete electronic devices. Ultra-pure silicon is conventionally utilized to produce silicon wafers, which are the main substrates for fabricating solar cells, integrated circuits (IC) chips and other electronic devices. To increase the conductivity, ultra-pure silicon materials are normally doped. The common dopants for p-type and n-type silicon are boron (acceptors) and phosphorus (donors), respectively.

Nowadays, Si is the most important material in the semiconductor industry for fabricating large-scale integration (LSI) and ultra large-scale integration (ULSI). It is also the indispensable material in microelectromechanical (MEMS) systems and photovoltaic (PV) devices. For production of Si wafers, growth of a silicon ingot is required, normally grown (crystal growth) by Czochralski process [1]. To turn a silicon ingot into final Si wafers, a sequence of machining and chemical processes is required, such as slicing, flattening, etching and polishing. After fabrication of final Si wafers, microstructures in Si substrates, such as interconnects, are constructed.

In this chapter, pore formation in Si, etching methods and some of important machining processes and related academic research are reviewed, which form the background of this thesis.

## 1.1 Formation of porous structures in Si

Formation of porous structures in silicon is an essential manufacturing step in the semiconductor industry. Porous structures fabricated in silicon with well-controlled feature sizes have received a great attentions. In the last two decades, it has been performed in various electronic devices such as trench capacitors [2,3], membrances [4-6], solar cells [7-9] and through-wafer interconnects [10,11]. Depending on these applications, the diameter and the depth of pores are quite divergent. Porous structures in silicon are usually formed by etching, which means the controlled removal of material by chemical reactions during manufacturing. The removal of material is either from the silicon substrate itself or from any film or layer of material on the wafer.

Generally, etching can be divided into two types, i.e. dry etching and wet etching. Figure 1 shows comparison of pattern transfer by wet etching and dry etching. The resist pattern is made by a lithographic process to serve as a mask, which defines the etching positions on Si surface. Wet etching is normally isotropic, which means its horizontal etching rate is the same as its vertical rate. Hence, when wet chemical etching is used, the isotropic nature of etching can cause unwanted undercutting of the oxide beneath the protective photoresist mask. The undercutting beneath the mask usually occurs in a shape as seen in Figure 1(a). As a result,

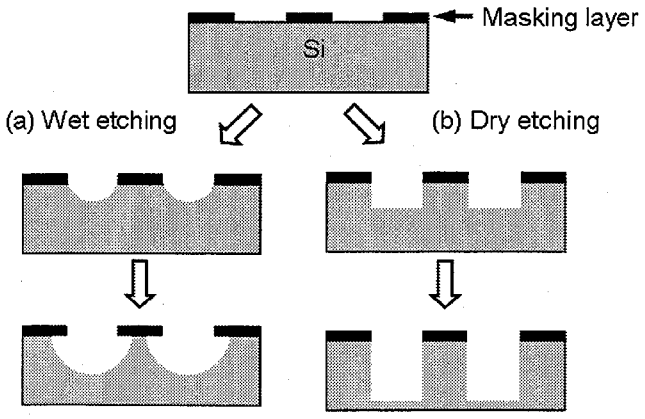


Figure 1. Comparison of (a) wet etching and (b) dry etching for pattern transfer.

the pattern transfer by wet etching cannot form a pore with high aspect ratio.

On the other hand, an etching process that proceeds in only one direction (e.g., vertical only) is said to be completely anisotropic. Unlike many of the wet chemical etchants used in wet etching, anisotropic etching of silicon is possibly performed by most of the dry etching processes. Since dry etching only etches away materials that are not covered by a patterned mask, the surfaces covered by the mask are almost intact without any etching as shown in Figure 1(b). By using dry etching, therefore, needed pores or trenches with various geometry or high aspect ratio can be formed in silicon according to the shape of the mask and etching time. Although dry etching is a common method for fabricating high-aspect-ratio pores, the dry process is complex and the facility cost is very expensive. In the following sections, the two etching processes are explained in more detail emphasizing especially wet etching which is used in the whole thesis.

### 1.1.1 Dry etching

Dry etching technology is a standard method used in fabricating integrated circuits and patterning Si wafers. It allows a reproducible, uniform etching of all materials used in silicon and III-V-semiconductor technology. The method refers to the removal of material, typically a masked pattern of semiconductor material, by exposing the material to a bombardment of reactive ions. A mask on top of the substrate is used to protect certain areas from etching, exposing only the uncovered areas to be etched. Dry etching is synonymous with plasma-assisted etching, which denotes several techniques that use plasma in the form of low-pressure discharges. Typically, dry etching includes sputter etching, plasma etching and reactive ion etching (RIE).

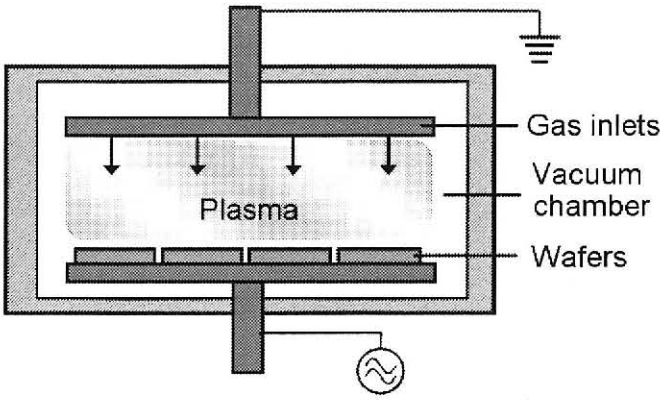


Figure 2. Schematic diagram of a typical reactor used for reactive ion etching.

Figure 2 shows a schematic diagram of reactive ion etching (RIE). The etching process is carried out in a reactor with plasma containing reactive ions. Plasma is a fully or partially ionized gas composed of equal numbers of positive and negative charges and a different number of unionized molecules. Plasma is generated under low pressure (vacuum) when an electric field is applied to a gas, resulting in the ionization of the gas molecules. Then, high-energy reactive ions diffuse to the Si surface and react with Si atoms. As shown in Figure 2, the gas is pumped into the vacuum chamber through small inlets. Sulfur hexafluoride ($SF_6$) is common gas used for etching Si substrates.

Figure 3 illustrates six primary steps of the plasma etching process. The first step is the generation of the etchant species in the gas phase. The reactive species are then transported by diffusion to the surface where they become adsorbed and react with the surface. Finally, the volatile byproducts are desorbed from the surface and diffused into the bulk gas. Because dry etching results in a faithful copy of the mask pattern, it is widely used in fabricating microstructures with high aspect ratio features, smooth morphology, and vertical profiles.

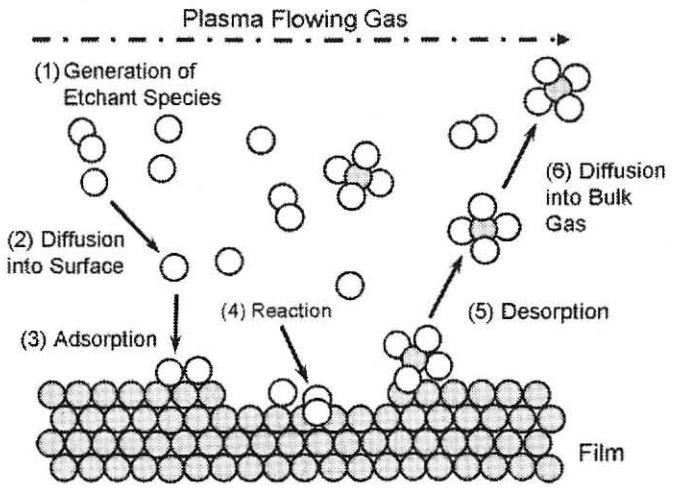


Figure 3. Basic steps in a dry etching processing.

### 1.1.2 Wet etching

Wet etching is an etching method extensively used in semiconductor processing. Normally, it is done by immersing silicon wafers in a liquid bath containing chemical etchants. Wet chemical etching of silicon is nearly related to the electrochemical behavior of Si electrodes. It is a process for removal of materials or silicon dioxide films from silicon wafers through dissolution in solutions. Compared to dry etching, wet etching is good in that it is fairly cheap and capable of processing many wafers quickly. The disadvantage is that wet etching does not produce micrometer-size critical geometries that are needed for MEMS.

In general, a wet etching process involves one or more chemical reactions that consume the original reactants and produce new species. By exposing silicon surface in an etching solution, reduction-oxidation (redox) reactions commonly take place at the silicon/electrolyte interface. During wet etching, silicon is oxidized, forming silicon oxide layers on the surface. Then, the silicon oxide layers are dissolved by a chemical reaction in the etching solution.

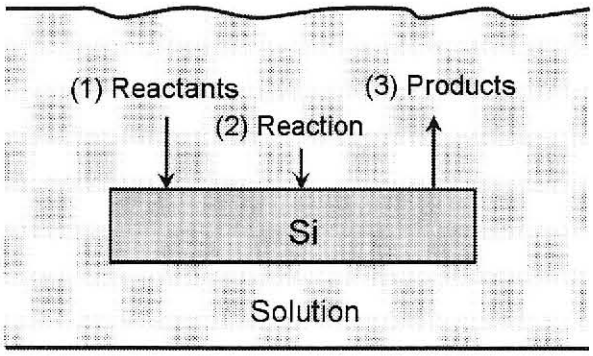


Figure 4. Basic mechanisms in wet etching.

The mechanisms of wet etching can be broken down into three essential steps, as illustrated in Figure 4. First, the reactants diffuse to the silicon surface. Chemical reactions occur at the surface, and the products from the surface are removed by diffusion. The etching rate is influenced by many factors, such as pH, concentration and temperature of the etching solution.

The two main etching solution systems for silicon are HF solutions and alkaline solutions. This is because silicon is inactive in any kind of aqueous solutions due to the formation of an insoluble surface oxide except for alkaline solutions or HF solutions in which the oxide can be dissolved. However, dependence of crystalline orientations on etching rate is a principal difference between the two systems, as shown in Figure 5. When silicon is etched in HF solutions, the etching rate is similar regardless of the crystalline orientation, i.e. isotropic etching. On the other hand, the etching rate strongly depends on the crystalline orientation in alkaline solutions, i.e. anisotropic etching. Currently, the combination of photolithographic patterning and anisotropic as well as isotropic etching of silicon have led to a multitude of applications in the fabrication of MEMS.

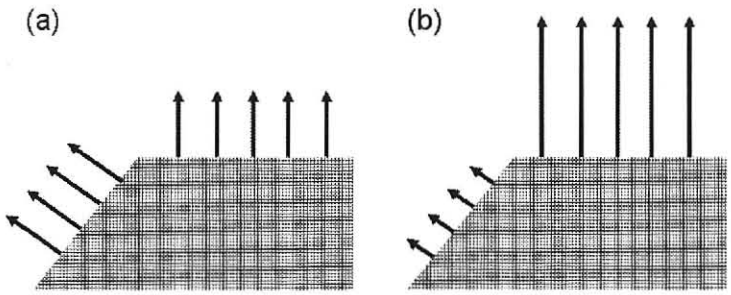


Figure 5. Schematic diagrams of (a) isotropic and (b) anisotropic etching.

*Wet etching in alkaline solutions: Anisotropic etching*

Wet chemical anisotropic etching, mostly performed using alkaline solutions, is mainly used to dissolve silicon in an anisotropic manner for micromachining of silicon. Because of anisotropic etching, the dissolution rate of both (100) and (110) is much larger than that of (111) [12-13]. The etch rate ratio between other planes, such as (100) and (110), depends on etchant concentration and etching temperature, but is usually within a factor of two [14].

All alkaline solutions show the sensitivity of etch rate to crystal orientation, which is the basis for anisotropic etching. Among the all alkaline solutions, potassium hydroxide (KOH) is most commonly used because its high (100)/(111) etch rate ratio and nontoxic nature. Anisotropic etching using a KOH solution has long been utilized for fabricating very complex microstructures, which include Si nano-beams and cantilevers on a silicon substrate [15,16]. Other solutions are also used, such as concentrated ammonia solutions ($NH_4OH$) and tetramethyl ammonium hydroxide (TMAH). Addition of oxidizing agents reduces the anisotropy.

The etching of silicon in alkaline solutions accompanies hydrogen evolution. In the dissolution process using alkaline solutions, $OH^-$ and $H_2O$ are the active species for silicon dissolution while the cations play a minor role [17]. The mechanism of anisotropic etching of silicon can be represented in a model proposed by Lehmann, as shown in Figure 6. Silicon

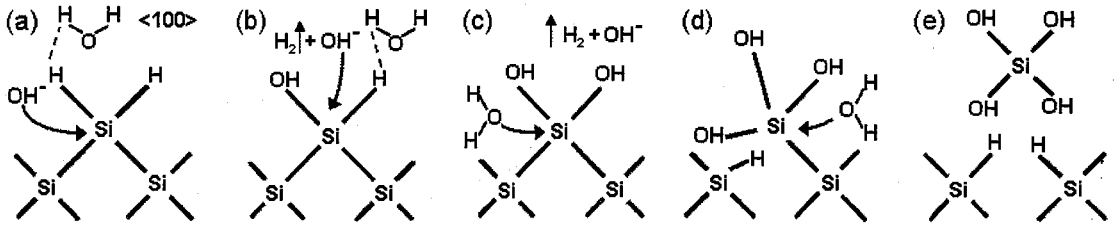


Figure 6. Scheme of reaction for the chemical dissolution of Si(100) in alkaline solutions proposed by Lehmann. The figure is from Ref. 17.

(100) with hydrogen terminated surface is assumed in this model. As shown in step (a), $OH^-$ is responsible for initiating the attack by replacing the surface hydrogen atoms. An Si-OH bond is generated under evolution of hydrogen with a ratio of one $H_2$ molecule to one OH group introduced. In step (b), the second Si-H on the Si surface is replaced by Si-OH under formation of another $H_2$. The attraction of electrons by OH group weakens the silicon back-bonds, making them susceptible to be attacked by $H_2O$ as shown in steps (c) and (d). The silicon surface atom is dissolved in a form of $Si(OH)_4$ and the surface remains covered with Si-H bonds.

On the other hand, the low dissolution rate of Si(111) surfaces can be explained by the scheme of Figure 7. Because only one OH group can be introduced, polarization of three silicon back-bonds is insufficient to break the Si-Si bond. As a result, the three Si back-bonds are difficult to be attacked by $OH^-$.

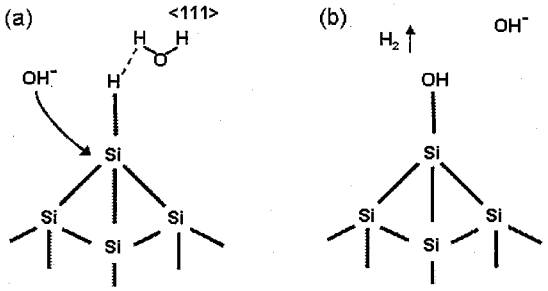


Figure 7. The chemical dissolution rate of Si (111) surface in alkaline solutions. The figure is from Ref. 17.

Wet chemical etching using alkaline solutions provides a superior method for the micromachining of silicon. Nowadays, it is an indispensable step in the processing of varied complicated microstructures for application to MEMS. Using a $SiO_2$ or $Si_3N_4$ layer patterned by photolithography, a variety of geometric microstructures can be fabricated, such as pyramids and grooves formed on Si wafers. [18-20]. In the field of solar cells, anisotropic wet etching is used for fabrication of pyramidal structures on single crystalline silicon solar cells [21-23]. The textured structures are effective to lower surface reflection and to increase the amount of light absorbed into devices.

*Wet etching of Si in solutions containing HF: Isotropic etching*

Wet chemical isotropic etching of silicon is a common method used in fabrication of porous silicon (PS) on silicon wafers. It is conventionally performed in aqueous solutions containing hydrofluoric acid (HF). In isotropic etching, HF plays a very important role, which is used to dissolve silicon oxide layers formed on Si surface. In general, a silicon wafer immersed in HF-based solutions is predominantly terminated by hydrogen, forming a hydrophobic surface. There may also be a small amount of Si atoms terminated by oxygen and/or fluorine atoms depending on the solution composition.

The wet etching of silicon involves two essential steps, i.e. oxidation and dissolution. To increase the etch rate of silicon, therefore, both rates of oxidation and dissolution must be increased. Oxidation of silicon can be significantly enhanced by addition of effective oxidizing agents into the HF solution or by anodic polarization of silicon which increases the surface concentration of positive holes (or holes).

In electrochemical etching, anodic polarization of silicon is achieved by changing the electrode potential of silicon using an electrochemical instrument. There are two modes of the

electrochemical instrument, i.e., those providing constant potential (potentiostat) and constant current (galvanostat). During anodic etching, the valence electrons of silicon are removed via the external circuit of an electrochemical cell. Anodic reaction of silicon typically involves positive holes which are the majority carriers in p-type silicon but are the minority carriers in n-type silicon. Therefore, extra generation of positive holes is needed for electrochemical etching of n-type silicon. They are produced either by very strong field strength or by illumination.

Figure 8 shows an electrochemical system with its complete electrical connections for anodic etching of n-type silicon [24]. In the electrochemical system, three electrodes are conventionally used, i.e., working electrode, counter electrode and reference electrode. The counter electrode is commonly made of a platinum mesh or sheet. The most common reference electrode is the saturated Ag/AgCl electrode with a potential versus SHE. Normally, the reference electrode is placed close to the silicon surface in a HF solution. A silicon sample is mounted in the electrochemical cell and connected to an electrochemical instrument. An ohmic contact is made by rubbing Ga-In eutectic at the interface between silicon and the instrument. The silicon sample is illuminated from its front side or back side. By using the

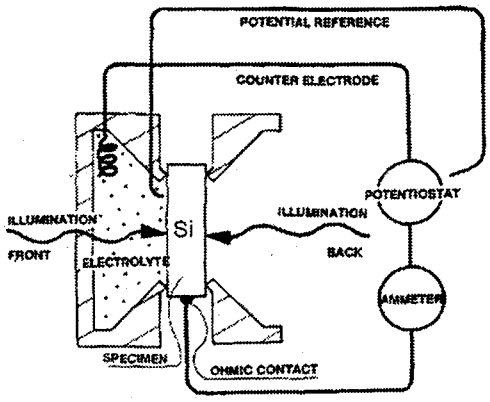


Figure 8. An electrochemical cell for electrochemical etching of n-type silicon under illumination. The figure is from Ref. 24.

potentiostat, the potential of the sample to the reference electrode can be adjusted before anodic etching. As the sample is polarized anodically, current flowing between the sample and the counter electrode can be obtained. The anodic behavior of silicon can be easily characterized by current-potential curves using an electrochemical instrument. The same electrochemical cell can be used for anodic etching of p-type silicon samples. In this case, however, illumination is unnecessary.

*Wet etching of Si in solutions containing HF: Etching with oxidants*

Addition of effective oxidants to the HF solution is another useful way to oxidize silicon without anodic polarization and illumination [26-30]. Valence electrons can be removed by an oxidant in solution, i.e. positive holes are injected into the valence band, resulting in high etch rate of silicon. The injected positive holes are consumed in the dissolution reaction of silicon. The oxidant is simultaneously reduced by accepting electrons from silicon. The rate of oxidation of silicon (holes consumption) is equal to the rate of reduction of the oxidants (holes injection). The etching of silicon in HF solutions containing oxidants is actually a localized electrochemical process, that is, there are anodic and cathodic sites on silicon surface with local cell currents flowing between them.

Nahidi and Kolasinski constructed an energy level diagram which shows the redox potentials of oxidants, p- and n-type Si, as shown in Figure 9 [25]. The redox potential interprets the tendency of the species to accept or give up electrons. Therefore, if an energy level of an oxidant is lower than the valence band maximum of silicon, the oxidant spontaneously accepts electrons from silicon, resulting in the oxidation of silicon. From the energy level diagram, an oxidant with an energy level higher than $Fe^{3+}$ is unlikely to be an effective holes injector for the oxidation of silicon.

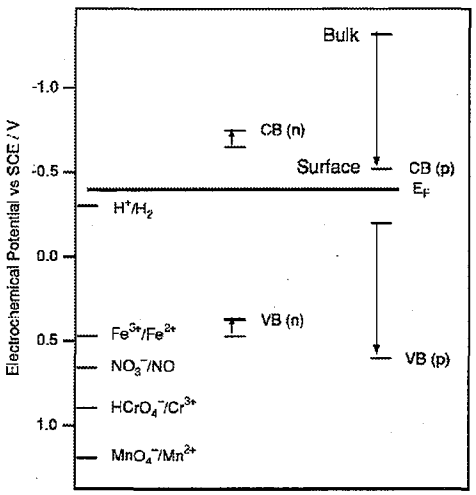


Figure 9. An energy-level diagram for conduction band minimum (CB) and valence band maximum (VB) of n- and p-type Si, and oxidants in HF solution. The figure is from Ref. 25.

*Wet etching of Si in solutions containing HF: Metal-assisted etching*

In recent years, a new wet etching technique using the catalytic effects of noble metal particles or thin films has been widely investigated for fabricating pores and other Si microstructures [31-42]. It is believed that the charge transfer from Si surface to the oxidants is easier through the Si/metal interfaces than through the bare wafer. The characteristic of the metal-assisted etching is that the pores or pits are formed at the places where metals exist when Si is oxidized by the oxidants and the oxide layer is removed by HF simultaneously.

Morinaga *et al.* reported that Cu ions deposited on the Si surface in the form of metallic particles [31]. The Cu deposition on Si surface in HF solutions resulted in the formation of pits on the surface. They also proposed the mechanism of Cu deposition on Si surfaces in HF solutions, as shown in Figure 10. Because the $Cu^{2+}$ ion has a much higher redox potential than Si, the $Cu^{2+}$ ions near the Si surface can be spontaneously reduced in a form of a metallic

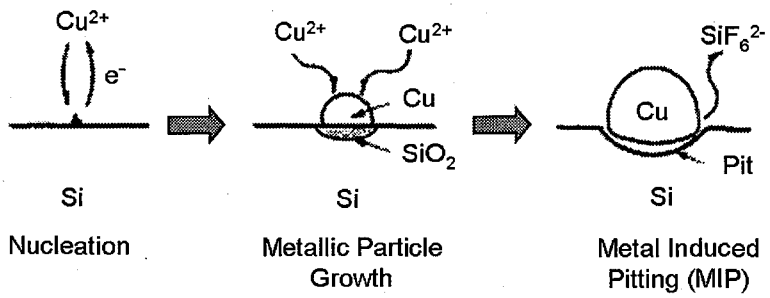


Figure 10. Mechanism of Cu deposition on Si surface in HF solutions. The figure is from Ref. 31.

particle by receiving electrons from Si. The redox potentials of the $Cu^{2+}$ ion and Si are around +0.34 and -0.84 (V vs. SHE), respectively.

The Cu nucleus forms on the surface can accept electrons from Si. Hence, other $Cu^{2+}$ ions close to the Si surface receive electrons via the Cu nucleus and deposit on it, resulting in the growth of the Cu particle. Silicon oxide is simultaneously formed beneath the Cu particle, as shown in Figure 10. The silicon oxide is sequentially dissolved by HF in a form of $SiF_6^{2-}$, resulting in the formation of a pit on Si surface.

Matsumura and his co-workers found that pores with diameters of 50 nm to a few micrometers were formed in Si using fine metal particles such as Ag and Au as catalysts in a solution containing HF and $H_2O_2$ [39-41]. The pores were almost perpendicular to a (100) surface. It was also possible to make helical pores using Pt particles [42]. These straight and helical pores were formed as the metal particles dropped into the Si bulk due to the oxidative dissolution of Si. They also used the etching method for making a porous silicon layer as an anti-reflective coating on the top of crystalline silicon solar cells [43, 44]. They reported that the low reflection surfaces were obtained by the simple and mild wet process.

The fabrication of photoluminescent porous silicon using the metal-assisted etching has been developed further by Bohn and his co-workers [45-47]. In their works, thin Pt films were

deposited on a Si patterned substrate by spin-casting of Pt complex [45] or sputtering [46, 47]. Before Pt deposition, the Si substrate was patterned by using resist template or a mask. By patterning the substrate, photoluminescent porous silicon can be selectively fabricated on the substrate. After deposition of Pt on the substrate, metal-assisted etching was carried out in a solution containing HF, $H_2O_2$ and methanol (or ethanol). After etching, a porous silicon layer was fabricated on the surface, and upon irradiation with ultraviolet light, the light-emitting of porous silicon was in a visible spectral range. Depending on the etching time and Si doping type, porous silicon films with different morphologies and photoluminescent properties were produced.

### 1.2 Through-wafer interconnects and Cu filling

In recent years, smaller, lighter portable devices (cellular phones, digital cameras and MP3 players) with higher performance and more features are demanded by consumers. The urgent demand to reduce size, weight and cost, while increasing the functionality of portable products, has led to innovative three-dimensional (3D) packaging concepts. The 3D packaging using stacked chips for high density has received a considerable attention over the last few years [48-50]. Among all kinds of 3D packaging techniques, 3D integration using through-wafer interconnects (TWIs) is currently considered to be one of the most advanced technologies in the semiconductor industry [51-56].

TWIs have many superior advantages over wire-bonding [57, 58] and other technologies for MEMs packaging. 3D stacking with TWIs electrodes can overcome the limitation of traditional 3D packaging methods. Additional miniaturization, increased interconnect density, and high performance are possible by stacking silicon dies with TWIs. Figure 11 represents a

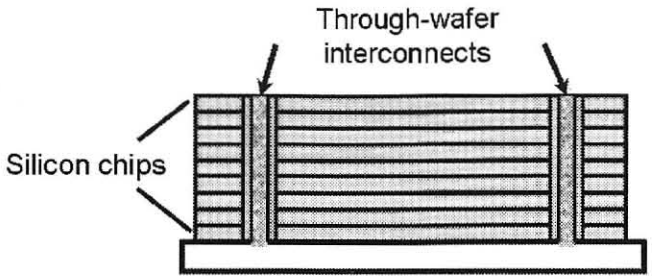


Figure 11. Scheme of through-wafer interconnects structure.

scheme of TWIs structure. As shown in Figure 11, TWIs are electrical pathways formed vertically through the wafers, enabling to decrease the complexity of interconnect pathways. It can provide vertical connections with the shortest distance. Conventionally, these vertical pores through the whole thickness of a silicon wafer are fabricated by deep reactive ion etching (DRIE) [59, 60].

Deposition of a metal within the vertical pores to make interconnects is also one of the key technologies for 3D chip stacking. The most common material for interconnect filling is copper, due to its high electrical conductivity and good compatibility [61]. Deposition of metals into such pores with high aspect ratio is a challenge. The common shortcoming of most methods is that for deep pores the so-called bottleneck effect occurs during the Cu filling process, as shown in Figure 12.

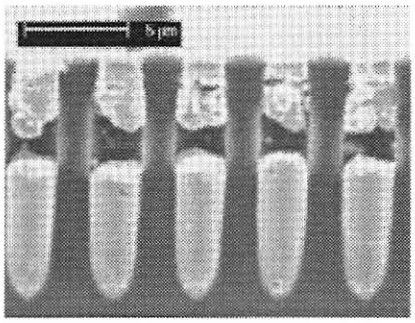

Figure 12. A cross-sectional SEM image of bottleneck formation in macropores formed in silicon. The image is from Ref. 74.

Copper can be deposited into deep pores using either dry or wet methods. Chemical vapor deposition (CVD) and physical vapor deposition (PVD) are the representative dry methods for pore filling with Cu [62-65]. However, the cost of these methods is very high and fabrication process for Cu filling is complicated.

On the other hand, wet methods such as electrodeposition and electroless deposition have superior advantages due to their simplicity and higher cost performance than dry methods. As a result, Cu filling into pores in silicon by electrodeposition has been studied by many researchers [66-70]. Ogata and his co-workers investigated Cu filling into ordered macropores prepared in p-type silicon by electrodeposition [71-73]. They also studied electrodeposition of noble metals into ordered macropores. Metal microrods were obtained by dissolution of silicon after the complete filling by electrodeposition [72, 73]. Fang *et al.* reported that macropores as deep as 150 μm with a diameter of 2 μm formed in n-type silicon could be filled with Cu by electrodeposition [74].

### 1.3 Slicing methods for wafers fabrication

A Silicon wafer is a thin slice of semiconductor material, widely used in the fabrication of integrated circuits (IC), solar cells and other electronic devices. After production of a Si ingot by a crystal growth technique, the substrate wafers are fabricated from the Si ingot through a series of processes, such as slicing, flattening, etching and polishing. The crystal growth technique generally used is the Czochralski method. The process for manufacturing silicon wafers from the ingot stage is shown in Figure 13. After the growth of crystalline materials in the form of ingots, slicing of the ingots into wafers is the first step for manufacturing electronic devices.

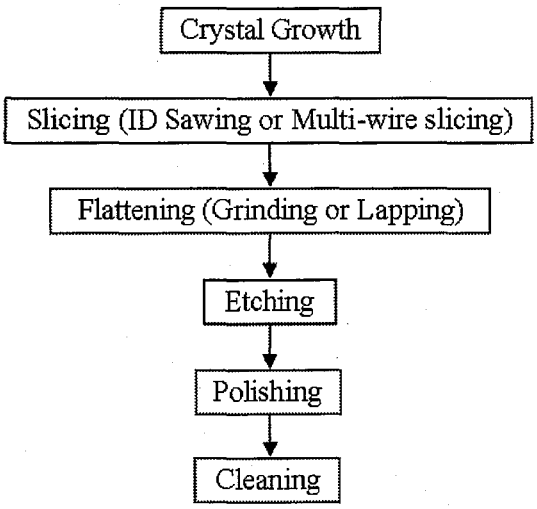


Figure 13. A flow chart of wafer fabrication from the ingot stage to the wafer stage.

Today more than 80% of solar cell production needs the wafer slicing. Currently, wafer slicing is carried out by either inner diameter (ID) sawing or multi-wire slicing. The two well-known methods utilize mechanical forces to slice a Si ingot. In recent years, to replace these methods, non-mechanical methods such as wire electrical discharge machining (WEDM) are being investigated.

### 1.3.1 Inner diameter sawing

Slicing technology is essential to silicon industries for manufacturing semiconductor and photovoltaic devices. Inner diameter (ID) sawing is a commonly used technique for slicing hard and brittle materials, such as glasses, ceramics and silicon. To manufacture Si wafers, the technique has been used for slicing Si ingots for the past three decades [75, 76].

The ID sawing method uses a rotating thin stainless-steel blade with a circular hole at the center, as shown in Figure 14. The blade is the heart of an ID sawing machine. The inner edge of the blade is coated with an abrasive layer, normally nickel-bonded diamonds [75]. The

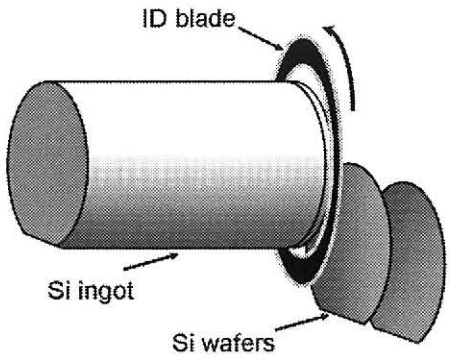

Figure 14. Illustration of ID sawing for fabricating Si wafers from a Si ingot.

metallic bonded diamonds act as a sawing tool. A Si ingot to be sliced is fed into the center hole of the blade. During the slicing process, the stainless steel blade rotates under high tension and traverses through the Si ingot. After the whole ingot is cut through by the blade, slices of wafer are produced. The blade should be as thin as possible to reduce the kerf width but thick enough to maintain stability and hardness during the operation. The kerf means material loss due to the width of sawing during machining. Typically, the kerf loss of ID sawing is over 250 μm per wafer and requires etching of a 100-μm-thick surface layer to remove the damages [77]. Concerning the damage, since the slicing is performed by mechanical forces, it causes damage to the Si crystal on Si surface to the depth of about 100 μm from the surface [77]. After the slicing process, Si wafers are lapped or ground in order to obtain the correct thickness and flatness [78-83]. From the view of saving materials, the kerf loss of the slicing process and the damage have to be largely decreased.

### 1.3.2 Multi-wire slicing

As introduced above, ID sawing is a mature technique for wafer slicing. However, it takes time and only cuts one slice at a time with large kerf loss. Besides, it is difficult to apply ID sawing to slicing Si ingots with a diameter of 12 inches or 16 inches.

Multi-wire slicing is another slicing method [84, 85]. To avoid large kerf loss and to increase the slicing efficiency, multi-wire slicing has been developed and widely used for wafer slicing [86-91], especially for large-size Si ingots. Basic mechanisms of multi-wire slicing were reviewed by Möller [90]. Since multi-wire slicing is able to slice an ingot into hundreds of wafers at the same time, this slicing technique is now replacing ID sawing especially for slicing ingots with a diameter over 30 cm.

The multi-wire slicing is a slicing technology which uses tensioned stainless steel wires and working fluid containing abrasive particles. Diamonds and silicon carbide (SiC) are the most commonly used abrasives, which are very expensive and account for 25-35% of the total slicing cost [86]. The recycle of expensive abrasives from wasted slurry was studied by Nishijima *et al* [92].

The principle of the multi-wire slicing is depicted in Figure 15. The diameter of wires is typically around 175 μm and stretched with high tension of 20-35 N [89]. The slicing wires are wound on wire-guides carefully grooved with a constant pitch, forming a horizontal web of 500-700 parallel wires [90]. The wire-guides are rotated to move the entire wire-web at a high speed of 5-20 m/s [90]. During slicing, the kerf loss and damages on crystal are unavoidably produced as are produced by ID sawing. At present, the kerf loss resulted from multi-wire slicing is typically 200-250 μm [91].

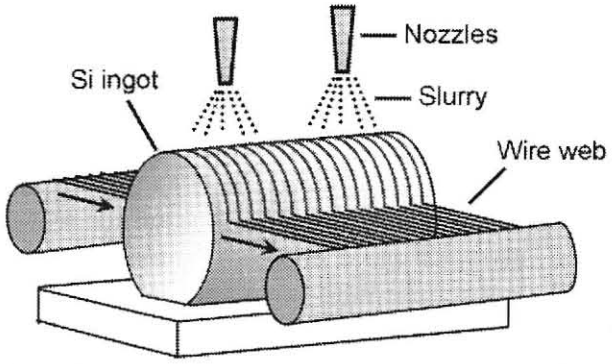


Figure 15. Scheme depicting the principle of the multi-wire slicing technique.

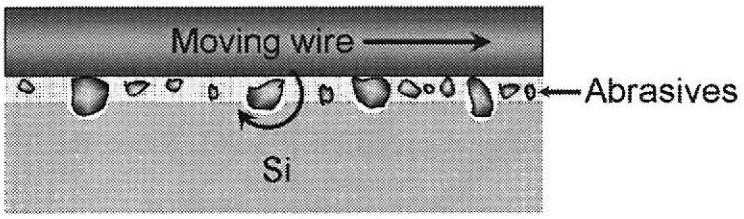


Figure 16. Scheme of wire and slurry with abrasives in the cutting zone during slicing.

Multi-wire slicing is achieved by the abrasive slurry which is continuously supplied through high flow-rate nozzles over the whole wires. The wires, acting as a slurry carrier, bring the abrasive slurry into the sawing interface between wires and crystal surface. By the parallel shear motion of these two bodies, rolling abrasive particles are squeezed and forced to rotate at the interface, as shown in Figure 16. Since abrasive particles are facetted and contain sharp edges and tips, they can exert very high local pressures on the Si surface. The action of the abrasive particles depends on several factors such as wire speed, force between wire and crystal, viscosity of the slurry and so on. During the rotation, the abrasive particles transmit part of the applied compressive forces from the tensioned wires to crystal. The rotation of the abrasive particles makes themselves indent, penetrate and scratch Si crystal to generate cracks until thin Si pieces are chipped away.

### 1.3.3 Wire electro-discharge machining (WEDM)

During the last decade, the semiconductor and photovoltaic (PV) industry based on silicon has tremendously grown, resulting in the shortage of silicon supply. As described in former sections, ID sawing and multi-wire slicing are typical mechanical methods for wafer manufacturing. However these methods cause mechanical damages on Si surface and large kerf loss during slicing. The kerf loss causes the waste of material and high production cost.

Therefore, in the recent years, a demand for reducing the kerf loss is increasing.

Electrical discharge machining (EDM) is an indispensable machining method in the mold industry due to its good dimensional precision [93-96]. Since the 1980s, EDM has been utilized as a method for machining hard and brittle non-metallic materials. It is primarily used for hard metals or those that would be very difficult to machine with traditional techniques. The use and application of EDM within the past decade was reviewed by Ho and Newman [97]. Recently, Kumar *et al.* [98] presented a review about surface modification by EDM and future trends of its application.

Wire electrical discharge machining (WEDM) is one kind of EDM process. It uses a single metal wire as the electrode for machining various conductive materials such as metals, ceramics and metal matrix composites [99-102]. Since a numerically controlled, modified technique, WEDM provides an effective method for machining intricate and complex shapes in conductive materials. In recent years, WEDM has been improved significantly to meet the requirements in various machining fields. WEDM is a thermo-electrical process without contact forces to a workpiece, resulting in many advantages over conventional slicing methods. Recently, WEDM has been introduced to wafer manufacturing to reduce the kerf loss [103-106]. Since WEDM is a non-mechanical technique, the diameter of wire is possible to be decreased, resulting in reduction of kerf loss. Moreover, slurry with expensive abrasives is not necessary. Consequently, WEDM is expected as a promising candidate of wafer slicing. Luo *et al.* [103] used WEDM to slice n-type single-crystalline Si ingots. Peng and Liao [104] studied the machining rate and surface roughness of Si wafers produced by the WEDM process. Ho *et al.* [107] reviewed the vast array of academic research and suggested the future WEDM research direction.

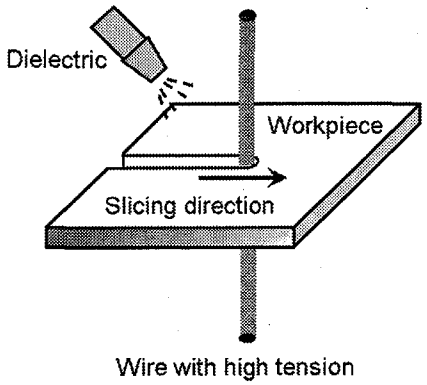


Figure 17. Scheme of WEDM technique.

The scheme of WEDM is shown in Figure 17. This method is performed in a tank of dielectric fluid, typically in a bath of deionized water or oil. The metal wire is usually made of brass with a diameter of 0.05 mm to 0.3 mm [103].

In WEDM, there is no mechanical contact between the electrode and workpiece, resulting in no residual stresses left on the workpiece. The metal wire with high tension is slowly fed through the workpiece. As the wire is extremely close to the workpiece, a rapid series of repetitive electrical discharges, *i.e.* visible electrical sparks, occur between the wire and the workpiece. The spark generates intense pressure and heat, resulting in material erosion at the localized point. The small amount of eroded material particles that is removed from the workpiece is flushed away by the flowing dielectric fluid. The repetitive discharges create a set of successively deeper craters in the workpiece until the final shape is produced. Up to now, however, WEDM, is not used in wafer slicing industry due to low throughput.

## 1.4 Scope and outline of the thesis

This thesis deals with a chemical method for making pores in Si and an electrochemical method for grooving Si. In both processes, silicon is oxidatively etched in HF solution using metallic catalysts. The pores formed in Si are used to make interconnects in Si by filling the pores using the metal particles, which are used as catalysts for pore formation, as seeds for electrodeposition of Cu. The groove formation process is applied to making Si wafers by slicing Si blocks using Pt wires as the catalytic electrodes.

The background, results, and conclusions of the study are described in 6 chapters; the outlines of the chapters are as follows:

### Chapter 1

A general introduction concerning pore formation in Si, etching methods and some of important machining processes and related academic research are reviewed, which form the background of this thesis. Problems in the silicon technologies, such as through-wafer interconnects and wafer fabrication by slicing, are pointed out as well. The following chapters are devoted to new chemical and electrochemical methods for solving these problems.

### Chapter 2

In order to apply pores formed in Si to through-wafer interconnects, the research in this chapter focuses on the fabrication of pores with diameters larger than 1 μm by applying the metal-assisted etching technique. The wet process for pore formation is carried out in HF solutions containing $H_2O_2$ as an oxidant. Two types of spherical Au particles with sizes of ca. 1 μm and 40 μm are used as catalysts for the fabrication of pores in Si(100) wafers by wet etching. The pore formation process is studied by observing the morphologies of the pores

formed in Si after the wet process. In addition, the effect of HF and $H_2O_2$ concentrations on pore formation in Si is discussed.

**Chapter 3**

We report the filling of micropores formed in Si with Cu to make interconnects in Si wafers. Pores are formed on the basis of the wet etching process as described in Chapter 2 using aggregated Au particles. The use of the aggregated Au particles enables the fabrication of large pores with a diameter of about 5 μm. At the bottom of each pore, the Au aggregates remain, which are used as seeds for Cu filling. The Cu filling is conducted in a solution containing 0.1 M $CuSO_4$ and 1.8 M $H_2SO_4$. The filling of the pores with Cu is demonstrated by SEM image of the cross section of the samples.

**Chapter 4**

In the chapter, an entirely new slicing method for processing Si by means of catalytic reactions is proposed. The mechanism for pore formation described in Chapter 2 is applied to grooving silicon by using catalytic wire electrodes, with anodic potentials being applied to the catalytic wire electrodes instead of using chemical oxidants such as $H_2O_2$. We used different kinds of catalytic wires with a diameter of 50 μm, such as Ag, Au and Pt. In the groove formation process, metal wires work as catalysts and induce hole injection into Si through the Si/metal interface. To investigate the effect of diameters of Pt wires, we used Pt wires with different diameters. In addition, we studied the groove formation in Si by using 50-μm-thick Pt plates as catalysts.

**Chapter 5**

In this chapter, we study some experimental conditions, such as anodic potentials applied to the Pt wires, temperature of HF solution, and HF concentration, on the grooving rate of silicon. Because the anodic dissolution of Si occurs at the Si/Pt interface, the effect of pressure applied to the Si/Pt interface is investigated as well.

**Chapter 6**

Based on the results described in chapter 4 and chapter 5, we try to slice Si blocks with a size of $1 \times 1 \times 2$ $cm^3$ (W × H × L) by the electrochemical method. Besides a free-falling system for grooving Si used in Chapter 4 and 5, an instrument with a function of vertical motion of Pt wires is utilized for grooving Si blocks. Production of Si wafers by the electrochemical process, which is completely different from the conventional mechanical process, is reported.

**Chapter 7**

General conclusions of this thesis are given in the last chapter.

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# *CHAPTER 2*

*Wet Etching for Vertical Micropores Formation in Si Wafers*

*Using Au Particles as Catalysts*

# Chapter 2

# Wet etching for vertical micropores formation in Si wafers using Au particles as catalysts

## 2.1 Introduction

Deep straight pores formed in silicon (Si) have attracted attention for their applications in many fields such as membranes [1, 2], trench capacitors [3], and through-wafer interconnects [4-6]. Dry etching combined with photolithography has been commonly used for the fabrication of deep pores or trenches in Si [7, 8]. However, a major problem of this method is that it involves complicated processes for forming deep pores in Si, especially for making pores as deep as several tens of micrometers. Fabrication of pores in Si by this method is therefore costly, and the method is limited to small-scale production. Wet anisotropic etching in alkaline solution is another approach for making pores in Si. Although this method is attractive owing to its simplicity compared to dry etching, the realizable structures for desired applications are limited. Anodic etching, a process by which Si wafers are electrochemically anodized in solutions containing hydrofluoric acid (HF), is another attractive method because it enables the formation of deep pores [9, 10]. However, the complexity of pretreatment that is required for making the patterned structure impedes the application of this method to mass production.

Metal-assisted etching has been studied as a novel method for production of a porous structure in Si. In this method, thin metal films or particles loaded on Si wafers are used as catalysts for etching of Si in aqueous solutions containing HF and oxidants such as $H_2O_2$ [2,

11-16], $Fe(NO_3)_3$ [17], $K_2Cr_2O_7$ [18] and $O_2$ [19] without the need for external electrical power. Because of the simplicity of this method compared to the common techniques described above, the method is promising for application to mass production if efficient control of the geometrical structure is achieved.

Tsujino and Matsumura found that cylindrical pores of several tens of nanometers in diameters were formed in Si preferentially in the <100> direction by wet etching using Ag particles as catalysts [14]. This process was carried out in aqueous solutions containing HF and $H_2O_2$. The Ag particles were loaded on the Si surface before the etching [14, 16]. During the process, the Ag particles gradually sank into the bulk of Si and formed pores. When Pt particles with granular surfaces were used instead of Ag particles, helical pores were formed [15]. In this process, it is thought that Si is oxidized selectively at the Si/catalyst interface and then the oxidized Si dissolves in the solution containing HF.

In order to apply the pores to through-wafer interconnects, the pore diameter should be larger than 1 μm [4-6]. Hence, the research in this chapter focuses on the fabrication of pores with diameters larger than 1 μm by applying the metal-assisted etching technique. We also investigate the effect of HF and $H_2O_2$ concentrations on pore formation in Si.

## 2.2 Experimental

Silicon wafers used in this study were p-type Si(100) (boron-doped, 7−13 Ωcm), which were obtained from Shin-Etsu Handoutai Co. The wafer was 625 μm in thickness, and one of the faces was mirror-polished. The wafer was cut into $20 \times 20$ $mm^2$ pieces and used as test samples. Two types of Au particles were used as catalysts for pore formation in Si. Spherical

Au particles with a size of ca. 1 μm and 40 μm were used purchased from Tokuriki Chemical Research and Tanaka Kikinzoku Group, respectively. Laboratory-grade ultra-pure water (UPW) with a resistivity of 18.2 MΩcm was prepared using a Milli-Q pure water system (YAMATO-Millipore). Other chemicals were used as received.

Before the pore formation, the silicon sample was cleaned by immersing it in a sulfuric acid-hydrogen peroxide mixture (97% $H_2SO_4$ : 30% $H_2O_2$ = 4:1, v/v) for 10 min, in 1% HF for 1 min, and in UPW for 10 min for rinsing. Then it was again immersed in a sulfuric acid-hydrogen peroxide mixture for 10 min, rinsed with UPW for 10 min, and dried by air blowing. The surface of the sample was hydrophilic. On the mirror-polished face of the sample, the dispersion of metal particles suspended in water or isopropyl alcohol was placed dropwise and spin-cast with a Mikasa 1H-D7 spincoater at a speed of 3000 rpm. Then the silicon sample loaded with the metal particles was immersed in an aqueous solution containing HF and $H_2O_2$ for etching for certain periods. After the etching treatment, the silicon sample was rinsed successively with UPW for 10 sec, ethanol for 3 min, and pentane for 3 min, and dried in air. Morphologies of the metal particles and pores formed in silicon samples were observed using a Hitachi S-5000 scanning electron microscope (SEM). Cross-sectional views of samples were obtained for the surfaces exposed by mechanically cleaving the sample. Pores were preferentially formed in the <100> direction [14], especially when spherical particles were used as the catalysts. When a sample with pores that developed in the <100> direction at a high density was cleaved mechanically, the sample tended to be cleaved along the pores. As a result, the cleaved pores were easily observed on the surface of such samples. However, the observation of cleaved pores was rather difficult when the density of the pores was low or the pores were crooked. In such samples, cross sections of the

pores could be observed on the cleaved surfaces. Energy dispersive X-ray spectroscopy (EDX) was used for the elemental analysis or chemical characterization of a sample.

## 2.3 Results and Discussion

*Pore formation using spherical Au particles as catalysts*

Figure 2(a) shows a typical SEM image of spherical Au particles loaded on a Si(100) surface by the spin-coating method. The Au particles had diameters of about 0.5-1.5 μm. They were randomly distributed: there were isolated particles and aggregated particles. Figure 2(b) represents a cross-sectional SEM image after immersion in an aqueous solution containing 2.6 M HF and 8.1 M $H_2O_2$ for 1 min. About half of Au particles sank into Si at the initial stage of 1 min etching, resulting in the formation of pores in a hemispherical shape. It demonstrates that the oxidative dissolution of Si occurred at the Si/Au interface. When the Si sample loaded with spherical Au particles was processed for 1 h, Au particles sank into the bulk of Si completely, and micrometer-sized pores were generated, as shown in Figure 2(c). The density of pores formed was almost equivalent to that of Au particles loaded, while the sizes of these pores were larger than that of Au particles. Corresponding cross-sectional SEM images revealed the presence of the Au particles at the bottoms of pores shown in Figure 3. Hence, like the formation of nanometer-sized pores with Ag nanoparticles [14, 16], micrometer-sized pores were found to be formed with Au particles, which sank into the bulk of Si as the pores were formed. This result is also in agreement with the pores formed by using Ag nanoparticles as catalysts [14, 16].

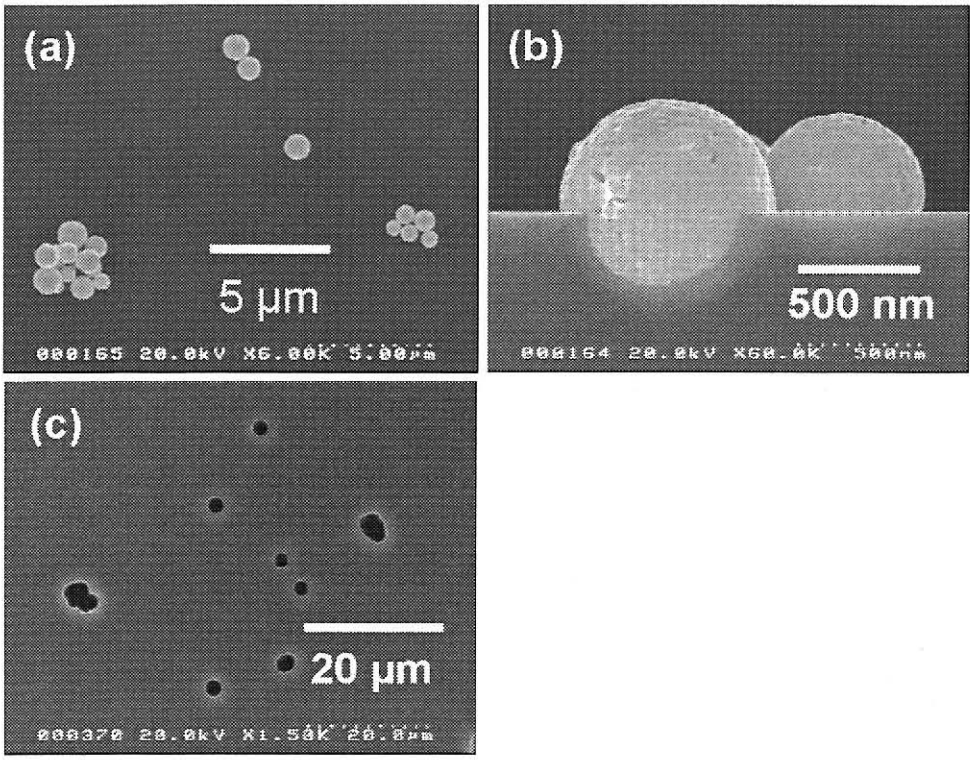


Figure 2. (a) SEM image of a Si(100) surface loaded with spherical Au particles before etching. (b) Cross-sectional SEM image after 1 min treatment and (c) a plan-view SEM image after 1-h treatment in an aqueous solution containing 2.6 M HF and 8.1 M $H_2O_2$.

The pore formation in Si is initiated by the reduction of $H_2O_2$, as represented by equation (1) [14, 16].

$$H_2O_2 + 2H^+ = 2H_2O + 2h^+ \quad (1)$$

Owing to low catalytic ability of the Si surface for the reaction, the etching of Si is slow in a HF-$H_2O_2$ solution. However, the reaction is catalyzed by metal particles. Since these metal particles donate electrons to $H_2O_2$ and accept electrons from Si, positive holes are generated in Si. The positive holes injected into Si induce oxidative dissolution of Si in the form of $SiF_6^{2-}$ in a solution containing HF, which is represented by equation (2).

$$Si + 4h^{+} + 6HF = SiF_6^{2-} + 6H^{+} \quad (2)$$

Since the oxidative dissolution occurs preferentially near the Si/metal interface, micrometer-sized pores are formed. As typically shown in Figure 3(a), the pores formed with the isolated Au particles were mostly linear and oriented in the <100> direction.

The preferential boring in the <100> direction is attributed to the chemical instability of the (100) face. It has been reported in literature that the oxidative dissolution of Si in HF solution, either caused by chemical oxidation or electrochemical oxidation, is accompanied by the

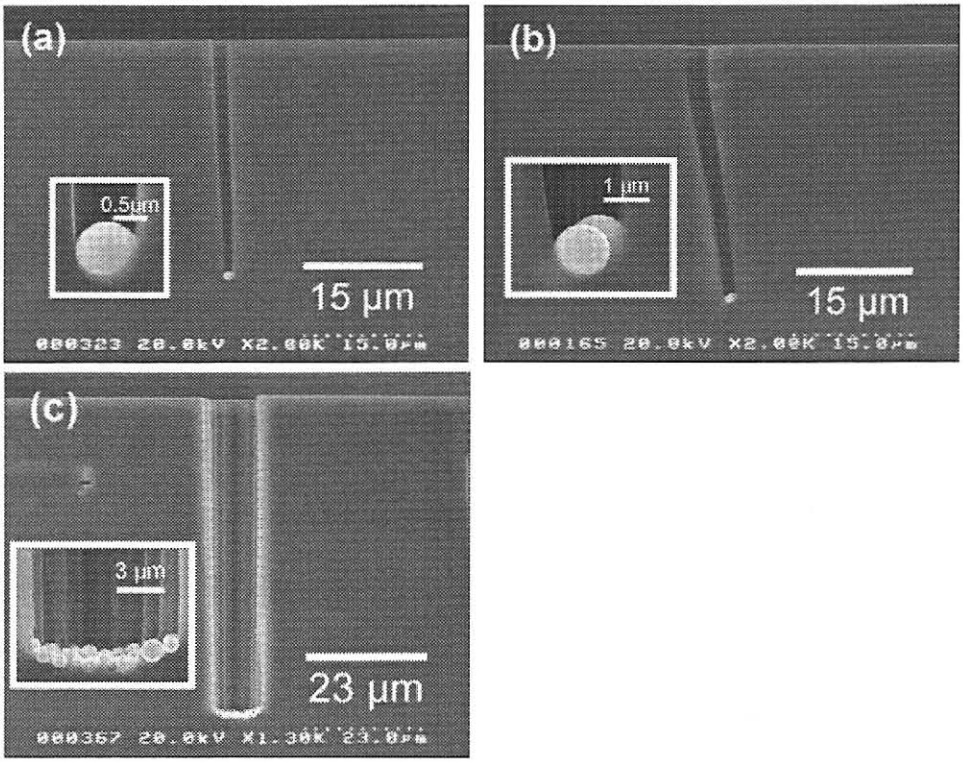


Figure 3. Cross-sectional SEM images of the pores bored in a Si(100) sample with (a) a single spherical Au particle, (b) an aggregate composed of two Au particles, and (c) an aggregate composed of a large number of Au particles after etching in an aqueous solution containing 2.6 M HF and 8.1M $H_2O_2$ for 1 h. Insets show their corresponding enlarged images of the bottom parts of pores.

formation of a nanoporous Si layer on the surface [11]. The formation of the nanoporous Si layer is enhanced under the conditions in which a large number of positive holes are injected into Si. Such nanoporous Si layers were observed in our samples in the magnified SEM images of pore sidewalls and top surfaces of samples after the treatment. The thickness was about 100 nm.

In contrast to the pores formed with isolated Au particles, those formed with Au deposits consisting of a few Au particles were often crooked, as seen in Figure 3(b). A probable explanation for the results is that the irregular geometry of the Si/Au interface on the deposit induced different local etching rates on the deposit, resulting in the deviation of the pore growth direction from the <100> direction. However, when the deposit consisted of a larger number of Au particles, especially more than 10 particles, the pores again grew in the <100> direction, as shown in Figure 3(c). In this case, the local difference in the etching rate at the Si/Au interface was probably averaged and, as a result, straight pores were formed. This result is similar to the growth of Si nanowires using densely deposited nanometer-sized Ag particles [13, 17]. Our finding indicates that such an averaging effect occurs even with deposits consisting of only 10 or more particles.

As seen in Figures 3(a) and 3(c), the straight pore formed with aggregated Au particles is almost twice as deep as that formed with an isolated Au particle, both being formed by a 1 h treatment. Figure 4 shows the depths of pores generated with isolated Au particles and Au aggregates consisting of more than 10 particles as a function of the treatment time. The faster boring speed for the aggregated Au particles is attributable to the larger surface area of the 3-dimensionally aggregated structure of the Au particles. This structure allows the reduction of $H_2O_2$ in a larger amount per unit area of the cross section of the pore and an increase in the number of positive holes injected into Si. The efficient diffusion of HF, $H_2O_2$ and $SiF_6^{2-}$ in the

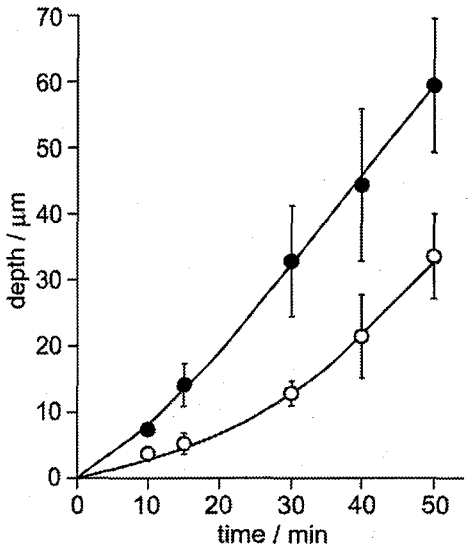


Figure 4. Depth of pores formed with isolated Au particles (○) and Au aggregates consisting of more than 10 particles (●) *vs.* etching time. Each point shows the average for about 10 pores and the bar represents the standard deviation.

large pores bored by them may also contribute to the rapid growth of pores. The relatively slow boring speed in the initial period, as seen in Figure 4, suggests that the Au particles deposited on the Si surface by spin-casting do not make good physical contact with Si. In addition, when the particles are deposited on Si with a flat surface, the contact area must be small. However, after the particles start sinking into Si, the contact area between Au and Si increases, leading to the increased boring speed.

To bore larger pores on Si surface, spherical large Au particles with a diameter of 40 μm were used as catalysts. Figure 5(a) shows the SEM images of Au particles loaded on a Si(100) surface by the spin-coating method as described in the experimental section. It is observed that all of Au particles were isolated particles. After immersing the Si sample loaded with large Au particles in a solution containing 2.6 M HF and 8.1 M $H_2O_2$ for 12 h, the Au particles did not sink into the bulk of Si. As shown in Figure 5(b), the Au particle remained on the Si

surface and shallow pores in a bowl shape formed under the Au particles. The bowl-shape pores had a diameter of about 40 μm, which was nearly the same as the diameter of large Au particles.

Numerous nanometer-sized pores generated on the Si surface and the surface of bowl-shape pores. Additionally, it was observed that small particles with a size of less 1 μm were found on the Si surface, as shown in Figure 5(d). The small particles confirmed by EDX analysis were Au. We speculate that large size of the Au particles made it difficult to diffuse HF solution into the Si/Au interface beneath large Au particles. Instead of oxidative dissolution of Si, 40-μm-sized Au particles were dissolved into Au ions in the HF solution containing $H_2O_2$.

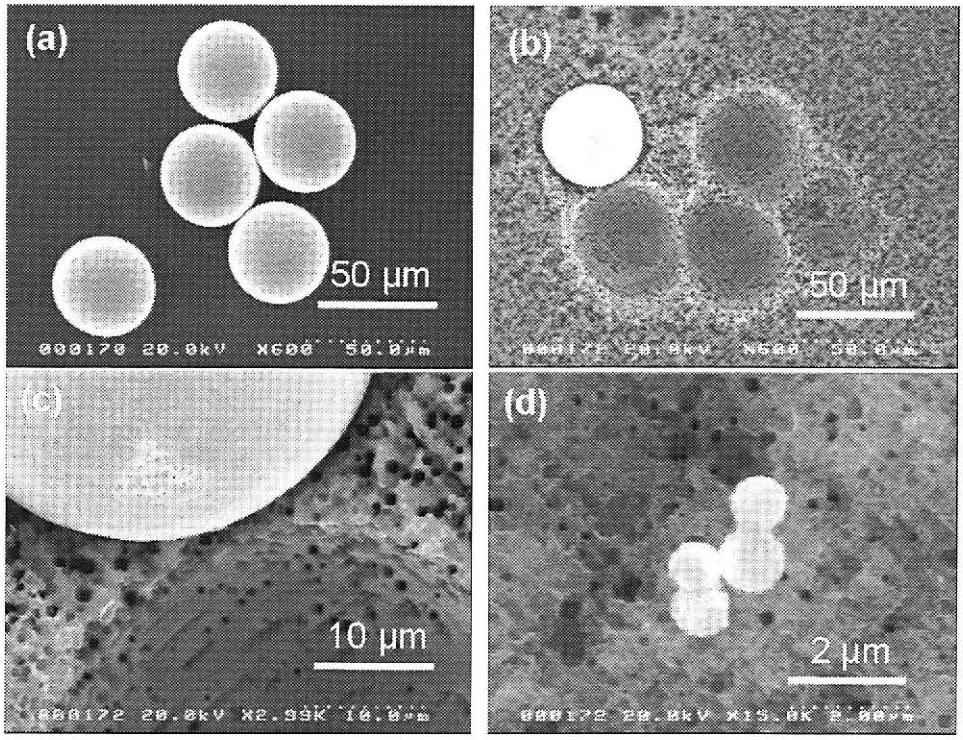


Figure 5. SEM images of (a) a Si(100) surface loaded with spherical 40-μm-sized Au particles and (b) the surface after 12-h treatment in an aqueous solution containing 2.6 M HF and 8.1 M $H_2O_2$. (c) An enlarged Si surface image of (b) near the Si/Au boundary. (d) An enlarged image of small particles forming on the Si surface.

Then the Au ions precipitated on the surface of silicon to form small particles. We consider that the small Au particles sank into silicon due to the redox reaction and then nanometer-sized pores were formed densely on the silicon surface. The result demonstrates that using aggregated Au particles was better than 40-μm-sized Au particles for making vertical micropores in Si.

*Effect of HF and $H_2O_2$ concentration*

Because the pore formation in Si is due to the oxidative dissolution of Si, the concentrations of HF and $H_2O_2$ are the important parameters. In this section, the effect of HF and $H_2O_2$ concentrations for the process was investigated. First, the effect of different HF concentrations for pore formation was studied by keeping the $H_2O_2$ concentration at 8.1 M. The HF concentrations used were 0.26 M, 1.3 M, and 2.6 M. Figure 6(a) and (c) show the plan-view images of pore formation on Si after 1-h processing in a solution containing 8.1 M $H_2O_2$ and HF at concentrations of 0.26 M and 1.3 M. Figure 6(b) and (d) show cross-sectional SEM images of Figure 6(a) and (c), respectively. These pores were shallower than the pores formed in the solution containing 2.6 M HF, which were shown in Figure 3(a). This is attributed to slow dissolution of oxidized Si layers, which are formed at the Si/Au interface, in HF solutions with low concentration. This suggests that HF plays a very important role in controlling the rate of pore formation in Si.

Another feature of the pores is that the widths were larger at the upper part of the pores when HF concentration is lowered, as shown in Figure 6(b) and (d). This phenomenon suggests that part of the positive holes diffused from the bottom of the pores, where Au particles existed, to the sidewalls of the Si sample and formed nanoporous Si layers. Since the nanoporous Si gradually dissolves into the HF solution [20-22], Si is etched more at places

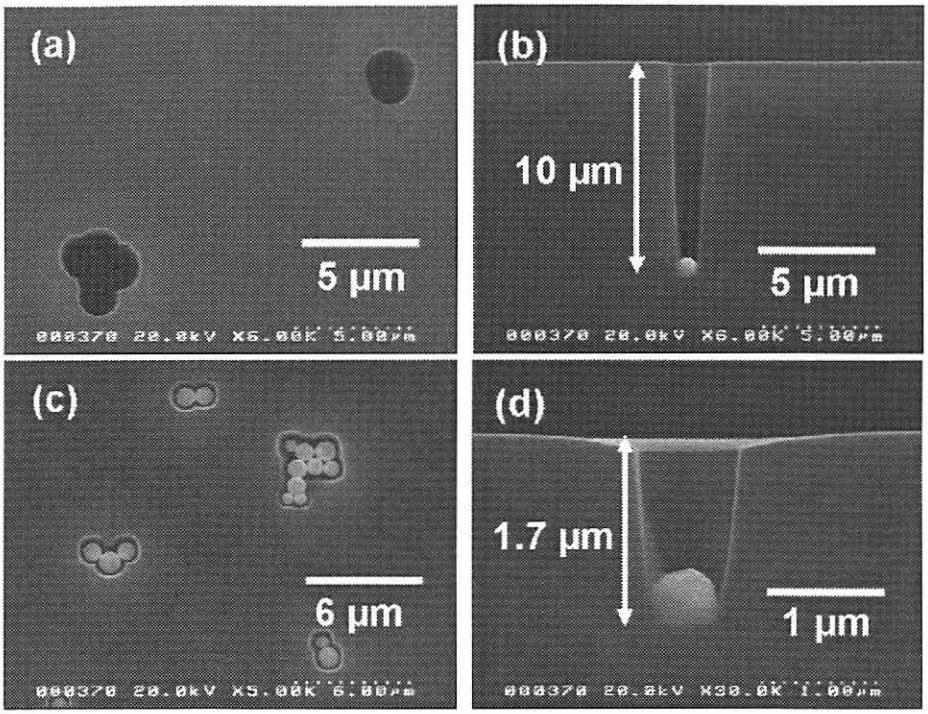


Figure 6. (a) Surface and (b) cross-sectional SEM images of a Si(100) sample loaded with Au particles after 1-h processing in an aqueous solution containing 8.1 M $H_2O_2$ and 1.3 M HF. (c) Surface and (d) cross-sectional SEM images of a Si(100) sample loaded with Au particles after 1-h processing in an aqueous solution containing 8.1 M $H_2O_2$ and 0.26 M HF.

where the surface is in contact with the HF solution for a longer time.

The pore formation in an aqueous solution containing 2.6 M HF and diluted $H_2O_2$ was investigated as well. The concentration of $H_2O_2$ was diluted to 4 M and 0.81 M. Figure 7(a) and (c) shows plan-view images after 1-h processing in the solution containing 2.6 M HF and diluted $H_2O_2$. When the concentration of $H_2O_2$ was 4 M, a few crooked pores were observed on the Si surface after 1-h processing, as shown in Figure 7(a). The majority of the pores were preferentially formed in the <100> direction (Figure 7(b)). When the concentration of $H_2O_2$ was further reduced to 0.81 M, the ratio of crooked pores to whole pores significantly

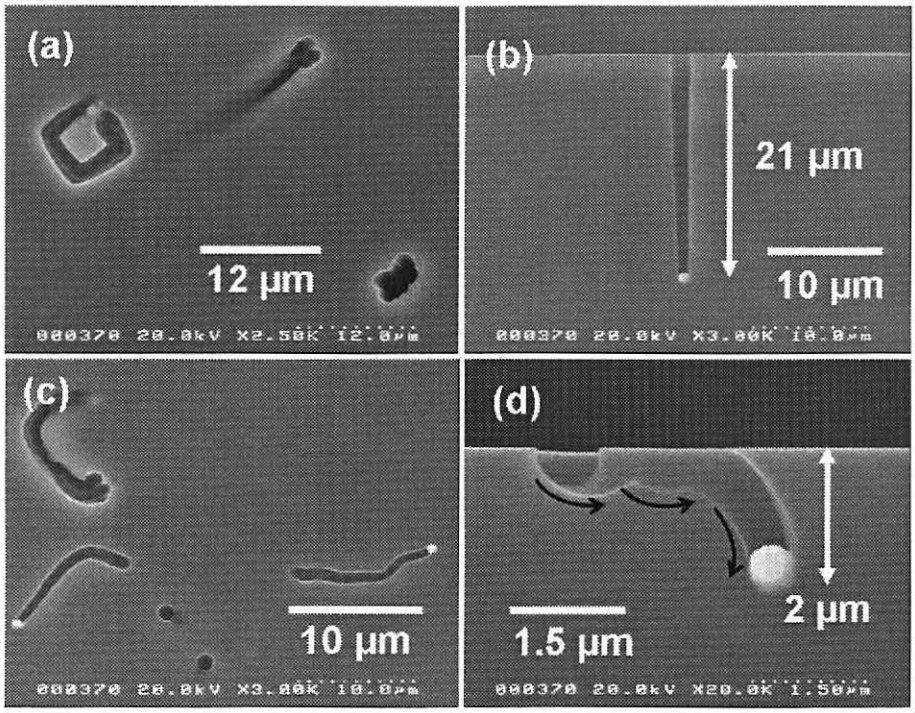


Figure 7. (a) Surface and (b) cross-sectional SEM images of a Si(100) sample loaded with Au particles after 1-h processing in an aqueous solution containing 4 M $H_2O_2$ and 2.6 M HF. (c) Surface and (d) cross-sectional SEM images of a Si(100) sample loaded with Au particles after 1-h processing in an aqueous solution containing 0.81 M $H_2O_2$ and 2.6 M HF.

increased. As shown in Figure 7(c), the growing direction of pores was very random. The crooked pores were formed not only horizontally on the surface but also in the bulk of Si in an irregular way, as typically seen in Figure 7(d). These pores were observed only in a very shallow zone from the Si surface. Similar phenomena were observed in pores formed using Ag nanoparticles in HF solutions containing $H_2O_2$ at low concentrations [16]. The reason for the generation of the crooked pores in HF solutions containing $H_2O_2$ at low concentrations is not fully understood. One possible explanation is that the uneven distribution of $H_2O_2$ near the Si/Au interface may cause the irregular dissolution of Si.

## 2.4 Conclusions

In this chapter, we have studied the usefulness of micrometer-sized metal particles as catalysts for the fabrication of micrometer-sized pores in Si(100) wafers by wet etching. The formation of pores includes various elementary steps, *e.g.*, reduction of $H_2O_2$ on metal catalysts, injection of electrons from Si to metal catalysts, and oxidative dissolution of Si with positive holes and HF. The pore formation and the morphologies of the pores are affected not only by the size and numbers of the particles but also by the concentration of etching solutions. We found that spherical Au microspheres are promising candidates for making straight pores with micrometer-sized diameters. They can be used as isolated particles or in the state of relatively large aggregates (>10 particles).

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# *CHAPTER 3*

*Cu Electrodeposition in Micropores Formed in Si Wafers*

# Chapter 3

# Cu electrodeposition in micropores formed in Si wafers

## 3.1 Introduction

Due to the increasing demand for smaller and lighter electronic devices, there is a urgent need for reduction in the size of electronic chips. Innovative chip packaging technologies with through-wafer interconnects, which are advantageous to increasing the density due to the 3D stacking, have been developed.

Micromachining of silicon is important in fabrication of semiconductor devices and micro electro-mechanical systems (MEMSs) [1-3]. The most fundamental processes for these purposes are etching and deposition. A variety of methods has been reported for these processes, such as reactive ion etching and metallorganic chemical vapor deposition. Etching methods for micromachining are classified into dry and wet processes. In both processes, resist masks are used to define the places where etching proceeds.

The electrodeposition of a metal in pores and grooves of silicon is also an important process in the semiconductor industry. For example, through-wafer interconnects formed by filling pores with Cu is used in advanced packaging of large-scale integrations [4-7]. In addition, various types of MEMSs and 3D integrated circuits have been proposed using through-wafer interconnects [8-10]. The formation of interconnects by filling through-wafer pores with Cu was proposed by Paraszczak et al. [11] and has been studied by many researchers [12-16]. Recently, Yae *et al.* [17] reported the formation of Co-Ni nanorods in the pores of silicon by electroless plating using metal particles that were used for the formation of

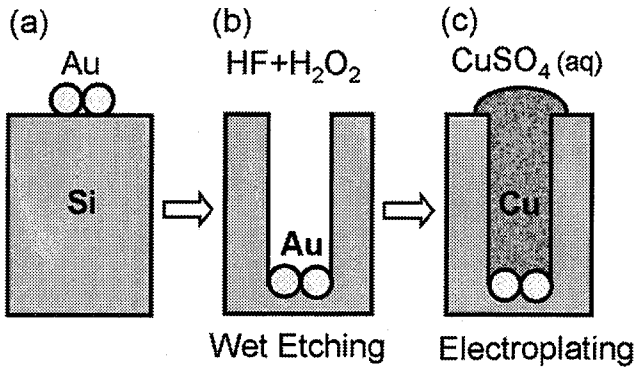


Figure 1. The process of Cu electrodeposition inside Si Wafers by filling pores formed in Si using Au particles as catalysts.

nanopores in silicon. However, the formation of long Cu wires with a diameter of 5 μm in Si would be more meaningful for applications in semiconductor devices. Filling of pores with metals has also been used for manufacturing of printed circuit boards [18].

In Chapter 2, the formation of vertical micrometer-sized pores in Si wafers by wet etching using Au particles as catalysts was described. The pores are preferentially formed in the <100> direction in an aqueous solution of HF and $H_2O_2$ without using resist masks. The pore formation using metal particles is based on the catalytic activity of the metal particles for electron transfer from Si to $H_2O_2$. Because the pores are formed as a result of oxidative dissolution of Si at the interface between Si and metal particles, metal particles remain at the bottom of each pore formed in silicon.

In order to apply the pores to through-wafer interconnects, the pore diameter should be larger than 1 μm [19-21]. In this chapter, as shown in Figure 1, we report the usefulness of micrometer-sized Au particles as catalysts for the fabrication of such large pores by applying the metal-assisted etching technique. We also report the filling of the micropores with Cu by electroplating using Au aggregates. Aggregated Au particles existing at the ends of the pores are utilized as seeds for Cu deposition.

### 3.2 Experimental

n-Type Si(100) wafers with a resistivity of 8-12 Ω cm, which were obtained from Shin-Etsu Handoutai Co., were used as test samples in this study. The wafers were 625 μm thick, and one of the faces was mirror-polished. The wafers were cut into pieces of 30×30 mm. Spherical Au particles of about 1 μm (TAU-100) were purchased from Tokuriki Chemical Research and used as catalysts. Laboratory-grade ultrapure water (UPW) with a resistivity of 18.2 M Ω cm was prepared using a Milli-Q pure water system (Yamato Millipore) and used in the experiments.

Before pore formation, the Si sample was sequentially cleaned by immersion in a sulfuric acid–hydrogen peroxide mixture (97% $H_2SO_4$ : 30% $H_2O_2$ = 4:1, v/v) for 10 min, in UPW for 10 min, in 1% HF for 1 min, in UPW for 10 min, in a sulfuric acid–hydrogen peroxide mixture for 10 min, and in UPW for 10 min for rinsing, and then dried by air blowing. The surface of the sample after the cleaning was hydrophilic. On the mirror-polished surface of the sample, droplets of a suspension of Au particles were deposited, and liquid was spin-cast at a speed of 1500 rpm for 30 s. For the deposition of Au particles on the Si surface, a suspension containing 1 wt % of Au particles, which had been dispersed and suspended in water by sonication for 5 min, was used immediately after preparation. After the deposition of the Au particles, the Si sample was immersed in a mixed solution containing 2.6 M HF and 8.1 M $H_2O_2$, which was prepared by mixing 50 wt % HF, 30 wt % $H_2O_2$, and $H_2O$ at a volume ratio of 1:9:1, to make pores [22]. Then, the sample was successively rinsed with UPW, ethanol, and pentane, each for 3 min, and dried in air.

Figure 2 shows the experimental setup for electrodeposition of Cu in pores formed in Si. For the electrodeposition of Cu in the pores of Si, the Si sample was connected to a wire on

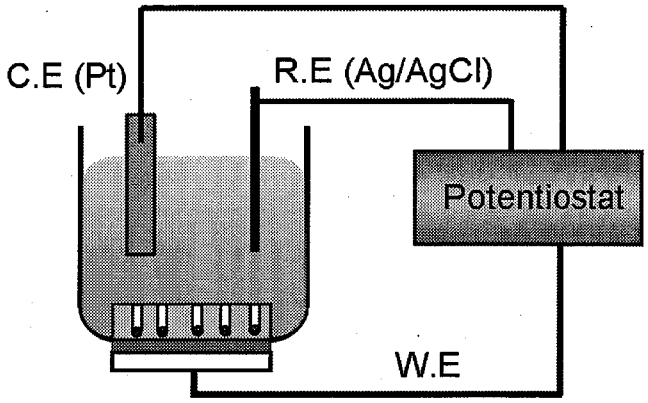


Figure 2. Experimental setup for the electrodeposition of Cu in the pores of Si in a solution containing 0.1 M $CuSO_4$ and 1.8 M $H_2SO_4$ using a potentiostat.

the back side of the sample, at which ohmic contact was made using a Ga–In eutectic. The wire and the back side were sealed using a glass tube and an epoxy resin. Cu was deposited on Si by applying a cathodic potential to a Si sample in a solution containing 0.1 M $CuSO_4$ and 1.8 M $H_2SO_4$ using a potentiostat (Hokuto Denko, HSV-100). An Ag/AgCl electrode and a Pt plate were used as a reference electrode and a counter electrode, respectively, and the solution was unstirred during Cu electrodeposition.

The morphologies of the pores before and after the deposition of Cu were observed with a Hitachi S-5000 scanning electron microscope (SEM). Cross-sectional views of the pores were obtained for surfaces exposed by mechanically cleaving the samples. Energy dispersive X-ray spectroscopy (EDX) was used for the elemental analysis.

### 3.3 Results and Discussion

*Formation of pores with a diameter of about 5 μm*

The Au particles deposited on the Si(100) surface by the method described in the experimental section were aggregated. Each aggregate consisted of about 7 to 15 Au particles and was about 3 to 6 μm. The average number of constituent particles was about 10 and the average size of the aggregates was about 5 μm. Figure 3(a) shows a typical structure of an aggregate, which consists of seven Au particles.

Pores were formed in Si by immersing the sample loaded with Au particles in a mixed solution of HF, $H_2O_2$, and $H_2O$. Figure 3(b) shows the plan view of the Si wafer, in which

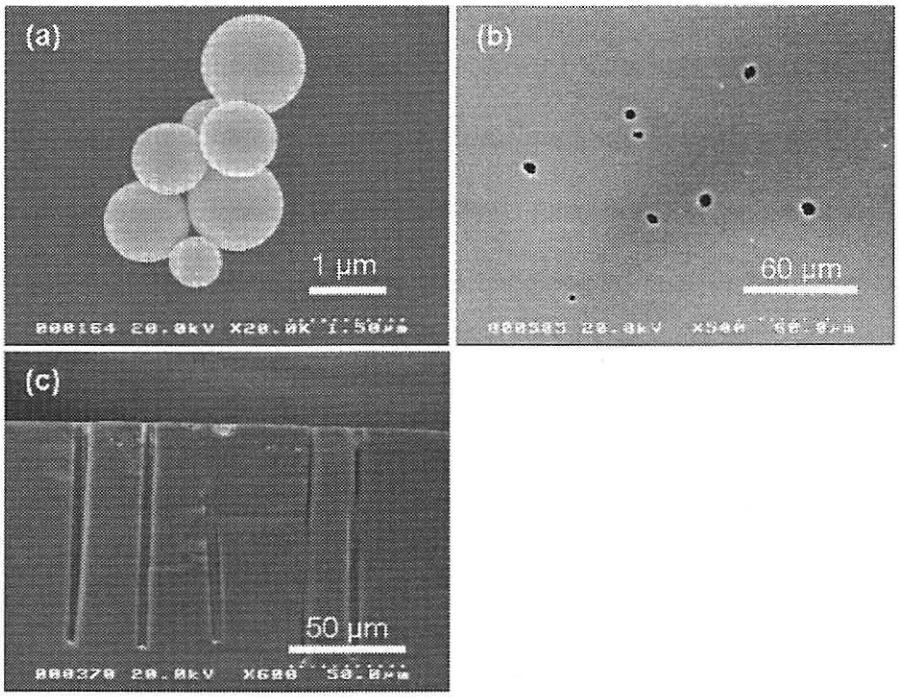


Figure 3. SEM images of (a) Au particles deposited on a Si surface by spin-casting, (b) pores formed on Si, and (c) a cross-section of pores formed in Si. The pores were formed by immersing the Si sample in a solution containing 2.6 M HF and 8.1 M $H_2O_2$ for 5 h using the Au particles as catalysts.

pores were formed by etching in the solution for 5 h. The pores seen on the surface have a diameter of about 5 μm, and their shapes reflect the morphology of the Au aggregates loaded on the surface. When this sample was mechanically cleaved, the cross sections of pores were exposed on the cleaved plane, as shown in Figure 3(c). The depths of the pores were about 100 μm. By observing cross sections of many pores, we found that depths of most of the pores ranged from 90 to 110 μm, except for some very shallow pores. These shallow pores may be formed by Au aggregates which had inadequate contacts with Si. Another feature of the pores is that they were formed in the direction perpendicular to the surface, i.e., in the <100> direction. This result was the same as the pores formed using nanometer-sized Ag particles [23, 24]. However, the pore seen in the middle of Figure 3(c) is slightly tilted, perhaps owing to uneven distribution of Au particles in the aggregate. Such a tendency for tilting was more obvious for aggregates consisting of a few particles [22].

For aggregates consisting of a larger number of particles, as used in this experiment, there was much less tilting, probably because the morphological unevenness of the aggregates was moderated by a larger number of particles. Most of these pores grew perpendicular to the surface, when the aggregates consisted of 10 or more particles.

It was possible to make pores with a diameter of about 3 μm using an Au particle as large as 3 μm as a catalyst. However, the speed of pore formation was very slow, probably because the mass transfer of the etching solution to the Si/Au interface existing under large Au particles is difficult [22]. Pores were not formed in Si using 40-μm Au particles, as described in Chapter 2. In contrast, when aggregates made of 1-μm-sized Au particles were used, the pores were formed at a much higher speed, because the etching solution could penetrate to the Si/Au interface through the gaps of Au particles.

A probable mechanism of the pore formation is that the oxidative dissolution of Si preferentially occurs at the Si/Au interface, resulting in the dropping of aggregated Au particles into Si below the original Si surface as it is gradually etched [22]. Pore formation is initiated by the reduction of $H_2O_2$ on Au particles

$$H_2O_2 + 2\,H^+ + 2\,e^- \rightarrow 2H_2O \qquad E^0 = 1.763\ \text{V (vs. SHE)} \qquad [1]$$

where SHE is standard hydrogen electrode. Because the Au particles donate electrons to $H_2O_2$ and accept electrons from Si, positive holes are generated in Si near the Au particles. The positive holes induce oxidative dissolution of Si and produce $SiF_6^{2-}$ in a solution containing HF. This reaction is written as

$$Si + 6F^- + 4\,h^+ \rightarrow SiF_6^{2-} \qquad E^0 = -1.370\ \text{V (vs SHE)} \qquad [2]$$

*Deposition of Cu on Si wafers with and without pores*

We tried to deposit Cu electrochemically on Si wafers with 70 μm deep pores. The current-potential characteristics of Si samples with and without the pores were measured in an aqueous solution containing 0.1 M $CuSO_4$ and 1.8 M $H_2SO_4$. The samples with and without the pores showed onsets of cathodic current due to deposition of Cu at about -0.25 V and -0.30 V vs Ag/AgCl, respectively, as shown in Figure 4. The appearance of the onset at more anodic potential for the Si sample with pores is attributed to lower over potential for the deposition of Cu on Au (or Cu) than on bare Si. Although the difference in the onset potential between the samples with and without pores is not large, the result suggests that Cu can be

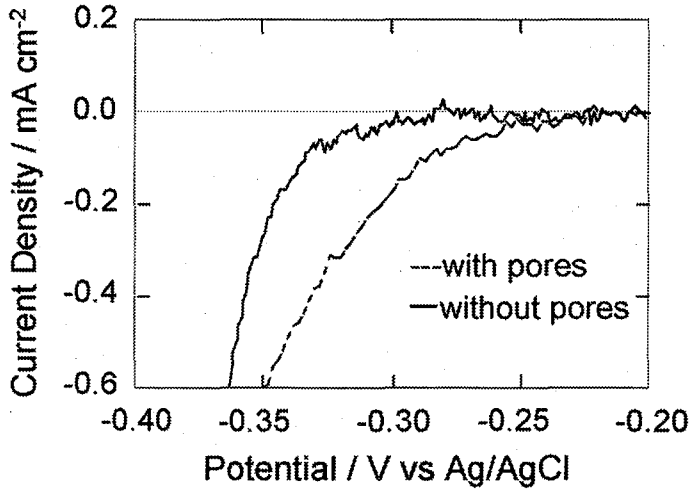


Figure 4. Current – potential curves measured in a solution containing 0.1 M $CuSO_4$ and 1.8 M $H_2SO_4$ using n-Si samples with and without pores. The pores were formed by using Au particles as catalysts and reached to a depth of about 70 μm from the surface.

deposited only in the pores by applying appropriate potential to the sample.

To confirm the deposition of Cu in the pores of Si, we observed the cross sections of Si samples after depositing Cu electrochemically. Figure 5 shows SEM images of samples after depositing Cu for 5 h at different electrode potentials between -0.25 V and -0.40 V vs Ag/AgCl in a solution containing 0.1 M $CuSO_4$ and 1.8 M $H_2SO_4$. When a potential of -0.25 V vs Ag/AgCl was applied to Si wafers with and without pores, Cu was not deposited on the surface or on the Au particles, as shown in Figure 5(a). When a Si wafer without pores was processed at a potential of -0.275 V vs Ag/AgCl, Cu was not deposited on the surface. However, when a Si wafer with pores were processed at this potential for 5 h, Cu was deposited from the bottoms of the pores to a height of about 30 μm from the bottoms, as shown in Figure 5(b). Cu was selectively deposited on the surface of the Au particles and grew up toward the Si surface. The selective Cu deposition in the pores is because the

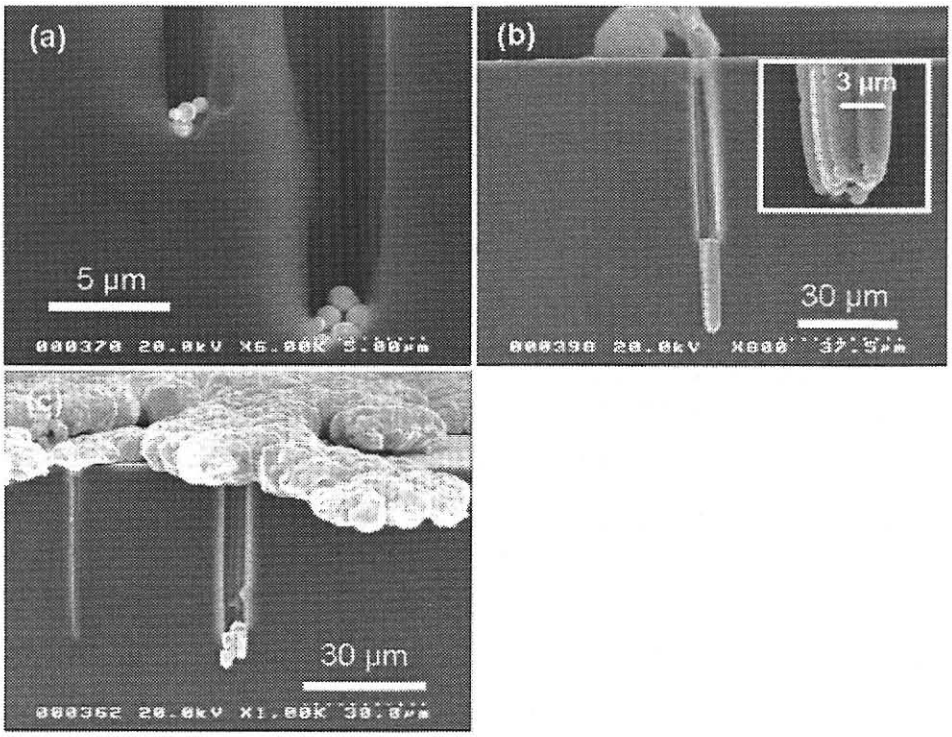


Figure 5. Cross-sectional SEM images of 70 μm deep pores of Si after electroplating Cu for 5 h at potentials of (a) -0.25 V, (b) -0.275 V, and (c) -0.40 V. The inset in (b) is a magnification of the bottom part. The solution for electroplating contained 0.1 M $CuSO_4$ and 1.8 M $H_2SO_4$.

exchange current density for Cu electrodeposition is much higher on Au/Cu than on Si. However, a few Cu deposits were formed on the top surface of Si. Such a Cu deposit is shown in Figure 5(b). These Cu deposits on the surface were probably formed as a result of Cu deposition on Au particles existing at bottoms of shallow pores. As discussed before, some shallow pores were formed besides deep pores.

When cathodic potential was further lowered to -0.40 V vs Ag/AgCl, the deposition of Cu took place on the surfaces of Si wafers with and without pores. As a result, a large amount of Cu was deposited on the surface of Si wafers. However, deposition of Cu at the bottom of the

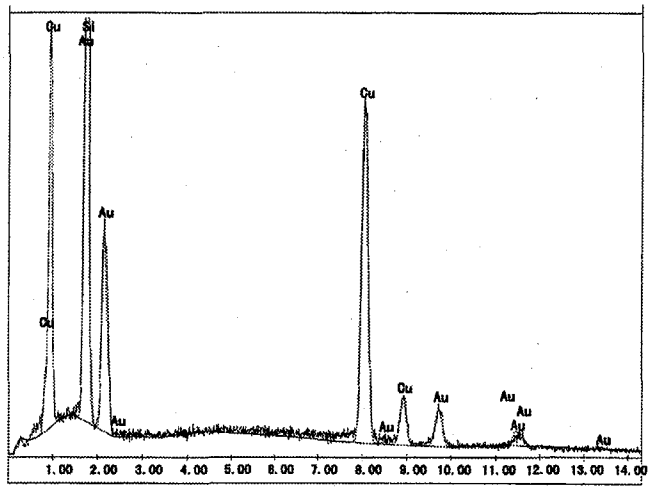


Figure 6. EDX analysis of deposited Cu in pores formed in Si after electroplating Cu for 5 h at potentials of -0.25 V in a solution containing 0.1 M $CuSO_4$ and 1.8 M $H_2SO_4$.

pore was scarce even after processing for 5 h, as shown in Figure 5(c). This is probably because the mouth of the pore was capped by the Cu deposited on the surface. In addition, Cu ions might be consumed at the surface before penetrating into the pores. The deposition of Cu was confirmed by EDX analysis, as shown in Figure 6. Signals due to Au were also detected because the detected area was close to the interface between deposited Cu and Au. From these results obtained, we concluded that the appropriate potential for Cu electrodeposition in the pores is about -0.275 V vs Ag/AgCl.

*Growth of Cu wires in pores*

To fill the 70 μm deep pores in Si with Cu, the processing time was extended up to 10 h and 16 h with potential kept at -0.275 V vs Ag/AgCl. The results are shown in Figure 7(a) and (b), respectively. Pores were filled to about 50 μm from the bottom after processing for 10 h, and they were filled up to the surface without the formation of any voids. When the Cu wire

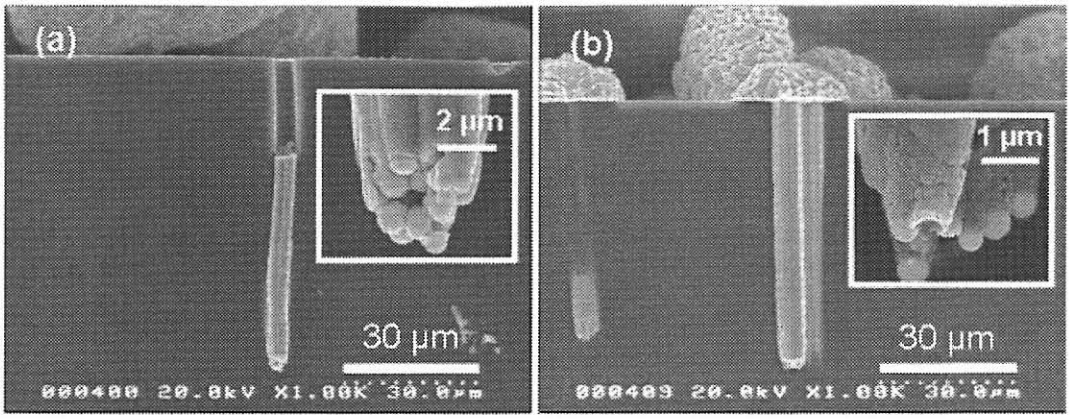


Figure 7. Cross-sectional SEM images of 70 μm deep pores of Si after electroplating Cu at -0.275 V for (a) 10 h and (b) 16 h. The insets are magnifications of the bottom parts. The solution for electroplating contained 0.1 M $CuSO_4$ and 1.8 M $H_2SO_4$.

reached the Si surface, it caused a deposition of Cu on the surface, forming hemispherical deposits. The growth rate of the Cu wires, before reaching the surface, was estimated to be about 5 μm/h.

Cathodic current was measured during Cu deposition at a potential of -0.275 V vs Ag/AgCl. In the Si sample without pores, the current was negligibly small. This result is consistent with the fact that no Cu was deposited on the surface of the sample without pores at this potential. When Si samples with pores were used, a cathodic current was observed, as shown in Figure 8. The initial current density was about 0.05 $mA/cm^2$. Then, the current density increased and became almost constant in about 100 min at 0.27 $mA/cm^2$. The current density estimated from the total area of pores on the Si surface (0.68 %) and the rate of Cu electrodeposition (5 μm/h) is about 0.06 $mA/cm^2$. The larger current observed after the initial 30 min is probably due to deposition of Cu on the Si surface from Au particles existing near the surface, as expected from the SEM image shown in Figure 5(b). The increase in the current density for the initial 30 min may be due to the increase in the size of the Cu deposits.

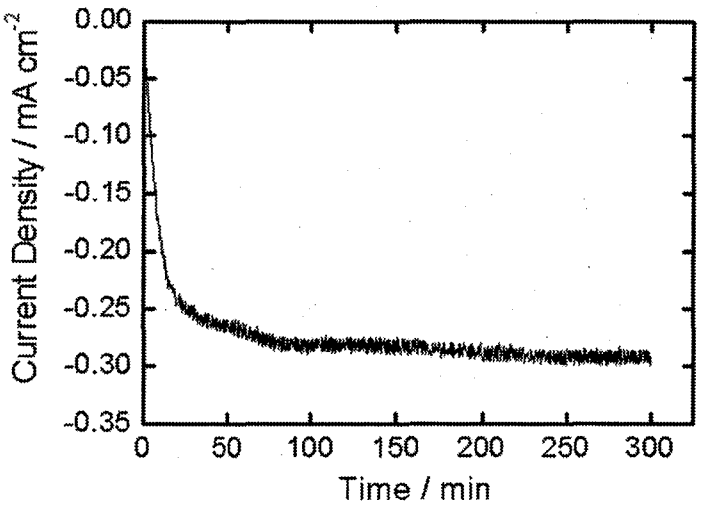


Figure 8. Current observed during electroplating of Cu on Si with 70 μm deep pores at -0.275 V in a solution containing 0.1 M $CuSO_4$ and 1.8 M $H_2SO_4$.

To further demonstrate the usefulness of Au particles as seeds for Cu deposition, we investigated Cu deposition into pores from which Au particles had been removed. The Au particles at the bottoms of the pores were removed by immersing the samples in a mixed solution of 70% $HNO_3$ and 35% HCl at a volume ratio of 1:3 for 30 min. Using these samples, Cu deposition by electroplating was carried out at a potential of -0.275 V vs Ag/AgCl for 5 h. After this process, fine Cu particles were randomly deposited on the wall of the pore, and bottlenecking occurred in the upper part, as shown in Figure 9. This result indicates the usefulness of Au particles existing at the bottoms of the pores for Cu electrodeposition in the pores of Si.

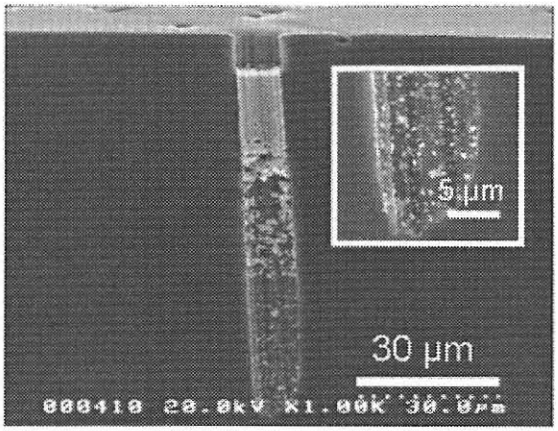


Figure 9. Cross-sectional SEM images of a 70 μm deep pore of Si after electroplating Cu at -0.275 V for 5 h. Au particles were removed from the pore before the electroplating process. The inset is a magnification of the bottom part.

### 3.4 Conclusions

In this chapter, we made vertical pores with diameters of about 5 μm in Si (100) wafers by a wet process using aggregated Au particles as catalysts. The pores reached 100 μm deep after etching for 5 h, and then Cu was electrochemically deposited in the pores. When potentials about -0.275 V vs Ag/AgCl was applied to the Si sample, the pores were filled with Cu. By continuing the deposition of 16 h, 70 μm deep pores were filled with Cu completely. In the process, Au particles, which had been used as catalysts for pore formation, acted as seeds for the bottom-up Cu filling. Because of its simplicity, this method is useful for making through-wafer wiring. If we can make pores in Si at a higher rate at desired positions by controlling the positions of Au particles, the method may be used for fabricating trench capacitors, through-wafer interconnects of high-density electronic packaging, and carrier-correcting electrodes for solar cells.

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# *CHAPTER 4*

*Electrochemical Groove Formation in Silicon Wafers*

*Using Catalytic Wire Electrodes*

# Chapter 4

# Electrochemical groove formation in silicon wafers using catalytic wire electrodes

## 4.1 Introduction

As described in chapter 1, the multi-wire slicing [1,2] is advantageous over inner diameter (ID) sawing [3] for slicing Si ingots because it enables an ingot to be sliced into hundreds of wafers at the same time. Currently, the multi-wire slicing is the leading technology for high precision machining of large cross-sectional area wafers for both the semiconductor and photovoltaic industries. However, the slicing cost remains high; it accounts for about 30% of the cost of wafer manufacture [1]. Besides, the multi-wire slicing produces Si waste, i.e., so-called kerf loss, which is usually about 200-250 μm in width per wafer [2]. It means that half of a silicon ingot changes to waste during slicing. Moreover, it causes surface damage (microcracks) to the Si crystal near the cutting part due to the mechanical force applied. The kerf loss and mechanical damage are also problems in dicing chips by the mechanical process. Hence, the elimination of these disadvantages due to the mechanical processes is important for improving the productivity and reducing the production cost.

To solve these problems, we considered a new method for processing Si by means of catalytic reactions. In chapter 2, we reported that cylindrical micropores are formed in Si by a wet process using Au particles as catalysts in aqueous HF solutions containing $H_2O_2$ as an oxidant [4]. As the pore grows, the metal particle existing at the end of a pore sinks into the bulk of Si. This suggests that Si is oxidized at the Si/catalyst interface, and then the Si oxide is

dissolved into the solution containing HF. The mechanism for pore formation using nanometer-sized metal particles as catalysts has been reported by Tsujino and Matsumura [5-7]. We expected that this mechanism can be applied to grooving Si wafers and slicing Si ingots if metal wires are used instead of metal particles. We also thought that it would be possible to use electrochemical anodic potential for the oxidation of Si in place of chemical oxidants.

An electrochemical method for making grooves in Si would be advantageous over conventional mechanical processes because the process does not cause mechanical damage to the substrate. In addition, kerf loss can be greatly reduced by using very thin wires. In this chapter, we report groove formation in Si wafers by an electrochemical process using different kinds of catalytic wires with a diameter of 50 μm, such as Ag, Au and Pt. To investigate the effect of diameters of Pt wires, Pt wires with different diameters were used. Additionally, we also studied the grooves formation in Si by using Pt plates with 50 μm as catalysts. The results may lead to the development of methods for grooving and dicing chips and for slicing Si wafers from ingots. It should be noted that the process is entirely different from electrochemical polishing [8] (or machining) because no electrochemical potential is applied to Si.

## 4.2 Experimental

In the grooving experiments, p-type (boron-doped) Si (100) wafers with a resistivity of 90-110 Ωcm were used. The wafers were obtained from Electronics and Materials Co. The thickness was 250 μm and one side was mirror-polished. The wafers were cut into rectangles of about $10 \times 5$ mm$^2$ in size. The long sides of the samples were usually directed to <010>.

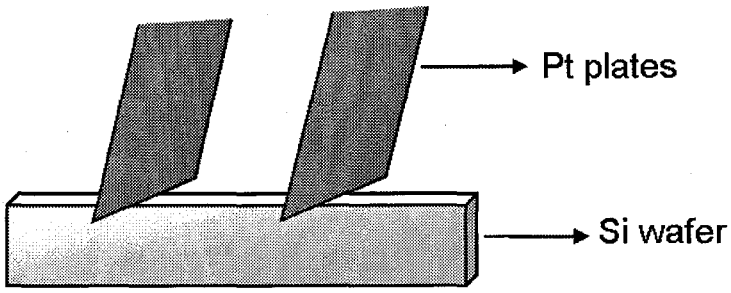


Figure 1. A setup for grooving Si using 50-μm-thick Pt plates as catalysts for grooving Si wafers.

Prior to the experiment, the samples were cleaned by immersing in a mixture of hydrogen peroxide and sulfuric acid mixture (30% $H_2O_2$ : 97% $H_2SO_4$=1:4 in volume) for 10 min followed by rinsing with ultrapure water (UPW, $>$18 MΩcm) for 10 min.

Au, Ag and Pt wires with 50 μm in diameter were used as the catalytic wires for grooving Si wafers. Additionally, Pt wires with diameters of 30 μm, 50 μm and 100 μm were used as the catalytic wires for investigating the effect of the diameter of Pt wires. 50-μm-thick Pt plates were utilized as well. A setup for grooving using the Pt plates as catalysts for grooving Si wafers is shown in Figure 1. The two Pt plates were pressed to the Si wafer when a grooving experiment was carried out. All of the catalytic materials were purchased from Nilaco Co. The experimental setup for electrochemical grooving of Si wafers is illustrated in Figure 2. First, a Si sample was mounted in a slit made in a Teflon holder. The long side of the sample was placed horizontally. Next, two catalytic wires, about 0.7 mm apart from each other, were set on a Teflon jig and brought into contact with the Si sample at the long side. The Teflon jig was positioned using guides (not shown in Figure 2), and the catalytic wires were pressed to the Si wafer by the gravity of the Teflon jig, which was about 20 g.

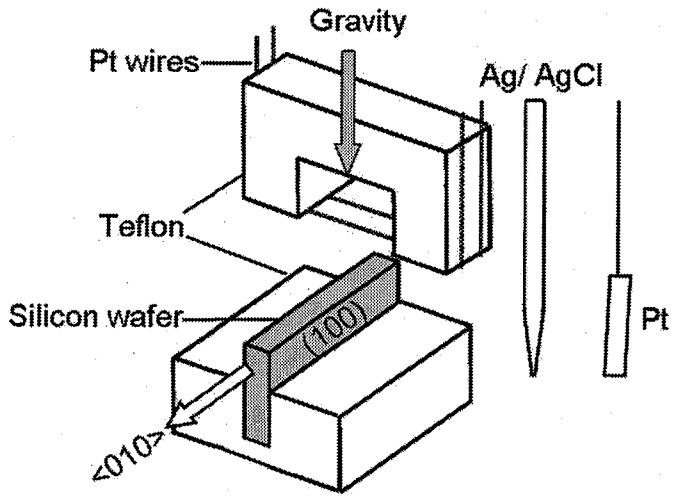


Figure 2. Experimental setup for electrochemically grooving a Si wafer in HF solution. The long side of the Si sample was usually directed to <010>.

An aqueous solution of 30 M HF was then poured into the Teflon beaker. Finally, an anodic potential of 2 V was applied to the catalytic wires by using a potentiostat (Hokuto Denko, HSV-100). An Ag/AgCl electrode and a Pt plate were used as a reference electrode (RE) and a counter electrode (CE), respectively. The total length of the catalytic wires immersed in the HF solution was about 40 mm. All of these processes using the HF solution were carried out in a hood equipped with a scrubber.

After the electrochemical process, the morphologies of the grooves formed in the Si sample were observed with a scanning electron microscope (SEM, Hitachi S-5000). In some experiments, energy dispersive X-ray spectroscopy (EDX) was used for the elemental analysis of the samples.

## 4.3 Results and Discussion

*Investigation of Pt plates and different kinds of metal wires as catalysts*

In general, catalytic property is strongly dependent on metals. Hence, the grooving of Si using different kinds of wires was investigated in this section. Pt, Ag, Au wires with 50 μm in diameter were used as the catalytic wires for grooving Si wafers. An anodic potential of 2 V was applied to the catalytic wires and all the treatments were carried out in 30 M HF solution for 2 h. When 50-μm Pt wires were used for grooving, two parallel grooves were formed in Si to a depth of 895 μm, as shown in Figure 3 (a). Because the Pt wires accept electron from Si, positive holes are generated in Si. The positive holes injected into Si result in oxidation of Si. The grooving proceeds as oxidized Si dissolves into a HF solution by producing $SiF_6^{2-}$ by [4]

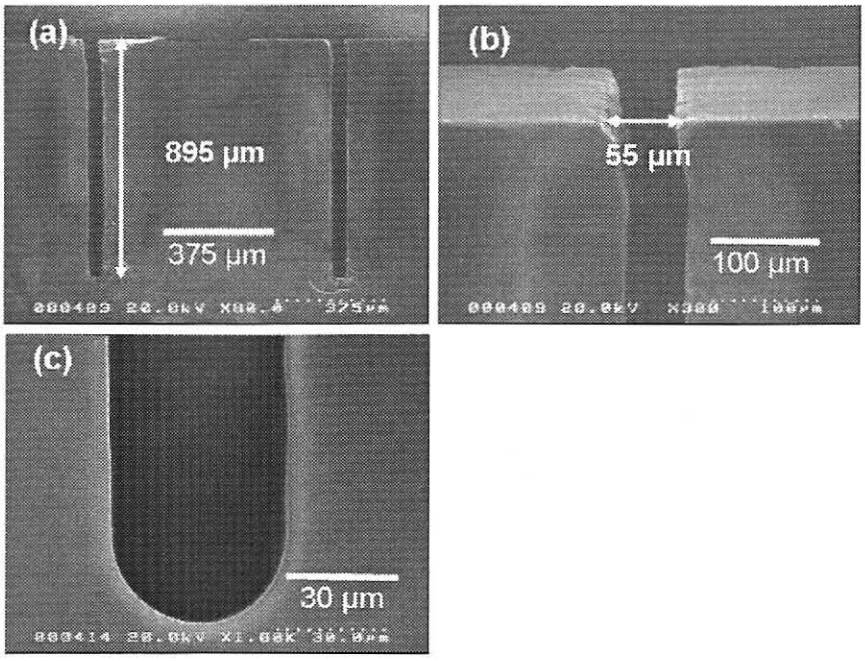


Figure 3. (a) SEM images of grooves formed in Si(100) wafers using Pt wires with a diameter of 50 μm. The wafer was electrochemically processed for 2 h in 30 M HF solution at 22 °C. (b) and (c) were magnified images of (a) at the top and bottom of the grooves, respectively.

$$Si + 6\,HF - 4\,e^- \rightarrow SiF_6^{2-} + 6\,H^+ \qquad (1)$$

As discussed in Chapter 2, the reaction occurs as a result of catalytic oxidation of Si at Si/metal interface. Figure 3(b) shows that the width of one groove was around 55 μm, which was approximately the same as the diameter of the Pt wires (50 μm). This suggests that by this electrochemical method, kerf loss can be reduced down to one fourth of that produced by the multi-wire slicing. The edges of the grooves were sharp and the bottom was hemispherical, representing the shape of the Pt wire, as shown in Figure 3(c). These results indicate that the grooves were formed at the Si/Pt interface.

Figure 4 shows the current flowing during the electrochemical process at 2 V vs Ag/AgCl was about 0.28 mA. The large fluctuation of the current is probably due to oxygen bubbles formed on the Pt wires, especially in the grooves. When the Pt wires were not in contact with the Si wafer, the current was about 0.02 mA. This current was attributed to oxidation of water in the solution. Hence, when the Pt wires were in contact with the Si sample, about 90- 95% of the current was used for oxidation of the Si sample, including the grooving. The current in

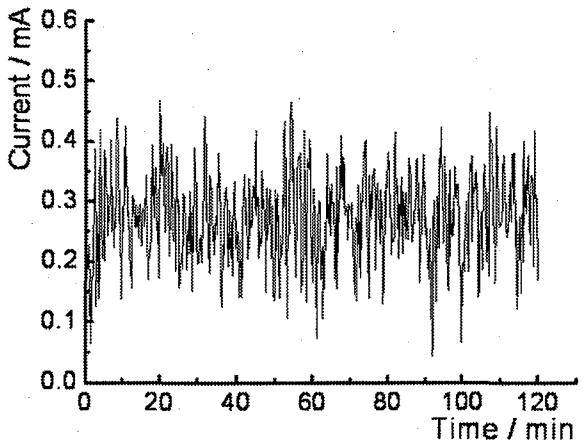


Figure 4. Current vs time during electrochemical grooving using Pt wires with a diameter of 50 μm at 2 V vs Ag/AgCl in 30 M HF at 22 °C.

the initial 5 min was low, as seen in Figure 4, probably due to the small area of the Si/Pt interface until the Pt wires sank into Si. The total charge of the current during the 2-h processing was 1.97 C. During this period, $2.46 \times 10^{-5}$ $cm^3$ ($2.04 \times 10^{-6}$ mol) of Si was dissolved judging from the shape of the grooves formed. By assuming that 4 electrons are removed to oxidize a Si atom, the current efficiency of the grooving is estimated to be 40.1%. In other words, about 59.9% of the electric charge was not used for groove formation. We speculate that it was consumed for the etching of Si at places apart from the grooves and for oxidation of water in HF solution. We found that the current efficiency of grooving depended on the concentration of the HF solution and the properties of the Si samples.

To clarify the grooving process in detail, the growth of grooves with processing time was investigated. The depths of grooves formed after processing for different time periods under the condition of applied voltage of 2 V vs Ag/AgCl in 30 M HF are shown in Figure 5.

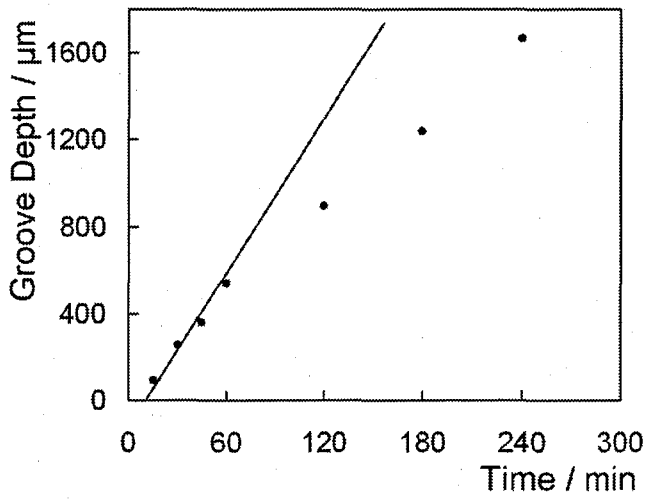


Figure 5. Relationship between depth of grooves formed in Si wafers and processing time. The grooves were formed by applying 2 V vs Ag/AgCl to Pt wires with a diameter of 50 μm in 30 M HF at 22 °C.

For the first hour, the depth increases linearly at a rate of about 11 μm $min^{-1}$. After this period, the relationship deviates downward to some extent from the linear relationship. This tendency is probably due to the lowered diffusion of chemical species, i.e., supply of HF and removal of dissolved Si species in the form of $SiF_6^{2-}$ [9], into and out of the deep grooves.

Besides wire electrodes, Pt plates with 50 μm in thickness were utilized for grooving of Si because the Pt plates are mechanically stronger than Pt wires. Figure 6 shows the SEM images of groove formation in Si using Pt plates after 2-h treatment in 30 M HF solution. The grooves with a depth of 340 μm were formed in Si, as shown in Figure 6(a). However, the grooving formation was relatively slow, compared to that formed by using Pt wires as shown in Figure 3(a). In addition, the width of grooves broadened as large as about 78 μm (Figure 6(b)). We speculate that as the grooving proceeded, the oxidative dissolution of Si occurred not only at the bottom of the grooves but also at the interface between Si and the sides of Pt plates.

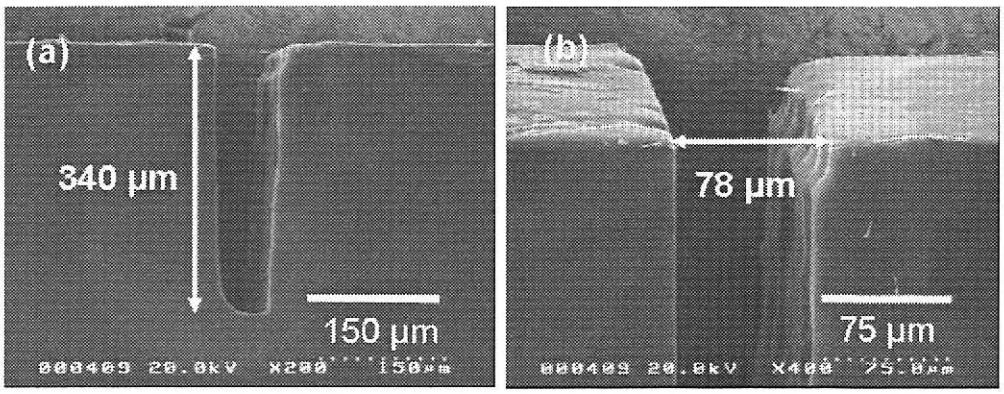


Figure 6. (a) A SEM image of grooves formed in Si(100) wafers using Pt plates with 50 μm in thickness. The wafer was electrochemically processed for 2 h in 30 M HF at 22 °C. (b) was a magnified image of (a) at the top of one groove.

The lateral etching caused enlargement of the groove width and also lowering of the grooving rate. The grooving rate was lowered because the etchant (HF) was consumed at the sides of the Pt plates. This problem may be solved by coating the sides of Pt plates with an insulating thin film.

When an anodic potential of 2 V was applied on the Au wires with a diameter of 50 μm in 30 M HF for 2 h, grooves in Si reached a depth of 1,700 μm, as shown in Figure 7. The grooves were almost twice as deep as those formed by Pt wires under the same conditions (Figure 3(a)). We speculate that the injection of positive holes into Si is easier at the Si/Au interface than at the Si/Pt interface. However, we found that the Au wires dissolve gradually into the 30 M HF solution at 2 V vs Ag/AgCl. As shown in Figure 7(b), plenty of nanometer-sized particles were observed on the silicon surface, especially near the grooves.

Figure 8 shows the EDX analysis of the nanometer-sized particles, existing on the Si surface near grooves. It confirms that the nanometer-sized particles were Au. The result indicates that Au wires were dissolved as Au ions and then the Au ions reprecipitated on the surface of silicon to form a lot of nanometer-sized particles. Hence, the operational voltage

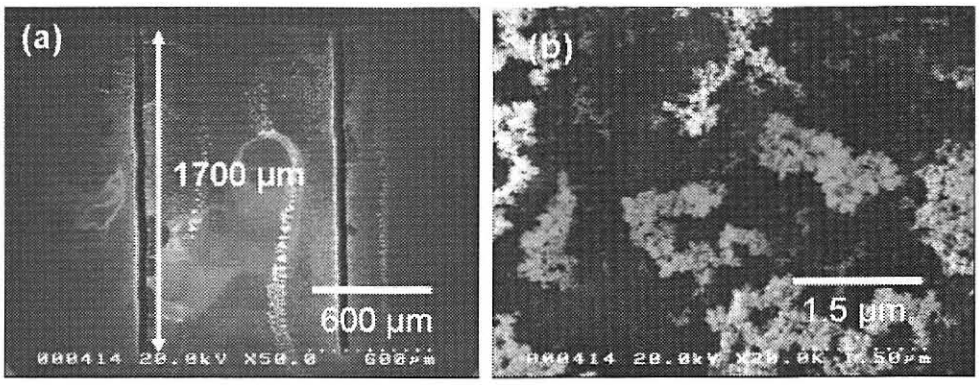


Figure 7. (a) SEM images of grooves formed in Si(100) wafers using Au wires with a diameter of 50 μm. The wafer was electrochemically processed for 2 h in 30 M HF at 22 °C (b) was the magnified surface image of (a).

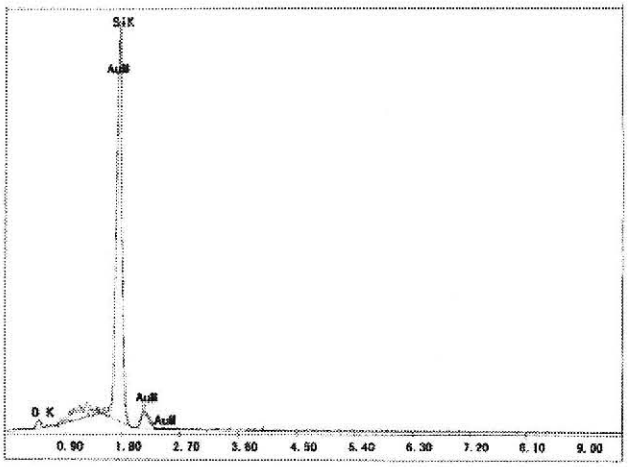


Figure 8. EDX analysis for the nanometer-sized particles existing near the grooves.

should be lower to use the Au wires. This would inevitably lower the grooving speed and impair the merit of using Au wires.

On the other hand, when 2 V vs Ag/AgCl was applied to Ag wires, the Ag wires dissolved into the HF solution at much faster speed and the wires were cut in less than 5 min. No grooves were formed in Si before the wires were cut and only the corners of the sample, at which the Ag wires were in contact, were shaved, as shown in Figure 9(a). The Si surface near the corners became rough. On the surface, large Ag aggregates and nanometer-sized Ag

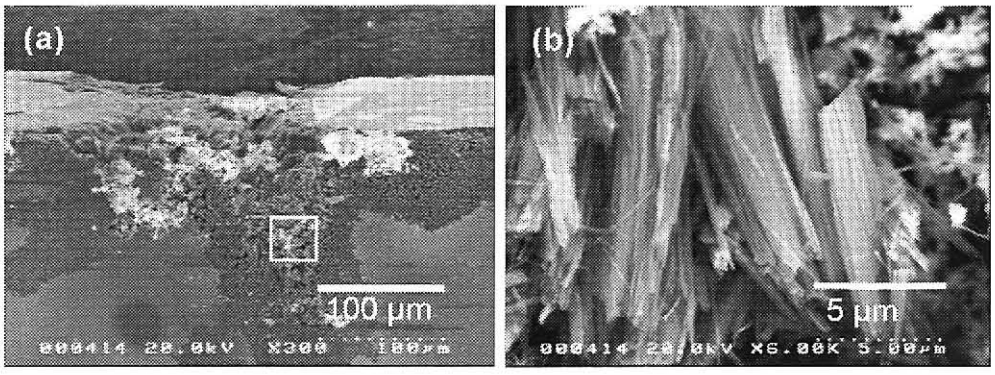


Figure 9. (a) SEM images of Si wafers treated for 2 h with Ag wires by applying 2 V vs Ag/AgCl to the wires in 30 M HF at 22 °C. The Ag wires were cut in about 5 min after starting the treatment. (b) was the magnified surface image of (a).

particles were observed. The roughening of the Si surface near the corners is attributed to the nanometer-sized pores generated by the Ag particles, which were reprecipitated from the solution. On the roughened Si surface, Si nanowires were formed as shown in Figure 9(b). The formation of Si nanowires on the Si surface, on which nanometer-sized Ag particles are deposited, has been reported by Qiu *et al.* and Peng *et al.* [10, 11]. We consider that numerous nanometer-sized Ag particles migrated into silicon as Si was oxidatively dissolved in a HF solution, forming the nanometer-sized pores. The nanowires were the undissolved part when the nanometer-sized pores were formed in Si. We also consider that dissolved oxygen in the HF solution may act as an oxidant for the oxidative dissolution of Si [12].

The precipitation of Ag on the Si surface was confirmed by the EDX analysis as shown in Figure 10. Compared to Pt and Au wires, it was found that the Ag wires were more easily dissolved into the Ag ions in a HF solution. Because Si is more likely to be oxidized than Ag [13, 14], the Ag ions can be reduced and precipitated as Ag masses and particles on the Si surfaces concomitantly with the oxidative dissolution of Si in HF solutions. The same phenomenon was found in pore formation in Si using Ag particles with a diameter of 1 μm as catalysts [4].

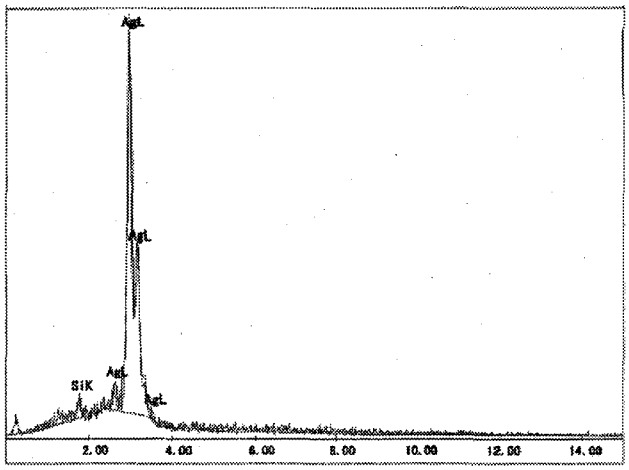


Figure 10. EDX analysis for the particles precipitating on the roughened Si surface.

*Effect of the diameter of Pt wires*

From the comparison of different metal wires, we found that Pt wires are appropriate for grooving Si wafers in HF solutions. Because kerf loss significantly depends on the diameter of slicing wires, the diameter of catalytic wires is another important factor influencing the saving of Si. Hence, experiments using Pt wires with diameters of 30 and 100 μm as grooving tools were carried out for 2-h processing by applying 2 V vs Ag/AgCl in a 30 M HF solution. As shown in Figure 11(a) and (c), the depths of the grooves formed using Pt wires with diameters of 30 and 100 μm were 974 and 538 μm, respectively. The curved grooves seen in Figure 11(a) were due to the structure of the jig for guiding Pt wires. This problem can be solved by improving the structure. As shown in Figure 11(b) and (d), the widths of the

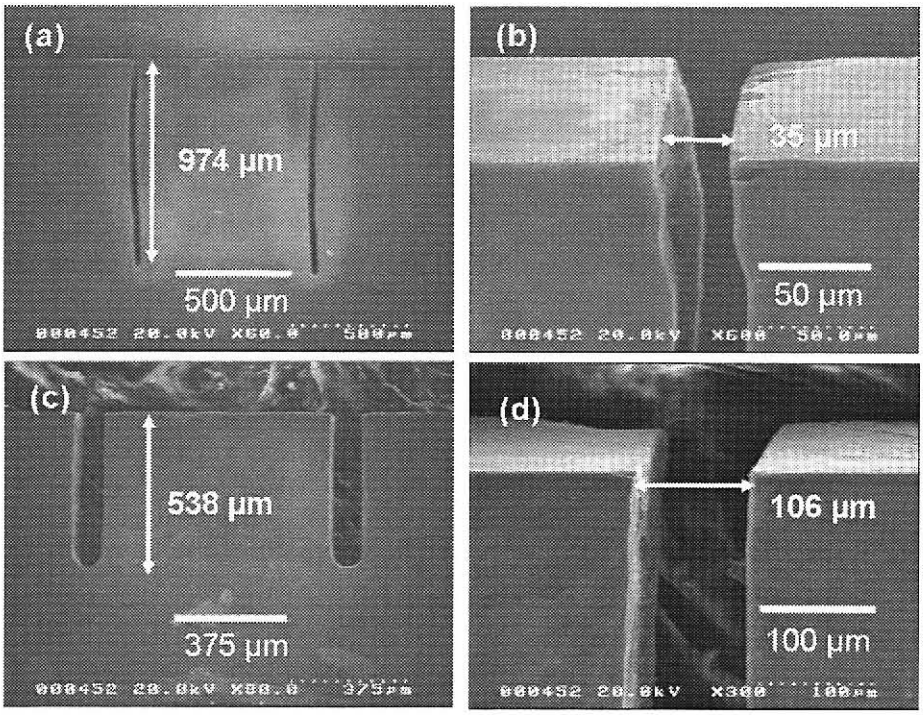


Figure 11. (a) and (c) were SEM images of groove formation in Si using 30 μm Pt wires and 100 μm Pt wires, respectively. (b) and (d) were the magnified images of (a) and (c), respectively. The wafers were electrochemically processed for 2 h in 30 M HF at 22 °C.

grooves formed by Pt wires with diameters of 30 and 100 μm were about 35 and 106 μm, respectively. These widths are much smaller than that produced by the multi-wire slicing method. Because in principle no mechanical force is needed for the electrochemical grooving, the width of the grooves can be further decreased by using fine wires.

It is found that the grooving rate became faster as the diameter of Pt wires was smaller, as shown in Figure 3(a), Figure 11(a) and (c). In the experiments, the catalytic wires were pressed by the gravity of the jig. However, because of the difference in the diameters of the wires, the pressure applied to the Si/Pt interface became higher for the wires with smaller diameters. We consider that this is responsible to the fast grooving for the wires with small diameters. The relationship between the grooving rate and the pressure is plotted in Figure 12. The pressure was calculated from the effective contact area of the interface, i.e., the diameter of the Pt wires × the thickness of the Si wafer. The grooving rate increased when the pressure

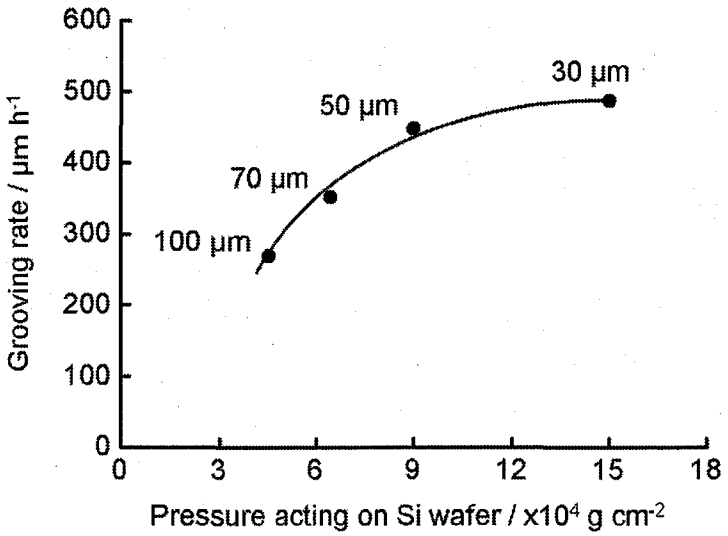


Figure 12. Relationship between the grooving rate in 250-μm-thick Si wafers and the pressure applied to the Si/Pt interface. The grooves were formed in Si using Pt wires with different diameters to which 2 V vs Ag/AgCl was applied in 30 M HF.

applied to the Si/Pt interface was high as shown in Figure 12. However, the grooving rate did not increase when the pressure reached $15 \times 10^4$ g $cm^{-2}$ using Pt wires with a diameter of 30 μm. It may be due to the difficulty of diffusion of chemical species at the very narrow Si/Pt interface. The effect of the pressure at the Si/Pt interface on the grooving rate is discussed in more detail in Chapter 5.

## 4.4 Conclusions

In this chapter, the electrochemical grooving of Si wafer using catalytic wire electrodes is reported. The grooves formed in Si were significantly affected by the kind of metal wires used as catalysts. It was also found that the grooving rate was greatly affected by the diameter of the metal wires: it became faster as the diameter decreased. By using Pt wires with a diameter of 50 μm, grooves with a width of about 55 μm were formed. Because this width is much smaller than the width of the kerf formed by the multi-wire slicing, this process is useful for reducing material loss. Another advantage of the method is that theoretically no defects are introduced into the Si crystal lattice because the grooves are formed by a chemical process, not by a mechanical process. These properties are desirable as a process for slicing Si wafers from ingots and dicing chips from wafers. The problem to be solved for application of the method to real processes is its low grooving speed. We think that the method can also be used for making grooves in other semiconductors and metals.

## 4.5 References


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# *CHAPTER 5*

*Parameters Affecting Electrochemical Groove Formation in Silicon Wafers Using Catalytic Wire Electrodes*

# Chapter 5

# Parameters affecting electrochemical groove formation in silicon wafers using catalytic wire electrodes

## 5.1 Introduction

Multi-wire slicing and inner diameter (ID) sawing have conventionally been used for slicing ingots. In recent years, the multi-wire slicing is the leading technology of fabricating Si wafers for both the semiconductor and photovoltaic industries. However, the slicing cost amounts to about one third of the total processing cost for solar cells and module fabrication [1]. The high slicing cost mainly results from low throughput and inefficient use of materials due to kerf loss and mechanical damages produced during slicing. Therefore, minimizing the kerf loss and damages is very important to reduce the production cost of silicon wafers. They are also important to extend the utilization of solar power generation because the high cost of the electricity produced by solar panels hampers their installation in a large scale.

In order to solve the problems of the mechanical slicing methods, wafer slicing by wire electrical discharge machining (WEDM) has been proposed [2-4]. Formation of damages on the machined surface is decreased by this method since the machining force acting on the workpiece in this method is extremely small compared to that in conventional slicing methods. Recently, Ideno *et al.* utilized atmospheric-pressure reactive microplasma, as another possible new method, to slice Si [5]. However, these methods need to be improved for practical applications.

The electrochemical groove formation in Si wafers using different kind of metal wires was described in chapter 4. In the groove formation process, metal wires work as catalysts and

induce hole injection into Si through the Si/metal interface. It was found that by using Pt wires with a diameter of 50 μm, grooves with a width of 55 μm were formed in Si [6]. It proves that the kerf loss during a slicing process can drastically be decreased by the electrochemical method. In this chapter, we study some experimental conditions such as anodic potentials applied to the Pt wires, temperature of HF solution, and HF concentration, which may significantly influence the grooving rate. Because the anodic dissolution of Si occurs at the Si/Pt interface, effect of pressure applied to the Si/Pt interface is investigated as well.

## 5.2 Experimental

In this work, p-type (boron-doped) Si (100) wafers with a resistivity of 90-110 Ωcm were used as samples after cutting into rectangles with a size of 10 x 5 $mm^2$. The thickness of the wafers was 250 μm. The wafers were obtained from Electronics and Materials Co. Prior to the experiment, the samples were cleaned by immersing in a mixture of hydrogen peroxide and sulfuric acid mixture (30% $H_2O_2$ : 97% $H_2SO_4$=1:4 in volume) for 10 min followed by rinsing with ultrapure water (UPW, $>$18 MΩcm) for 10 min.

Pt wires with a diameter of 50 μm, which were purchased from Nilaco Co., were used as the catalytic wires for grooving Si wafers. The experimental setup for electrochemical grooving of Si wafers was the same as that described in chapter 4, which is schematically illustrated in Figure 1. First, a Si sample was mounted in a slit made in a Teflon holder. The long side of the sample was placed horizontally. Next, two catalytic wires, about 0.7 mm apart from each other, were set on a Teflon jig and brought into contact with the Si sample at the

long side. The Teflon jig was positioned using guides (not shown in Figure 1), and the catalytic wires were mechanically pressed to the Si wafer using the gravity of a Teflon jig. Normally, the gravity of the Teflon jig was around 20 g. In some experiments, Teflon jigs with gravities of about 20, 60, 95, and 135 g were used for investigating effect of pressure applied to the Si/Pt interface. Then, an aqueous HF solution, typically at a concentration of 30 M, was then poured into the Teflon beaker. For the investigation of the effect of HF concentrations, HF solutions with concentrations 5 M to 30 M were used. Finally, a positive potential was applied to the catalytic wires using a potentiostat (Hokuto Denko, HSV-100). To investigate the effect of anodic potentials applied to Pt wires, anodic potentials 1 V, 2 V and 3 V vs Ag/AgCl were applied to Pt wires. In other experiments, an anodic potential applied to Pt wires was 2 V or 2.25 V vs Ag/AgCl.

An Ag/AgCl electrode and a Pt plate were used as a reference electrode (RE) and a counter electrode (CE), respectively. The total length of the catalytic wires immersed in the HF solution was about 40 mm. All of these processes using the HF solution were carried out in a

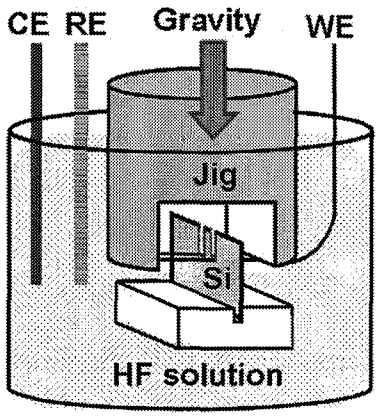


Figure 1. Experimental setup for the electrochemical grooving of a Si wafer in HF solution.

hood equipped with a scrubber.

After the electrochemical process, the morphologies of the grooves formed in the Si sample were observed with a scanning electron microscope (SEM, Hitachi S-5000).

## 5.3 Results and Discussion

*Effect of anodic potentials applied to Pt wires*

In Chapter 3, the grooves were successfully formed in Si after applying an anodic potential of 2 V vs Ag/AgCl to the Pt wires that were in contact with a Si wafer in 30 M HF solution. In this section, to increase the grooving rate, different anodic potentials for a certain period to the Pt wires were investigated. The structures of the grooves formed at different anodic potentials after the electrochemical processing for 2 h are shown in Figure 2. The upper side of the samples shown in Figure 2 (a) and (b) was directed to <010>. When an anodic potential of 1 V vs Ag/AgCl was applied to the Pt wires, grooves were barely formed except shaving of the corners of the wafer, as seen in Figure 2(a). In contrast, when processed at a potential of 2 V vs Ag/AgCl for 2 h, grooves were formed in Si to a depth of 895 μm, as shown in Figure 2(b). The width of the grooves was around 55 μm, which was nearly the same as the diameter of the Pt wires ($\varphi$ = 50 μm).

In most cases, the grooves were formed in the direction normal to the upper side of the sample, i.e., the grooves were directed to <001>. However, the direction of the grooves formed in the samples sometimes deviated slightly from the direction normal to the upper side of the samples, probably because of an unintentional slant of the samples or lateral forces unintentionally applied.

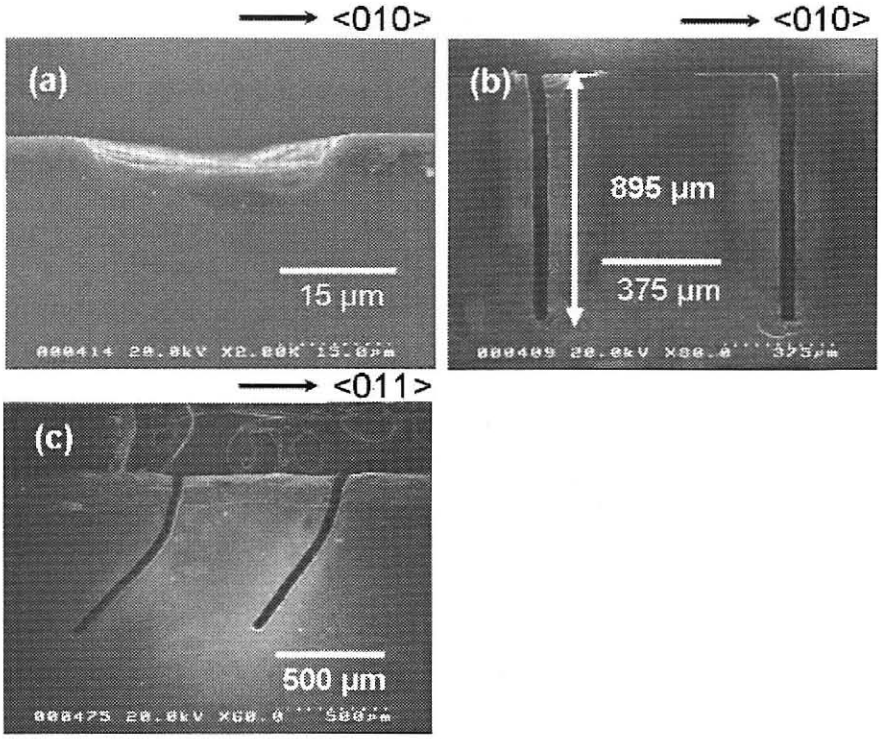


Figure 2. SEM images of grooves formed in Si (100) wafers using Pt wires with a diameter of 50 μm. The wafers were electrochemically processed for 2 h in 30 M HF at 22 °C by applying (a) 1 V and (b)-(c) 2 V vs Ag/AgCl to the Pt wires. The upper sides of the Si wafers were oriented in (a)-(b) <010> and (c) <011> directions.

When we used samples that were cut so that they have the long sides in the <011> direction, grooves were often formed in the direction that was about 45° from the long side of the sample, i.e., in the <100> direction, as shown in Figure 2 (c). More precisely, as seen in Figure 2 (c), the grooving direction came to the final direction of <100> after a short unstable period. In some cases, however, the grooves in these samples were formed normal to the long side, i.e., in the direction of <101>. These results suggest that the grooving direction is determined not only by the direction of the force applied to the wires but also by the crystallographic orientation; probably the (100) face is etched more easily than the (101) face.

When the potential was further raised to 3 V vs Ag/AgCl, the grooving speed increased. The grooves reached a depth of 1,240 μm with the 2-h processing, as shown in Figure 3(a). This depth is about 40% deeper than that of the grooves formed at 2 V vs Ag/AgCl. At this potential, however, the surface of the sample was roughened after the processing. A magnified SEM image of the Si surface near the groove revealed that many small particles were deposited on it, as shown in Figure 3(b). This result suggests that the Pt wires were anodically dissolved to some extent at this high voltage and that the dissolved Pt ions reprecipitated on the surface as metallic Pt particles, which occurred concomitantly with the oxidation of Si [7]. Because the Pt particles have the catalytic activity for the etching of Si in HF solution [8], the Si surface was roughened by the catalytic etching. Although we have not determined the optimal voltage for grooving Si at a high rate without damaging the Si surface, it should be around 2 V vs Ag/AgCl.

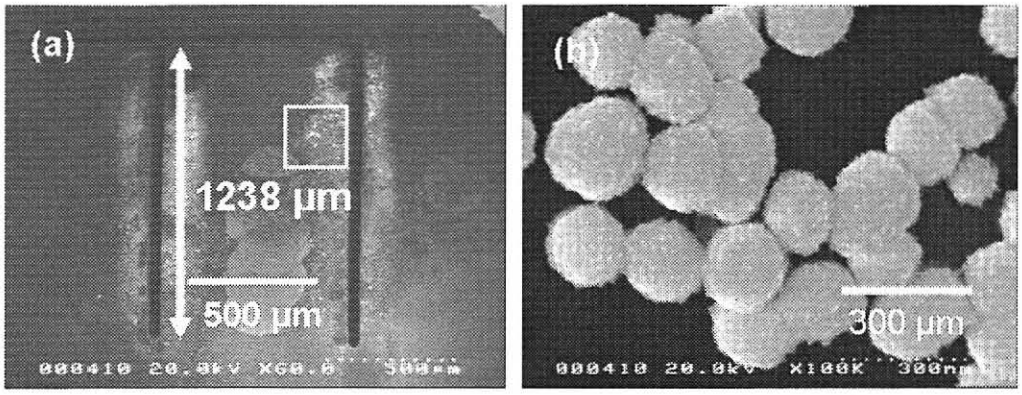


Figure 3 (a) An SEM image of grooves formed in Si wafers after processing for 2 h in 30 M HF at 22 °C by applying 3 V vs Ag/AgCl to the Pt wires with a diameter of 50 μm and (b) an enlarged image of the Si surface near a groove. The upper side of the Si sample was oriented in the <010> direction.

*Effect of temperature of HF solution*

The depth of grooves formed in Si depended on temperature of the HF solution. Using 50 μm-Pt wires and processing at 2 V for 2 h, the depths of the grooves formed in 30 M HF solutions of 7, 22, 33 and 45 °C were 485, 895, 1320 and 1520 μm, respectively, as shown in Figure 4 and Figure 2 (b). The widths of the grooves were almost independent of temperature; they were all about 55 μm. As the temperature of the HF solution increased, the surface of the samples became somewhat roughened on a micrometer scale and a so-called porous Si layer was formed around the grooves when processed at 45 °C, as shown in Figure 4(c). At high temperatures, more positive holes are injected into Si over an energy barrier existing at the

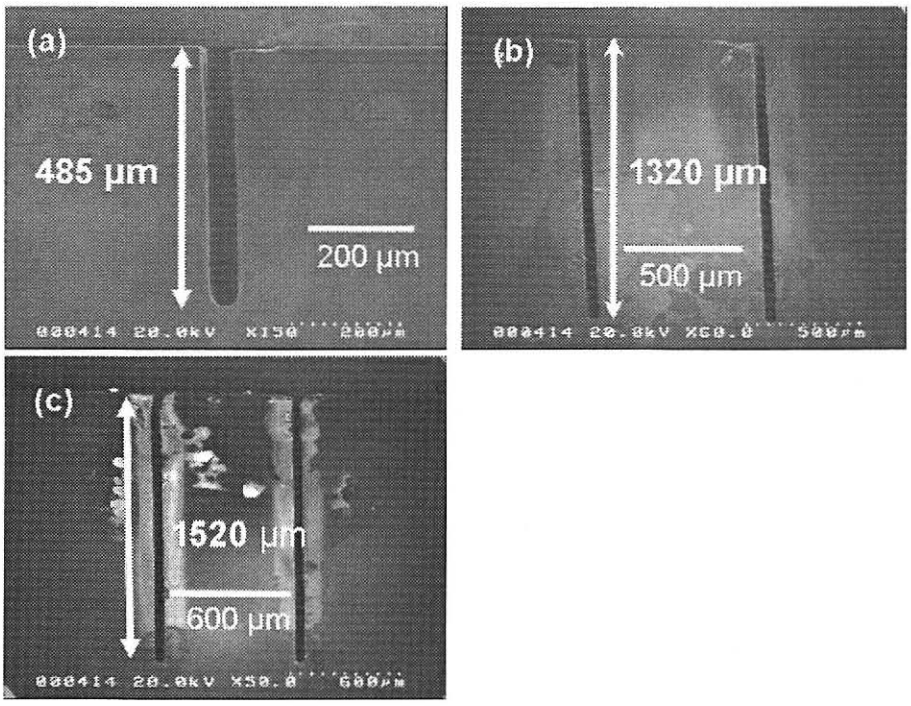


Figure 4. SEM images of grooves formed in Si wafers after processing for 2 h by applying 2 V vs Ag/AgCl to the Pt wires with a diameter of 50 μm in 30 M HF at (a) 7 °C, (b) 33 °C, and (c) 45 °C. An SEM image of grooves formed at 22 °C under the same conditions is shown in Figure 2(b).

Si/Pt interface, leading to fast grooving and also formation of a porous Si layer. The enhanced diffusion of chemical species in the grooves may also contribute to the fast grooving at higher temperatures.

*Investigation of HF concentration*

As a preparatory study for slicing silicon blocks, experiments were carried out to investigate the optimal experimental conditions by using single crystalline Si wafers. As one of the crucial parameters, the optimal concentration of HF for this process was elucidated. To find the optimal concentration, groove formation in single crystalline Si was investigated using Pt wires ($\varphi$ = 50 μm). In the grooving process, an electrochemical potential of 2.25 V vs Ag/AgCl was applied to the two Pt wires in contact with a Si wafer for 1 h. The concentration of HF solution was changed in the range of 5 to 30 M. The grooving rate was highest at the HF concentration of about 15 M and the rate reached about 1750 μm $h^{-1}$, as shown in Figure 5(a). The grooving proceeds as silicon is oxidatively dissolved into a HF solution by producing $SiF_6^{2-}$ by [9]

$$Si + 6\,HF - 4\,e^- \rightarrow SiF_6^{2-} + 6\,H^+ \qquad (1)$$

The reaction occurs as a result of catalytic oxidation of Si at the Si/Pt interface. Since the reaction needs HF, it is reasonable that the reaction rate increases with increase in HF concentration. The decrease in grooving rate at HF concentrations higher than 15 M may be due to the lowered solubility of $SiF_6^{2-}$ in the solutions with high HF concentration. Another possible explanation is that the oxidation of Si becomes slow in solutions with very high HF concentration (or with low $H_2O$ concentration); etching is a two-step process, i.e., oxidation by water and dissolution of the oxide into HF solutions.

The insets of Figure 5 show the morphologies of grooves formed in 5 M, 15 M and 30 M HF solutions. When processed in 5 M HF solution, grooves were V-shaped as shown in Figure 5 (b). This result indicates that holes migrated in the bulk of silicon and oxidatively dissolved silicon at sites not in contact with Pt wires. This is attributed to the slow dissolution of silicon at the Si/Pt interface in 5 M HF solution. At concentrations higher than 10 M, the width of the grooves was about 55 μm, which is nearly equal to the diameter of the Pt wires. This suggests that the dissolution rate of silicon is higher than the rate of hole injection at least at the potential of 2.25 V vs Ag/AgCl.

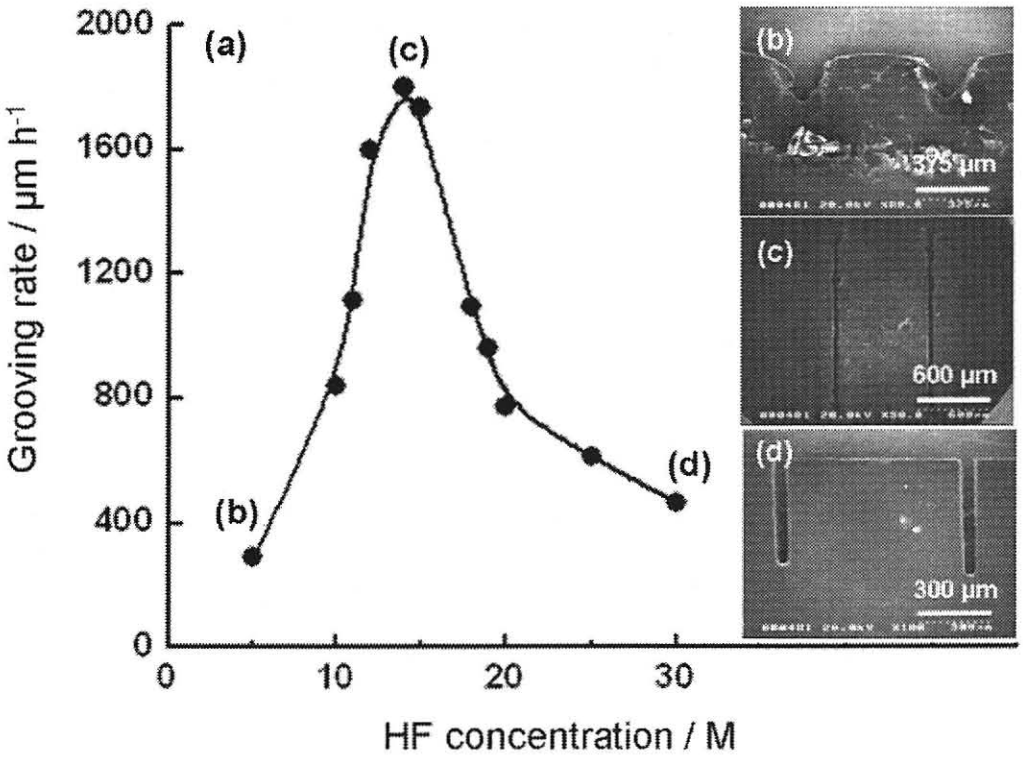


Figure 5. (a) Rate of grooving in 250-μm-thick Si wafers in HF solutions with different concentrations using Pt wires (φ, 50 μm) to which 2.25 V vs Ag/AgCl was applied, and SEM images of the grooves formed in (b) 5 M, (c) 15 M and (d) 30 M HF solutions.

*Morphologies of walls of grooves*

To observe the walls of grooves formed by the electrochemical process using Pt wire electrodes, Si samples were mechanically cleaved at the grooves. Figure 6(a) and (b) show SEM images of the walls of grooves formed by 1-h processing in 15 M and 30 M HF solutions, respectively.

The samples are the same as those shown in Figure 5(c) and (d). The arrows in the figures show the direction of groove formation. The pattern appearing on the wall processed in the solution of 15 M HF (Figure 6(a)) shows a more regular structure than that processed in 30 M HF solution. The difference in morphology is clearly seen in magnified images shown in

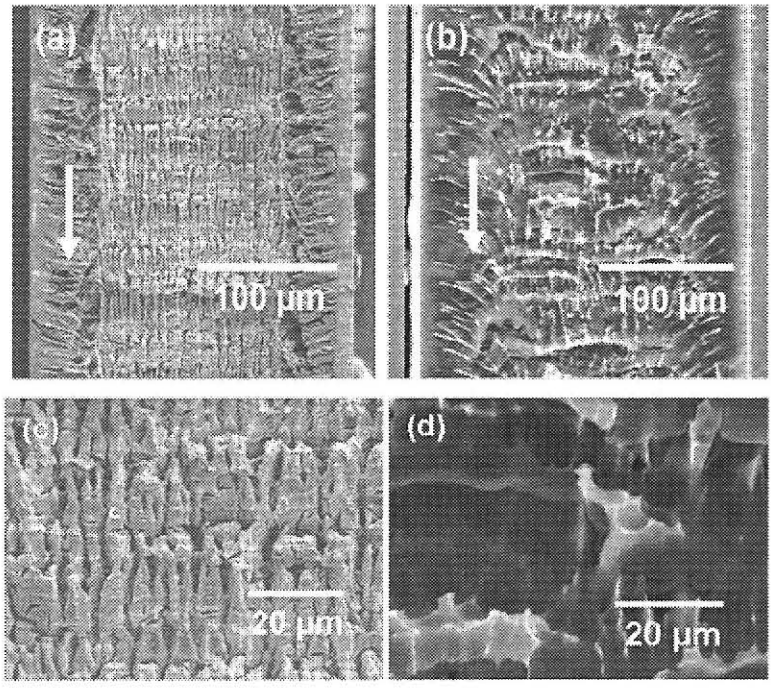


Figure 6. SEM images of walls of grooves formed in 250-μm-thick Si. The grooves were formed using Pt wires (φ, 50 μm) to which 2.25 V vs Ag/AgCl was applied in (a) 15 M and (b) 30 M HF; (c) and (d) are magnified images of (a) and (b), respectively.

Figure 6(c) and (d). In 15 M HF solution, the grooving rate was 4-times faster than the rate in 30 M HF solution, as shown in Figure 5. The regular morphology of the wall formed in 15 M HF solution is thought to be related to the rapid dissolution of Si in the solution. In the middle of the wall, shallow furrows with a length of about 20 μm are seen. However, at the edges of the groove wall, pores are seen in the direction perpendicular to the grooving direction. These holes are thought to have acted as channels for transferring the etching solution to and from the Si/Pt interface during the grooving process.

To further observe the detailed surface structure of the walls, samples were again cleaved to show cross sections of the walls. Figure 7(a) shows an SEM image of the sample processed in 15 M HF solution. In the observation, the sample was slightly tilted. The cross-sectional image shows that the pores formed on the wall are about 5 μm in depth, making the wall surface rough in this range. In contrast, when processed in 30 M HF solution, the pores formed on the wall were rougher to the degree of about 10 μm (image not shown). Another

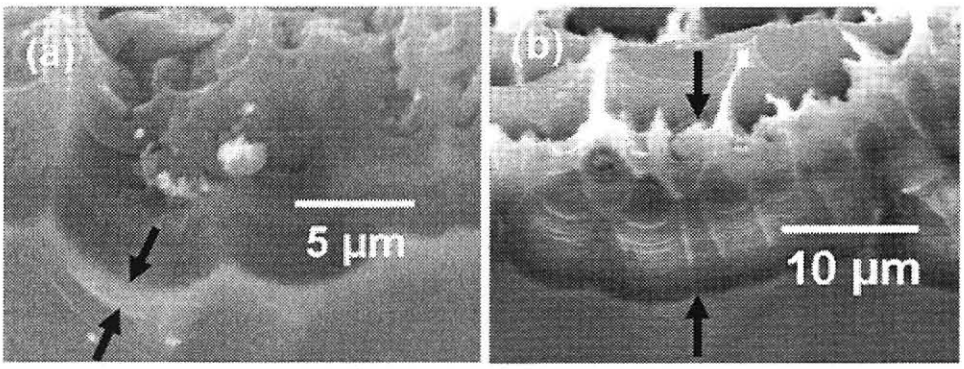


Figure 7. Cross-sectional SEM images of walls of grooves formed in 250-μm-thick Si wafers. The grooves were formed using Pt wires (φ, 50 μm) to which 2.25 V vs Ag/AgCl was applied in (a) 15 M and (b) 30 M HF solutions. The arrows show porous silicon layers.

notable property of the surface is that it is covered with a layer with a thickness of about 15 μm, as shown in Figure 7(b). The layer luminesced under UV irradiation, indicating that the surface is covered with a so-called microporous silicon layer [10]. It is thought that a thin microporous silicon layer was formed on the wall surface of the groove formed in 15 M HF solution because it weakly luminesced under UV irradiation. Formation of the microporous porous silicon layer was prevented by processing at lower voltages. However, the grooving speed was also lowered, as mentioned before. Hence, we processed at 2.25 V vs Ag/AgCl in this study unless otherwise stated.

*Effect of pressure applied to the Si/Pt interface*

In the results so far explained, Pt wires were pressed to a Si wafer by the gravity of the Teflon jig of about 20 g. Therefore, the Si/Pt interface received pressure from the gravity of the jig. The effect of the pressure on grooving rate was investigated by using four different jigs with gravities of about 20, 60, 95, and 135 g at an anodic potential of 2.25 V vs Ag/AgCl in 15 M HF solution for 1 h. The pressure was estimated from the effective contact area of the interface, i.e., the diameter of the Pt wires × the thickness of the Si wafer. The grooving rate increased with increase in pressure and reached about 3,200 μm $h^{-1}$ under a pressure of $54 \times 10^4$ g $cm^{-2}$, as shown in Figure 8.

By using Pr-Ir alloy wires, which are mechanically stronger than Pt wires, with a diameter of 30 μm, the highest grooving rate of 4,550 μm $h^{-1}$ was achieved at 4 V vs Ag/AgCl in 15 M HF solutions. However, at this potential, the wires were broken in about 60 min because the wires (Pt-Ir or Pt) gradually dissolved into the HF solution.

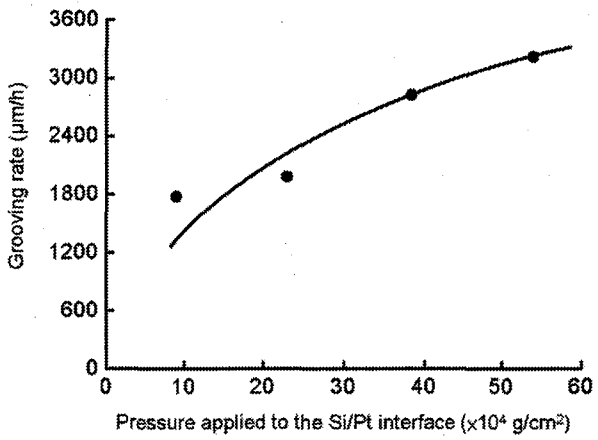


Figure 8. Relationship between rate of grooving in 250-μm-thick Si wafers and pressure applied to the Si/Pt interface. The grooves were formed using Pt wires (φ, 50 μm) to which 2.25 V vs Ag/AgCl was applied in 15 M HF solution.

The current flow during the grooving process increased with pressure applied to the Si/Pt interface, as shown in Figure 9. We speculate that a thin microporous layer, which was formed on the Si surface during grooving, was destroyed under high pressure. If this is the case, the high pressure will lead to increased grooving rate because the microporous silicon layer impedes the anodic dissolution of silicon due to its high electric resistivity.

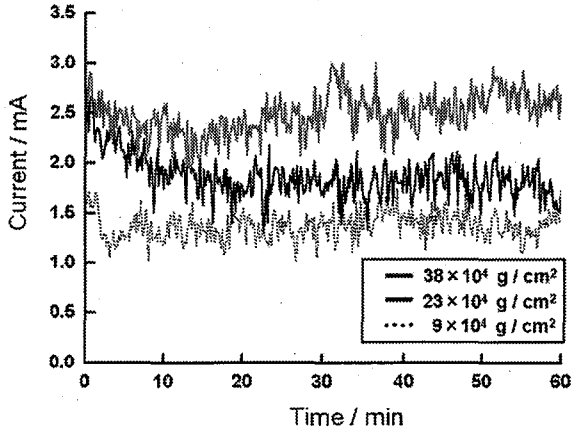


Figure 9. Anodic currents observed during electrochemical grooving in 250-μm-thick Si wafers using Pt wires (φ, 50 μm) to which 2.25 V vs Ag/AgCl was applied in 15 M HF solution with application of different pressures to the Si/Pt interface: (a) 9 , (b) 23 , and (c) $38 \times 10^4$ g $cm^{-2}$.

## 5.4 Conclusions

Optimal conditions for grooving in Si wafers by an electrochemical method were studied. It was found that the grooving rate and morphologies of grooves generated in Si were strongly depended on HF concentration and anodic potentials applied to Pt wires. Anodic potentials applied to Pt wires around 2 V vs Ag/AgCl and a HF solution with concentration of 15 M were suitable for grooving in Si. The grooving rate was also significantly increased by temperature of HF solution and the pressure applied to the Si/Pt interface. By applying appropriate pressure at the Si/Pt interface, grooving at a speed of about 3 mm $h^{-1}$ was achieved in 15 M HF solution. Although the grooving rate in this method is a problem, this method may be used to cutting small pieces from Si wafers. We think that the electrochemical method can also be used for making grooves in other semiconductor devices.

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# *CHAPTER 6*

*Electrochemical Method for Slicing Si Blocks into Wafers*

*Using Platinum Wire Electrodes*

# Chapter 6

# Electrochemical method for slicing Si blocks into wafers using platinum wire electrodes

## 6.1 Introduction

In recent years, shortage of silicon feedstock is one of the greatest obstacles to the spread of photovoltaic cells. As described in previous chapters, multi-wire slicing is the most popular technique to slice silicon ingots [1-3]. The multi-wire slicing has a limit to reducing the wire diameter due to the limit of pulling strength of the wire. Therefore, the reduction in kerf loss is difficult. Normally, kerf loss is as large as 150 μm when Si wafers are produced by the multi-wire slicing method. Moreover, mechanical damage arises on the surfaces of the sliced wafers during slicing and must be removed in a post process. Recently, reduction in both kerf loss and wafer thickness below 100 μm is required. However, achievement of these targets by the multi-wire slicing is thought to be difficult.

In chapter 2, we reported that micropores perpendicular to the surface are formed in Si by wet etching using aggregated Au particles as catalysts in aqueous HF solutions containing $H_2O_2$ as an oxidant [4]. In these processes, silicon is oxidized by using the oxidation power of $H_2O_2$ at sites where the metallic catalysts are in contact, and then the oxidized silicon dissolves in the HF solution.

As a totally different approach to slicing silicon, we applied this phenomenon for grooving silicon by using catalytic wire electrodes [5, 6], with anodic potentials applied to the catalytic wire electrodes instead of using chemical oxidants such as $H_2O_2$. In chapter 4, groove formation in Si wafers by an electrochemical process using varied kinds of catalytic wires of

50 μm was described. By this method, grooves with a width of about 55 μm were formed at the edge of a 250-μm-thick single crystalline Si wafer. It was found that Pt wires were the most suitable for grooving Si wafers. In chapter 5, optimal conditions for grooving in Si wafers by the electrochemical method were investigated. The grooving rate and morphologies of grooves generated in Si were strongly depended on HF concentration and anodic potentials applied to Pt wires. We also found that the grooving rate was also significantly increased by temperature of HF solution and the pressure applied to the Si/Pt interface.

For application of this electrochemical process to the slicing technology, the size of samples must be increased. In this chapter, therefore, to determine its applicability to slicing silicon blocks or ingots, we try to slice Si blocks with a size of $1 \times 1 \times 2$ $cm^3$ (W × H × L) by the electrochemical method. We utilize the optimal conditions, which are obtained from the results described in chapter 4 and chapter 5.

## 6.2 Experimental

In this work, poly-crystalline Si blocks with a size of $1 \times 1 \times 2$ $cm^3$ (W × H × L) were used as samples, as shown in Figure 1. The Si blocks were purchased from Furuuchi Corporation. Prior

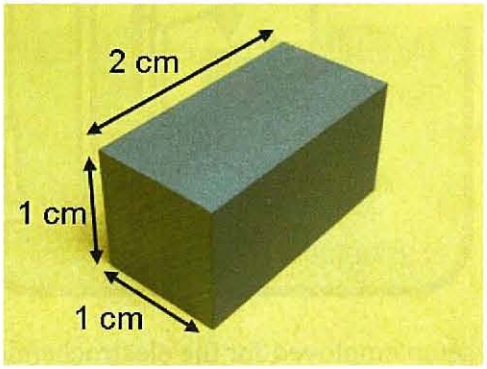


Figure 1. A photo of a poly-crystalline Si block purchased from Furuuchi Corporation.

to the grooving experiment, the samples were cleaned by immersing them in a solution of $H_2O_2$ and $H_2SO_4$ (30% $H_2O_2$ : 97% $H_2SO_4$=1:4 in volume) for 10 min followed by rinsing with ultrapure water (UPW, $>18$ MΩ cm) for 10 min.

Pt wires of 50 μm in diameter, which were purchased from Nilaco Corporation, were used as the catalytic wires for slicing Si blocks. Figure 2 shows the experimental setup for grooving a Si block. The setup is almost the same as that used for grooving Si wafers in previous chapters. First, a Si block was mounted in a Teflon holder. The long side of the sample was placed horizontally. Next, two catalytic wires, about 0.7 mm apart from each other, were set on a Teflon jig and brought into contact with the Si sample. The Teflon jig was positioned by using guides (not shown in Figure 1), and the catalytic wires were pressed to the Si wafer by the gravity of the Teflon jig. A special jig was designed for the processing of Si blocks. Normally, the gravity of jigs for electrochemical grooving of Si blocks was 60 g. To increase the slicing speed, the jigs with over 60 g were also utilized in some experiments. An aqueous solution containing HF was then poured into the Teflon beaker. Finally, a positive potential was applied to the catalytic wires using a potentiostat (Hokuto Denko, HSV-100).

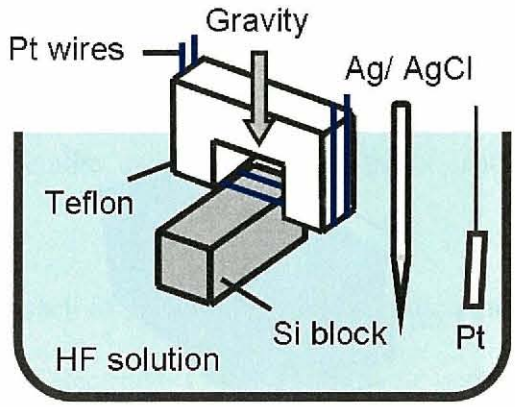


Figure 2. Experimental setup employed for the electrochemical grooving of a Si block.

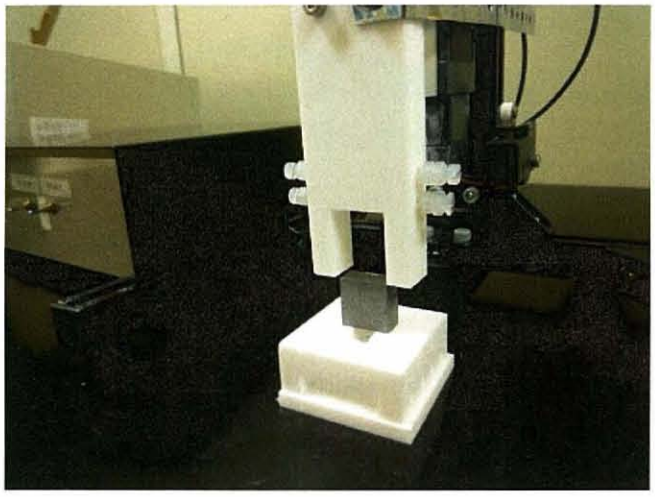

Figure 3. A slicing instrument with a function of vertical motion of Pt wires.

In this work, we also use a slicing instrument, which was designed by us, as shown in Figure 3. The slicing instrument has a function of vertical motion of Pt wires, the frequency and distance being controlled by a computer program. The motion of Pt wires is expected to improve the exchange of HF solution at the interface between Pt wires and a Si block and also from and to the grooves.

The potentials of the platinum wires were measured against an Ag/AgCl reference electrode (RE), and a platinum plate was used as a counter electrode (CE). All of these processes using the HF solution were carried out in a hood equipped with a scrubber. After the electrochemical process, the morphology of the grooves formed in the Si sample was observed with a scanning electron microscope (SEM, Hitachi S-5000) and a laser scanning microscope (Keyence VK-9710). Auger Electron Spectroscopy (AES, Ulvac-Phi PHI-680) was used to detect the elements after processing.

## 6.3 Results and Discussion

*Grooving of a poly-crystalline Si block using a free-falling system*

On the basis of the results of grooving experiments with single crystalline Si wafers, which were described in chapters 4 and 5, we tried to apply the electrochemical grooving method to slicing Si blocks with a size of $1 \times 1 \times 2$ $cm^3$. Figure 4 shows an image of two grooves formed in a Si block after a slicing process for 6 h using Pt wires of 50 μm in diameter at 2.25 V vs Ag/AgCl in 15 M HF solution. The depth of two grooves was about 1400 μm, indicating that the electrochemical method can be applied to grooving Si blocks.

When the processing time was extended to 48 h, two parallel grooves were formed in the Si block to a depth of about 0.9 cm, as shown in Figure 5. The width of the grooves near the mouth of the grooves was about 53 μm, which is nearly the same as the diameter of the Pt wires, as in the case of grooving Si wafers. This result suggests that the method is useful for slicing Si, especially, in terms of small kerf loss. The slightly crooked grooves as seen in Figure 5 were due to the structure of the jig for guiding Pt wires. This problem can be solved by improving the structure.

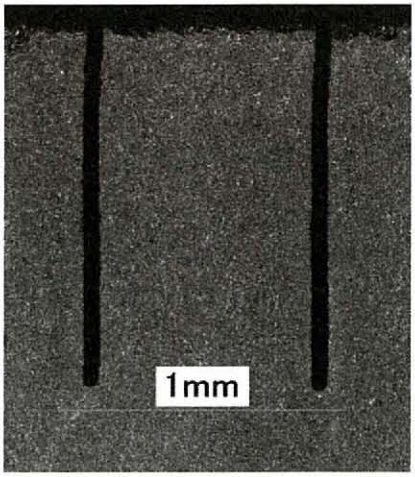


Figure 4. Grooves formed in a poly-crystalline Si block by applying 2.25 V vs Ag/AgCl to Pt wires (φ, 50 μm) for 6 h in 15 M HF solution.

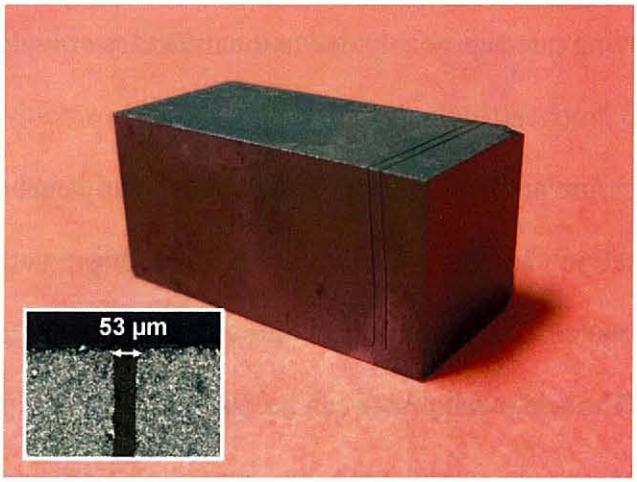


Figure 5. Deep grooves formed in a poly-crystalline Si block by applying 2.25 V vs Ag/AgCl to Pt wires (φ, 50 μm) for 48 h in 15 M HF solution.

The depths of grooves formed after processing for different time periods under the condition of applied voltage of 2.25 V vs Ag/AgCl in 15 M HF solution are shown in Figure 6. The grooving rate seems to be almost constant until the groove reaches a depth of about 1.5 mm. However, the grooving rate became gradually slow when the processing time was over

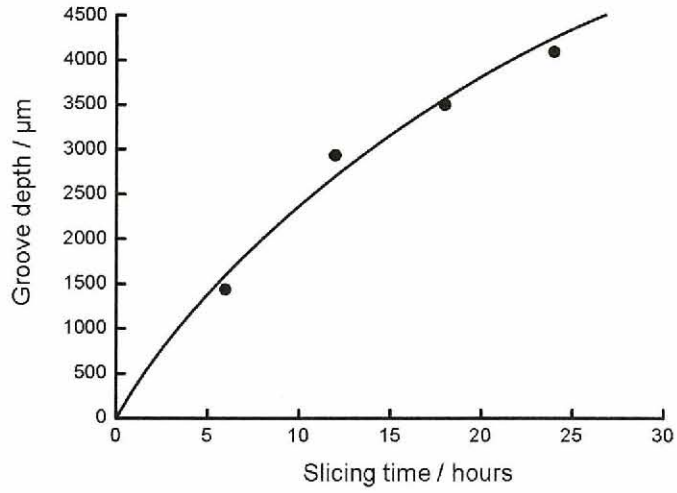


Figure 6. Depth of grooves formed in a poly-crystalline Si block as a function of processing time. Grooves were formed by applying 2.25 V vs Ag/AgCl to Pt wires (φ, 50 μm) in 15 M HF solution.

18 h. The lowered grooving rate is probably due to the difficulty of replacement of the etching solution within the deep grooves.

We found that the pressure applied to the Si/Pt interface greatly enhanced the grooving rate of Si wafers, as described in chapter 5. Therefore, the effect of pressure on the grooving rate of Si blocks was investigated. The experiments were carried out at 2.25 V vs Ag/AgCl in 15 M HF solution for 6 h. The relationship between the grooving rate and pressure was plotted in Figure 7. The grooving rate increased with the increasing pressure applied to the Si/Pt interface. The result was similar to that obtained in Chapter 5. However, the grooving rate became slow as the pressure became high, especially over $1.25 \times 10^4$ g $cm^{-2}$. We speculate that the mass transport of the HF solution to Si/Pt interface is difficult because of very narrow space beneath the Pt wires due to high pressure. A similar phenomenon was observed when the Si surface was etched by using large Au particles as catalysts in a mixture of HF and $H_2O_2$ investigated in Chapter 2. Another feature of grooving in Si blocks is that the grooving rate

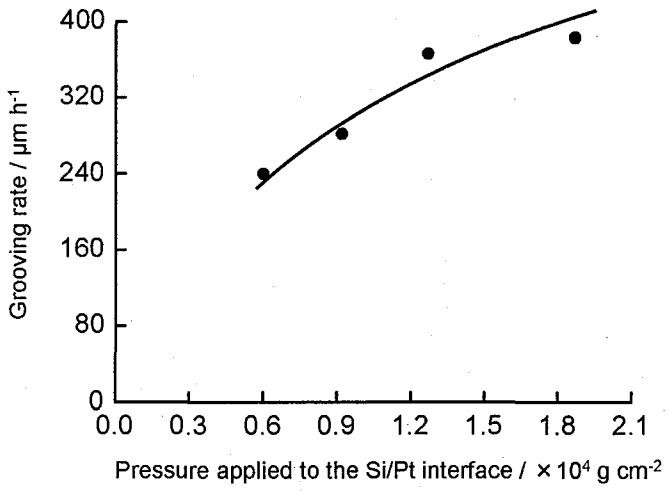


Figure 7. Relationship between grooving rate and pressure applied to the Si/Pt interface. Experiments were carried out at 2.25 V vs Ag/AgCl in 15 M HF solution for 6 h.

for the blocks was much lower than that for wafers. The initial grooving rate seen in Figure 7 is about 240 μm $h^{-1}$, which was only about 1/10 of the rate observed for the wafers in chapter 5. The pressure applied to the Si/Pt interface of the block was about $6\times10^3$ g $cm^{-2}$, which was about 1/50 of the pressure applied to the Si/Pt interface of Si wafers. The low pressure is probably the reason for the slow grooving rate. It was difficult to apply pressure higher than $2\times10^4$ g $cm^{-2}$ to the interface of 1-cm-long Si blocks because the Pt wires (or Pt-Ir wires) could not withstand the weight.

*Grooving of a poly-crystalline Si block by an instrument with a function of vertical motion of Pt wires*

In order to improve the exchange of HF solution at the Si/Pt interface and in the grooves, an instrument was designed, which had a function of vertical motion of Pt wires. Because the movement of Pt wires was automatically controlled by a program, the motion of Pt wires was set before grooving experiments. Figure 8 shows an example of the programmed movement of Pt wires. The Pt wires were set to move upward and then downward in every 2 min. When the Pt wires moved downward, the Pt wires exceeded their original position about 4 μm. As a

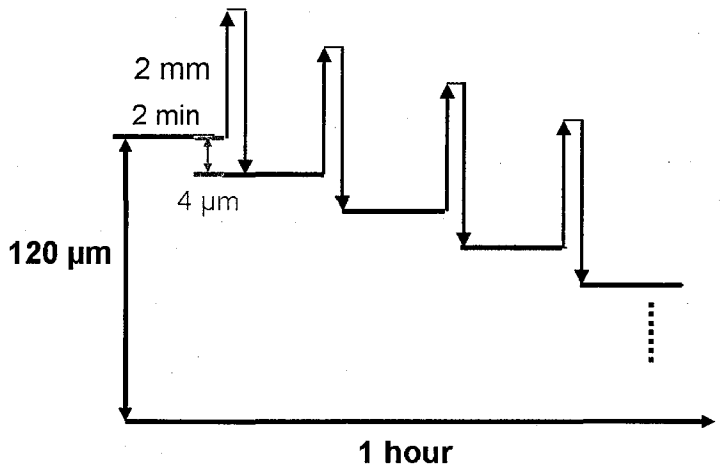


Figure 8. Movement of Pt wires controlled by a computer program.

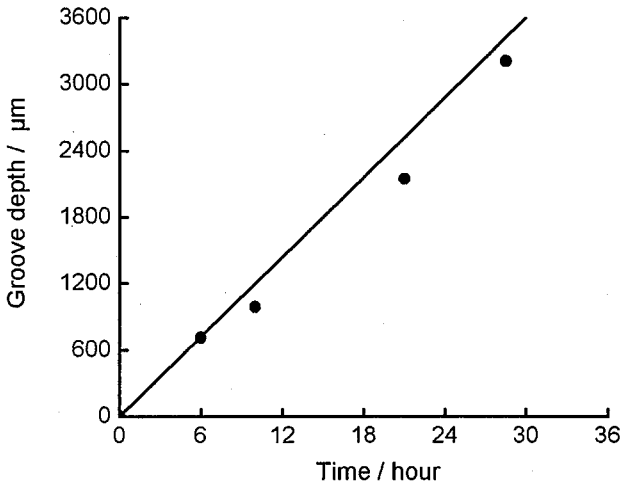


Figure 9. Relationship between depth of grooves and processing time. Grooves were formed in a poly-crystalline Si block by applying 2.25 V vs Ag/AgCl to 50-μm Pt wires in 15 M HF solution. The straight line represents the moving rate of Pt wires.

result , the moving rate of Pt wires toward the Si block was estimated about 120 μm/h. After the setting, grooving experiments were carried out by applying 2.25 V vs Ag/AgCl to Pt wires in 15 M HF solution. When a grooving experiment was carried out for 6 h, the 710 μm deep grooves were formed in a Si block. The relationship between the groove depth and the processing time is shown in Figure 9. The straight line and solid dots represented the moving rate of Pt wires controlled by the program and the groove depth formed in a Si block after processing, respectively. The grooving rate nearly agreed with the moving rate of Pt wires. The results show that the movement of Pt wires is effective to exchange HF solution at the Si/Pt interface and in the grooves. However, we found that the movement of Pt wires is not uniform, as discussed later. The non-uniform movement of Pt wires inhibited the increase of the grooving rate.

We tried to make a silicon wafer from the Si block by processing for longer time period under the conditions used in the experiment, as shown in Figure 9. Figure 10(a) shows a

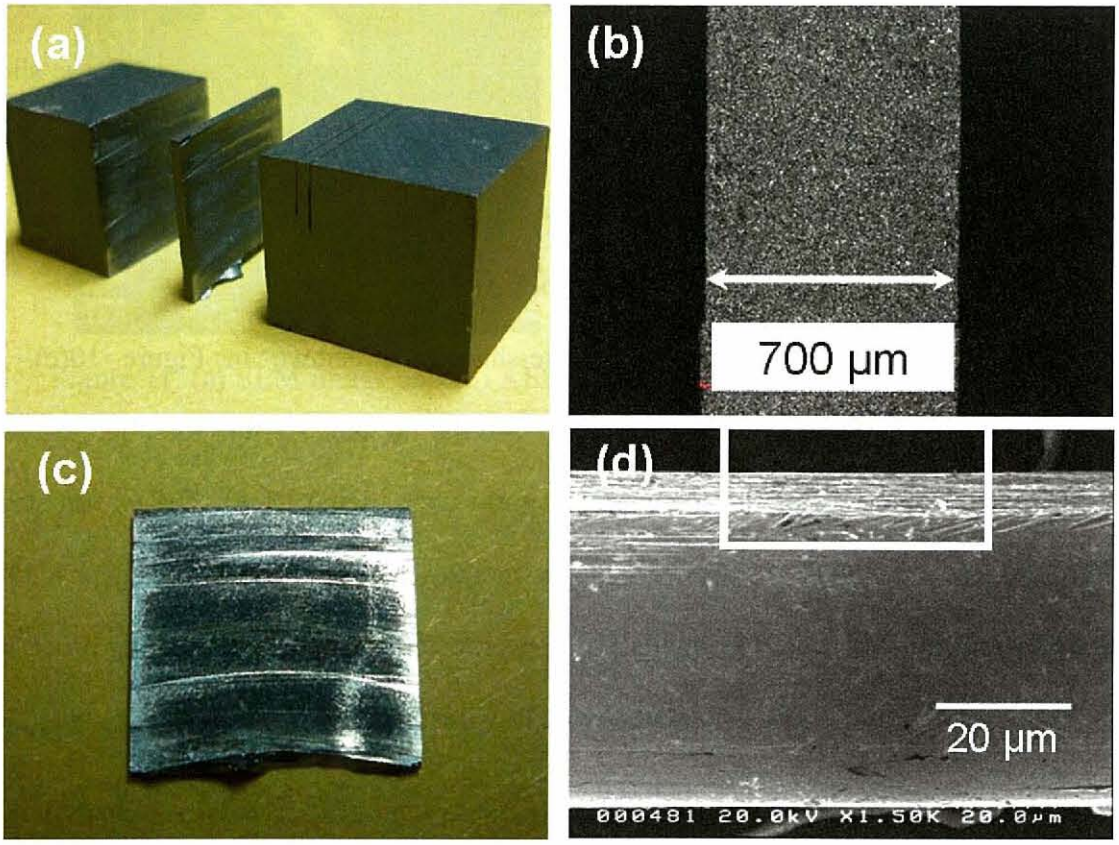


Figure 10. (a) A Si wafer produced electrochemically using Pt wires (φ, 50 μm) to which 2.25 V vs Ag/AgCl was applied in 15 M HF solution for 120 h. (b) A side-view image of the sliced wafer, taken by laser scanning microscope. (c) A photograph of sliced wafer surface. (d) A SEM image of Pt wires after a grooving experiment.

photograph of the silicon wafer we obtained after processing for 120 h. The results indicate that the method can be applied to slicing silicon ingots, if the long processing time is not a problem. However, the slicing speed is far from the practical level. However, to improve the slicing speed, we must develop machine mechanisms for increasing the pressure at the Si/Pt interface and for further assisting the replacement of solution in the grooves. The thickness of sliced wafer was about 700 μm shown in Figure 10(b), which was the same as the distance

between two catalytic wires before processing, as described in the experimental section. Compared to Figure 5, the problem of crooked grooves was greatly improved by the slicing system. A sliced wafer with a thinner thickness below 200 μm may be possibly produced only by shortening the interval of Pt wires. It is possible to make many thin Si wafers at one time by the electrochemical method using many Pt wires, which are placed in parallel.

The surface of sliced Si wafer was wave-shaped, as shown in Figure 10(c). The morphology of wave-shaped texture was very similar to that of the so-called waviness unavoidably formed on wafer surface by using multi-wire slicing [7, 8]. The waved surface structure suggests that the Pt wires did not move smoothly probably because the gaps between the Pt wires and grooves were too small. The appearance of Pt wires after slicing process for 120 h is shown in Figure 10(d). The diameter of Pt wires was still about 50 μm, but the shape was deformed to some extent. As marked in rectangular frame, the part of Pt wires was flattened and micrometer-sized notches were formed on the flattened surface. The flattened surface and notches may result from the mechanical friction occurred between silicon walls and Pt wires during the processing. These phenomena may partly be due to dissolution of Pt wires in an amount in the HF solution.

The sliced surface of the sample shown in Figure 10(c) was further analyzed by SEM and AES. It was found that some micrometer-sized masses existed on the surface, as shown in Figure 11(a). From the AES analysis, as shown in Figure 11(b), the masses were found to be Pt. They deposited on the surface probably as a result of friction or dissolution of Pt, as described above. This problem may be solved by using mechanically and chemically more robust wires such as Ir alloy wires instead of Pt wires.

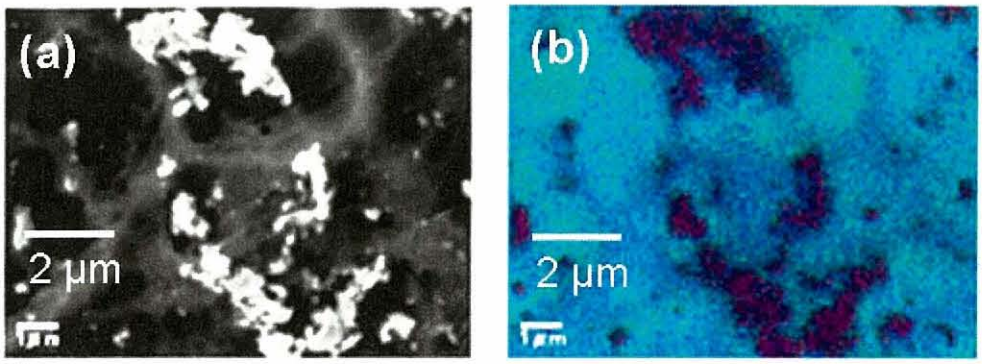


Figure 11. (a) SEM image and (b) AES image (Pt) of the sliced wafer, which is shown in Figure 10(c).

### 6.4 Conclusions

On the basis of the results for optimizing conditions for grooving Si, as described in chapters 4 and 5, silicon blocks were sliced into wafers. A 700 μm thick wafer was fabricated by the electrochemical method. Although it was not experimentally confirmed, production of very thin wafers is possible by shortening the distance between Pt wires. Kerf loss by slicing silicon blocks can be reduced to a level of 50 μm, which is much smaller than that by the conventional multi-wire slicing method. However, the slow slicing speed in this method is a problem that needs to be solved. The present method may be applicable to slicing or cutting technology for small Si pieces. On the other hand, its application to practical technology for slicing silicon ingots seems to be very difficult unless methods are established for applying appropriate pressure to the Si/Pt interface and for exchanging solutions in the grooves.

**Acknowledgements**

We are thankful to Mr. Saito (MST) for the measurements of SEM and AES, which are shown in Figure 11.

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# *CHAPTER 7*

*General Conclusions*

## 7.1 General Conclusions

This thesis deals with chemical methods for making micrometer-sized pores in Si and an electrochemical method for grooving Si. In both processes, metallic catalysts are used to induce hole injection into Si through the Si/metal interface, resulting in the oxidative dissolution of Si in a solution containing HF. The pores formed in Si are filled with Cu by electrodeposition to make interconnects in Si. The groove formation process is applied to slicing Si blocks to make Si wafers using Pt wires as the catalytic electrodes. The main findings obtained through this work are summarized as follows:

**Chapter 2:**

Fabrication of micrometer-sized pores in Si(100) wafers was studied using micrometer-sized metal particles as catalysts in HF solution. The mechanism of pore formation by the metal-assisted etching was discussed on the basis of the morphologies of the pores formed in Si after the wet process. The formation of pores includes various elementary steps, *e.g.*, reduction of $H_2O_2$ on metal catalysts, injection of electrons from Si to metal catalysts, and oxidative dissolution of Si with positive holes and HF. The pore formation and the morphologies of the pores are affected not only by the size and numbers of the particles but also by the concentration of etching solutions. Spherical Au microspheres are promising candidates of the catalysts for making straight pores with micrometer-sized diameters. They can be used in the forms of isolated particles and relatively large aggregates (>10 particles). The pore size can be controlled by the number of the particles forming the aggregates.

**Chapter 3:**

Large vertical pores with a diameter of about 5 μm were fabricated using aggregated Au particles on the basis of the wet etching process as described in Chapter 2. Au particles, which had been used as catalysts for pore formation, at the bottom of the pores were used as seeds for the bottom-up Cu filling. Cu was electrochemically deposited in the 100-μm-deep pores from a solution containing 0.1 M $CuSO_4$ and 1.8 M $H_2SO_4$. The optimal cathodic potential for the deposition of Cu in the pores was about -0.275 V vs Ag/AgCl. By continuing the deposition of 16 h, whole pores were filled with Cu completely. On the other hand, in the absence of Au aggregates as seeds, the pores could not be filled with Cu; fine Cu particles were randomly deposited on the wall of the pore and bottlenecking occurred in the upper part of pores.

**Chapter 4:**

In this chapter, the electrochemical grooving of Si wafers using catalytic wire electrodes is reported. The grooves formed in Si were significantly affected by the kind of metal wires used as catalysts. The grooving rate was also greatly affected by the diameter of the metal wires: it became faster as the diameter decreased. By using Pt wires with a diameter of 50 μm, grooves with a width of about 55 μm were formed. This result suggests that the kerf loss of Si can drastically be decreased by using the electrochemical method.

**Chapter 5:**

In this chapter, we studied some experimental conditions, such as anodic potentials applied to the Pt wires, temperature of HF solution, and HF concentration, in terms of the grooving rate of Si. Because the anodic dissolution of Si occurs at the Si/Pt interface, effect of pressure

applied to the Si/Pt interface was investigated as well. The results showed that the grooving rate and morphologies of grooves generated in Si were strongly depended on HF concentration and anodic potentials applied to Pt wires. Anodic potential of about 2 V vs Ag/AgCl and HF concentration of about 15 M were found to be suitable for grooving Si. The grooving rate was significantly increased by elevating the temperature of HF solution and increasing the pressure at the Si/Pt interface.

**Chapter 6:**

Based on the results of grooving experiments with single crystalline Si wafers, which are described in Chapters 4 and 5, we tried to apply the electrochemical grooving method to slicing Si blocks with a size of 1 x 1 x 2 $cm^3$. By using the electrochemical method, a Si wafer was fabricated from a Si block. The kerf loss was about 50 μm, which was much smaller than that of the conventional multi-wire slicing method. Although the slow slicing speed of this method is slow, this method may be used as slicing and cutting technologies for small Si devices.

# *List of Publications*

1. "Formation of 100 μm Deep Vertical Pores in Si Wafers by Wet Etching and Cu Electrodeposition"
   Chia-Lung Lee, Shinsuke Tsuru, Yuji Kanda, Shigeru Ikeda and Michio Matsumura
   *Journal of The Electrochemical Society*, **156**, 543-547 (2009).

2. "Electrochemical Grooving of Si Wafers Using Catalytic Wire Electrodes in HF solution"
   Chia-Lung Lee, Yuji Kanda, Takeshi Hirai, Shigeru Ikeda and Michio Matsumura
   *Journal of The Electrochemical Society*, **156**, H 134-137 (2009).

3. "Pore Formation in Silicon by Wet Etching Using Micrometer-sized Metal Particles as Catalysts"
   Chia-Lung Lee, Kazuya Tsujino, Yuji Kanda, Shigeru Ikeda and Michio Matsumura
   *Journal of Materials Chemistry*, **18**, 1015-1020, (2008).

*The papers not included in the thesis:*

1. "Acceleration of Groove Formation in Silicon Using Catalytic Wire Electrodes for Development of a Slicing Technique"
   Mohamed Shaker Salem, Chia-Lung Lee, Shigeru Ikeda and Michio Matsumura
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