Low-Voltage and Small-Area Design and Implementation of Narrowband and Wideband CMOS Low-Noise Amplifiers
（狭帯域・広帯域CMOS低雑音増幅器の低電圧化および小面積化に関する研究）

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Abstract

This dissertation addressed low-voltage and small-area design and implementation of narrowband and wideband CMOS low-noise amplifiers (LNAs). It was organized into five chapters and two appendixes. The summaries of each chapter were as follows:

Chapter 1

A background for this work and fundamentals of LNAs were described.

Chapter 2

A 1.0 V, 5 GHz two-stage CMOS LNA with inductive source degeneration was demonstrated. Its design methodology based on analytical expressions was also presented. The two-stage topology consisting of common-source and common-gate stages was more suitable for low-voltage operation than a conventional cascode topology. The complete analytical expressions of the LNA performance were first derived from the small-signal equivalent circuits. The LNA fabricated in a 0.15 μm fully-depleted silicon-on-insulator (FD-SOI) CMOS process occupied 0.25 mm^2 and achieved an S_{11} of less than -10 dB, NF of 1.7 dB, voltage gain of 23 dB, and IIP_3 of -6.1 dBm at 5.4 GHz with a power consumption of 8.3 mW. These measurements were consistent with calculations obtained from the derived analytical expressions.

Chapter 3

A 0.5 V, 5 GHz transformer folded-cascode CMOS LNA was demonstrated. The chip area of a conventional folded-cascode LNA was reduced by partially coupling the internal inductor with the load inductor. The effects of the magnetic coupling between these inductors on the LNA performance were also analyzed. The LNA fabricated in a 90 nm digital CMOS process achieved an S_{11} of -14 dB, NF of 3.9 dB, and voltage gain of 16.8 dB at 4.7 GHz with a power consumption of 1.0 mW. The chip area of the presented LNA was 25% (0.21 mm^2) smaller than that of the conventional folded-cascode LNA (0.29 mm^2).

Chapter 4

A 1.0 V, 3.1–10.6 GHz transformer noise-canceling CMOS LNA based on a common-gate topology was demonstrated. The transformer consisting of the input and shunt-peaking inductors partly canceled the noise originating from the common-gate transistor and load resistor. The combination of the transformer with the output series inductor provided wideband input impedance matching. The LNA designed for ultra-wideband (UWB) applications was fabricated in a 90 nm digital CMOS process. It achieved an S_{11} of less than -10 dB, NF of less than 4.4 dB, and S_{21} of more than 9.3 dB with a power consumption of 2.5 mW and occupied the smallest chip area (0.12 mm^2) among previously reported 3.1–10.6 GHz CMOS LNAs.

Chapter 5

The achievements obtained in this work were summarized and this dissertation was concluded.

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Chapter 1

Introduction

1.1 Background

The high-frequency performance of metal-oxide semiconductor field-effect transistors (MOSFETs) has improved rapidly, due to advances in complementary metal-oxide-semiconductor (CMOS) process technologies [1]. This allows us to implement radio-frequency integrated circuits (RFICs) for the front-ends of wireless transceivers by using Si CMOS technologies. The Si CMOS technology has two advantages over SiGe or III-V compound semiconductor technologies, conventionally used for RFICs. First, the CMOS technology costs lower than the others, due to fewer masks layers and processing steps. For example, a 0.13 μm CMOS process costs approximately 20% lower than a 0.13 μm SiGe BiCMOS process [1, 2]. Second, the CMOS technology allows high integration of RF circuits with digital circuits on one chip, called system-on-a-chip (SoC), which can achieve higher performance and lower chip cost [3, 4]. Thus, CMOS implementation of RFICs is indispensable for creating low-cost and high performance wireless communication devices.

However, the scaling of MOSFETs has imposed two stringent requirements on CMOS RFICs.

One is low-voltage operation. As MOSFETs scale down, the allowable supply voltages of ICs decrease to maintain the device reliability. Reference [5] predicts that the supply voltage of low-power digital ICs will decrease to 0.5 V in 2016. Considering the integration with digital circuits, we need to design RF circuits that can operate at the same supply voltage. Most existing RF circuits, which require more than 1.0 V supplies, can not operate under such a low supply voltage. Low-voltage circuit topologies are becoming more important.

The other is small chip area or low cost. The CMOS fabrication cost has been increasing dramatically with the scaling of MOSFETs. Reference [6] shows that a 45 nm (state-of-the-art) CMOS process costs approximately 10 times as much as a 0.13 μm (most widely used) CMOS process. The chip cost of ICs mainly depends on the chip area. The chip area of digital circuits, which mostly consist of transistors, decreases as CMOS processes scale down, and consequently the chip cost does not increase dramatically. On the other hand, the chip area of RFICs remains almost constant even with the scaling of CMOS processes, because RF circuits require many pas-

sive components such as inductors, capacitors, and transmission lines. They shrink very slowly compared to transistors. Thus, the small-area implementation of RF circuits is another important consideration when using state-of-the-art CMOS technologies.

The goal of this research is to propose and demonstrate low-voltage (1.0 V or less) and small-area (0.25 mm^2 or less) CMOS low-noise amplifiers (LNAs) for narrowband (5 GHz) and wideband (3.1–10.6 GHz) wireless receivers. Narrowband receivers, which have input bandwidths of less than 1 GHz, are employed in cellular phones, global positioning systems (GPS), Bluetooth systems, and wireless local area network (WLAN) systems, etc. On the other hand, wideband receivers are mainly used in ultra-wideband (UWB) systems and can be applied to multiband/multistandard systems. LNAs are essential building blocks for all wireless receivers, while they require relatively high supply voltages and large chip area (i.e., many inductors). This causes the difficulties for creating low-voltage and small-area receiver chips. In addition, the circuit topologies of narrowband LNAs are quite different from those of wideband ones, which means that different topologies suitable for each receiver are required. Low-voltage, small-area and narrowband/wideband CMOS LNAs can therefore contribute to low-voltage and low-cost wireless receivers.

1.2 Fundamentals of Low-Noise Amplifiers

1.2.1 Low-Noise Amplifier

The LNA is the first building block of RF front-ends for wireless receivers. Figure 1.1 shows a block diagram of a typical wireless receiver. The RF front-end, which consists of an LNA, mixer, local oscillator (LO), low-pass filter (LPF), and variable gain amplifier (VGA), amplifies and converts high-frequency signals into low-frequency ones with the desired signal-to-noise ratio (SNR). First, the LNA amplifies signals received by an antenna. Second, the mixer downconverts the high-frequency signals to low-frequency ones by using the LO and then the LPF filters out unwanted high-frequency components in the signals. Finally, the VGA adjusts the signal levels

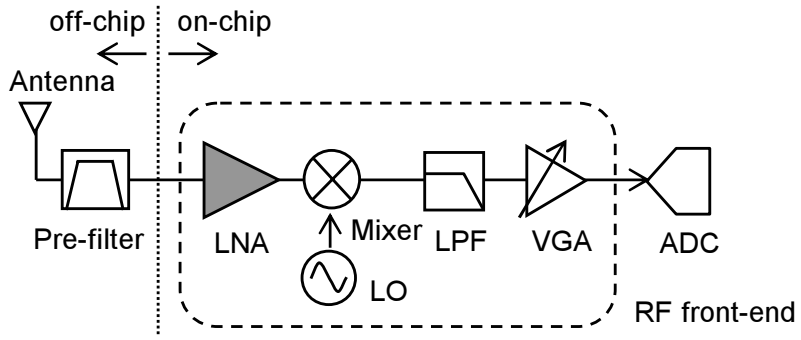

Figure 1.1: Block diagram of a typical wireless receiver.

for an analog-to-digital converter (ADC). The RF front-end is usually integrated on one chip.

The LNA determines the input bandwidth and noise performance of the wireless receiver and must meet the following requirements:

- Input impedance matching — The input impedance of the LNA is set to the characteristic impedance of the transmission line (i.e., $Z_0 = 50\ \Omega$) for a small input reflection coefficient and maximum power transfer.
- Sufficient gain — The LNA gain must be large enough to reduce the noise contributions from the following building blocks (mixer, LPF, and VGA) to the receiver.
- Low noise performance — The noise performance of the receiver is mainly determined by that of the LNA.
- High linearity — The maximum achievable linearity of the receiver is limited by the linearity of the LNA.
- Stability — The LNA oscillates when it has a negative input or output resistance.

1.2.2 Performance Metrics

LNA performance metrics for input impedance matching, noise, gain, and linearity are described in terms of an LNA with a buffer with a 50 Ω output impedance, as shown in Fig. 1.2. RF devices are generally terminated with a resistance R_L of 50 Ω, and then measured using a signal source with a resistance R_s of 50 Ω. However, the output impedances of LNAs are not designed to 50 Ω but to be high, because the LNAs need to drive capacitive inputs of on-chip mixers or additional amplifiers. This means that, in the measurement of stand-alone LNAs, the 50 Ω termination causes inaccurate measurements, in particular, lower gain measurements. For accurate measurements of LNA performance, the LNAs are usually integrated together with buffers, whose input impedances are capacitive, emulating the practical termination. In addition, the buffers have 50 Ω

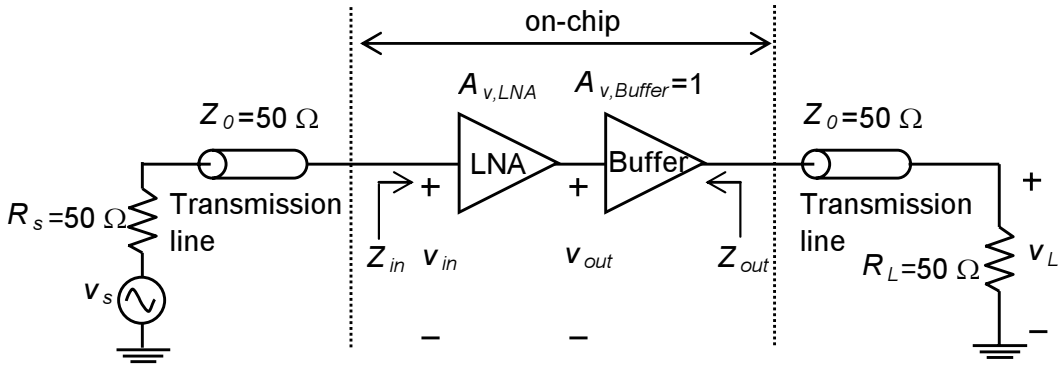

Figure 1.2: LNA cascaded with a buffer for measurement.

output impedances, providing output impedance matching. The effects of the buffers on the LNA performance can be ignored or de-embedded, as will be shown below.

Input Impedance Matching

The quality of input impedance matching is evaluated by the input reflection coefficient S_{11}, given by [7]

$$S_{11} = \frac{Z_{in} - R_s}{Z_{in} + R_s}, \tag{1.1}$$

where Z_{in} is the input impedance of the LNA. Equation (1.1) indicates that the buffer has little impact on S_{11}. Figure 1.3 shows the frequency characteristic of S_{11} for $Z_{in} = R + sL + 1/sC$, which represents the input impedance of a typical narrowband LNA. An S_{11} of less than -10 dB is generally required for input impedance matching and the frequency range is called the input bandwidth.

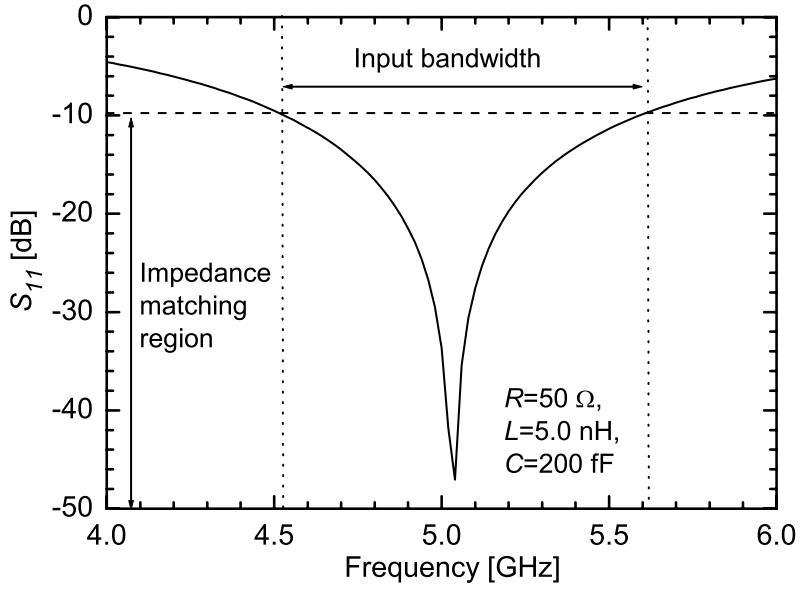

Figure 1.3: Calculated S_{11} for $Z_{in} = R + sL + 1/sC$.

Gain

The LNA gain is measured as the forward transmission coefficient S_{21} [7]. The voltage gain of the LNA is defined as the ratio of the output voltage v_{out} to the input one v_{in}:

$$A_v \equiv \frac{v_{out}}{v_{in}}. \tag{1.2}$$

When the LNA is followed by a unity-gain buffer with $Z_{out} = R_L$ as shown in Fig. 1.2, S_{21} can be expressed as

$$S_{21} = \frac{v_L}{v_s/2} = 2\frac{v_{out}}{v_s}, \tag{1.3}$$

where v_s represents the signal voltage and v_L the output voltage at R_L. The input voltage of the LNA is given by

$$v_{in} = \frac{Z_{in}}{R_s + Z_{in}} v_s. \tag{1.4}$$

Substituting Eq. (1.4) into Eq. (1.3), we obtain

$$S_{21} = \frac{2Z_{in}}{R_s + Z_{in}} \frac{v_{out}}{v_{in}} = \frac{2Z_{in}}{R_s + Z_{in}} A_v, \tag{1.5}$$

which corresponds to A_v for $Z_{in} = R_s$. This means that, under input impedance matching condition, the S_{21} of the LNA with the unity-gain buffer equals the voltage gain of the stand-alone LNA.

Noise Figure

The noise performance of the LNA is evaluated by the noise figure (NF), defined as $10 \log_{10} F$, where F is the ratio of the input SNR_{IN} to the output SNR_{OUT} [8]:

$$F \equiv \frac{SNR_{IN}}{SNR_{OUT}}. \tag{1.6}$$

Equation (1.6) indicates that NF is a measure of the degradation of the SNR. By introducing the total output noise power $P_{n,OUT}$ and the output noise power due to the source, P_{n,OUT,R_s}, we can express Eq. (1.6) as

$$F = \frac{P_{n,OUT}}{P_{n,OUT,R_s}}, \tag{1.7}$$

which allows the NF calculations of the LNA.

The overall F of a cascaded system (i.e., receiver or LNA with a buffer) is given by the Friis formula [9]:

$$F_{all} = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_p}, \tag{1.8}$$

where F_1 and F_2 represent the noise factor of the first and second stages, respectively, and G_p the power gain of the first stage. Equation (1.8) indicates that the noise performance of the first stage is critical to the overall noise performance of the cascaded system and the gain of the first stage reduces the noise contribution from the second stage. In the case of wireless receivers, the first stage represents an LNA, and the second stage the other building block consisting of a mixer, filter, and VGA. In the measurement of the LNA with the buffer, the LNA usually has so large gain that the influence of the buffer on NF measurements is small.

Third-Order Intercept Point

The LNA linearity is evaluated by the third-order intercept point (IP_3), measured from a two tone test [10]. The input-output relationship of the LNA can be approximated by

$$v_{out}(t) \approx \alpha_1 v_{in}(t) + \alpha_2 v_{in}^2(t) + \alpha_3 v_{in}^3(t). \tag{1.9}$$

Applying two tones with the same amplitude A ($v_{in}(t) = A\cos\omega_1 t + A\cos\omega_2 t$) to the LNA, we obtain the output voltage as

$$\begin{aligned} v_{out}(t) = &\left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right) A\cos\omega_1 t + \left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right) A\cos\omega_2 t \\ &+ \frac{3}{4}\alpha_3 A^3 \cos\left(2\omega_1 - \omega_2\right) t + \frac{3}{4}\alpha_3 A^3 \cos\left(2\omega_2 - \omega_1\right) t + \cdots. \end{aligned} \tag{1.10}$$

The components at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are called third-order intermodulation (IM_3) products and appear in the vicinity of ω_1 and ω_2 for $\omega_1 \simeq \omega_2$. The fundamental component and IM_3 product are plotted versus the input on a logarithmic scale as shown in Fig. 1.4. The IM_3 products increase with the slope of three, whereas the fundamental components increase with the slope of one. The intersection of the two lines is IP_3, and the horizontal and vertical coordinates of IP_3 are called the input IP_3 (IIP_3) and output IP_3 (OIP_3), respectively. At the IP_3, the fundamental components have the same amplitude as the IM_3 products:

$$|\alpha_1| A_{IIP_3} = \frac{3}{4}|\alpha_3| A_{IIP_3}^3, \tag{1.11}$$

where $9\alpha_3 A^2/4$ is ignored against α_1. The IIP_3 is thus given by

$$A_{IIP_3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}, \tag{1.12}$$

and the OIP_3 is equal to $\alpha_1 A_{IIP3}$. The IIP_3 expressed in power is as follows:

$$P_{IIP_3} = \frac{A_{IIP_3}^2}{2R_s}, \tag{1.13}$$

which we will simply express as IIP_3.

The A_{IIP_3} of a cascaded system is approximated as [10]

$$\frac{1}{A_{IIP_3}^2} \approx \frac{1}{A_{1,IIP_3}^2} + \frac{A_{v1}^2}{A_{2,IIP_3}^2}, \tag{1.14}$$

where A_{1,IIP_3} and A_{2,IIP_3} represent the A_{IIP_3} of the first and second stages, respectively, and A_{v1} the voltage gain of the first stage. Equation (1.14) indicates that the achievable maximum linearity of the cascaded system is limited by the first stage and the nonlinearity of the second stage become significant when the gain of the first stage is large. In the measurement of the LNA with the buffer, the IIP_3 without the effect of the buffer can be calculated from Eq. (1.14).

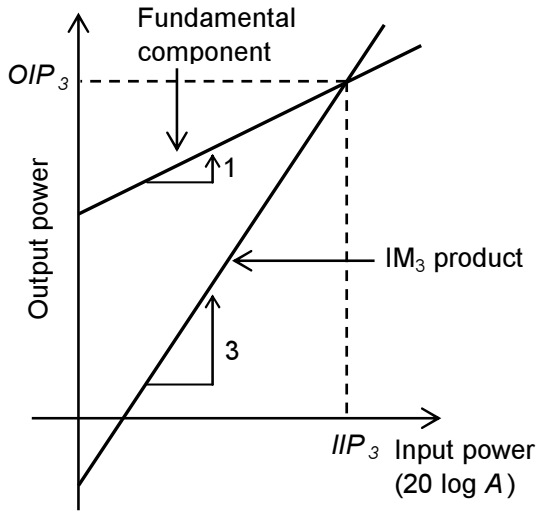

Figure 1.4: Third-order intercept point.

Stability

A two-port network like an LNA oscillates when either the input or output port presents a negative resistance. The two-port is unconditionally stable when it meets the following conditions [7]:

$$|\Gamma_s| < 1, \tag{1.15}$$

$$|\Gamma_L| < 1, \tag{1.16}$$

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1, \tag{1.17}$$

$$|\Gamma_{OUT}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \right| < 1, \tag{1.18}$$

where Γ_s, Γ_{IN}, Γ_L, and Γ_{OUT} represent the source, input, load, and output reflection coefficients, respectively, as show in Fig. 1.5. Equations (1.15)–(1.18) state that the real parts of the input and output impedances must be positive [7]:

$$\text{Re}[Z_{IN}] > 0, \tag{1.19}$$

$$\text{Re}[Z_{OUT}] > 0. \tag{1.20}$$

The unconditional stability of the two-port can be evaluted by other parameters: K and B_1, given by [7]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}, \tag{1.21}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2, \tag{1.22}$$

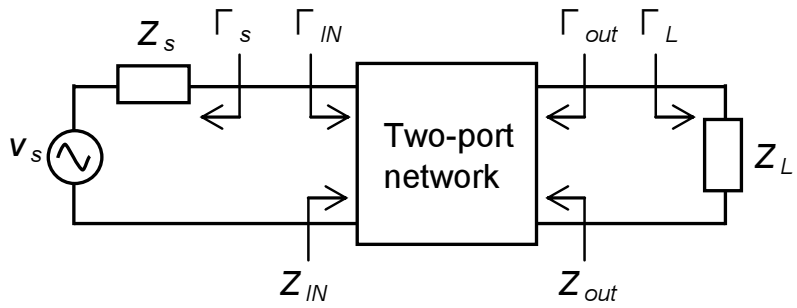

Figure 1.5: Stability of a two-port network.

respectively, where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. The necessary and sufficient conditions for unconditional stability are $K > 1$ and $B_1 > 0$.

1.3 Outline of This Dissertation

This dissertation proposes and demonstrates low-voltage and small-area CMOS LNAs for narrowband and wideband wireless receivers. The dissertation is organized as follows.

Chapter 2 presents a 1.0 V two-stage CMOS LNA with inductive source degeneration for 5 GHz applications. Complete analytical expressions of the LNA performance are derived, and then the design methodology based on the derived expressions are presented.

Chapter 3 presents a 0.5 V, 5 GHz area-efficient transformer folded-cascode CMOS LNA, which consumes much smaller chip area than the two-stage CMOS LNA presented in Chapter 2. The transformer reduces the chip area of a conventional folded-cascode CMOS LNA, but affects the LNA performance. The effects of the transformer are analyzed, and a transformer structure that has a small impact on the LNA performance are presented.

Chapter 4 presents a 1.0 V transformer noise-canceling CMOS LNA for fullband UWB (3.1–10.6 GHz) applications. The transformer partly cancels the noise originating from the transistor and load resistor, thereby improving the LNA noise performance without increased chip area and power consumption. The noise cancellation mechanisms are described and a wideband impedance matching technique is also presented.

Chapter 5 concludes the dissertation.

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Chapter 2

Two-Stage CMOS LNA

2.1 Introduction

Cascode CMOS LNAs with inductive source degeneration [1–3] are widely used for narrowband wireless receivers, such as GPS [4, 5], cellular phone [6–8], and WLAN receivers [9–11]. The cascode LNAs have achieved both good input impedance matching ($|S_{11}| < -10$ dB) and low noise performance ($NF \simeq 2.0$ dB) with reasonable power consumption ($\sim$10 mW), due to many design methodologies [1, 12–17] and advances in CMOS processes. However, the LNAs require relatively high supply voltages ($>$1.0 V) to achieve both good noise and linearity performance.

In addition, the previous design methodologies pay much attention on noise optimization, but little on its linearity. Modern wireless systems, in particular, cellular and WLAN systems impose high linearity requirements on LNAs [18, 19]. Low-voltage circuit topologies and design methodologies considering both noise and linearity are required.

This chapter proposes a two-stage CMOS LNA suitable for low-voltage operation and its design methodology based on the analytical expressions of the gain, noise, and linearity. These expressions are derived from the small-signal equivalent circuits of the LNA. The proposed design methodology is expanded from the previous my work [20], which is applied to the cascode CMOS LNA. The 1.0 V two-stage LNA designed for 5 GHz WLAN applications is implemented in a 0.15 μm fully-depleted silicon-on-insulator (FD-SOI) CMOS technology [21, 22], and both its performance and design methodology are verified.

This chapter is organized as follows. Section 2.2 overviews the conventional cascode CMOS LNA with inductive source degeneration and describes its simple analytical expressions and limitations. Section 2.3 presents the two-stage CMOS LNA and its small-signal equivalent circuit, and then derives the analytical equations of the gain, noise, and linearity. Section 2.4 presents the design methodology based on these equations. Section 2.5 shows the measurement results of the fabricated LNA, and Section 2.6 concludes the chapter.

2.2 Cascode LNA with Inductive Source Degeneration

Figure 2.1 shows the conventional cascode LNA with inductive source degeneration [1–3]. The inductors L_g and L_s are connected to the gate and source terminals of the common-source transistor M_1, providing input impedance matching at an operating frequency. The cascode transistor M_2 reduces the Miller effect due to the gate-drain capacitance of M_1, improving the reverse isolation performance of the LNA. The load inductor L_L resonates with the load parasitic capacitance C_L, providing a high impedance.

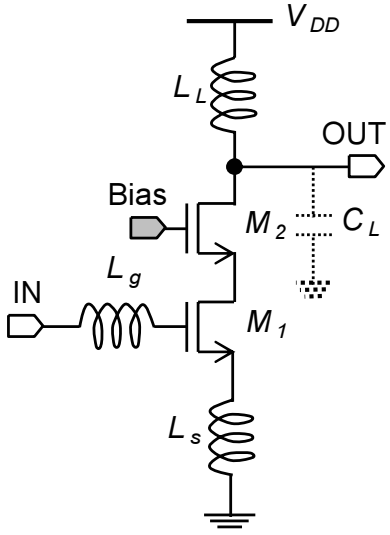

Figure 2.1: Schematic of the cascode LNA with inductive source degeneration.

2.2.1 Analytical Expressions

Analytical expressions of the input impedance, gain, noise, and linearity of the cascode LNA are derived from the small-signal equivalent circuit shown in Fig. 2.2, where the resistors, $1/g_{m2}$ and R_s, represent M_2 and the signal source resistance, respectively.

Input Impedance

The source inductor L_s provides a resistive component for the LNA input impedance Z_{in}, and the gate inductor L_g adjusts the resonance frequency of Z_{in} to the desired operating frequency. The small-signal equivalent circuit shown in Fig. 2.2 gives the input impedance:

$$Z_{in} = \omega_{T_1} L_s + j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs1}}, \tag{2.1}$$

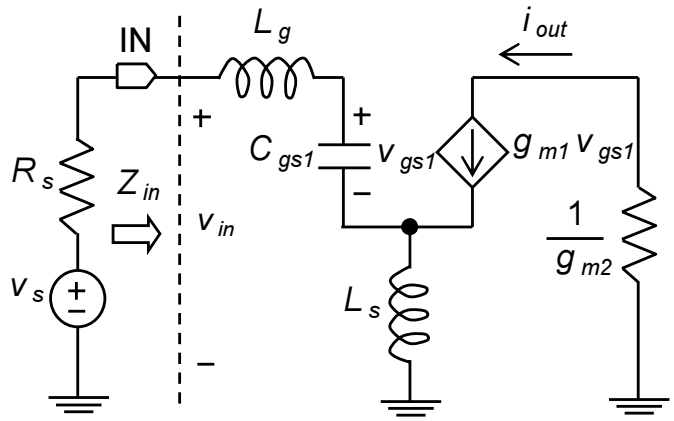

Figure 2.2: Small-signal equivalent circuit of the cascode LNA.

where $\omega_{T_1} = g_{m1}/C_{gs1}$ is the unity current gain frequency of M_1 and g_{m1} and C_{gs1} are the transconductance and gate-source capacitance of M_1, respectively. Selecting L_s such that $L_s = R_s/\omega_{T_1}$ allows input impedance matching around the resonance frequency:

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs1}}}. \tag{2.2}$$

Gain

The voltage gain of the LNA is determined by the equivalent resistance of the load LC tank and ω_{T_1}. The output current i_{out}, given by $g_{m1}v_{gs1}$ where $v_{gs1} = v_{in}/sC_{gs1}Z_{in}$, flows into the load LC tank, and the voltage gain at ω_0 is therefore given by

$$A_v = \left|\frac{v_{out}}{v_{in}}\right| = \left|\frac{i_{out}R_{L_L}}{v_{in}}\right| = \left|\frac{g_{m1}R_{L_L}}{j\omega_0 C_{gs1}Z_{in}}\right| = \frac{g_{m1}R_{L_L}}{\omega_0 C_{gs1}\omega_{T_1}L_s} = \frac{R_{L_L}}{R_s}\left(\frac{\omega_{T_1}}{\omega_0}\right), \tag{2.3}$$

where R_{L_L} is the equivalent resistance of the load LC tank at the resonance frequency of ω_L $(= 1/\sqrt{L_L C_L})$ and is approximated by [23]

$$R_{L_L} \approx \frac{\omega_L^2 L_L^2}{R_{L_L,s}} = Q_{L_L}^2 R_{L_L,s}, \tag{2.4}$$

where Q_{L_L} and $R_{L_L,s}$ are the quality factor and parasitic series resistance of L_L, respectively. The resonance frequency of the load LC tank, ω_L, is generally set to ω_0.

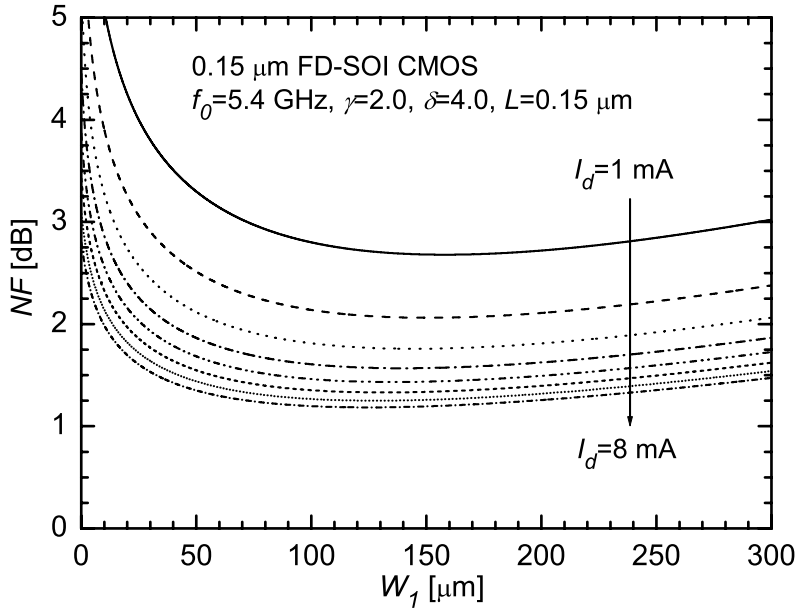

Figure 2.3: Calculated NF versus W_1 with I_d as a parameter.

Noise

The LNA noise performance depends on the gate width of M_1, W_1, for a fixed current consumption. The noise factor of the LNA is given by [1, 15]

$$F = 1 + \frac{\gamma\chi}{\alpha_1} g_{m1} R_s \left(\frac{\omega_0}{\omega_{T_1}}\right)^2 + \frac{\alpha_1 \delta}{\kappa g_{m1} R_s}, \tag{2.5}$$

$$\chi = 1 - 2|c|\alpha_1 \sqrt{\frac{\delta}{\kappa\gamma}} + \frac{\delta\alpha_1^2}{\kappa\gamma}, \tag{2.6}$$

where $\alpha_1 = g_{m1}/g_{d01}$ and g_{d01} is the zero-bias drain conductance of M_1; γ and δ are the drain noise current factor ($\gamma = 2/3$ in long-channel MOSFETs [24, 25], but $\gamma > 2/3$ in short-channel MOSFETs [26]) and the induced gate noise current factor ($\delta = 2\gamma$ [27]), respectively, and c is the correlation coefficient between these noise currents ($c \simeq j0.395$ [24]); κ is the Elmore constant ($\kappa = 5$ [27]). Equations (2.5) and (2.6) provide an optimum g_{m1} or W_1 for noise performance. The calculated NF versus W_1 with the drain current I_d as a parameter is shown in Fig. 2.3, where 0.15 μm FD-SOI CMOS process parameters are used. Increasing I_d leads to a lower NF, and the optimum gate width $W_{1,opt}$ is found for each I_d. The gate width W_1 is generally set to $W_{1,opt}$.

Linearity

The cascode LNA consists of the common-source and cascode transistors, and hence the overall IIP_3 of the LNA can be approximated as that of a cascade system, as shown in Section 1.2.2:

$$\frac{1}{A^2_{LNA,IIP_3}} \approx \frac{1}{A^2_{1,IIP_3}} + \frac{A^2_{v1}}{A^2_{2,IIP_3}}, \tag{2.7}$$

where A_{1,IIP_3} and A_{2,IIP_3} represent the IIP_3 of the common-source and cascode transistors in the expression of the voltage amplitude, respectively; A_{v1} represents the voltage gain of the common-source transistor and is given by

$$A_{v1} = \frac{1}{g_{m2}R_s}\left(\frac{\omega_{T_1}}{\omega_0}\right). \tag{2.8}$$

The IIP_3 of each transistor M_i ($i = 1, 2$) can be derived from the drain current equation, given by [28]:

$$I_{di} = \frac{1}{2}\mu_0 C_{ox}\frac{W_i}{L_i}\frac{V^2_{odi}}{1+\Theta V_{odi}}\frac{1}{1-\lambda V_{dsi}}, \tag{2.9}$$

where V_{odi}, defined by $V_{odi} = V_{gsi} - V_{thi}$, is the overdrive voltage of M_i and V_{thi} is the threshold voltage of M_i; W_i and L_i are the gate width and length of M_i, respectively; λ is the channel-length modulation coefficient; $\Theta = \mu_0/(2v_{sat}L)+\theta$ and v_{sat} is the saturation velocity of the carrier, μ_0 the carrier mobility under low electric field, and θ the mobility reduction parameter. For a signal small $v_{in}(t)$ applied to the LNA, the output current of each transistor is expressed as [19]

$$I_{di}(t) = \frac{c_0(c_1 + c'_i v_i(t))^2}{c_2 + c_3 v_i(t) + c'^2_i c_4 v^2_i(t)} \quad (i = 1, 2), \tag{2.10}$$

$$c'_i = \frac{1}{j\omega_0 C_{gs1} Z_{in}} \quad (i = 1), \quad -1 \quad (i = 2), \tag{2.11}$$

$$c_0 = \frac{1}{2}\mu_0 C_{ox}\frac{W_i}{L_i}, \tag{2.12}$$

$$c_1 = V_{odi}, \tag{2.13}$$

$$c_2 = (1+\Theta V_{odi})(1-\lambda V_{dsi}), \tag{2.14}$$

$$c_3 = (1+\Theta V_{odi})\lambda A_{vi} + c'_i(1-\lambda V_{dsi})\Theta, \tag{2.15}$$

$$c_4 = \Theta\lambda A_{vi}, \tag{2.16}$$

where $v_1(t) = v_{in}(t)$ and $v_2(t) = -A_{v1}v_{in}(t)$. Substituting the Taylor expansion coefficients of Eq. (2.10) such as α_1 and α_3 into Eq. (1.12), we obtain

$$A^2_{i,IIP_3} = \frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right| = \frac{4}{3}\left|\frac{c_1 c_2^2(c_1c_3 - 2c'_i c_2)}{(-c'_i c_2 + c_1 c_3)[(-c'_i c_2 + c_1 c_3)c_3 - 2c'_i c_1 c_2 c_4]}\right|. \tag{2.17}$$

Substituting Eqs. (2.8) and (2.17) into Eq. (2.7) gives the overall IIP_3 of the cascode LNA.

2.2.2 Limitations

Circuit Topology

The cascode LNA is not suitable for low-voltage operation, because it requires a supply voltage of more than two drain-source saturation voltages ($V_{DD} > 2V_{DS,sat}$) to operate the cascode transistor. No cascode transistor allows the LNA to operate at lower supply voltages, but causes poor performance (i.e., a lower gain and higher NF) due to the Miller effect. An alternative circuit to reduce the effect is required.

Small-Signal Equivalent Circuit

The small-signal equivalent circuit shown in Fig. 2.2 ignores the gate-drain capacitance of M_1, C_{gd1} and input parasitic capacitance C_p originating from a gate inductor, input pad, and electro-static-discharge (ESD) devices. These capacitances cause the following effects on the LNA performance:

- C_{gd1} increases effective C_{gs1} and L_s (i.e., the Miller effect), having an impact on the input impedance matching as well as the noise and gain performance [19].

- C_p reduces Z_{in}, changing the input impedance matching condition [15, 29].

The next section will present a low-voltage circuit topology with a small Miller effect and its complete small-signal equivalent circuit including the above parasitic capacitances.

2.3 Two-Stage LNA with Inductive Source Degeneration

This section presents a two-stage LNA with inductive source degeneration and describes its small-signal equivalent circuit and analytical expressions.

2.3.1 Circuit Topology

Figure 2.4 shows the two-stage LNA that consists of the common-source stage with inductive source degeneration and the common-gate stage. The two internal LC tanks, $L_{I1}C_{I1}$ and $L_{I2}C_{I2}$, provide high impedances at the resonance frequencies, and thereby the signal current amplified by the common-source transistor M_1 flows into the common-gate transistor M_2, which alleviates the Miller effect of M_1. The common-gate stage converts the current to the output voltage using the load LC tank L_LC_L. The DC-blocking capacitor C_c separates the DC voltages of two stages. The required supply voltage of the two-stage LNA is only more than $V_{DS,sat}$, so that the LNA can operate at lower supply voltages than the cascode LNA.

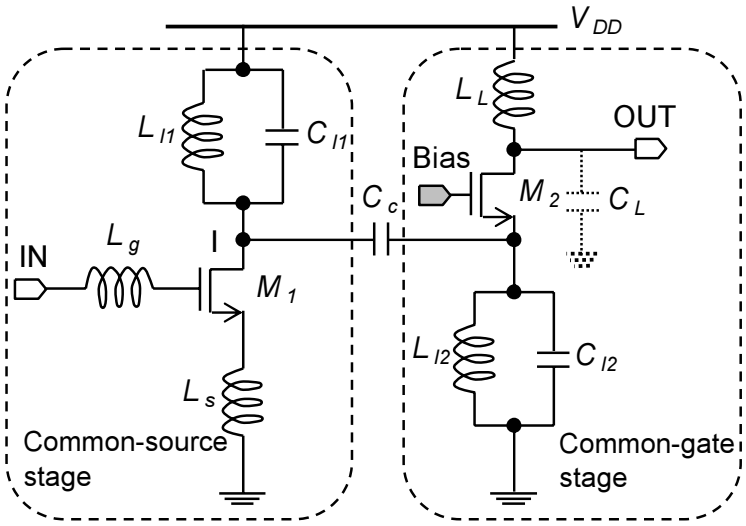

Figure 2.4: Schematic of the two-stage LNA with inductive source degeneration.

2.3.2 Small-Signal Equivalent Circuit

The input parasitic capacitance C_p varies the LNA input impedance. The input section of the two-stage LNA is shown in Fig. 2.5(a). The input impedance looking into the right hand side of reference plane 1 is given by

$$Z'_{in} = \frac{R_{in}(1-\omega_0^2 L_g C_p) + j(\omega_0 L_g + X_{in} - \omega_0^2 L_g C_p X_{in})}{1-\omega_0 C_p X_{in} + j\omega_0 C_p R_{in}}, \tag{2.18}$$

where R_{in} and X_{in} are the resistance and reactance of the input impedance looking into the right hand side of reference plane 2, respectively. On the other hand, the equivalent source impedance looking into the left hand side of reference plane 2, $R_{eq} + j\omega_0 L_{eq}$, is given by

$$R_{eq} = \frac{R_s}{\omega_0^2 C_p^2 R_s^2 + (1-\omega_0^2 C_p L_g)^2}, \tag{2.19}$$

$$L_{eq} = \frac{L_g - C_p(\omega_0^2 L_g^2 + R_s^2)}{\omega_0^2 C_p^2 R_s^2 + (1-\omega_0^2 C_p L_g)^2}. \tag{2.20}$$

Using the above impedances, we can derive the input impedance matching condition as

$$Z'_{in} = R_s \tag{2.21}$$

or

$$R_{eq} = R_{in}, \tag{2.22}$$

$$\omega_0 L_{eq} = -X_{in}. \tag{2.23}$$

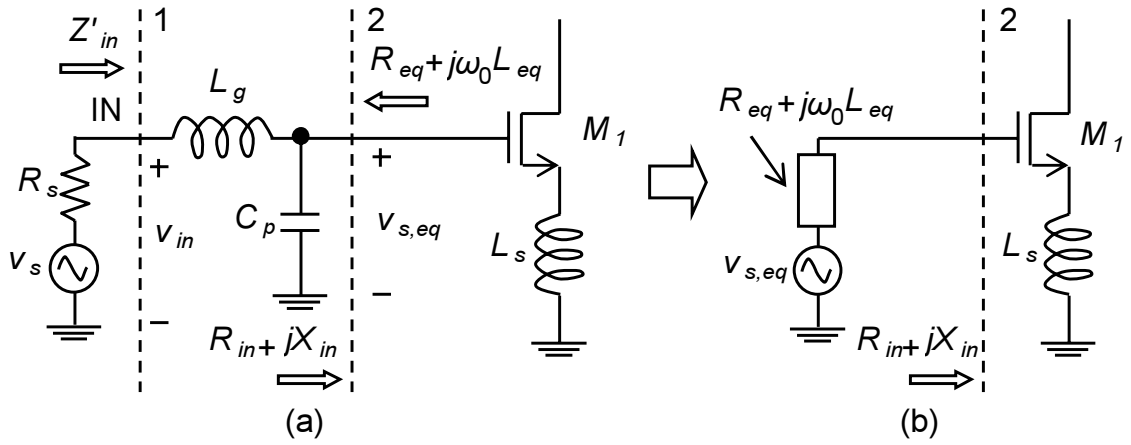

Figure 2.5: (a) Input section of the LNA and (b) the Thevenin's equivalent circuit of the input section.

The equivalent signal source voltage $v_{s,eq}$ applied to reference plane 2 is also given by

$$v_{s,eq} = \frac{v_s}{1 - \omega_0^2 C_p L_g + j\omega_0 C_p R_s}. \tag{2.24}$$

From Thevenin's theorem, the input section can be expressed as Fig. 2.5(b).

The gate-drain capacitance of M_1, C_{gd1}, causes the Miller effect, varying the LNA input impedance. Figure 2.6 shows the small-signal equivalent circuit of the common-source stage including C_{gd1}. For more accurate analysis, the non-quasi-static (NQS) resistance $r_{nqs} = 1/\kappa g_{m1}$ [19] is also included. Using Figure 2.6, we can derive the input impedance $Z_{in} = R_{in} + jX_{in}$ at reference plan 2 as

$$R_{in} = \frac{r_{nqs} + \omega_{T_1} L_s}{\alpha_M}, \tag{2.25}$$

$$X_{in} = \frac{\omega_0 L_s - \frac{1}{\omega_0 C_{gs1}}}{\alpha_M}, \tag{2.26}$$

$$\begin{aligned} \alpha_M &= 1 + \frac{g_{m1}}{Y_I/\alpha_{gd1} + j\omega C_{gs1}} + \frac{Y_I\left(1 - \omega^2 L_s C_{gs1} + j\omega L_s g_{m1}\right)}{Y_I/\alpha_{gd1} + j\omega C_{gs1}} \\ &\approx 1 + \alpha_{gd1}\left(\frac{g_{m1}}{Y_I} + 1 - \omega^2 L_s C_{gs1} + j\omega L_s g_{m1}\right), \end{aligned} \tag{2.27}$$

$$\alpha_{gd1} = \frac{C_{gd1}}{C_{gs1}}, \tag{2.28}$$

$$Y_I = \frac{1}{R_I} + g_{m2}, \tag{2.29}$$

where Y_I represents the input admittance of the common-gate stage at node I. In Eq. (2.27), $j\omega C_{gs1}$ is ignored against Y_I/α_{gd1}. The resistance R_I represents the parallel resistance of $R_{L_{I1}}$

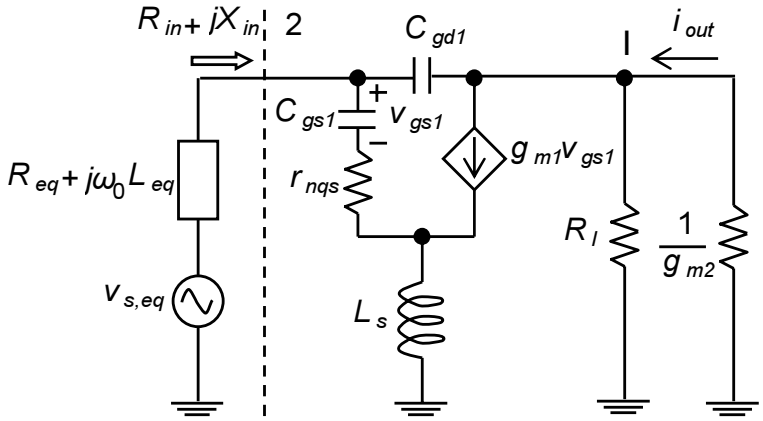

Figure 2.6: Small-signal equivalent circuit of the common-source stage.

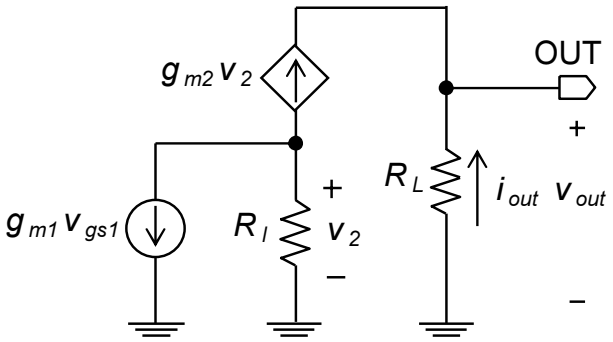

Figure 2.7: Small-signal equivalent circuit of the common-gate stage.

and $R_{L_{I2}}$ (i.e., $R_{L_{I1}}//R_{L_{I2}}$), where $R_{L_{Ii}}$ (i =1, 2) is the equivalent resistance of the internal LC tank, $L_{Ii}C_{Ii}$, at the resonance frequency of $\omega_{L_{Ii}} = 1/\sqrt{L_{Ii}C_{Ii}}$ and is approximated by Eq. (2.4). The transconductance g_{mi} of M_i is given by a derivative of Eq. (2.9):

$$g_{mi} = \frac{\partial I_{di}}{\partial V_{odi}} = \frac{1}{2}\mu_0 C_{ox}\frac{W_i}{L_i}\frac{V_{odi}(2+\Theta V_{odi})}{(1+\Theta V_{odi})^2}\frac{1}{1-\lambda V_{dsi}}. \tag{2.30}$$

Equations (2.27) and (2.29) show that decreasing g_{m2} leads to a larger α_M, resulting in a lower Z_{in}.

Figure. 2.7 shows the small-signal equivalent circuit of the common-gate stage. The Miller effect due to C_{gd2} is negligible, because the gate terminal of M_2 is connected to the AC ground. The NQS resistance of M_2 is also negligible. The resistance R_L represents the equivalent resistance of the load LC tank L_LC_L, and is given by Eq. (2.4).

2.3.3 Analytical Expressions

The equivalent circuit presented in the previous subsection provides more precise analytical expressions of the LNA performance than the simple equivalent circuit shown in Section 2.2. The analytical equations of the gain, noise, and linearity are derived in this subsection.

Gain

The output current i_{out} flows into the output load R_L, generating the output voltage:

$$v_{out} = -i_{out} R_L. \tag{2.31}$$

From Figs. 2.6 and 2.7, i_{out} is given by

$$i_{out} = \frac{g_{m1} v_{s,eq}}{2R_{in} \cdot j\omega_0 \alpha_M C_{gs1}} \left(\frac{R_I}{R_I + 1/g_{m2}} \right), \tag{2.32}$$

where input impedance matching is assumed (i.e., $R_{eq} = R_{in}$ and $\omega_0 L_{eq} = -X_{in}$). The voltage gain of the LNA is defined as the ratio of the output voltage to the input voltage at reference plane 1 (see Fig. 2.5(a)):

$$A_{v,LNA} \equiv \left| \frac{v_{out}}{v_{in}} \right| = 2 \left| \frac{v_{out}}{v_s} \right| = 2 \left| \frac{v_{out}}{v_{s,eq}(1 - \omega_0^2 C_p L_g + j\omega_0 C_p R_s)} \right|, \tag{2.33}$$

where $Z'_{in} = R_s$ is assumed. Substituting Eqs. (2.31) and (2.32) into (2.33) gives

$$A_{v,LNA} = \frac{R_L}{R_{in}\alpha_M} \left(\frac{\omega_{T_1}}{\omega_0} \right) \left| \frac{1}{1 - \omega_0^2 C_p L_g + j\omega_0 C_p R_s} \right| \left(\frac{R_I}{R_I + 1/g_{m2}} \right), \tag{2.34}$$

which indicates that a large C_p and small g_{m2} lead to a decrease in $A_{v,LNA}$.

Noise

The noise of M_1, M_2, R_I, and R_L contribute to the overall LNA noise. The LNA noise factor can be derived from the small-signal equivalent circuits shown in Figs. 2.6 and 2.7:

$$F_{LNA} = 1 + F_{M_1} + F_{M_2} + F_{R_I} + F_{R_L}, \tag{2.35}$$

$$F_{M_1} = \frac{\gamma_1 \chi_1}{\alpha_1} g_{m1} R_{eq} \left(\frac{\omega_0}{\omega_{T_1}} \right)^2 + \frac{\alpha_1 \delta_1}{\kappa_1 g_{m1} R_{eq}}, \tag{2.36}$$

$$F_{M_2} = 4R_{eq}\alpha_M^2 \left(\frac{\omega_0}{\omega_{T_1}} \right)^2 \frac{\gamma_2 \chi_2 g_{m2}}{\alpha_2}, \tag{2.37}$$

$$F_{R_I} = 4R_{eq}\alpha_M^2 \left(\frac{\omega_0}{\omega_{T_1}} \right)^2 \frac{1}{R_I}, \tag{2.38}$$

$$F_{R_L} = 4R_{eq}\alpha_M^2 \left(\frac{\omega_0}{\omega_{T_1}} \right)^2 \frac{(1 + 1/g_{m2}R_I)^2}{R_{L_{3,p}}}, \tag{2.39}$$

where F_{M_1}, F_{M_2}, F_{R_I}, and F_{R_L} represent the noise contributions from M_1, M_2, R_I, and R_L, respectively, and χ_1 and χ_2 are given by

$$\chi_1 = (1+\alpha_{gd1})^2 - 2|c|\alpha_1\sqrt{\frac{\delta_1}{\kappa_1\gamma_1}}(1+\alpha_{gd1}) + \frac{\alpha_1^2\delta_1}{\kappa_1\gamma_1}, \tag{2.40}$$

$$\chi_2 = \left(\frac{1+1/g_{m2}R_I}{1+g_{m2}R_I}\right)^2 + \left(\frac{\omega_0}{\omega_{T_2}}\right)^2\frac{\alpha_2^2\delta_2}{\kappa_2\gamma_2}, \tag{2.41}$$

respectively. The detailed derivations are summarized in Appendix A.1. Equations (2.36)–(2.39) indicate that increasing ω_{T_1} leads to a lower NF and a lower g_{m2} (higher α_M) results in the increase of F_{M_2}, F_{R_I}, and F_{R_L}.

Linearity

The two-stage LNA consists of the common-source and common-gate stages, and hence the overall IIP_3 of the LNA can be derived in the same way as that of the cascode LNA:

$$\frac{1}{A_{LNA,IIP_3}^2} \approx \frac{1}{A_{1,IIP_3}^2} + \frac{A_{v1}^2}{A_{2,IIP_3}^2}, \tag{2.42}$$

$$A_{v1} = \left|\frac{v_i}{v_{in}}\right| = \frac{\frac{1}{g_{m2}}//R_I}{R_{in}\alpha_M}\left(\frac{\omega_{T_1}}{\omega_0}\right)\left|\frac{1}{1-\omega_0^2C_pL_g+j\omega_0C_pR_s}\right|, \tag{2.43}$$

$$A_{i,IIP_3}^2 = \frac{4}{3}\left|\frac{c_1c_2^2(c_1c_3-2c_i'c_2)}{(-c_i'c_2+c_1c_3)[(-c_i'c_2+c_1c_3)c_3-2c_i'c_1c_2c_4]}\right|, \tag{2.44}$$

$$c_i' = \frac{1}{j\omega_0\alpha_MC_{gs1}R_{in}(1-\omega_0^2L_gC_p+j\omega_0C_pR_s)} \ (i=1), -1 \ (i=2), \tag{2.45}$$

where A_{1,IIP_3} and A_{2,IIP_3} represent the IIP_3 of the common-source and common-gate stages in the expression of the voltage amplitude, respectively; A_{v1} represents the voltage gain of the common-source stage and v_i the voltage at node I as shown in Fig. 2.6; $c_0 - c_4$ in Eq. (2.44) are given by Eqs. (2.12)–(2.16).

2.4 Design Methodology

This section describes a design methodology of the two-stage LNA that meets the typical specifications of LNAs for WLAN receivers [18], shown in Table 2.1. In this design, 0.15 μm FD-SOI CMOS process and device parameters are used, and the current consumption and supply voltage are set to 8.0 mA and 1.0 V, respectively. There are thirteen design variables: the bias currents of the two transistors (I_{d1} and I_{d2}), the overdrive voltages (V_{od1} and V_{od2}), the gate widths and lengths (W_1/L_1 and W_2/L_2), gate and source inductances (L_g and L_s), internal inductances (L_{I1} and L_{I2}), and load inductance (L_L). The gate lengths, L_1 and L_2, are set to the minimum gate length in order to increase ω_{Ti}, resulting in a lower NF [1]. Once I_{di} and V_{odi} are determined,

Table 2.1: Specifications of LNAs for WLAN receivers.

Frequency [GHz]	5.4
S_{11} [dB]	< -10
Voltage Gain [dB]	$>$20
NF [dB]	$<$2.0
IIP_3 [dBm]	> -5

W_i can be calculated from Eq. (2.9). Consequently, we can reduce thirteen design variables to nine ones such as I_{d1}, I_{d2}, V_{od1}, V_{od2}, L_g, L_s, L_{I1}, L_{I2}, and L_L. In what follows, these nine design variables are determined from the derived equations.

Bias Currents of M_1 and M_2

The gain specification determines the distribution of bias currents of M_1 and M_2, I_{d1} and I_{d2}. Equation (2.34) indicates that the voltage gain of the LNA mainly depends on ω_{T_1} ($\propto I_{di}$) and R_L (i.e., Q_L). The quality factors of on-chip inductors are determined by process technologies and inductor structures ($Q_L \simeq 8$ at 5 GHz in this design). Therefore, I_{d1} is selected to satisfy the gain specification, and then I_{d2} to the rest of the given bias current: $I_{d2} = I_{spec} - I_{d1}$. Figure 2.8 shows the calculated voltage gain versus V_{od1} with I_{d1} as a parameter. Note that g_{m2} is set to infinity in Eq. (2.34). For comparison, simulations for $I_{d1} = 7.0$ mA are also plotted in Fig. 2.8. This and the following simulations of the LNA were carried out using the small-signal and noise FD-SOI MOSFET models shown in [30] and Agilent Advanced Design System (ADS). Figure 2.8 shows that the calculations are comparable to the simulations, and the given specification is satisfied in the range of 4.0–8.0 mA. Taking account of process and temperature variations and the effect of M_2, we select I_{d1} to 7.0 mA for a voltage gain of 23 dB including a 3 dB margin, and then I_{d2} to 1.0 mA.

Overdrive Voltage of M_1

Increasing overdrive voltage of M_1, V_{od1}, leads to a lower NF and IIP_3. Figure 2.9 shows the calculated and simulated NF and IIP_3 versus V_{od1} for $I_{d1} = 7.0$ mA. In the calculations and simulations, M_2 was set to be noiseless, and g_{m2} and A^2_{2,IIP_3} to infinity in Eqs. (2.37)–(2.39) and (2.42), respectively. Besides, the noise parameters such as γ_i, δ_i, and α_i based on the experimental results [30] were used. Figure 2.9 shows that the calculations are comparable to the simulations and the noise performance improves with increasing V_{od1}, while the linearity deteriorates. The degradation of the linearity can be explained as follows: For input impedance matching ($Z'_{in} = R_s$), the constant current $i_{in} = v_{in}/R_s$ injects into the LNA. In this case, the

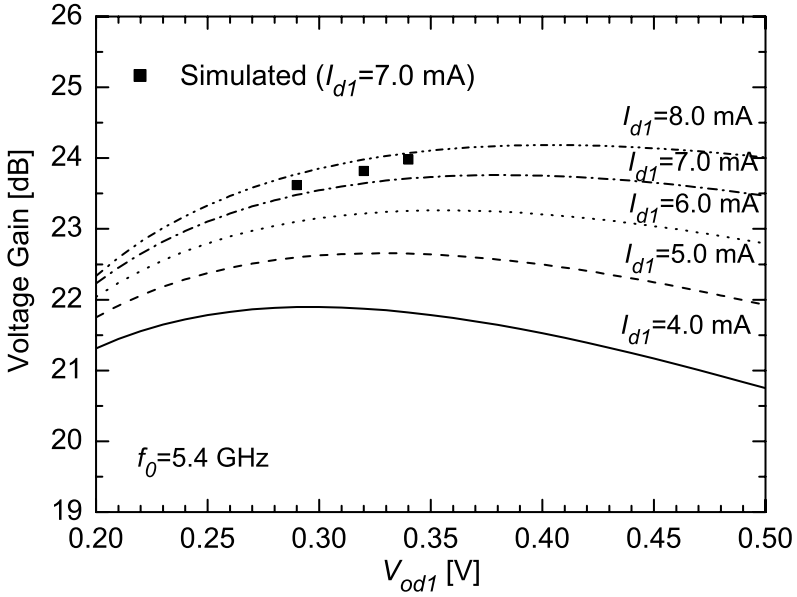

Figure 2.8: Calculated and simulated voltage gain versus V_{od1} with I_{d1} as a parameter.

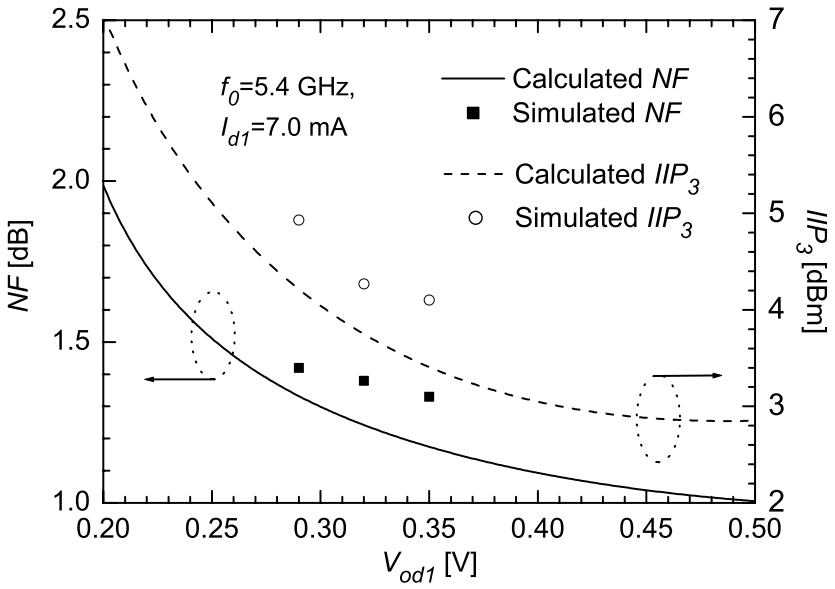

Figure 2.9: Calculated and simulated NF and IIP_3 versus V_{od1}.

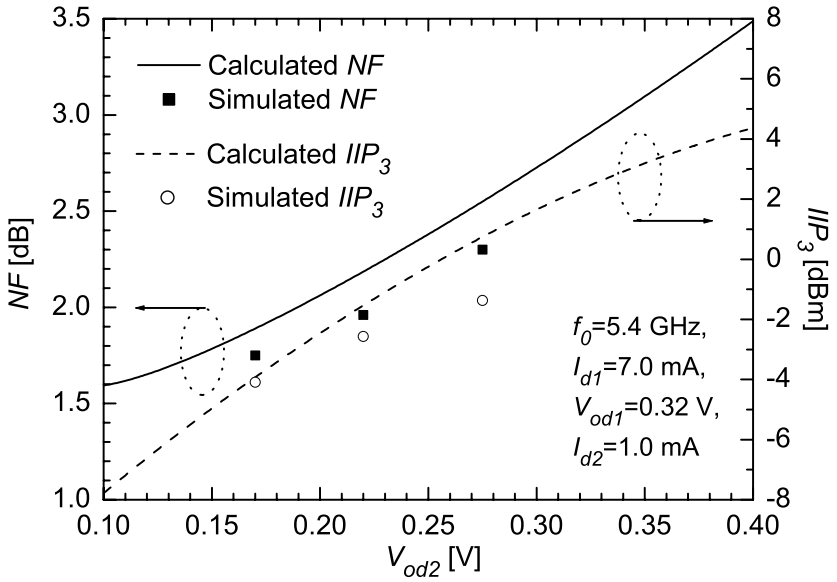

Figure 2.10: Calculated and simulated NF and IIP_3 versus V_{od2}.

gate-source voltage of M_1 is approximated by

$$v_{gs1} \approx \frac{i_{in}}{j\omega_0 C_{gs1}} = \frac{v_{in}}{j\omega_0 C_{gs1} R_s}. \tag{2.46}$$

For a fixed I_{d1}, the gate width, i.e., the gate-source capacitance of M_1, C_{gs1}, decreases with increasing V_{od1}, which results in an increase of v_{gs1}, as shown in Eq. (2.46). Although the MOSFET generally has higher linearity with increasing V_{od} (because I_{di} is proportional to V_{odi} when V_{odi} is large), the degradation of linearity due to the increase in v_{gs1} becomes significant in the range of 0.20–0.50 V, causing poor linearity. Taking account of additional noise of the common-gate stage, we set V_{od1} to 0.32 V, which results in W_1 =5×24 μm (24 gate fingers, each with a unit of 5 μm width) and provides calculated $NF = 1.25$ dB and $IIP_3 = 3.8$ dBm.

Overdrive Voltage of M_2

Increasing the overdrive voltage of M_2, V_{od2}, allows high linearity, but causing a higher NF. Figure 2.10 shows the calculated and simulated NF and IIP_3 versus V_{od2} for $I_{d1} = 7.0$ mA, $V_{od1} = 0.32$ V, and $I_{d2} = 1.0$ mA. Increasing V_{od2} results in better linearity but poor noise performance. The reason for a higher NF is that increasing V_{od2} leads to a decrease in g_{m2} and increase in α_M for a fixed I_{d2}, which results in a larger F_{M_2}, F_{R_I}, and F_{R_L}, as shown in Eqs. (2.37)–(2.39). Figure 2.10 also shows that the difference between the IIP_3 calculations and simulations increases at higher V_{od2}: the calculated IIP_3 becomes higher than the simulated IIP_3 as V_{od2} increases. This difference originates form the simplification of I_{di} (Eq. (2.9)) and

the IIP_3 approximation of two nonlinear stages in cascade (Eq. (2.42)). With a few simulations, we can avoid to overestimate the achievable IIP_3. From Fig. 2.10, we can find $V_{od2} = 0.17$ V, at which the noise and linearity specifications are satisfied on both calculation and simulation. This results in $W_2 = 50$ μm and calculated $NF = 1.85$ dB and $IIP_3 = -4.1$ dBm.

Inductors

The gate and source inductances, L_g and L_s, are determined from the impedance matching conditions. Substituting the determined design variables into Eqs. (2.22) and (2.23) gives $L_g \simeq 3.3$ nH and $L_s \simeq 1.0$ nH. The source inductor L_s is implemented by a 2.5-turn square spiral inductor with a diameter of 115 μm, a metal width of 8 μm, and a metal spacing of 2 μm, while the gate inductor L_g by a bonding wire [29], which has a higher Q than on-chip inductors [19, 31], resulting in a smaller NF.

The inductances in the LC tanks, L_{I1}, L_{I2}, and L_L, are determined from the resonance frequency, given by $\omega = 1/\sqrt{LC}$. Substituting $f = 5.4$ GHz and $C = 300$ fF into $L = 1/\omega^2 C$, we obtain an L of 3.1 nH. For these inductors, 3.5-turn square spiral inductors with a diameter of 170 μm, a metal width of 8 μm, and a metal spacing of 2 μm are used.

Figure 2.11 shows the complete schematic of the designed two-stage LNA. For measurements, a unity-gain common-source amplifier with a 50 Ω output resistor is used as a buffer. The 10 pF capacitor provides the AC ground for the gate terminal of M_2. The bias voltages are generated by current mirror circuits (not shown).

2.5 Experimental Results and Discussion

The designed two-stage LNA was fabricated in a 0.15 μm FD-SOI CMOS process with a high resistivity substrate ($\sim$1 kΩ·cm), metal-insulator-metal (MIM) capacitors, and five metal layers including a 1.95-μm thick metal layer. The cut-off frequency of a 0.15 μm NMOS consisting of 48 gate fingers with a unit of 5 μm width was approximately 54 GHz for $V_{ds} = 1$ V and $I_d = 7$ mA [21]. A micrograph of the fabricated LNA is shown in Fig. 2.12. The active chip area excluding pads was 0.46 mm $\times$ 0.53 mm. The input and output pads were not ESD protected. The stand-alone buffer and inductor for L_{I1}, L_{I2}, and L_L were also fabricated on the same chip. The current consumption of the LNA and buffer were 8.3 mA and 5.8 mA from a 1.0 V supply voltage, respectively. The S-parameters, NF and IIP_3 of the LNA without L_g were measured using on-wafer RF probes. The above characteristics of the LNA with L_g were calculated based on the measurements [30]. This avoids instrumental error originating from a bonding wire L_g.

2.5.1 Inductor

The S-parameters of the fabricated 3.1 nH inductor were measured using an Agilent Technologies HP8722ES network analyzer and then converted into Y-parameters. The inductance and quality

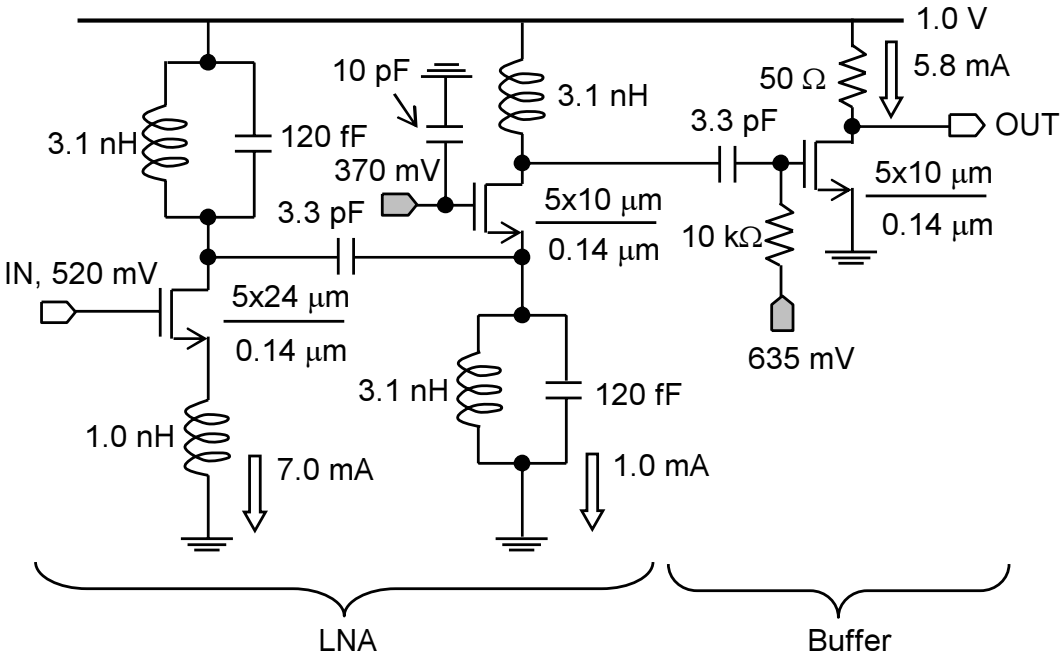

Figure 2.11: Complete schematic of the designed two-stage LNA.

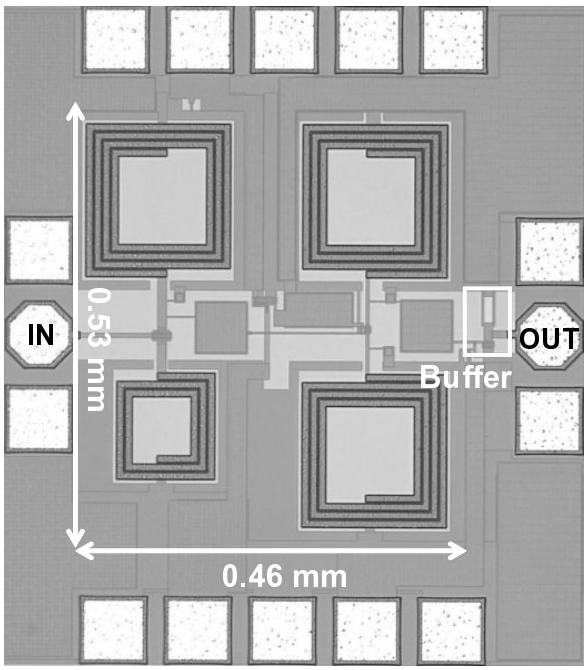

Figure 2.12: Micrograph of the fabricated LNA.

factor, L and Q, can be calculated from the Y-parameters and following equations [32]:

$$L = \text{Im}\left[\frac{1/Y_{11}}{\omega}\right], \tag{2.47}$$

$$Q = \frac{\text{Im}\left[1/Y_{11}\right]}{\text{Re}\left[1/Y_{11}\right]}. \tag{2.48}$$

Figures 2.13 and 2.14 show the measured L and Q of the inductor, respectively. For comparison, the L and Q achieved using a three-dimensional (3-D) electromagnetic simulator (Ansoft HFSS) are also shown in Figs. 2.13 and 2.14, respectively. The measured L was 3.2 nH and Q was 8.0 at 5.4 GHz.

2.5.2 S-parameters

Figures 2.15 and 2.16 show the measured and simulated S-parameters of the LNA with an ideal gate inductor of 3.3 nH. The S-parameters were measured using the same network analyzer as in the inductor measurements. An S_{11} of less than -10 dB was achieved around 5.4 GHz, where a maximum S_{21} was 23 dB, which met the WLAN specification shown in Tab. 2.1. The agreements between the measurements and simulations are due to the small-signal FD-SOI MOSFET models proposed in [30]. Figure 2.16 shows that S_{12} and S_{22} are -46 dB and -9.9 dB at 5.4 GHz, respectively. The discrepancy between the measured and simulated S_{12} is attributed to measurement limits. The measured S_{12} of the stand-alone buffer (not shown) was -29 dB. The S_{12} of the stand-alone LNA was thus approximately -17 dB.

2.5.3 NF

Figure 2.17 shows the measured and simulated NF. The NF was measured using an Agilent Technologies HP8970B noise figure meter and Maury automated tuner system. The LNA achieved an NF of 1.7 dB at 5.4 GHz, satisfying the noise specification. The measurements agree well with the simulations, due to the noise models proposed in [30].

2.5.4 Linearity

Figures 2.18 and 2.19 show the measured output power of the fundamental tones and third-order intermodulation (IM_3) products for two tones (5.4 and 5.41 GHz), applied to the LNA and stand-alone buffer. The two tones were generated by Agilent Technologies HP8671B and E4438C signal generators, and the fundamental and IM_3 tones were measured using an Agilent Technologies E4448A spectrum analyzer. The measured IIP_3 of the LNA with the buffer was -18.0 dBm, while that of the stand-alone buffer was 4.8 dBm. The IIP_3 of the LNA without the buffer can be calculated from the following equation:

$$\frac{1}{A^2_{LNA,IIP_3}} \approx \frac{1}{A^2_{LNA+Buf,IIP_3}} - \frac{A^2_{v,LNA}}{A^2_{Buf,IIP_3}}, \tag{2.49}$$

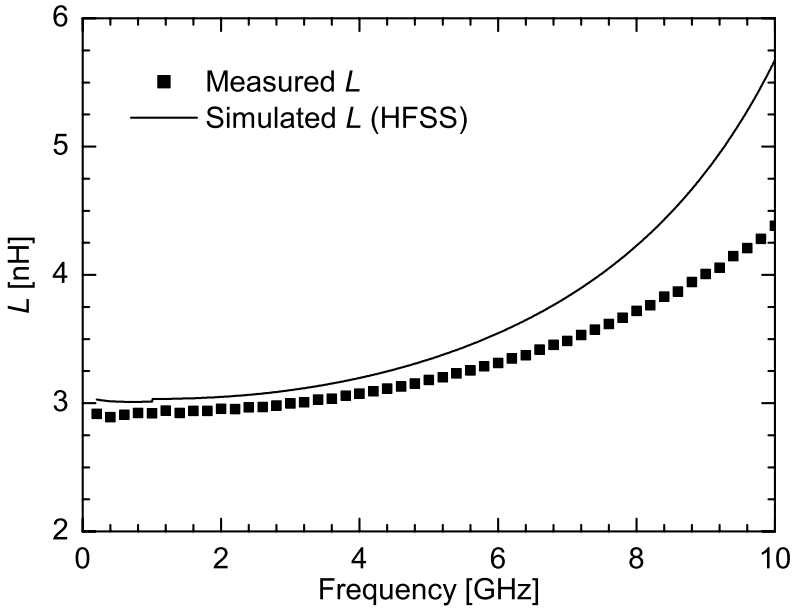

Figure 2.13: Measured and simulated L of the fabricated 3.1 nH inductor.

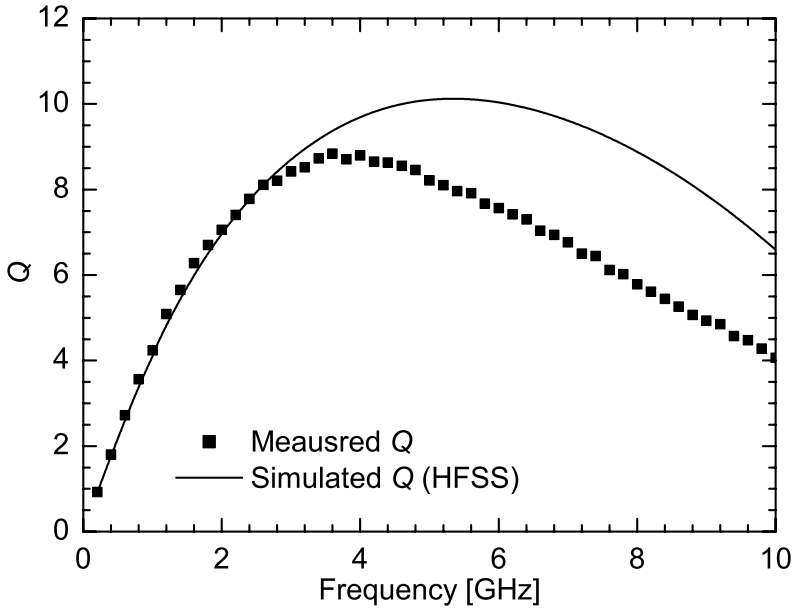

Figure 2.14: Measured and simulated Q of the fabricated 3.1 nH inductor.

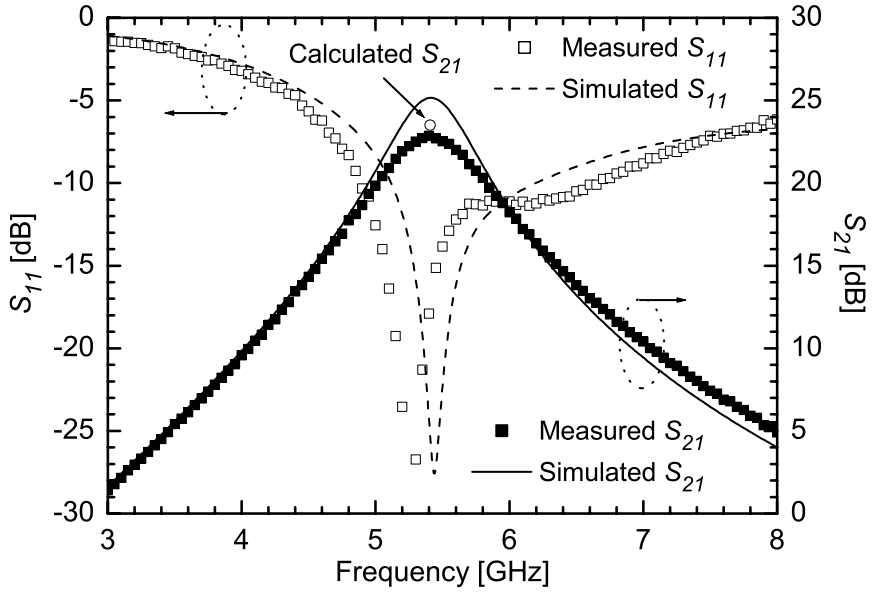

Figure 2.15: Measured and simulated S_{11} and S_{21} of the LNA.

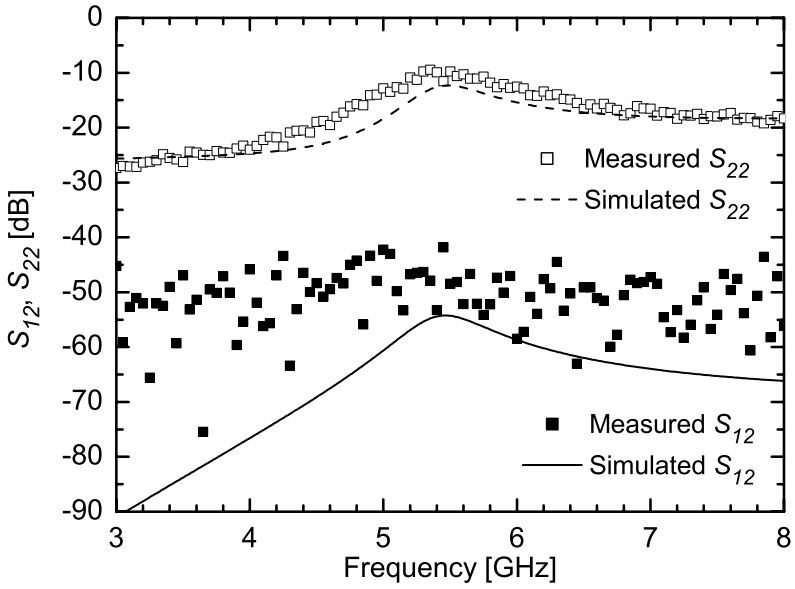

Figure 2.16: Measured and simulated S_{12} and S_{22} of the LNA.

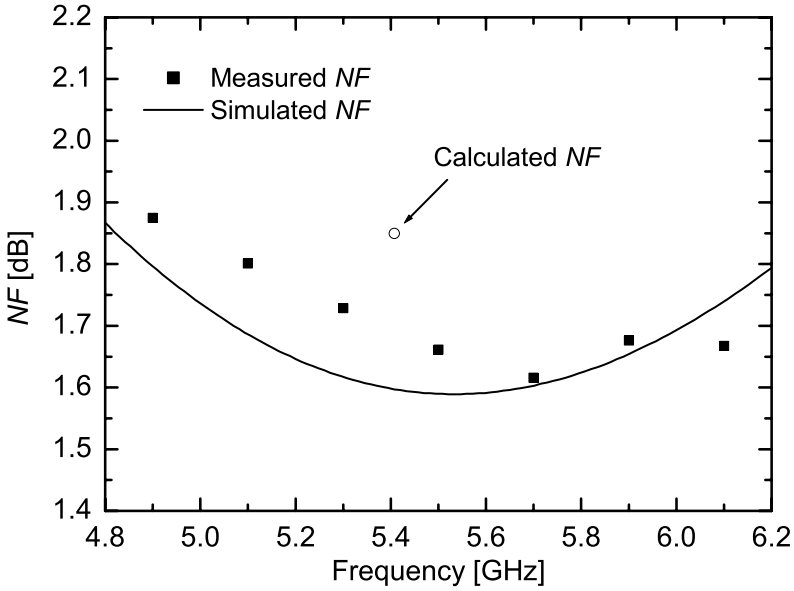

Figure 2.17: Measured and simulated NF of the LNA.

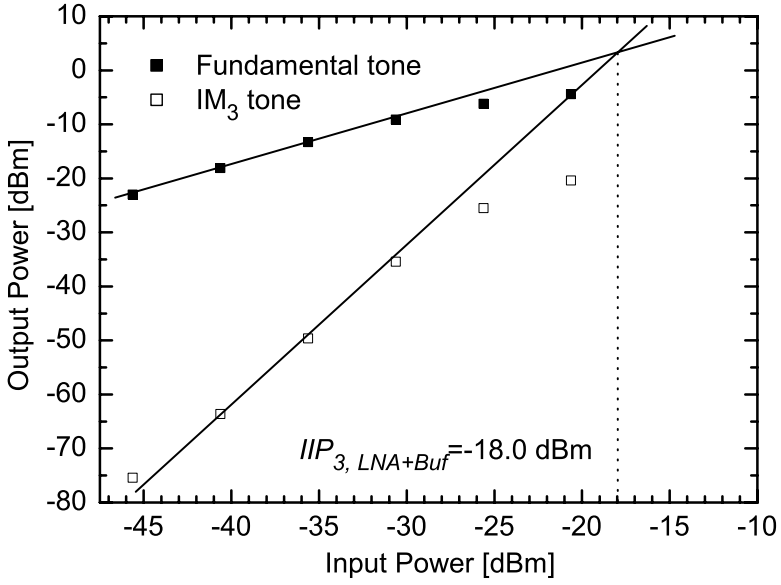

Figure 2.18: Measured IIP_3 of the LNA with the buffer.

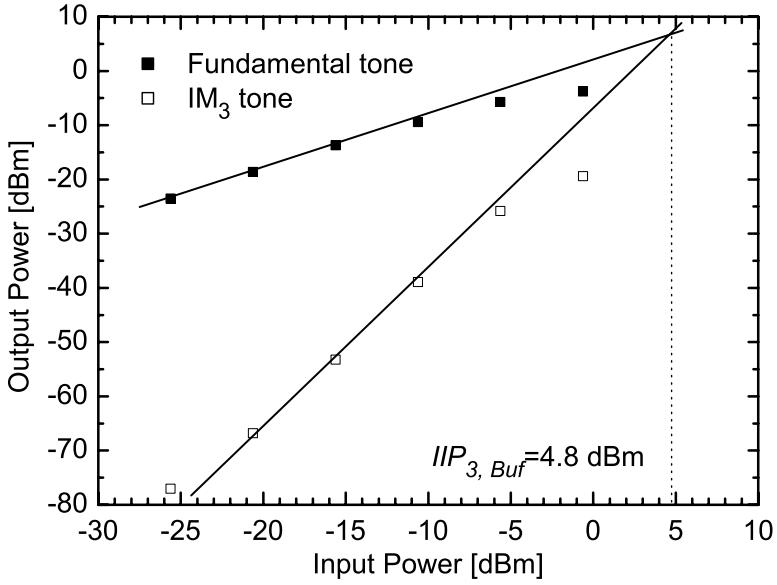

Figure 2.19: Measured IIP_3 of the stand-alone buffer.

where $A_{v,LNA}$ is the voltage gain of the LNA and A_{LNA,IIP_3}, A_{Buf,IIP_3}, and $A_{LNA+Buf,IIP_3}$ represent the IIP_3 of the LNA, buffer, and LNA cascaded with the buffer in the expression of voltage amplitude, respectively. Substituting $IIP_{3,LNA+Buf} = -18.0$ dBm, $IIP_{3,Buf} = 4.8$ dBm and $A_{v,LNA} = 22.5$ dB into Eq. (2.49) gives $IIP_{3,LNA} = -6.1$ dBm.

2.5.5 Comparison

Table 2.2 shows a comparison of the LNA performance obtained from the measurements, simulations, and calculations. The simulated and calculated voltage gain and NF were consistent with the measured results, which satisfied the specifications. The calculated IIP_3 agreed well with the simulated one, but these results were slightly different from the measured IIP_3. The difference can be attributed to inaccurate FD-SOI MOS device parameters used in the simulations

Table 2.2: Comparison of the LNA performance at 5.4 GHz.

	Gain [dB]	NF [dB]	IIP_3 [dBm]
Specification	20	2.0	-5.0
Measurement	23	1.70	-6.1
Simulation	25	1.60	-3.0
Calculation	23	1.85	-4.1

and calculations. Although the fabricated LNA did not meet the IIP_3 specification, its linearity can be improved by increasing I_{d2} as shown in Section 2.4.

Table 2.3 shows a summary of the LNA and a comparison with previously reported 1.0 V, 5 GHz CMOS LNAs. The figure of merits for LNAs, FoM_1 and FoM_2 included in Table 2.3, are defined as [36]:

$$FoM_1[\text{mW}^{-1}] = \frac{Gain[\text{lin}]}{Power[\text{mW}] \cdot (NF[\text{lin}] - 1)}, \tag{2.50}$$

$$FoM_2[\text{–}] = \frac{Gain[\text{lin}] \cdot IIP_3[\text{mW}] \cdot f_0[\text{GHz}]}{Power[\text{mW}] \cdot (NF[\text{lin}] - 1)}. \tag{2.51}$$

The proposed LNA obtained the best FoM_1 among the other 1.0 V, 5 GHz CMOS LNAs. Although the LNA reported in [34] achieved the lowest NF and best FoM_2, it adopted an input-output differential topology and had difficulty in achieving input impedance matching.

2.6 Conclusion

This chapter has demonstrated a 1.0 V two-stage CMOS LNA and its design methodology based on derived analytical expressions. The presented two-stage topology that consists of common-source and common-gate stages is more suitable for low-voltage operation than a conventional cascode topology. The analytical expressions show that a higher V_{od1} results in a lower NF and IIP_3 while a higher V_{od2} leads to a higher NF and IIP_3. The proposed design methodology based on the expressions allows us to efficiently design two-stage LNAs that satisfy target specifications. The 1.0 V, 5.4 GHz LNA implemented with a 0.15 μm FD-SOI CMOS technology achieved an NF of 1.7 dB, voltage gain of 23 dB, and IIP_3 of -6.1 dBm with a power consumption of 8.3 mW. These measurements were consistent with the calculations obtained from the derived expressions. This ensures the validity of the analytical expressions and design methodology.

Table 2.3: Measured performance and comparison of 1.0 V, 5 GHz CMOS LNAs.

Reference	CMOS Technology	Frequency [GHz]	S_{11} [dB]	NF [dB]	S_{21} [dB]	IIP_3 [dBm]	Power [mW]	Area [mm^2]	FoM_1 [mW^{-1}]	FOM_2 [-]
This work	150 nm FD-SOI	5.4	-18	1.7	23	-6.1	8.3	0.25	3.55	4.71
[33]*	90 nm	5.5	-12.7	2.8	15.0	-5.6	11.1	0.30	0.56	0.85
[34]†	180 nm	5.75	N/A	0.9	14.2	0.9	16	0.24	2.78	9.85
[35]*	180 nm	5.8	-5.3	2.5	13.2	N/A	22.2	0.54	0.26	N/A

*On-chip gate inductor used

†Input-output differential topology

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Chapter 3

Transformer Folded-Cascode CMOS LNA

3.1 Introduction

Although the continuous scaling of CMOS technologies has improved the high-frequency performance of MOSFETs, it has imposed two challenges on CMOS RFICs: low-voltage operation and small chip area. The ITRS [1] predicts that the supply voltages of low-power digital circuits will decrease to 0.5 V in the near future. Reference [2] shows that a 45 nm (state-of-the-art) CMOS process costs approximately 10 times as much as a 0.13 μm (most widely used) CMOS process. Considering the integration of RF circuits with digital circuits, we need to develop low-voltage and small-area (low-cost) RF circuits.

Folded-cascode CMOS LNAs with inductive source degeneration [3, 4] are the most promising candidates for low-voltage and small-area CMOS LNAs. Although a two-stage CMOS LNA, presented in the previous chapter, achieves higher performance with lower power consumption than the folded-cascode LNAs, it requires more inductors (i.e., five inductors). Other reported low-voltage LNAs [5, 6] consume much larger chip area and less performance than the above LNAs.

This chapter proposes a 0.5 V, 5 GHz transformer folded-cascode CMOS LNA [7], which has a smaller chip area than the conventional folded-cascode LNA. The transformer consists of the internal and load inductors and reduces the chip area of the LNA, while affecting the LNA performance. This chapter is organized as follows. Section 3.2 describes the circuit topology of the proposed LNA. The effects of the transformer on the LNA performance are analyzed in Section 3.3. Section 3.4 describes the design of the LNA and transformer. Section 3.5 presents the measurements of the LNA fabricated in a 90 nm digital CMOS process, and then Section 3.6 concludes the chapter.

3.2 Circuit Topology

Figure 3.1 shows a schematic of the proposed LNA, based on the conventional folded-cascode LNA with inductive source degeneration. The PMOS transistor M_2 reduces the Miller effect of

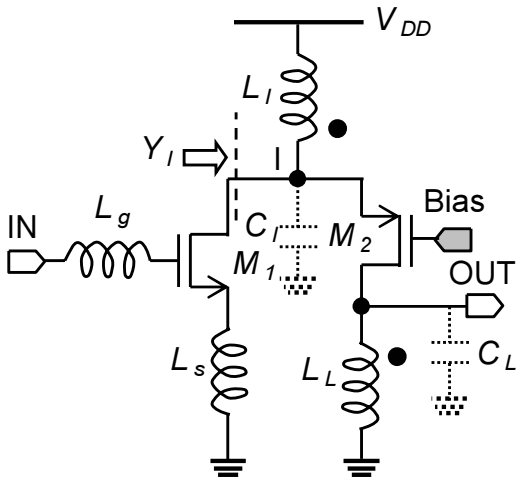

Figure 3.1: Schematic of the proposed LNA.

the gate-drain capacitance of the input transistor M_1, improving the reverse isolation performance of the LNA. It allows less inductors than the NMOS transistor in the two-stage LNA, although it leads to less gain and a larger NF due to a larger parasitic capacitance at node I. The gate and source inductors, L_g and L_s, provide input impedance matching at an operating frequency [8]. The internal inductor L_I, resonating with the parasitic capacitance C_I at node I, provides a high impedance, thereby the signal current amplified by M_1 flows into M_2. The load inductor L_L also resonates with the parasitic capacitance C_L, resulting in a high impedance. These inductors, L_I and L_L, are magnetically coupled to form a transformer in such a way as to have a positive magnetic coupling with retaining the LNA performance.

The positive magnetic coupling of L_I and L_L is the most effective way to reduce the chip area of the folded-cascode LNA. Increasing the magnetic coupling leads to a smaller L_I and L_L (smaller chip area), as will be shown in the next section. On the contrary, the negative magnetic coupling requires a larger L_I and L_L (larger chip area). The coupling of L_g or L_s and L_I or L_L is also not beneficial for the following reasons:

1. L_g is often implemented with a bonding wire.
2. L_s is usually small (< 1.0 nH) for input impedance matching.
3. The coupling makes the LNA unstable.

3.3 Effect of Magnetic Coupling

The magnetic coupling between L_I and L_L affects the LNA performance in terms of input impedance, gain, and noise. In this section, the effects of the magnetic coupling are analyzed, and the stability of the LNA is also discussed.

3.3.1 Input Impedance

The magnetic coupling changes the frequency response of the LNA input impedance Z_{in} through the gate-drain capacitance of M_1, C_{gd1}. The small-signal equivalent circuit of the input stage, shown in Fig. 3.2, yields Z_{in}, given by

$$Z_{in} = j\omega L_g + \frac{\omega_{T1} L_s + j\omega L_s + \frac{1}{j\omega C_{gs1}}}{\alpha_M}, \tag{3.1}$$

$$\begin{aligned}\alpha_M &= 1 + \frac{g_{m1}}{Y_I/\alpha_{gd1} + j\omega C_{gs1}} + \frac{Y_I\left(1 - \omega^2 L_s C_{gs1} + j\omega L_s g_{m1}\right)}{Y_I/\alpha_{gd1} + j\omega C_{gs1}} \\ &\approx 1 + \alpha_{gd1}\left(\frac{g_{m1}}{Y_I} + 1 - \omega^2 L_s C_{gs1} + j\omega L_s g_{m1}\right),\end{aligned} \tag{3.2}$$

where $\omega_{T_1} = g_{m1}/C_{gs1}$ is the unity current gain frequency of M_1; $\alpha_{gd1} = C_{gd1}/C_{gs1}$ is the ratio between C_{gd1} and C_{gs1}; $j\omega C_{gs1}$ is ignored against Y_I/α_{gd1}. The input admittance of the common-gate stage, shown in Fig. 3.3, is given by

$$\begin{aligned}Y_I = \frac{i_i}{v_i} &= g_{m2} + j\omega C_I + \frac{1}{j\omega L_I + R_I} - \frac{j\omega M}{j\omega L_I + R_I}\,\frac{g_{m2} - j\omega C_L \cdot \frac{j\omega M}{j\omega L_I + R_I}}{1 - \omega^2 L_L C_L - j\omega C_L \cdot \frac{(j\omega M)^2}{j\omega L_I + R_I} + j\omega R_L C_L} \\ &\approx g_{m2} + j\omega C_I + \frac{1}{j\omega L_I + R_I} - \frac{nk\left(g_{m2} - j\omega nk C_L\right)}{1 - \omega^2(1-k^2) L_L C_L + j\omega R_L C_L},\end{aligned} \tag{3.3}$$

where g_{m2} is the transconductance of M_2; R_I, ignored in the last term for simplicity, and R_L are the parasitic resistances of L_I and L_L, respectively; M is the mutual inductance of the transformer, and k and $n = \sqrt{L_L/L_I}$ are the coupling factor and turn ratio, respectively. The frequency responses of Y_I and $1/Y_I$ are described in Appendix B. The calculated real and imaginary parts of α_M and Z_{in} are shown in Figs. 3.4(a) and (b), respectively. Using Re[α_M] and Im[α_M], we can approximate Z_{in} as

$$\mathrm{Re}[Z_{in}] \approx \frac{\omega_{T1} L_s \cdot \mathrm{Re}[\alpha_M] - \frac{\mathrm{Im}[\alpha_M]}{\omega C_{gs1}}}{|\alpha_M|^2}, \tag{3.4}$$

$$\mathrm{Im}[Z_{in}] \approx \omega L_g - \frac{\omega_{T1} L_s \cdot \mathrm{Im}[\alpha_M] + \frac{\mathrm{Re}[\alpha_M]}{\omega C_{gs1}}}{|\alpha_M|^2}, \tag{3.5}$$

where ωL_s is ignored against $1/\omega C_{gs1}$. As shown in Fig. 3.4(a), Re[α_M] increases and Im[α_M] decreases at low frequencies, which results in an increase of Re[Z_{in}]. For a low k (<0.6), Re[Z_{in}] becomes a maximum around the frequency at which Im[α_M] becomes a minimum. Meanwhile, Im[Z_{in}] with k approaches zero faster than Im[Z_{in}] without k ($k = 0$), due to the increase in Re[α_M] at low frequencies.

The magnetic coupling shifts the input impedance matching region ($|S_{11}| < -10$ dB) toward lower frequencies. Due to good reverse isolation of the folded-cascode topology ($S_{12} \simeq 0$), the

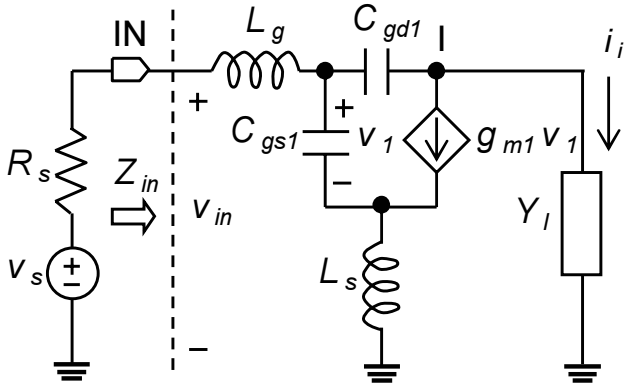

Figure 3.2: Small-signal equivalent circuit of the input stage.

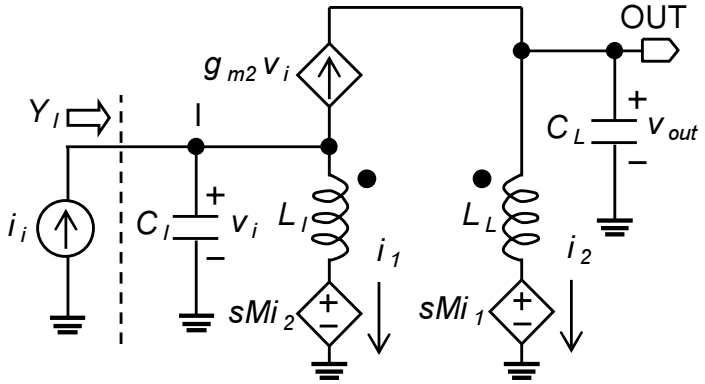

Figure 3.3: Small-signal equivalent circuit of the common-gate stage.

S_{11} of the LNA can be approximated as Eq. (1.1). For input impedance matching at ω_0, the following conditions must be satisfied:

$$\mathrm{Re}[Z_{in}] \simeq R_s, \tag{3.6}$$

$$\mathrm{Im}[Z_{in}] \simeq 0, \tag{3.7}$$

$$\mathrm{Im}[\alpha_M] \simeq 0, \tag{3.8}$$

which give the following conditions:

$$\frac{\omega_{T1} L_s}{\mathrm{Re}[\alpha_M(j\omega_{0,\alpha_M})]} \simeq R_s, \tag{3.9}$$

$$\omega_0 \approx \frac{1}{\sqrt{L_g C_{gs1} \cdot \mathrm{Re}[\alpha_M(j\omega_{0,\alpha_M})]}}, \tag{3.10}$$

$$\omega_{0,\alpha_M} \approx \frac{1}{\sqrt{L_I(C_I + n^2 k^2 C_L)}}, \tag{3.11}$$

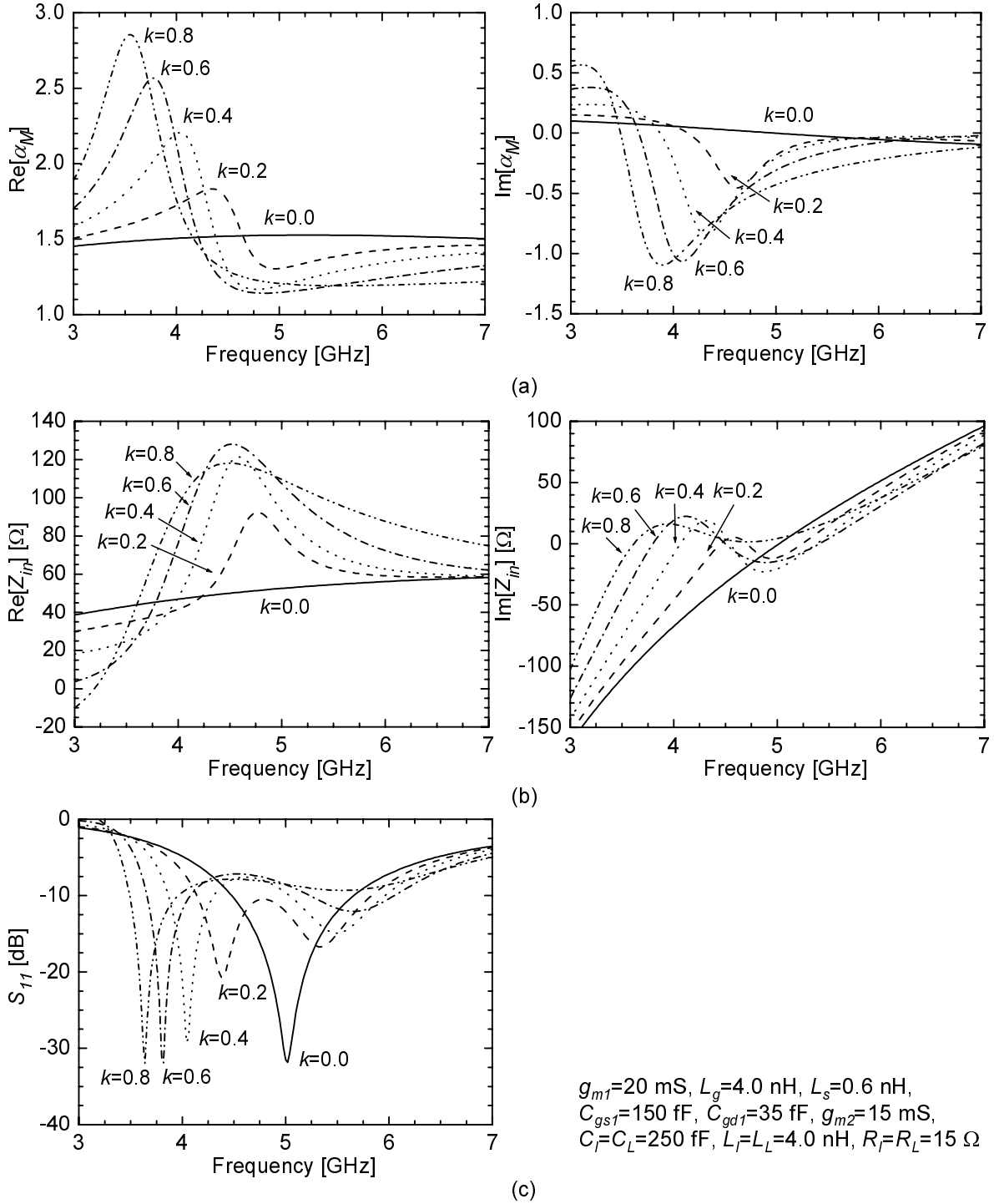

Figure 3.4: Calculated (a) α_M, (b) Z_{in}, and (c) S_{11} with k as a parameter.

respectively, where $\mathrm{Re}[\alpha_M(j\omega_{0,\alpha_M})]$ is approximated as

$$\mathrm{Re}[\alpha_M(j\omega_{0,\alpha_M})] \approx 1 + \alpha_{gd1} + \frac{\alpha_{gd1} g_{m1}}{(1-nk) g_{m2}}. \tag{3.12}$$

Equations (3.9)–(3.12) show that ω_0 and ω_{0,α_M} decrease and $\mathrm{Re}[\alpha_M]$ increases as k increases. Figure 3.4(c) shows the calculated S_{11} with k as a parameter. Input impedance matching is achieved around ω_0, which decreases with increasing k.

3.3.2 Gain

The magnetic coupling reduces the peak frequency and magnitude of the LNA gain. The common-gate stage acts as a transimpedance, which converts the input signal current i_i to the output voltage v_{out}, as shown in Fig. 3.3. The input current i_i amplified by the first stage is derived from Fig. 3.2:

$$i_i \approx -\frac{g_{m1}}{j\omega_0 C_{gs1} R_s \cdot \mathrm{Re}[\alpha_M]} v_{in}, \tag{3.13}$$

where input impedance matching is assumed (i.e., $Z_{in} = R_s$) and v_{in} represents the input voltage of the LNA as shown in Fig. 3.2. The transimpedance from node I to the output is given by

$$\begin{aligned} Z_T &= \frac{v_{out}}{i_i} = \frac{v_{out}}{v_i}\frac{v_i}{i_i} \\ &= \frac{nk + g_{m2}[R_L + j\omega(1-k^2)L_L]}{1 + j\omega C_L[R_L + j\omega(1-k^2)L_L]} \cdot \frac{1}{Y_I} = \frac{\frac{nk}{R_L + j\omega(1-k^2)L_L} + g_{m2}}{D}, \end{aligned} \tag{3.14}$$

$$\begin{aligned} D = &\left(j\omega C_I + \frac{1}{j\omega L_I + R_I}\right)\left(j\omega C_L + \frac{1}{j\omega(1-k^2)L_L + R_L}\right) \\ &+ g_{m2}\left(j\omega C_L + \frac{1-nk}{j\omega(1-k^2)L_L + R_L}\right) + \frac{j\omega n^2 k^2 C_L}{j\omega(1-k^2)L_L + R_L}. \end{aligned} \tag{3.15}$$

Around $\omega = 1/\sqrt{L_I C_I} = 1/\sqrt{L_L C_L}$, the first term in Eq. (3.15) is approximated by zero:

$$D \approx g_{m2}\left(j\omega C_L + \frac{1-nk}{j\omega(1-k^2)L_L}\right) + \frac{n^2 k^2 C_L}{(1-k^2)L_L}, \tag{3.16}$$

where R_I and R_L are ignored for simplicity. The magnitude of Z_T becomes a maximum when the first term in Eq. (3.16) equals zero. The voltage gain of the LNA and its peak frequency can be therefore expressed as

$$A_{v,LNA} = \left|\frac{v_{out}}{v_{in}}\right| = \left|\frac{i_i Z_T}{v_{in}}\right| = \left|\frac{g_{m1} Z_T}{j\omega_0 C_{gs1} R_s \cdot \mathrm{Re}[\alpha_M]}\right|, \tag{3.17}$$

$$\omega_p \approx \frac{1}{\sqrt{\frac{1-k^2}{1-nk} L_L C_L}}, \tag{3.18}$$

respectively. Equations (3.17) and (3.18) show that the magnitude and peak frequency of the voltage gain decrease with increasing k. Figure 3.5 shows the calculated $A_{v,LNA}$ with k as a parameter. The increase of k shifts the gain peak toward a lower frequency and reduces the gain magnitude. The peak frequency in Fig. 3.5 corresponds well to that calculated from Eq. (3.18).

The LNA with the magnetic coupling sacrifices a maximum voltage gain to achieve the target peak frequency, $\omega_{p,t}$. Equation (3.18) gives the following condition:

$$L_L = L_I = \frac{1}{\omega_{p,t}^2(1+k)C_L} \quad (\text{for } n = 1). \tag{3.19}$$

A turns ratio of one provides the smallest chip area of the transformer, because L_L and L_I simultaneously decrease with increasing k. Equation (3.19) shows that a smaller L_I and L_L are required to achieve $\omega_{p,t}$ as k increases. Reducing L_I and L_L leads to a smaller chip area, but to a decrease in the parallel impedances of the internal and load LC tanks at the resonance frequencies ($Z_p \approx (\omega_0 L_{I,L})^2/R_{I,L}$), causing a lower voltage gain. Figure 3.6 shows the calculated $A_{v,LNA}$ for $f_{p,t} = 5.0$ GHz where L_L and L_I satisfy Eq. (3.19). A peak frequency of approximately 5.0 GHz can be achieved even for a large k, while the maximum gain decreases with increasing k ($A_{v,LNA} \propto (1+k)^{-2}$). However, a small coupling factor such as 0.2 is acceptable for the LNA, due to a small gain reduction of 3 dB.

3.3.3 Noise

The transformer reduces the output noise originating from the common-gate transistor and the parasitic resistance of L_L, thereby improving the noise performance. Figure 3.7 conceptually illustrates how the transformer reduces the drain noise current of M_2, represented by i_{nd2}. The primary (internal) inductor L_I detects i_{nd2}, and then induces a noise voltage to the secondary (load) inductor L_L. The induced noise voltage is correlated and anti-phase to the output noise voltage produced by i_{nd2} flowing through L_L, reducing the output noise caused by M_2. The other output noise originating from L_L is also reduced by the transformer in the same way.

The magnetic coupling affects the noise contributions from M_2, L_I, and L_L to the LNA (F_{M_2}, F_{L_I}, and F_{L_L}, respectively), but not that from M_1 (F_{M_1}). The LNA noise factor is given by

$$F = 1 + F_{M_1} + F_{M_2} + F_{L_I} + F_{L_L}, \tag{3.20}$$

$$F_{M_1} \approx \frac{\gamma_1\chi_1}{\alpha_1} g_{m1} R_s \left(\frac{\omega_0}{\omega_{T_1}}\right)^2 + \frac{\alpha_1\delta_1}{\kappa_1 g_{m1} R_s}, \tag{3.21}$$

$$\chi_1 = (1+\alpha_{gd1})^2 - 2|c|\alpha_1\sqrt{\frac{\delta_1}{\kappa_1\gamma_1}}(1+\alpha_{gd1}) + \frac{\delta_1\alpha_1^2}{\kappa_1\gamma_1}, \tag{3.22}$$

$$F_{M_2} \approx 4\left|\frac{Y_I}{Y_0+Y_I}\right|^2 \frac{\gamma_2}{\alpha_2} g_{m2} R_s \left(\frac{\omega_0}{\omega_{T_1}}\right)^2 |\alpha_M|^2 \left|\frac{(1-k)\left(1-j\frac{Y_0+Y_{L_I C_I}}{\omega_0 C_L}\right)}{k+j\frac{g_{m2}(1-k)}{\omega_0 C_L}}\right|^2, \tag{3.23}$$

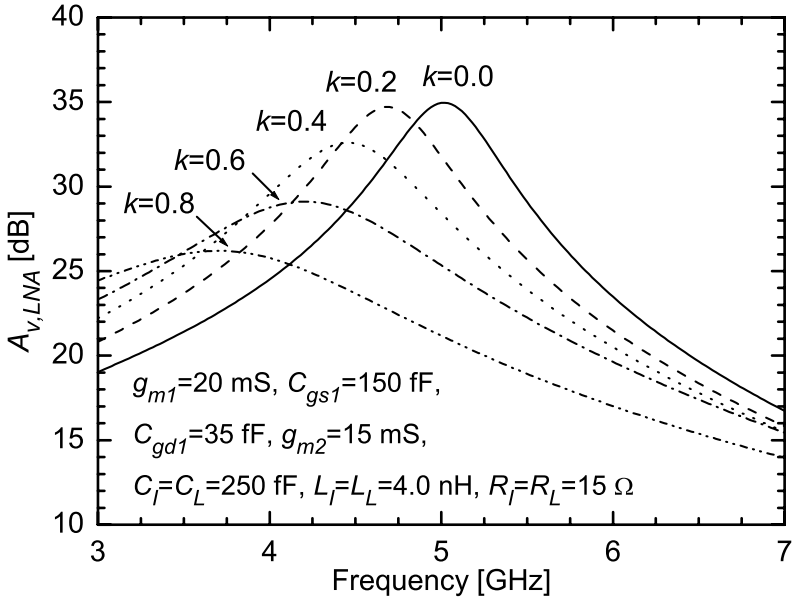

Figure 3.5: Calculated voltage gain with k as a parameter.

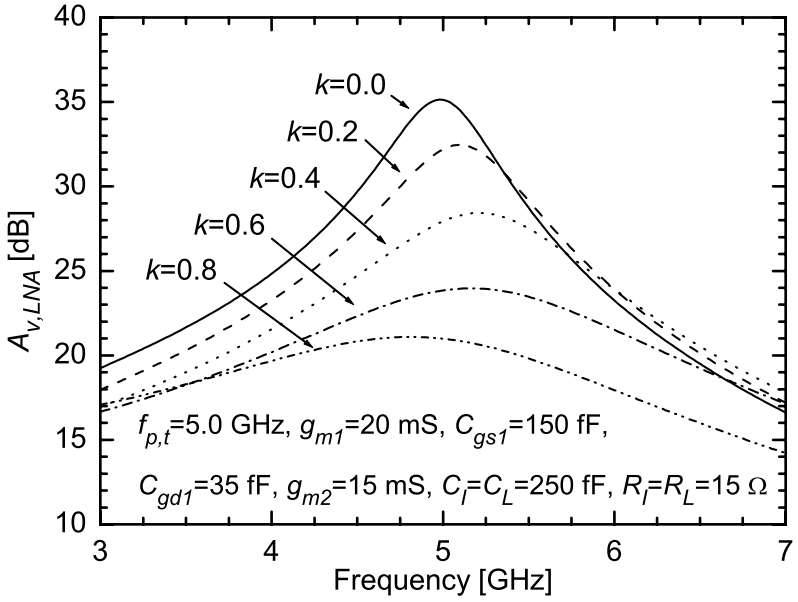

Figure 3.6: Calculated voltage gain with k as a parameter for $L_L = L_I = 1/\omega_{p,t}^2(1+k)C_L$.

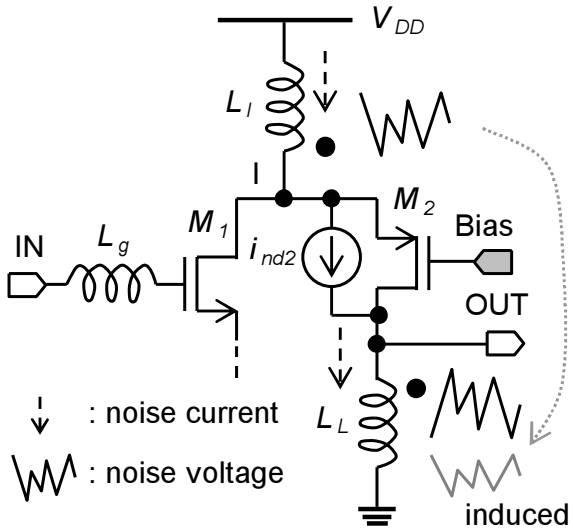

Figure 3.7: Mechanisms for noise reduction of i_{nd2}.

$$F_{L_I} \approx 4 \left| \frac{Y_I}{Y_0 + Y_I} \right|^2 R_I R_s \left(\frac{\omega_0}{\omega_{T_1}} \right)^2 |\alpha_M|^2 \left| \frac{(1-k)g_{m2} - k\left(Y_0 + j\omega_0 C_I\right)}{k + j\frac{g_{m2}(1-k)}{\omega_0 C_L}} \right|^2, \tag{3.24}$$

$$F_{L_L} \approx 4 \left| \frac{Y_I}{Y_0 + Y_I} \right|^2 R_L R_s \left(\frac{\omega_0}{\omega_{T_1}} \right)^2 |\alpha_M|^2 \left| \frac{(1-k)g_{m2} + Y_0 + Y_{L_I C_I}}{k + j\frac{g_{m2}(1-k)}{\omega_0 C_L}} \right|^2, \tag{3.25}$$

where $\alpha_i = g_{mi}/g_{d0i}$ and g_{d0i} is the zero bias drain conductance of M_i $(i = 1, 2)$; γ_i and δ_i are the drain noise current factor and the induced gate noise current factor, respectively, and c is the correlation coefficient between these noise currents ($\simeq j0.395$ [9]); κ_i is the Elmore constant (=5 [10]); $L_I = L_L = 1/\omega_0^2(1+k)C_L$; Y_0 represents the output admittance of the input stage at node I and is approximated as $j\omega C_{gd1}$; $Y_{L_I C_I} = j\omega C_I + 1/(j\omega L_I + R_I)$. The detailed derivations are summarized in Appendix A.2. Equations (3.21)–(3.25) show that F_{M_1} is independent of k while F_{M_2}, F_{L_I}, and F_{L_L} are functions of k. Figure 3.8 shows the calculated F_{M_2}, F_{L_I}, and F_{L_L} versus k. As Eq. (3.23) shows, F_{M_2} approaches zero with increasing k. Meanwhile, F_{L_I} increases and F_{L_L} slightly decreases. This difference originates from the different numerators in Eqs. (3.24) and (3.25), i.e., $-k\left(Y_0 + j\omega_0 C_I\right)$ and $Y_0 + Y_{L_I C_I}$.

The noise improvement by the transformer is limited in the folded-cascode topology. The calculated noise figure (NF, defined by $10\log F$) versus k are shown in Fig. 3.9, where 90 nm CMOS process parameters are used. The NF simulated using Agilent Advanced Design System (ADS) are also plotted. Figure 3.9 shows that the calculated NF is comparable to the simulated NF, and the magnetic coupling reduces the NF by up to 0.08 dB (calculated) or 0.12 dB (simulated) for $g_{m2} = 15$ mS. The amount of noise reduction is relatively small, because the noise of M_1 is the dominant noise source in the LNA ($F_{M_1} \simeq 1.20$ and 1.05 in the calculations and simulations, respectively).

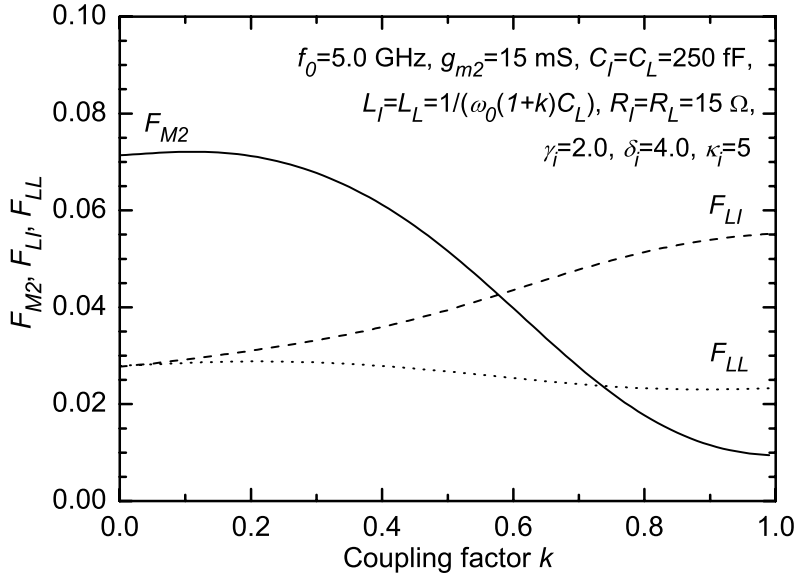

Figure 3.8: Calculated F_{M_2}, F_{R_I}, and F_{R_L} versus k.

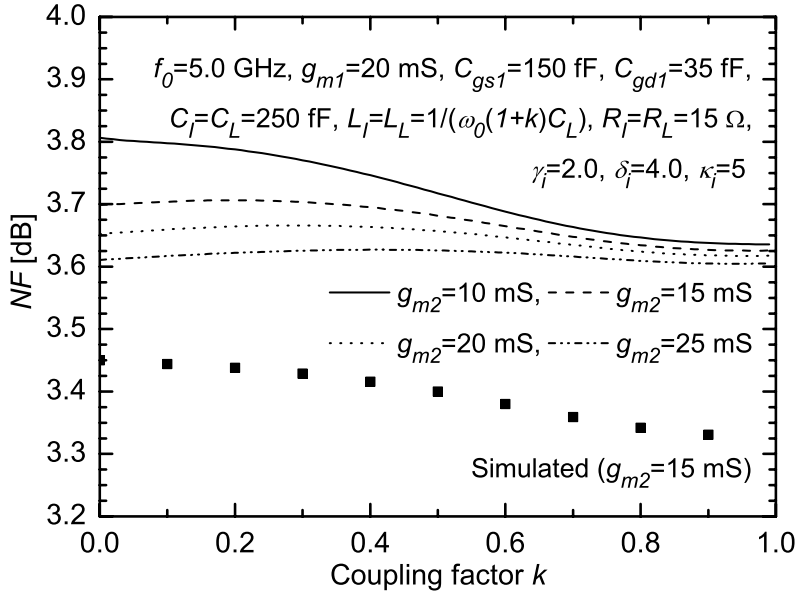

Figure 3.9: Calculated and simulated NF versus k.

3.3.4 Stability

A small L_I or large C_L ensures the stability of the LNA. The proposed LNA becomes potentially unstable, because the transformer provides a positive feedback from the output to node I, as shown in Fig. 3.1. For stability, the LNA must satisfy the following condition [11]:

$$\text{Re}[Z_{in}] > 0. \tag{3.26}$$

For $k = 1$ and low frequencies (the worst case), Re$[Z_{in}]$ is approximated as (Eq. (3.1) for $Y_I = 1/j\omega L_I$)

$$\text{Re}[Z_{in}] \approx \frac{\omega_{T1}[L_s(1+\alpha_{gd1}) - L_I\alpha_{gd1}]}{(1+\alpha_{gd1})^2 + \omega^2 L_I^2 \alpha_{gd1}^2 g_{m1}^2}. \tag{3.27}$$

Substituting Eq. (3.27) in Eq. (3.26), we have

$$L_I < L_s\left(1 + \frac{1}{\alpha_{gd1}}\right), \tag{3.28}$$

which shows that a smaller L_I ensures the stability. Using Eq. (3.19), we can rewrite the above condition as

$$C_L > \frac{1}{2\omega_{p,t}^2 L_s\left(1 + \frac{1}{\alpha_{gd1}}\right)}. \tag{3.29}$$

For example, $C_L > 160$ fF is calculated from $f_{p,t} = 5$ GHz, $L_s = 0.6$ nH, and $\alpha_{gd1} = 0.2$. This capacitance value can be satisfied with the parasitic capacitances of L_L and the input capacitance of the following stage.

3.4 Design

3.4.1 Transistors

The input transistor M_1 is designed to achieve a minimum NF at 5 GHz with a bias current I_{d1} of 1.0 mA at a supply voltage of 0.5 V. Equations (3.21) and (3.22) provide an optimum (for noise performance) gate width for M_1 of 4×40 μm (40 gate fingers, each with a unit of 4 μm width) and a minimum gate length of 100 nm. Although the calculated minimum NF is 3.6 dB for I_{d1} =1.0 mA, increasing I_{d1} leads to a lower NF (i.e., 2.2 dB for I_{d1} =2.0 mA).

The size of the common-gate transistor M_2 is selected as a compromise between noise and linearity performance. For a fixed bias current of 1.0 mA, a small gate width of M_2 provides high linearity as shown in Chapter 2, but leads to a lower g_{m2}, which results in the increase of F_{M_2}, F_{L_I}, and F_{L_L} as shown in Eqs. (3.23)–(3.25). Figure 3.9 shows less NF degradation for $g_{m2} > 15$ mS than for $g_{m2} < 15$ mS at a low k. Thus, g_{m2} is selected to be approximately 15 mS, which results in a gate width of 4×40 μm and gate length of 100 nm.

3.4.2 Transformer and Inductor

A partially-coupled transformer, shown in Fig. 3.10(a), allows us to simultaneously achieve a small chip area (0.314×0.200 mm^2) and reduce the magnetic coupling ($k \simeq 0.1$). On the other hand, a stacked transformer, shown in Fig. 3.10(b), provides a smaller chip area (0.210×0.200 mm^2), thereby reducing the cost. However, a large k of the stacked transformer ($k \simeq 0.9$) leads to poor gain, and does not significantly reduce the NF of the LNA, as shown in Section 3.3.3. Figure 3.11 shows the ADS simulated voltage gain and NF of the LNAs employing the transformers shown in Figs. 3.10(a) and (b). The transformers were designed using a three-dimensional (3-D) electromagnetic simulator (Ansoft HFSS), and L_s and L_g in both the LNAs were adjusted to achieve an S_{11} of less than -10 dB at 5 GHz. The LNA with the stacked transformer had 13 dB lower gain than the LNA with the partially-coupled transformer at 5 GHz. This leads to an increase in the overall NF of the receiver. A larger k also leads to an increase in the voltage swing at node I (Fig. 3.1), causing poor reverse isolation. Simulations (not shown) showed degradation of approximately 10 dB in the reverse isolation performance (S_{12}) of the LNA with the stacked transformer.

The inductances of the transformer are selected to resonate at a frequency of approximately 5 GHz. The outer diameter of each inductor is 200 μm, the metal width 7 μm, and the metal spacing 2 μm. Electromagnetic simulations resulted in $L_I = L_L = 3.6$ nH and quality factors (Q) of 6.7 at 5 GHz.

The inductances of L_s and L_g are determined by the input impedance matching conditions, derived from Eqs. (3.6)–(3.8): $L_s \simeq 0.8$ nH and $L_g \simeq 4.3$ nH. The outer diameter of L_g is 200 μm, the metal width 5 μm, and metal spacing 2 μm. The simulated Q of L_g was 7.5 at 5 GHz.

3.5 Experimental Results and Discussion

The designed LNA with the partially-coupled transformer shown in Fig. 3.12 was fabricated in a 90 nm digital CMOS process with seven metal layers including a 1.9-μm thick metal layer and without metal-insulator-metal (MIM) capacitors. For comparison, a conventional folded-cascode LNA with the same device sizes except the magnetic coupling as in Fig. 3.12 was also fabricated on the same chip. A micrograph of the fabricated LNAs is shown in Fig. 3.13. The active chip areas (without the pads) of the proposed and conventional LNAs were 0.39×0.55 mm^2 and 0.52×0.55 mm^2, respectively. The input and output pads were not electrostatic-discharge (ESD) protected. Metal fills consisting of metal 1–6 layers were placed both inside and outside the fabricated transformer and inductors to meet metal density rules in the CMOS process. They were 1.5 μm by 1.5 μm squares with a spacing of 0.2 μm. For the measurements, a unity-gain common-source amplifier with a 50 Ω output resistor was used as a buffer, shown in Fig. 3.12. The S-parameters, noise, and linearity of the LNAs were measured using on-wafer RF probes. The power consumption of each LNA and the buffer were 1.0 mW and 1.8 mW at a supply voltage of 0.5 V, respectively.

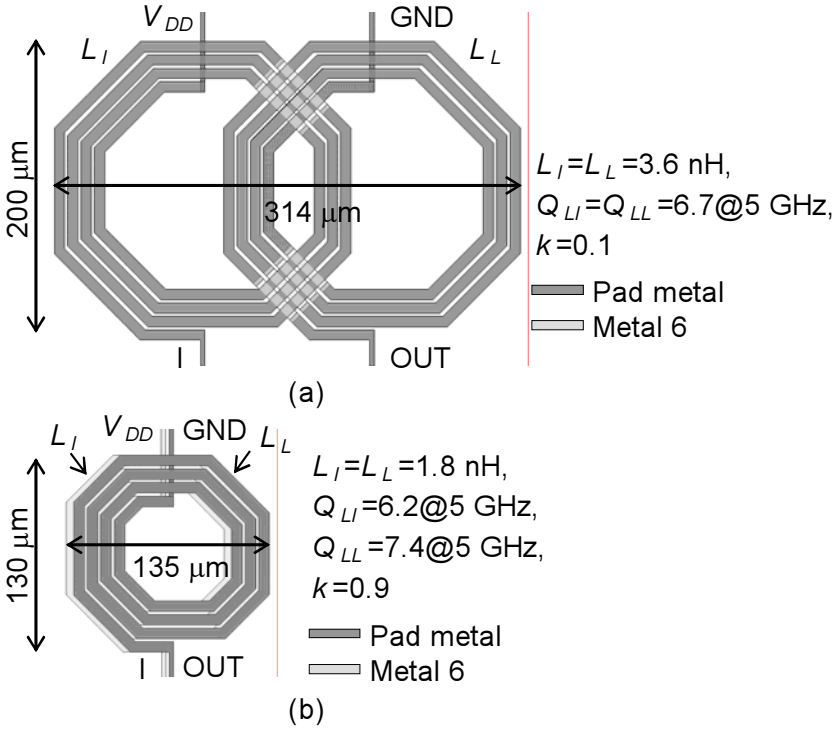

Figure 3.10: Layout of (a) a partially-coupled transformer and (b) a stacked transformer.

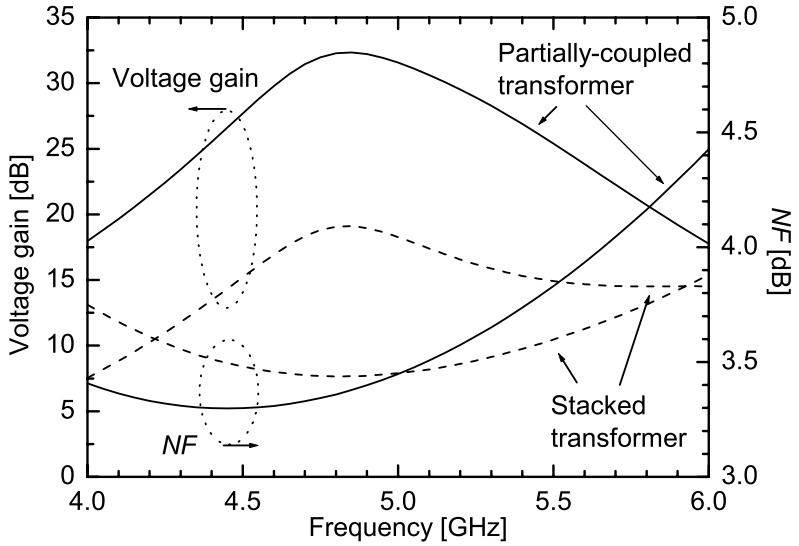

Figure 3.11: Simulated voltage gain and NF of LNAs employing the partially-coupled transformer (solid line) and stacked transformer (dashed line).

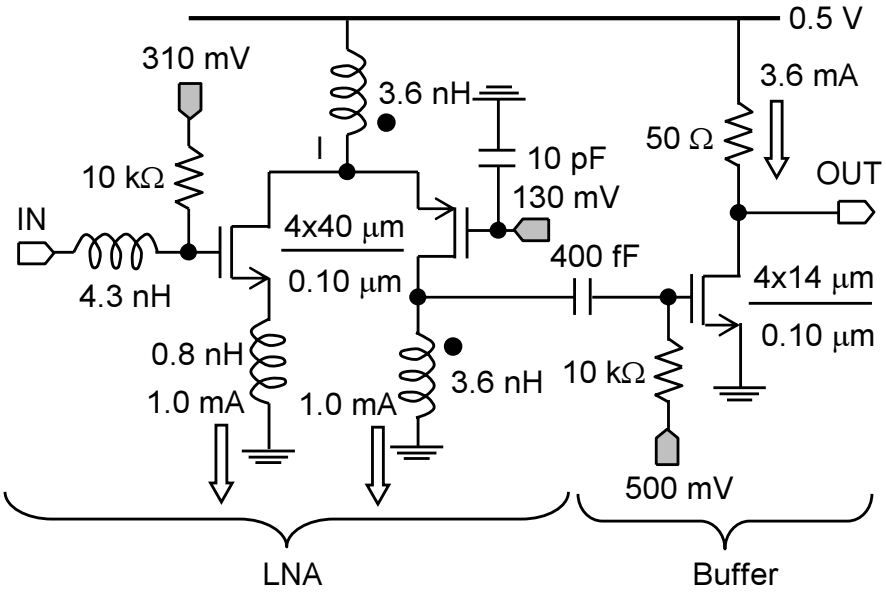

Figure 3.12: Complete schematic of the designed transformer folded-cascode LNA.

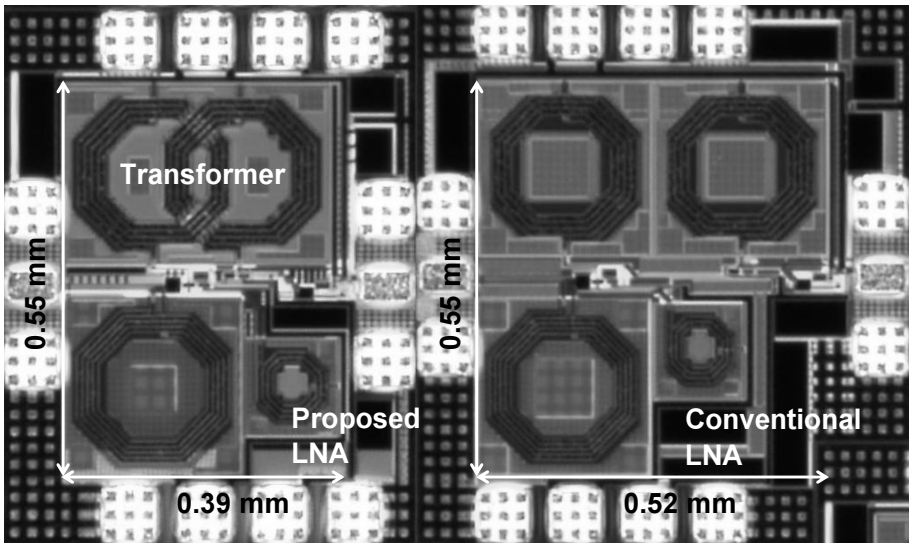

Figure 3.13: Micrograph of the proposed LNA (left) and conventional folded-cascode LNA (right).

3.5.1 S-parameters

Figures 3.14 and 3.15 show the measured and simulated S_{11} and S_{21} of the fabricated LNAs, respectively. The S-parameters were measured using an Agilent Technologies HP8722ES network analyzer. The proposed LNA obtained an S_{11} of less than -10 dB around 5 GHz and a maximum S_{21} of 16.8 dB at 4.7 GHz. The magnetic coupling in the proposed LNA had a small impact on the S_{11} performance, while the measured peak of S_{21} was shifted to a lower frequency than the simulated one, due to the increased magnetic coupling of the fabricated transformer ($k \simeq 0.2$). This frequency shift can be reduced by using a smaller L_I and L_L (3.4 nH).

The discrepancy between the measured and simulated S_{21} is mainly attributed to insufficient accuracy in the simulation of the inductors used. The HFSS simulation models of the transformer and inductors included no metal fills to solve convergence problems and reduce the memory requirement. The metal fills decrease the quality factors of the transformer and inductor [12–14], which results in a lower gain.

Figures 3.16 and 3.17 show the measured and simulated S_{12} and S_{22} of the LNAs with the buffers, respectively. The propose LNA with the buffer achieved an S_{12} of -47 dB at 5.0 GHz, while the stand-alone buffer obtained an S_{12} of -30 dB at 5.0 GHz (not shown). Thus, the S_{12} of the proposed LNA without the buffer was approximately -17 dB. Figure 3.16 also shows that the inductor coupling deteriorates the reverse isolation by a factor of 12 dB at 5 GHz, compared to the conventional LNA. This deterioration is not problematic, because the proposed LNA still has good isolation, due to the folded-cascode topology. Both the LNAs achieved an S_{22} of less than -10 dB around 5.0 GHz as shown in Fig. 3.17.

3.5.2 NF

Figure 3.18 shows the measured and simulated NF of the LNAs. The NF was measured using an Agilent Technologies HP8970B noise figure meter. The proposed LNA obtained a minimum NF of 3.9 dB at 4.7 GHz, while the conventional LNA achieved a minimum NF of 4.1 dB at the same frequency. The difference between the measured minimum NF can be attributed to more input-referred noise of the buffer in the conventional LNA than that in the proposed LNA. The LNAs had different values of S_{21} at 4.7 GHz, resulting in different input-referred noise of the buffer.

3.5.3 Linearity

Figure 3.19 shows the measured output power of the fundamental tone and third-order intermodulation (IM_3) products for two tones (4.999 GHz and 5.000 GHz), applied to the LNA. The two tones were generated by Agilent Technologies HP8671B and E4438C signal generators, and the fundamental and IM_3 tones were measured using an Agilent Technologies E4448A spectrum analyzer. The measured IIP_3 of the proposed LNA with the buffer was -18.5 dBm, and that of the stand-alone buffer was -0.25 dBm (not shown). The IIP_3 of the LNA without the buffer can be calculated from Eq. (2.49). Substituting $IIP_{3,LNA+Buf} = -18.5$ dBm, $IIP_{3,Buf} = -0.25$ dBm

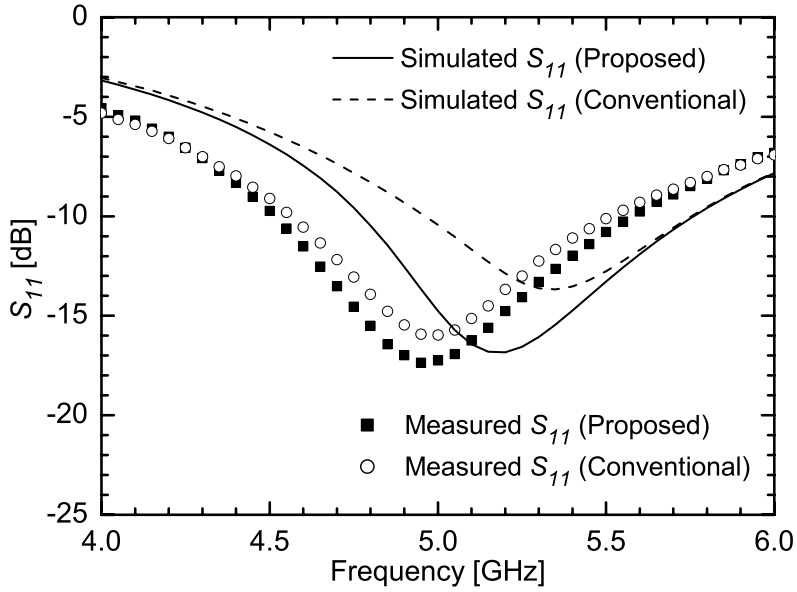

Figure 3.14: Measured and simulated S_{11} of the LNAs.

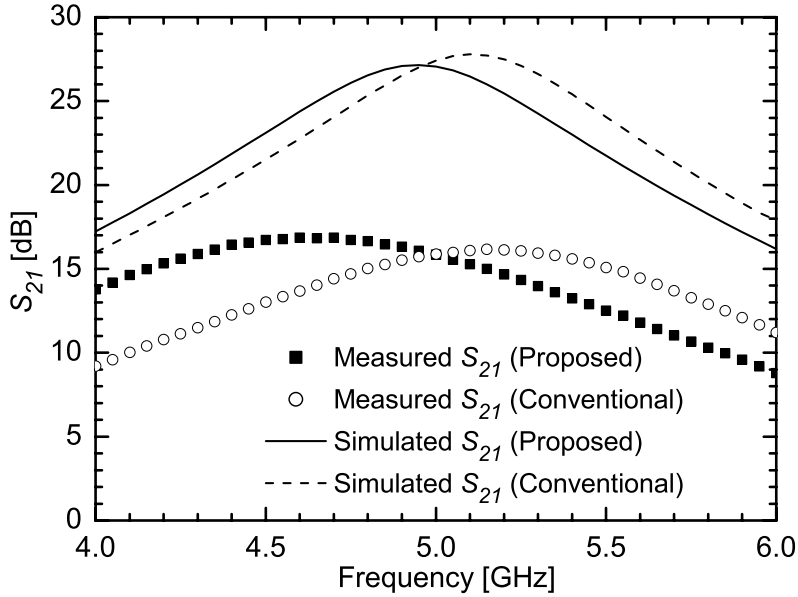

Figure 3.15: Measured and simulated S_{21} of the LNAs.

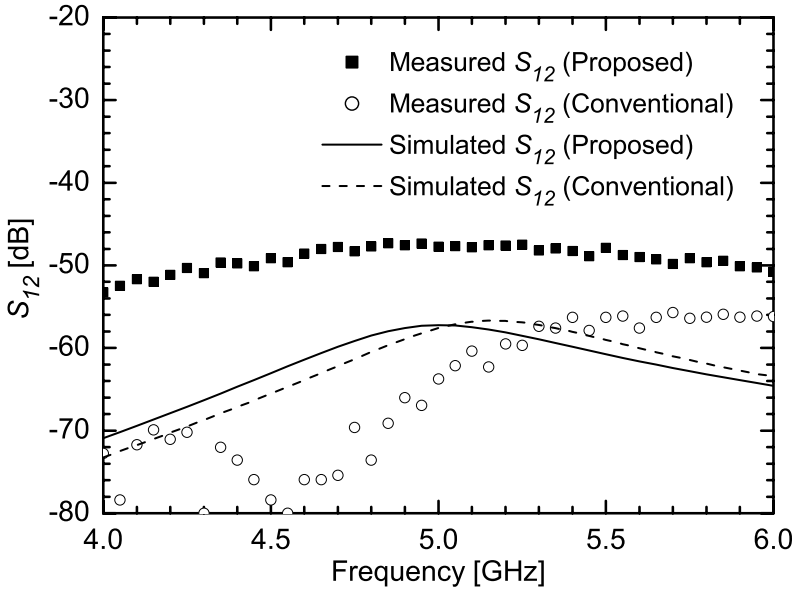

Figure 3.16: Measured and simulated S_{12} of the LNAs.

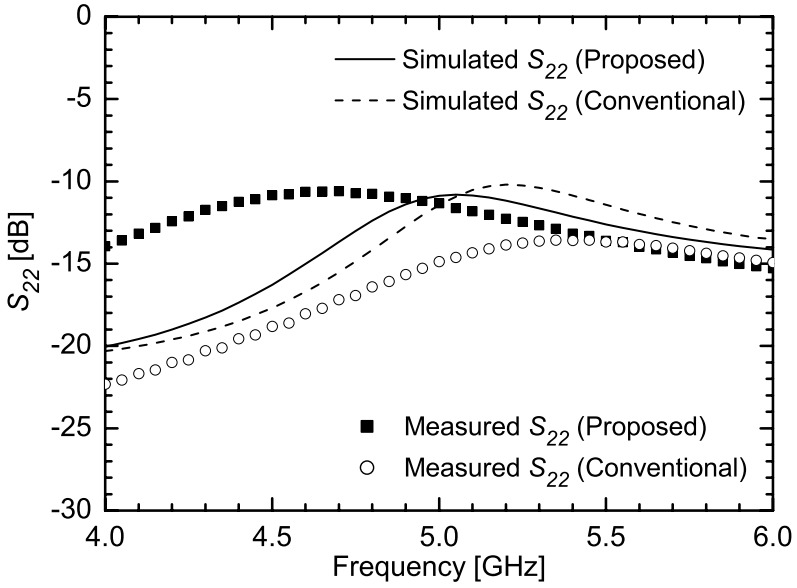

Figure 3.17: Measured and simulated S_{22} of the LNAs.

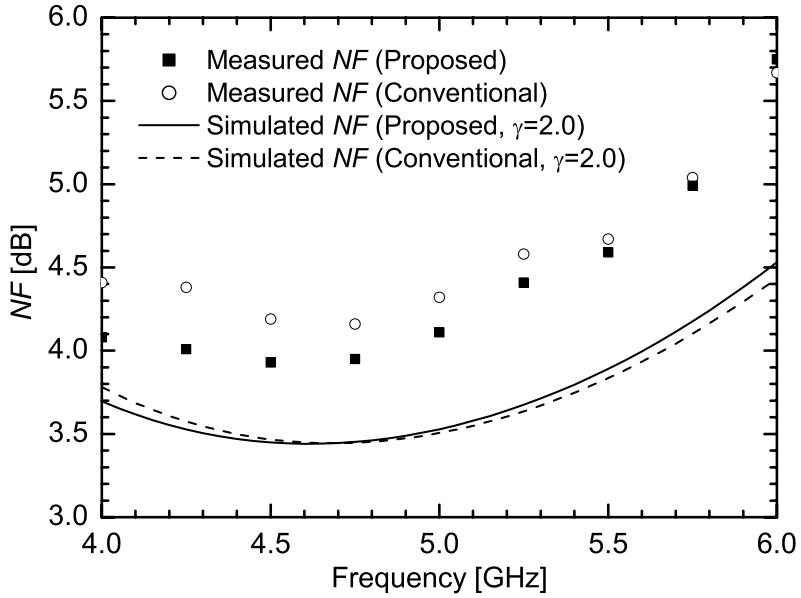

Figure 3.18: Measured and simulated NF of the LNAs.

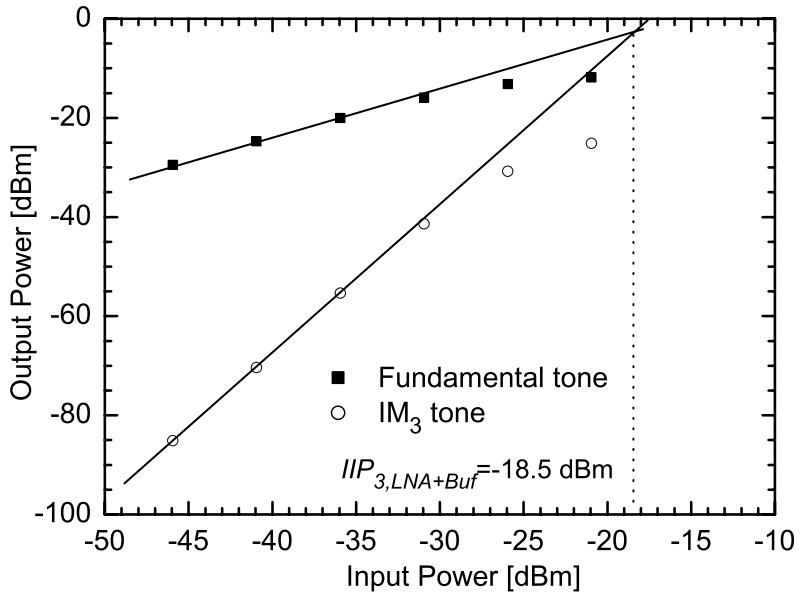

Figure 3.19: Measured IIP_3 of the proposed LNA with the buffer.

and $A_{v,LNA} = 15.8$ dB (at 5.0 GHz) into Eq. (2.49) gives $IIP_{3,LNA} = -14.8$ dBm. The IIP_3 of the conventional LNA was also -14.8 dBm.

3.5.4 Comparison

Table 3.1 shows a summary of the LNA performance and a comparison with previously reported low-voltage ($\sim$0.6 V) CMOS LNAs for 5 GHz applications. The proposed LNA achieved performance comparable to the conventional folded-cascode LNA, while consuming three fourths of the chip area of the conventional LNA. The figure of merits for the LNAs, FoM_1 and FoM_2, included in Table 3.1, are defined by Eqs. (2.50) and (2.51), respectively. The proposed LNA obtained the best FoM_1 (4.8 mW^{-1}) with the smallest chip area among the reported low-voltage CMOS LNAs, whereas it achieved a lower FoM_2 than that of the LNA reported in [3], due to a lower IIP_3.

3.6 Conclusion

This chapter has demonstrated a transformer folded-cascode CMOS LNA, in which the internal and load inductors have been magnetically coupled to reduce the chip area. Circuit analysis showed that the magnetic coupling between these inductors decreases the resonance frequency of the input matching network, the peak frequency and magnitude of the gain, and the noise figure. The partially-coupled transformer reduced the chip area, while having a small impact on the LNA performance. The LNA implemented with a 90 nm CMOS technology occupied 0.21 mm^2 and achieved an S_{11} of -14 dB, NF of 3.9 dB, and voltage gain of 16.8 dB at 4.7 GHz with a power consumption of 1.0 mW from a 0.5 V supply. The chip size of the proposed LNA was 25$\%$ smaller than that of the conventional folded-cascode LNA. It has been demonstrated that the proposed LNA can replace conventional low-voltage CMOS LNAs.

Table 3.1: Measured performance and comparison of low-voltage CMOS LNAs.

Reference	CMOS Technology	Frequency [GHz]	NF [dB]	S_{21} [dB]	IIP_3 [dBm]	$P_{\text{in-1 dB}}$ [dBm]	Supply [V]	Power [mW]	Area [mm^2]	FoM_1 [mW^{-1}]	FoM_2 [–]
This work	90 nm	4.7	3.9	16.8	-14.8	-27	0.5	1.0	0.21	4.8	0.74
Folded-cascode	90 nm	5.0	4.1	16.1	-14.8	-27	0.5	1.0	0.29	4.1	0.67
[3]	90 nm	5.5	3.6	9.2	-7.25	-15.8	0.6	1.0	0.30	2.2	2.31
[4]	180 nm	5.8	2.9	7.0	N/A	-9	0.7	12.5	0.40	0.2	N/A
[5]	130 nm	5.1	5.3	10.3	N/A	-22	0.4	1.0	0.75	1.4	N/A
[6]	180 nm	5.0	4.5	9.2	-16	-27	0.6	0.9	0.54	1.8	0.22
[15]	180 nm	5.0	3.65	14.1	-17.1	-25	0.6	1.68	0.46	2.3	0.22

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Chapter 4

Transformer Noise-Canceling UWB CMOS LNA

4.1 Introduction

The ultra-wideband (UWB) technology has attracted much interest in recent years, because of its ability to realize high-speed wireless personal area networks (WPANs), in which electronic devices are required to transfer large amounts of data, such as audio or video files, at a high data transfer rate. UWB frequency bands assigned from 3.1 to 10.6 GHz (Fig. 4.1) are utilized by two different communication systems: multiband orthogonal frequency division multiplexing (MB-OFDM) UWB [1] or single-carrier direct sequence (DS) UWB [2]. The MB-OFDM UWB system using 14 sub-bands, each with a bandwidth of 528 MHz, transmits signals modulated by OFDM in the subband. The data rate is up to 480 Mbps. The DS-UWB system spreads the spectrum over the low band (3.1–4.85 GHz) or high band (6.2–9.7 GHz), and provides a maximum data rate of 1320 Mbps. In either case, wideband low-noise amplifiers (LNAs) are essential for the RF front-ends of UWB receivers.

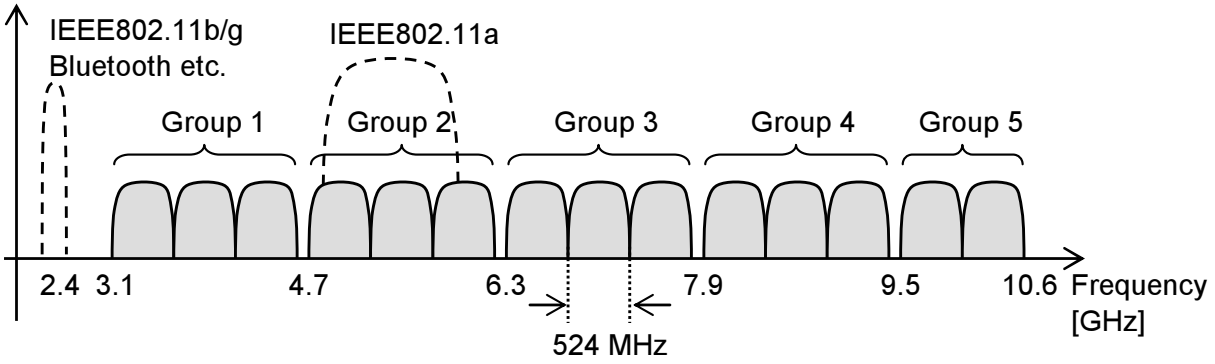

Figure 4.1: UWB frequency bands

The UWB LNA must meet several stringent requirements: input impedance matching, low noise performance, and sufficient gain across 3.1–10.6 GHz at low power consumption, low supply voltage, and low cost (i.e., small area and requiring no additional layers). In addition, it is desirable to implement the LNA with digital CMOS technologies for the integration of RF front-ends and digital circuits. Although several wideband CMOS LNAs have been proposed in recent years, none of them have simultaneously met all these requirements. An LNA with wideband LC matching networks [3] consumes a large chip area. Although resistive-feedback LNAs [4–6] and common-drain feedback LNAs [7, 8] occupy small chip areas, they require high power consumption and high supply voltages to simultaneously achieve wideband input impedance matching and low noise performance. A reactive-feedback LNA [9, 10] demands two thick metal layers to form a transformer that provides a reactive feedback. Noise-canceling LNAs [11–14] require additional circuits and power consumption. Distributed LNAs [15, 16] consume much higher power and larger areas than other LNAs.

This chapter proposes a transformer noise-canceling common-gate LNA employing an output series inductor [17]. The proposed LNA is suitable for low-power and low-voltage operation, and achieves $|S_{11}| < -10$ dB, $NF < 4.4$ dB, and $|S_{21}| > 9.3$ dB across 3.1–10.6 GHz. This chapter is organized as follows. Section 4.2 describes previously proposed wideband CMOS LNAs and their drawbacks. Section 4.3 shows the proposed circuit topology and the noise cancellation mechanisms. The noise, input admittance, gain, stability, and group delay of the proposed LNA are analyzed in Section 4.4. Section 4.5 describes the design methodology for the LNA. Section 4.6 shows the measurements of the LNA implemented in a 90 nm digital CMOS process, and Section 4.7 concludes the chapter.

4.2 Wideband CMOS LNAs

Wideband CMOS LNAs can be generally categorized into two types: common-source (CS) LNAs, and common-gate (CG) LNAs. LC matching networks or feedback techniques allow the CS LNAs to achieve wideband input bandwidth. Feedback techniques applied to CS LNAs can be divided into three categories: resistive feedback, reactive feedback, and common-drain feedback. A gm-boosting or noise-canceling technique is employed to CG LNAs for noise reduction.

4.2.1 Common-Source LNAs

Input Matching Network

Input LC matching networks based on Chebyshev or Butterworth configurations are used for CS LNAs to achieve wideband impedance matching [3]. However, they require several high-Q inductors: four inductors in an LNA employing the input matching network based on the fifth-order Chebyshev filter [3]. The use of many inductors increases the chip area and the parasitic resistances and capacitances, causing noise and gain degradation at high frequencies.

Resistive Feedback

Resistive-feedback LNAs require high power consumption and high supply voltages to simultaneously achieve wideband impedance matching and a low NF. Figure 4.2(a) shows the basic topology of the LNA, whose input impedance is expressed as

$$Z_{in} \approx \frac{1}{sC_p} // \frac{R_f}{1+A_v}, \tag{4.1}$$

where C_p is the input parasitic capacitance, R_f the feedback resistance, and A_v the voltage gain of the LNA. Increasing R_f reduces the NF of the LNA [4], but A_v must also be increased accordingly to obtain the desired input impedance (50 Ω) as shown in Eq. (4.1). This requires high current consumption and a large load resistor and transistor, which results in a reduction of the input bandwidth. Even with a state-of-the-art CMOS technology, the resistive-feedback LNA [5] demanded 12 mW from a 1.8-V supply to achieve $NF < 2.6$ dB; the input bandwidth was limited to less than 5.0 GHz.

Common-Drain Feedback

A common-drain (CD) stage shown in Fig. 4.2(b) detects the output voltage and feeds part of the voltage back to the input, thereby producing a resistive component for the input impedance:

$$Z_{in} \approx \frac{1}{g_{m3}(1+g_{m1}R_L)} \tag{4.2}$$

where g_{m3} is the transconductance of the CD transistor M_3, and R_L is the load resistance. However, the extra CD and current source transistors increase the noise and input parasitic capacitance. Hence, the topology also has difficulties in achieving wideband impedance matching and low noise performance at simultaneously low power consumption ($|S_{11}| < -10$ dB and $NF < 4.3$ dB in the frequency range of 0–6 GHz at 3.4 mW [7]).

Reactive Feedback

The input stage of the reactive-feedback LNA [9, 10] is shown in Fig. 4.2(c). The transformer connected to the gate and source of M_1 detects the source current, returning part of it to the gate. Although this topology provides $|S_{11}| < -10$ dB and $NF < 3$ dB across 3.1–10.6 GHz [9, 10], it requires a transformer with very low parasitic resistances. The input impedance of the LNA is given by [10]

$$Z_{in} \approx \frac{1}{(1+\beta)\,\beta}\left(r_{pri} + \frac{1}{g_{m1}}\right), \tag{4.3}$$

where β is the feedback factor and equals k/n, and k and n are the magnetic coupling factor and the turns ratio of the transformer, respectively; r_{pri} is the parasitic resistance of the primary inductor L_p; g_{m1} is the transconductance of M_1. For $\beta = 0.19$ [10] and $g_{m1} = 50$ mS, the upper limit on r_{pri} for $S_{11} < -10$ dB is calculated as 1.7 Ω. It is difficult to implement such

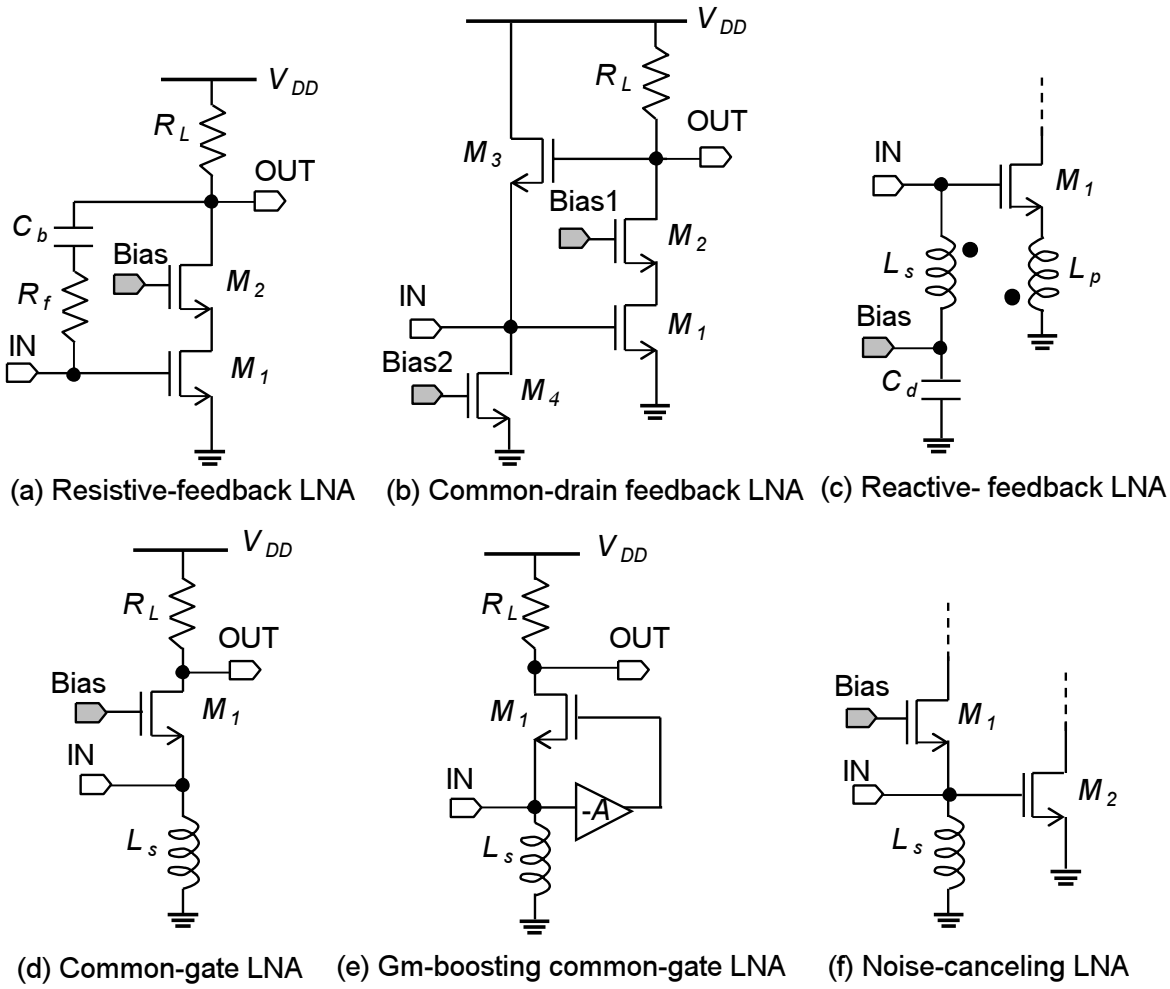

Figure 4.2: Wideband CMOS LNAs.

a primary inductor using a lower thin metal layer[1]. Increasing β and g_m alleviates the above limitation but leads to an increase in NF [10] and high power consumption, respectively. In fact, the transformer in [9,10] consisted of two thick metal layers (3–4 μm). An additional thick metal layer increases the fabricating cost.

4.2.2 Common-Gate LNAs

The CG LNA (Fig. 4.2(d)) is suitable for wideband and low-voltage operation, because it has a low quality factor of the input network and does not require a cascode transistor to alleviate

[1]The secondary inductor, stacked on the primary one, must be implemented with a top thick metal layer for low noise performance [10].

the Miller effect from the CG transistor M_1 [18]. The main drawback of the LNA is poor noise performance. The noise factor is given by

$$F \approx 1 + \gamma + \frac{4R_s}{R_L}, \tag{4.4}$$

where R_s is the input signal source resistance. The coefficient of the channel thermal noise in the MOSFET, γ, equals $2/3$ in long-channel MOSFETs, but exceeds this value in short-channel MOSFETs [19–21]. For $\gamma = 2$, $R_L = 200\ \Omega$, and $R_s = 50\ \Omega$, the NF is calculated as approximately 6.0 dB, which is unacceptable for wideband LNAs.

Gm-Boosting Technique

A gm-boosting technique [18] reduces the noise factor contributed from M_1 by a factor of $(1+A)$:

$$F \approx 1 + \frac{\gamma}{1+A} + \frac{4R_s}{R_L}, \tag{4.5}$$

where A, shown in Fig. 4.2(e), is an inverting gain and assumed to be noiseless. An additional circuit providing A is required for practical use of the technique. A differential capacitor cross-coupling topology [22, 23] provides $A \simeq 1$ ($NF \simeq 4.8$ dB), but requires an external wideband balun. A transformer-coupled topology [24], which provides $A > 1$, is not suitable for wideband operation, due to a larger effective C_{gs}, which becomes more than four times as large as that of the CG LNA.

Noise-Canceling Technique

A noise-canceling technique based on [25] has also been applied to the CG LNA for noise reduction [11–13]. This technique cancels the noise of the CG transistor using an additional CS one (Fig. 4.2(f)). However, the noise of the CS transistor is not canceled, and hence the NF of this LNA is less than or comparable to that of the CG LNA, even with higher power consumption and a larger chip area.

4.3 Transformer Noise-Canceling LNA

This section presents the circuit topology of the transformer noise-canceling LNA and the noise cancellation mechanisms.

4.3.1 Circuit Topology

Figure 4.3 shows a schematic of the proposed LNA, based on a CG LNA with a shunt-peaking inductor. The main difference between the proposed LNA and the CG LNA is that the input and shunt-peaking inductors, L_p and L_s, are magnetically coupled to form a transformer. A similar

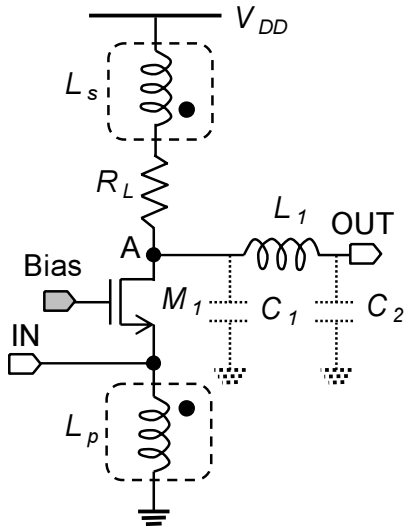

Figure 4.3: Schematic of the proposed LNA.

topology has been reported for narrowband applications [26]. The transformer reduces the noise of M_1 and the load resistor R_L, thereby improving the noise performance without additional circuits or increased power consumption. The transformer also provides a positive feedback, whose mechanism is as follows: An output current generated by a signal voltage flows through L_s, which induces a voltage that is in phase with the signal voltage to L_p. The output series inductor L_1 forms a π network with the parasitic capacitances, C_1 and C_2, extending not only the gain bandwidth, but also the input bandwidth. The chip area of the proposed LNA is the same as that of the CG LNA with the shunt-peaking inductor, because L_p can be stacked on L_s, i.e., a stacked transformer, which occupies the area of one inductor.

4.3.2 Noise Cancellation

The transformer partly cancels the output noise originating from the CG transistor M_1 and load resistor R_L, thereby improving the LNA noise performance. The small-signal circuit of the proposed LNA are shown in Fig. 4.4, where the voltage supply terminal (V_{DD}) is connected to the AC ground; the noise of the signal source resistance R_s, M_1, and R_L are represented by the noise current sources i_{ns}, i_{nd}, and noise voltage source v_{nR_L}, respectively; M, given by $k\sqrt{L_pL_s}$, is the mutual inductance of the transformer and k the magnetic coupling factor; C_p represents the sum of the gate-source capacitance of M_1 and the parasitic capacitances of the input pad and L_p; Z_L is the load impedance considering the right hand side of output node A. The mechanisms for the noise cancellation are conceptually illustrated in Figs. 4.5(a) and (b). The transformer detects noise currents flowing through the primary (or secondary) inductor L_p, inducing voltages correlated with the currents to the secondary (or primary) inductor L_s.

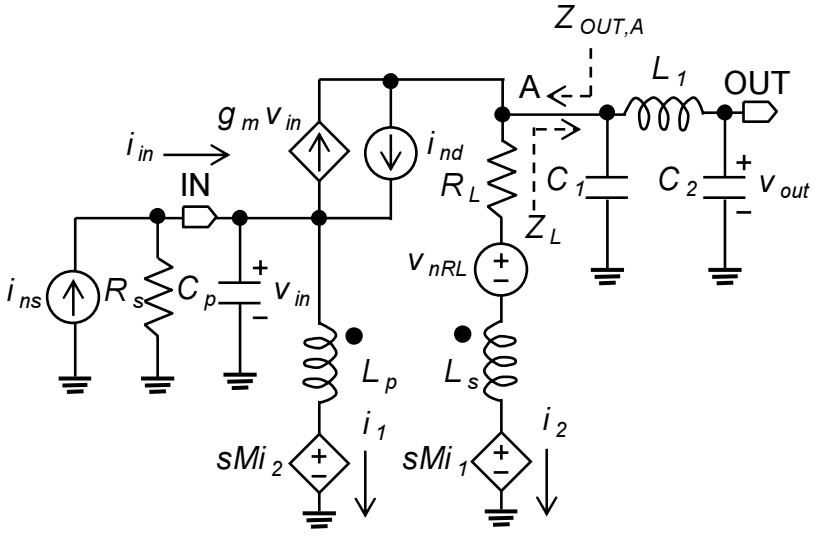

Figure 4.4: Small-signal equivalent circuit with noise sources.

Transistor Noise Cancellation

The output noise voltage generated by i_{nd} is partly canceled by the induced noise voltage originating from i_{nd} flowing through L_p, as shown in Fig. 4.5(a). The noise current i_{nd} first flowing through L_s and R_L generates a noise voltage $v_{n1} = -i_{nd}(R_L + sL_s)$, and then a noise voltage $v'_{n1} = -i_{nd} \cdot sM$ is induced to L_p. Next, i_{nd} flows through L_p, producing a noise voltage $v_{n2} = i_{nd} \cdot sL_p$, which is canceled by v'_{n1}. Here, the transformer induces a noise voltage $v'_{n2} = i_{nd} \cdot sM$ to L_s. The induced noise voltage v'_{n2} is correlated and in antiphase with v_{n1} and hence the total output noise voltage is reduced: $-i_{nd}(R_L + sL_s - sM)$. The expression of the output noise voltage (at node A) including the effect of Z_L can be derived from Fig. 4.4:

$$v_{out,i_{nd}} = -Z_L \frac{n^2k^2 - nk + \left(\frac{1}{R_s} + sC_p + \frac{1}{sL_p}\right)(R_L + s(1-k^2)L_s)}{\left(\frac{1}{R_s} + Y_{IN}\right)(Z_L + R_L + s(1-k^2)L_s)}, \tag{4.6}$$

where $n = \sqrt{L_s/L_p}$ is the turn ratio of the transformer; $Y_{IN} = i_{in}/v_{in}$, described in the next section, is the input admittance of the LNA, and i_{in} and v_{in} are the input current and voltage, respectively, as shown in Fig. 4.4. The term of $s(1-k^2)L_s$ in the numerator of Eq. (4.6) shows that the transistor noise is partly canceled by the transformer.

Load Resistor Noise Cancellation

The CG transistor M_1 drains a part of the output noise current originating from v_{nR_L}, reducing the output noise voltage, as shown in Fig. 4.5(b). The noise current due to v_{nR_L}, which is given by $v_{nR_L}/(sL_s + R_L + Z_L)$, first flows through L_s and then the transformer induces a noise voltage

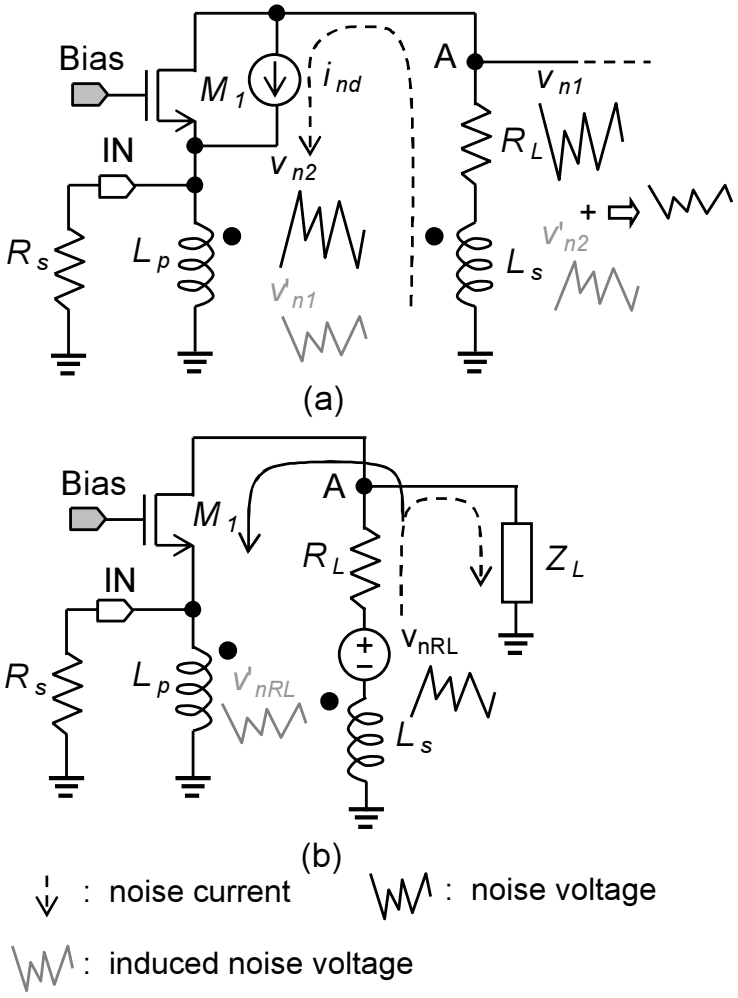

Figure 4.5: Mechanisms for noise cancellation of (a) i_{nd} and (b) v_{nR_L}.

$v'_{nR_L} = -sMv_{nR_L}/(sL_s + R_L + Z_L)$ to L_p. The transistor M_1 detects a gate-source voltage $v_{gs} = v'_{nR_L}/sL_p(1/R_s + g_m + sC_p + 1/sL_p)$, and drains noise current of $g_m v_{gs}$ accordingly. This results in a reduction of the output noise current originating from v_{nR_L}. Considering the noise current due to M_1, we can obtain the output noise current flowing Z_L:

$$i_{out,v_{nR_L}} = \frac{\left(\frac{1}{R_s} + (1-nk)g_m + sC_p + \frac{1}{sL_p}\right) v_{nR_L}}{\left(\frac{1}{R_s} + Y_{IN}\right)(Z_L + R_L + s(1-k^2)L_s)}, \tag{4.7}$$

and the output noise voltage (at node A), $v_{out,v_{nR_L}}$, is given by $Z_L i_{out,v_{nR_L}}$. The term $-nkg_m$ in Eq. (4.7) originates from the noise cancellation.

Verification

The effectiveness of the transformer noise cancellation is verified through simulation. Figure 4.6 shows the simulated NF and NF_{min} of the proposed LNAs with and without the noise cancellation (i.e., $k = 0, 1.0$), where 90 nm CMOS process parameters are used and R_p represents the parasitic resistance of L_p. The LNA with $k = 0$ corresponds to a CG LNA with a load resistor and shunt-peaking inductor. The NF of the LNA with $k = 1.0$ is up to 2.2 dB lower than that of the LNA with $k = 0$. Figure 4.7 shows the simulated noise factors contributed from M_1, R_L, and R_p (F_{M_1}, F_{R_L}, and F_{R_p}, respectively) with and without the noise cancellation. The transformer reduces F_{M_1} by up to 35 % and F_{R_L} by 65 %. The contribution from R_p also slightly decreases and hence R_p contributes little to the overall NF (i.e., 0.1 dB in Fig. 4.6). The noise contributions from M_1 and R_L change with the turn ratio. A noise optimization procedure will be presented in the next section.

4.4 Circuit Analysis

The transformer improves the LNA noise performance at the cost of the input and gain bandwidths. The output series inductor L_1 extends both the bandwidths. In this section, the noise, input admittance, gain, stability, and group delay of the LNA are analyzed, and noise optimization and impedance matching procedures are presented.

4.4.1 Noise

The amount of noise cancellation is mainly determined by the turn ratio of the transformer. From the small-signal equivalent circuit shown in Fig. 4.4, the output noise voltage due to R_s is given by

$$v_{out,i_{ns}} = Z_L \frac{(g_m R_L + nk + s(1-k^2)L_s g_m)\, i_{ns}}{\left(\frac{1}{R_s} + Y_{IN}\right)(Z_L + R_L + s(1-k^2)L_s)}. \tag{4.8}$$

Using Eqs. (4.6)–(4.8), we obtain the noise factor of the proposed LNA:

$$F \approx 1 + F_{M_1} + F_{R_L}, \tag{4.9}$$

$$F_{M_1} = \left|\frac{v_{out,i_{nd}}}{v_{out,i_{ns}}}\right|^2 = \left|\frac{n^2 - n + \left(\frac{1}{R_s} + j\omega C_p + \frac{1}{j\omega L_p}\right) R_L}{g_m R_L + n}\right|^2 \gamma g_{d0} R_s, \tag{4.10}$$

$$F_{R_L} = \left|\frac{v_{out,v_{nR_L}}}{v_{out,i_{ns}}}\right|^2 = \left|\frac{(1-n)\, g_m R_L + \left(\frac{1}{R_s} + j\omega C_p + \frac{1}{j\omega L_p}\right) R_L}{g_m R_L + n}\right|^2 \frac{R_s}{R_L}, \tag{4.11}$$

where g_{d0} is the zero-bias drain conductance of M_1. The value of γ in a fabricated 90 nm MOSFET is approximately two, shown by the measured and simulated NF of the LNA, as will be

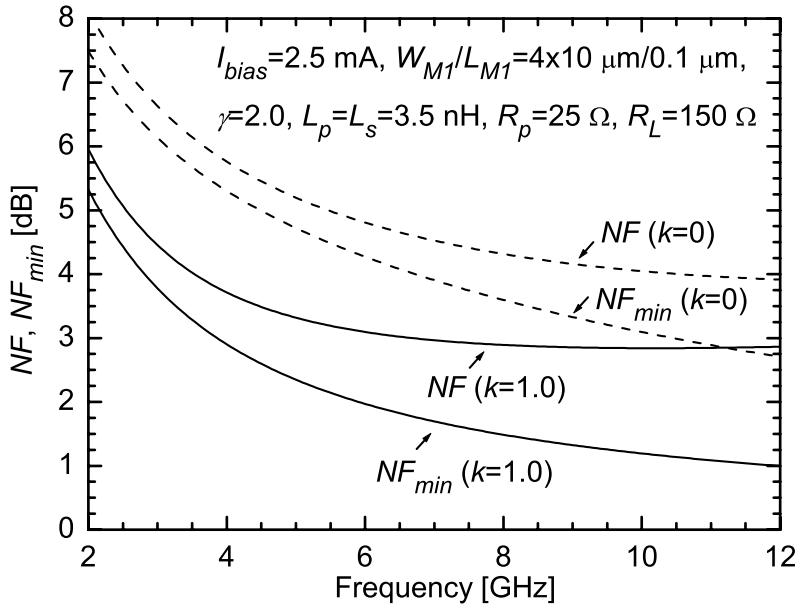

Figure 4.6: Simulated NF and $NF_{\min}$ of the LNAs with and without noise cancellation ($k = 0, 1.0$)

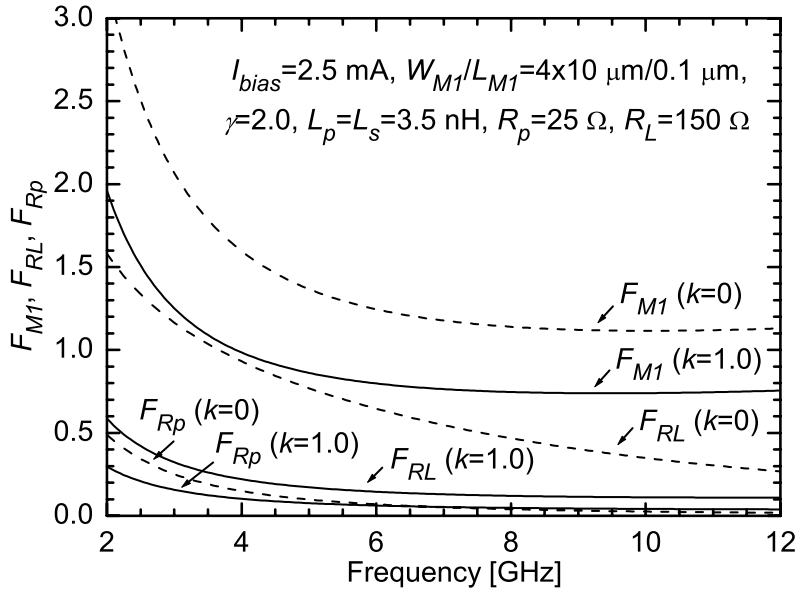

Figure 4.7: Simulated noise contributions from M_1, R_L, and R_p to the LNAs with and without noise cancellation ($k = 0, 1.0$).

shown in Section 4.6. For simplicity, the magnetic coupling factor k is assumed to be one. The parasitic resistance of L_p, the parasitic capacitance between L_p and L_s, and the induced-gate noise current of M_1 are ignored, because they do not have a significant effect on the overall NF. The transconductance g_m and load resistance R_L cannot be optimized for noise, because they are determined from input impedance matching conditions, as will be shown in the following subsection.

The optimum n for the noise performance can be obtained from Eqs. (4.9)–(4.11). Setting the derivatives of Eqs. (4.10) and (4.11) with respect to n to zero (i.e., $\partial F_{M_1}/\partial n = 0$ and $\partial F_{R_L}/\partial n = 0$ for $\omega = 1/\sqrt{L_p C_p}$), we can obtain

$$n_{opt,i_{nd}} = -g_m R_L + \sqrt{(g_m R_L)^2 + g_m R_L + \frac{R_L}{R_s}}, \tag{4.12}$$

$$n_{opt,v_{nR_L}} = 1 + \frac{1}{g_m R_s}, \tag{4.13}$$

for which a minimum F_{M_1} and F_{R_L} are achieved, respectively. Similarly, the optimum n for F, n_{opt}, can be obtained from $\partial F/\partial n = 0$:

$$\left(n_{opt}^2 - n_{opt} + \frac{R_L}{R_s}\right)\left(n_{opt}^2 + (2n_{opt} - 1)g_m R_L - \frac{R_L}{R_s}\right)\gamma g_{d0} - \left((1 - n_{opt})\, g_m + \frac{1}{R_s}\right)\left(g_m^2 R_L + g_m + \frac{1}{R_s}\right) R_L = 0. \tag{4.14}$$

Figures 4.8(a) and (b) show the calculated F, F_{M_1}, and F_{R_L} ($R_L = 50\ \Omega$) versus n and NF with R_L as a parameter at $\omega = 1/\sqrt{L_p C_p}$, respectively. For $R_L = 50\ \Omega$, minimum F_{M_1}, F_{R_L}, and F are achieved for n of 0.68, 1.66, and 1.0, given by Eqs. (4.12)–(4.14), respectively. Figure 4.8(b) shows that the calculated NF ($R_L = 150\ \Omega$) for $n = 1.0$ is consistent with the simulated NF ($k = 1.0$) at 7.2 GHz, shown in Fig. 4.6, although R_p is ignored in Eqs. (4.9)–(4.11). Moreover, the NF becomes a minimum around one even with varying R_L from 50 to 200 Ω. A large n makes the LNA unstable, as will be explained in Section 4.4.4, and leads to an increase in the parasitic capacitance of L_s, causing poor high-frequency performance. The optimum n is thus determined to be one.

4.4.2 Input Impedance Matching

In the proposed topology with input and shunt-peaking inductors coupled, the output load affects the LNA input impedance through the coupling. The output series inductor L_1 contributes to wideband input impedance matching. From Fig. 4.4, the input admittance of the proposed LNA, Y_{IN}, is given by

$$Y_{IN}(j\omega) = g_m + j\omega C_p + \frac{1}{j\omega L_p} + Y_T. \tag{4.15}$$

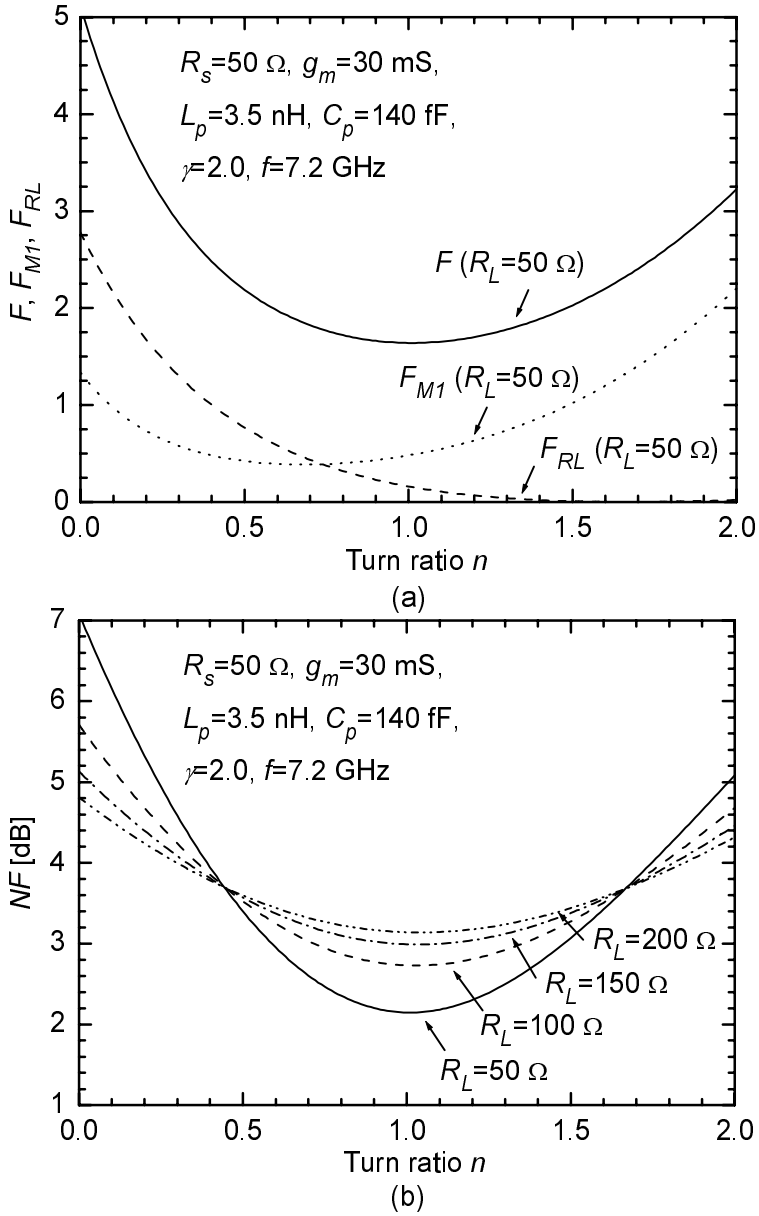

Figure 4.8: Calculated (a) F, F_{M_1}, and F_{R_L} ($R_L = 50\ \Omega$) versus n and (b) NF with R_L as a parameter.

The first three terms in Eq. (4.15) represent the input admittance of the CG LNA. The last term Y_T is generated by coupling L_p and L_s, and is given by

$$Y_T(j\omega) = \frac{nk(nk - g_m Z_L)}{R_L + Z_L + j\omega n^2 L_p(1-k^2)}. \tag{4.16}$$

When L_1 is connected in series with the output, Z_L is expressed as

$$Z_L(j\omega) = \frac{1}{j\omega C_1} // \left(j\omega L_1 + \frac{1}{j\omega C_2} \right), \tag{4.17}$$

where C_1 represents the sum of the gate-drain capacitance of M_1 and the parasitic capacitance of L_1; C_2, which is typically larger than C_1, represents the sum of the input capacitance of the following stage and the parasitic capacitance of L_1. Equations (4.15)–(4.17) show that Y_{IN} is a function of Y_T, whose frequency behavior significantly depends on that of Z_L. From Eqs. (4.15)–(4.17), the calculated frequency behavior of Y_T is shown in Fig. 4.9(a) (solid line), and that of Y_T for $Z_L(j\omega) = 1/j\omega(C_1 + C_2)$ is also shown for comparison (dashed line). The π network consisting of C_1, L_1, and C_2 acts as a short or an open [27] (i.e., $Z_L = 0$ or ∞), providing a maximum and minimum Re[$Y_T(j\omega)$] and Im[$Y_T(j\omega)$]:

$$\text{Re}[Y_T(j\omega)]_{\text{max}} \approx \frac{n^2k^2}{R_L}, \tag{4.18}$$

$$\text{Re}[Y_T(j\omega)]_{\text{min}} \approx -nkg_m, \tag{4.19}$$

$$\text{Im}[Y_T(j\omega)]_{\text{max}} \approx \frac{nk}{2}\left(g_m + \frac{nk}{R_L} \right), \tag{4.20}$$

$$\text{Im}[Y_T(j\omega)]_{\text{min}} \approx -\frac{nk}{2}\left(\frac{g_m \frac{L_1C_2}{C_1+C_2}}{\frac{L_1C_2}{C_1+C_2} + n^2(1-k^2)L_p} + \frac{nk}{R_L} \right), \tag{4.21}$$

at the following frequencies:

$$\omega_1 = \frac{1}{\sqrt{L_1C_2}}, \tag{4.22}$$

$$\omega_2 = \frac{1}{\sqrt{L_1 \frac{C_1C_2}{C_1+C_2}}}, \tag{4.23}$$

$$\omega_3 \approx \frac{1}{R_L(C_1+C_2)}, \tag{4.24}$$

$$\omega_4 \approx \frac{R_L}{\frac{L_1C_2}{C_1+C_2} + n^2(1-k^2)L_p}, \tag{4.25}$$

respectively. The above equations and approximations are derived from the following conditions: $Z_L = 0$ and $j\omega n^2(1-k^2)L_p$ is ignored against R_L in Eqs. (4.18) and (4.22); $Z_L = \infty$ in Eqs. (4.19) and (4.23); $Z_L = 1/j\omega(C_1 + C_2)$ and $\omega^2 n^2(1-k^2)L_p(C_1+C_2) \ll 1$ in Eqs. (4.20)

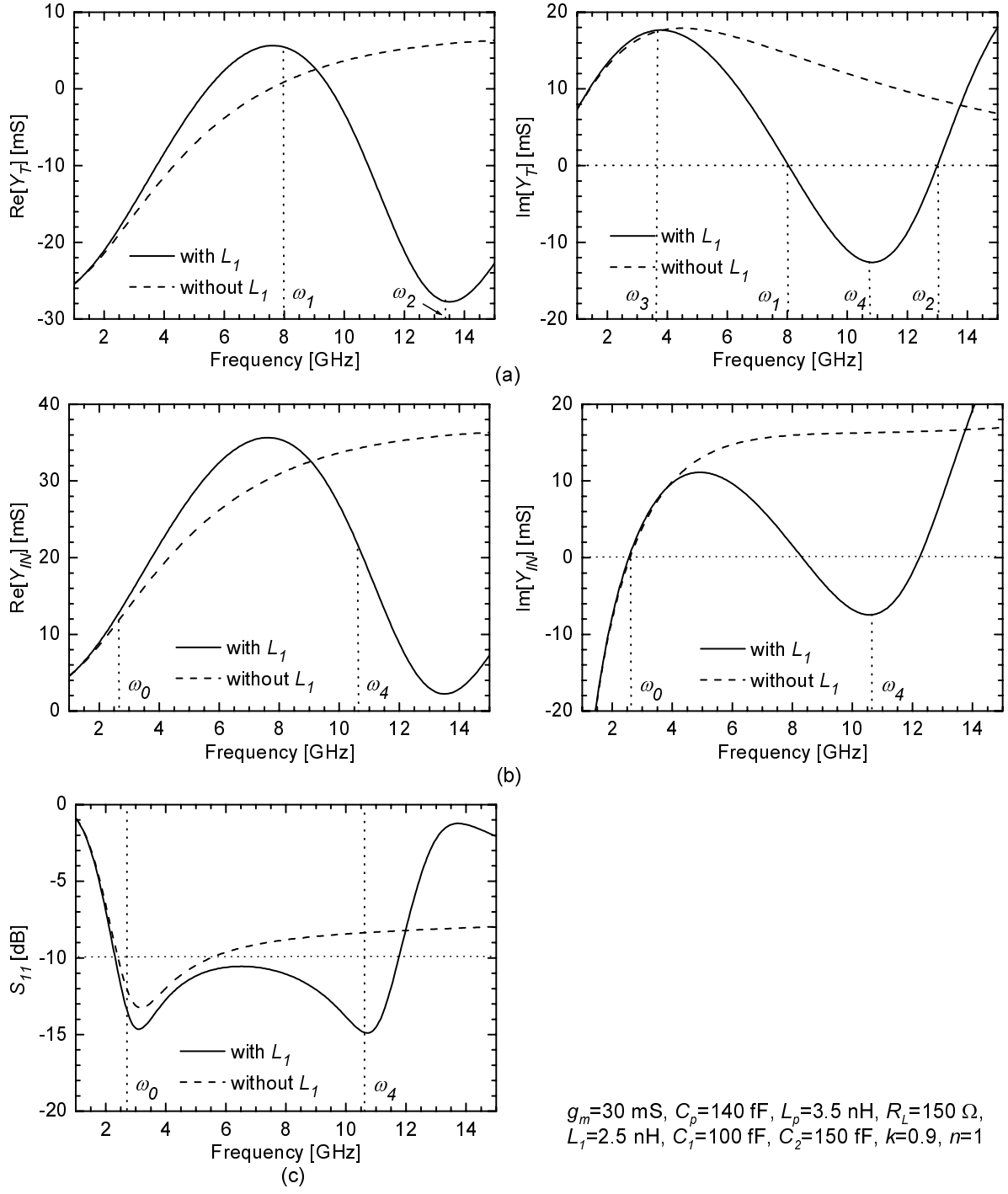

Figure 4.9: Calculated real and imaginary parts of (a) Y_T and (b) Y_{IN}, and (c) S_{11} of the LNAs with and without L_1.

and (4.24); $Z_L = j\omega L_1 C_2/(C_1 + C_2)$ in Eqs. (4.21) and (4.25). A negative Re$[Y_T(j\omega)]$ shown in Eq. (4.19) originates from the positive feedback provided by the transformer. The calculated Y_{IN} is also shown in Fig. 4.9(b). The real part of Y_{IN}, Re$[Y_{IN}(j\omega)]$, is simply shifted by g_m from Re$[Y_T(j\omega)]$, and the imaginary part of Y_{IN}, Im$[Y_{IN}(j\omega)]$, becomes zero at resonance frequencies. The first resonance frequency ω_0 is derived from the following equation:

$$\text{Im}[Y_{IN}(j\omega_0)] \approx j\omega_0 C_p + \frac{1}{j\omega_0 L_p} + j\omega_0 \frac{nk(C_1 + C_2)(nk + g_m R_L)}{1 + \omega_0^2 R_L^2 (C_1 + C_2)^2} = 0, \tag{4.26}$$

where the last term in Im$[Y_{IN}(j\omega_0)]$ is Im$[Y_T(j\omega_0)]$ for $Z_L = 1/j\omega_0(C_1 + C_2)$ and $\omega_0^2 n^2(1 - k^2)L_p(C_1 + C_2) \ll 1$.

Input impedance matching conditions are derived from $Y_{IN}(j\omega_0)$ and $Y_{IN}(j\omega_1)$. At ω_0, the real part of $Y_{IN}(j\omega)$ is approximated as

$$\text{Re}[Y_{IN}(j\omega_0)] \approx g_m \left(1 - \frac{nk}{1 + \omega_0^2 R_L^2 (C_1 + C_2)^2}\right), \tag{4.27}$$

where $\omega_0^2 nk R_L (C_1 + C_2)^2/g_m \ll 1$. At ω_1, Im$[Y_{IN}(j\omega)]$ is negligible against Re$[Y_{IN}(j\omega)]$:

$$Y_{IN}(j\omega_1) \approx \text{Re}[Y_{IN}(j\omega_1)] = g_m + \frac{n^2 k^2}{R_L}. \tag{4.28}$$

For input impedance matching ($|S_{11}| < -10$ dB), Y_{IN} must satisfy the following condition:

$$|S_{11}| = \left|\frac{1 - R_s Y_{IN}}{1 + R_s Y_{IN}}\right| < 0.316. \tag{4.29}$$

When Im$[Y_{IN}(j\omega)] = 0$, Eq. (4.29) can be simplified to

$$10 \text{ mS} < \text{Re}[Y_{IN}(j\omega)] < 38 \text{ mS}. \tag{4.30}$$

Substituting Eqs. (4.27) and (4.28) into Eq. (4.30), we can derive the following impedance matching conditions:

$$10 \text{ mS} < g_m \left(1 - \frac{nk}{1 + \omega_0^2 R_L^2 (C_1 + C_2)^2}\right), \tag{4.31}$$

$$g_m + \frac{n^2 k^2}{R_L} < 38 \text{ mS}. \tag{4.32}$$

Equations (4.31) and (4.32) determine the lower and upper limits to g_m and the lower limit to R_L.

An impedance matching procedure for the proposed LNA is as follows:

1. Select g_m and R_L to satisfy Eqs. (4.31) and (4.32)
2. Select L_p such that ω_0 equals the lower edge of the desired input band

3. Select L_1 such that ω_4 equals the upper edge of the desired input band

Figure 4.9(c) shows the calculated S_{11} of the LNAs with and without L_1, where ω_0 and ω_4 are set to approximately 3.1 GHz and 10.6 GHz, respectively. A transconductance of 30 mS and load resistance of 150 Ω allow $|S_{11}| < -10$ dB from ω_0 to ω_1. Around ω_4, the π network including L_1 decreases Re$[Y_{IN}(j\omega)]$ and Im$[Y_{IN}(j\omega)]$:

$$\text{Re}[Y_{IN}(j\omega_4)] = g_m - \frac{nk}{2R_L}\left(\frac{\omega_4 L_1 C_2 g_m}{C_1 + C_2} - nk\right), \tag{4.33}$$

$$\text{Im}[Y_{IN}(j\omega_4)] = \omega_4 C_p - \frac{1}{\omega_4 L_p} - \frac{nk}{2R_L}\left(\frac{\omega_4 L_1 C_2 g_m}{C_1 + C_2} + nk\right), \tag{4.34}$$

providing $|S_{11}| < -10$ dB. Consequently, the input impedance matching is achieved from ω_0 to ω_4.

4.4.3 Gain

The transformer provides the positive feedback from node A to the input, as shown in Section 4.3.1. The transformer positive feedback reduces the gain (S_{21}) bandwidth of the LNA. The S_{21} of the LNA with output impedance matching is given by

$$S_{21} = \frac{v_{out}}{v_s/2} = \frac{2v_{in}}{v_s}\frac{v_{out}}{v_{in}} = \frac{2}{1 + R_s Y_{IN}} A_v, \tag{4.35}$$

where v_s is the signal voltage and A_v, defined by v_{out}/v_{in}, is the voltage gain from the input to the output of the LNA, as shown in Fig. 4.4. Equation (4.35) shows that the frequency response of A_v is shaped by that of Y_{IN} (i.e., S_{11}), which results in that of S_{21}.

The frequency response of A_v of the proposed LNA is similar to that of a CG LNA with a load resistor and output series inductor. The output network combined a shunt-peaking inductor with an output series inductor gives a larger bandwidth than the counterpart with either inductor, as explained in [23, 27]. However, the shunt-peaking inductor L_s in the proposed LNA does not increase the bandwidth. The A_v of the LNA is given by

$$A_v(s) = \frac{g_m R_L\left(1 + \frac{nk}{g_m R_L} + \frac{1-k^2}{m_1}\frac{s}{\omega_c}\right)}{1 + \frac{s}{\omega_c} + \left(\frac{1-k^2}{m_1} + \frac{1-k_c}{m_2}\right)\frac{s^2}{\omega_c^2} + \frac{k_c(1-k_c)}{m_2}\frac{s^3}{\omega_c^3} + \frac{1-k^2}{m_1}\frac{k_c(1-k_c)}{m_2}\frac{s^4}{\omega_c^4}}, \tag{4.36}$$

where $\omega_c = 1/R_L(C_1 + C_2)$, $k_c = C_1/(C_1 + C_2)$, $m_1 = R_L^2(C_1 + C_2)/L_s$, and $m_2 = R_L^2(C_1 + C_2)/L_1$ [23]. Substituting $k = 0$ into Eq. (4.36) gives the A_v of the CG LNA with both the shunt-peaking and output series inductors. Equation (4.36) shows that all m_1 are divided by a factor of $(1 - k^2)$, i.e., L_s is multiplied by a factor of $(1 - k^2)$. This means that the effective L_s in the proposed LNA becomes small, compared with the shunt-peaking inductor in the CG LNA, and then contributes less to bandwidth extension. The calculated A_v with k as a parameter is shown in

Fig. 4.10, where $f_c = 4.2$ GHz, $k_c = 0.4$, $m_1 = 1.6$, and $m_2 = 2.25$ originate from $C_1 = 100$ fF, $C_2 = 150$ fF, $L_s = 3.5$ nH, $L_1 = 2.5$ nH, and $R_L = 150\ \Omega$. A very large peak (ripple) is found when $k = 0$, because L_s is larger than L_1, i.e., $m_1 < m_2$ [23, 27]. Figure 4.10 shows that both the peak and bandwidth decrease as k increases. Consequently, the bandwidth of the proposed LNA ($k \simeq 0.9$) closely equals that of the CG LNA with only the output series inductor. A flat voltage gain of the CG LNA across the entire UWB frequency band can be obtained by selecting an appropriate value of m_2 (approximately 2), as discussed in [23].

An S_{21} variation of the proposed LNA mainly originates from the characteristic of Y_{IN} (S_{11}). As shown in Fig 4.9(c), the input impedance matching condition improves around ω_0 and ω_4, but deteriorates around ω_1. This means that an input signal of ω_1 is less transferred to the input of the LNA, compared to that of ω_0 or ω_4, which results in a reduction in the magnitude of S_{21} around ω_1. The difference between $S_{21}(j\omega_0)$ and $S_{21}(j\omega_1)$ can be approximated from Eq. (4.35):

$$\Delta S_{21} = \frac{S_{21}(j\omega_0)}{S_{21}(j\omega_1)} = \frac{1 + R_s Y_{IN}(j\omega_1)}{1 + R_s Y_{IN}(j\omega_0)} \approx \frac{1 + R_s \cdot \mathrm{Re}[Y_{IN}(j\omega_1)]}{1 + R_s \cdot \mathrm{Re}[Y_{IN}(j\omega_0)]}, \tag{4.37}$$

where $A_v(j\omega_0) = A_v(j\omega_1)$ is assumed, the real parts of $Y_{IN}(j\omega_0)$ and $Y_{IN}(j\omega_1)$ are given by Eqs. (4.27) and (4.28), respectively, and the imaginary parts of $Y_{IN}(j\omega_0)$ and $Y_{IN}(j\omega_1)$ can be neglected, as shown in the previous subsection. Figure 4.11 shows the calculated A_v and S_{21} of the proposed LNA with $k = 0.9$. Substituting the parameters shown in Fig. 4.11 into Eq. (4.37) gives $\Delta S_{21} = -3.6$ dB, while an S_{21} variation of -4.7 dB is seen in Fig. 4.11, and then -1.1 dB originates from the difference of A_v. The difference of S_{21} can be reduced by decreasing R_L, as shown by Eqs. (4.27), (4.28), and (4.37). Moreover, using a common-source (CS) amplifier with a gain peak around ω_1 as the second stage, we can obtain a flat gain.

4.4.4 Stability

The proposed LNA becomes potentially unstable, due to the transformer positive feedback. For unconditionally stable, the LNA must meet the following conditions, as shown in Section 1.2.2:

$$\mathrm{Re}[Z_{IN}] > 0, \tag{4.38}$$

$$\mathrm{Re}[Z_{OUT}] > 0. \tag{4.39}$$

In what follows, to simplify the expression of the output impedance of the LNA, we will verify whether the LNA without the output π network (C_1, L_1, and C_2) satisfies the above conditions or not.

First, the real part of the input admittance of the LNA can be derived from Eqs. (4.15)–(4.16) for $Z_L = \infty$:

$$\mathrm{Re}[Y_{IN}(j\omega)] = g_m\,(1 - nk)\,. \tag{4.40}$$

In the case of the proposed LNA, n is selected to be one, shown in Section 4.4.1, and k of the on-chip transformer is less than one [28]: $nk < 1$. The requirement of Eq. (4.38) is thus satisfied.

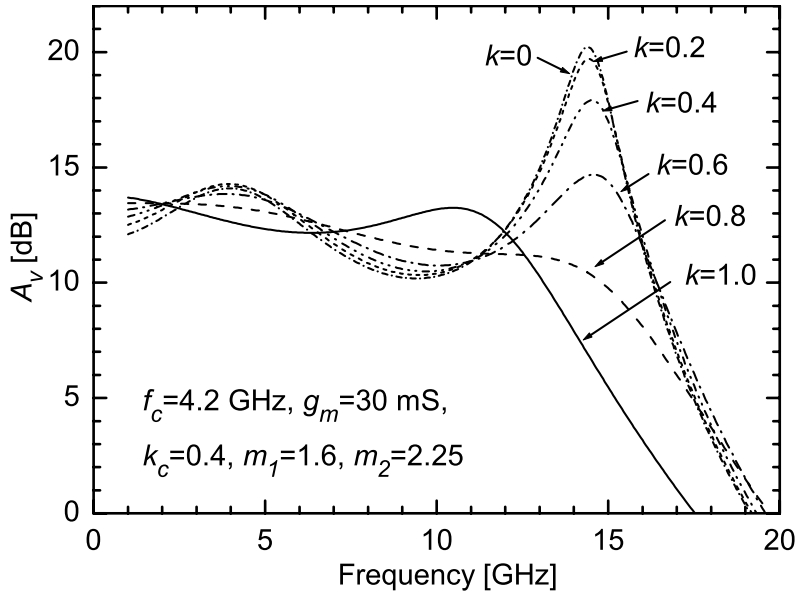

Figure 4.10: Calculated A_v of the proposed LNA with k as a parameter.

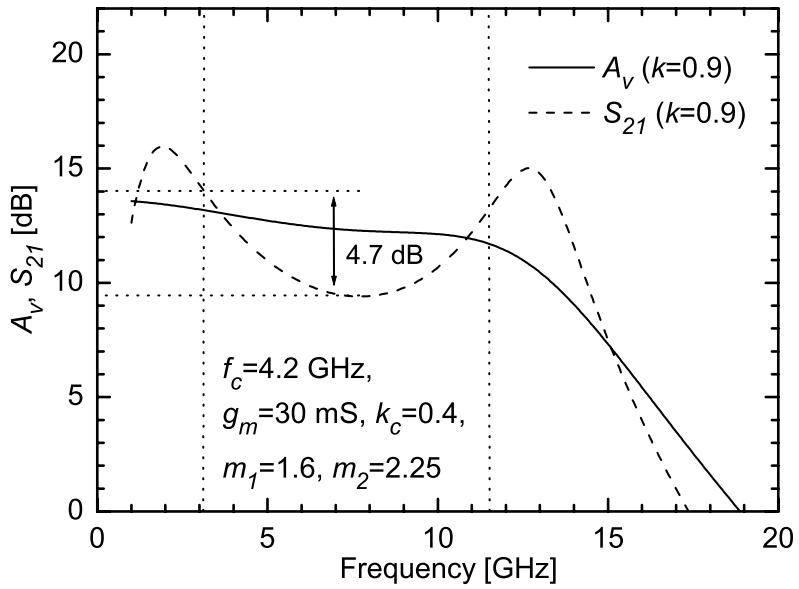

Figure 4.11: Calculated A_v and S_{21} of the proposed LNA with $k = 0.9$.

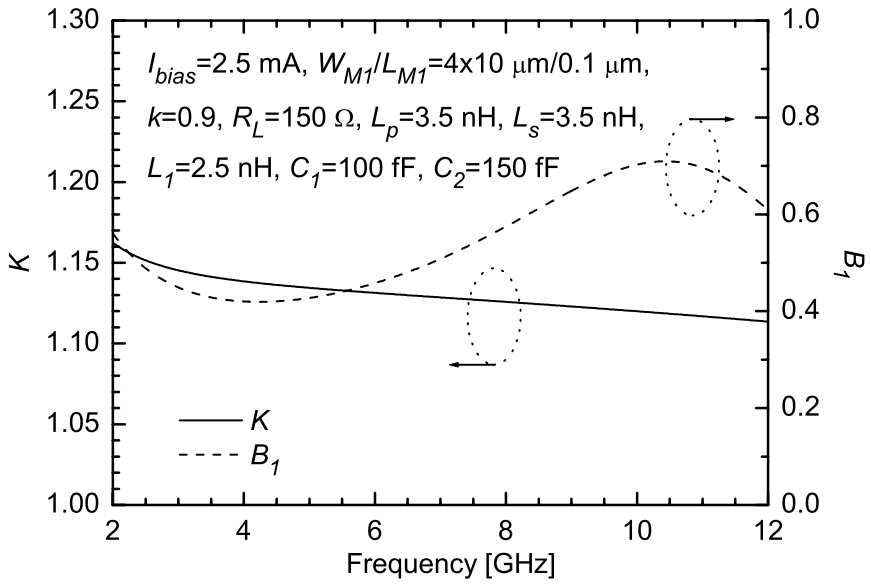

Figure 4.12: Simulated K and B_1 of the proposed LNA.

Next, the output impedance considering the left hand side of output node A (Fig. 4.4) is given by

$$Z_{OUT,A}(j\omega) = \frac{\left(\frac{1}{R_s} + g_m + j\omega C_p\right)(R_L + j\omega(1-k^2)L_s) + n^2 + \frac{R_L}{j\omega L_p}}{\frac{1}{R_s} + g_m(1-nk) + j\omega C_p + \frac{1}{j\omega L_p}}. \tag{4.41}$$

Equation (4.41) indicates that the real part of $Z_{OUT,A}$ becomes a maximum around $\omega = 1/\sqrt{L_p C_p}$ and can be approximated by

$$\text{Re}[Z_{OUT,A}(j\omega)] \approx R_L, \tag{4.42}$$

$$\text{Re}[Z_{OUT,A}(j\omega)] \approx R_L + \frac{(1-k^2)L_s}{C_p}\left(\frac{1}{R_s} + g_m\right), \tag{4.43}$$

at low and high frequencies (i.e., $\omega \ll 1/\sqrt{L_p C_p}$ and $\omega \gg 1/\sqrt{L_p C_p}$), respectively. The requirement of Eq. (4.39) is therefore satisfied.

The stability is also ensured through simulation. Figure 4.12 shows the simulated K and B_1 of the proposed LNA, which are given by [29]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}, \tag{4.44}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2, \tag{4.45}$$

respectively, where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. The necessary and sufficient conditions for unconditional stability are $K > 1$ and $B_1 > 0$ [29]. The simulations show that the LNA satisfies these conditions across the entire UWB frequency band.

4.4.5 Group Delay

A group delay variation is important for DS-UWB or pulse-based UWB systems. The group delay is the derivative of the phase of the signal transfer function (S_{21}), and hence any resonance in the signal path contributes to the variation [30]. The critical resonances in the proposed LNA originate from the combinations of L_p (transformer) and C_p at the input, and L_1, C_1, and C_2 at the output, and these resonance frequencies, ω_0 and ω_2, are given by Eqs. (4.26) and (4.23), respectively. Pushing the resonance frequencies out of the desired frequency band (i.e., increasing L_p or decreasing L_1) allows a small group delay variation. Figure 4.13 shows that the simulated group delays of the proposed LNA with L_p and L_1 as a parameter. The group delay (for $L_p = 3.0$ nH in Fig. 4.13(a)) dramatically changes around 3 GHz (ω_0) and 11 GHz (ω_2). The simulations also show that the variation can be reduced by increasing L_p or decreasing L_1.

4.5 Design

By using a 90 nm CMOS process and device parameters, the proposed LNA is designed to satisfy the following typical specifications of the UWB LNA: $|S_{11}| < -10$ dB, $NF < 4$ dB, and $|S_{21}| > 10$ dB across the entire UWB frequency band (3.1–10.6 GHz). Current consumption is set to 2.5 mA at a 1.0 V supply.

4.5.1 Input Transistor and Load Resistor

The transconductance g_m and load resistance R_L are determined by the input impedance matching conditions, given by Eqs. (4.31) and (4.32), and the desired gain. A transconductance of 30 mS and load resistance of 145 Ω provide both $|S_{11}| < -10$ dB and $A_v \simeq 14$ dB[2] in the lower UWB band (3.1–5 GHz). The load resistance includes the parasitic resistance of L_s. A bias current of 2.5 mA and g_m of 30 mS result in a gate width of 4×10 μm (10 gate fingers, each with a unit of of 4 μm width) and gate length of 100 nm.

4.5.2 Transformer

The transformer adopts a stacked configuration in which L_p is stacked on L_s. This configuration provides the largest coupling factor and a small area [28]. The large parasitic resistance of L_s, due to the lower thin metal layer, is not problematic, because it can be absorbed into R_L.

The parasitic capacitance between L_p and L_s, C_c, has a relatively small effect on the LNA performance. This capacitance significantly affects the frequency response of a noninverting transformer [28]. Although the proposed LNA employs the noninverting stacked transformer, the signal current injected into L_s by M_1 reduces the effect of C_c. Figure 4.14 shows the simulated S_{11} and NF of the LNA including C_c. In the lower UWB band, C_c slightly increases the magnitude of the S_{11} and has little impact on the NF; in the higher, a large C_c decreases the

[2] At low frequencies, $A_v \approx g_m R_L + nk = 5.25$.

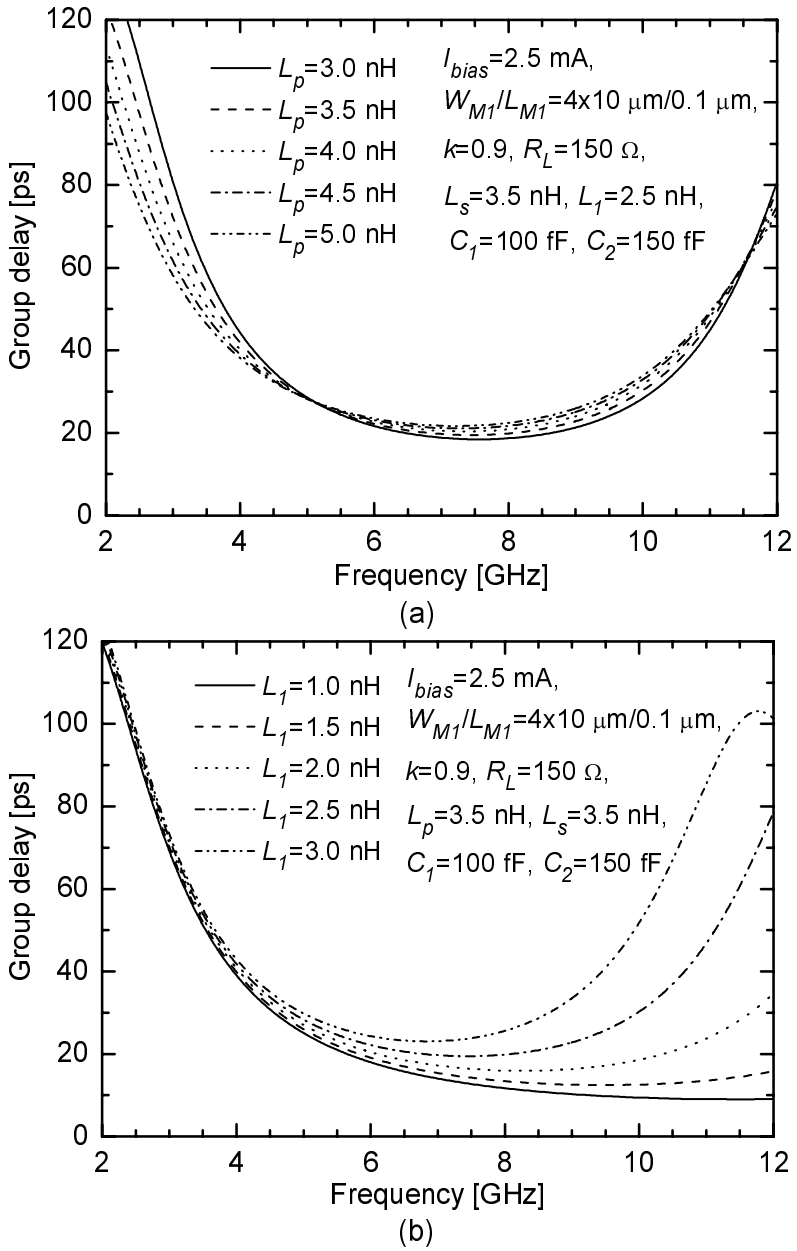

Figure 4.13: Simulated group delays with (a) L_p and (b) L_1 as a parameter.

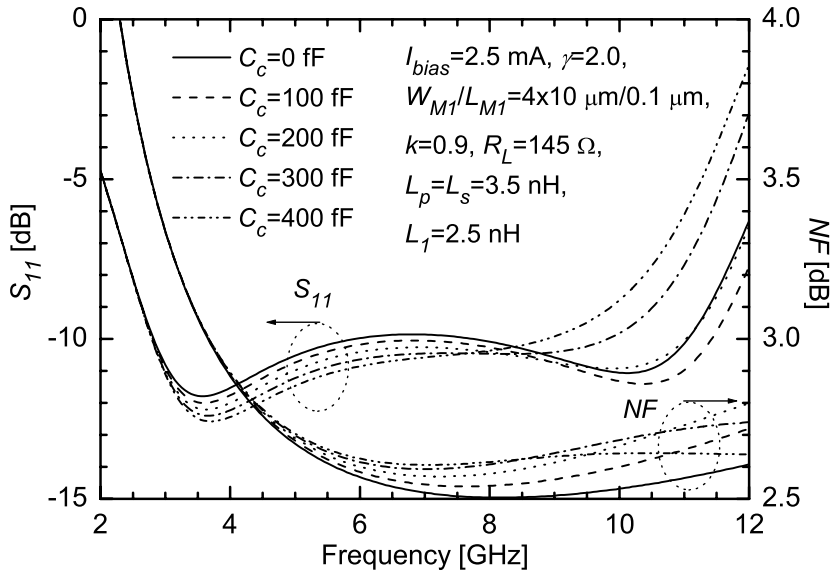

Figure 4.14: Simulated S_{11} and NF of the LNA with C_c as a parameter.

input bandwidth and increases the NF by up to 0.20 dB. In the simulations, for wideband input impedance matching, C_c must be less than 300 fF, which can be realized even with the stacked transformer.

The transformer is designed to achieve $|S_{11}| < -10$ dB (of the LNA) in the lower UWB band and $NF < 4.0$ dB across the entire UWB band. Figure 4.15 shows the top view and cross section of the designed transformer. Selecting L_p such that ω_0 equals approximately 3.1 GHz allows the LNA to achieve $|S_{11}| < -10$ dB in the lower band. A wide metal for realizing L_p reduces the parasitic resistance; however, it leads to a large chip area and large parasitic capacitance. For L_p, we adopt a 3.5-turn square inductor with an outer diameter of 165 μm, metal width of 3 μm, and metal spacing of 2 μm. To achieve a turn ratio of one, L_s is designed as follows: an outer diameter is 165 μm, a metal width 2 μm, and a metal spacing 3 μm. The metal thicknesses of L_p (top pad metal) and L_s (metal 6) are 1.9 μm and 0.9 μm, respectively. The parasitic capacitance C_c is reduced by offsetting the upper metal layer from the lower by short horizontal distance (3 μm), which results in $C_c \simeq 240$ fF. Three-dimensional (3-D) electromagnetic (EM) simulations by Ansoft HFSS showed $L_p = L_s = 4.0$ nH and $k = 0.9$.

4.5.3 Output Series Inductor

The output series inductor L_1 is designed to set ω_4 to the upper edge of the desired input band (10.6 GHz). We use a relatively low Q inductor to reduce the chip area and parasitic capacitance, which reduces the gain bandwidth of the LNA. The outer diameter of L_1 is 140 μm, the metal width 3 μm, the metal spacing 2 μm, and the metal thickness 1.9 μm (top pad metal). EM

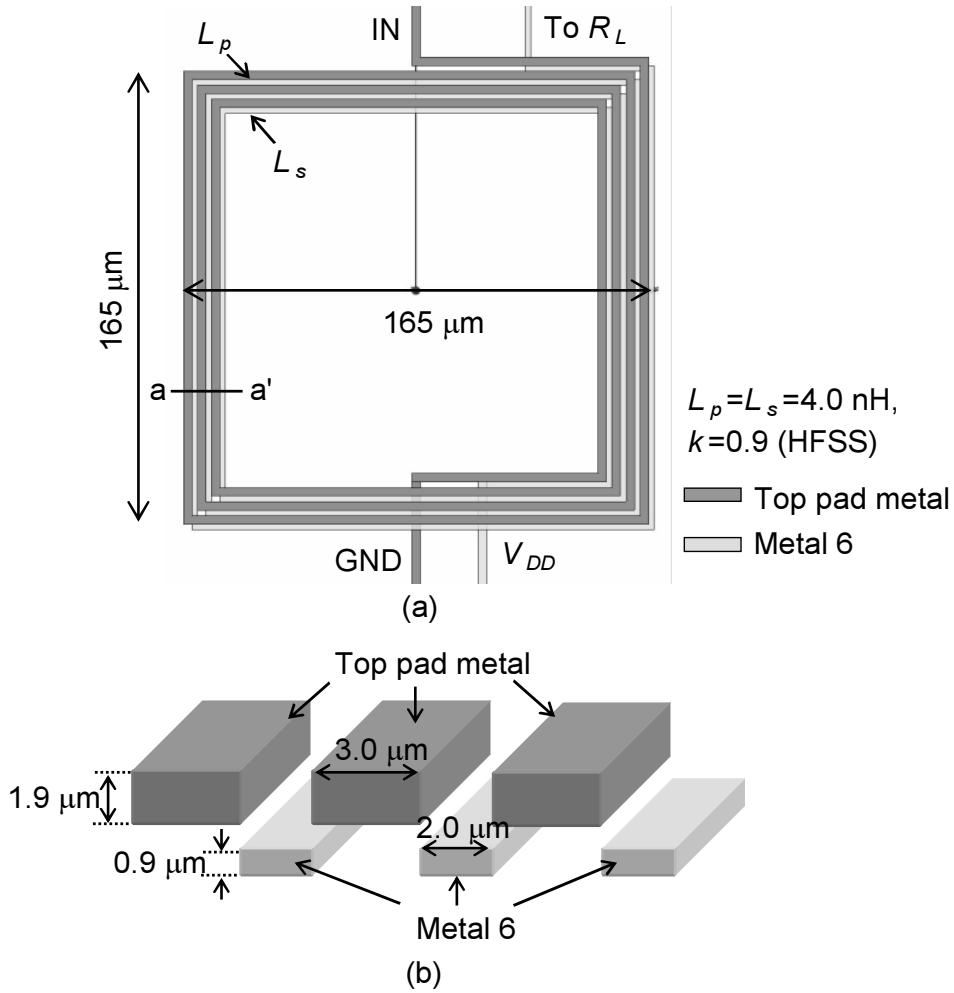

Figure 4.15: (a) Top view and (b) cross section a–a' of the designed transformer.

simulations showed that the inductance and maximum Q were 3.2 nH and 6.0 (at 5.0 GHz), respectively.

4.6 Experimental Results and Discussion

The designed LNA shown in Fig. 4.16 was fabricated in a 90 nm digital CMOS process without metal-insulator-metal (MIM) capacitors. A DC-blocking capacitor of 400 fF consisted of vertical parallel plates [31], due to low input and output parasitic capacitances ($\sim$ 25 fF). A micrograph of the fabricated LNA is shown in Fig. 4.17. The active chip area excluding pads was 0.48×0.25 mm^2. The input and output pads was not electrostatic-discharge (ESD) protected. Metal fills consisting of metal 1–6 layers were placed both inside and outside the fabricated transformer and

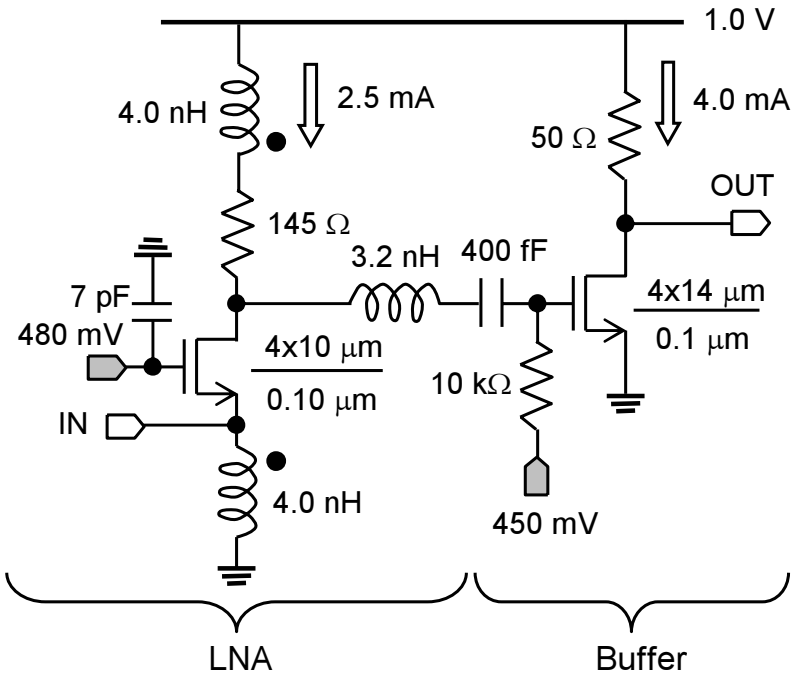

Figure 4.16: Complete schematic of the designed transformer noise-canceling LNA

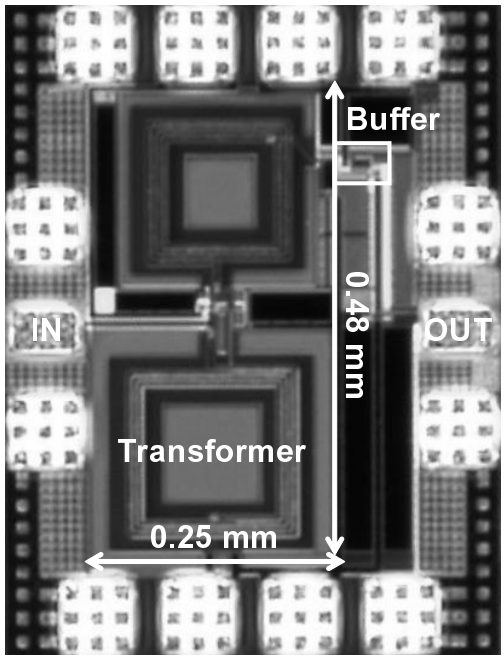

Figure 4.17: Micrograph of the fabricated LNA.

inductor to meet metal density rules in the CMOS process. They were 1.5 μm by 1.5 μm squares with a spacing of 0.2 μm. The average horizontal distance between the metal fills and traces of the inductors was 15 μm. For measurements, a unity-gain CS amplifier with a 50 Ω output resistor was used as a buffer. The S-parameters, noise, and linearity of the LNA were measured using on-wafer RF probes. The power consumption of the LNA and buffer were 2.5 mW and 4.0 mW, respectively, at a supply voltage of 1.0 V.

4.6.1 S-parameters

Figure 4.18 shows the measured and simulated S_{11} and S_{21} of the LNA. The S-parameters was measured using an Agilent Technologies HP8722ES network analyzer. The LNA achieved $|S_{11}| < -10$ dB and $|S_{21}| > 9.3$ dB across 3.1–10.6 GHz. The discrepancy between the measurements and simulations at frequencies above 4 GHz is mainly attributed to insufficient accuracy in the simulations of the transformer and inductor used. The HFSS simulation models of the transformer and inductor included no metal fills to solve convergence problems and reduce the memory requirement. The metal fills increase the parasitic capacitances and resistances of the transformer and inductor [32–34], which results in the discrepancy.

Figure 4.19 shows the measured and simulated S_{12} of the LNA with the buffer. The difference between the measured and simulated S_{12} is due to substrate effects. The LNA achieved $|S_{12}| < -34$ dB across 3.1–10.6 GHz. The measured S_{12} of the stand-alone buffer (not shown) was less than -24 dB over the same frequency range. Thus, the S_{12} of the LNA without the buffer was less than -10 dB. The poor reverse isolation performance is due to the transformer, and an additional stage may be required to improve the isolation performance.

Figure 4.20 shows the measured and simulated group delays. The group delay variation increased around the edge of the UWB frequency band, as analyzed in Section 4.4.5. A group delay variation of approximately 60 ps was achieved for the entire band.

4.6.2 NF

Figure 4.21 shows the measured and simulated NF of the LNA. The NF was measured using an Agilent Technologies HP8970B noise figure meter. Note that these results included the noise of the output buffer, which increased the overall NF by 0.8 dB for an LNA gain of 10 dB in simulation. The LNA with the buffer achieved an NF of 3.8–4.4 dB across the entire UWB band. This means that the proposed LNA with an additional CS amplifier like the buffer can achieve $NF < 4.4$ dB. The difference between the measurements and simulations can be explained by the extra input-referred noise of the buffer, caused by the lower measured gain than the simulated one.

4.6.3 Linearity

Figure 4.22 shows the output power of the fundamental tone and third-order intermodulation (IM_3) products for two tones (3.000 GHz and 3.001 GHz), measured using an Agilent Tech-

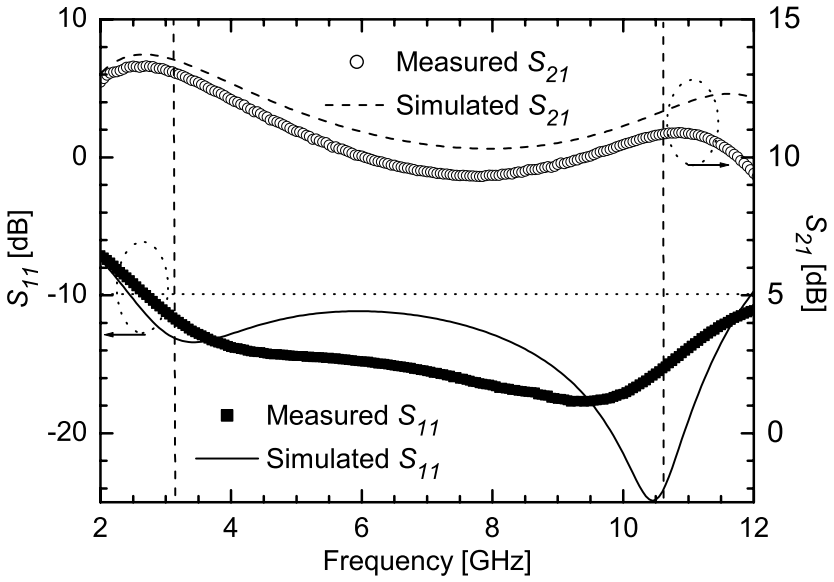

Figure 4.18: Measured and simulated S_{11} and S_{21} of the LNA.

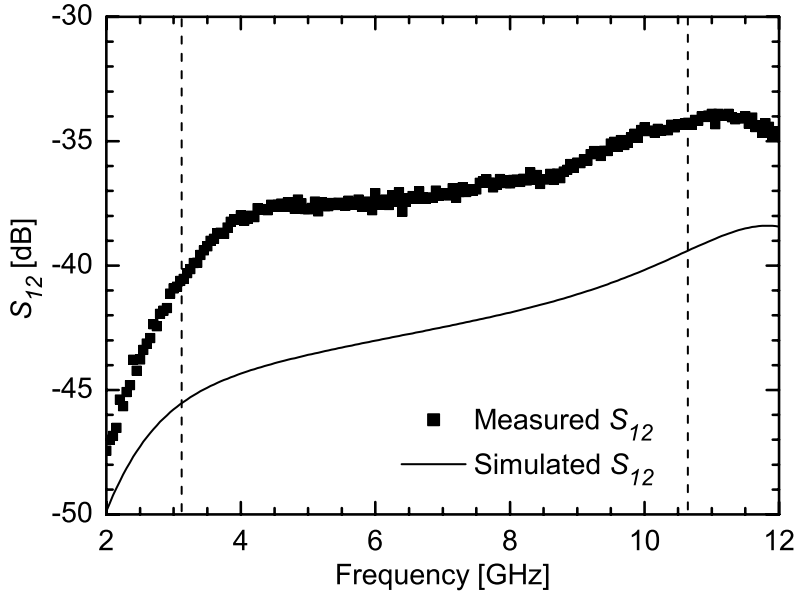

Figure 4.19: Measured and simulated S_{12} of the LNA.

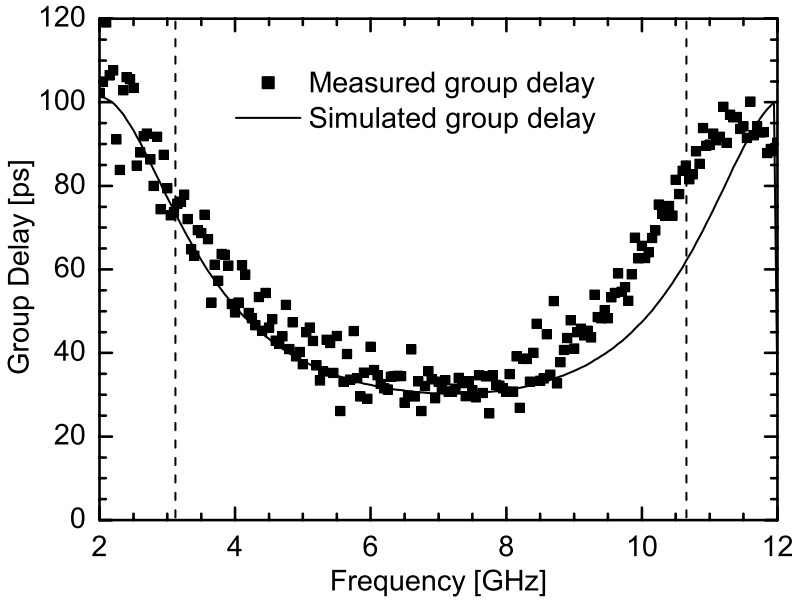

Figure 4.20: Measured and simulated group delays of the LNA.

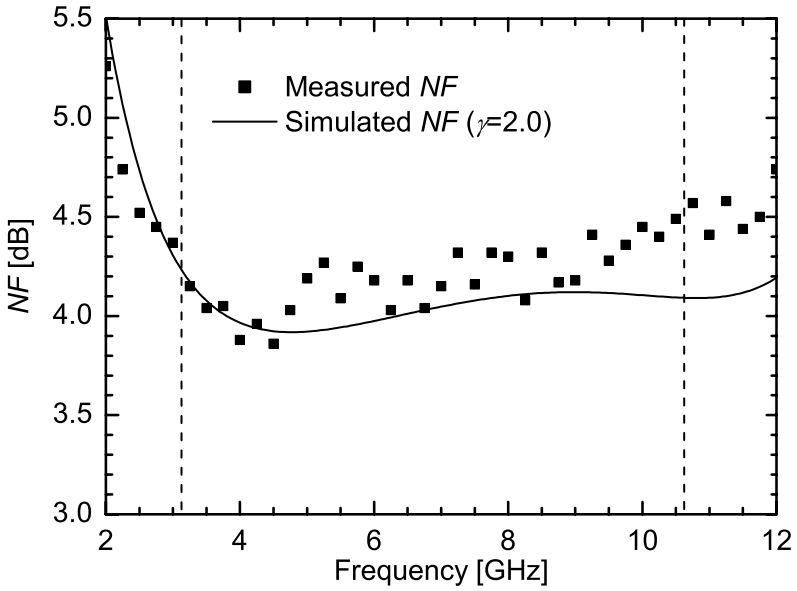

Figure 4.21: Measured and simulated NF of the LNA.

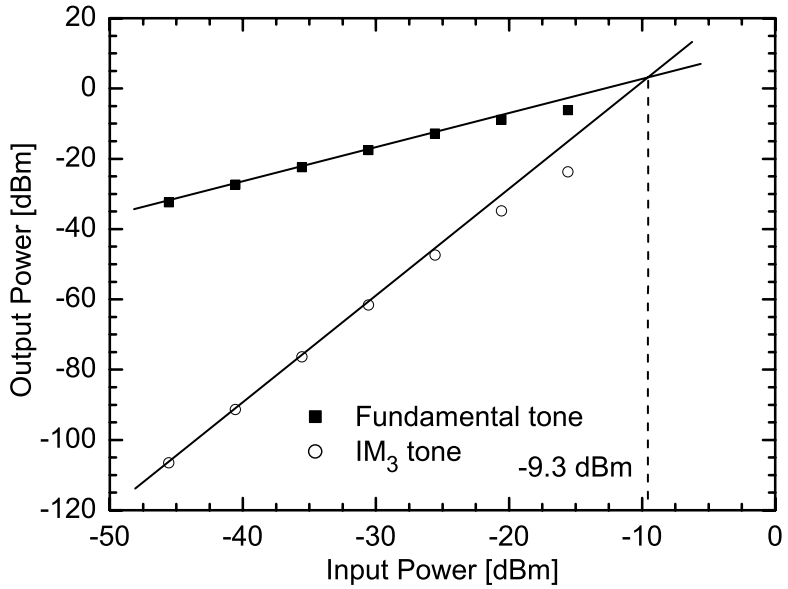

Figure 4.22: Measured IIP_3 of the LNA at 3 GHz.

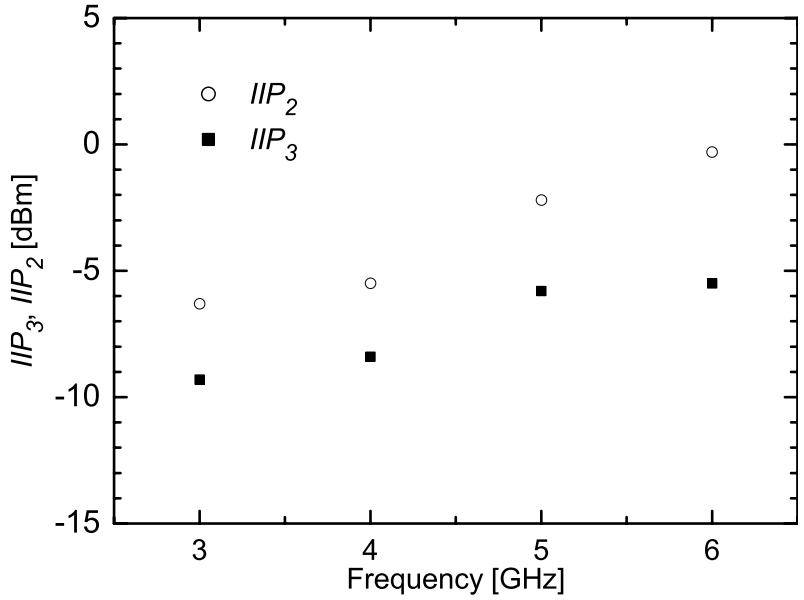

Figure 4.23: Measured IIP_3 and IIP_2 of the LNA.

nologies E4448A spectrum analyzer. The two tones were generated by Agilent Technologies HP8671B and E4438C signal generators. The measured IIP_3 and 1-dB compression point were approximately -9.3 dBm and -20 dBm, respectively. Figure 4.23 shows IIP_3 and IIP_2 measured by applying two tones with 1-MHz spacing. The measured frequency range of 3–6 GHz was limited by the signal generator. An $IIP_3 > -9.3$ dBm and $IIP_2 > -6.3$ dBm were obtained in the frequency range.

4.6.4 Comparison

Table 4.1 shows a summary of the LNA performance and a comparison with previously reported 3.1–10.6 GHz CMOS LNAs. The proposed LNA achieved input impedance matching and comparable noise performance across the entire UWB band with the lowest reported power consumption and supply voltage. The LNA also consumed the smallest chip area among the wideband LNAs employing inductors [10, 11, 16, 23].

An additional amplifier stage can allow the proposed LNA to achieve a more and flatter gain across 3.1–10.6 GHz. A relatively low gain of the implemented LNA (>9.3 dB) leads to an increase in the overall NF of the receiver. For instance, the NF specification for RF receivers of the MB-OFDM UWB system is less than 6.6 dB [35, 36]. A receiver employing the proposed LNA may have difficulty in satisfying such an NF specification. A CS amplifier with a load inductor, shown in Fig. 4.24, improves the LNA gain, alleviating this problem. The CS amplifier is designed to have a gain peak around 8.0 GHz and a power consumption of 2.0 mW. The 2.6-nH inductor consists of stacked square spiral inductors implemented by the top pad metal and metal 6 layers, and occupies only 55×55 μm^2. Figure 4.25 shows the simulated S_{21} and NF of the LNAs with and without the CS amplifier. The inductor was designed by using the EM simulator. The LNA with the CS amplifier achieved more and flatter gain ($|S_{21}| > 20$ dB) and the same noise performance as the LNA without the CS amplifier ($NF < 4.3$ dB) across 3.1–10.6 GHz. The group delay variation (not shown) was reduced to approximately 20 ps. Considering the measurements of the fabricated LNA, we conclude that the proposed LNA with the CS amplifier can achieve $|S_{21}| > 20$ dB and $NF < 4.4$ dB across 3.1–10.6 GHz with an additional power consumption of 2.0 mW and chip area of 55×55 μm^2.

4.7 Conclusion

We have demonstrated a transformer noise-canceling UWB CMOS LNA with an output series inductor. The transformer partly cancels the noise of the common-gate transistor and load resistor, thereby improving the LNA noise performance. The output series inductor improves both the gain and input bandwidths. Circuit analysis showed that the best turn ratio for the noise performance is one and input impedance matching depends not only on the common-gate transistor but also on the load resistor. The LNA designed for UWB applications was fabricated in a 90 nm digital CMOS process. The fabricated LNA occupied 0.12 mm^2, and achieved $|S_{11}| < -10$ dB, $NF < 4.4$ dB, and $|S_{21}| > 9.3$ dB across 3.1–10.6 GHz, while consuming 2.5 mW from a 1.0 V

Table 4.1: Measured performance and comparison of wideband CMOS LNAs.

Reference	CMOS Technology	BW* [GHz]	NF [dB]	S_{21} [dB]	IIP_3 [dBm]	Supply [V]	Power† [mW]	Area [mm^2]	Topology
This work	90 nm	2.8–13.2	3.8–4.4‡	9.3–13.1‡	−9.3	1.0	2.5	0.12	Transformer noise-canceling
[4]	90 nm	0.5–6.2	1.9–2.6	25◇	−16	2.7	35.2	0.025	Resistive feedback CS
[6]	90 nm	0.5–5.0	2.3–2.6	21–22◇	−8.8	1.8	12	0.012	Resistive feedback CS
[7]	90 nm	0–6	3.4–4.3	12.5–15.3	N/A	1.0	3.4	0.0017	Common-drain feedback CS
[8]	130 nm	1–7.4	>2.4	15–17◇	−4.1	1.4	25	0.019	Common-drain feedback CS⋆
[10]	130 nm	3.1–10.6	2.1–2.9	13.7–16.5	−8.5	1.2	9.0	0.40	Reactive feedback CS
[11]	180 nm	0–14.1	4.5–5.1‡	12.0–13.7‡	−6.2	1.8	20	0.50	Noise-canceling CG using CS
[13]	65 nm	0.2–6.2	2.8–4.2	9.9–15.6◇	0	1.2	14	0.009	Noise-canceling CG using CS
[14]	130 nm	3.7–8.8	3.6–4.5	8.1–11	−7.2	1.5	19	0.05	Noise-canceling CS
[16]	180 nm	1–11	2.9–3.0	8–9	−3.55	1.8	21.6	0.20	Distributed
[23]	180 nm	2.6–10.7	4.4–5.3‡	6.0–8.5‡	7.4	1.8	4.5	0.40	Capacitor cross-coupled CG⋆

*Input bandwidth

†Without buffers

‡3.1–10.6 GHz frequency range

◇Voltage gain

⋆Input-output differential topology

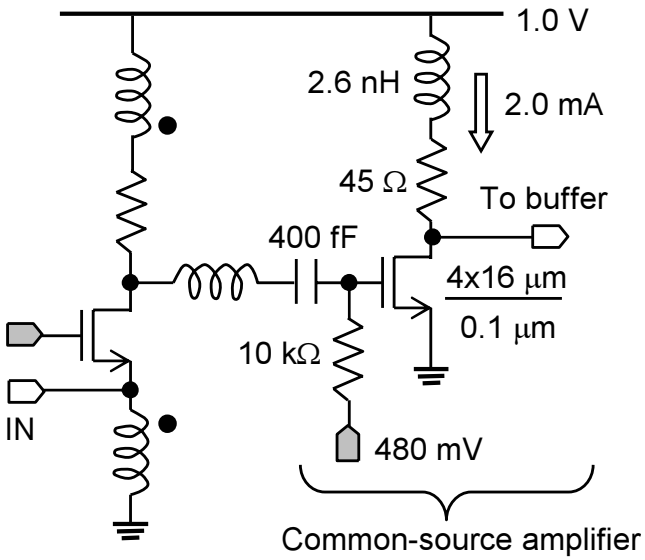

Figure 4.24: Common-source amplifier with a load inductor.

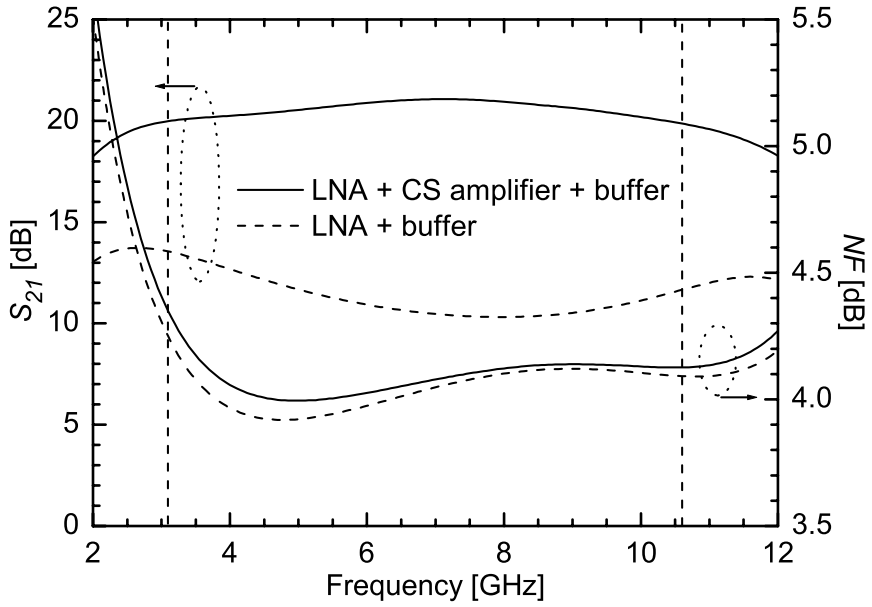

Figure 4.25: Simulated S_{21} and NF of the LNAs with and without the common-source amplifier.

supply. The proposed topology is the most suitable for low-power and low-voltage UWB CMOS LNAs.

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Chapter 5

Conclusion

In this dissertation, I have proposed and demonstrated low-voltage and small-area CMOS LNAs for narrowband and wideband applications.

Chapter 2 has demonstrated a 1.0 V, 0.25 mm^2 two-stage CMOS LNA with inductive source degeneration for 5 GHz applications. The presented two-stage topology that consists of common-source and common-gate stages is more suitable for low-voltage operation than a conventional cascode topology. The complete analytical expressions of the LNA performance were derived from the small-signal equivalent circuits that include an input parasitic capacitance and the Miller effect due to the gate-drain capacitance of the common-source transistor. These derived expressions showed that a higher V_{od1} results in a lower NF and IIP_3 while a higher V_{od2} leads to a higher NF and IIP_3. The proposed design methodology based on these expressions allows us to efficiently design a two-stage LNA that satisfies desired gain, NF, and IIP_3. The measurements were consistent with the calculations obtained from the analytical expressions.

Chapter 3 has demonstrated a 0.5 V, 0.21 mm^2 transformer folded-cascode CMOS LNA for 5 GHz applications. The internal and load inductors in a conventional folded-cascode LNA were magnetically coupled to reduced the chip area. The effects of the magnetic coupling between these inductors were analyzed. More magnetic coupling leads to a decrease in the resonance frequency of the input matching network, the peak frequency and magnitude of the gain, and the noise figure. The proposed partially-coupled transformer reduces the chip area, while having a small effect on the LNA performance. The folded-cascode LNA employing the transformer fabricated in a 90 nm CMOS process achieved the performance comparable to the conventional folded-cascode LNA, while consuming three fourths of the chip area of the conventional LNA. The fabricated LNA also achieved the best FoM with the smallest chip area among previously reported 0.4–0.6 V, 1.0 mW, 5 GHz CMOS LNAs. It has been demonstrated that the transformer folded-cascode LNA can replace conventional low-voltage CMOS LNAs.

Chapter 4 has demonstrated a 1.0 V, 0.12 mm^2 transformer noise-canceling CMOS LNA for fullband UWB (3.1–10.6 GHz) applications. The transformer noise cancellation scheme and output series inductor was incorporated into a conventional common-gate LNA. The transformer consisting of the input and shut-peaking inductors partly cancels the noise of the common-gate transistor and load resistor, thereby improving the LNA noise performance without increased

power consumption and chip area. The output series inductor improves both the gain and input bandwidths. Circuit analysis showed that the best turns ratio for the noise performance is one and input impedance matching depends not only on the common-gate transistor but also on the load resistor. The LNA fabricated in a 90 nm digital CMOS process achieved an S_{11} of less than -10 dB, NF of less than 4.4 dB, and S_{21} of more than 9.3 dB with the smallest supply voltage, power consumption (2.5 mW), and chip area, among previously reported 3.1–10.6 GHz CMOS LNAs. The proposed circuit topology is the most suitable for low-voltage, low-cost, and low-power UWB CMOS LNAs.

In summary, two circuit techniques allow the low-voltage and small-area design and implementation of CMOS LNAs. The first one is to use no cascode transistor, which alleviates the Miller effect but consumes voltage headroom. As alternative approaches, a common-gate stage is connected to a common-source LNA with inductive source degeneration as shown in Chapters 2 and 3; a common-gate topology, which needs no cascode transistor, is adopted for wideband applications as shown in Chapter 4. The second one is to magnetically couple two inductors to form a transformer, which consumes smaller chip area than two inductors, resulting in smaller area LNAs. In addition, the transformer consisting of the inductors connected to the source and drain terminals of the transistor in a common-gate topology partly cancels the noise produced by the transistor, improving the noise performance of the topology. This transformer noise cancellation scheme can be applied to all LNAs based on the common-gate topology. I conclude that the presented circuit techniques and LNAs contribute to low-voltage and low-cost CMOS RF front-ends.

Appendix A

NF Derivations

A.1 Two-Stage LNA

The noise of the two-stage LNA originates from M_1, M_2, R_I, and R_L. All output noise currents due to these elements flow into the equivalent resistance of the load LC tank, R_L. The LNA noise factor is given by

$$\begin{aligned} F_{LNA} &= \frac{\overline{|i_{o,s,eq}|^2} + \overline{|i_{o,M_1}|^2} + \overline{|i_{o,M_2}|^2} + \overline{|i_{o,R_I}|^2} + \overline{|i_{o,R_L}|^2}}{\overline{|i_{o,s,eq}|^2}} \\ &= 1 + F_{M_1} + F_{M_2} + F_{R_I} + F_{R_L}, \end{aligned} \tag{A.1}$$

where $i_{o,s,eq}$, i_{o,M_1}, i_{o,M_2}, i_{o,R_I}, and i_{o,R_L} are the output noise currents due to R_{eq}, M_1, M_2, R_I, and R_L, respectively.

The output noise current originating from the equivalent signal source R_{eq}, $i_{o,s,eq}$, can be derived from the noise equivalent circuit of the input stage, shown in Fig. A.1. The noise current produced by R_{eq} is given by

$$\overline{|i_{ns,eq}|^2} = \frac{4k_BT\Delta f}{R_{eq}}, \tag{A.2}$$

where k_B is Boltzmann's constant, T the absolute temperature, and Δf the noise bandwidth. The transfer function from $i_{ns,eq}$ to $i_{o,s,eq}$ is derived from Fig. A.1:

$$H_{ns,eq}(j\omega_0) \approx \frac{g_{m1}R_{eq}}{j\omega_0\alpha_M C_{gs1}(R_{eq}+R_{in})(1+1/g_{m2}R_I)}, \tag{A.3}$$

where $\omega_0 L_{eq} = -X_{in}$ is assumed and $r_{nqs,eff} \ll R_{eq}$. The output noise current originating form R_{eq} is therefore given by

$$\begin{aligned} \overline{|i_{o,s,eq}|^2} &= |H_{ns,eq}(j\omega_0)|^2 \, \overline{|i_{ns,eq}|^2} \\ &= \frac{4k_BTR_{eq}\omega_{T1}^2\Delta f}{\omega_0^2\alpha_M^2(R_{eq}+R_{in})^2(1+1/g_{m2}R_I)^2}. \end{aligned} \tag{A.4}$$

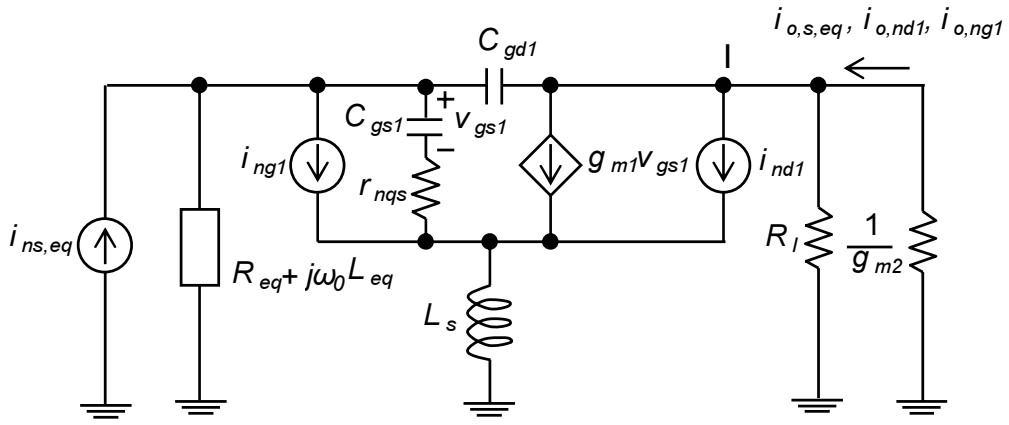

Figure A.1: Noise equivalent circuit of the input stage

A.1.1 F_{M_1}

The main noise sources in a MOSFET are the drain noise current i_{nd} and induced-gate noise current i_{ng}, expressed as [1, 2]

$$\overline{|i_{nd}|^2} = 4k_BT\gamma g_{d0}\Delta f, \tag{A.5}$$

$$\overline{|i_{ng}|^2} = 4k_BT\delta\frac{(\omega C_{gs})^2}{\kappa g_{d0}}\Delta f, \tag{A.6}$$

respectively, where g_{d0} is the zero-bias drain conductance of a MOSFET; γ, δ, and κ represent the noise parameters. The induced-gate noise current correlates to the drain noise current, and the correlation coefficient is given by [1]

$$c = \frac{\overline{i_{ng}\cdot i_{nd}^*}}{\sqrt{\overline{|i_{ng}|^2}}\sqrt{\overline{|i_{nd}|^2}}}. \tag{A.7}$$

Using this coefficient, we can express the induced-gate noise as [3]

$$\begin{aligned}\overline{|i_{ng}|^2} &= \overline{|i_{ngc}|^2} + \overline{|i_{ngu}|^2} \\ &= \overline{|i_{ng}|^2}|c|^2 + \overline{|i_{ng}|^2}(1-|c|^2),\end{aligned} \tag{A.8}$$

where i_{ngc} and i_{ngu} are the correlated and uncorrelated components, respectively. The output noise current originating from M_1 is therefore expressed as

$$\begin{aligned}\overline{|i_{o,M_1}|^2} &= \overline{|i_{o,nd1} + i_{o,ng1}|^2} \\ &= \overline{|i_{o,nd1} + i_{o,ngc1}|^2} + \overline{|i_{o,ngu1}|^2} \\ &= \overline{|i_{o,nd1}|^2} + \overline{i_{o,ngc1}\cdot i_{o,nd1}^*} + \overline{i_{o,nd1}\cdot i_{o,ngc1}^*} + \overline{|i_{o,ngc1}|^2} + \overline{|i_{o,ngu1}|^2},\end{aligned} \tag{A.9}$$

where $i_{o,nd1}$, $i_{o,ngc1}$ and $i_{o,ngu1}$ are the output noise currents due to i_{nd1}, i_{ngc1}, and i_{ngu1}, respectively. From Fig. A.1, the transfer function from i_{nd1} to $i_{o,nd1}$ is given by

$$\begin{aligned} H_{nd1}(j\omega_0) &= \frac{(R_{eq}+j\omega_0 L_{eq})(1+\alpha_{gd1})+j\omega_0 L_s+\frac{1}{j\omega_0 C_{gs1}}}{R_{eq}+j\omega_0 L_{eq}+\left(\omega_{T1}L_s+j\omega_0 L_s+\frac{1}{j\omega_0 C_{gs1}}\right)/\alpha_M}\cdot\frac{1}{\alpha_M(1+1/g_{m2}R_I)} \\ &\approx \frac{R_{eq}(1+\alpha_{gd1})}{\alpha_M(R_{eq}+R_{in})(1+1/g_{m2}R_I)}, \end{aligned} \tag{A.10}$$

where $r_{nqs,eff} \ll R_{eq}$ and $j\omega_0(L_{eq}+L_s/\alpha_M)+1/j\omega_0\alpha_M C_{gs1} \simeq 0$ under input impedance matching condition. The transfer function from i_{ng1} to $i_{o,ng1}$ is also given by

$$\begin{aligned} H_{ng1}(j\omega_0) &= -\frac{\frac{g_{m1}}{j\omega_0 C_{gs1}}(R_s+j\omega_0 L_{eq}+j\omega_0 L_s)-\alpha_{gd1}(R_s+j\omega_0 L_{eq})}{R_s+j\omega_0 L_{eq}+\left(\omega_{T1}L_s+j\omega_0 L_s+\frac{1}{j\omega_0 C_{gs1}}\right)/\alpha_M}\cdot\frac{1}{\alpha_M(1+1/g_{m2}R_I)} \\ &\approx -\frac{g_{m1}(R_{eq}+j/\omega_0 C_{gs1})}{j\omega_0\alpha_M C_{gs1}(R_{eq}+R_{in})(1+1/g_{m2}R_I)}, \end{aligned} \tag{A.11}$$

where $\alpha_M \ll g_{m1}/\omega_0 C_{gs1}$. Using Eqs. (A.5), (A.6), (A.10), and (A.11), we have

$$\begin{aligned} \overline{|i_{o,nd1}|^2} &= |H_{nd1}(j\omega_0)|^2\,\overline{|i_{nd1}|^2} \\ &= \frac{4k_BT\gamma_1 g_{m1}R_{eq}^2(1+\alpha_{gd1})^2\Delta f}{\alpha_1\alpha_M^2(R_{eq}+R_{in})^2(1+1/g_{m2}R_I)^2}, \end{aligned} \tag{A.12}$$

$$\begin{aligned} \overline{i_{o,ngc1}\cdot i_{o,nd1}^*}+\overline{i_{o,nd1}\cdot i_{o,ngc1}^*} &= H_{ngc1}(j\omega_0)i_{ngc1}\cdot H_{nd1}^*(j\omega_0)i_{nd1}^*+H_{nd1}(j\omega_0)i_{nd1}\cdot H_{ngc1}^*(j\omega_0)i_{ngc1}^* \\ &= -2|c|\sqrt{\frac{\delta_1}{\kappa_1\gamma_1}}\frac{4k_BT\gamma_1 g_{m1}R_{eq}^2\Delta f}{\alpha_M(R_{eq}+R_{in})^2(1+1/g_{m2}R_I)^2}, \end{aligned} \tag{A.13}$$

$$\begin{aligned} \overline{|i_{o,ngc1}|^2}+\overline{|i_{o,ngu1}|^2} &= |H_{ng1}(j\omega_0)|^2\,\overline{|i_{ng1}|^2} \\ &= \frac{4k_BT\alpha_1\delta_1 g_{m1}(R_{eq}^2+1/\omega_0^2C_{gs1}^2)\Delta f}{\kappa_1\alpha_M^2(R_{eq}+R_{in})^2(1+1/g_{m2}R_I)^2}. \end{aligned} \tag{A.14}$$

Substituting Eqs. (A.12)–(A.14) into Eq. (A.9) gives the output noise current originating from M_1 as

$$\overline{|i_{o,M_1}|^2} = \frac{4k_BTR_{eq}\Delta f}{\alpha_M^2(R_{eq}+R_{in})^2(1+1/g_{m2}R_I)^2}\left(\frac{\gamma_1\chi_1}{\alpha_1}g_{m1}R_{eq}+\frac{\alpha_1\delta_1 g_{m1}}{\kappa_1\omega_0^2C_{gs1}^2R_{eq}}\right), \tag{A.15}$$

where χ_1 is given by Eq. (2.40). Dividing Eq. (A.15) by Eq. (A.4), we obtain F_{M_1} (Eq. (2.36)).

A.1.2 F_{M_2}

The noise contribution from M_2, F_{M_2}, can be derived in the same way as the derivation of F_{M_1}. The noise equivalent circuit of the common-gate stage, shown in Fig. A.2, gives the transfer

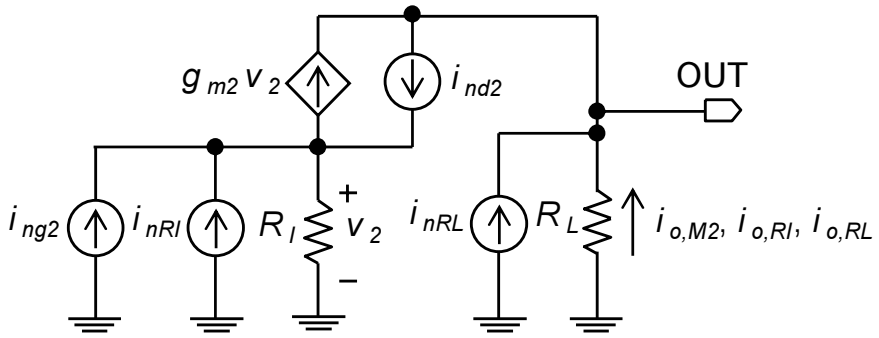

Figure A.2: Noise equivalent circuit of the common-gate stage

functions from the drain and induced-gate noise currents to the output currents:

$$H_{nd2}(j\omega_0) = \frac{1}{1+g_{m2}R_I}, \tag{A.16}$$

$$H_{ng2}(j\omega_0) = \frac{1}{1+1/g_{m2}R_I}, \tag{A.17}$$

respectively. Using Eqs. (A.5), (A.6), (A.16), and (A.17), we have

$$\overline{|i_{o,nd2}|^2} = \frac{4k_BT\gamma_2 g_{m2}}{\alpha_2(1+g_{m2}R_I)^2}, \tag{A.18}$$

$$\overline{i_{o,ngc2}\cdot i^*_{o,nd1}} + \overline{i_{o,nd2}\cdot i^*_{o,ngc2}} = 0, \tag{A.19}$$

$$\overline{|i_{o,ngc2}|^2} + \overline{|i_{o,ngu2}|^2} = \frac{4k_BT\delta_2\alpha_2(\omega_0 C_{gs2})^2}{\kappa_2 g_{m2}(1+1/g_{m2}R_I)^2}, \tag{A.20}$$

where $i_{o,nd2}$, $i_{o,ngc2}$ and $i_{o,ngu2}$ are the output noise currents due to i_{nd2}, i_{ngc2}, and i_{ngu2}, respectively. Using Eqs. (A.18)–(A.20), we obtain

$$\begin{aligned}\overline{|i_{o,M_2}|^2} &= \overline{|i_{o,nd2}|^2} + \overline{i_{o,ngc2}\cdot i^*_{o,nd2}} + \overline{i_{o,nd2}\cdot i^*_{o,ngc2}} + \overline{|i_{o,ngc2}|^2} + \overline{|i_{o,ngu2}|^2} \\ &= 4k_BT\frac{\gamma_2}{\alpha_2}\chi_2\frac{g_{m2}}{(1+1/g_{m2}R_I)^2}\Delta f,\end{aligned} \tag{A.21}$$

where χ_2 is given by Eq. (2.41). Dividing Eq. (A.21) by Eq. (A.4) gives F_{M_2} (Eq. (2.37)).

A.1.3 F_{R_I} and F_{R_L}

The noise currents due to the internal and load LC tanks are given by

$$\overline{|i_{nR_I}|^2} = \frac{4k_BT\Delta f}{R_I}, \tag{A.22}$$

$$\overline{|i_{nR_L}|^2} = \frac{4k_BT\Delta f}{R_L}, \tag{A.23}$$

respectively. From Fig. A.2, the output noise currents originating from the internal and load LC tanks are derived as

$$\overline{|i_{o,R_I}|^2} = \frac{4k_BT\Delta f}{R_I(1+1/g_{m2}R_I)^2}, \tag{A.24}$$

$$\overline{|i_{o,R_L}|^2} = \overline{|i_{nR_L}|^2} = \frac{4k_BT\Delta f}{R_L}, \tag{A.25}$$

respectively. Dividing Eqs. (A.24) and (A.25) by Eq. (A.4) gives F_{R_I} (Eq. (2.38)) and F_{R_L} (Eq. 2.39)), respectively.

A.2 Transformer Folded-Cascode LNA

The noise of M_1, M_2, R_I, and R_L contribute to the overall LNA noise. The LNA noise factor is given by

$$\begin{aligned} F &= \frac{\overline{|v_{o,R_s}|^2}+\overline{|v_{o,M_1}|^2}+\overline{|v_{o,M_2}|^2}+\overline{|v_{o,R_I}|^2}+\overline{|v_{o,R_L}|^2}}{\overline{|v_{o,R_s}|^2}}, \\ &= 1 + F_{M_1} + F_{M_2} + F_{L_I} + F_{L_L}, \end{aligned} \tag{A.26}$$

where v_{o,R_s}, v_{o,M_1}, v_{o,M_2}, v_{o,R_I}, and v_{o,R_L} are the output noise voltages originating from R_s, M_1, M_2, R_I, and R_L, respectively.

The output noise voltage originating from R_s, v_{o,R_s}, can be derived from the noise equivalent circuit of the input stage, shown in Fig. A.3. The signal source noise current is expressed as

$$\overline{|i_{ns}|^2} = \frac{4k_BT\Delta f}{R_s}, \tag{A.27}$$

where k_B is Boltzmann's constant, T the absolute temperature, and Δf the noise bandwidth. The transfer function from i_{ns} to the noise current at node I, $i_{I,Rs}$, is given by

$$H_{ns}(j\omega_0) = \frac{g_{m1}R_s}{j\omega_0\alpha_M C_{gs1}\,(R_s+\omega_T L_s/\alpha_M)}, \tag{A.28}$$

where Im[$Z_{in}(j\omega_0)$]=0 and α_M is approximated as Re[α_M] for input impedance matching as shown in Section 3.1. Using Eq. (A.28), we have

$$\begin{aligned} \overline{|i_{I,Rs}|^2} &= |H_{ns}(j\omega_0)|^2\,\overline{|i_{ns}|^2} \\ &= \frac{4k_BTR_s\omega_{T1}^2\Delta f}{\omega_0^2|\alpha_M|^2(R_s+\omega_T L_s/|\alpha_M|)^2}. \end{aligned} \tag{A.29}$$

The common-gate stage converts $i_{I,Rs}$ to the output voltage:

$$\overline{|v_{o,Rs}|^2} = |Z_T|^2\,\overline{|i_{I,Rs}|^2}, \tag{A.30}$$

where Z_T is the transimpedance of the common-gate stage and is given by Eq. (3.14).

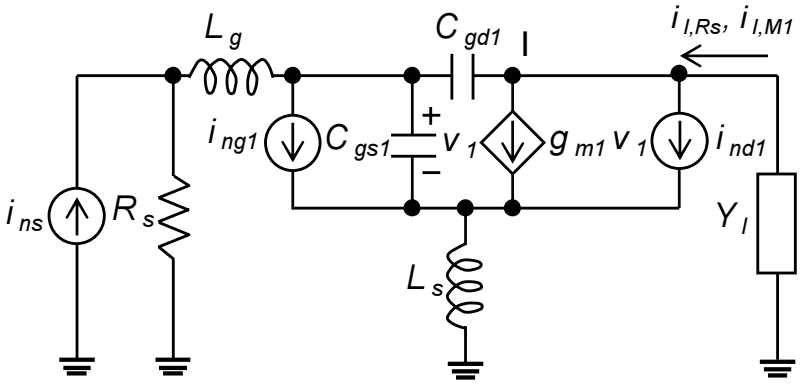

Figure A.3: Noise equivalent circuit of the input stage.

A.2.1 F_{M_1}

The noise current of M_1 is also converted by the common-gate stage. The noise contribution from M_1 can be expressed as

$$F_{M_1} = \frac{\overline{|v_{o,M_1}|^2}}{\overline{|v_{o,R_s}|^2}} = \frac{|Z_T|^2\overline{|i_{I,M_1}|^2}}{|Z_T|^2\overline{|i_{I,R_s}|^2}} = \frac{\overline{|i_{I,M_1}|^2}}{\overline{|i_{I,R_s}|^2}}, \tag{A.31}$$

where i_{I,M_1} is the noise current at node I as shown in Fig. A.3.

The main noise sources in a MOSFET are the drain noise current i_{nd} and induced-gate noise current i_{ng}, expressed as Eqs. (A.5) and (A.6), respectively. Considering the correlation between i_{nd} and i_{ng}, we can express the noise current due to M_1 at node I as

$$\begin{aligned}\overline{|i_{I,M_1}|^2} =& \overline{|i_{I,nd1} + i_{I,ng1}|^2} \\ =& \overline{|i_{I,nd1} + i_{I,ngc1}|^2} + \overline{|i_{I,ngu1}|^2} \\ =& \overline{|i_{I,nd1}|^2} + \overline{i_{I,ngc1}\cdot i^*_{I,nd1}} + \overline{i_{I,nd1}\cdot i^*_{I,ngc1}} + \overline{|i_{I,ngc1}|^2} + \overline{|i_{I,ngu1}|^2},\end{aligned} \tag{A.32}$$

where $i_{I,nd1}$, $i_{I,ngc1}$, and $i_{I,ngu1}$ are the noise currents due to i_{nd1}, i_{ngc1}, and i_{ngu1} at node I, respectively. From Fig. A.3, the transfer function from i_{nd1} to $i_{I,nd1}$ is approximated as

$$\begin{aligned}H_{nd1}(j\omega_0) &= \frac{(R_s + j\omega_0 L_g)(1+\alpha_{gd1}) + j\omega_0 L_s + \frac{1}{j\omega_0 C_{gs1}}}{R_s + j\omega_0 L_g + \left(\omega_{T1} L_s + j\omega_0 L_s + \frac{1}{j\omega_0 C_{gs1}}\right)/\alpha_M} \cdot \frac{1}{\alpha_M} \\ &\approx \frac{R_s(1+\alpha_{gd1})}{\alpha_M(R_s + \omega_{T1}L_s/\alpha_M)},\end{aligned} \tag{A.33}$$

where $j\omega_0(L_g + L_s/\alpha_M) + 1/j\omega_0\alpha_M C_{gs1} \simeq 0$ under input impedance matching condition. The

transfer function from i_{ng1} to $i_{I,ng1}$ is also approximated as

$$H_{ng1}(j\omega_0) = -\frac{\frac{g_{m1}}{j\omega_0 C_{gs1}}\left(R_s + j\omega_0 L_g + j\omega_0 L_s\right) - \alpha_{gd1}\left(R_s + j\omega_0 L_g\right)}{R_s + j\omega_0 L_g + \left(\omega_{T1} L_s + j\omega_0 L_s + \frac{1}{j\omega_0 C_{gs1}}\right)/\alpha_M} \cdot \frac{1}{\alpha_M}$$
$$\approx -\frac{g_{m1}\left(R_s + j\frac{1}{\omega_0 C_{gs1}}\right)}{j\omega_0 \alpha_M C_{gs1}\left(R_s + \omega_{T1} L_s/\alpha_M\right)}, \tag{A.34}$$

where $\alpha_M \ll g_{m1}/\omega_0 C_{gs1}$ and $j\omega_0(L_g + L_s/\alpha_M) + 1/j\omega_0\alpha_M C_{gs1} \simeq 0$. Using Eqs. (A.5), (A.6), (A.33), and (A.34), we have

$$\overline{|i_{I,nd1}|^2} = |H_{nd1}(j\omega_0)|^2\,\overline{|i_{nd1}|^2}$$
$$= \frac{4k_B T\gamma_1 g_{m1} R_s^2\left(1+\alpha_{gd1}\right)^2 \Delta f}{\alpha_1|\alpha_M|^2(R_s + \omega_{T1}L_s/|\alpha_M|)^2}, \tag{A.35}$$

$$\overline{i_{I,ngc1}\cdot i_{I,nd1}^*} + \overline{i_{I,nd1}\cdot i_{I,ngc1}^*} = H_{ngc1}(j\omega_0) i_{ngc1}\cdot H_{nd1}^*(j\omega_0) i_{nd1}^* + H_{nd1}(j\omega_0) i_{nd1}\cdot H_{ngc1}^*(j\omega_0) i_{ngc1}^*$$
$$= -2|c|\sqrt{\frac{\delta_1}{\kappa_1\gamma_1}}\frac{4k_B T\gamma_1 g_{m1} R_s^2\left(1+\alpha_{gd1}\right)\Delta f}{|\alpha_M|^2(R_s + \omega_{T1}L_s/|\alpha_M|)^2}, \tag{A.36}$$

$$\overline{|i_{I,ngc1}|^2} + \overline{|i_{I,ngu1}|^2} = |H_{ng1}(j\omega_0)|^2\,\overline{|i_{ng1}|^2}$$
$$= \frac{4k_B T\alpha_1\delta_1 g_{m1}\left(R_s^2 + \frac{1}{\omega_0^2 C_{gs1}^2}\right)\Delta f}{\kappa_1|\alpha_M|^2(R_s + \omega_{T1}L_s/|\alpha_M|)^2}. \tag{A.37}$$

Substituting Eqs. (A.35)–(A.37) into Eq. (A.32) gives the noise current of M_1 at node I:

$$\overline{|i_{I,M_1}|^2} = \frac{4k_B T R_s \Delta f}{|\alpha_M|^2(R_s + \omega_{T1}L_s/|\alpha_M|)^2}\left(\frac{\gamma_1\chi_1}{\alpha_1} g_{m1} R_s + \frac{\alpha_1\delta_1 g_{m1}}{\kappa_1\omega_0^2 C_{gs1}^2 R_s}\right), \tag{A.38}$$

where χ_1 is given by Eq. (3.22). Substituting Eqs. (A.29) and (A.38) into Eq. (A.31) gives F_{M_1} (Eq. (3.21)).

A.2.2 F_{M_2}

In the common-gate topology, the gate-induced noise current of the MOSFET can be ignored against the drain noise current:

$$\overline{|v_{o,M_2}|^2} \approx \overline{|v_{o,nd2}|^2}, \tag{A.39}$$

where $v_{o,nd2}$ is the output voltage originating from the drain noise current of M_2, i_{nd2}, and is derived from the noise equivalent circuit of the common-gate stage, shown in Fig. A.4:

$$\overline{|v_{o,nd2}|^2} = \left|\frac{N_{nd2}}{Y_0 + Y_I}\right|^2 \overline{|i_{nd2}|^2}$$
$$= \left|\frac{N_{nd2}}{Y_0 + Y_I}\right|^2 \cdot 4k_B T\frac{\gamma_2}{\alpha_2} g_{m2}\Delta f, \tag{A.40}$$

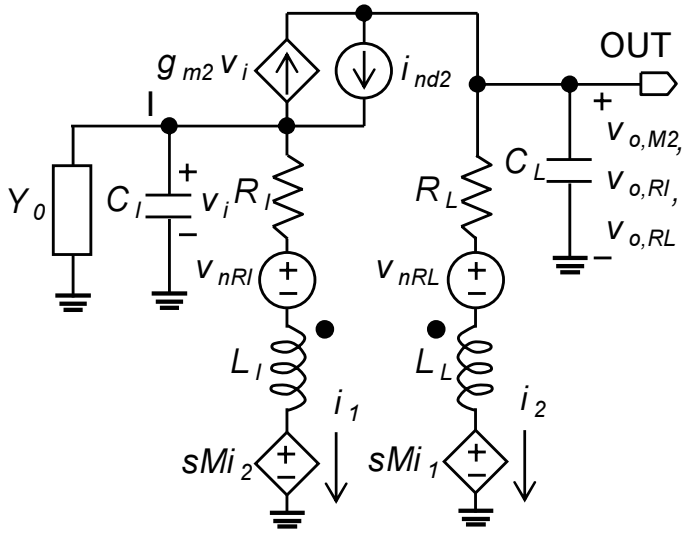

Figure A.4: Noise equivalent circuit of the common-gate stage.

$$N_{nd2} = -\left(j\omega L_L + R_L - \frac{(j\omega M)^2}{j\omega L_I + R_I}\right)(Y_0 + Y_{L_I C_I}) + \frac{j\omega M}{j\omega L_I + R_I}\left(1 - \frac{j\omega M}{j\omega L_I + R_I}\right)$$
$$\approx -j\omega n^2(1-k^2)L_I \cdot (Y_0 + Y_{L_I C_I}) + nk(1-nk), \tag{A.41}$$

where R_I and R_L are ignored for simplicity; Y_0 represents the output admittance of the input stage at node I; $Y_{L_I C_I} = j\omega C_I + 1/(j\omega L_I + R_I)$, as shown in Section 3.3. Rewriting Eq. (A.30) in terms of $Y_0 + Y_I$, we have

$$\overline{|v_{o,Rs}|^2} = \left|\frac{N_{ns}}{Y_0 + Y_I}\right|^2 \left|\frac{Y_0 + Y_I}{Y_I}\right|^2 \overline{|i_{I,Rs}|^2}, \tag{A.42}$$

$$N_{ns} = \frac{j\omega M}{j\omega L_I + R_I} + g_{m2}\left(j\omega L_L + R_L - \frac{(j\omega M)^2}{j\omega L_I + R_I}\right)$$
$$\approx nk + g_{m2} \cdot j\omega n^2(1-k^2)L_I, \tag{A.43}$$

where R_I and R_L are ignored for simplicity. Dividing Eq. (A.40) by Eq. (A.42) with $L_I = 1/\omega_0^2(1+k)C_L$ and $n = 1$, we obtain F_{M_2} (Eq. (3.23)).

A.2.3 F_{L_I} and F_{L_L}

The noise voltages of the parasitic resistances of L_I and L_L are given by

$$\overline{|v_{nR_I}|^2} = 4k_B T R_I \Delta f, \tag{A.44}$$

$$\overline{|v_{nR_L}|^2} = 4k_B T R_L \Delta f, \tag{A.45}$$

respectively. The output noise voltages due to v_{nR_I} and v_{nR_L} can be expressed from Fig. A.4:

$$\overline{|v_{o,R_L}|^2} = \left|\frac{N_{nR_L}}{Y_0 + Y_I}\right|^2 \overline{|v_{nR_L}|^2}, \tag{A.46}$$

$$\begin{aligned} N_{nR_L} &= g_{m2}\left(1 - \frac{j\omega M}{j\omega L_I + R_I}\right) + Y_0 + Y_{L_I C_I} \\ &\approx g_{m2}(1 - nk) + Y_0 + Y_{L_I C_I} \end{aligned} \tag{A.47}$$

and

$$\overline{|v_{o,R_I}|^2} = \left|\frac{N_{nR_I}}{Y_0 + Y_I}\right|^2 \overline{|v_{nR_I}|^2} \tag{A.48}$$

$$\begin{aligned} N_{nR_I} &= g_{m2}\left(\frac{j\omega L_L + R_L}{j\omega L_I + R_I} - \frac{j\omega M}{j\omega L_I + R_I}\right) - \frac{j\omega M}{j\omega L_I + R_I}\left(Y_0 + j\omega C_I\right) \\ &\approx n(n-k)g_{m2} - nk\left(Y_0 + j\omega C_I\right), \end{aligned} \tag{A.49}$$

respectively, where R_I and R_L are ignored for simplicity. Dividing Eqs. (A.46) and (A.48) by Eq. (A.42) with $L_I = 1/\omega_0^2(1+k)C_L$ and $n = 1$, we derive F_{L_I} (Eq. (3.24)) and F_{L_L} (Eq. (3.25)), respectively.

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Appendix B

Frequency Responses of Y_I and $1/Y_I$

B.1 Y_I

The frequency response of Y_I of the transformer folded-cascode CMOS LNA is shown in Fig. B.1(a). At low frequencies ($1 \gg -\omega^2(1-k^2)L_LC_L + j\omega R_LC_L$), Eq. (3.3) can be approximated as

$$\text{Re}[Y_I] \approx g_{m2}(1-nk), \tag{B.1}$$

$$\text{Im}[Y_I] \approx \omega\left(C_I + n^2k^2C_L\right) - \frac{1}{\omega L_I}, \tag{B.2}$$

which shows that Im[Y_I] becomes zero around

$$w_{0,Y_I} = \frac{1}{\sqrt{L_I\left(C_I + n^2k^2C_L\right)}}. \tag{B.3}$$

At $\omega_{1,Y_I} = 1/\sqrt{(1-k^2)L_LC_L}$, Re[$Y_I$] exceeds g_{m2} and Im[Y_I] becomes a maximum:

$$\text{Re}[Y_I] \approx g_{m2} + \frac{n^2k^2}{R_L}, \tag{B.4}$$

$$\text{Im}[Y_I] \approx \omega_{1,Y_I}C_I - \frac{1}{\omega_{1,Y_I}L_I} + \frac{nkg_{m2}}{\omega_{1,Y_I}R_LC_L}, \tag{B.5}$$

respectively, where $1 - \omega_{1,Y_I}^2(1-k^2)L_LC_L \simeq 0$. Above ω_{1,Y_I}, Re[Y_I] and Im[Y_I] approach gradually g_{m2} and $\omega C_I - 1/\omega L_I$, respectively.

B.2 $1/Y_I$

The reverse of Y_I is expressed as

$$\frac{1}{Y_I} = \frac{sC_L + \frac{1}{s(1-k^2)L_L + R_L}}{D}, \tag{B.6}$$

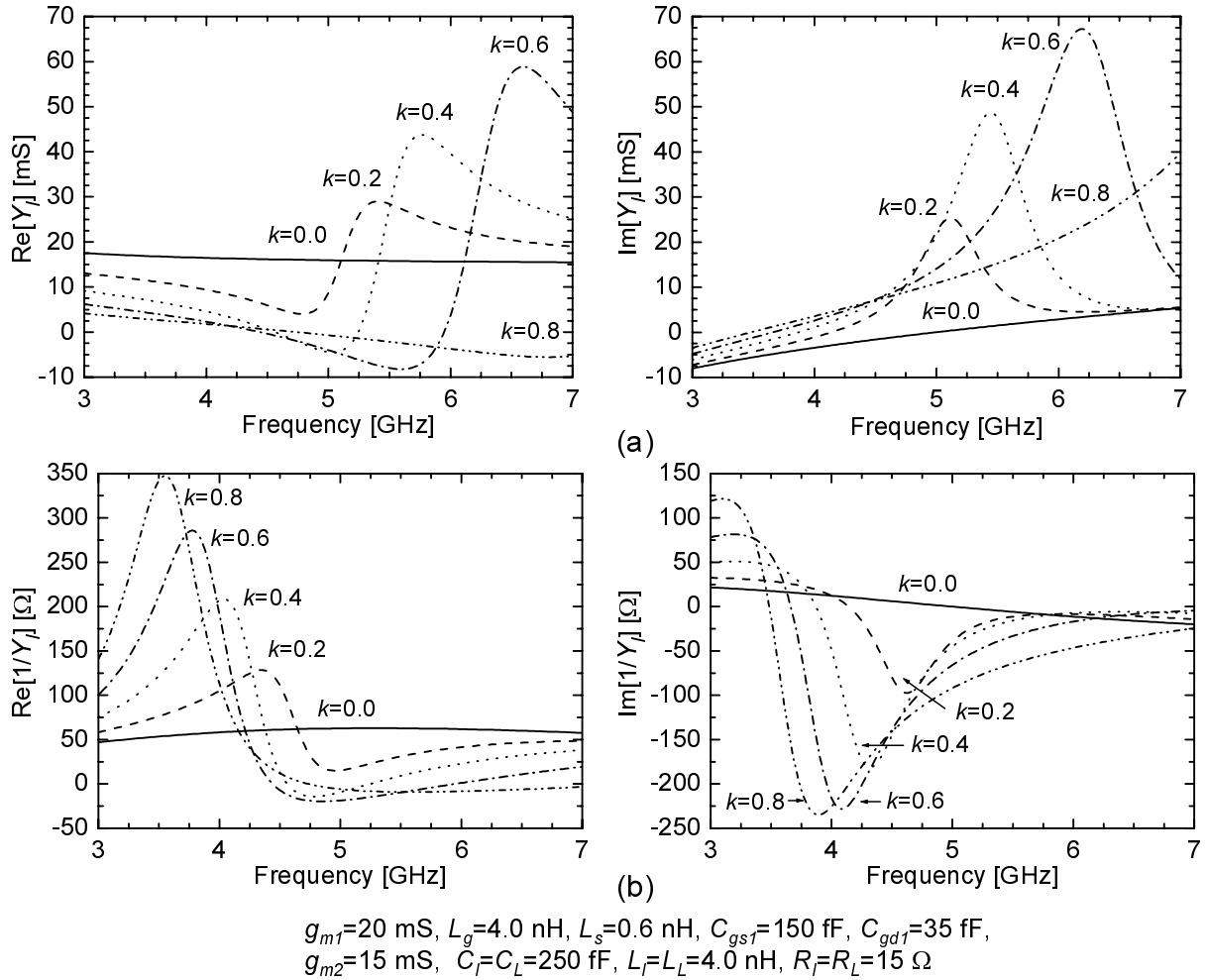

Figure B.1: Calculated (a) Y_I and (b) $1/Y_I$ with k as a parameter.

where D is given by Eq. (3.15). Figure B.1(b) shows the calculated frequency response of $1/Y_I$ with k as a parameter. At low frequencies ($\omega \simeq 0$), $1/Y_I$ is approximated as

$$\mathrm{Re}\left[\frac{1}{Y_I}\right] \approx \frac{R_I}{1 + R_I g_{m2}(1 - nk)}, \tag{B.7}$$

$$\mathrm{Im}\left[\frac{1}{Y_I}\right] \approx 0. \tag{B.8}$$

Equation (3.15) indicates that Re$[1/Y_I]$ and Im$[1/Y_I]$ have peaks around ω_p, given by Eq. (3.18). Above ω_p, Re$[1/Y_I]$ and Im$[1/Y_I]$ approach gradually $1/g_{m2}$ and $1/(\omega C_I - 1/\omega L_I)$, respectively.

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