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Study on Ultra-Thin Silicon Dioxide Layer Formed by Nitric Acid Oxidation Method and Application to Ultra-low Power Poly-Si TFT

（硝酸酸化法により形成した極薄二酸化シリコン膜と
その超低消費電力多結晶シリコン薄膜トランジスタへの
応用に関する研究）

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February, 2012

Preface

This thesis is the corpus of the study on a nitric acid oxidation method and its application to poly-crystalline silicon thin film transistors, which I have worked at the Institute of Science and Industrial Research, Osaka University, from 2010 to 2012 under the guidance of Dr. Hikaru Kobayashi and his group.

In Section I, I show the background and the object of this study as an introduction. In Section II, a novel direct oxidation method of Si at low temperature, the NAOS method, is described, and the properties of Si films and SiO_2/Si interfaces are also discussed in detail. In Section III, I demonstrate that the excellent characteristics of MOS diodes with NAOS films are applicable to the gate insulators of polycrystalline silicon thin film transistors. The electrical characteristics of the poly-crystalline silicon thin film transistors are shown in Section IV, and I demonstrate a vast decrease in power consumption of electrical circuits and LCD panels as applications of the NAOS films in Section V. In Section VI, the conclusions of this study are summarized.

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I. Introduction

I – 1. Background

A silicon dioxide (SiO_2) layer and its interface with silicon (Si) have been studied widely for several decades, because they greatly affect electrical properties of semiconductor devices. Thermally grown SiO_2 is proven to possess excellent properties [1,2], and thus it is generally used for the gate insulator in metal-oxide-semiconductor (MOS) transistors [3].

However, it is difficult to achieve both the excellent properties and the low temperature formation at the same time. Figure 1-1 compares SiO_2 layers formed by a deposition method (a) and a direct oxidation method (b).

In the case of the deposition method such as chemical vapor deposition (CVD), interfacial characteristics are poor due to incomplete chemical bond formation and presence of metal contaminants before deposition, leading to a high interface state density [4-6]. Moreover, an SiO_2 layer with a uniform thickness cannot be produced, especially on rough surfaces such as poly-crystalline silicon (poly-Si) thin films with a ridge structure [7]. A high-density leakage current flows through thin SiO_2 regions (i.e., in the top regions of the ridge structure). The bulk properties are also poor due to a low atomic density and incorporation of undesirable species such as water and hydrocarbon [8-11].

In the case of the direct oxidation method, on the other hand, a uniform thickness SiO_2 layer can be formed even on rough Si surfaces. The SiO_2/Si interface is formed in the Si bulk before the formation, and therefore the interface is much cleaner. Formation of the interfacial chemical bonds is more complete, leading to much less Si dangling bonds which act as interface states. An SiO_2 layer formed by the direct oxidation method is denser with a much higher purity, resulting in better bulk properties (e.g., low tunneling probability of charge carriers) [12-16]. Due to these excellent properties, a leakage current flowing through SiO_2 can be suppressed, which makes it possible to use a thinner gate oxide layer. The thinner gate oxide layer, in turn, enables to miniaturize semiconductor devices such as thin film transistors (TFTs), leading to high performance and low fabrication cost.

Recently, mobile equipments, such as cellular phones, tablet computers,

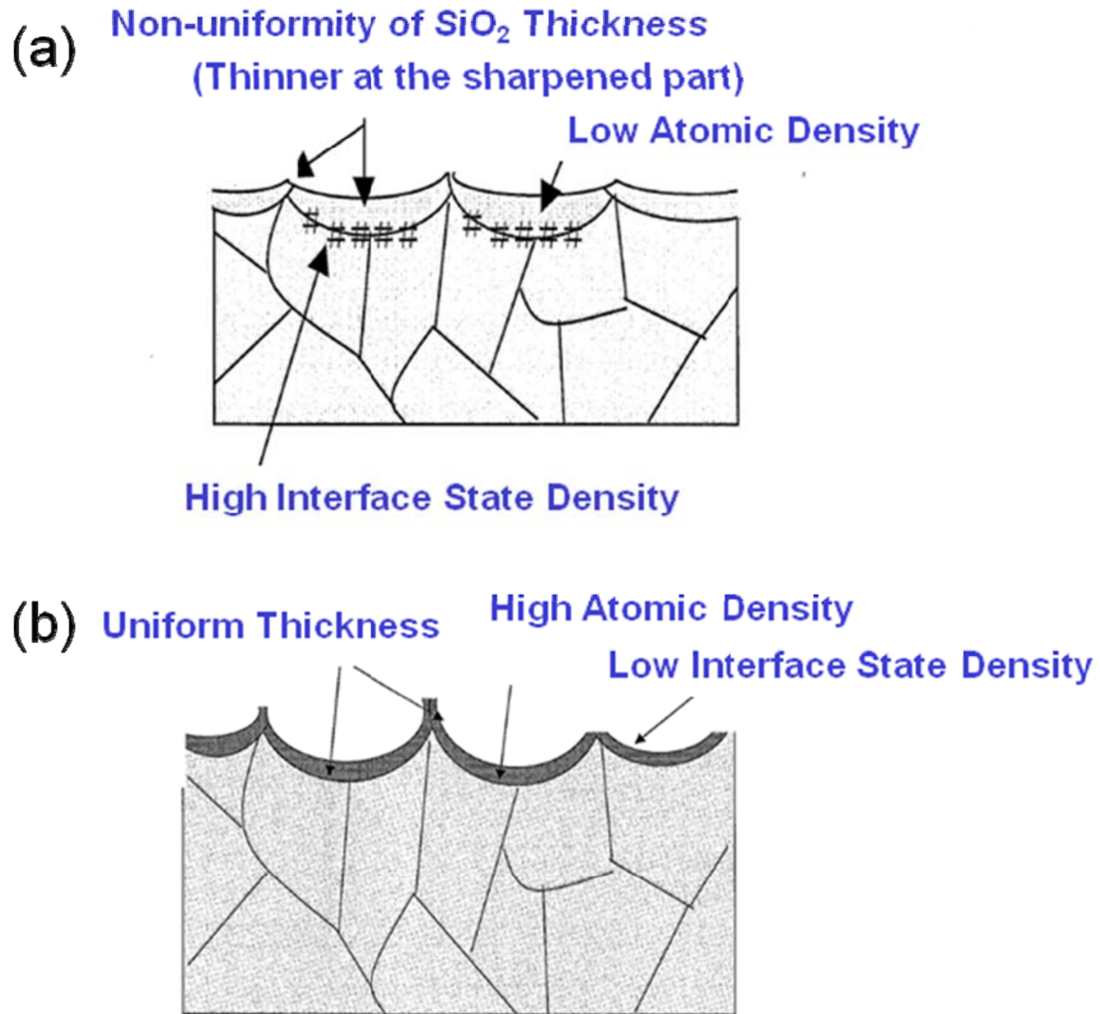

Figure 1-1. Schematic cross-sections of thin SiO_2/poly-Si thin film structures fabricated by the following methods: (a) conventional CVD; (b) direct oxidation.

notebook computers, portable music players, and mobile games shown in Figure 1-2, have been widely popularized with the wireless internet environment, leading to lifestyle changes.

Power consumption by these equipments tends to increase significantly when they have high performance and additional functions. For these equipments, the input/output interface plays the most important role, and most of the mobile

Figure 1-2. Various mobile equipments operated by batteries are widely used in the world.

equipments are furnished with display devices as the output interface. The performance of the display device installed in the mobile equipments has been improved year after year, e.g., larger display size, higher definition, higher brightness, wider viewing angle, shorter response time, and narrower bezel size.

Among many kinds of display devices such as liquid crystal displays (LCDs), organic light emitting diodes (OLEDs), and electronic papers, LCDs are utilized most widely for various equipments because of their high cost performance. Especially, LCDs based on the poly-Si TFTs are used widely for mobile equipments, because they can realize small-size and high-resolution displays which are suitable for their applications.

These mobile equipments are usually operated by batteries (primary cells or rechargeable batteries), and the period of use is determined by the battery capacity and the power consumption. Therefore, decreasing the power consumption, which contributes to increase period of use and downsize the batteries, is very significant at the point of the product concept. In this situation, low power consumption of the mobile equipments is strongly required. Moreover, the trend of the low power consumption is accelerated in every field because of the supply-demand of electric

energy and the protection of the global environment.

The display devices, as the output interface, are required to show more information and all the times. However, satisfying these requirements increase power consumption. As describe above, a vast reduction of power consumption is one of the most significant issues for display devices.

I – 2. Object of Study

Consumed power of display devices is divided into two portions, i.e., the backlight system and the electronic system (circuit and driving method). In this study, I focus the electronic system, assuming the reflective display with no backlight for ultimately low power consumption. As described above, low power consumption is strongly required for electronic devices, especially for mobile equipments, and LCDs are widely used for mobile application because of their power consumption lower than those of other display devices. LCDs are usually fabricated on glass substrates, and are often driven by peripheral circuits composed of poly-Si TFTs.

Ignoring a leakage current, consumed power, P, of the circuits is expressed as [17]

$$P = fCV^2 \tag{1-1}$$

where f is a signal frequency, C is a charging and discharging capacitance, and V is a supply voltage. Therefore, consumed power can be decreased by a reduction of f, C, and/or V.

In order to achieve a decrease of the operation voltage of the circuits, the threshold voltage should be decreased to less than about a half of the operation voltage. On the other hand, the leakage current of TFTs becomes large when the TFTs are in the depletion mode (normally-on). Therefore, the threshold voltage should be controlled within a narrow range, which can be realized by a small sub-threshold coefficient, for low voltage operation. Furthermore, a large on-current (I_{on}) is also significant to function the circuits with desired performance at a low

operation voltage, and I_{on} is related to the TFT dimension and the carrier mobility.

For improvement of electrical characteristics of TFTs, a decrease in the thickness of a gate insulating layer is indispensable. The decrease in the gate insulator thickness can reduce the operation voltage, leading to a vast decrease in the power consumption because it is proportional to the square of the operation voltage as described in Equation (1-1). Moreover, the decrease in the gate insulator thickness makes it possible to miniaturize TFTs, which greatly improves electrical characteristics of TFTs.

It is well known that the consumed power is inversely proportional to the square of the scaling factor, *K*, referring to Dennerd's scaling law [18]. This law indicates that the device dimension (length, width, and thickness) is scaled by *K*. Table 1-1 shows the relation between the device parameters and their scaling factors

Parameter		Scaling Factor
Channel Length	L	1/K
Channel Width	W	1/K
Gate Insulator Thickness	T_{OX}	1/K
Impurity Concentration	N	K
Junction depth	x_j	1/K
Power Supply Voltage	V_{DD}	1/K
Device Area	S	$1/K^2$
Electric Field	E	1
Parasitic Capacitance	C	1/K
Current	I	1/K
Power Consumption	P	$1/K^2$
Delay Time	t	1/K

Table 1-1. The scaling law for LSI proposed by Dennerd.

suggested by Dennerd's scaling law, and Figures 1-3 and 1-4 show the device structures of a MOS transistor and a TFT. This law indicates that when device dimension and supply voltage are scaled by K, the delay time is inversely proportional to K and the power consumption to K^2. This scaling law suggests that shrinkage of the TFTs, especially the channel length and the gate insulator thickness, is very important for a decrease in the power consumption. Consequently, one of the key factors is to achieve an extremely thin gate insulator with high performance, i.e., low leakage current and low interface state density.

On the other hand, the carrier mobility is affected strongly by crystallinity of poly-Si films, and also by interface properties between the gate insulator and the poly-Si film [19-20].

In my thesis, I have focused on the fabrication process for poly-Si TFTs, especially the formation method of an ultra-thin gate insulator, which possesses high performance and process capability of fabricating at low temperature on a glass substrate.

Direct oxidation methods such as thermal oxidation can form an SiO_2 film with excellent electrical characteristics [1,2]. However, conventional thermal oxidation needs high temperature above 800 °C, and therefore this method cannot be applied to TFTs on glass substrates whose softening temperature is below 500 °C. On the other hand, the nitric acid oxidation of Si (NAOS) method can oxidize Si at temperatures below 120 °C to form an SiO_2 film. In my thesis, I have analyzed properties of the NAOS oxide film and its interface. In addition, I have achieved excellent electrical characteristics of poly-Si TFTs with the NAOS gate insulator and the circuit performance composed of these TFTs.

The main object of this study is to fabricate a high quality SiO_2 layer at lower temperature (below softening temperature of glass), to evaluate the oxidation mechanism, and to investigate properties of the SiO_2 film and its interface, all of which result in formation of an SiO_2 film with extremely high quality on a glass substrate.

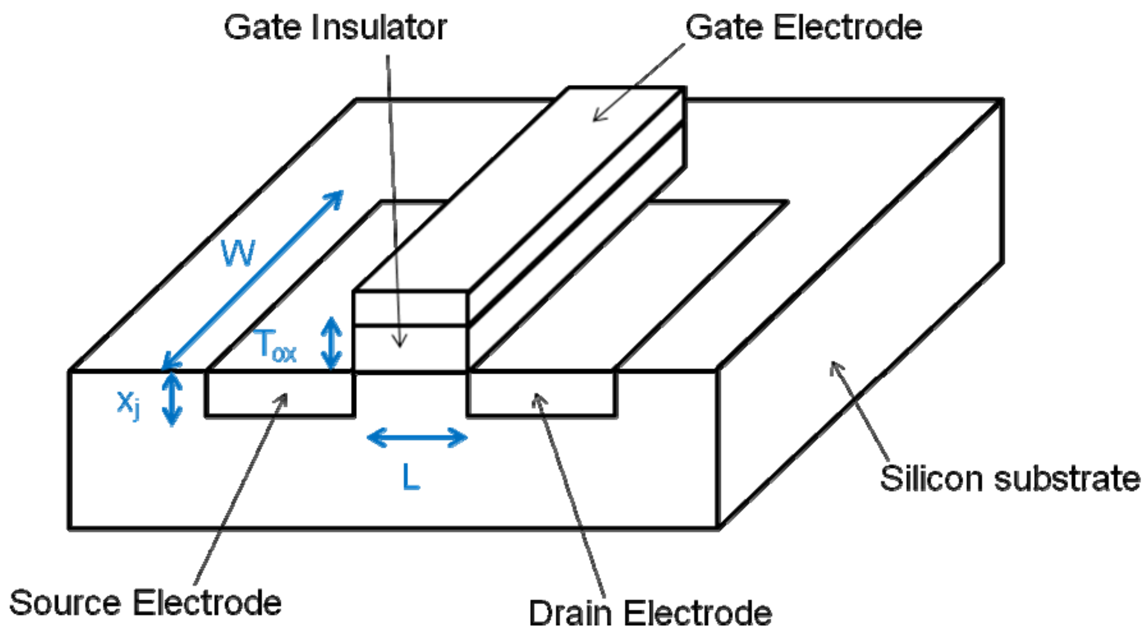

Figure 1-3. Structure of a silicon-based MOS transistor. L : channel length, W : channel width, T_{ox} : gate insulator thickness, x_j : junction depth.

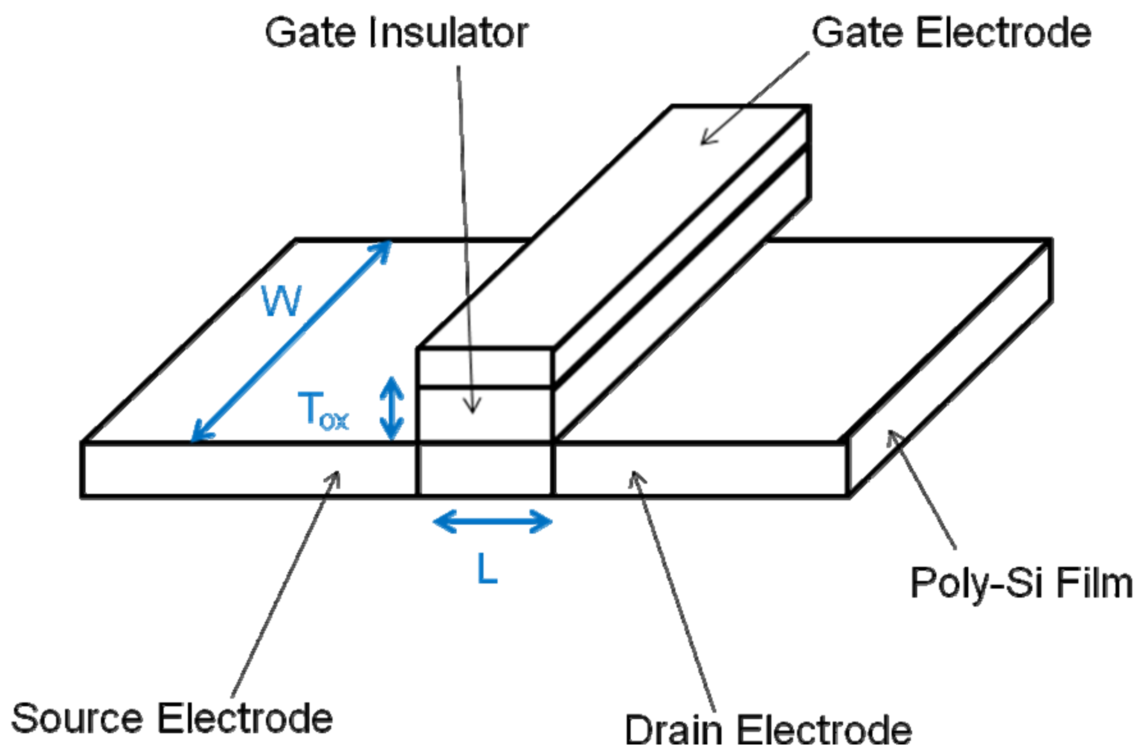

Figure 1-4. Structure of a poly-Si-based TFT. L : channel length, W : channel width, T_{ox} : gate insulator thickness.

The other object is to demonstrate that the NAOS SiO_2 film can be utilized as the gate insulator of poly-Si TFTs to achieve ultra-low power consumption. I would like to aim to decrease the consumed power for driving LCDs to less than 1/100 than that fabricated using the conventional technologies.

I – 3. Previous Studies

According to the Dennerd's scaling law, miniaturization is very effective for a reduction of power consumption [18]. However, miniaturization is much more difficult for TFTs than LSIs mainly because of a much thicker gate insulating layer in the range of 80~150 nm and the use of poly-Si instead of single crystalline Si.

Since TFTs are usually produced on glass substrates whose softening temperature is lower than 500 °C [20-22], high temperature processes such as thermal oxidation of Si (≥800 °C) are unavailable. Consequently, a gate insulating layer is usually formed by deposition methods such as plasma-enhanced chemical vapor deposition (PE-CVD) [23-28]. However, the deposition methods have following demerits: i) incomplete interfacial bond formation and presence of contaminants, both leading to poor interfacial characteristics such as high interface state densities [4-6], ii) poor bulk characteristics due to porous structure and inclusion of undesirable species such as hydrocarbon and hydroxyl species [8-11], iii) difficulty in formation of a uniform thickness insulating layer, especially on rough poly-Si surfaces arising from laser annealing of amorphous Si films to crystallize [4], as shown in Figure 1-1 (a).

The demerit i) results from a phenomenon that an initial Si surface becomes an SiO_2/Si interface after the SiO_2 deposition. This disadvantage can be avoided by direct oxidation methods because the SiO_2/Si interface is formed in Si bulk before oxidation. Concerning the demerit ii), it is well known that a thermally grown SiO_2 layer possesses a higher density than a deposited oxide layer [1,2], leading to better electrical characteristics. Concerning the demerit iii), the direct oxidation method can form a uniform thickness SiO_2 layer even on rough surfaces such as poly-Si thin

films [16] since the oxidation rate in the NAOS method is independent of Si surface orientations.

Extensive studies have been performed for developing direct Si oxidation methods at low temperatures including plasma oxidation [29-32], photo-oxidation [33,34], ozone oxidation [35,36], metal-promoted oxidation [37-38], etc.

In order to solve the above problems for deposition methods, a low temperature direct Si oxidation method, i.e., the NAOS method, has been developed in this study. This method simply involves immersion of Si in high concentration (i.e., 68~98 wt%) nitric acid (HNO_3) aqueous solutions at temperatures below 120°C. By use of the NAOS method using e.g., azeotropic HNO_3 aqueous solutions (cf. 68 wt% HNO_3), an ultra-thin (i.e., 1.1~1.8 nm) SiO_2 layer with a leakage current density much lower than that of a thermally grown SiO_2 layer with the same thickness can be formed.

II. Formation of Ultra-Thin SiO_2 Layer by the NAOS Method

II -1. Mechanism of Oxidation

In order to form a thin SiO_2 film with excellent properties, I have adopted the NAOS method in which Si substrates or poly-Si thin films are immersed in HNO_3 aqueous solutions. The reaction of the SiO_2 formation is described by the following chemical equations;

$$4HNO_3 \rightleftarrows 4H^+ + 4NO_3^- \quad (2\text{-}1)$$

$$4NO_3^- \rightarrow 4NO_2 + 4O^- \quad (2\text{-}2)$$

$$Si + 2O^- \rightarrow SiO_2 + 2e^- \quad (2\text{-}3)$$

$$4H^+ + 2O^- + 2e^- \rightarrow 2H_2O \quad (2\text{-}4)$$

The oxidation equipment used for the NAOS method is shown in Figure 2-1.

Figure 2-1. Photograph of the equipment for the NAOS oxidation.

I think that oxidation by the HNO_3 aqueous solutions can proceed smoothly even at low temperatures below 120 °C for the following reasons.

1) Dissociated oxygen ions (O^-) are produced by decomposition of HNO_3 and/or NO_3^-, and they oxidize Si at low temperatures due to low activation energy for the reaction.
2) Dissociated oxygen ions, which are smaller than oxygen molecules (O_2), can easily diffuse through SiO_2 and reach at the SiO_2/Si interface as shown in Figure 2-2.

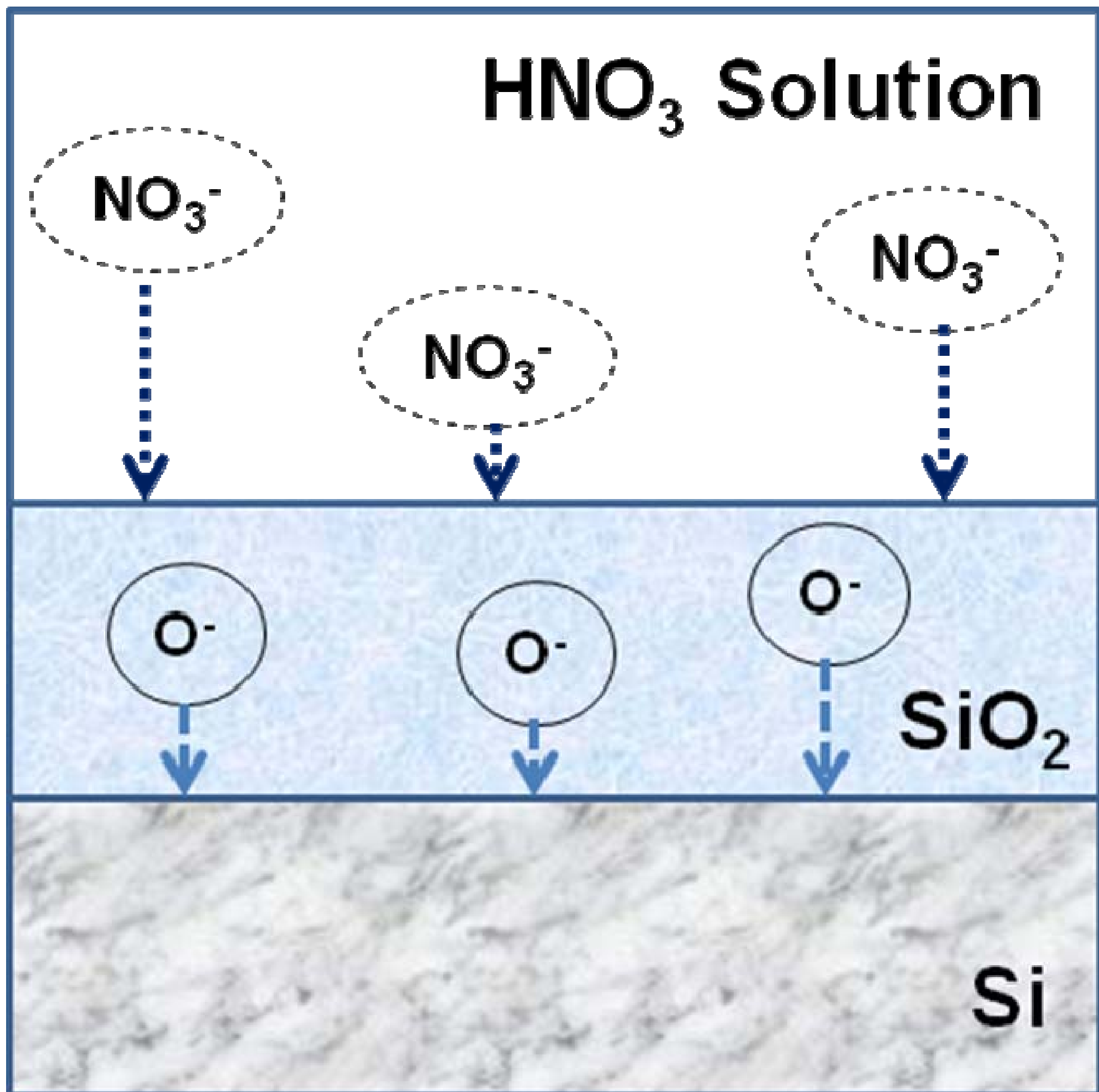

Figure 2-2. Mechanism of nitric acid oxidation of silicon (NAOS).

Because of the above two reasons, an ultra-thin (i.e., 1.1~1.8 nm) SiO_2 layer can be formed by the NAOS method at temperature below than 120 °C.

For the NAOS method, it is considered that there are other advantages as explained below.

1) Since the NAOS method is the direct oxidation method, the SiO_2/Si interface is not exposed by atmosphere and/or solutions during the oxidation process, leading to avoidance of contaminations at the interface, which results in clean interface.
2) Since the oxidation temperature is lower than the glass softening temperature, the deformation of the glass substrate and contamination such as sodium (Na) from the glass substrate can be avoided.

Figure 2-3 is the phase diagram of HNO_3 aqueous solutions. In the NAOS method, azeotropic HNO_3 aqueous solutions, i.e. 68 wt% HNO_3, is expected to form an

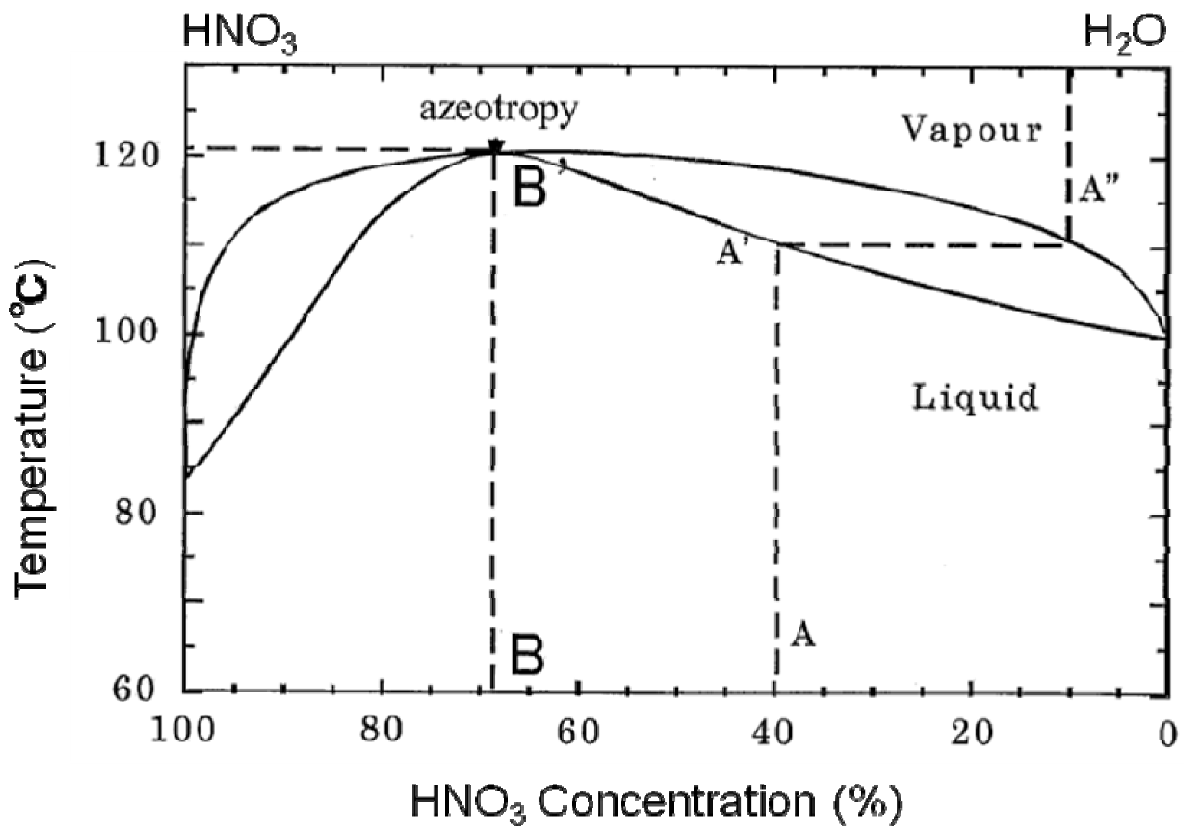

Figure 2-3. Phase diagram of the HNO_3 aqueous solutions. The concentration of azeotropic solution is 68 wt%.

SiO_2 film with good uniformity and high properties. That is because the concentration of the solution and that of the vapor are the same (point B and B'), i.e., 68 wt%, and the concentration of the HNO_3 solution is constant during the oxidation process at boiling temperature.

On the other hand, when the HNO_3 concentration is different from 68 wt%, e.g., 40 wt% (point A'), the concentration of the vapor is about 10 wt% (point A") as is evident from Figure 2-3. Due to evaporation of low-concentration HNO_3, the concentration of the HNO_3 solution increases with the times. In this case, the properties of the SiO_2 are likely to be changed with the depth due to the change in the concentration of the HNO_3 aqueous solutions.

Here, I compare the developed NAOS method with the conventional CVD method [12-16]. The NAOS method possesses the following advantages over the conventional CVD method for deposition of SiO_2 on glass substrates (cf. Figure 2-4 and Table 2-1).

Concerning the interface between the SiO_2 and Si, a NAOS SiO_2 film is expected to possess much better properties than those for the CVD oxide film. This is because the interface of the NAOS SiO_2 layer is formed in the Si bulk while that for the CVD SiO_2 layer is formed at the surface before deposition.

Regarding the film thickness, the uniformity of a NAOS SiO_2 layer is excellent because of the direct oxidation method, while that of the CVD oxide is not good, especially on rough surfaces such as poly-Si thin films, where ridge structure arises from laser annealing of amorphous Si for crystallization [7]. The SiO_2 film thickness at the top part of the rough (a few tens nm) surfaces becomes much thinner than that on flat regions for the CVD method. Moreover, with the NAOS method, the ridge structure becomes smooth, and the electric field at sharp-edged portions is expected to decrease. The density of the NAOS film is much higher than that of the CVD oxide film [39,40], because of the direct oxidation mechanism. For these reasons, a leakage current flowing through the oxide film is much lower for the NAOS method than that for the CVD method.

Furthermore, the oxide formation temperature by the NAOS method is much

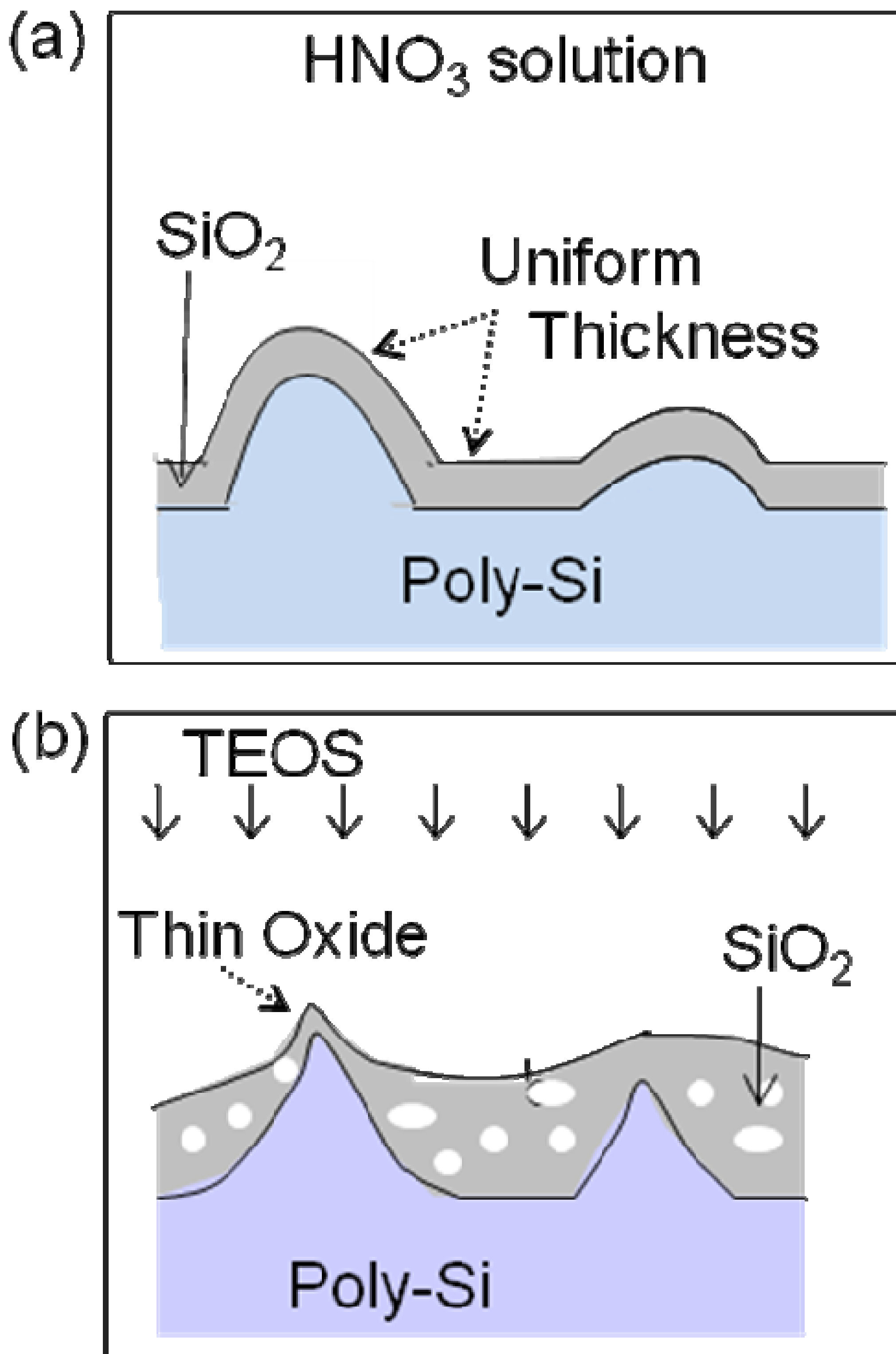

Figure 2-4. Comparison of the thin SiO_2/poly-Si thin film structures by (a) NAOS and (b) PE-CVD. TEOS (Tetraethyl orthosilicate) : $Si(OC_2H_5)_4$.

NAOS SiO_2		PE-CVD SiO_2
Uniform	Thickness Uniformity	Non-uniform
Good (high density)	Bulk Property	Poor
Good	Interface property	Poor
Low	Leakage Current	High
Low (RT~120 ℃))	Forming Temperature	High (500~600 ℃)
10~40 nm	Practical Total Thickness	80~150 nm

Table 2-1. Comparison of the thin SiO_2 structures by NAOS and PE-CVD.

lower (room temperature ~120 °C) than that of the CVD method of 500~600 °C, and therefore diffusion of the contaminants (such as Na) from glass substrates can be avoided.

II -2. Sample Preparation

Boron-doped p-type and phosphorus-doped n-type Si(100) wafers with resistivity in the range 1~20 Ωcm were cleaned using the RCA method [41] and etched with dilute hydrofluoric acid (HF). Then, the Si wafers were immersed in various concentrations (40, 68, and 98 wt%) of HNO_3 aqueous solutions at various temperatures (room temperature and the boiling temperature). The boiling temperature is 108, 121, and 83 °C for the HNO_3 concentration of 40, 68 (azeotropic HNO_3 aqueous solutions), and 98 wt%, respectively.

I also fabricated NAOS SiO_2/poly-Si/glass and PE-CVD SiO_2/poly-Si/glass specimens for comparison. Poly-Si thin films were formed by the metal-induced

crystallization method using excimer laser annealing with metal catalysts.

At first, a silicon nitride (SiN) layer was deposited on Corning 1737 glass to prevent diffusion of metal contaminants from glass substrates. Then, amorphous Si was deposited by the PE-CVD method at 400 °C. After coating nickel (Ni) solutions on the amorphous Si film, amorphous Si was crystallized by thermal annealing at 500 °C followed by excimer laser annealing [42-44]. This two-step crystallization is very effective to form poly-Si thin films with large grains and excellent electric characteristics.

Figure 2-5 shows the scanning electron microscope (SEM) photograph of the poly-Si thin film after treated with a $HF/H_2O_2/H_2O$ solution. The grain boundaries were easily recognized after chemical etching with the $HF/H_2O_2/H_2O$ solution [45]. It is found that the grain size of the poly-Si thin film was in the range of a few µm.

Figure 2-6 shows the cross-sectional transmission electron microscope (TEM) image of the fabricated poly-Si thin film. The crystal orientations of the neighboring grains are nearly the same, leading to low potential energy barrier between the

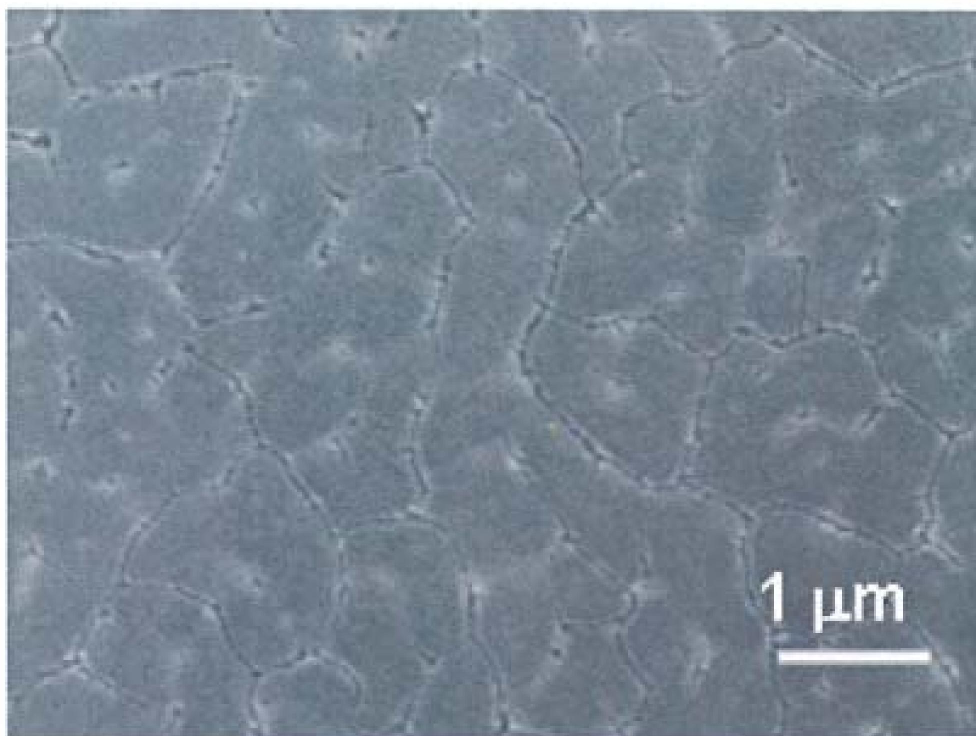

Figure 2-5. SEM micrograph of poly-Si thin film after chemical etching by $HF/H_2O_2/H_2O$.

Figure 2-6. TEM micrograph of poly-Si film. The index in the parenthesis is Miller index indicating the Si crystal direction.

grains.

The oxide formation rate of the NAOS method is not high and long time is required to realize the thickness necessary for the practical TFTs (i.e., ≥10 nm) [46]. In order to solve this problem, the NAOS SiO_2/CVD SiO_2 stacked structure was fabricated, where a 10~40 nm thick SiO_2 layer was deposited by PE-CVD method on

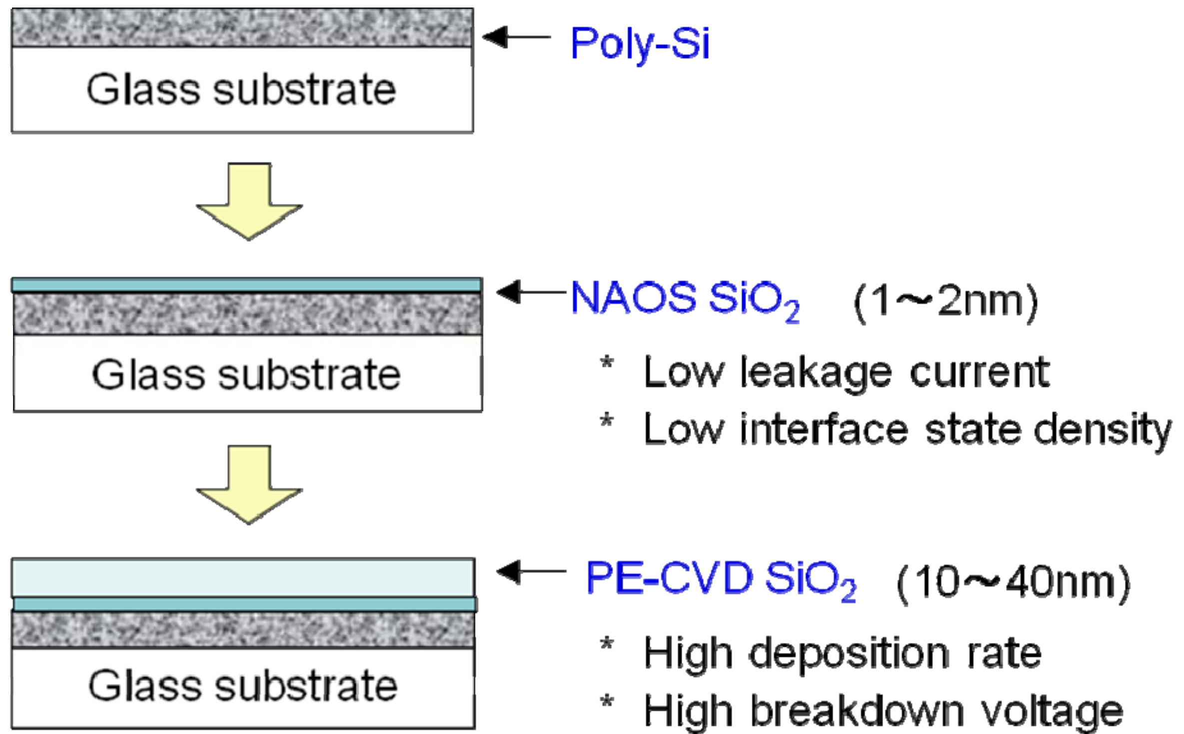

Figure 2-7. Process flow and structure of the NAOS SiO_2/PE-CVD SiO_2 stacked insulator.

the ultra-thin NAOS SiO_2 layer (cf. Figure 2-7). The ultra-thin NAOS layer possesses good interface properties such as a low interface state density and a low leakage current, and the thicker CVD oxide improves the breakdown voltage of the insulating film.

II - 3. Microphotograph of NAOS Layer

Figure 2-8 shows the TEM micrograph of the SiO_2 layer formed on p-type Si(100) substrate by the NAOS method with 68 wt% azeotropic HNO_3 aqueous solutions at 120 °C for 10 min. It is clearly seen that the uniform thickness (i.e., 1.39 nm) NAOS SiO_2 layer was formed on an Si substrate.

Figure 2-9 shows the TEM micrograph of the cross-section of NAOS SiO_2/PE-CVD SiO_2 stacked insulator formed on a poly-Si thin film. The 1.4 nm thick NAOS layer was formed with 68 wt% HNO_3 solutions at 120 °C for 10 min, and the thickness of the PE-CVD SiO_2 layer was 10 nm. The NAOS SiO_2 layer was observed with the relatively darker color. The darkness indicates a higher atomic density

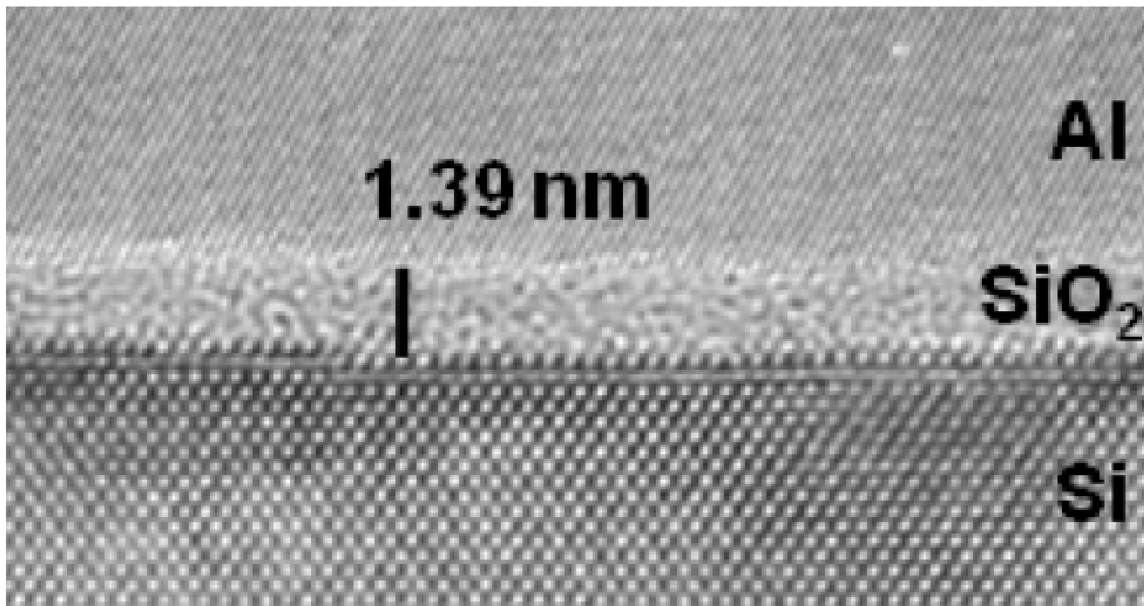

Figure 2-8. TEM micrograph of the cross-section of the Al/NAOS SiO_2/Si(100) structure. An ultra-thin SiO_2 layer of 1.39 nm was formed on Si with high uniformity.

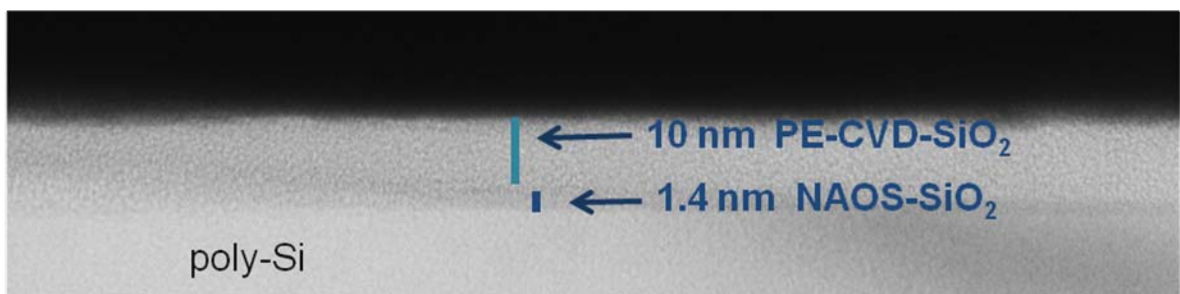

Figure 2-9. Cross-sectional TEM micrograph of the NAOS SiO_2/PE-CVD SiO_2 stacked oxide on a poly-Si thin film. The darker layer is due to NAOS SiO_2. The thicknesses of NAOS SiO_2 and PE-CVD SiO_2 are estimated to be 1.4 and 10 nm, respectively.

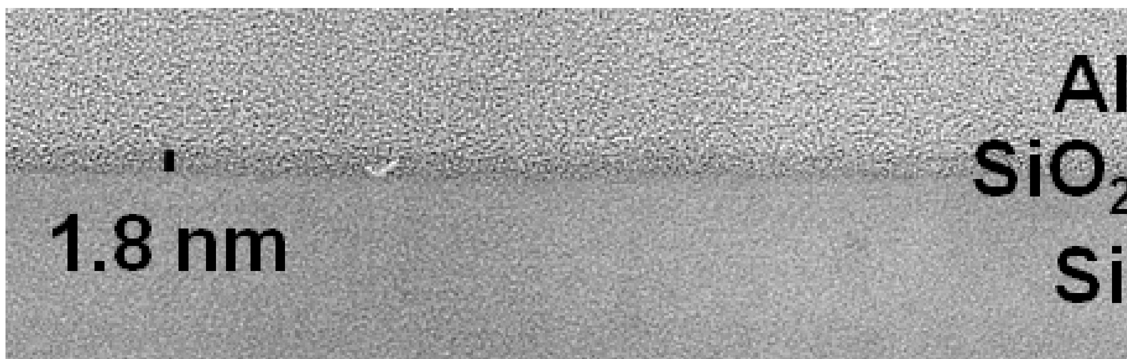

Figure 2-10. TEM image of the cross-section of the SiO_2 layer formed on Si(100) by the NAOS method at room temperature.

than that of the CVD SiO_2 layer, as explained in the following sections.

Figure 2-10 shows the TEM image of the cross-section of the SiO_2 layer formed on the Si(100) substrate by the NAOS method with 68 wt% azeotropic HNO_3 aqueous solutions at room temperature. It is evident that an uniform and 1.8 nm thick SiO_2 layer could be formed on Si(100) even at room temperature.

II - 4. XPS Core Level Spectra and Oxide Thickness

Figure 2-11 shows the principle of X-ray photoelectron spectroscopy (XPS). When X-ray is irradiated on the specimen, electrons in core orbitals absorb the X-ray energy and are ejected outside as photoelectrons. The photoelectron has a kinetic energy (E_k) equal to the difference between the energy of incident X-ray ($h\nu$) and the binding energy of an electron (E_b) in the core shell. Therefore, by measuring the kinetic energy of photoelectrons, the binding energy can be determined, and the element and its oxidation state can be identified. In addition, the concentration of the material can be also evaluated from the photoelectron intensity. It is noted that the detection depth is limited to a few nm from the surface, because of a short photoelectron mean free path in the range of a few nm.

XPS spectra were measured using an ESCALAB 220i-XL spectrometer with a

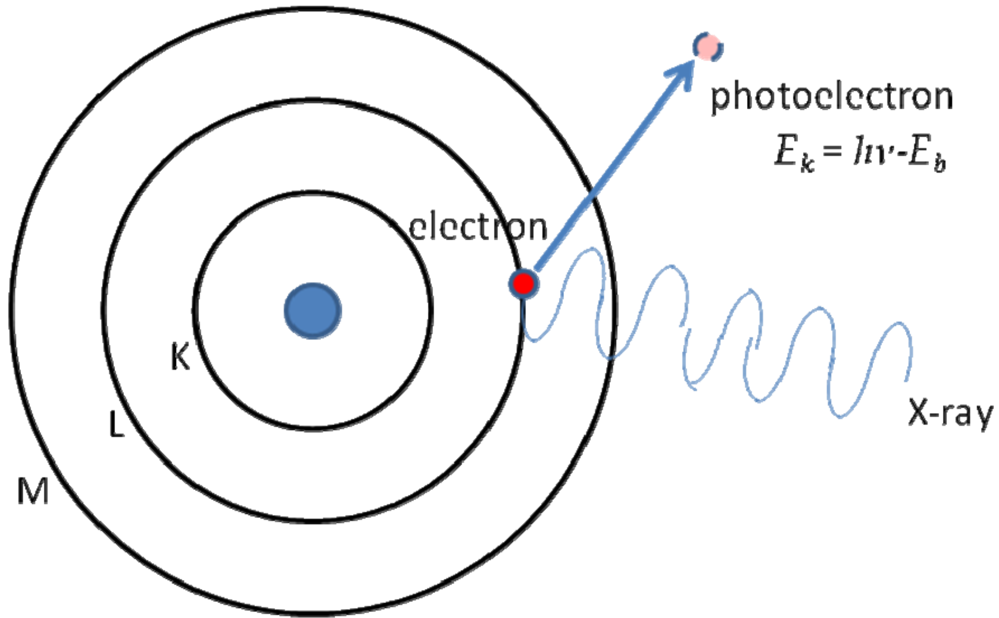

Figure 2-11. The principle of X-ray photoelectron spectroscopy. E_k : kinetic energy of photoelectron, $h\nu$: incident X-ray energy, E_b : binding energy of a core level.

monochromatic Al Kα radiation source. Photoelectrons were collected in the surface normal direction.

Figure 2-12 shows an XPS spectrum in the Si 2p region for the SiO_2/Si structure formed by immersion of Si(100) wafers in 68wt% HNO_3 aqueous solutions at room temperature. The doublet peaks were attributable to Si $2p_{3/2}$ and $2p_{1/2}$ levels of the Si substrate and the broad peak in the higher energy region was due to the SiO_2 layer [47,48].

The thickness of the SiO_2 layer (d_{ox}) can be calculated from the ratio in the area intensity between these two peaks as using following equation [47],

$$d_{ox} = \lambda_{ox}[\ln \frac{D_{ox}\sigma_{ox}\lambda_{ox}}{D_{Si}\sigma_{Si}\lambda_{Si}} \frac{I_{Si}}{I_{ox}} + 1] \tag{2-5}$$

where λ_{OX} and λ_{Si} are the electron mean free paths in the SiO_2 layer and the Si

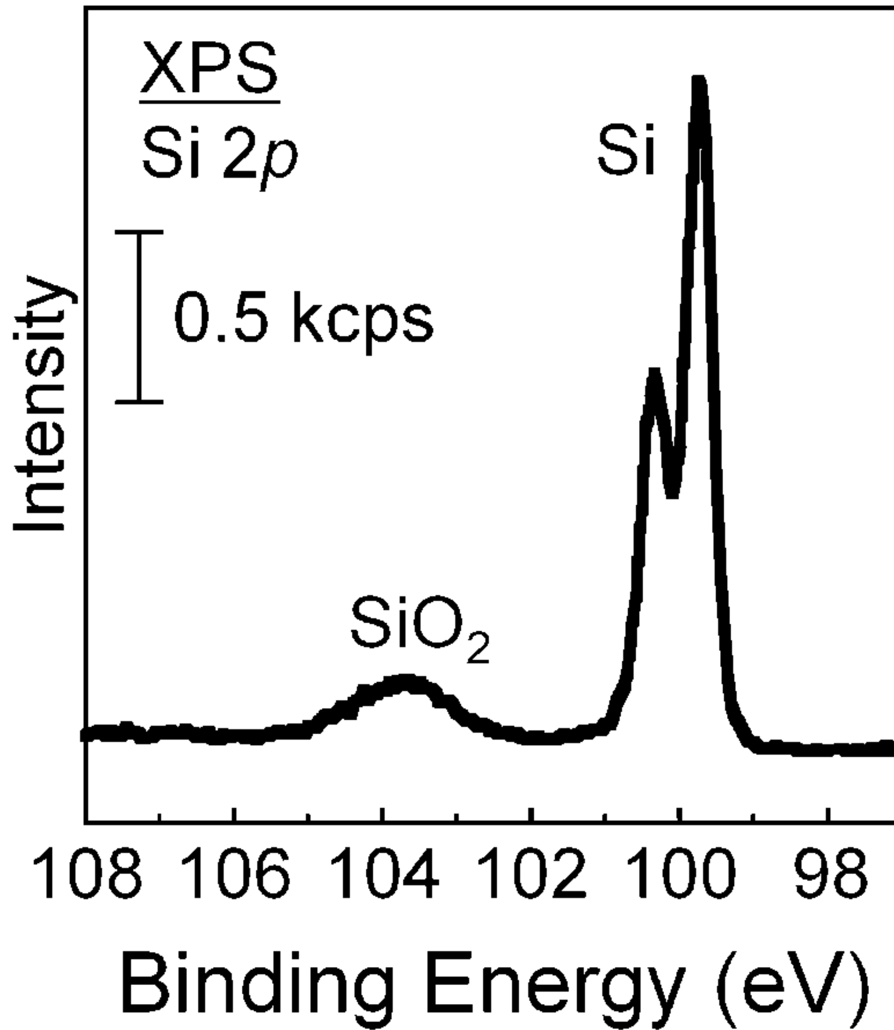

Figure 2-12. XPS spectrum for the SiO_2/Si(100) structure formed with 68 wt% HNO_3 aqueous solutions at room temperature.

substrate, respectively, D_{ox} and D_{Si} are the atomic densities of SiO_2 and Si, respectively, σ_{ox} and σ_{Si} are the ionization cross-sections of SiO_2 and Si, respectively, and I_{ox} and I_{Si} are the XPS area intensities of the SiO_2 and Si peaks , respectively [30,31].

The thickness of the SiO_2 layer formed by the NAOS method was estimated to be 1.8 nm from Equation (2-5), adopting the values of 2.7 and 3.3 nm for the electron mean free paths in SiO_2 and Si, respectively [12]. The SiO_2 thickness of 1.8 nm was also confirmed by TEM measurements as shown in Figure 2-10.

There are no peaks besides Si and SiO_2 peaks in the spectra, indicating that the

densities of sub-oxide species, Si^{+}, Si^{2+}, and Si^{3+}, were negligibly low.

Figure 2-13 shows the HNO_3 concentration dependency of XPS spectra in the Si 2p region. The HNO_3 concentration was set at 40, 68, and 98 wt% for spectra b, c, and d, respectively. The oxide layer was formed at room temperature for 2 min. There is no difference in the intensity ratio for the three spectra, indicating that the SiO_2 thickness did not depend on the HNO_3 concentrations.

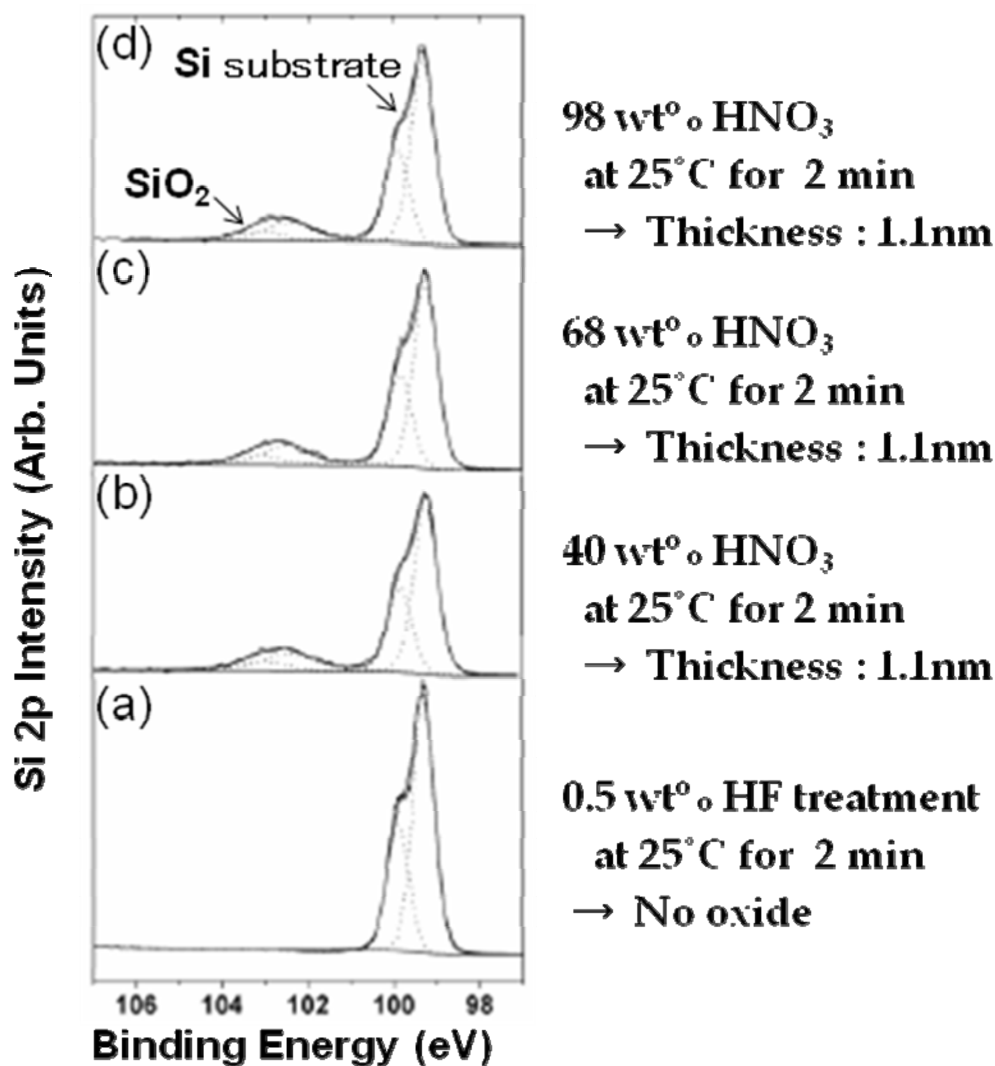

Figure 2-13. XPS spectra for the SiO_2/Si structures formed with various concentration HNO_3 aqueous solutions at room temperature.

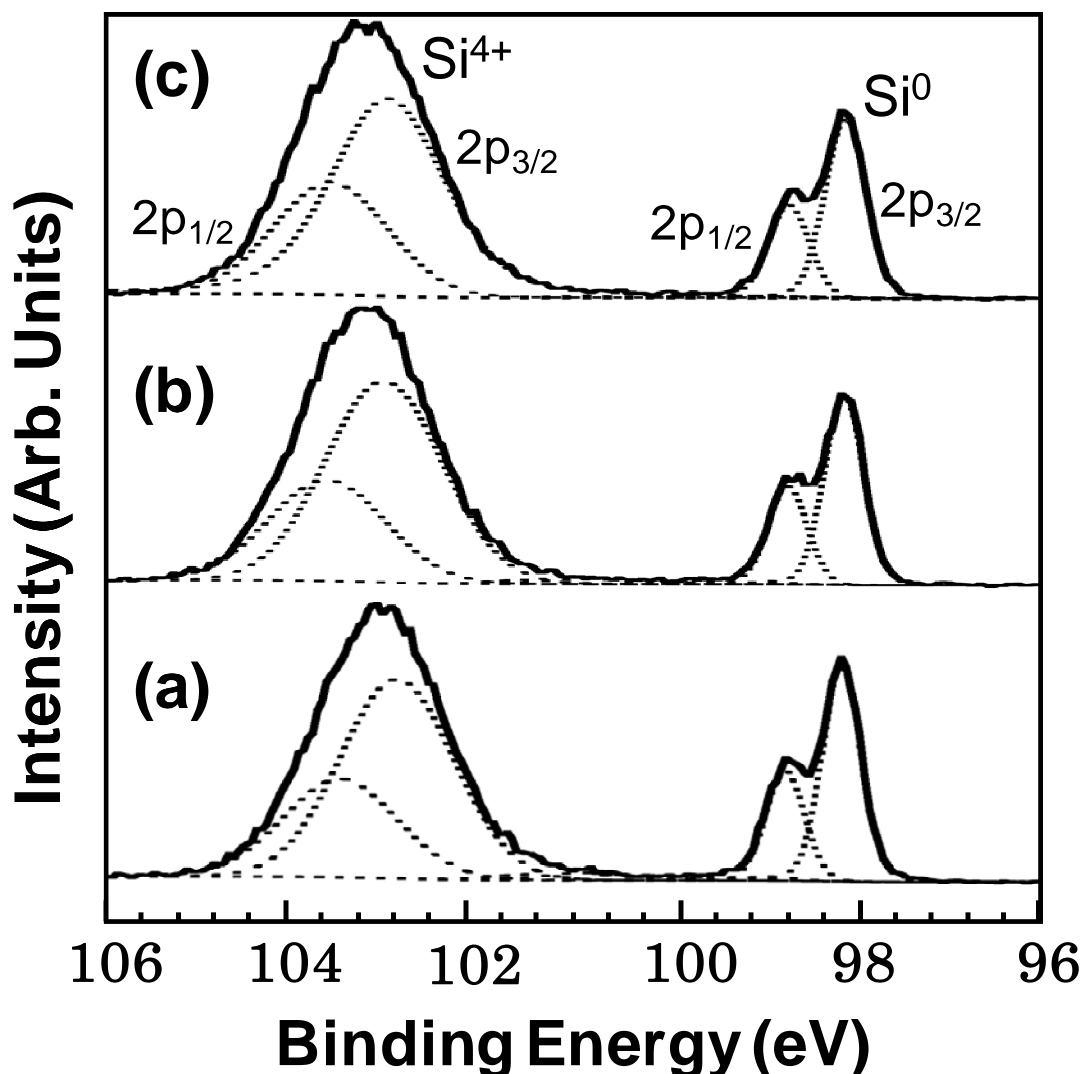

Figure 2-14. XPS spectra in the Si 2p region for the SiO_2/Si(100) structures formed by the NAOS method with 68 wt% HNO_3 solutions at 120 °C for 3.5 h: (a) as-formed; (b) after POA in dry-oxygen at 400 °C; (c) after POA in wet-oxygen at 400 °C. Deconvolution is shown by the dotted lines.

I have investigated the effect of post-oxidation annealing (POA) on the properties of the ultra-thin NAOS SiO_2 films. Figure 2-14 shows the XPS spectra for the SiO_2/Si structures formed by the NAOS method at 120 °C for 3.5 h. From the intensity ratio between the SiO_2 Si 2p peak and the substrate Si $2p_{3/2}$ and $2p_{1/2}$ peaks, the SiO_2 thickness was estimated to be 5.7 nm for specimen a (i.e., as-formed SiO_2

with the NAOS oxidation time of 3.5 h) and 6.0 nm for specimen b (after POA in dry-oxygen at 400 °C) and specimen c (after POA in wet-oxygen at 400 °C).

Deconvolution of the XPS spectra is shown by the dotted lines in Figure 2-14, and it is easily seen that the densities of sub-oxide species, Si^{+}, Si^{2+} and Si^{3+}, are negligibly low.

II - 5. FT-IR Spectra and Atomic Density

I measured Fourier transform infrared absorption (FT-IR) spectra in order to estimate the atomic density of the SiO_2 layer formed by the NAOS method.

FT-IR spectroscopy is a useful tool for analysis of molecular vibration by measuring infrared absorption of materials. The vibration energy is determined by the atomic mass and the force constant of chemical bonds. Only vibrational modes changing dipole moment are infrared active. As the asymmetric Si-O-Si stretching vibration mode has a dipole moment change, FT-IR spectra of this mode are observable.

FT-IR spectra were recorded at the incident angle of 65° using a Nicolet Nexus 370S spectrometer.

Figure 2-15 shows the FT-IR spectra for the SiO_2/poly-Si structures with the SiO_2 layer formed by the NAOS method at 25 °C with the HNO_3 concentrations of 40, 68, and 98 wt%. Peaks present at ~1050 and ~1200 cm^{-1} are attributable to transverse optical (TO) and longitudinal optical (LO) phonons of asymmetric Si-O-Si stretching vibrational modes, respectively [49-51]. Figures 2-16 and 2-17 show the schematic diagrams of LO and TO vibrational modes, respectively.

Figure 2-18 shows the vibrational frequency of LO and TO phonons vs. the HNO_3 concentration. The vibrational frequency of the LO and TO modes are changed, and the frequency separation increases with the HNO_3 concentrations.

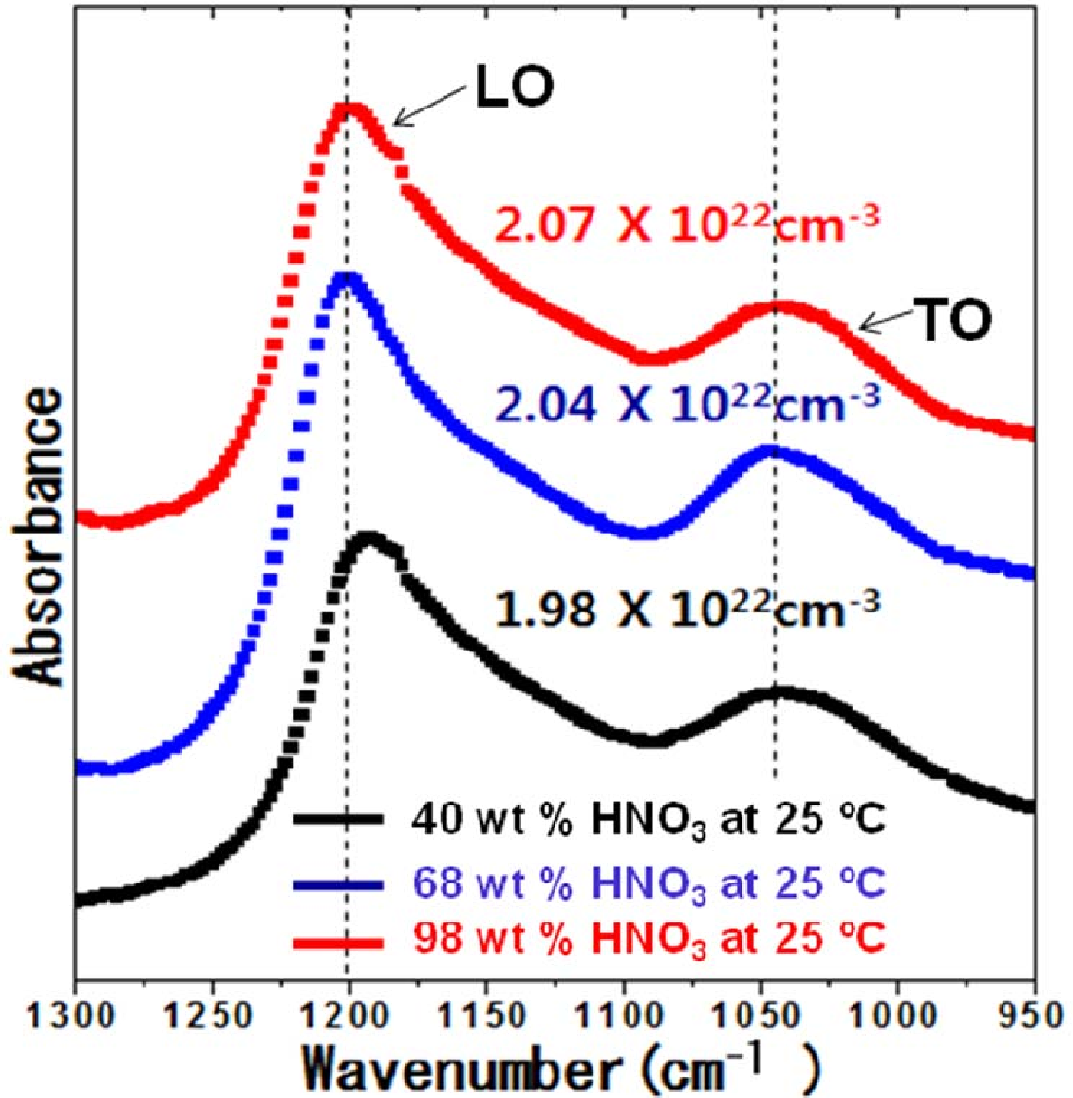

Figure 2-15. FT-IR spectra for SiO_2/poly-Si structures formed by the NAOS method with various HNO_3 concentrations at room temperature.

The atomic density of SiO_2 (ρ) can be estimated using the following equation in which central and non-central force model is assumed [52],

$$C \cdot \rho = \nu_{LO}^2 - \nu_{TO}^2 \qquad (C = 1.71\times10^{-17}\ \text{cm}) \qquad (2\text{-}6)$$

where ν_{LO} and ν_{TO} are the oscillating frequencies of LO and TO phonons of asymmetric Si-O-Si stretching vibrational modes, respectively, and C is a constant

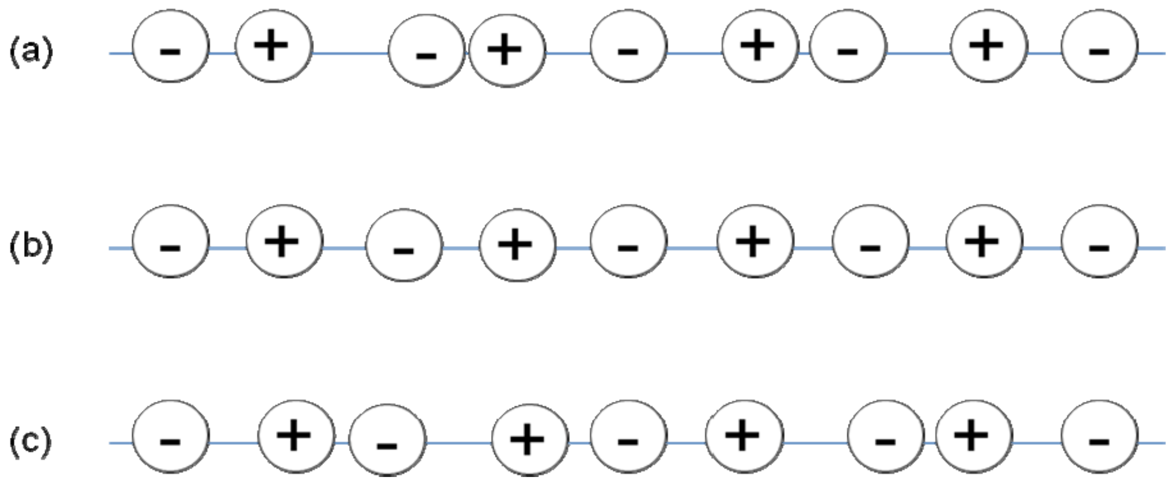

Figure 2-16. Schematic diagram of the longitudinal optical (LO) vibrational mode.

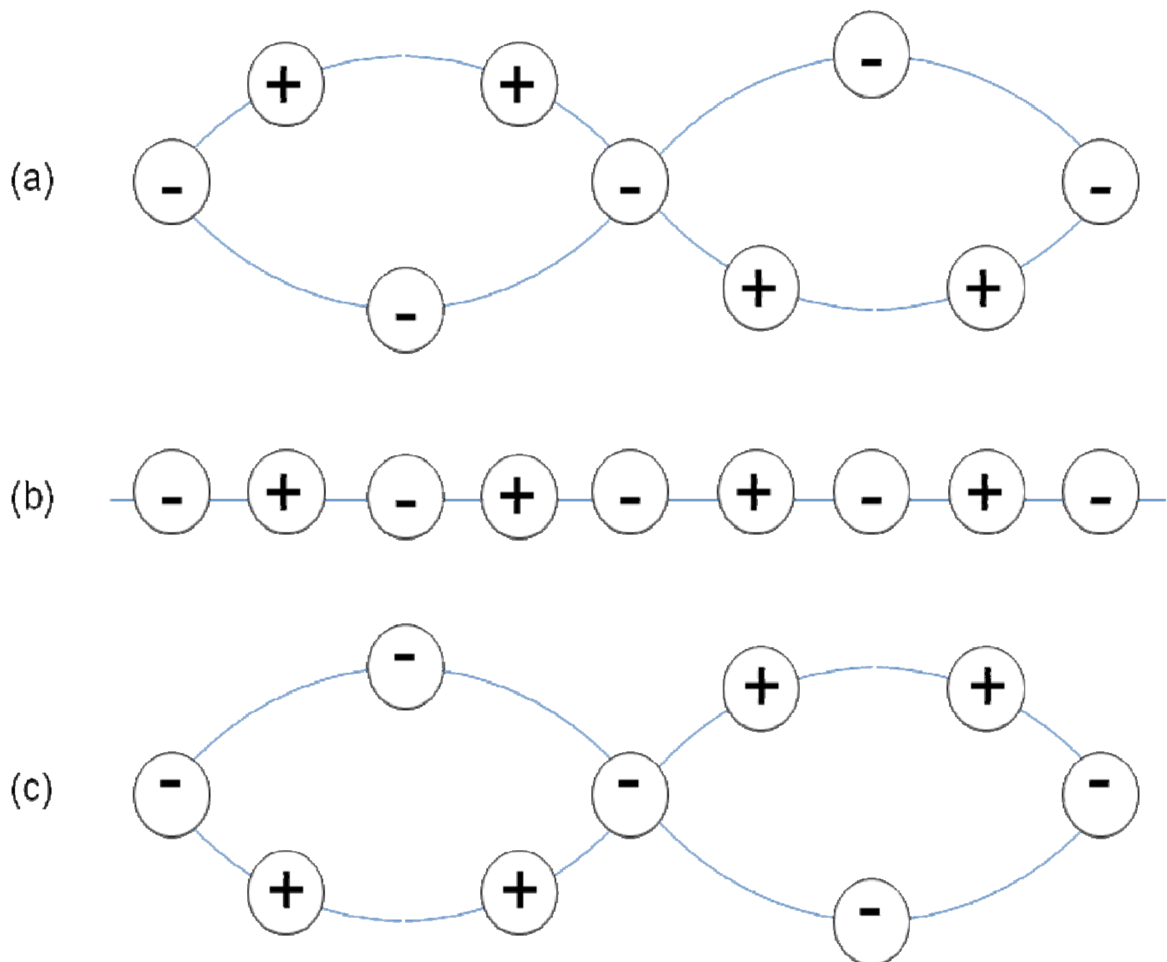

Figure 2-17. Schematic diagram of the transverse optical (TO) vibrational mode.

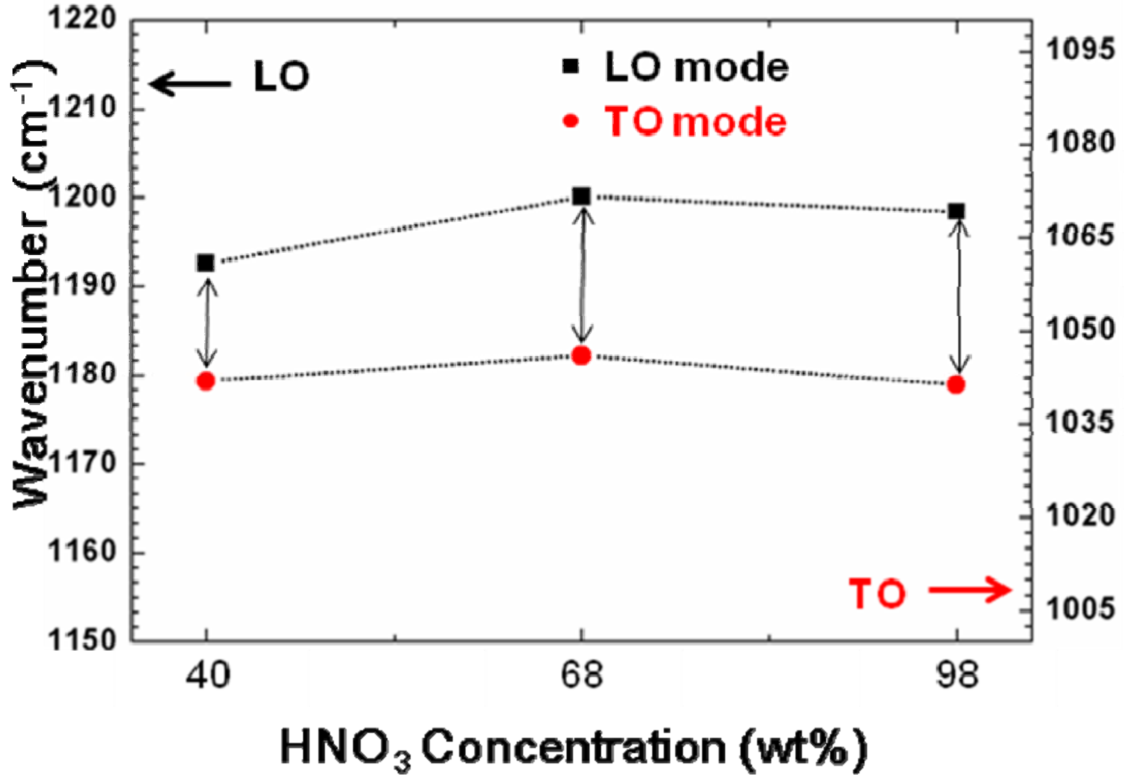

Figure 2-18. Vibrational frequency of LO and TO modes vs. the HNO_3 concentration. The NAOS SiO_2 layer was formed on poly-Si film at room temperature for 2 min.

explained below.

The vibrational frequencies of LO and TO phonons of asymmetric Si-O-Si stretching vibrational modes are expressed as

$$\nu_{LO} = \frac{1}{2\pi}\left[\frac{2}{m_o}\left\{\alpha \sin^2\frac{\theta}{2} + \beta \cos^2\frac{\theta}{2} + C'\cdot\rho\right\}\right]^{1/2} \tag{2-7}$$

$$\nu_{TO} = \frac{1}{2\pi}\left[\frac{2}{m_o}\left\{\alpha \sin^2\frac{\theta}{2} + \beta \cos^2\frac{\theta}{2}\right\}\right]^{1/2} \tag{2-8}$$

$$C' = \frac{\left(Z_{OS}^T\right)^2}{\varepsilon_{OX}\,\varepsilon_0\left(2m_0 + M\right)} \tag{2-9}$$

where θ is the bond angle of Si-O-Si, ρ is the atomic density of SiO_2, m_0 is the mass

of an oxygen atom, M is the mass of an Si atom, α and β are the constant values on mechanics, Z^T_{OS} is the electric charge related to oxygen atom oscillation, ε_0 is the permittivity in vacuum, and ε_{OX} is the relative dielectric constant of SiO_2.

The vibrational frequency of the LO mode is a function of both the Si-O-Si bond angle (θ) and the atomic density (ρ), while that of the TO mode is a function of only the bond angle (θ). Therefore, the atomic density can be calculated from the vibrational frequencies of the TO and LO modes using the above equations. C is determined to be 1.71×10^{-17} cm using the values for a thick thermally grown SiO_2 layer (i.e., ν_{TO}=1090 cm^{-1}, ν_{LO}=1256 cm^{-1}, and $\rho=2.28\times10^{22}$ /cm^3 [1]).

The atomic density of the NAOS SiO_2 layer was calculated to be 1.98×10^{22}, 2.04×10^{22}, and 2.07×10^{22} atoms/cm^3 for 40, 68, and 98 wt% of HNO_3 aqueous solutions, respectively. The estimated atomic densities are displayed in Figure 2-15, which indicates that the atomic density increases with the HNO_3 concentration.

Figure 2-19 shows the FT-IR spectra for the SiO_2/poly-Si structure with the SiO_2 layer formed by the NAOS method at the boiling point with the HNO_3 concentrations of 40, 68, and 98 wt%. The calculated atomic densities are 2.16×10^{22}, 2.20×10^{22}, and 2.25×10^{22} atoms/cm^3 for oxidation with 40, 68, and 98 wt% of HNO_3 aqueous solutions, respectively. These densities are higher than those for the NAOS method at 25 °C and very close to that of a thick thermally grown SiO_2 layer of 2.28×10^{22} atoms/cm^3 [1].

The absence of sub-oxides is supposed to be one of the reasons for the high atomic density of the NAOS SiO_2 layer.

I have investigated the effect of POA on the FT-IR spectra. Figure 2-20 shows the FT-IR spectra for the SiO_2/Si(100) structures with the SiO_2 layer formed by the NAOS method at 120 °C. POA at 400 °C in dry-oxygen (spectrum b) did not change the vibrational frequency of LO phonons at 1242 ±2 cm^{-1} while that in wet-oxygen increased it to 1244 ±2 cm^{-1} (spectrum c). Both the POA treatments decreased the vibrational frequency of TO phonons from 1074 ±2 cm^{-1} to 1072 ±2 cm^{-1}.

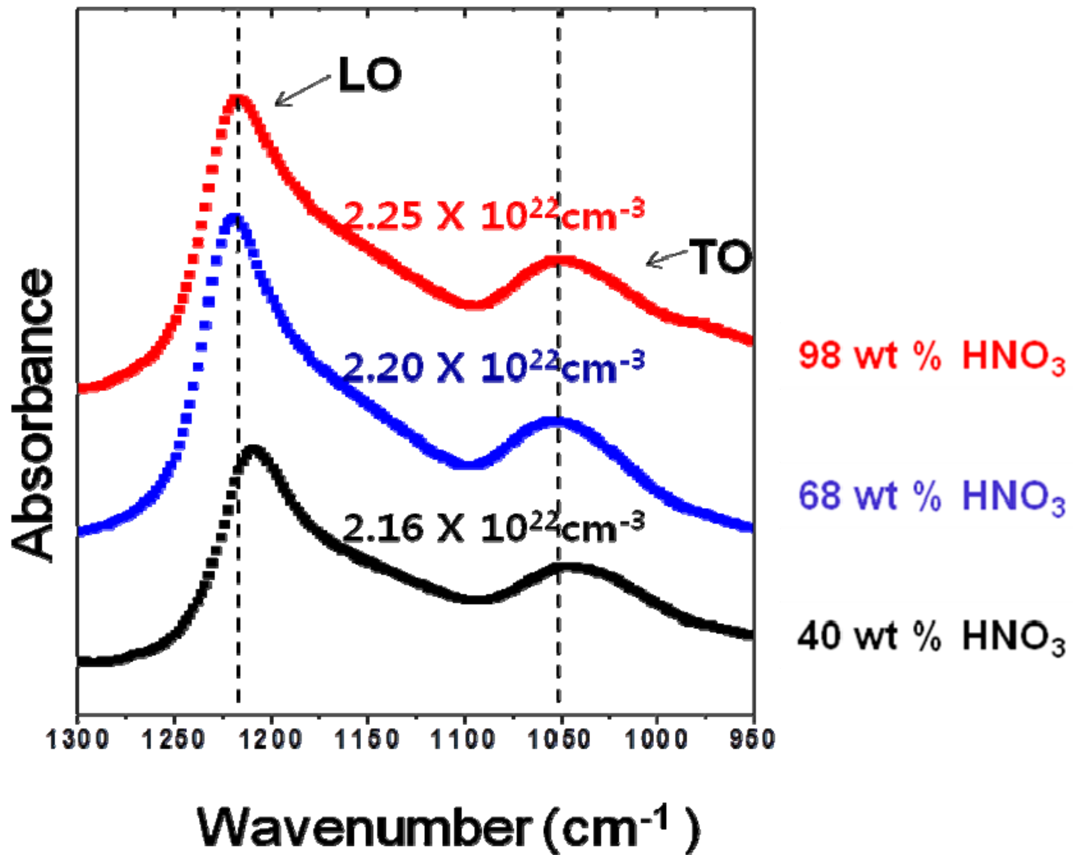

Figure 2-19. FT-IR spectra for SiO_2/poly-Si structures formed by the NAOS method with various HNO_3 concentrations at the boiling point.

Consequently, the frequency separation between TO and LO phonons became larger by 2 cm^{-1} and 4 cm^{-1}, by POA in dry-oxygen and wet-oxygen, respectively.

Figure 2-21 shows the calculated atomic density of the SiO_2 layer formed by the NAOS method with and without POA. The as-formed SiO_2 layer possesses an atomic density of $2.28\times10^{22} \pm 0.05\times10^{22}$ atoms/cm^3 which is the same as that of a thick thermally grown SiO_2 layer. After POA in dry-oxygen at 400 °C, the POA in wet-oxygen at the same temperature increased the atomic density to a large extent to $2.32\times10^{22} \pm 0.05\times10^{22}$ atoms/cm^3.

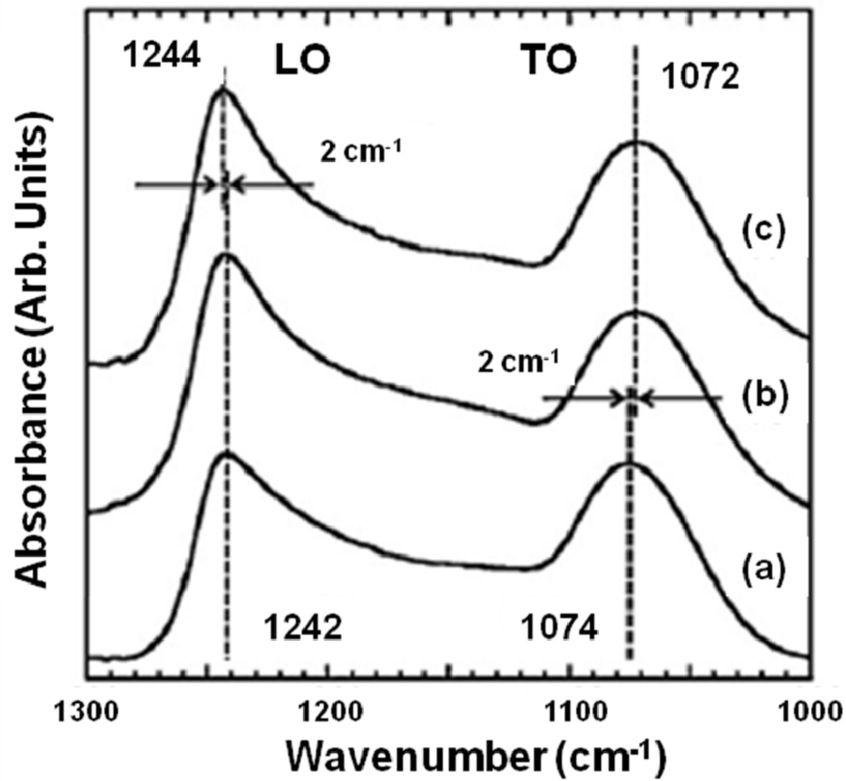

Figure 2-20. FT-IR spectra for SiO_2/Si(100) structures formed by the NAOS method with 68 wt% HNO_3 at 120 °C: (a) as-formed; (b) after POA in dry-oxygen at 400 °C; (c) after POA in wet-oxygen at 400 °C.

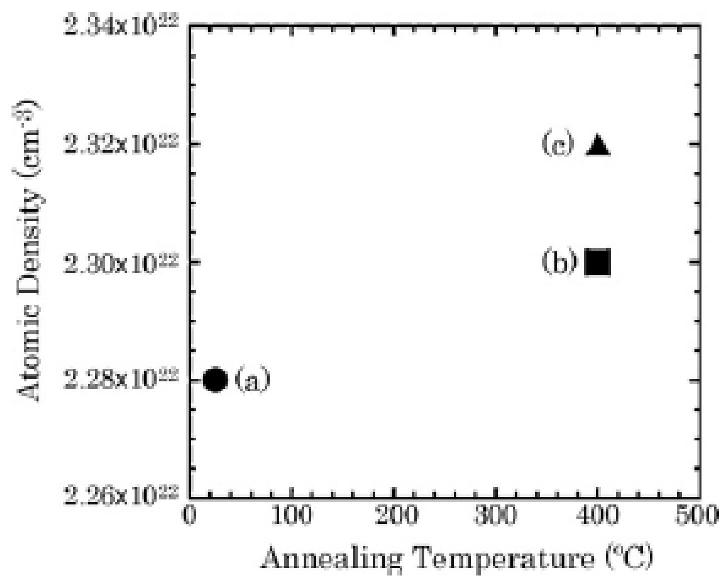

Figure 2-21. Atomic density of the SiO_2 layers formed by the NAOS method with and without POA: (a) without POA; (b) with POA in dry-oxygen at 400 °C; (c) with POA in wet-oxygen at 400 °C.

II - 6. XPS Valence-Band Spectra and Band Discontinuity Energy

I measured the valence-band XPS spectra for the NAOS SiO_2 layers formed on the Si substrate and estimated the band discontinuity energy at the NAOS SiO_2/Si interface. The spectra give the energy difference between the SiO_2 and Si valence bands, ΔE_V (cf. Figure 2-22).

The XPS spectra were measured using an ESCALAB 220i-XL spectrometer with a monochromatic Al Kα radiation source, and the photoelectrons were collected in the surface-normal direction.

Figure 2-23 shows the valence-band XPS spectra for the Si substrate and the NAOS SiO_2 layers formed with the various concentrations of HNO_3 solutions. The spectra for NAOS SiO_2 were obtained after subtraction of the spectrum of Si substrate from the measured spectra for the SiO_2/Si(100) structure.

In the case of the SiO_2 layer formed with 40 wt% HNO_3, the valence band maximum (VBM) of SiO_2 was located at 4.16 eV below the Si VBM. For the SiO_2 layers formed with 68 and 98 wt% HNO_3, on the other hand, the valence-band discontinuity energy ΔE_V between SiO_2 and Si increased to 4.26 and 4.31 eV,

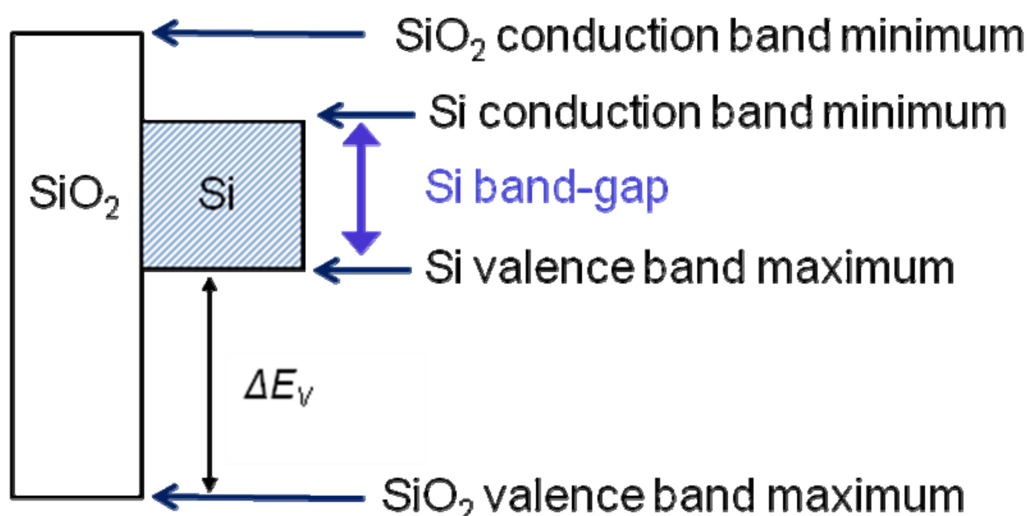

Figure 2-22. Band diagram of SiO_2/Si structure.

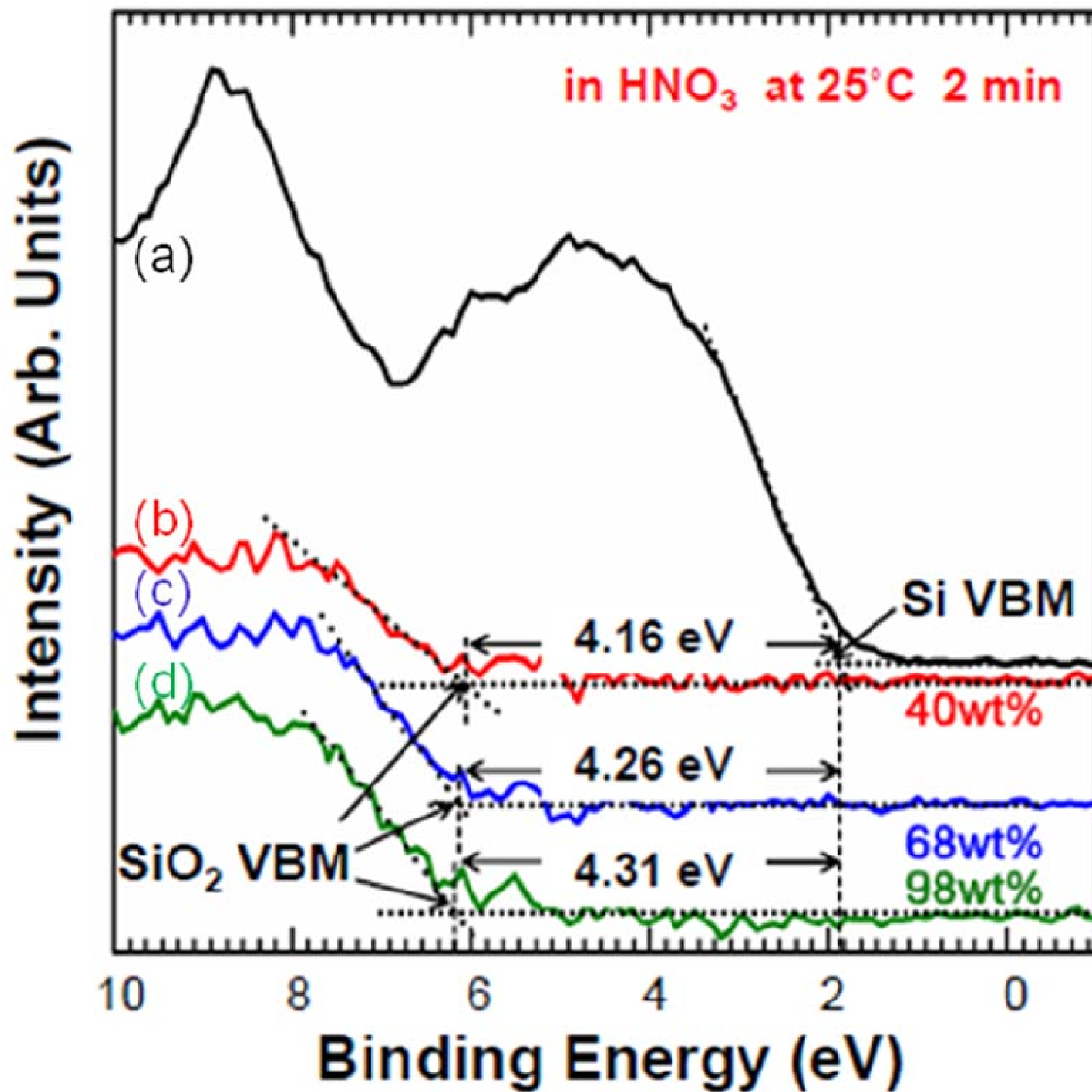

Figure 2-23. Valence-band XPS spectra for Si(100) and NAOS SiO_2 layers formed with HNO_3 aqueous solutions having following concentrations at room temperature: (a) Si substrate; (b) NAOS SiO_2 with 40 wt% HNO_3; (c) with 68 wt% HNO_3; (d) with 98 wt% HNO_3.

respectively. Namely, it was found that the valence-band discontinuity energy increased with the concentration of HNO_3 solutions. The possible reason for the increase in the band discontinuity energy with the HNO_3 concentration is given as below.

The atomic density of NAOS SiO_2 increases with the HNO_3 concentration as is

evident from the FT-IR spectra as described in Section II - 5. The SiO_2 layer with the higher densities is likely to have shorter Si-O bonds, which in turn results in stronger interaction between the atoms in the SiO_2 layer. The enhanced interaction is thought to enlarge the SiO_2 band-gap by a increase in the energy difference between the bonding states (i.e., SiO_2 valence band) and the anti-bonding states (i.e. SiO_2 conduction band). The large band-gap leads to a high valence-band discontinuity energy ΔE_V at the SiO_2/Si interface.

Figure 2-24 shows the valence-band XPS spectra of the NAOS SiO_2 layers

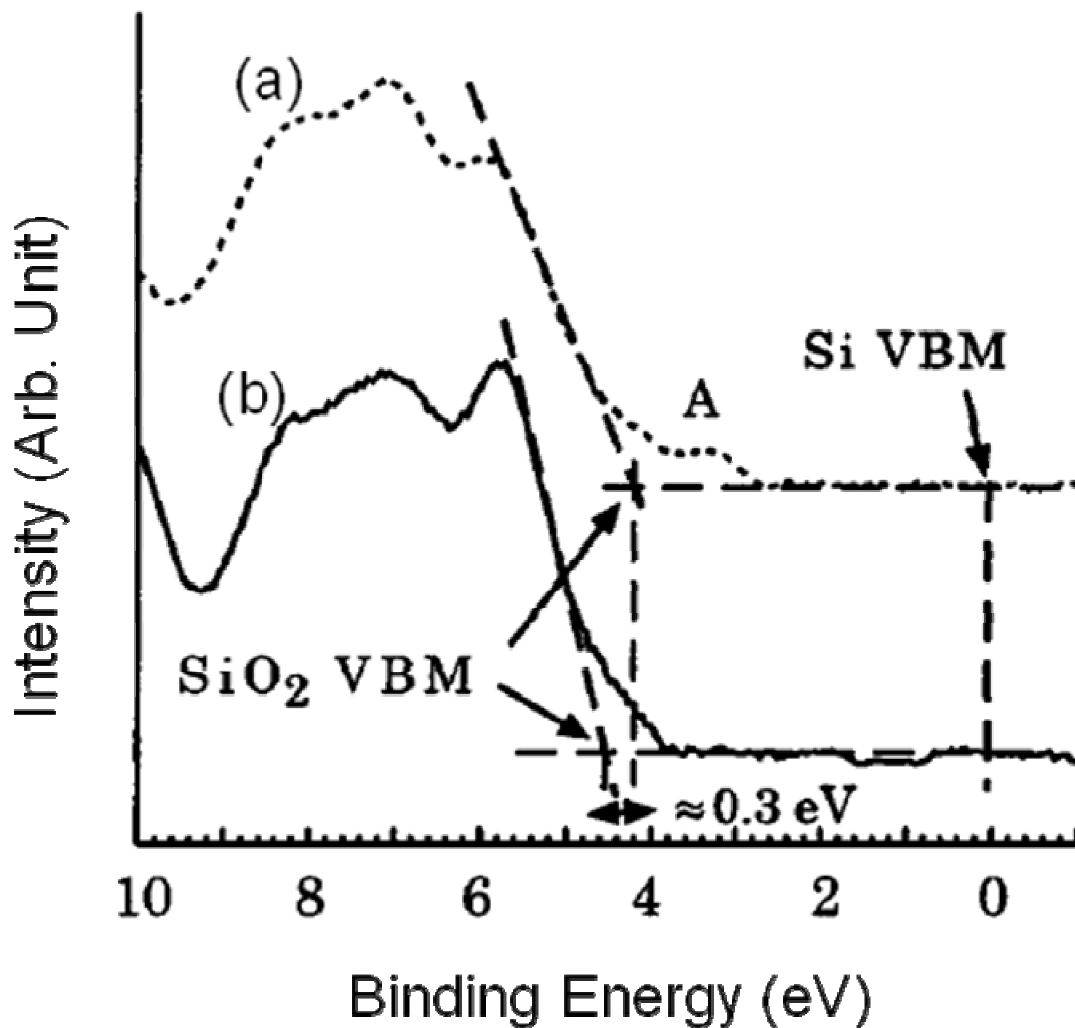

Figure 2-24. Valence-band XPS spectra for the NAOS SiO_2 layers formed with 68 wt% HNO_3 aqueous solutions at 120 °C: (a) as-formed; (b) PMA in hydrogen at 200 °C.

formed with 68 wt% HNO_3 at 120 °C (spectrum a) and that with post-metallization annealing (PMA) (spectrum b). The PMA treatment was performed in hydrogen at 200 °C after the formation of the Al electrode. Similar to Figure 2-23, the component from the Si substrate was removed. Without PMA, there was a peak A in the spectrum (a), which indicates the existence of high-density energy states in the SiO_2 band-gap. Furthermore, the valence-band discontinuity energy at the SiO_2/Si interface increased by ~0.3 eV with PMA.

The presence of the high-density energy states in the band-gap causes the hopping conduction mechanism [53,54], which may increase the leakage current. The quantum-mechanical tunneling probability of charge carriers through an SiO_2 layer is a strong function of the band discontinuity energy [55], and the density of a current flowing with the Fowler-Nordheim mechanism also depends exponentially on the band discontinuity energy [56]. Therefore, the leakage current through the SiO_2 layer will exponentially decrease with the band discontinuity energy. In fact, the leakage current densities decreased by PMA as discussed in the next section.

II - 7. Summary

I have fabricated SiO_2/Si(100) substrate and SiO_2/poly-Si thin film structures by the NAOS method at low temperature below 120 °C, and analyzed the properties of ultra-thin SiO_2 layers in details by measuring the XPS and the FT-IR spectra. The summaries of this section are as follows:

1) An ultra-thin SiO_2 layer can be formed by the NAOS method with various HNO_3 concentrations and temperatures on Si(100) substrates and poly-Si thin films.
2) The NAOS SiO_2 thickness is estimated to be 1.1~1.8 nm by measurements of the Si 2p XPS spectra.
3) The SiO_2 thickness does not depend on the HNO_3 concentration in the range between 40 and 98 wt%.
4) The densities of sub-oxide species, Si^{+}, Si^{2+}, and Si^{3+}, in the NAOS SiO_2 layer are

negligibly low.

5) The FT-IR measurements indicate that the atomic density of the NAOS SiO_2 layer formed with 68 wt% HNO_3 at 120 ºC is 2.32×10^{22} atoms/cm^3, which is higher than that of thermally grown SiO_2 of 2.28×10^{22} atoms/cm^3.
6) The atomic density of the NAOS SiO_2 increases with the HNO_3 concentration and the temperature.
7) The valence-band discontinuity energy at the NAOS SiO_2/Si interface increases with the HNO_3 concentration.
8) A low leakage current through the NAOS SiO_2 layer is expected by a decrease in the tunneling probability of carriers caused by SiO_2 band-gap widening.

III. Characteristics of MOS Diodes with NAOS SiO_2 Layer

III - 1. Sample Preparation

In order to evaluate the electrical characteristics of the NAOS SiO_2 layer, I fabricated metal-oxide-semiconductor (MOS) diodes on p-type (boron-doped) and n-type (phosphorus-doped) Si(100) substrates. The structure of the Si-based MOS diode is shown in Figure 3-1. After the formation of NAOS SiO_2 layer on Si substrate, aluminum (Al) dots of 0.3 mm diameter were formed by the vacuum evaporation method. For some specimens, the SiO_2/Si structure was heated at 400 ºC in wet-oxygen (H_2O) or dry-oxygen (O_2) for 70 min before evaporating Al electrodes. In this case, PMA was carried out at 200 ºC in 5 vol% hydrogen atmosphere for 20 min after forming Al electrodes.

I also fabricated MOS diodes with poly-Si thin films on glass substrates in order to measure a leakage current flowing though ultra-thin SiO_2 on the rough poly-Si thin film. Figure 3-2 shows the cross-sectional TEM microphotograph of the poly-Si-based MOS diode. The thickness of the poly-Si layer was ~50 nm and the grain size was in the range between 200 and 800 nm. The thickness of the NAOS SiO_2 layer was 1.8 nm.

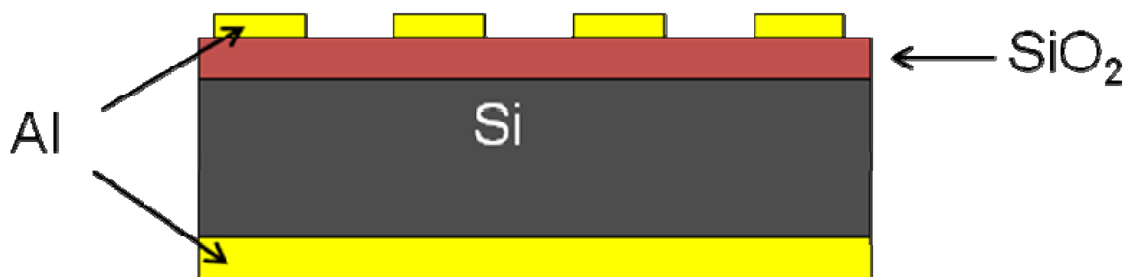

Figure 3-1. Structure of Si-based MOS diode. The diameter of Al dots is 0.3 mm.

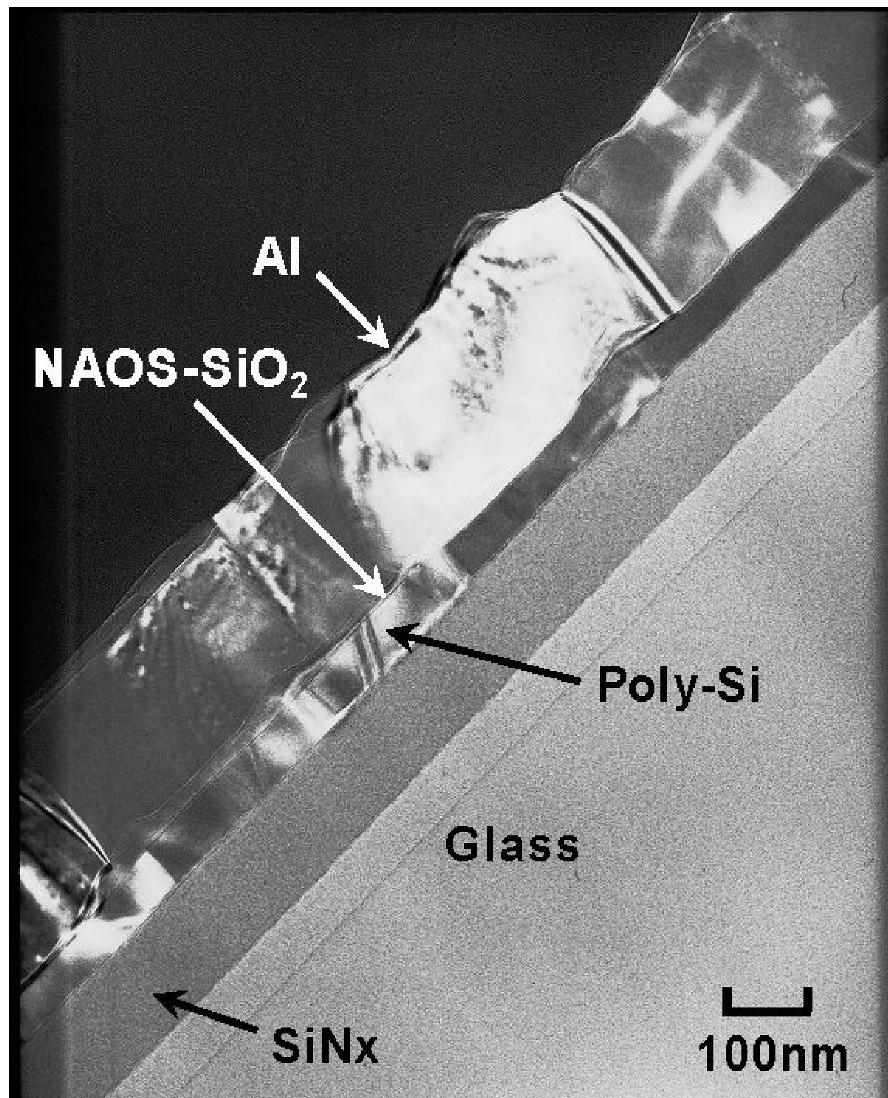

Figure 3-2. Cross-sectional TEM image of the <Al/NAOS SiO_2/poly-Si> MOS structure on the glass substrate.

III - 2. I-V Characteristics

Figure 3-3 shows the current-voltage (I-V) curves for the Al/1.3 nm NAOS SiO_2 /n-type Si(100) MOS structure formed by 68 wt% HNO_3 at 120 °C for 10 min. The leakage current density through the 1.3 nm-thick NAOS SiO_2 film was less than 1 A/cm^2 at the applied voltage of 1.0 V, and this value was approximately one order of magnitude lower than that of the thermally grown SiO_2 film with the equivalent

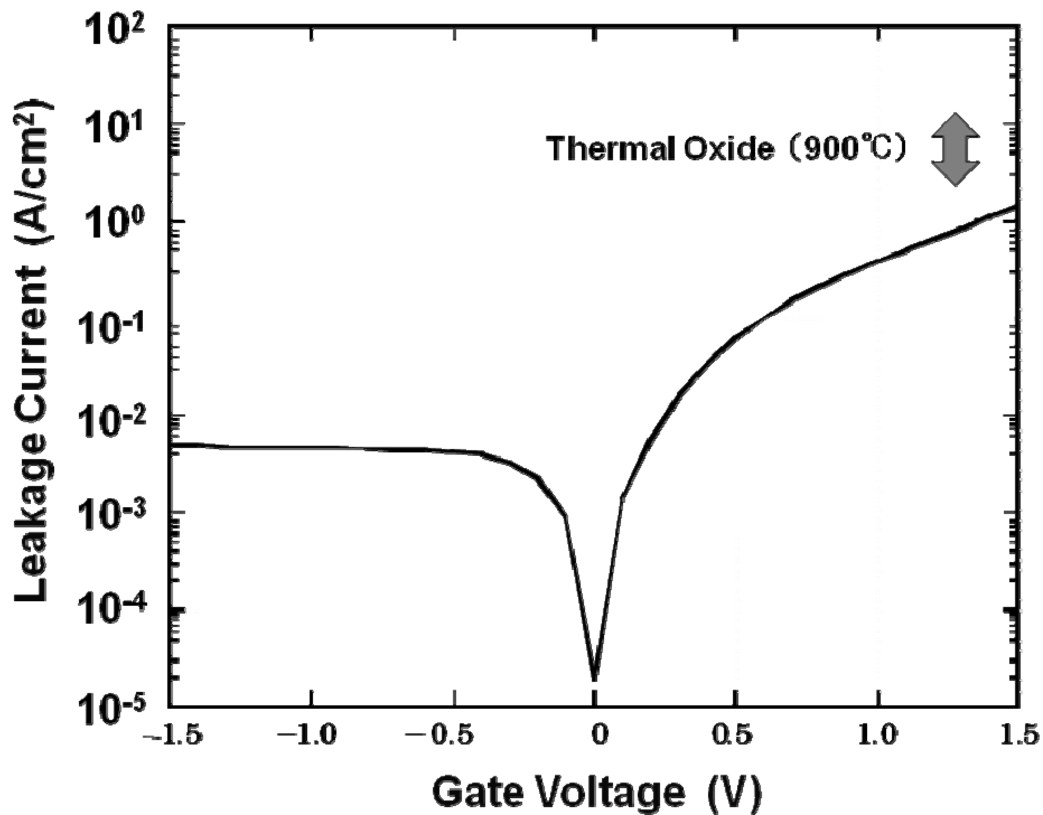

Figure 3-3. I-V characteristics of the <Al/NAOS SiO_2 (1.3nm)/n-type Si(100)> MOS diode formed with 68 wt% HNO_3 solutions at 120 °C for 10 min.

thickness [2].

Table 3-1 shows the leakage current density of the <Al/NAOS SiO_2 (1.3 nm)/n-type Si(100)> MOS diodes with HNO_3 concentrations of 40, 68, 90, and 98 % at various applied voltage in the range between 0.25 and 1.50 V. The NAOS SiO_2 layer was formed at the boiling point for 10 min. The leakage currents of thermally grown SiO_2 and SiON films were also listed in Table 3-1.

As seen in Table 3-1, the leakage current decreased with the HNO_3 concentration. With the PMA in H_2 at 200 °C for 20 min, the leakage current density decreased to less than that for a SiO_2 layer thermally grown at 900 °C with the equivalent oxide thickness [57-59].

The atomic density of the SiO_2 layer increases with the HNO_3 concentration

Current Density (A/cm^2)

	HNO_3 concentration	Applied voltage (V) 0.25	0.50	0.75	1.00	1.25	1.50
with PMA (200 °C)	40%	2.1	9.4	21	35	48	70
	68%	0.052	0.33	1.1	2.5	5.2	7
	90%	0.026	0.21	0.57	1.2	2.9	5.5
	98%	0.0017	0.018	0.086	0.32	1	2.8
Ref.	Thermal SiO_2				5~10		
	SiON				0.8~1.5		

Table 3-1. Leakage current Density vs. applied voltage of the <Al/1.3 nm NAOS SiO_2/Si(100)> MOS diode for various HNO_3 concentrations.

(cf. Section II-5), leading to the increase in the band discontinuity energy (cf. Section II-6). The Fowler-Nordheilm tunneling current (J) flowing through an SiO_2 layer is given by

$$J \propto E_{OX}{}^{2} \exp\left(-\frac{4\sqrt{2m^*}(q\phi_B)^{\frac{3}{2}}}{3q\hbar E_{OX}} \right) \quad (3\text{-}1)$$

where Eox is electric field in the SiO_2 layer, m^* is the effective mass of an electron in SiO_2, $\hbar$ is the Plank constant, q is the elementary electronic charge, and ϕ_B is the barrier height (cf. Figure 3-4) [56]. From Equation (3-1), an increase of the barrier height, i.e., the band discontinuity energy plus the energy difference between the Si Fermi level and the valence band maximum, exponentially decreases the tunneling probability of charge carriers through SiO_2, leading to a vast decrease in the leakage current density flowing with the Fowler-Nordheilm mechanism.

Another reason for the low leakage current density of the NAOS SiO_2 is attributable to negligibly low densities of SiO_2 gap-states originating from sub-oxides in the SiO_2 layer as described in Section II-4. These states would cause that the charge carriers can transfer through SiO_2 by gap-states hopping conduction as shown in Figure 3-5, which increases the leakage current density.

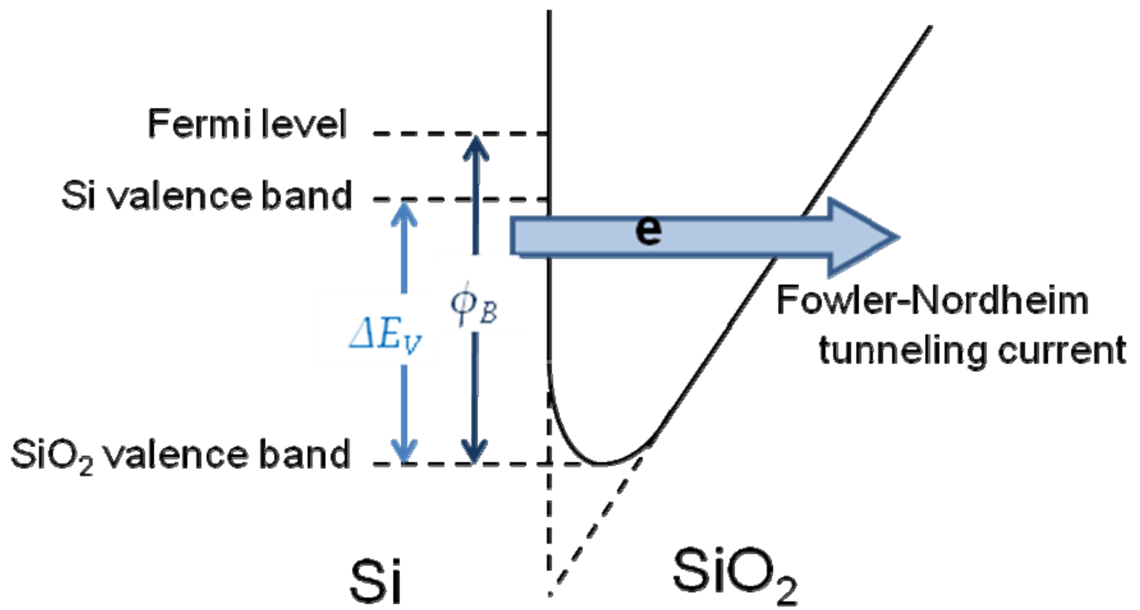

Figure 3-4. Mechanism of Fowler-Nordheim tunneling current flowing through SiO_2 layer. ΔE_V : valence-band discontinuity energy, ϕ_B : barrier height.

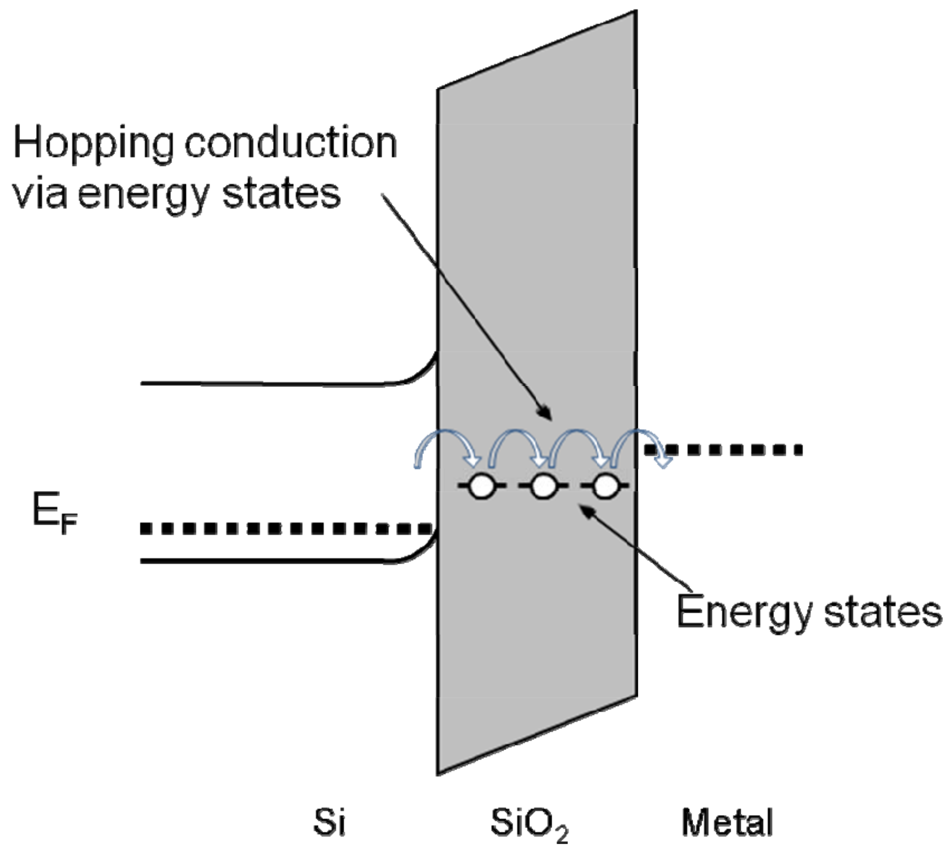

Figure 3-5. Mechanism of the hopping conduction current via energy states in the band-gap of SiO_2 layer.

Figure 3-6 shows the current-electric field (I-E) curves for the <Al/SiO_2/Si(100)> MOS diodes with the SiO_2 layers formed by the NAOS method with and without POA. The NAOS SiO_2 layers were formed with 68 wt% HNO_3 solutions at 120 °C. Even without POA (curve a), the leakage current density was considerably low (~10^{-6} A/cm^2 at 8 MV/cm) in spite of the low temperature SiO_2 formation at 120 °C. With POA in dry-oxygen at 400 °C (curve b), the leakage current density was nearly unchanged. When POA was performed in wet-oxygen (curve c), on the other hand, the leakage current density greatly decreased by 1~3 orders of magnitude (~10^{-9} A/cm^2 at 8 MV/cm).

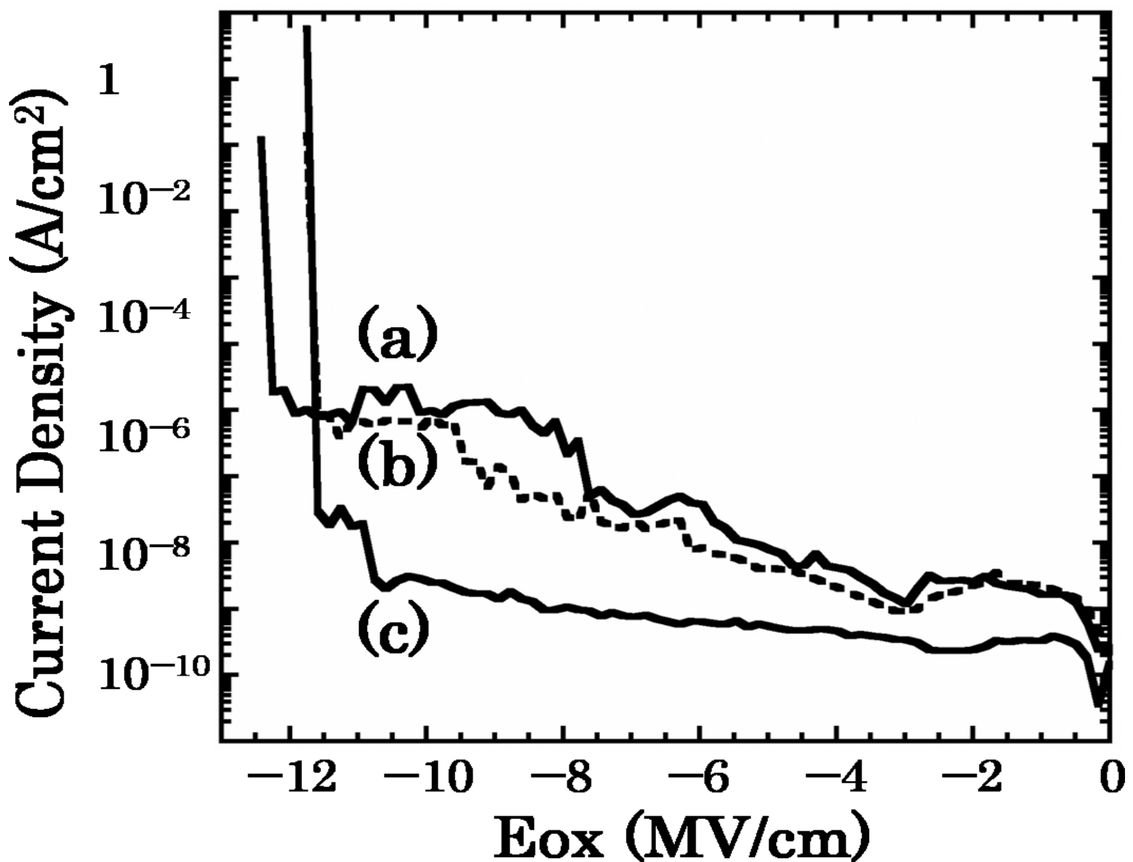

Figure 3-6. Leakage current density of the <Al/SiO_2/Si(100)> MOS diodes with the SiO_2 layers formed by the NAOS method at 120 °C vs. electric field: (a) without POA; (b) with POA in dry-oxygen at 400 °C; (c) with POA in wet-oxygen at 400 °C.

As described above, contrary to conventional low temperature SiO_2 fabrication methods such as CVD methods, a uniform thickness SiO_2 layer can be formed using the NAOS method, which leads to the lower leakage current density than that of an SiO_2 layers formed by deposition methods. The formation of the uniform thickness SiO_2 layer is due probably to isotropic supply of oxidizing species during the NAOS oxidation.

I think that an increase in the atomic density is another important reason for the decrease in the leakage current density, because the tunneling probability of charge carrier remarkably decreases with increasing the atomic density as described in Section II - 6.

III - 3. C-V Characteristics

Capacitance-voltage (C-V) curves were recorded at 1 MHz using a YHP 4192A impedance analyzer to obtain information on interface states, slow states, fixed charges, etc. It is generally difficult to measure C-V curves for an ultra-thin SiO_2 layer because of a high density leakage current. The fabricated NAOS SiO_2 layer possesses a high atomic density and a low leakage current density in spite of the ultra-thin thickness, and hence, the C-V curves are measurable.

Figure 3-7 shows the C-V curves of the <Al/NAOS SiO_2/Si(100)> MOS diodes formed by 68 wt% HNO_3 at 120 ºC with POA. Curves (a), (b), and (c) are for the MOS diodes without POA, with POA in dry-oxygen, and with POA in wet-oxygen, respectively.

Without POA (curve a), no hump was present in the C-V curve, while after POA in dry-oxygen (curve b), a hump appeared at –1 V, probably due to generation of high density interface states [60]. Moreover, there was a hysteresis with the magnitude of 0.12V ± 0.08 V after POA in dry-oxygen (curve b). When POA was performed in wet-oxygen at 400 ºC (curve c), on the other hand, neither a hump nor a hysteresis appeared at all. In addition, the C-V curve shifted by ~0.8 V in the positive gate bias

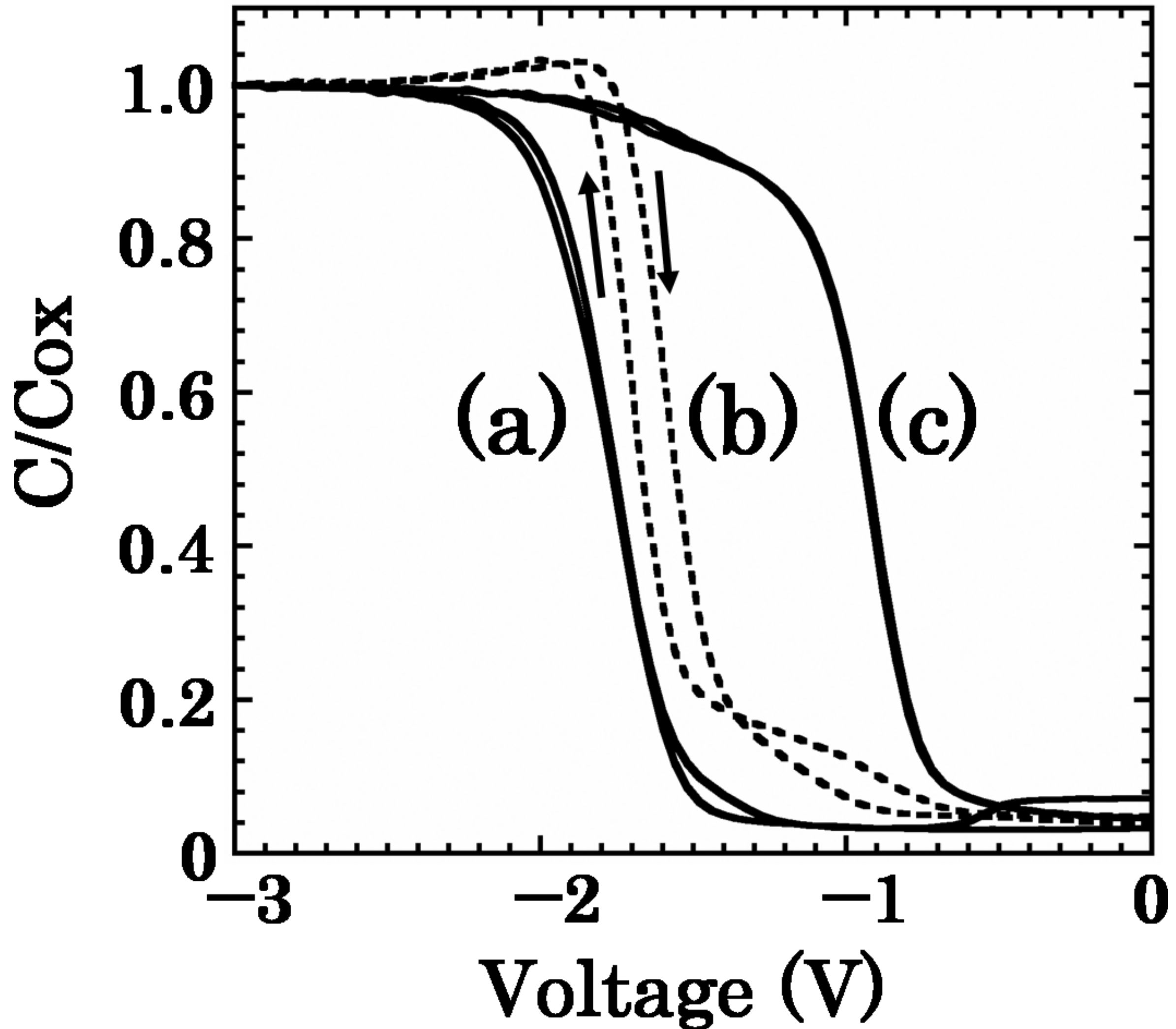

Figure 3-7. C-V curves of the <Al/NAOS SiO_2/p-type Si(100)> MOS diodes with the SiO_2 layers formed by the NAOS method with 68 wt% HNO_3 at 120 °C: (a) without POA; (b) with POA in dry-oxygen at 400 °C; (c) with POA in wet-oxygen at 400 °C.

direction.

It is considered that this hysteresis was caused by slow states, i.e., energy states near the interface, where electron injection and emission cannot respond to the scanning time of the C-V measurement because of a high emission energy (i.e., deep states) or of location slightly distant from the SiO_2/Si interface [61]. As shown in Figure 3-8, slow states above the SiO_2 Fermi level, E_F, are vacant in the accumulation

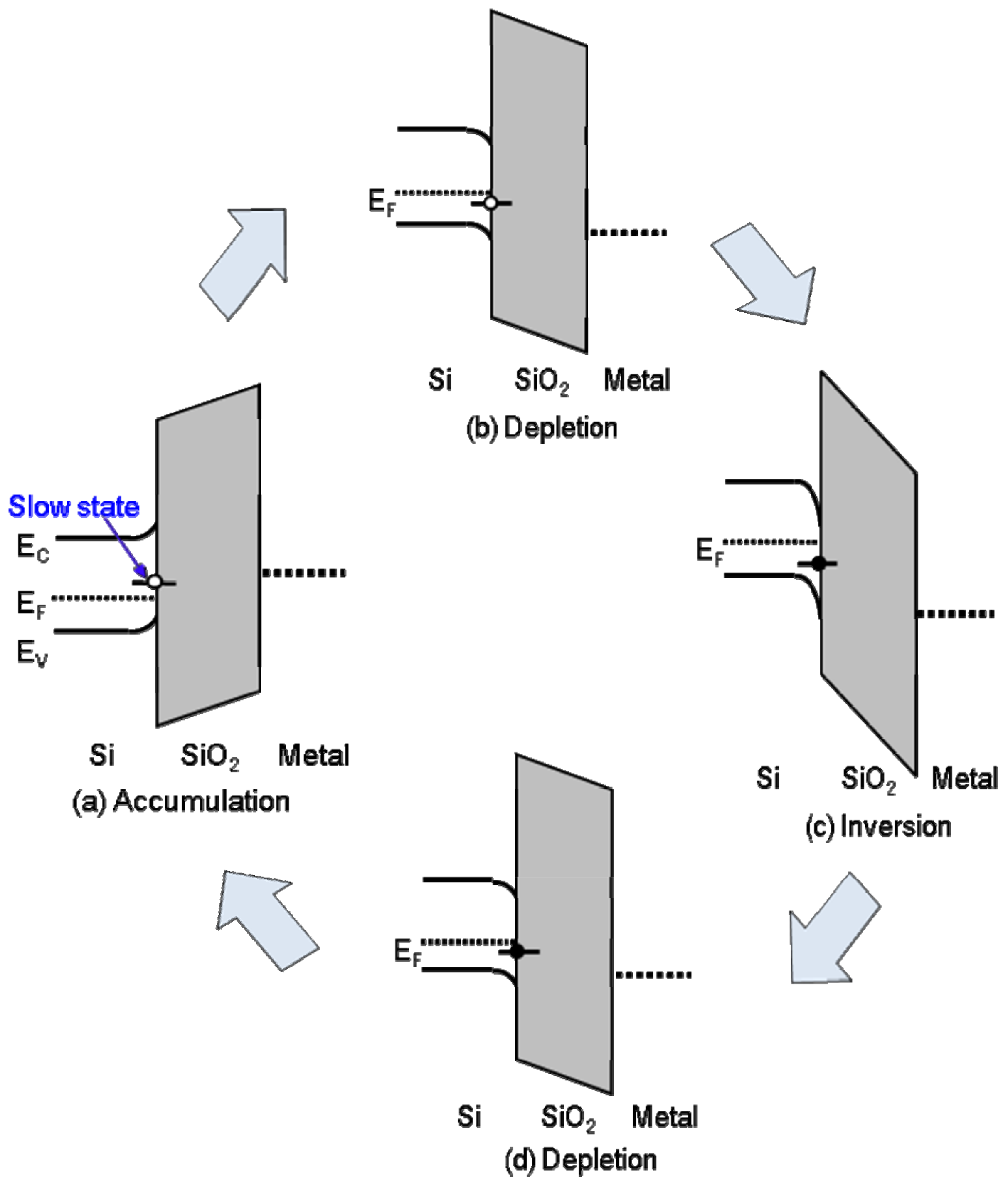

Figure 3-8. Schematics of the behavior of slow states at the SiO_2/Si interface. Black and white circles represent occupation and vacancy in the slow states, respectively: (a) accumulation condition; (b) depletion condition after accumulation condition; (c) inversion condition; (d) depletion condition after inversion condition.

condition (Figure 3-8 a), and they are still vacant when the energy level of the slow states is slightly below E_F in the depletion condition (Figure 3-8 b). By application of a sufficiently high positive bias to the metal electrode (i.e., under inversion condition), electrons occupy the slow states (Figure 3-8 c). When the positive voltage is decreased and the slow state level is located above E_F, they are still occupied by electrons (Figure 3-8 d).

The slow state density (N_{SS}) can be calculated from the hysteresis voltage (V_{Hy}) and the SiO_2 capacitance (C_{OX}) as the following equation [56].

$$V_{Hy} = \frac{qN_{SS}}{C_{OX}} \tag{3-2}$$

From Equation (3-2), N_{SS} for curve (b) in Figure 3-7 was estimated to be $4\times10^{11} \pm 3\times10^{11}$ /cm^2.

The flat-band voltage (V_F) is defined as the applied voltage where there is no band-bending of the semi-conductor, and the V_F shift is a useful information to estimate the fixed charges in the SiO_2 layer.

The V_F is the gate voltage when the MOS capacitance is equal to the flat-band capacitance. Here, the flat-band capacitance (C_{FB}) is expressed as

$$\frac{1}{C_{FB}} = \frac{1}{C_{OX}} + \frac{L_D}{\varepsilon_{Si}\varepsilon_0} \tag{3-3}$$

where L_D is the Debye length (i.e., depletion layer width at the flat-band condition) [56], which is defined as

$$L_D = \sqrt{\frac{\varepsilon_{Si}\varepsilon_0 kT}{q^2 N_A}} \tag{3-4}$$

and ε_{Si} is the relative dielectric constant of Si, ε_0 is the permittivity in vacuum, k is the Boltzmann constant, T is the absolute temperature, and N_A is the impurity (boron) concentration in the Si substrate, which is estimated to be 6×10^{15} /cm^3 from the minimum capacitance of the C-V curves in Figure 3-7 [56].

The measured V_F of the MOS diodes without POA was present at –1.58 ± 0.04 V. POA in dry-oxygen slightly shifted V_F to –1.10 ± 0.04 V, while that in wet-oxygen at 400 °C greatly changed it to –0.82 ± 0.04 V. The relation between V_F and the density of oxide fixed charges (N_{FC}) is expressed as

$$V_F = \Delta\phi + \left(-\frac{qN_{FC}}{C_{OX}} \right) \quad (3\text{-}5)$$

and

$$\Delta\phi = \phi_M - \left(\chi_{Si} + \frac{E_G}{2q} + \frac{kT}{q}\log\left(\frac{N_A}{n_i}\right)\right) \quad (3\text{-}5)$$

where $\Delta\phi$ is the energy difference between the Fermi level of the Si substrate and that of Al electrode under no applied bias, ϕ_M is work function of Al (4.20 V), χ_{Si} is electron affinity of Si (4.15 V), E_G is the band-gap energy of Si (1.12 V), n_i is the intrinsic carrier density of Si (1.45×10^{10} /cm^3 at 27 °C) [56]. Adopting –0.85 V as an ideal V_F estimated from $\Delta\phi$ in Equation (3-5), the density of the oxide fixed positive charges is estimated to be $+2.8\times10^{12} \pm 0.2\times10^{12}$ /cm^2 for the SiO_2 layer without POA, $+9.0\times10^{11} \pm 1\times10^{11}$ /cm^2 and $-1.0\times10^{11} \pm 1\times10^{11}$ /cm^2, respectively, for those with POA in dry-oxygen and wet-oxygen.

Oxide fixed charges may be dispersively located through the SiO_2 layer, and in this case, the term for oxide fixed charges in Equation (3-5) is written as

$$\frac{qN_{FC}}{C_{OX}} = \frac{1}{\varepsilon_{OX}\varepsilon_0}\int_0^{T_{OX}} x\rho_{OX}(x)dx \quad (3\text{-}7)$$

where ε_{OX} is the relative dielectric constant of SiO_2, T_{OX} is the thickness of SiO_2, and $\rho_{OX}(x)$ is the density of oxide fixed charges at the location of x. However, in order to simplify the discussion, the density of oxide fixed charges was estimated based on the assumption that they are located just at the SiO_2/Si interface.

POA in dry-oxygen generates interface states (curve b in Figure 3-7), probably due to desorption of OH species included in the NAOS SiO_2 layer, resulting in the

formation of Si dangling bonds. A leakage current can flow via interface states with increasing its density [53,54] by decreasing the barrier height from Φ_B to Φ_B^*, as shown in Figure 3-9. Due to the two competing effects, i.e., the increase in the SiO_2 atomic density and the formation of interface states, the leakage current density is nearly unchanged by POA in dry-oxygen (curve b in Figure 3-6). POA in wet-oxygen, on the other hand, does not form interface states (curve c in Figure 3-7). In this case, some of Si-OH bonds are likely to be replaced by Si-H bonds by the reaction of hydrogen atoms generated by decomposition of water. It is also likely that hydrogen atoms eliminate oxide fixed charges. In fact, the density of oxide fixed positive charges decreases from $+2.8\times10^{12}$ to -1.0×10^{11} /cm^2 by POA in wet-oxygen.

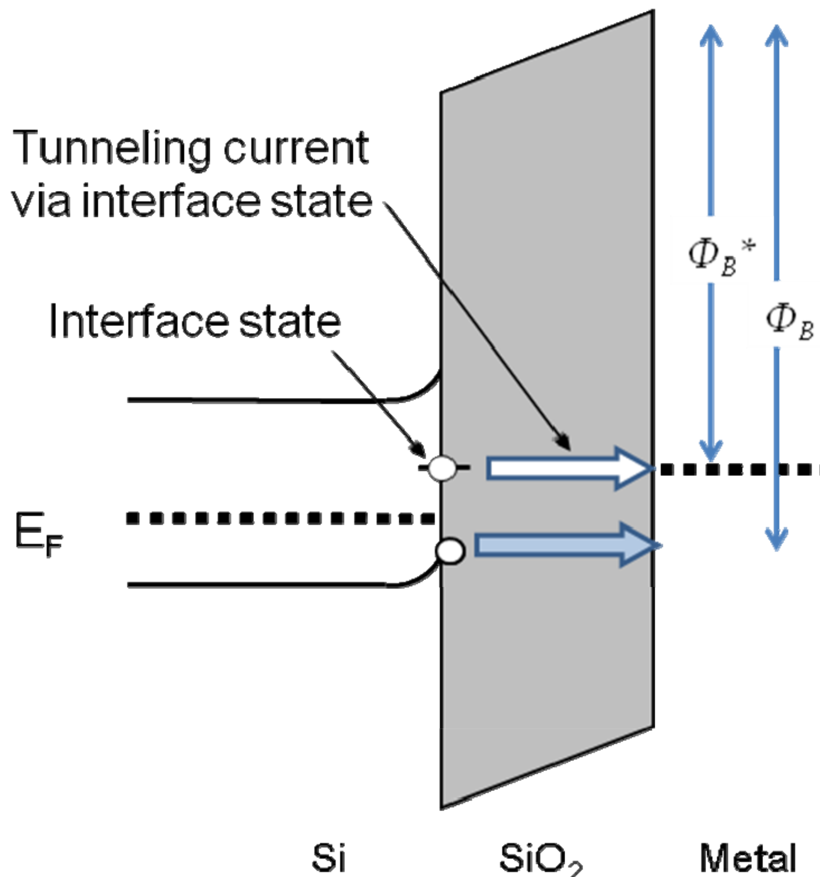

Figure 3-9. Mechanism of the tunneling current via interface states. The barrier height Φ_B decreases to Φ_B^* with the existence of the interface states.

The threshold voltage (V_{th}) of TFTs corresponds to the bias voltage to achieve strong inversion condition, and this is the sum of the flat-band voltage and the bias to move to strong inversion condition from flat-band condition. This is because charges at the metal electrode (Q_M) necessary for the strong inversion condition is given by

$$Q_M = Q_n + Q_D + Q_f \quad (3\text{-}8)$$

where Q_n is the charges accumulated at the interface, Q_D is depletion layer charges, and Q_f is oxide fixed charges as shown in Figure 3-10. Therefore, V_{th} is changed by

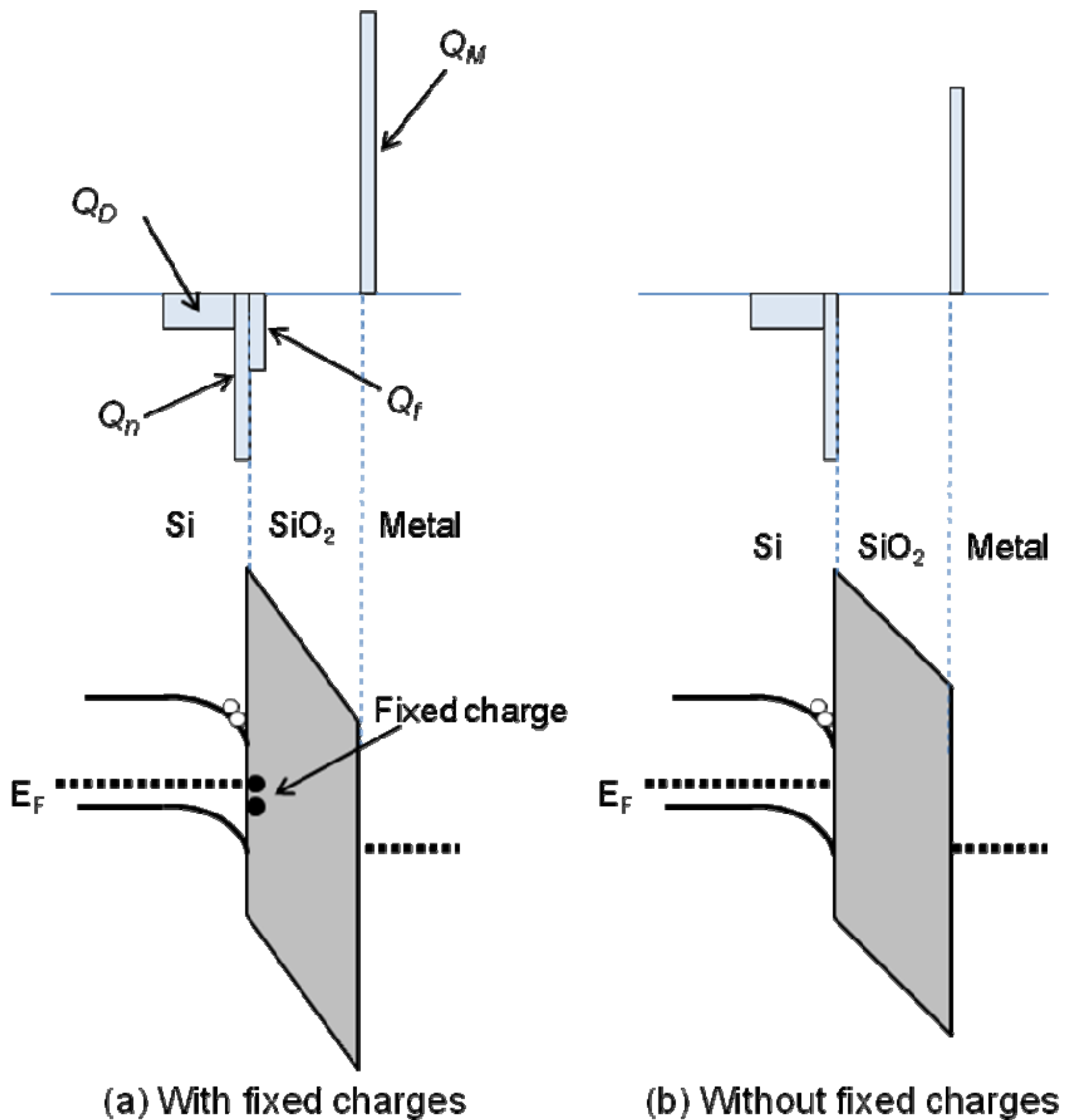

Figure 3-10. Schematics of charge distribution and band diagram of MOS diode: (a) with oxide fixed charges; (b) without oxide fixed charges.

the flat-band shift increased by oxide fixed charges in SiO_2. In the case of too low $|V_{th}|$, an undesirable current flows at zero bias, leading to an increase in the power consumption. On the other hand, when $|V_{th}|$ becomes very high, a supply voltage to operate TFTs should be higher, also leading to an increase in the power consumption. From the above reasons, the decrease in the oxide fixed charge density Q_f is effective for a reduction in TFT power consumption by achieving desirable V_{th}.

Figures 3-11 (a) and (b) show the band diagrams of the <Al/SiO_2/Si> MOS structures with poor and good properties of SiO_2 and its interface, respectively. For the SiO_2/Si structure with poor properties, high density interface states and SiO_2 gap-states in the bulk SiO_2 are present, and charge carrier flows through SiO_2 via interface states and gap-states, increasing a leakage current density. Furthermore, the band discontinuity energy (χ) at the SiO_2/Si interface is low, also leading to an increase in the leakage current density.

The conventional PE-CVD SiO_2 layer is supposed to have the band diagram shown in Figure 3-11 (a). Thermally grown SiO_2, on the other hand, has a band

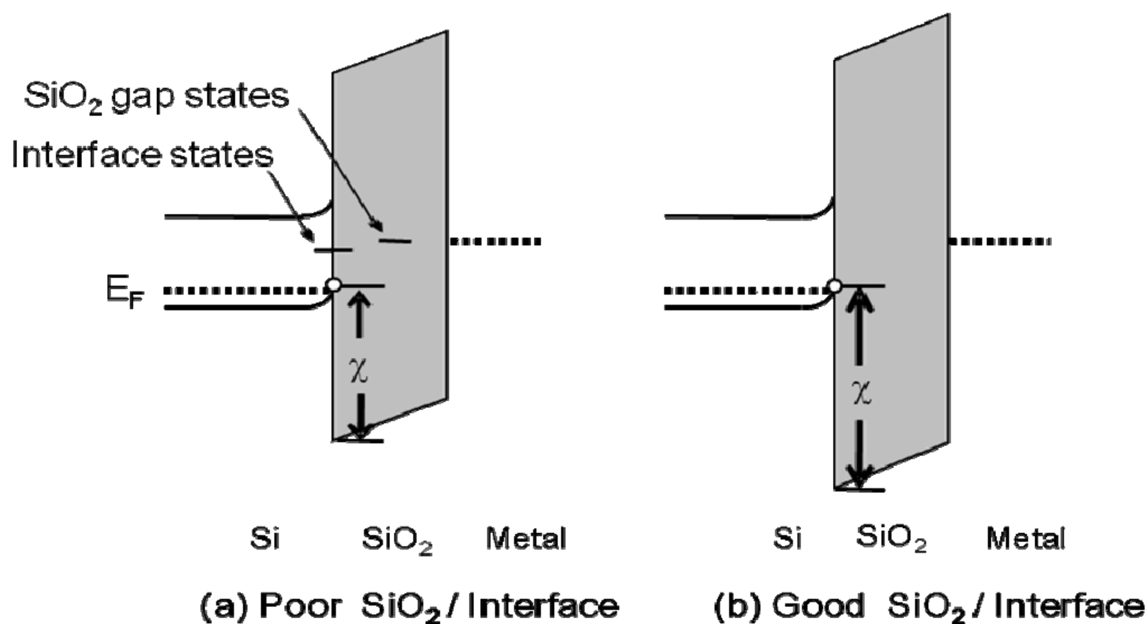

Figure 3-11. Band diagrams of <Al/SiO_2/Si> MOS structures with (a) poor and (b) good properties of SiO_2 bulk and SiO_2/Si interface.

diagram similar to Figure 3-11 (b).

The properties of the NAOS SiO_2 layer are much better than those of the conventional PE-CVD SiO_2 layer. Although the properties of the as-formed NAOS SiO_2 are not as good as those of thermally grown SiO_2, thermal treatments such as POA and PMA greatly improve the properties nearly to the same level as or above the thermally grown SiO_2.

III – 4. Summary

I have fabricated SiO_2/Si structures by use of the NAOS method, i.e., immersion of Si in HNO_3 aqueous solutions. Measurements of I-V and C-V curves lead to the following results and conclusion:

1) The NAOS SiO_2 layer possesses a considerably low leakage current density even without POA (e.g., 10^{-6} A/cm^2 at 8 MV/cm) and it is greatly decreased (e.g., 10^{-9} A/cm^2 at 8 MV/cm) by POA at 400 °C in wet-oxygen.
2) Interface states are generated by POA in dry-oxygen at 400 °C, while no generation occurs in the case of POA in wet-oxygen.
3) The density of oxide fixed charges decreases from $+2.8\times10^{12}$ to -1.0×10^{11} /cm^2 by POA at 400 °C in wet-oxygen.
4) The NAOS SiO_2 layer formed at 120 °C possesses excellent characteristics, such as low leakage current density, low interface state density, and low slow state density.

The decrease in the leakage current density by POA in wet-oxygen is attributable to i) an increase in the band discontinuity energy at the SiO_2/Si interface caused by an increase in the SiO_2 atomic density, ii) passivation of interface states, and iii) elimination of unfavorable species such as oxide fixed charges.

IV. Characteristics of Poly-Si TFTs with NAOS SiO_2 Layer

IV -1. TFT Structure and Fabrication Process

Figure 4-1 shows the cross-sectional schematic of the fabricated poly-Si TFT on a glass substrate. The TFT has a top-gate structure with NAOS SiO_2/PE-CVD SiO_2 stacked gate insulator. Figure 4-2 shows the cross-sectional TEM micrograph of the

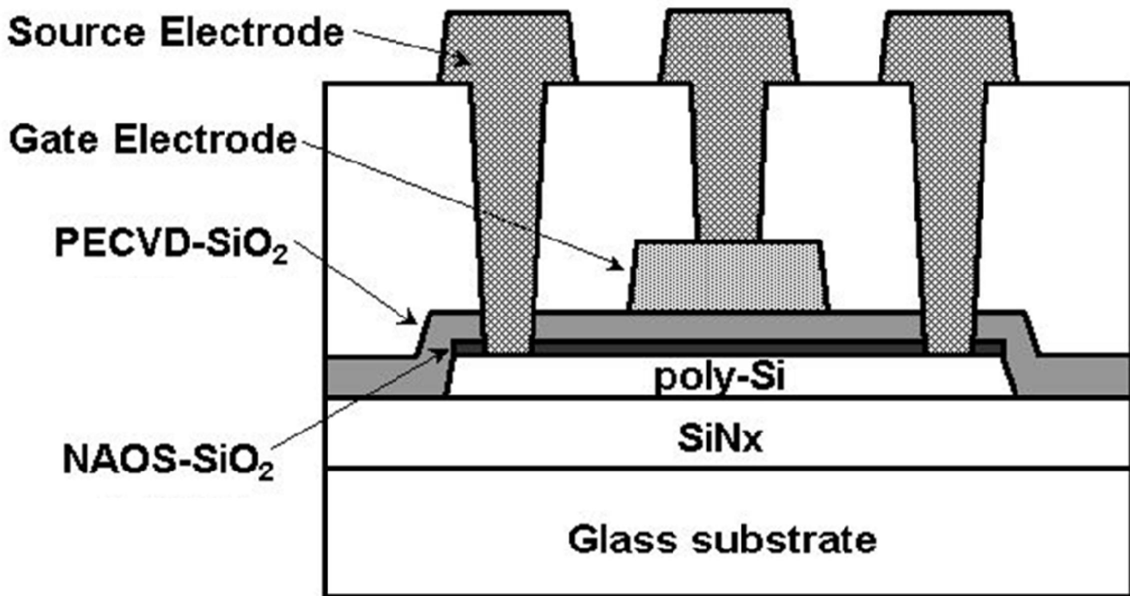

Figure 4-1. Schematic of cross-sectional structure of a poly-Si TFT with NAOS SiO_2/CVD SiO_2 stacked gate insulator.

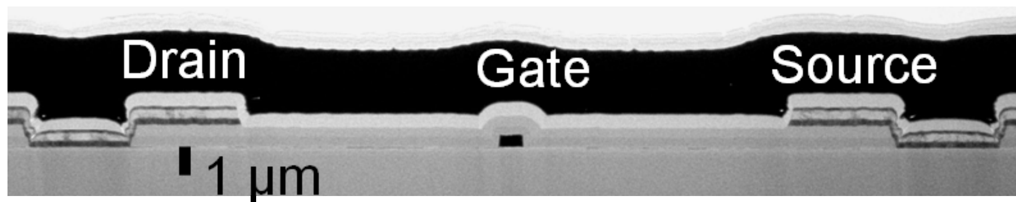

Figure 4-2. Cross-sectional TEM micrograph of the fabricated poly-Si TFT on a glass substrate.

poly-Si TFT.

The fabrication process flow of the poly-Si TFTs is shown in Figure 4-3 and it is described below. TFTs were fabricated on non-alkali metal glass substrates of 32×40 cm^2. After deposition of a 100 nm-thick silicon nitride (SiN) layer to prevent diffusion of undesirable species from the glass substrates, a 50 nm-thick amorphous Si thin film was deposited by use of the PE-CVD method. The amorphous Si films were thermally annealed and irradiated using an excimer laser in order to crystallize and form a poly-Si thin film. On the poly-Si thin film, an ultra-thin SiO_2 layer was formed by immersion in 68wt% HNO_3 aqueous solutions (i.e., azeotropic mixture of HNO_3 and water), followed by annealing at 400 °C. On the NAOS SiO_2 layer, an SiO_2 layer was deposited using the PE-CVD method. Tungsten (W) gate electrodes were formed by the sputtering method, and source and drain regions were defined by ion implantation with phosphorous ions (P^-) and boron ions (B^+) for n-channel (N-ch) and p-channel (P-ch) transistors, respectively, followed by activation annealing at 500 °C for 1 h in nitrogen atmosphere. Then, a dielectric interlayer was deposited by PE-CVD, and contact holes and wires of aluminum (Al) were fabricated for forming the electrodes. After that, the TFTs were annealed in hydrogen atmosphere at 200 °C as the PMA.

The TFTs with the gate insulator without a NAOS SiO_2 layer were also fabricated in order to compare the TFT characteristics and to confirm the effectiveness of the NAOS SiO_2 layer.

Electrical characteristics of the fabricated TFTs were measured using an Agilent B1500A semiconductor device analyzer. The threshold voltage (V_{th}) was defined as the gate-source voltage (V_{gs}) where the drain current (I_d) at $|V_{ds}|$ (the drain-source voltage)=0.1 V was $(W/L)\times10^{-7}$ A (W: gate width, L: gate length). The field-effect mobility (μ_{FE}) was calculated from the maximum transconductance at $|V_{ds}|$=0.1 V, and the effective mobility (μ_{eff}) was estimated from linear extrapolation of the I_d-V_{gs} curves in the region between the threshold voltage and the supply voltage to the voltage axis. Sub-threshold coefficient (S-value) is defined as a change of V_{gs} when I_d was increased by one order of magnitude in the sub-threshold

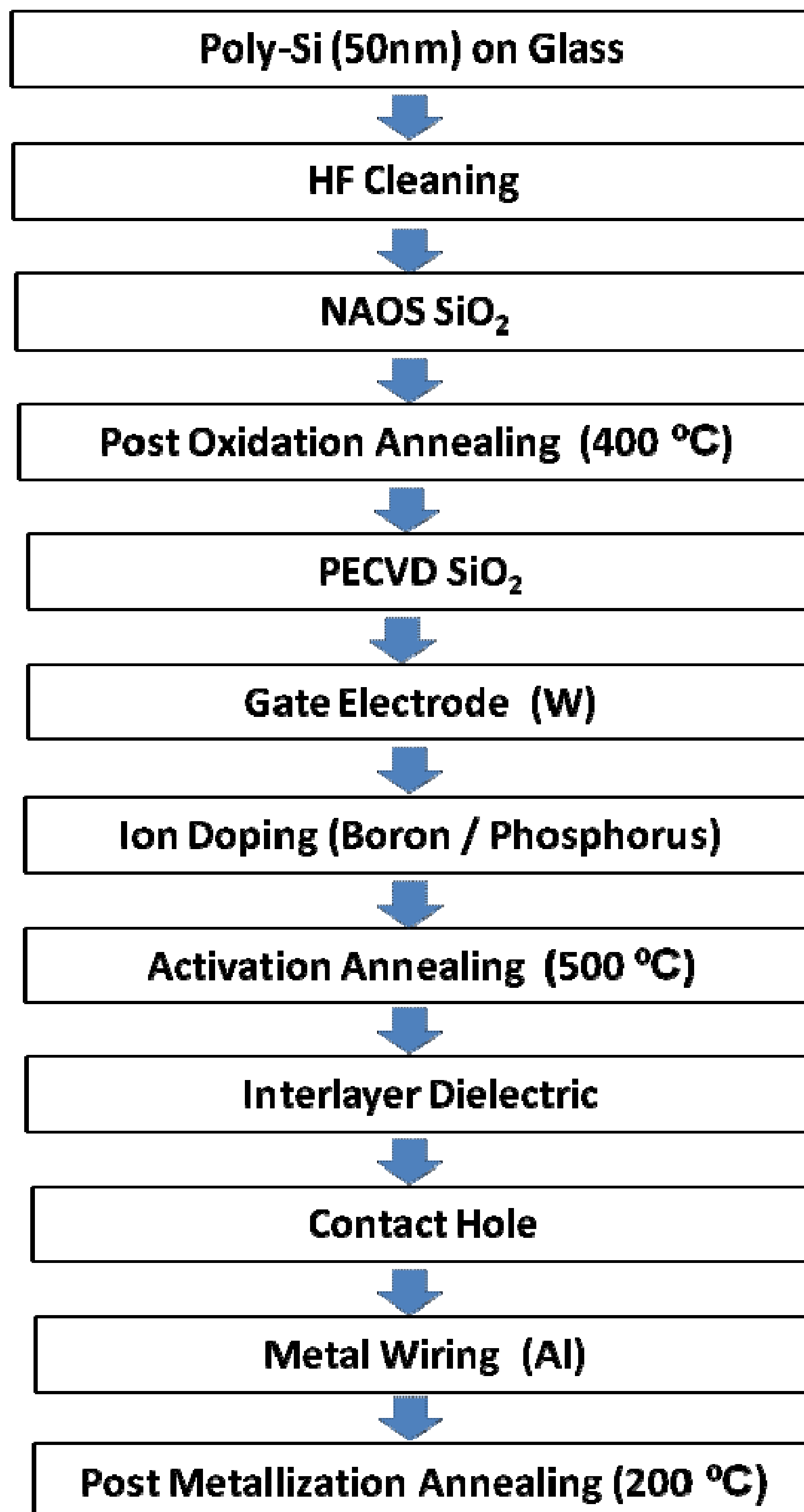

Figure 4-3. Process flow of TFT fabrication with a NAOS SiO_2/PE-CVD SiO_2 stacked gate insulator.

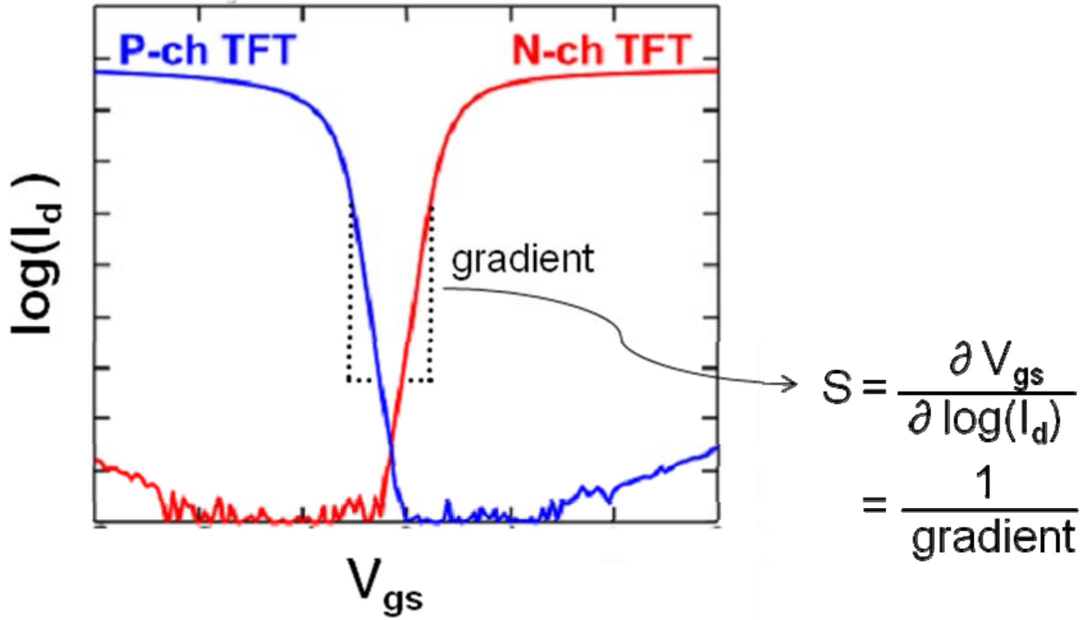

Figure 4-4. Definition of sub-threshold coefficient (S-value) of transistors.

region, and it was calculated from the gradient of log(I_d)- V_{gs} curve (cf. Figure 4-4).

IV -2. Characteristics of Poly-Si TFTs and Interface State Density

The drain current (I_d) of the MOS transistor is expressed as

$$I_d = \frac{\varepsilon_{ox}\varepsilon_0}{T_{ox}}\mu_{eff}\frac{W}{L}\left(V_{gs} - V_{th} - \frac{V_{ds}}{2}\right)V_{ds} \qquad (V_{ds} \le V_{gs} - V_{th}) \qquad (4\text{-}1)$$

$$I_d = \frac{1}{2}\frac{\varepsilon_{ox}\varepsilon_0}{T_{ox}}\mu_{eff}\frac{W}{L}\left(V_{gs} - V_{th}\right)^2 \qquad (V_{ds} \ge V_{gs} - V_{th}) \qquad (4\text{-}2)$$

under the gradual channel approximation [62]. Equation (4-1) indicates that I_d is proportional to V_{ds} in the linear region (i.e., $V_{ds} \le V_{gs} - V_{th}$), and I_d is not dependent on V_{ds} and saturated in the saturation region (i.e., $V_{ds} \ge V_{gs} - V_{th}$).

Figures 4-5 to 4-12 show the characteristics of the TFTs with a 1.4 nm NAOS SiO_2/10 nm CVD SiO_2 stacked gate insulator structure and the NAOS SiO_2 layer formed with 68 wt% HNO_3 at 120 °C.

Drain current vs. drain-source voltage (I_d- V_{ds}) curves for the TFTs with the above stacked gate insulator structure are shown in Figure 4-5. The gate length and the gate width are 0.9 and 10.0 μm, respectively. Due to the excellent leakage characteristics of the NAOS SiO_2 layer, the thickness of the gate oxide layer in the TFTs could be decreased to ~10 nm. The shrinkage of the gate oxide layer enables miniaturization of TFTs, and I have succeeded in the fabrication of sub-micrometer TFTs. It is noted that the sub-micrometer poly-Si TFTs could be operated correctly. In spite of the low driving voltage below 3.0 V, the I_d- V_{ds} curves possessed ideal features with high saturation currents. This result demonstrates that the TFTs can

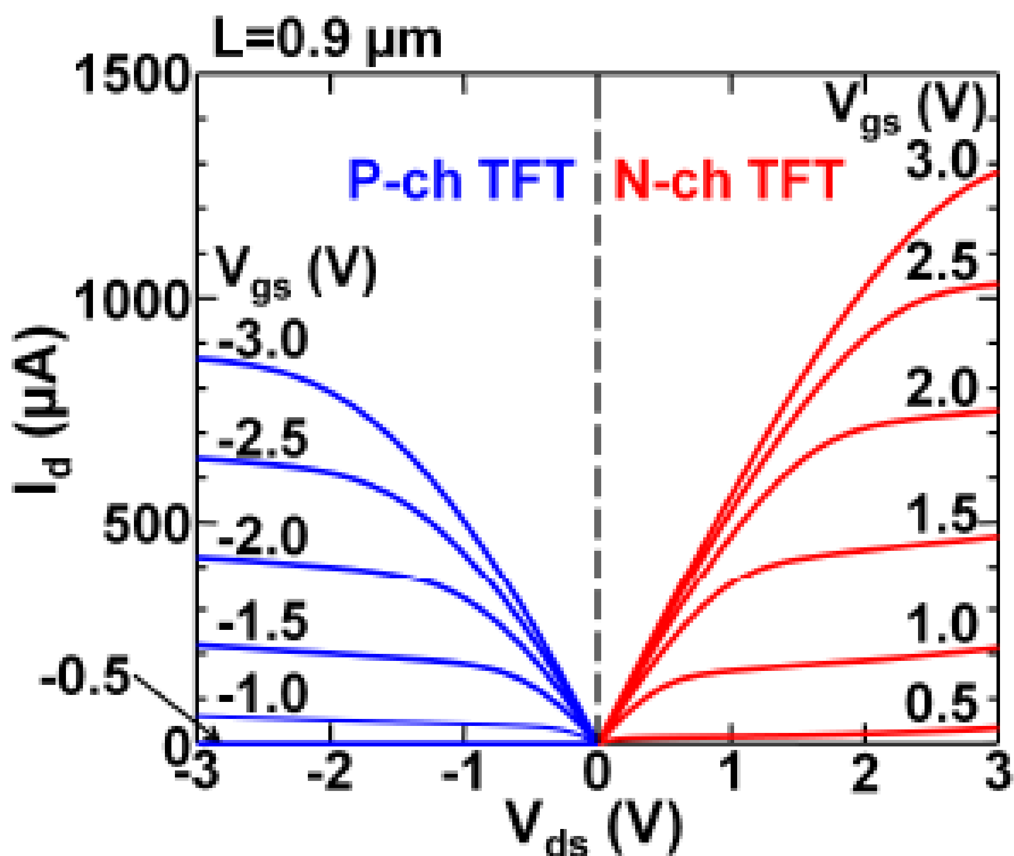

Figure 4-5. I_d- V_{ds} curves for the TFTs with the 1.4 nm NAOS SiO_2/10 nm CVD SiO_2 stacked gate insulator structure. L is 0.9 μm and W is 10.0 μm.

be operated even at 1.0 V.

Figures 4-6 and 4-7 show the drain current vs. gate-source voltage (I_d-V_{gs}) curves at $|V_{ds}|$=0.1 V for TFTs with and without a NAOS SiO_2 layer, respectively. The drain current largely changed with the gate voltages in the region between 0 and 1 V for the N-ch TFTs and between –1 and 0 V for the P-ch TFTs. The sharp features of the I_d-V_{gs} curves indicated low S-values.

Figures 4-8 and 4-9 show the scatter diagram of on-current (I_{on}) vs. off-current (I_{off}, i.e., current at $|V_{gs}|$>~1.5 V) for N-ch and P-ch TFTs, respectively. I_{on} was measured at $|V_{ds}|$=3.0 V and $|V_{gs}|$=3.0 V, while I_{off} at $|V_{ds}|$=3.0 V and $|V_{gs}|$=1.0 V. I_{off} for the N-ch and P-ch TFTs with the NAOS SiO_2 layer was lower by ~2 orders of magnitude than those without it. The I_{off} for the TFTs with the 1.4 nm NAOS SiO_2/10nm CVD SiO_2 stacked layer was nearly the same as that for the TFTs with the 20 nm CVD SiO_2 layer. Similar low I_{off} was obtained from the TFTs with the 3.6 µm gate length.

With the NAOS SiO_2 layer, I_{off} became much lower than that without it, which demonstrated that the 1.4 nm NAOS interfacial SiO_2 layer could effectively block the gate leakage current.

Figure 4-10 shows the S-values of the TFTs with and without a NAOS SiO_2 layer at $|V_{ds}|$=3.0 V. The S-values were between 65~80 mV/dec, and were almost the same for the TFTs with the gate length of 0.9 and 3.6 µm. These S-values were significantly low and close to the ideal value (i.e., theoretical limit) of 60 mV/dec at room temperature [63,64], which corresponded to the situation where the whole gate bias was applied to Si for the band bending. This situation is satisfied when the net bias voltage across gate oxide should be negligibly low, which is, in turn, satisfied by thin gate oxide and low interface state density [56].

The interface state density can be calculated from the S-values which represent the behavior of the sub-threshold current of TFTs. The sub-threshold current is expressed as

$$I_{ds} = \mu_{eff} \frac{W}{L} \sqrt{\frac{\varepsilon_{Si} q N_A}{4\Psi_B}} \left(\frac{kT}{q}\right)^2 \left(\exp\frac{q(V_{gs}-V_{th})}{nkT}\right)\left(1-\exp\frac{-qV_{ds}}{kT}\right) \quad (4\text{-}3)$$

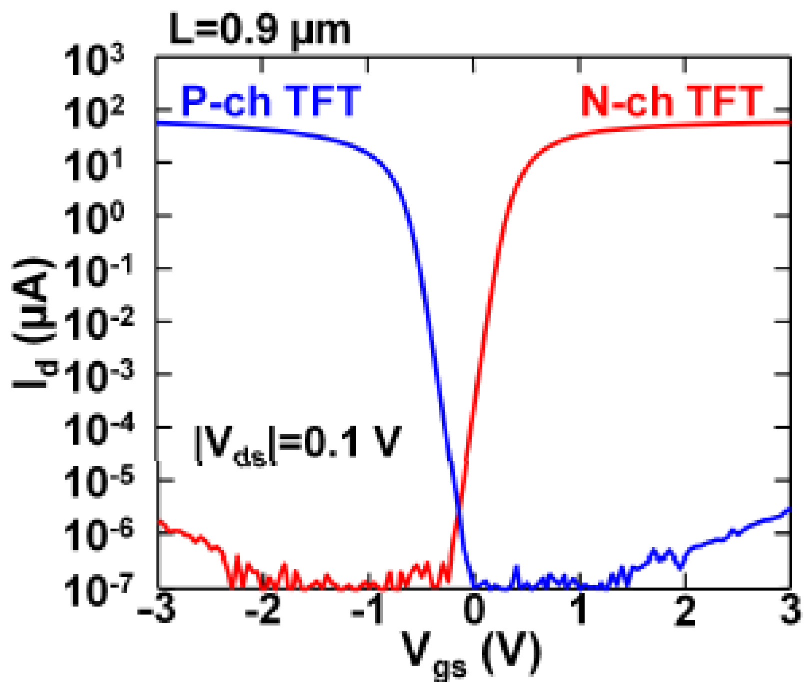

Figure 4-6. I_d- V_{gs} curves for the TFTs with the 1.4 nm NAOS SiO_2/10 nm CVD SiO_2 stacked gate insulator structure.

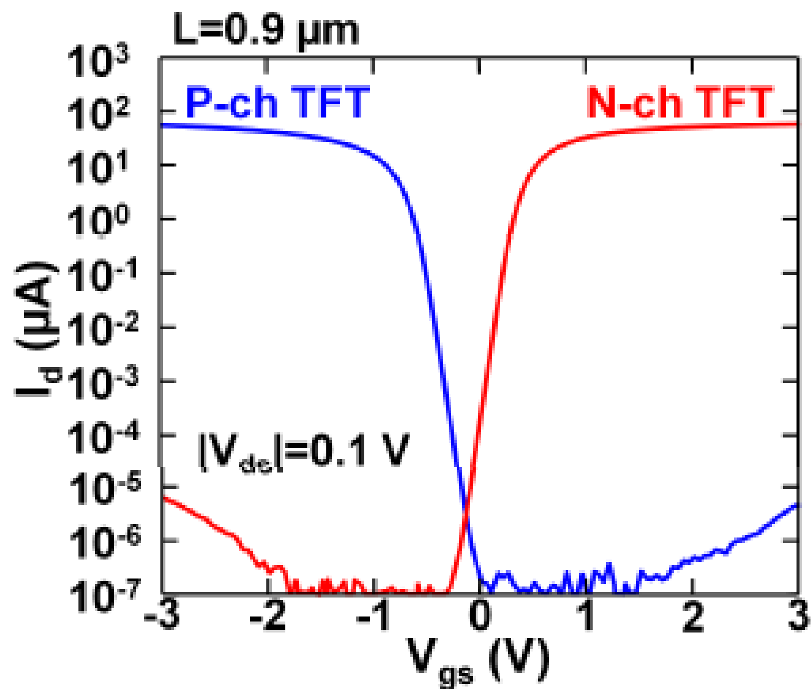

Figure 4-7. I_d- V_{gs} curves for the TFTs with the 10 nm CVD SiO_2 gate insulator structure.

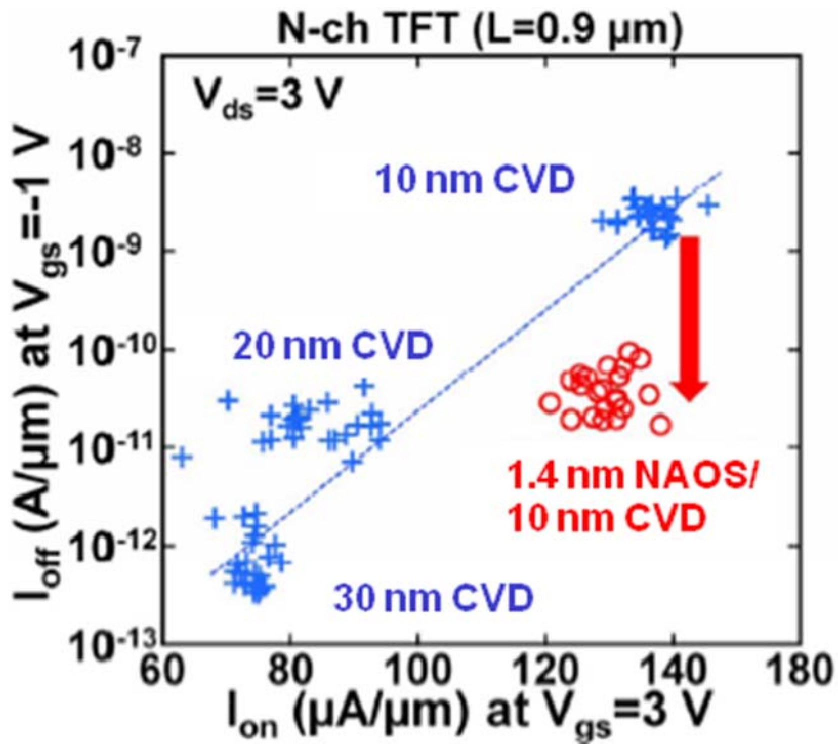

Figure 4-8. Scatter diagram of I_{on} vs. I_{off} for the N-ch TFTs with and without a NAOS layer.

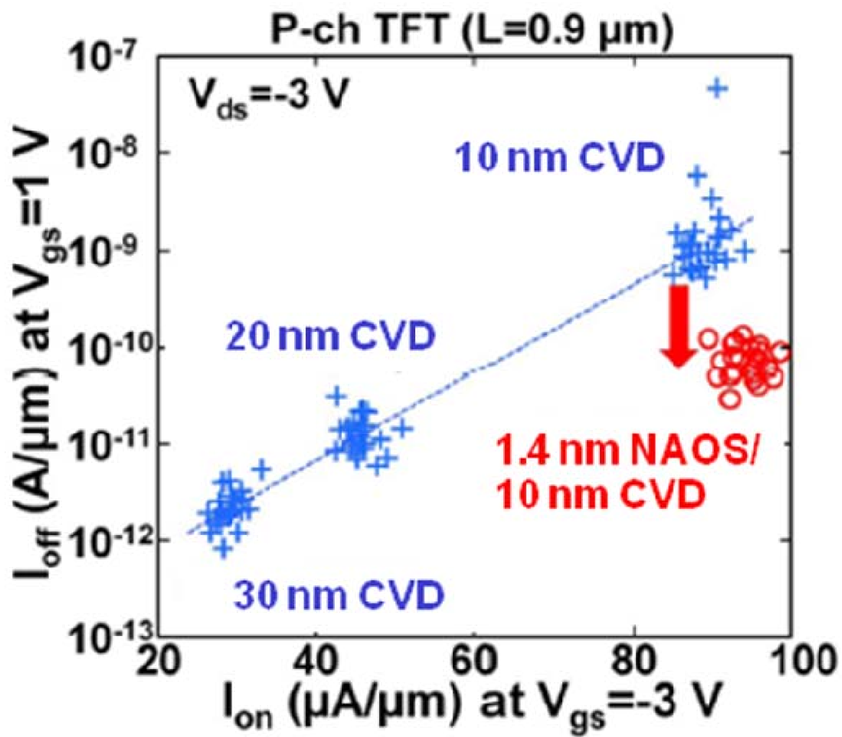

Figure 4-9. Scatter diagram of I_{on} vs. I_{off} for the P-ch TFTs with and without a NAOS layer.

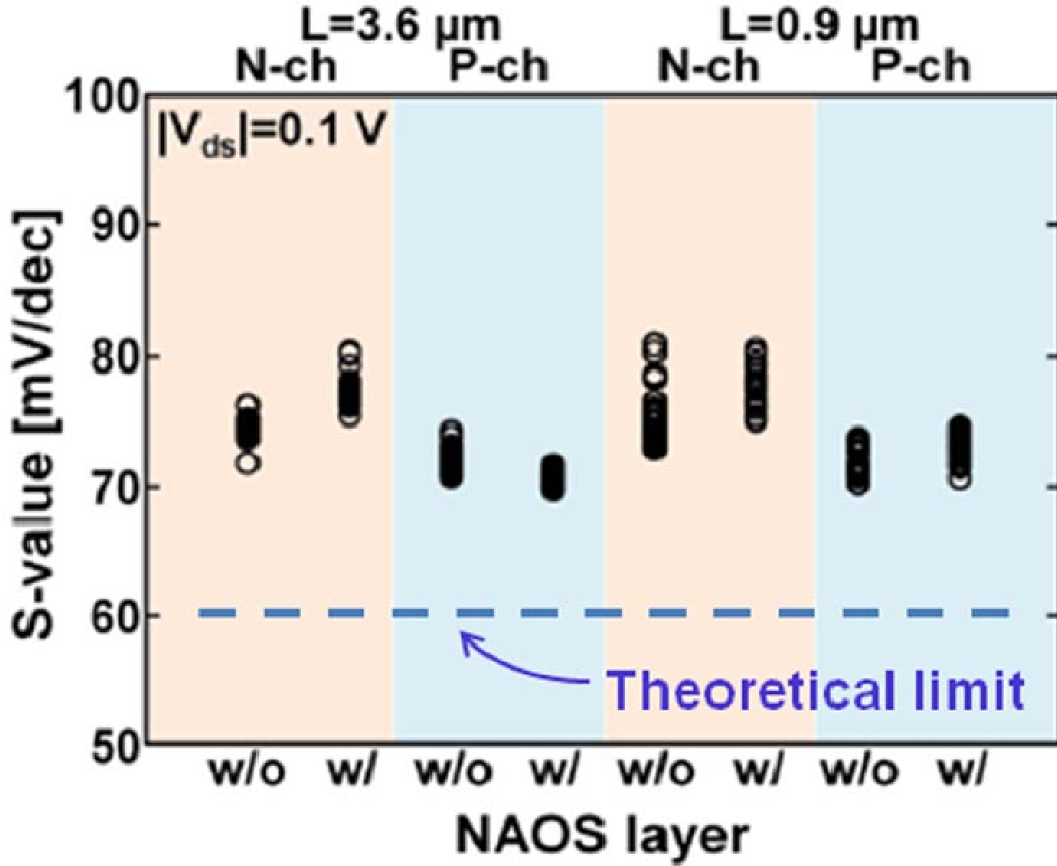

Figure 4-10. *S*-value of the TFTs having the 10 nm CVD SiO_2 gate insulator with (w/) and without (w/o) a NAOS SiO_2 layer.

where ε_{Si} is a relative dielectric constant of Si, q is the elementary electric charge, N_A is the donor (or accepter) density, Ψ_B is the surface potential, k is the Boltzmann constant, T is the absolute temperature, and n is given by

$$n = \frac{C_{OX} + C_d + C_{it}}{C_{OX}} \tag{4-4}$$

where C_{ox} is the gate insulator capacitance, C_d is the Si depletion capacitance, and C_{it} is the capacitance due to interface states [65]. Using these equations, the *S*-value at room temperature (300 K) is given by

$$S = \left[\frac{\partial(\log I_d)}{\partial V_{gs}}\right]^{-1} = \frac{nkT}{q\log e} \approx 0.06n \qquad [\mathrm{V}] \tag{4-5}$$

Using Equations (4-3) to (4-5) and assuming that C_d is much lower than C_{it}

because of the non-doped poly-Si layer, the interface state densities (D_{it}) for the N-ch and P-ch TFTs were calculated to be 5.5×10^{11} and 3.3×10^{11} /cm^{2}eV, respectively. These interface state densities are considerably low for the poly-Si TFTs fabricated with the low temperature process below 500 °C, considering that those for thermal oxide/Si(111) and Si(100) are 1.5×10^{11} and 2.0×10^{10} /cm^{2}eV, respectively (cf. Figure 4-13) [66]. The higher D_{it} for the N-ch TFT than that for the P-ch TFT indicates that D_{it} is higher near the conduction band than near the valence band. These low D_{it} and S-values were ascribed to the thin gate insulator and the high quality NAOS SiO_2/Si interface.

The field-effect mobilities (μ_{FE}) were 100-200 cm^2/Vs for the N-ch TFTs and 80-120 cm^2/Vs for the P-ch TFTs as shown in Figure 4-11. These mobilities were

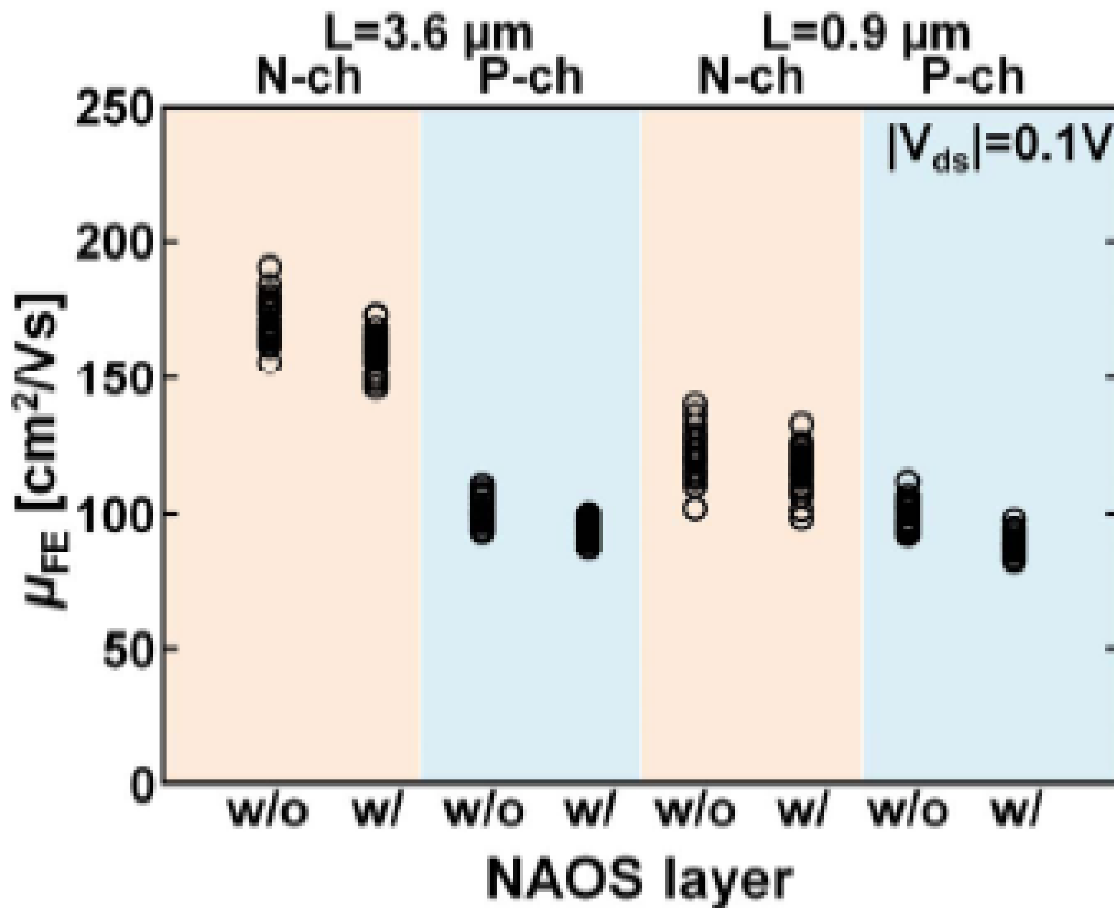

Figure 4-11. Field-effect mobility of the TFTs having the 10 nm CVD SiO_2 gate insulator with (w/) and without (w/o) a NAOS SiO_2 layer.

higher than those of poly-Si TFTs reported in previous literature [20,67], which is attributable to the lower scattering effect by high quality NAOS SiO_2/Si interfaces. The difference in the mobility for the N-ch and P-ch TFTs is most probably due to the difference in the hole (450 cm^2/Vs) and electron (1500 cm^2/Vs) intrinsic mobility of bulk Si [56].

The V_{th} was 0.2~0.4 V for the N-ch TFTs and –0.4~–0.5 V for the P-ch TFTs as shown in Figure 4-12. For achieving such low threshold voltages, the following requirements should be satisfied: 1) capacitance of an SiO_2 layer much higher than that of the poly-Si layer, 2) low interface state density, and 3) low oxide fixed charge density. When requirements 1) and 2) are satisfied, most of the bias voltage is applied to poly-Si, but not to SiO_2, leading to a change in the Si band-bending with

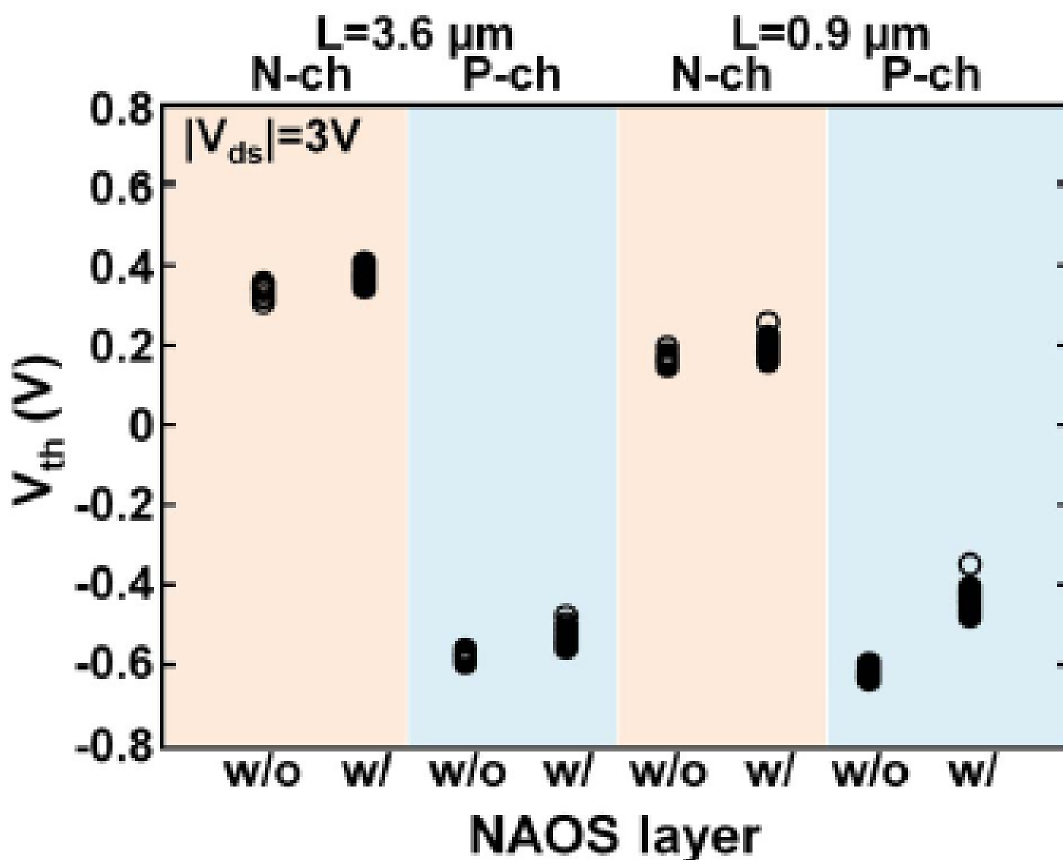

Figure 4-12. Threshold voltage of the TFTs having the 10 nm CVD SiO_2 gate insulator with (w/) and without (w/o) a NAOS layer.

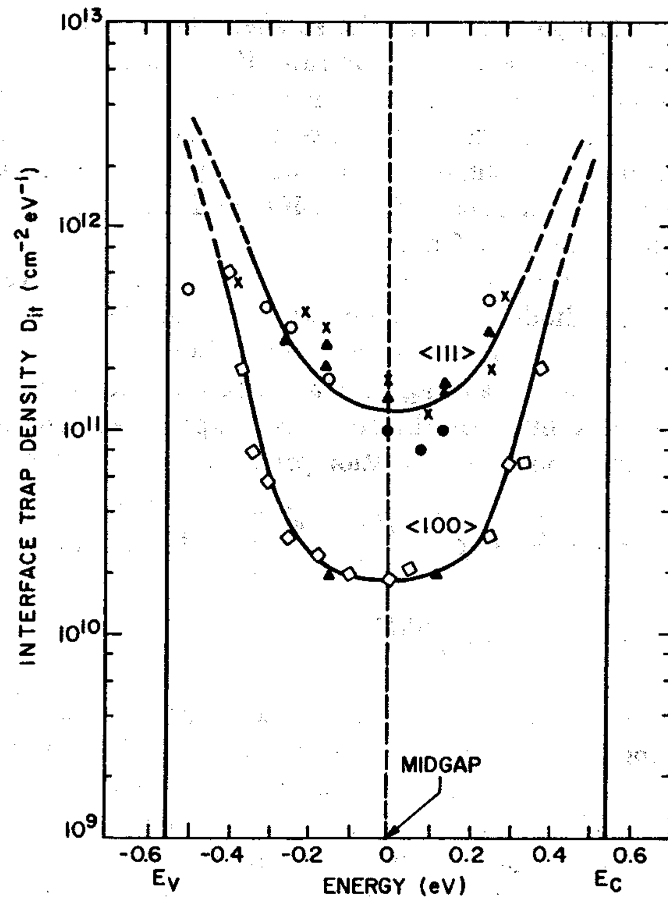

Figure 4-13. The interface state density in thermal SiO_2 on Si substrate [65].

nearly the same magnitude as the gate bias voltage.

The low V_{th} and the low I_{off} were achieved due to the small S-values, leading to the sharp switching characteristics of the TFTs.

As the low gate leakage current for the TFTs with the NAOS SiO_2 layer formed at 120 °C is ascribed to (i) a low interface states densities by direct oxidation of poly-Si surfaces, (ii) a uniform thickness NAOS SiO_2 layer, and (iii) a high atomic density of the NAOS SiO_2 layer resulting in a high band discontinuity energy at the SiO_2/Si interface.

Figures 4-14 to 4-18 show the characteristics of the TFTs with a 1.8 nm NAOS SiO_2/20 nm CVD SiO_2 stacked gate insulator structure with the NAOS SiO_2 layer

formed with 68 wt% HNO_3 at room temperature.

Figure 4-14 shows the I_d- V_{ds} curves for the TFTs with the above stacked gate insulator structure. The I_d- V_{ds} curves possessed ideal features with high saturation currents. The gate lengths for Figures 4-14 a, b, c, and d are 4, 2, 0.9, and 0.6 μm, respectively. The saturation current increased with a decrease in the gate length, and for the TFTs with sub-micrometer gate length, the saturation current was sufficiency high even at the supply voltage of 1.5 V, indicating that the TFTs could be operated at 1.5 V.

Figure 4-15 shows the threshold voltage, V_{th}, of the TFTs with the 1.8 nm NAOS SiO_2/20 nm CVD SiO_2 stacked gate insulator structure. V_{th} for both the P-ch (Figure 4-15 a) and N-ch (Figure 4-15 b) TFTs didn't strongly depend on the gate length and it was approximately −0.6 and 0.6 V, respectively. These low threshold voltages made it possible to operate the TFTs at the low voltage. No short-channeling effect [68,69] was observed even in the sub-micrometer gate length region by use of the thin gate insulator [70].

Figure 4-16 shows the I_d- V_{gs} curves for the TFTs with the stacked gate insulator structure. The drain-source voltage was 0.1 V for each curve. The drain current largely changed with the gate voltages in the regions between −1 and 0 V for the P-ch TFT and between 0 and 1 V for the N-ch TFT. The sharp features of the I_d- V_{gs} curves indicated low *S*-values as shown below. I_d in the positive gate voltage region for the P-ch TFT and the negative gate voltage region for the N-ch TFT, i.e., I_{off}, was 10^{-13}~10^{-14} A, i.e., as low as the noise level, demonstrating that the 1.8 nm NAOS SiO_2 layer effectively blocked the gate leakage current. The on/off current ratios for the P-ch and N-ch TFTs were both ~10^9 (cf. the on/off ratio for conventional poly-Si TFTs: ~10^7).

Figure 4-17 shows the *S*-value for the TFTs with the stacked gate insulator structure. The *S*-values for both the P-ch and N-ch TFTs were ~80 mV/dec in cases where the gate length was larger than 1.0 μm.

Figure 4-18 shows the field-effect mobility vs. the gate length for the TFTs with the stacked gate insulator structure. The mobilities of the P-ch and N-ch TFTs were approximately 100 and 200 cm^2/Vs, respectively, which could be considered to be sufficiently high for poly-Si-based TFTs. The slight decrease of mobility for the sub-micrometer TFTs with ~0.8 μm gate length is most probably due to dispersion

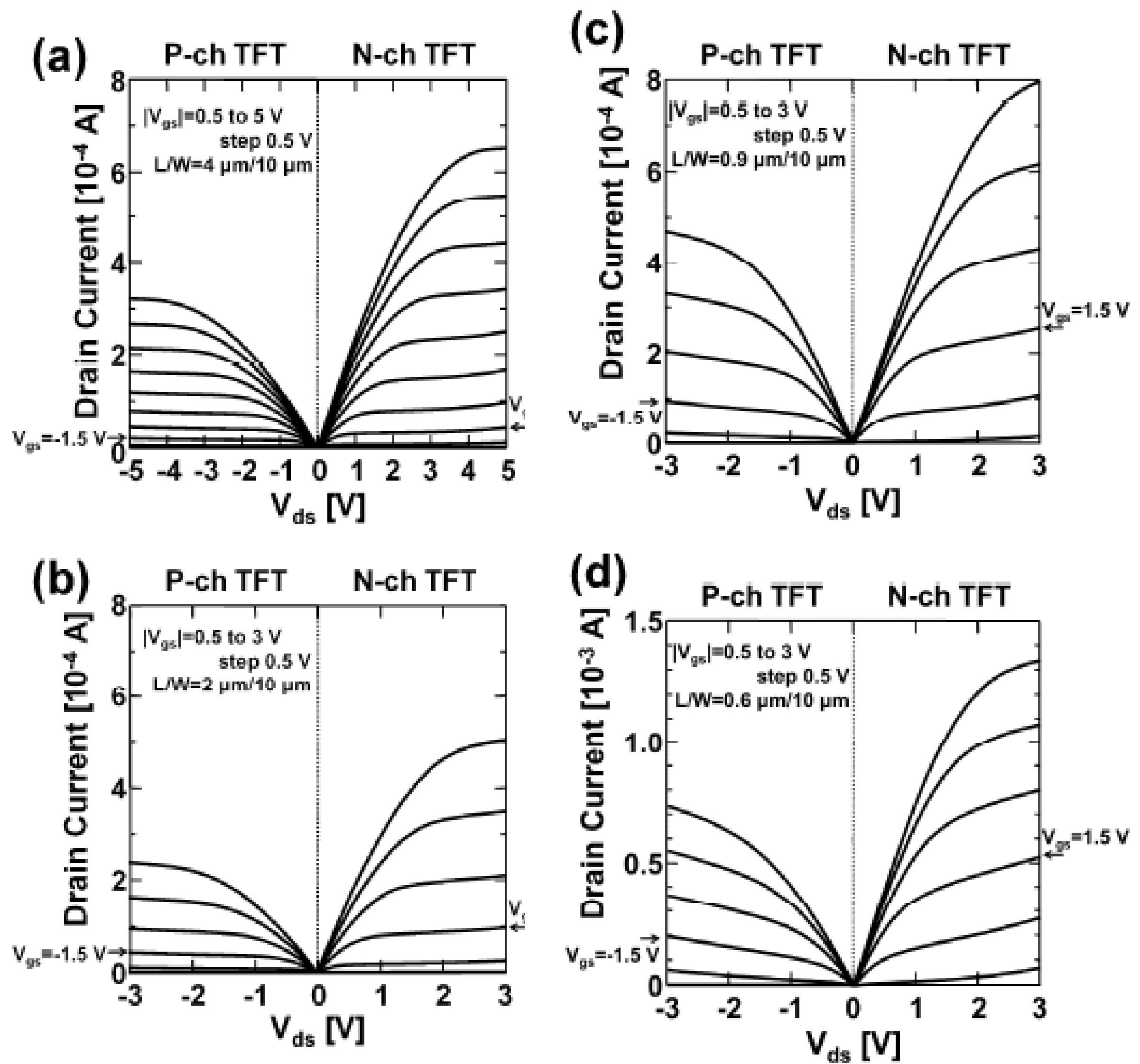

Figure 4-14. I_d- V_{ds} curves for the P-ch (left) and N-ch (right) TFTs with the 1.8 nm NAOS SiO_2/20 nm CVD SiO_2 stacked gate insulator structure having following gate length: (a) 4 μm; (b) 2 μm; (c) 0.9 μm; (d) 0.6μm.

because the size of a single grain in poly-Si is close to the channel length.

Figures 4-19 and 4-20 and Table 4-1 show the characteristics of the TFTs with a 1.8 nm NAOS SiO_2/40 nm CVD SiO_2 stacked gate insulator structure with the NAOS SiO_2 formed with 68 wt% HNO_3 at room temperature. The 40 nm-thick CVD SiO_2 layer was used in these TFTs in order to secure a large margin for proper operation of the large-scale circuits (cf. Section V).

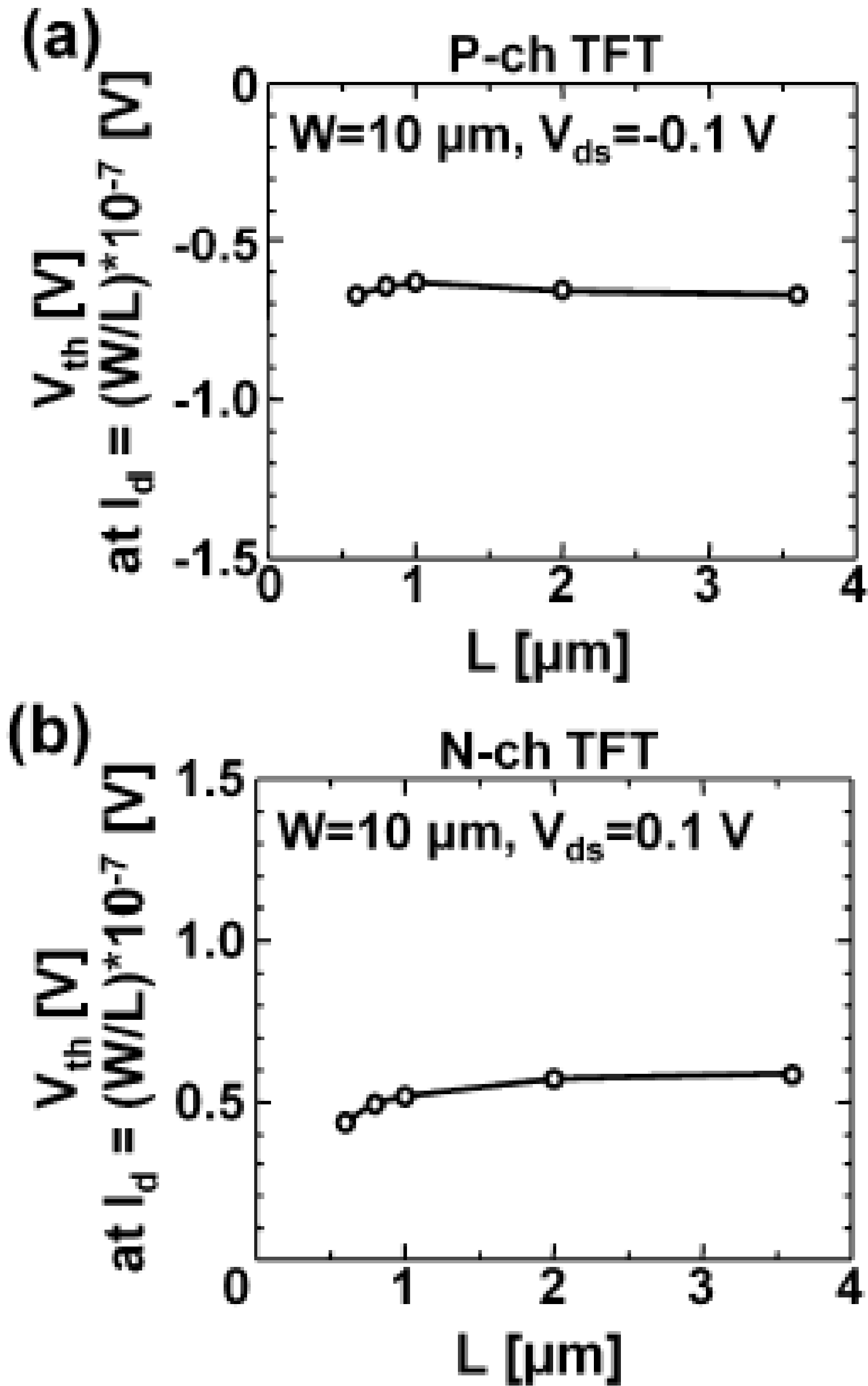

Figure 4-15. Threshold voltage vs. the gate length for the TFTs with the 1.8 nm NAOS SiO_2/20 nm CVD SiO_2 stacked gate insulator structure: (a) P-ch TFT; (b) N-ch TFT.

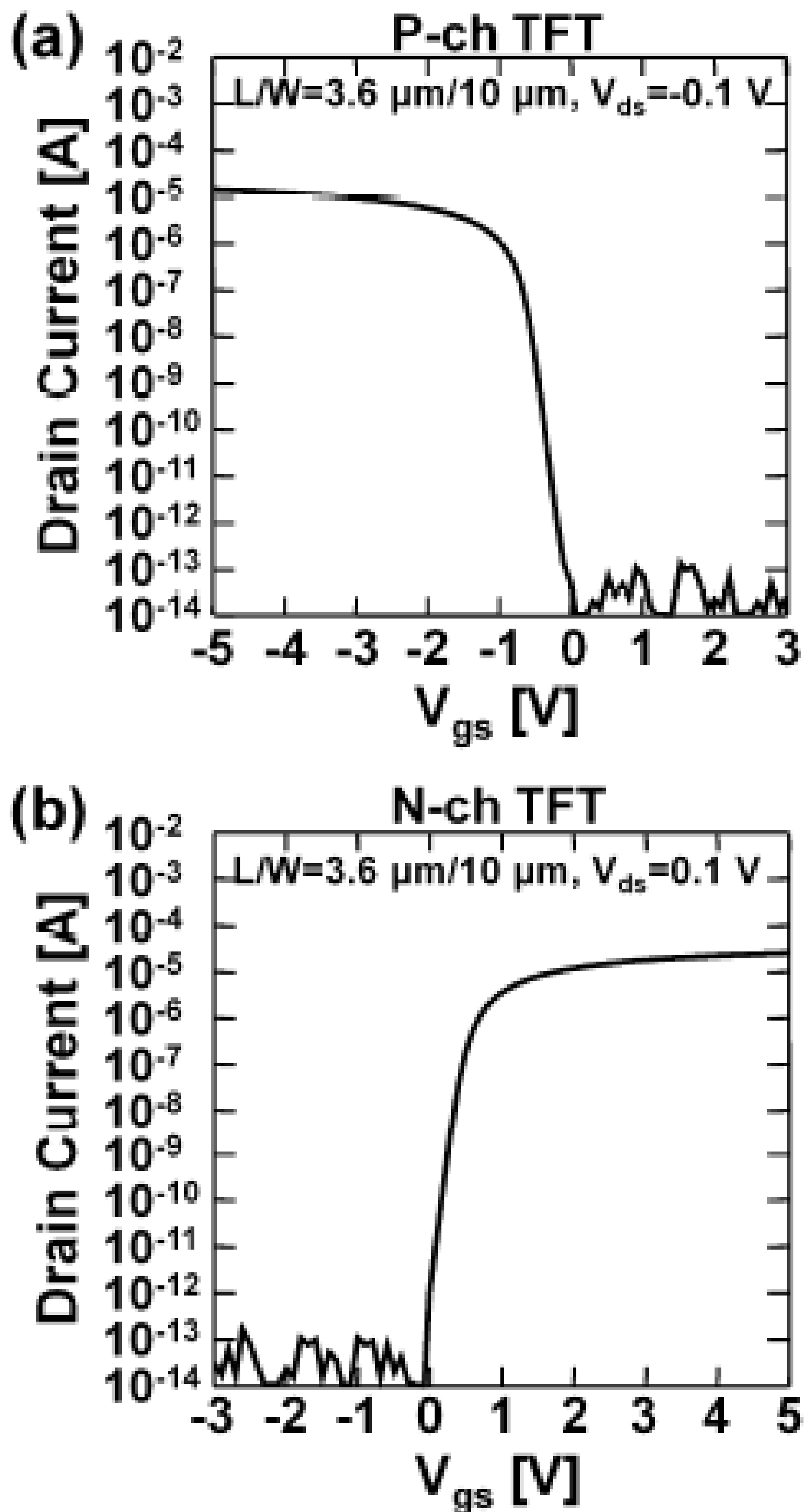

Figure 4-16. I_d- V_{gs} curves for the TFTs with the 1.8 nm NAOS SiO_2/20 nm CVD SiO_2 stacked gate insulator structure: (a) P-ch TFT; (b) N-ch TFT.

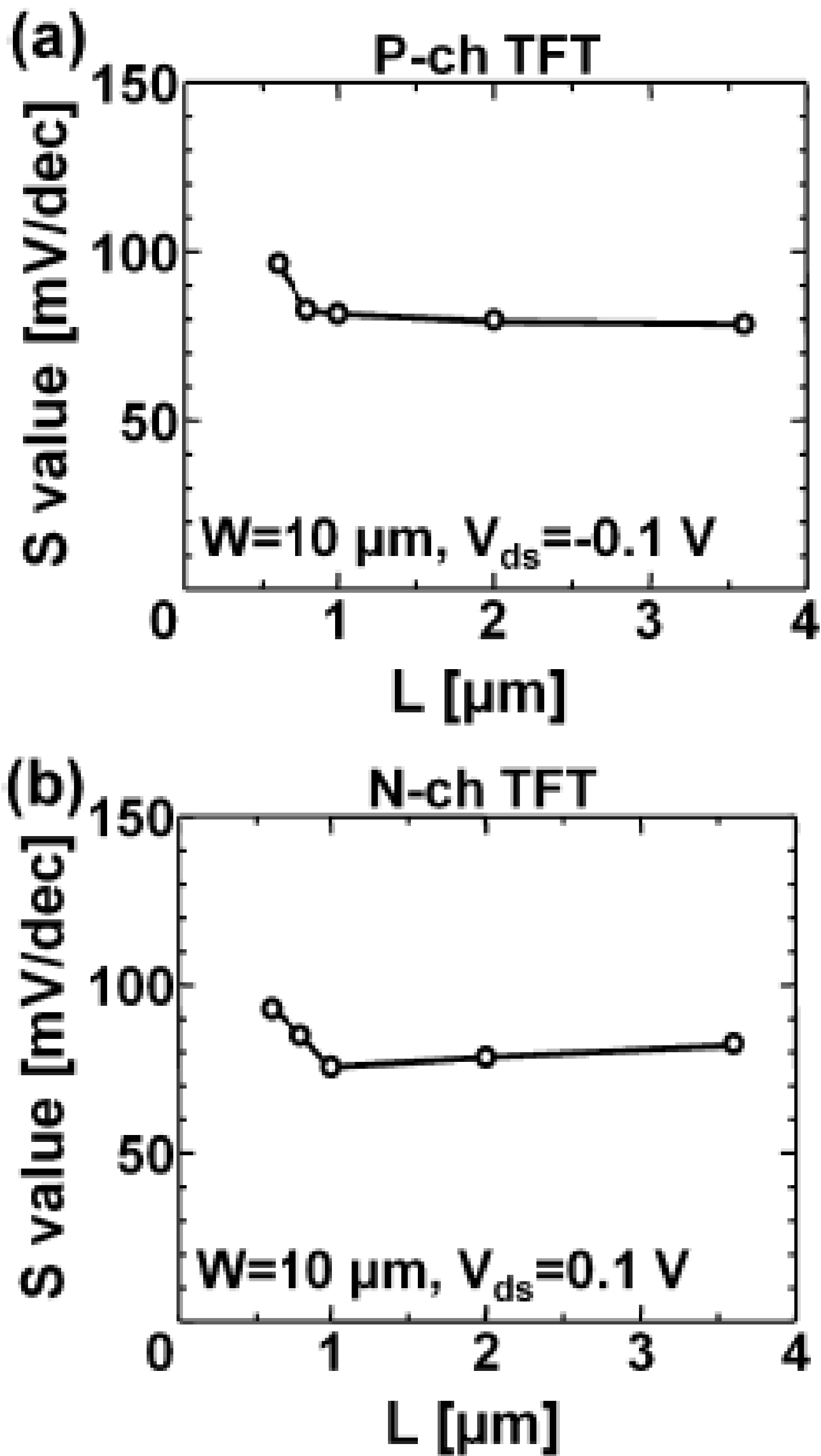

Figure 4-17. *S*-value vs. the gate length for the TFTs with the 1.8 nm NAOS SiO_2/20 nm CVD SiO_2 stacked gate insulator structure: (a) P-ch TFT; (b) N-ch TFT.

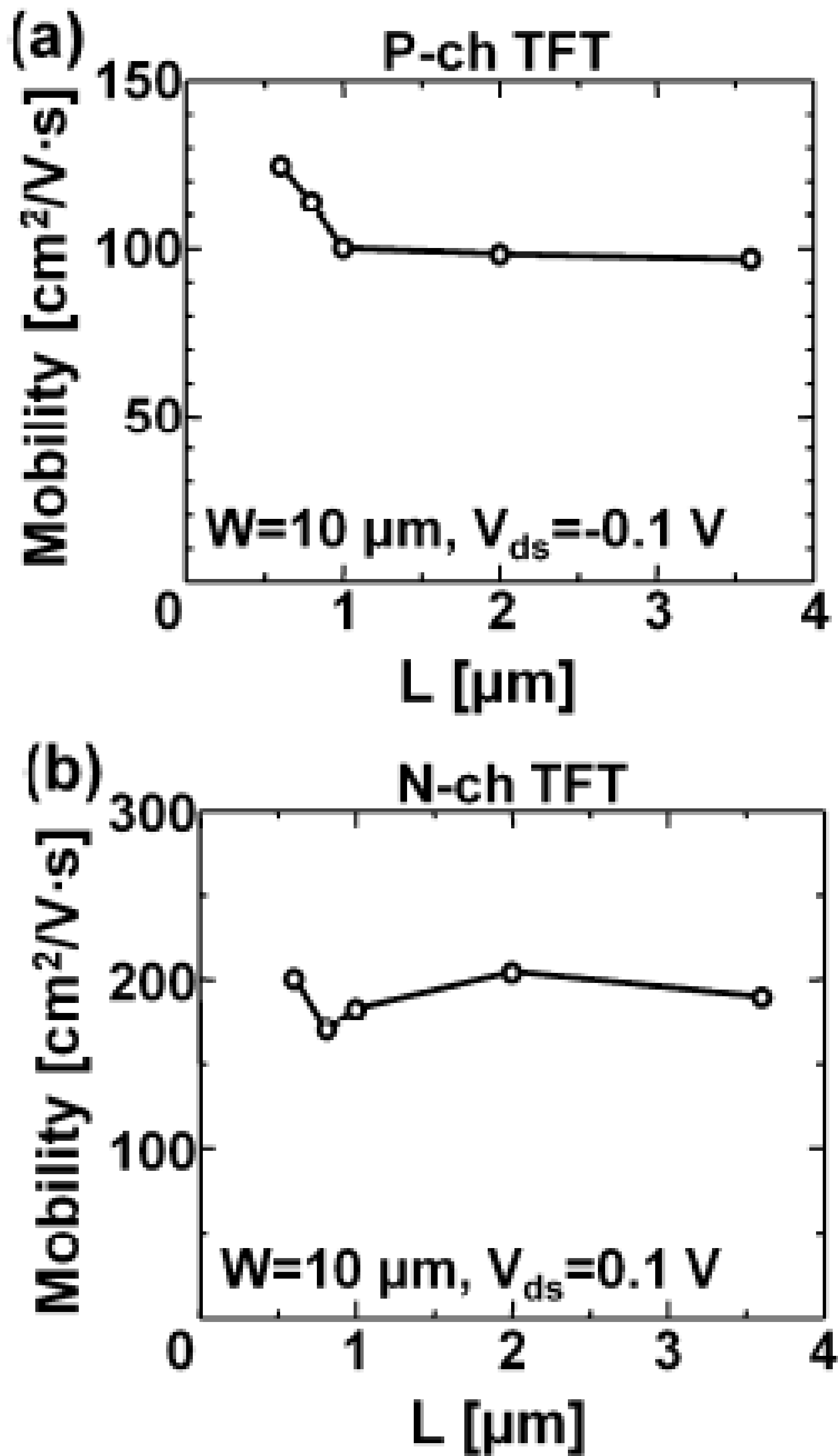

Figure 4-18. Field-effect mobility vs. the gate length for the TFTs with the 1.8 nm NAOS SiO_2/20 nm CVD SiO_2 stacked gate insulator structure: (a) P-ch TFT; (b) N-ch TFT.

Figure 4-19 shows the I_d- V_{gs} curves for the TFTs with the above stacked gate insulator structure. The gate lengths for Figures 4-19 a, b, and c are 3.5, 8, and 12 μm, respectively. The drain-source voltage was 0.1 V for each curve. Figure 4-20 shows the I_d- V_{ds} curves for the TFTs with the above stacked gate insulator structure. The gate length for Figures 4-20 a, b, and c, is 3.5, 8, and 12 μm, respectively. The I_d- V_{ds} curves were measured for various gate-source voltages between 0.5 and 5.0 V.

Table 1 shows the obtained electrical characteristics for the fabricated TFTs, i.e., threshold voltage (V_{th}), effective mobility (μ_{eff}), sub-threshold coefficient (S), and on/off ratio. Table 1 displays electrical characteristics of the fabricated TFTs obtained from averaging the values for 25 TFTs. The μ_{eff} estimated from linear extrapolation of the I_d- V_{gs} curves were 170~208 cm^2/Vs for the N-ch TFTs and 70~78 cm^2/Vs for the P-ch TFTs both with L=3.5 μm. The threshold voltage was 0.55~0.81 V for the N-ch TFTs and –1.23~–1.46 V for the P-ch TFTs both with L=3.5 μm. The S-values were 90~110 mV/dec. and 75~90 mV/dec. for the N-ch and P-ch TFTs both with L=3.5 μm, respectively. Using Equations (4-3) to (4-5), the interface state densities (D_{it}) for the N-ch and P-ch TFTs are calculated to be 3.2×10^{11} and 1.8×10^{11} /cm^{2}eV, respectively. The dispersion was found to be sufficient small to enable 1.5 V operation of the circuits.

Since a leakage current flows through the gate SiO_2 layer in thin regions and/or via defect states such as interface states and foreign species in SiO_2, a thick gate oxide layer in the range between 80 and 150 nm is needed to achieve a sufficiently low leakage current for commercial TFTs. The thick gate oxide layer seriously increases the threshold voltage and the TFT operation voltage. Since TFT power consumption, P, is proportional to the square of the operation voltage, V, (conventional TFT operation voltage: 12~15 V vs. commercial LSI operation voltage: 1.2~1.5 V), the thick gate oxide layer drastically increases TFT power consumption. Moreover, the thick gate oxide layer makes it difficult to miniaturize TFTs.

The above argument indicates that a decrease in the gate oxide thickness is indispensable for a vast decrease in the TFT power consumption and also for miniaturization [8]. Since the ultra-thin NAOS SiO_2 layer with a low leakage current is intervened between the poly-Si thin film and the CVD SiO_2 layer, the total

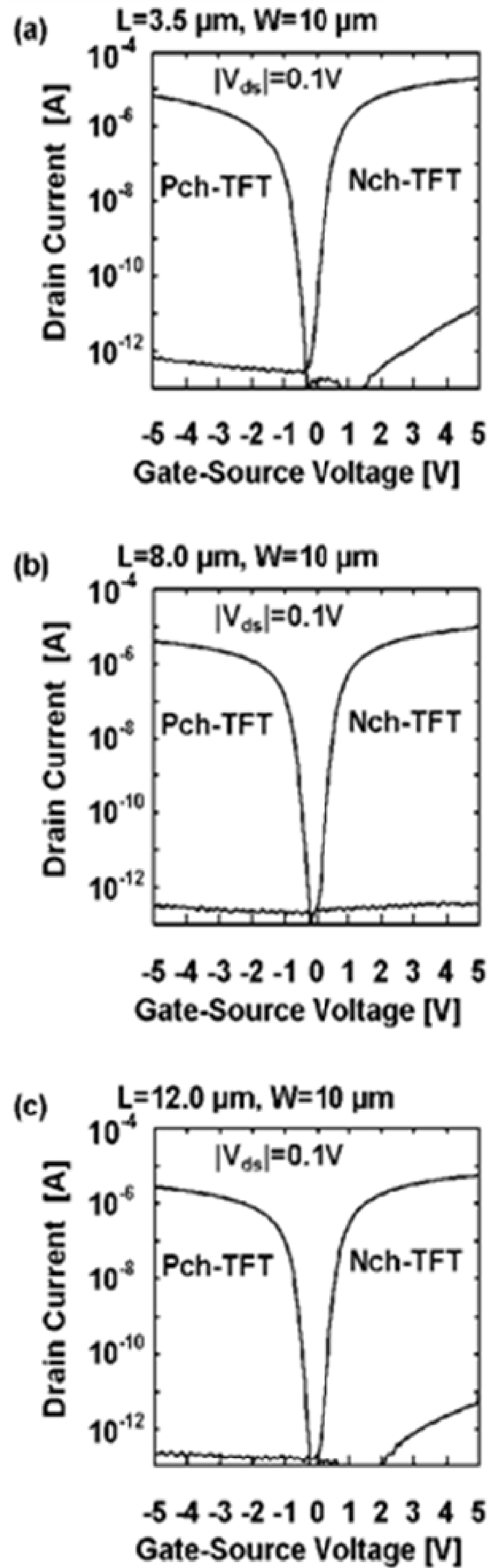

Figure 4-19. I_d- V_{gs} curves for the P-ch and N-ch TFTs with the 1.8 nm NAOS SiO_2/40 nm PE-CVD SiO_2 stacked gate insulator structure. The gate lengths of the TFTs are (a) 3.5, (b) 8, and (c) 12 μm.

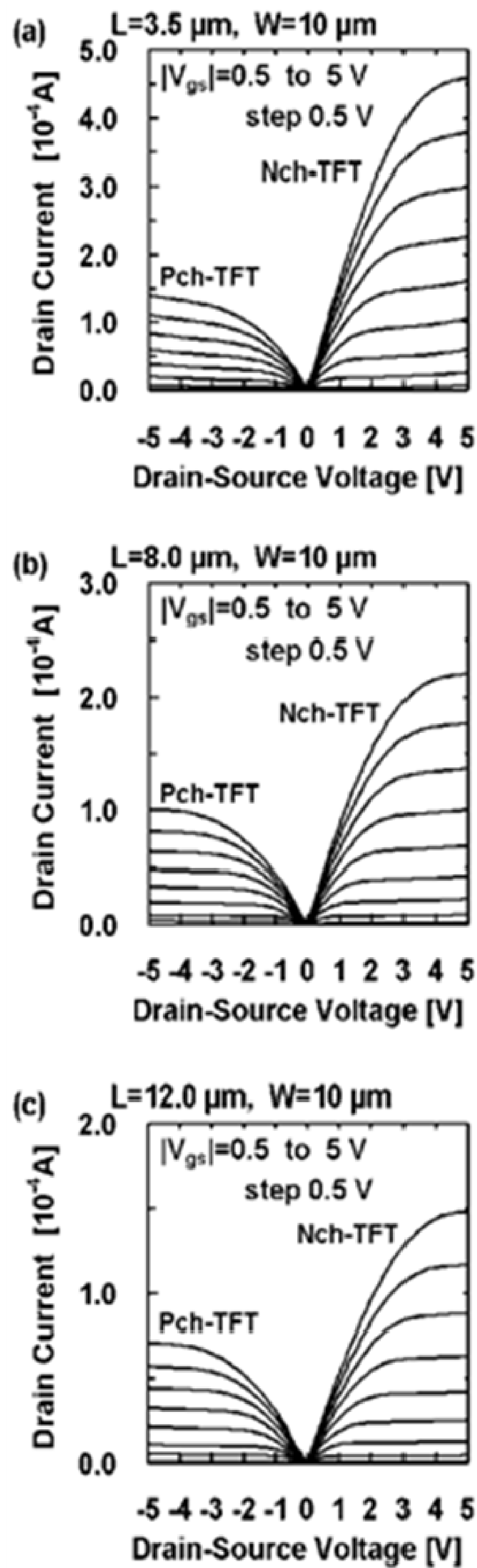

Figure 4-20. I_d- V_{ds} curves for the P-ch and N-ch TFTs with the 1.8 nm NAOS SiO_2/40 nm PE-CVD SiO_2 stacked gate insulator structure. The gate lengths of the TFTs are (a) 3.5, (b) 8, and (c) 12 μm.

n-ch

L[um]	μ_{eff} [cm²/Vs]	Vth [V]	S [mV/dec]	on/off
3.5	186	0.64	106	3.7×10^7
8	213	0.74	93	3.2×10^7
12	200	0.79	95	2.8×10^7

p-ch

L[um]	μ_{eff} [cm²/Vs]	Vth [V]	S [mV/dec]	on/off
3.5	75	-1.37	88	4.4×10^7
8	99	-0.98	77	1.6×10^7
12	99	-0.97	82	3.0×10^7

Table 4-1. Electrical characteristics of the N-ch and P-ch TFTs fabricated with the NAOS SiO_2/PE-CVD SiO_2 stacked gate insulator structure and various channel lengths (L).

oxide thickness could be reduced due to blocking the leakage current by the interfacial oxide layer. Consequently, the high μ_{eff} and the low V_{th} of the TFTs with the stacked gate insulator enable low voltage and high frequency operation of the electrical circuits, and the small S-value and the large on/off ratio make stable operation possible (cf. Section V).

As shown in Equation (1-1), the power consumed by TFTs is proportional to the square of the operation voltage, and therefore, the consumed power is expected to decrease to $(1.5/15)^2 \approx 1/100$ of currently commercially available TFTs with the operation voltage of 15 V. The consumed power can be further decreased by miniaturization of TFTs, which leads to a reduction in capacitive load.

IV – 3. Summary

I have fabricated poly-Si TFTs with the NAOS SiO_2/CVD SiO_2 stacked gate insulator structure on glass substrates. Measurements of I_d- V_{gs} and I_d- V_{ds} curves lead to the following results and conclusion:

1) For the poly-Si TFTs with 1.4 nm NAOS SiO_2/10 nm CVD SiO_2 stacked gate insulator, the I_d- V_{ds} curves show saturated behavior, and the saturation current is high enough for switching function even at the low operation voltage of 1.0 V.
2) The threshold voltages are lower than 0.5 V for both of the N-ch and P-ch TFTs.
3) The off-current is as low as the noise level (i.e., 10^{-13}~10^{-14} A), leading to the high on/off ratio of 10^9.
4) The S-values for both the N-ch and P-ch TFTs are as low as 65~80 mV/dec.
5) The interface state densities estimated from the S-values are 5.5×10^{11} /cm^{2}eV for the N-ch TFTs and 3.3×10^{11} /cm^{2}eV for the P-ch TFTs.
6) The field-effect mobility is ~200 cm^2/Vs for the N-ch TFTs and ~100 cm^2/Vs for the P-ch TFTs.
7) A short channel effect does not occur even for the TFTs with sub-micrometer gate length.

The excellent TFT characteristics, such as the high carrier mobility, low V_{th}, and small S-value, are attributable to 1) thin gate oxide thickness, 2) low interface state density, and 3) low oxide fixed charge density, all resulting from excellent electrical characteristics of the ultra-thin NAOS SiO_2 layer intervened between the poly-Si thin film and the CVD SiO_2 layer. These poly-Si TFTs are expected to operate electrical circuits at 1.5 V, leading to decreasing the power consumption to ~1/100 of that of conventional TFTs operated at 15 V.

V. Performance of Poly-Si TFT Circuits

V - 1. Ring Oscillators

A ring oscillator is composed of plural stages of CMOS inverters connected in series (cf. Figure 5-1), and is useful for evaluating dynamic characteristics of transistors. I have fabricated several ring oscillators composed of the poly-Si TFTs described in Figures 4-19 and 4-20, and the fundamental circuit performance was evaluated. The performance of the ring oscillators was characterized by measurements of their oscillating frequency and consumed current at various supply voltages.

The fabricated ring oscillators were composed of 19 and 37 stages of CMOS inverters, accompanied with additional buffering inverters with which the operating

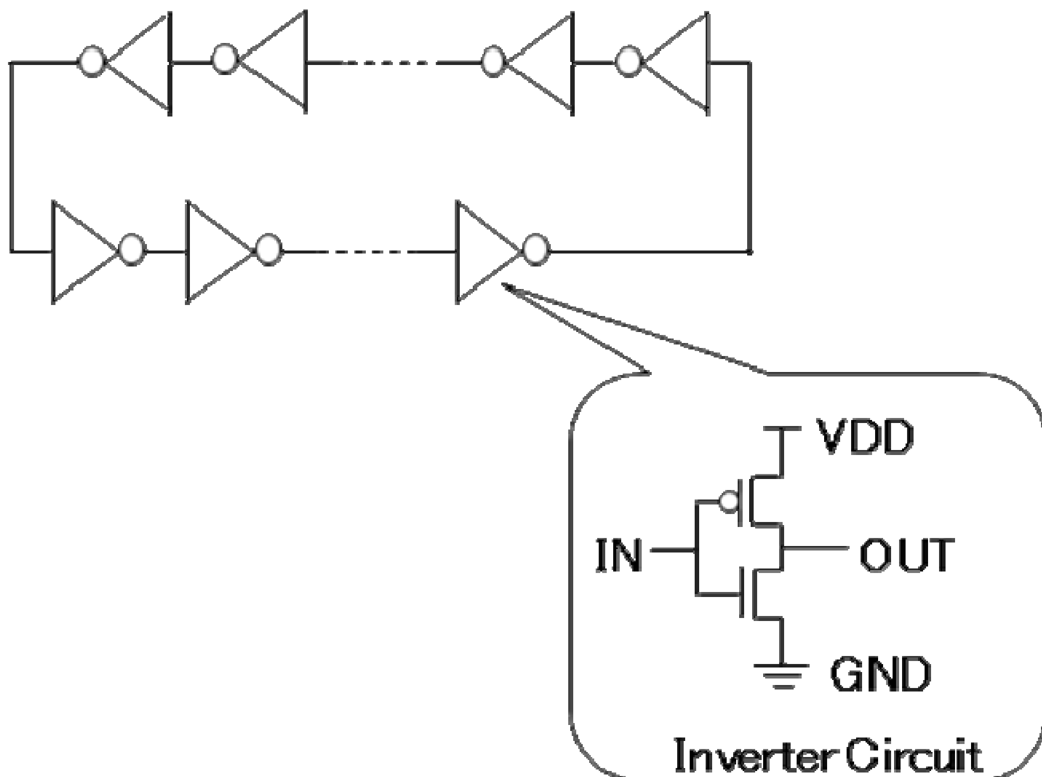

Figure 5-1. Schematic of the ring oscillator composed of 19 or 37 stages of CMOS inverters.

signal could be measured. The gate length (L) and the gate width (W) of the TFTs composing the ring oscillators were 3.5 and 10.0 μm, respectively.

Figure 5-2 shows the waveform of the ring oscillator with 37 stages of inverters at 3.0 V supply voltage. The waveform was observed at the output of the buffering circuit with a negligibly small load which did not influence the behavior of the ring oscillator. The period of the signal wave was 290 ns, corresponding to the oscillating frequency of 3.45 MHz.

Figure 5-3 shows the measured oscillating frequency vs. the supply voltage (V_{DD}) for the ring oscillators composed of (a) 19 and (b) 37 inverters with the TFTs of L=3.5 μm. It was found that the oscillating frequency was almost linearly dependent on the supply voltage with the offset of ~1 V. The delay time per one inverter is calculated to be 16.2~17.4 and 3.9~4.0 ns at V_{DD}=1.5 and 3.0 V, respectively. Here, the delay time is defined as the average value of the rise time

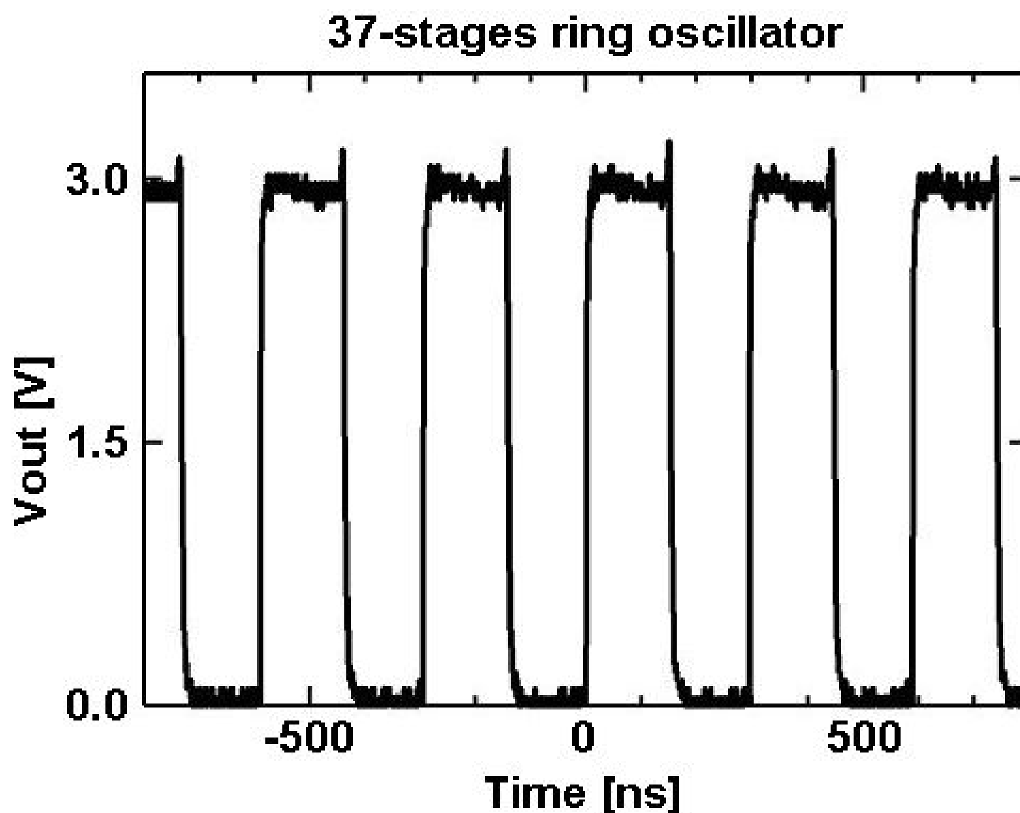

Figure 5-2. Waveform of the ring oscillator with 37 stages of inverters. The period of the waveform corresponds to the inverter delay time multiplied by twice of the number of the inverter stages.

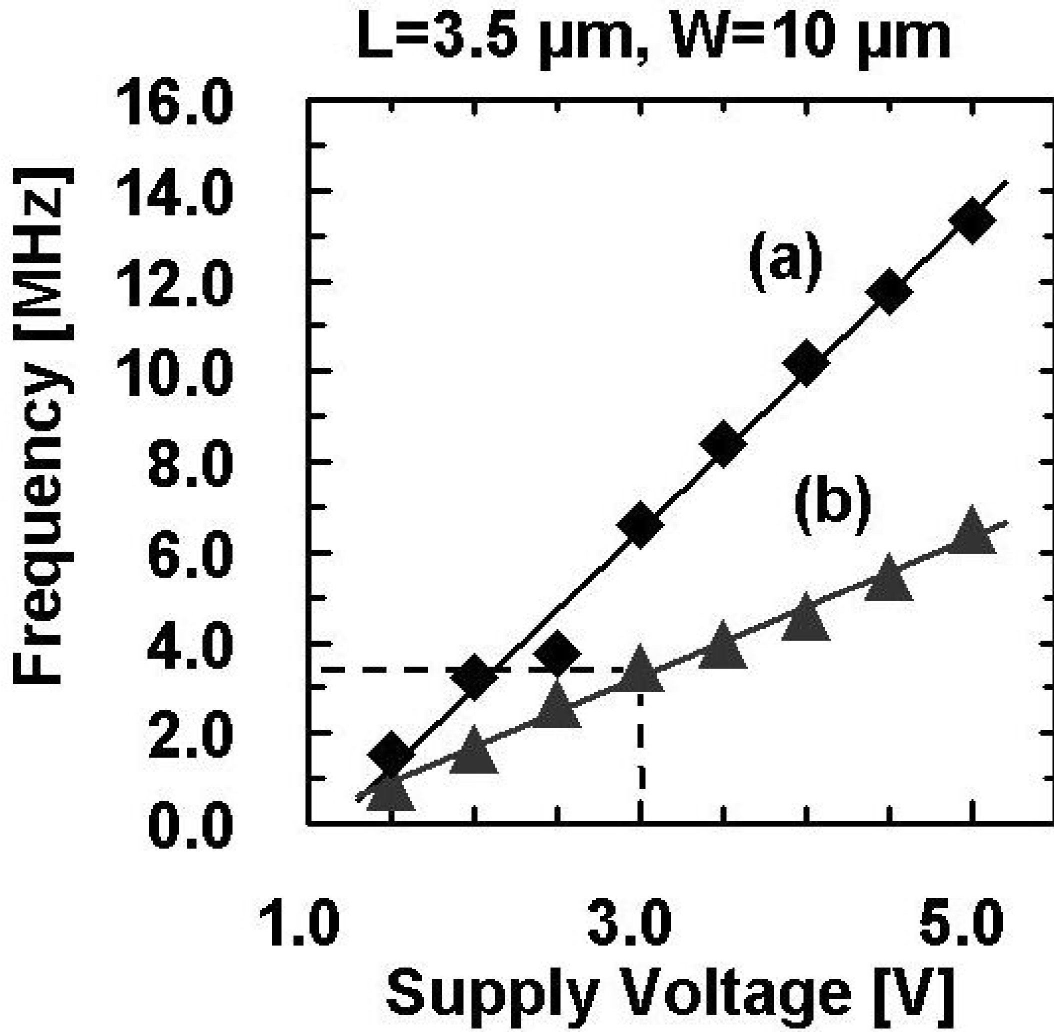

Figure 5-3. Oscillating frequency of the ring oscillators of (a) 19 stages and (b) 37 stages of inverters vs. the supply voltage. L and W are 3.5 and 10.0 μm, respectively, and the thickness of the CVD SiO_2 layer is 40 nm.

and the fall time, which correspond to the delay time of P-ch TFT and N-ch TFT, respectively.

The delay time t of an inverter can be theoretically calculated using the following equation [71,72],

$$t = \left[\frac{|V_{th}|/V_{DD} + \alpha}{1+\alpha} - \frac{1}{2} \right] t_T + \frac{C_L V_{DD}}{2 I_{DO}} \tag{5-1}$$

where

$$t_T = \frac{C_L V_{DD}}{I_{DO}} \left[\frac{0.9}{0.8} + \frac{V_{DO}}{0.8V_{DD}} \ln \frac{10V_{DO}}{\mathrm{e}V_{DD}} \right] \quad (5\text{-}2)$$

$$V_{DO} = V_{DD} - |V_{th}| \quad (5\text{-}3)$$

$$I_{DO} = \frac{1}{2} \frac{W}{L} \frac{\varepsilon_{OX}}{T_{OX}} \mu_{eff} \left(V_{DD} - |V_{th}| \right)^2 \quad (5\text{-}4)$$

$$C_L = 2LW \frac{\varepsilon_{OX}}{T_{OX}} \quad (5\text{-}5)$$

where e is the base of natural logarithm (i.e., 2.71• • •), α takes 2.0 under the Shockley model, ε_{ox} is the dielectric constant of SiO_2, T_{ox} is the thickness of the gate insulating layer, and μ_{eff} is the effective mobility of TFTs, and C_L is the load capacitance of each inverter. In this case, C_L is almost the same as the sum of the gate capacitance of the N-ch and P-ch TFTs of the next stage inverter, because of a negligibly low parasitic capacitance for the wiring on the glass substrate. From Equations (5-1) to (5-5), the oscillating frequency, f, which is inversely proportional to the delay time of the inverter, is expressed as

$$f = \frac{1}{s(t_n + t_p)} \quad (5\text{-}6)$$

where s is the number of the inverter stages in a ring oscillator, t_n is the falling delay time by N-ch TFT, and t_p is the rising delay time by P-ch TFT. Using Equation (5-6), the oscillating frequency was calculated to be 3.10 MHz for 37 stage ring oscillator at 3.0 V supply voltage, in good agreement with the measured value of 3.45 MHz as shown in Figure 5-3.

Figure 5-4 shows the consumed current vs. V_{DD} for the ring oscillators composed of (a) 19 and (b) 37 inverters with the TFTs of L=3.5 μm. It was found that the consumed current monotonically increased with the supply voltage. Since the frequency increased with the supply voltage as described above, the consumed current increased as a parabolic function of the supply voltage. The current increase resulted from 1) an increase of the supply voltage, and 2) an increase of the oscillation frequency which was caused by the increase in the supply voltage.

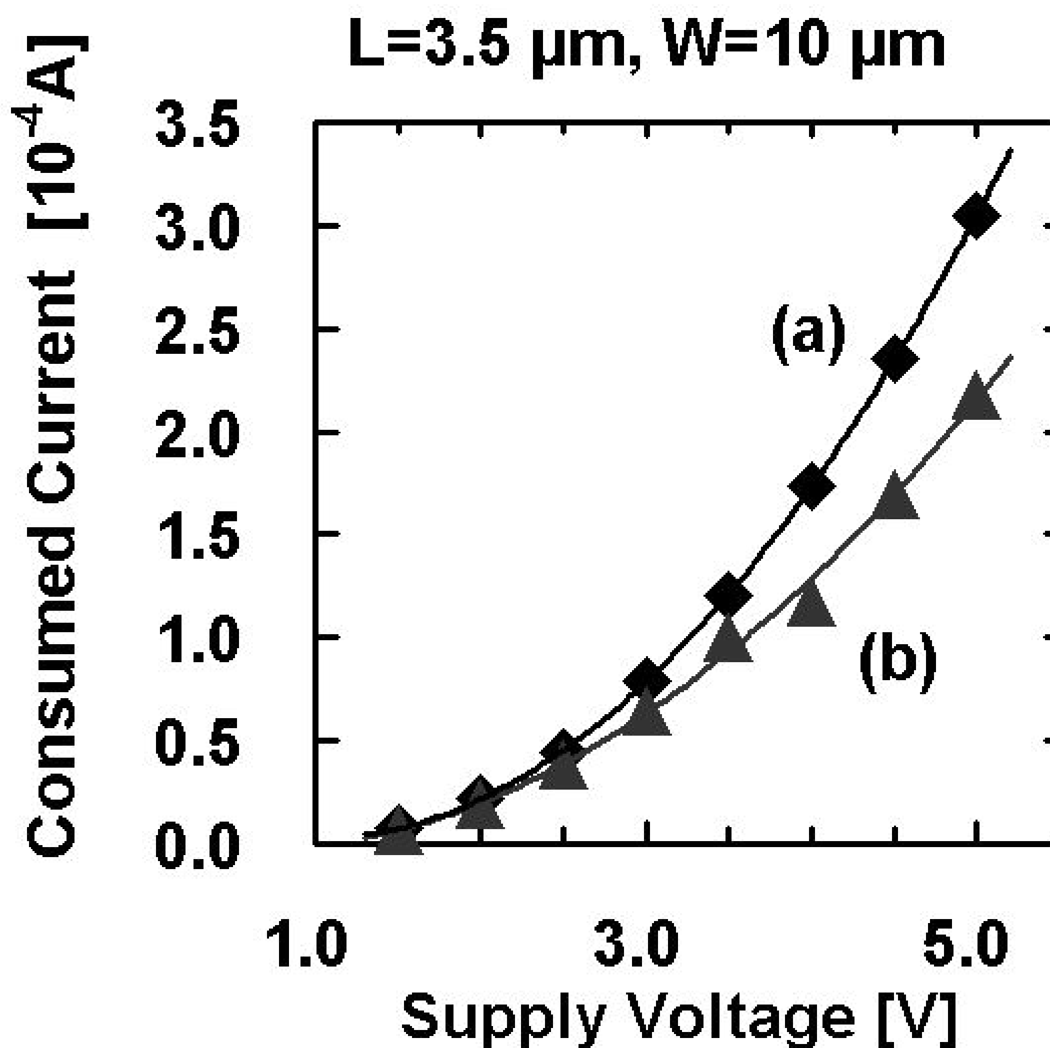

Figure 5-4. Consumed current of the ring oscillators of (a) 19 stages and (b) 37 stages of inverters vs. the supply voltage. L and W are 3.5 and 10.0 μm, respectively, and the thickness of the CVD SiO_2 layer is 40 nm.

V - 2. LCD Driver Circuits

I also designed and fabricated LCDs having monolithic driver circuits with the poly-Si TFTs described in Figures 4-19 and 4-20, and measured their consumed power and the highest frequency at which the circuits could be properly operated.

Figure 5-5 shows the schematic diagram of the LCD manufactured with the NAOS process. Table 5-1 shows the specification of the fabricated LCD. Figure 5-6

shows the photograph of the LCD taken from the backside, and the inset depicts the enlarged photograph of the gate driver circuit implemented in the LCD. The display format is QVGA (320×RGB×240 pixels), and the display size is 2.0 inch diagonal, which have been widely adopted for mobile digital equipments such as cellular phones and digital still cameras. As shown in Figures 5-5 and 5-6, the LCD was composed of three components: 1) a pixel array (active area), 2) a binary data driver located on the bottom side of the pixel array, which outputs the image data to the pixel array, and 3) a gate driver located on the left side of the pixel array, which writes and stores the image data in each pixel of the arrays.

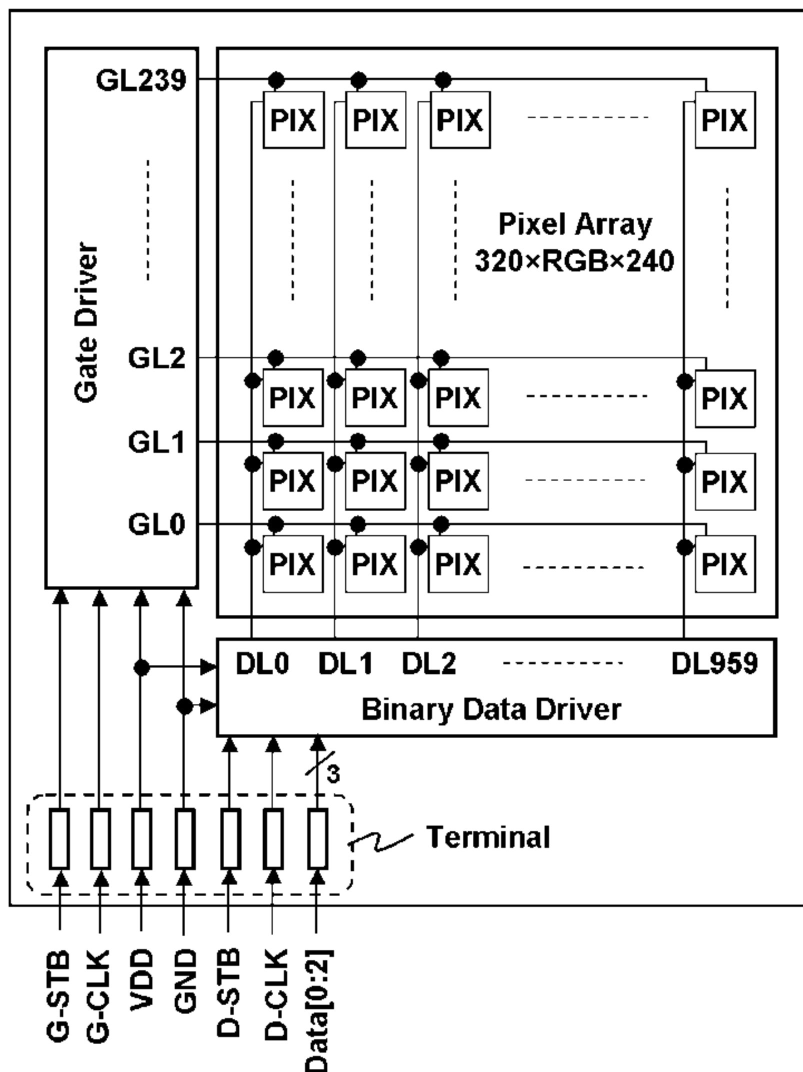

Figure 5-5. Block diagram of the LCD with the monolithic driver circuits. The display is composed of a pixel array, a gate driver, and a binary data driver.

Display Size	2 inch diagonal
Pixel Size	43 μm x 129 μm (200 dpi)
Number of Pixels	320 x RGB x 240
Active Area	41.28 mm (W) x 30.96 mm (H)
Outline Dimension	46.50 mm (W) x 45.00mm (H)
Design Rule	3 μm
Display Mode	Transmissive
Supply Voltage	1.5 V
Operation Frequency	3.0 MHz (Binary Data Driver)
Frame Rate	60 Hz
Power Consumption	100 μW

Table 5-1. Specification of the 2.0 inch-diagonal LCD fabricated by the NAOS process.

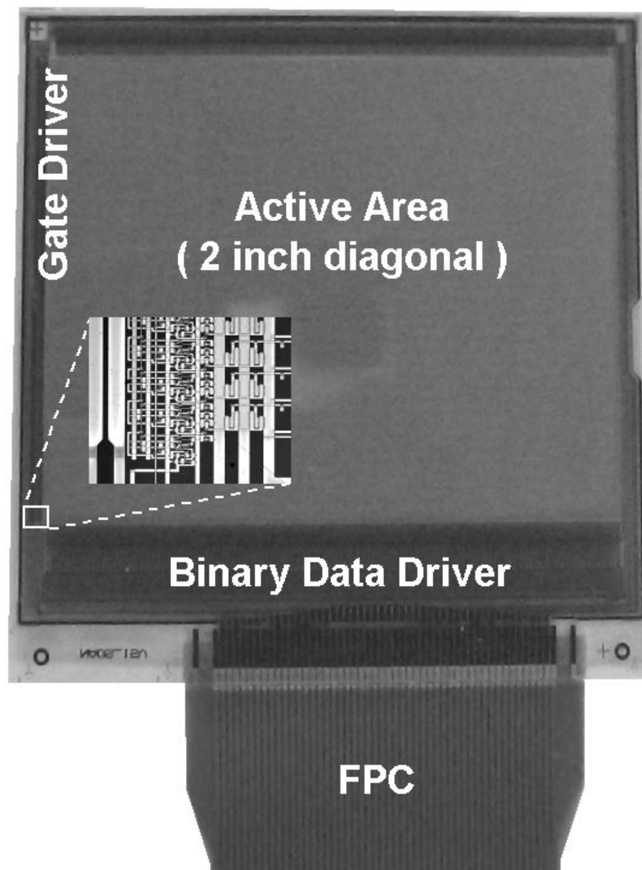

Figure 5-6. Photograph of the fabricated LCD with the monolithic driver circuits on the glass substrate. The inset depicts the enlarged photograph of the gate driver circuit.

The detailed schematic structure of the developed binary data driver is shown in Figure 5-7. The binary data driver was composed of plural sets of the clocked RS-flipflop (RS-FF), the D-latch (LAT), and the buffer circuit (BUF). Each of the serially-connected clocked RS-flipflops, which constructs a shift register, periodically generates the timing signals from the strobe signal (D-STB) and the clock signal (D-CLK). The timing signal samples the image datum (Data [0:2]) at each of the D-latches, and the buffer circuit outputs the image datum to each of the data lines (DL). The image data were written to the pixels (PIX) synchronously with the gate line (GL) signals which were controlled by the gate driver [73,74].

It is noted that the binary data driver includes no analog amplifiers which consume a high current. Therefore, the binary data driver for an LCD enables to reduce the power consumption greatly, which realizes displaying some information anytime on the mobile equipments, although the number of displaying colors is restricted to two or eight.

For general operation at 60 Hz frame frequency, the operation frequency of the binary driver was 3.0 MHz, and the gate driver was operated at 7.5 kHz at that time. I measured the maximum operation frequency of the binary data driver for various supply voltages, and its shmoo-plot is shown in Figure 5-8. The sign “P” in the

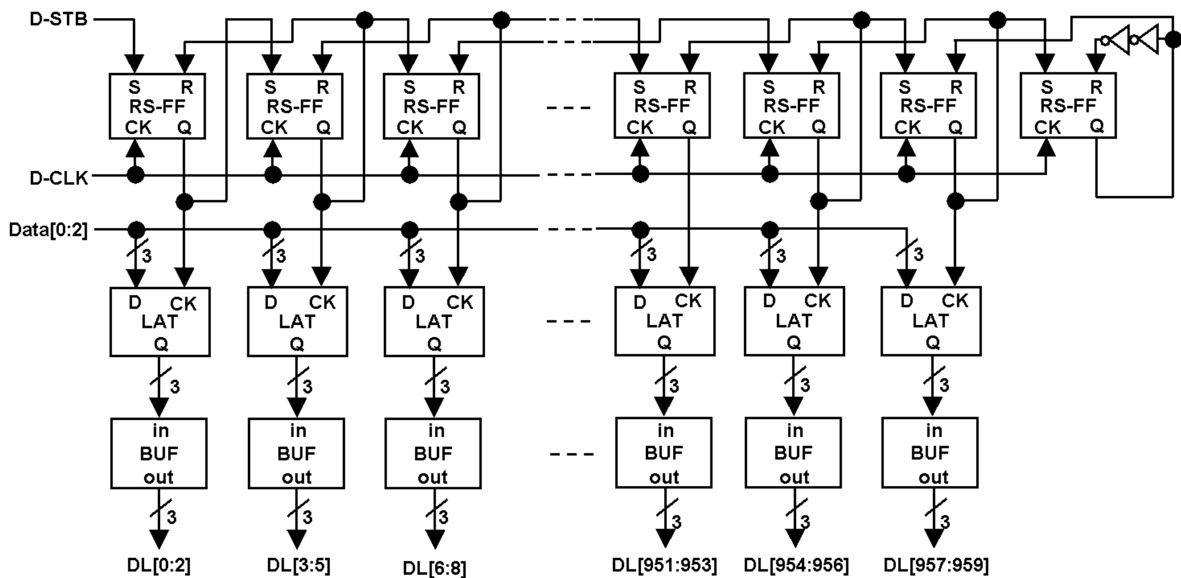

Figure 5-7. Schematic diagram of the binary data driver integrated on the LCD shown in Figures 5-5 and 5-6.

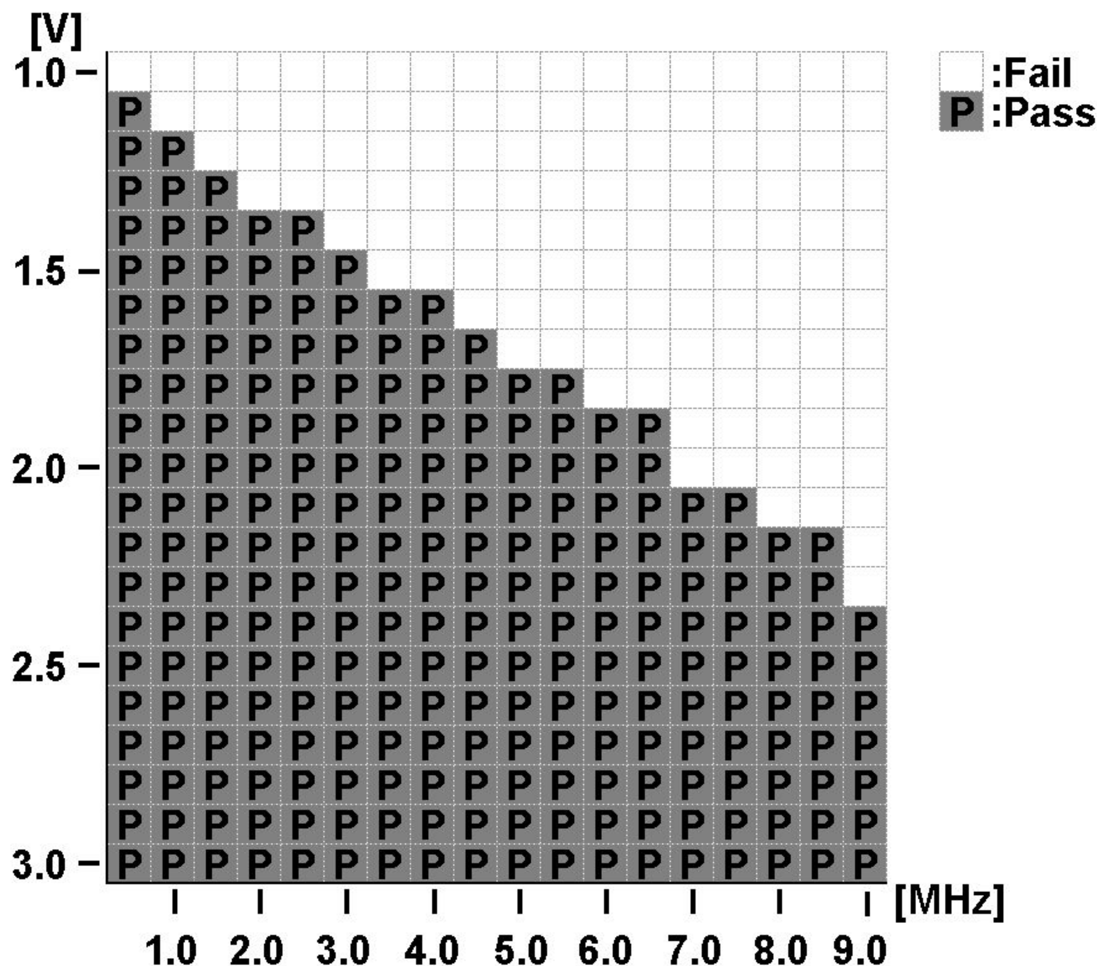

Figure 5-8. Shmoo-plot of the binary data driver circuit of the fabricated LCD. “P” indicates successful operation at each of the operation frequency and the supply voltage.

shmoo-plot indicates that the driver could be successfully operated under each condition of the operation frequency and the supply voltage. The plot demonstrates that this driver could be operated at 3.0 MHz with the supply voltage of 1.5 V, which was considerably low compared to 12~15 V for conventional poly-Si TFT-based LCDs [74].

Table 5-2 shows the consumed current measured for both the gate driver and the binary data driver circuits at various supply voltages and operation frequencies. The gray cells in Table 5-2 indicate the frequency region where the driver could not operate successfully at the given supply voltage. The power consumption at 1.5 V supply voltage for the typical operation frequency (3.0 MHz) was 100 μW which was

(a) Gate Driver [μA]

[V] \ [MHz]	0.6	1.0	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0
1.1	0.20									
1.5	0.25	0.34	0.58	0.84						
2.0	0.31	0.47	0.82	1.20	1.65	2.10	2.50			
2.5	0.39	0.61	1.07	1.59	2.17	2.74	3.27	3.79	4.32	5.00
3.0	0.48	0.75	1.33	2.00	2.70	3.40	4.07	4.73	5.33	6.20

(b) Binary Data Driver [μA]

[V] \ [MHz]	0.6	1.0	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0
1.1										
1.5	14.8	22.8	45.0	65.7						
2.0	20.9	33.9	65.8	96.2	117.3	131.2				
2.5	29.1	46.0	88.3	129.3	163.9	193.4	237.1	275.0	312.9	
3.0	37.4	59.1	112.4	164.6	215.4	265.5	314.5	362.3	399.4	431.9

Table 5-2. Consumed current by (a) the gate driver and (b) the binary data driver at each of the operation frequencies and the supply voltages. Gray cells mean that the driver could not operate successfully under the condition.

lower by approximately two orders of magnitude than those of conventional LCDs.

Figure 5-9 shows the display image of the checker pattern on the 2.0 inch-diagonal LCD fabricated by the NAOS process. It was found that both of the binary data driver and the gate driver could operate successfully and the LCD could also function properly.

V - 3. Summary

I have fabricated ring oscillators and driver-monolithic LCDs with the poly-Si TFTs which have 1.8 nm NAOS SiO_2/40 nm CVD SiO_2 stacked gate insulator structure on glass substrates. Measurements of the operation frequency and the consumed power lead to the following results and conclusion:

1) The fabricated ring oscillators oscillated even at 1.5 V supply voltage.
2) The oscillation frequency of the ring oscillator with 37 stages was 3.45 MHz at 3.0

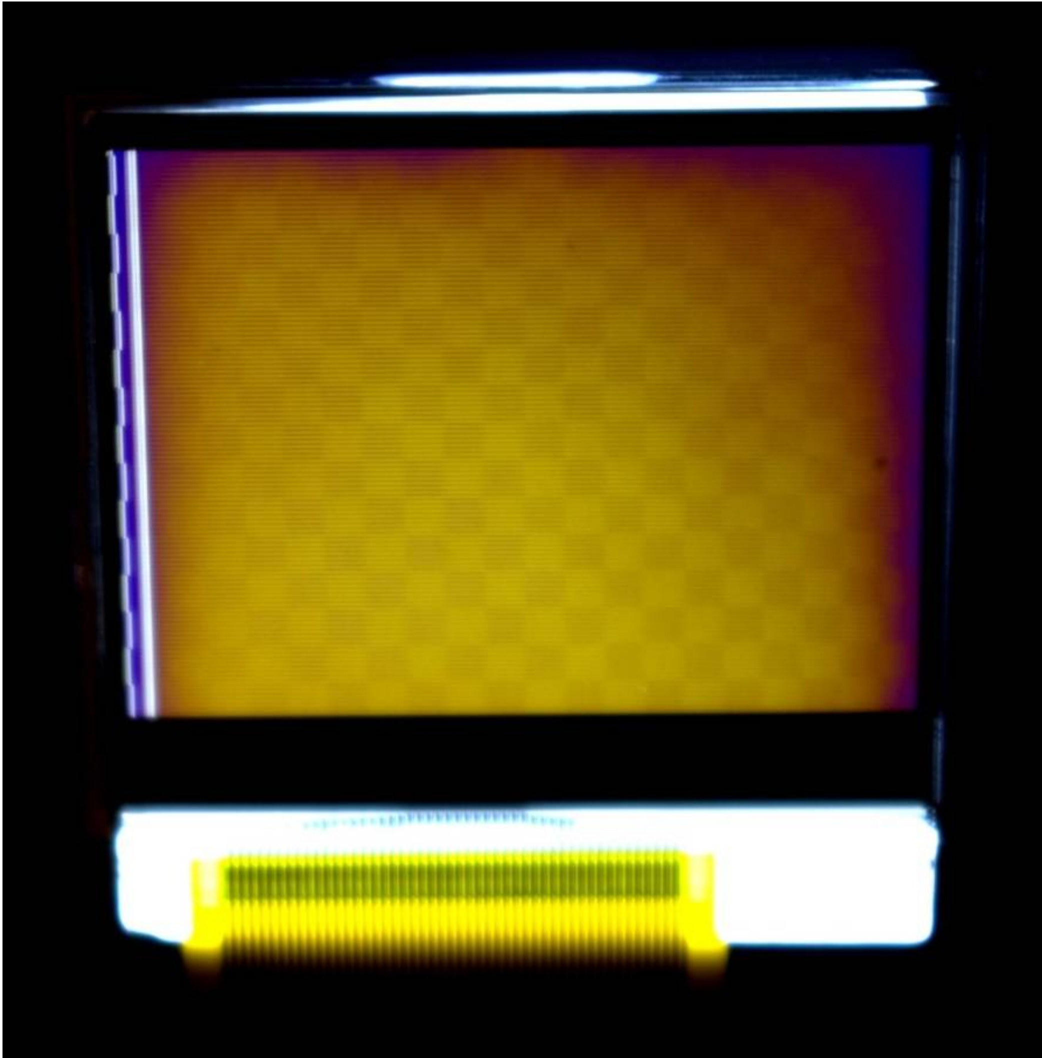

Figure 5-9. Photograph of the display image of the ultra-low power LCD fabricated with the NAOS process.

V supply voltage in good agreement with the theoretical calculation, indicating that the circuits operated ideally.

3) The driver circuits for 2.0 inch-diagonal LCD were operated successfully even at 1.5 V supply voltage, and the ultra-low power consumption of approximately 100 μW, which was about 1/100 compared to that of conventional ones, was achieved.

These performances of circuit operation were due to excellent performance of the poly-Si TFTs with the ultra-thin NAOS interfacial SiO_2 layer having excellent

properties as described in the previous sections. As a conclusion, it was proven that the ultra-low power consumption for LCDs can be achieved with the NAOS method.

VI. Conclusions and Future Work

In this thesis, I have described the NAOS method as a direct oxide method at low temperatures below 120 °C, and evaluation of properties of fabricated SiO_2/Si structure by spectroscopic analyses and electrical measurements. I have focused, especially, on an ultra-thin NAOS SiO_2 film on a poly-Si rough surface and confirmed that the NAOS method can achieve excellent SiO_2/Si interface properties as well as good bulk properties. I have also confirmed that poly-Si TFTs with the NAOS SiO_2/CVD SiO_2 stacked layer as a gate insulator can operate even at 1.0~1.5 V supply voltage, and thus, the consumed power can be decreased to ~1/100 of conventional TFTs with CVD SiO_2 operated at 15 V. The bulk and interfacial properties have been analyzed properly using XPS, FT-IR, and electrical measurements such as I-V and C-V characteristics. From these observations, the following conclusions are obtained:

Concerning the formation of the NAOS SiO_2 layer and their properties;

1) An ultra-thin SiO_2 layer can be formed by the NAOS method with various HNO_3 concentrations and temperatures on Si(100) substrates and poly-Si thin films.
2) Measurements of the Si 2p XPS spectra indicate that the NAOS oxide thickness is in the range between 1.1 and 1.8 nm and it does not depend on the HNO_3 concentration when it is higher than 40 wt%.
3) The densities of sub-oxide species, Si^{+}, Si^{2+}, and Si^{3+}, in the NAOS oxide layer are negligibly low.
4) FT-IR measurements indicate that the atomic density of the NAOS SiO_2 increases with the HNO_3 concentration and the temperature, i.e., 2.32×10^{22} atoms/cm^3 for oxidation with 68 wt% azeotropic HNO_3 at 120 °C, which is higher than that of thermally grown SiO_2 of 2.28×10^{22} atoms/cm^3.
5) The valence-band discontinuity energy at the NAOS SiO_2/Si interface increases with the HNO_3 concentration, which is caused by an increase of the SiO_2 atomic density.

Concerning the electrical characteristics of the MOS diodes with an ultra-thin NAOS SiO_2 layer;

6) I-V measurements indicate that the NAOS SiO_2 layer possesses a considerably low leakage current density (e.g., 10^{-9} A/cm^2 at 8 MV/cm), which is nearly the same as that of thermally grown SiO_2 layer
7) The leakage current is greatly decreased with the HNO_3 concentration and by POA at 400 °C in wet-oxygen, which is due to the large valence-band discontinuity energy, low interface state densities, and negligibly low densities of sub-oxide species.
8) C-V measurements show that the POA at 400 °C in wet-oxygen decreases the density of oxide fixed charges from $+2.8\times10^{12}$ to -1.0×10^{11} /cm^{2}.
9) C-V measurements indicate that SiO_2/Si interface states are not generated by the POA at 400 °C in wet-oxygen.
10) These excellent characteristics are due to a uniform thickness and high atomic densities of the NAOS SiO_2 layer and passivation of the SiO_2/Si interface states.

Concerning the electrical characteristics of the poly-Si TFTs with an ultra-thin NAOS SiO_2/CVD SiO_2 stacked layer;

11) I_d- V_{ds} measurements show that the V_{th} are lower than 0.5 V and the S-values are as low as 65~80 mV/dec for both of the N-ch and the P-ch TFTs, leading to the high saturation current enough for switching function even at the low operation voltage of 1.0 V.
12) The off-current is as low as the noise level (i.e., 10^{-13}~10^{-14} A), leading to the high on/off ratio of 10^9.
13) The interface state densities estimated from the S-values are 5.5×10^{11} /cm^{2}eV for the N-ch TFTs and 3.3×10^{11} /cm^{2}eV for the P-ch TFTs.
14) These excellent electrical characteristics are due to the ultra-thin NAOS SiO_2 layer intervened between the poly-Si thin film and the CVD SiO_2 layer.

Concerning the electrical performance of the poly-Si TFT circuits;

15) The ring oscillator with 37 stages is oscillated at 3.45 MHz and 3.0 V, in good agreement with the theoretical calculation, indicating that the TFTs with the

NAOS SiO_2 layer can be operated ideally.

16) The driver circuits for 2.0 inch-diagonal LCD can be operated successfully even at 1.5 V supply voltage, and the ultra-low power consumption of approximately 100 μW, which is about 1/100 of that of conventional LCDs, is achieved.

Concerning the analyses method for SiO_2 films and SiO_2/Si interfaces;

17) XPS core level spectra in the Si 2p region are useful to estimate the thickness of ultra-thin SiO_2 films and the concentration of sub-oxides species.
18) FT-IR spectra of asymmetric Si-O-Si stretching vibrational modes are available to estimate the atomic densities of SiO_2 films.
19) XPS valence-band spectra can be used for estimating the valence-band discontinuity energy at the SiO_2/Si interfaces.
20) Measurements of C-V characteristics give the densities of oxide fixed charges and slow states at the SiO_2/Si interfaces.
21) SiO_2/Si interface state densities can be estimated by sub-threshold coefficients derived from I_d- V_{gs} measurements of TFTs.

As described above, it has been found that the NAOS method can form an ultra-thin SiO_2 layer with excellent bulk and interfacial properties on a rough surface at low temperatures, and hence, the NAOS SiO_2 layer enables high performance of poly-Si TFTs and a vast power reduction of electrical circuits and systems.

It has been also found, in my study, that annealing processes such as POA and PMA treatments are effective to improve the properties of SiO_2 bulk and SiO_2/Si interface. Optimization of annealing conditions such as atmosphere, temperature, time will further improve the characteristics of the NAOS SiO_2/Si structure.

In this study, application of the ultra-thin NAOS SiO_2 to the gate insulator in TFTs has been found to greatly decrease power consumption to ~1/100, which is attributable to decrease in V and C (cf. Equation (1-1)). In order to further decrease power consumption, a decrease in frequency, f, i.e., the third factor, is necessary. For this approach, I have a promising candidate, which is called as Memory-in-Pixel (MIP) LCDs [75-77]. In the MIP LCD, each pixel has a static RAM which stores the image datum. Therefore, it is not necessary to rewrite image data

periodically, e.g., 60Hz. As a result, the MIP LCD can be operated at a much lower frequency, e.g., 1 Hz, and it enables a further vast reduction of power consumption. I believe that the combination of the NAOS process and the MIP technology is the most promising candidate to achieve ultra-low power LCDs.

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List of Publications

The main papers on this study are as follows.

1) Y. Kubota, T. Matsumoto, H. Tsuji, N. Suzuki, S. Imai and H. Kobayashi, "1.5 V-Operation Ultra-Low Power Circuit of Poly-Si TFTs Fabricated Using Nitric Acid Oxidation of Silicon (NAOS) Method," *IEEE Trans. Electron Devices,* **59** (2), 385-392 (2012).
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1) K. Edamoto, Y. Kubota, M. Onchi, and M. Nishijima, "Obserbation of the Methoxy Species on the Si(111)(7x7) Surface - A Vibrational Study," *Surface*

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