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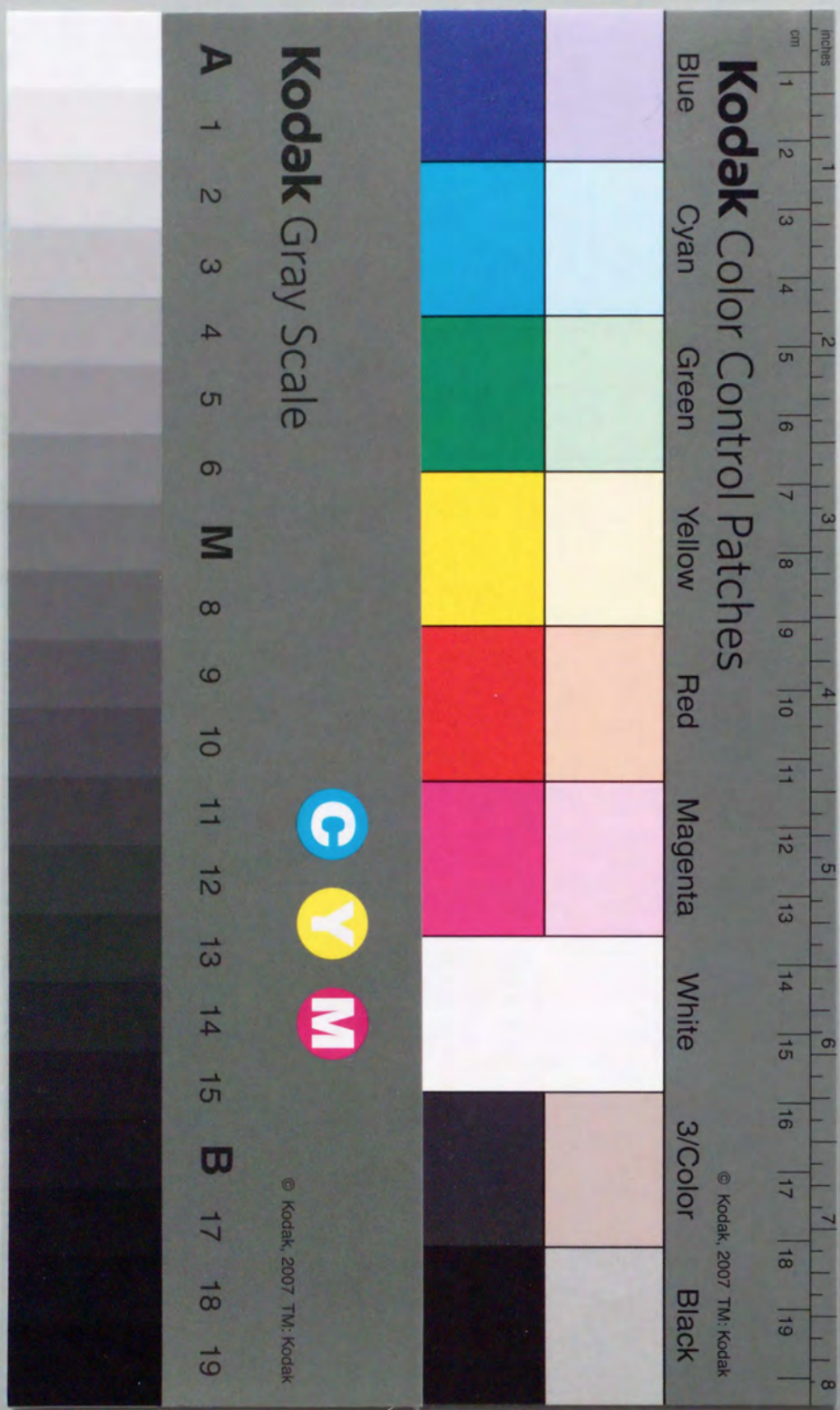
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Control Methods for  
Quality of Service on ATM Networks

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Osaka University  
December 1995



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Doctoral Dissertation  
Control Methods for  
Quality of Service on ATM Networks  
(ATM 網における通信品質保証のための制御技術に関する研究)

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December 1995

## Preface

This thesis investigates control methods guaranteeing QOS on the ATM network. The ATM network accommodates many kinds of services. These services are categorized into two groups, isochronous and error-free. For isochronous services, the QOS guarantee is important. We investigate former studied methods and propose a new scheme which satisfies all requirements of isochronous services. On the other hand, the decrease of the block(a unit of error control) loss probability is significant for error-free services. The FEC-SSCS technique is efficient to respond this demand, so we evaluate the message level performance of FEC-SSCS combined with Go-Back-N on the ATM network. This thesis consists of the following 5 chapters.

Chapter 1 provides a review of the ATM technology and its problems. The necessities of the control satisfying QOS for each connection and the significance of this research are clarified.

Chapter 2 proposes a new control method which guarantees QOS for isochronous services, e.g. voice or video. These services are very sensitive to a transmission delay, and it is difficult to introduce a retransmission mechanism because of its long delay. STM satisfies these requirements by allocating time slots for each connection. This allocation excludes an interference among connections in the network. On the other hand, because ATM is based on asynchronous multiplexing, the variation of a transmission delay and the loss of information occur in the ATM network.

It is efficient to allocate cell transmitted positions for each connection on the ATM network. This means a virtual STM transmission. We propose a new method based on this concept and call it Quasi-STM(Q-STM). This method achieves a cell loss free and delay jitter free transmission on the ATM network. Moreover, the Q-STM method suppresses the increase in a time switching delay by introducing a new concept, *subframe*. The statistical multiplexing gain is also obtained even in the Q-STM allocated slots, since a normal ATM service class is accommodated in addition to the Q-STM service class. The frame structure, the concept of the ATM service class, the switch architecture, and the call setup procedure are described respectively.

Chapter 3 investigates the performance of the Q-STM method, treating the design issues and the evaluation of availability. It is necessary to determine the algorithms of the call setup and the number of subframes. For the sake of obtaining the general indices for these design problems, (i)the availability of call setup algorithms considered in chapter 2 are evaluated and (ii)the influence of the number of subframes are investigated. Through these evaluation, the efficient algorithms and number of subframes are clarified.

In order to clarify the availability of the Q-STM method, (iii)the QOS of the ATM service class and (iv)the call setup time caused by introducing the Q-STM method are evaluated. Although the QOS of the Q-STM service class is guaranteed, that of the ATM service class seems to be degraded because this class has a lower priority than the Q-STM class. Besides, the treated bandwidth spreads widely in the B-ISDN environment. This brings the allocation of a large number of slots for one broadband Q-STM call. These demerits of the Q-STM method are evaluated quantitatively. For the first three evaluations, computer simulations are used.

Chapter 4 presents the performance analysis of the QOS control method for error-free services, e.g. data communication or high density picture. For error-free services, it is important to decrease

the block loss probability in the ATM network. The FEC-SSCS technique is efficient to satisfy this requirement. In this chapter, we analyze the message level performance of FEC-SSCS. The message level performance is significant, since it is what users actually feel. In order to evaluate the message level performance on the ATM network, three layers (*a message, a block, and a cell*) must be considered. However, the analysis considering these three layers has not been done yet. We re-evaluate the performance of the combination of FEC-SSCS and Go-Back-N when the three layers are considered.

Chapter 5 summarizes the overall conclusions reached in this thesis.

The work summarized in this thesis is conducted by the author during his Ph.D. course at the Department of Communication Engineering, Graduate School of Engineering, Osaka University.

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## Chapter 1

# Introduction

The establishment of a digital switching technology realizes an Integrated Services Digital Network (ISDN). Different kinds of services, e.g. voice, video, or computer communication, are accommodated in ISDN in the forms of a digital signal. This network can provide a unified interface to each terminal [1].

Recently, data communication between several kinds of computers has been increasing because of the appearance of distributed computing. A demand for services requiring broad bandwidth, e.g. a long distance simulation using a super computer or a high density picture for medical treatment is growing more and more [2]. Now, a Broadband-ISDN (B-ISDN) is expected to be the next-generation network satisfying these high demands [3]. B-ISDN is to accommodate many kinds of broadband services, whose rate exceeds  $10\text{Mbps}$ , in addition to ordinary services, e.g. voice communication. These services can be grouped into two categories, an *isochronous* service and an *error-free* service. Examples of an isochronous service are voice and video. These services are very sensitive to a delay variance quality. On the other hand, example of an error-free service is data communication. Although an error-free service does not require a timing synchronization, it demands error free transmission.

B-ISDN requires the following two abilities. The first is a high speed switching capability (the throughput of a switching node in B-ISDN will be in  $\text{Gbps}$  range [3]). The second is the flexible accommodation of various kinds of services, including bursty services whose rate changes widely with time. A Synchronous Transfer Mode (STM), which has provided isochronous services, satisfies the first requirement. On the other hand, a storing and forwarding type network which has accommodated error-free services, e.g. a packet switching or a frame relay network, meets the second one. However, none of these ordinary networks can satisfy both demands simultaneously.

A new technology called Asynchronous Transfer Mode (ATM) has been recommended as the transmission and switching system of B-ISDN in International Telecommunication Union Telecommunication Standardization Sector (ITU-TS) [4]. ATM has two main concepts [3]: (1) synchronous time switching using a time slot of fixed length and (2) asynchronous transmission based on a label multiplexing. Using a transmission unit of the fixed  $53\text{bytes}$  length, called "cell", enables it to switch information bits quickly as in STM. ATM is superior to packet based networks from the viewpoint of this high speed capability. In a packet based network using a variable length transmission unit, a switching delay can not be decreased enough to satisfy the B-ISDN requirements because of its software based processing.

Senders on the ATM network can insert cells into any slots, and each cell is distinguished by the 5bytes label attached for 48bytes ATM payload. The label multiplexing enables it to accommodate services flexibly whose rate changes widely. On the other hand, there is no label concept in the STM network. Because each connection is distinguished by its position within a time frame, information bits are sent within the preassigned positions. ATM is superior to STM from the viewpoint of this flexible capability. ATM is considered to be the most attractive transmission method which incorporates merits from both STM and packet based networks.

The functions of the ATM network are provided by three layers, a physical layer, an ATM layer, and an ATM Adaptation Layer(AAL) [3]. The protocols for packaging data into cells are collectively referred to as AAL. The purpose of this layer is to efficiently fragment various kinds of higher layer data, such as Internet Protocol(IP) packets, voice samples, and video frames, into cells and to reconstruct cells into a higher layer frame. AAL consists of two sublayers, a Segmentation And Reassembly(SAR) sublayer and a Convergence Sublayer(CS). The SAR sublayer is responsible for breaking data into cells and reassembling cells into upper layer data units. CS is responsible for managing the flow of data to and from the SAR sublayer.

Four types of AALs are considered [5, 7, 8]. AAL 1 and 2 is for an isochronous, continuous bit-rate transmission, e.g. voice and movie. On the other hand, AAL 3/4 and AAL 5 are for an error-free, bursty transmission, such as data communication. The description of AAL 3/4 and AAL 5 is shown in section 4.2.

In the ATM network, three methods are considered for service accommodation: a Constant Bit Rate(CBR), a Variable Bit Rate(VBR), and an Available Bit Rate(ABR) [5]. CBR is supported by AAL 1, and cells generated by one sender terminal are accommodated in the network at a constant rate. VBR is supported by AAL 2, and cells generated by the sender terminal are transmitted at a variable rate. However, a time frame concept exists in VBR, and the time frame synchronization is necessary for both sender and receiver terminals. Hence, these two classes are considered for isochronous services. On the other hand, ABR supports error-free services. Calls of this class are not allocated bandwidth, and their transmission rates are changed dynamically according to the network load.

Next, we describe how to accommodate an isochronous service and an error-free service respectively, as well as some problems caused in ATM for each service category.

*Isochronous* services, including voice and video, are almost treated as CBR [12]. The rate of video sources is variable because of an encoding which reduces required bandwidth. However, it is possible to treat a video source as CBR by means of providing a buffer at the sender terminal. If a video source is treated as CBR, an estimation of required bandwidth and a Usage Parameter Control(UPC) become simpler. However, accommodating video sources as VBR has some attractive merits. Through a statistical multiplexing, the network can carry more VBR video calls than CBR ones. Alternatively, users can obtain better quality with VBR than CBR video if both sources are accommodated with the same bandwidth [13]. In this case, video sources will use AAL 2(a complex UPC is necessary for this protocol, so the standardization is under way).

Next, we consider some problems in the ATM network for isochronous services. Each CBR(VBR) service should be allocated required bandwidth in order to guarantee QOS. The reason is as follows. The sensitiveness to a delay quality makes it difficult to introduce a retransmission mechanism. Without a bandwidth reservation, CBR(VBR) services are faced with a serious QOS degradation when congestion happens in the network.

Besides, it must be noted that the bandwidth allocation in the ATM network does not mean the assurance of QOS directly as the case of the STM network. The reason for this is as follows. We must pay attention to the propagation of the congestion caused among ABR services to CBR(VBR) services, because the CBR(VBR) traffic shares the same resources in the network with the ABR traffic. In addition to this factor, the "label multiplexing" of cells causes a variance in a cell transmission delay for CBR(VBR). Therefore, some controls which guarantee the QOS of CBR(VBR) must be introduced on the ATM network.

Senders of *error-free* services, such as data communication, tend to send cells with a high rate during a short period and remain idle for a long time. If bandwidth is allocated to these services, a peak rate will be assigned and the network efficiency will be degraded. A Fast Reservation Protocol(FRP) allocating bandwidth for each burst was proposed [14, 15]. The consumption of bandwidth is limited to the period when information is actually sent. However, the failure of a bandwidth reservation increases the data forwarding delay in FRP.

Now, the definition of ABR is in progress at the ATM Forum [16, 17]. The rate is controlled based on the load information generated by ATM nodes. Therefore, a congestion can occur because of the control delay between congested nodes and terminals. However, ABR can satisfy a required Quality Of Service(QOS), i.e. a cell loss rate, a cell forwarding delay, and a delay jitter, since error-free services are not sensitive to a delay quality(retransmission is possible). ABR is attractive because of the flexible accommodation of error-free services.

Next, we consider some problems in the ATM network for error-free services. The perfect prevention of bit errors and information loss caused by a congestion is impossible in the ATM network. However, the forwarding of the whole information bits without any error is necessary for error-free services, e.g. data communication, so an error control is indispensable for these services. The error control will be introduced in AAL or a transport layer in the ATM network. The unit of this error control is described as a "block" in this thesis. Both sender and receiver terminals must perform per-block processing for each block during the block period. Some examples of this per-block processing are a header and trailer generation, an error control, and a timer control. In general, it is better to use a few large blocks instead of many small blocks to carry a given amount of data, because the protocol processing time required for each block can be a bottleneck of throughput [18]. As a result, the block length tends to be longer as the interface rate increases: the size of a Transmission Control Protocol(TCP) block is 512bytes, 1500bytes for ethernet networks, 4352bytes for a Fiber Distributed Data Interface(FDDI) networks, and 9180bytes is the default for IP over ATM [19, 20].

The small size of a cell is desirable for isochronous services because of the following two reasons [5]. First, the longer cell causes a longer waiting time at switches. Second, it takes more time to get enough data to fill one ATM cell payload from a low rate voice source if the cell size becomes



longer<sup>1</sup>. Because the bandwidth of the ATM network will continue to grow, the first problem can be negligible, however the second problem will continue to remain. Therefore, the size of 53bytes has been recommended from ITU-TS. However, this size is too small compared to the block length.

As a result, each block is fragmented into many cells(in the case of the 9180bytes block size, one block consists of 192 cells using AAL 5). It has been known that the fragmentation of a block into small pieces can cause disastrously low performance if any of the pieces are lost in transit [18]. The loss of any cells constituting one block causes the retransmission of whole part of the block and a throughput degradation. When only the lost cells are retransmitted, this degradation can be relieved. However, cell-based retransmission requires an 8 byte sequence number field for each cell [22], then it becomes a high overhead of 15%. The superiority of a frame-based retransmission to a cell-based one has been also clarified numerically [23]. As a result, the throughput degradation of the ATM network caused by the fragmentation of a data block will be a serious problem [18, 24].

The interface rate in the ATM network will be much faster than ordinary data networks: it will be faster than 150Mbps in the ATM network and, on the other hand, it is less than 64kbps in packet exchange networks and, less than 1.5Mbps in frame relay networks. Moreover, it will continue to grow in the ATM network. A message(a unit of information expected to be transmitted, e.g. one data file) forwarding delay consists of two portions, a message transmission delay and a propagation delay. The improvement of the interface rate decreases only the transmission delay. The propagation delay will be large compared with the transmission one, then become a dominant factor of the forwarding delay in gigabit networks or ATM networks [25, 26]. Once retransmission occurs, one round trip propagation delay is added to the message forwarding delay. Hence, the delay caused by retransmission may be a dominant factor of the forwarding delay of a large volume message, so it is important to reduce the number of retransmission in the ATM network.

The control method diminishing the block loss probability is indispensable for ABR services. This is derived from the two reasons mentioned above: the throughput degradation caused by a block fragmentation and the relative increment of a propagation delay caused by a growth in the bandwidth.

Some control methods must be introduced to guarantee the QOS of isochronous services and improve the QOS of error-free services. The main purpose of this thesis is to investigate control methods which aim to satisfy above requirements.

In chapter 2, control methods guaranteeing some of QOS for isochronous services are discussed. Among the proposed methods so far, three representative control methods are considered in this thesis: a delay jitter compensation method introduced in AAL 1 [27, 28, 29, 30, 31], a buffer priority control [26, 32, 34, 35, 36, 37], and stop-and-go queueing [38, 39, 40, 41, 42]. We summarize the purposes and limits of these schemes.

The STM network has satisfied the QOS of isochronous services in addition to realizing a high speed transmission by means of hardware based switching. The allocation of time slots for each connection enables it to achieve high performance because this reservation excludes the interference among connections. However, error-free services are not suited for a STM type network. Therefore,

<sup>1</sup>There is a concept of a partially filled cell [21] in which each cell is transmitted when a part of ATM payload(e.g. 8bytes) is filled. In this case, the delay caused by making up one cell is small even when the cell size is large. However, partially filled cells waste bandwidth and costly.

a number of literatures have argued for a technology which combines a packet-based transmission with a Time Division Multiplexing(TDM) system(such as STM) [43, 44, 45, 46]. Here, it is efficient to consider allocating cell transmitted positions for each call on the ATM network. This means a virtual STM transmission on ATM. We propose a new method based on this concept and call it Quasi-STM(Q-STM) [47, 48, 49].

This method realizes a cell loss free and delay jitter free transmission on the ATM network. In order to allocate a cell transmitted position for each call, frame and slot concepts are introduced on a time axis. The frame is a period of bandwidth allocation, and the slot is a unit of it. Because this method is based on the ATM network, the time slot corresponds to the ATM cell slot. This slot length is too long compared with the STM network, so the frame length becomes large(if 64kbps voice source is accommodated, the frame size is 6ms). Thus, the time switching delay becomes large, so we newly introduce a new concept, *subframe*, which is composed by splitting one frame into multiple equivalent time intervals. The subframe concept can decrease the time switching delay. As a result, this method constructs three layers on a time axis, the *frame*, the *subframe*, and the *slot*. By the way, the statistical multiplexing gain is also obtained even in the allocated slots, since a normal ATM service class is accommodated in addition to the Q-STM service class. A frame structure, a concept of ATM service class, a switch architecture, and a call setup procedure are described respectively.

In chapter 3, we investigate performance of the Q-STM method, treating design issues and evaluating the availability [50, 51]. Because the Q-STM method regards the subframe as a period of time switching and uses Time switch-Space switch-Time switch(TST) structure to exchange Q-STM cells, the call setup procedure of the Q-STM method consists of three processes: the calculation of the number of slots allocated within each subframe, the slots allocation on each link, and the reservation of intra-switch routes. Except for the third process, algorithms of each process affect some properties of Q-STM and ATM cells. Through the performance evaluation of these call setup algorithms, the efficient algorithms for each process are clarified.

The subframe length can not be obtained easily, because this size affects three qualities: the Q-STM cell end-to-end delay, the Q-STM call blocking probability, and the QOS of the ATM service class. We evaluate the influence of the number of subframes for these three qualities, then roughly obtain the most efficient value.

In order to clarify the availability of the Q-STM method, we evaluate the QOS of the ATM service class and the call setup time caused by introducing the Q-STM method. Though the QOS of the Q-STM service class is guaranteed, the QOS of the ATM service class seems to be degraded. This is because that the ATM class corresponds to a low priority class compared with the Q-STM class. To understand the degree of the degradation numerically, the mean intra-switch cell delay of the ATM service class is compared to a buffer priority control and a normal ATM.

Because treated bandwidth spreads widely in the B-ISDN environment, the frame length must be long in order to accommodate a narrowband service. Therefore, a large number of slots must be allocated for a broadband service. This leads the apprehension of an unpardonable growth of the Q-STM call setup time. We construct the algorithms and sum up the all required steps, then clarify the additional call setup time.

In chapter 4, we consider some methods decreasing the block loss probability of error-free services.

There are three factors that cause a block loss: a random bit error, a burst bit error, and congestion [52]. Although errors in fiber transmission are extremely rare, it is known to take the long burst mode if they do occur [5]. AAL introduces a Cyclic Redundancy Check(CRC) to detect or correct a few bit errors. However, CRC can not correct a burst bit error. Therefore, a burst bit error as well as a congestion result in a cell loss, so the techniques which consider cell loss are important in decreasing the block loss rate.

Two kinds of methods have been proposed: one is the selective cell discarding method [6, 19, 53], and the other is a cell based Forward Error Correction(FEC) introduced in a Service Specific Convergence Sublayer(SSCS) [54, 55, 56, 57, 58]. SSCS is an upper sublayer of CS and treats the process depending on the service. The former method needs a software-based complex processing at ATM switching nodes. On the other hand, the additional process is necessary only to both sender and receiver terminals for the latter method. The B-ISDN environment requires a high speed switching capability, so we consider that FEC-SSCS is superior to the selective cell discarding method. By adding some FEC redundant cells to each block, FEC-SSCS makes it possible to recover the block containing some lost cells without retransmission if the number of lost cells is less than or equal to the number of redundant cells within the block. We analyze the performance of FEC-SSCS to clarify the efficiency for several parameters [59].

The message level performance is significant, since it is what users actually feel. In order to evaluate the message level performance on the ATM network, three layers(a *message*, a *block*, and a *cell*) must be considered. However, the performance of FEC-SSCS considering the three layers has not been analyzed yet. We respect these three layers. When the number of lost cells among a block exceeds the number of redundant cells, FEC-SSCS can not recover the block. In this case, it is assumed that the corrupted block is retransmitted based on a Go-Back-N(GBN) in this thesis. The two state Markov chain is applied to the cell loss process in order to consider the burst cell loss tendency at ATM nodes. The mean message forwarding delay is evaluated for the case of fixing cell loss rate. On the other hand, in the case of reflecting the network load to the cell loss rate, the maximum throughput is investigated. We evaluate these qualities against the network load, the block length, the interface rate, and the mean number of consecutive cell losses.

In chapter 5, we summarize the overall conclusions obtained in this thesis.

## Chapter 2

# Synchronous Transmission in ATM Networks

### 2.1 Introduction

One important category of services accommodated in B-ISDN is an isochronous service. The examples of this kind of service are an ordinary telephone supported by a circuit switching network(i.e. STM) or Narrowband-ISDN(N-ISDN). A video distribution, e.g. video on demand [60, 61, 62], television conference, or remote education are new applications and also good representatives of isochronous services. These new services will become one of the main applications of B-ISDN in future.

Isochronous services have a strict requirement for a forwarding delay quality: both a mean value and a variance(jitter). If the forwarding delay becomes large, receivers experience an unnatural pause of a conversation in voice or a distortion of a picture in video. The large delay variance causes an information loss because information bits which do not arrive in time for their playing back are dropped at the receiver. Therefore, the delay jitter also degrades these qualities.

In addition to this requirement, a video service needs to be assured a low cell loss rate(for example, broadcast quality video requires less than  $1.2 \times 10^{-9}$  end-to-end cell loss rate [12]) because users are very sensitive to a degradation of a picture quality. As a result, high requirements for these QOSs(the mean delay, the delay jitter, and the cell loss rate) exist in the ATM network for isochronous services.

The ATM network permits each sender to transmit a cell in an arbitrary time slot and cells are multiplexed by a label attached in the cell header. Hence, there is a possibility that plural number of cells arrive at a certain output port of an ATM switching fabric at the same time, and some amount of a memory facility are necessary to store cells. This principle makes the following four problems for isochronous services: (1)a delay jitter, (2)a buffer overflow caused by VBR, (3)a cell collision in the ATM switching fabric, and (4)propagation of congestion caused by ABR. The explanation of these four problems is shown in section 2.2.

Some control methods must be introduced to guarantee the QOS of isochronous services. In section 2.3, we consider some methods which aim for the assurance of the isochronous service QOS. Among proposed methods so far, three representative control methods are considered: a delay jitter compensation method introduced in AAL 1, a buffer priority control, and a stop-and-go queueing.

The simplest method to answer the first problem, i.e. recovering a timing of CBR services, may be the attachment of some memories to receivers. AAL 1 absorbs the delay jitter caused in the ATM

network by means of adding some amount of delay [27, 28, 29, 30, 31]. The amount of the required memory will become extremely large because the number of connections communicating with the same receiver simultaneously continues to increase. The another problem is that the establishment of the volume of the additional delay to recover a delay jitter is difficult.

To resolve the second and fourth problem, buffer priority controls have been proposed [26, 32, 33, 34, 35, 36, 37]. Introducing a concept of priorities among isochronous services can avoid the second problem, and establishing them between CBR(VBR) and ABR enables it to prevent the fourth one. Although these methods can guarantee the cell loss rate and the worst-case queueing delay (statistically), the maximum delay jitter and the deterministic guarantee of the worst-case delay can not be assured.

The stop-and-go queueing method [38, 39, 40, 41, 42] responds to the second and the fourth problems and partially the first one by introducing a time frame concept. It provides guaranteed services per connection with no cell loss and end-to-end delay of a constant plus a small bounded jitter term. However, the cell queueing delay is much larger than any other methods if the flexibility of bandwidth allocation is kept. Furthermore, the fluctuation of cell delay within a frame can occur because of interaction among cells of other connections.

The STM network has satisfied the QOS of isochronous services in addition that a high speed transmission has been realized by a hardware based switching. The allocation of time slots for each connection enables it because this reservation excludes the interference among connections. However, error-free services are not suited for a STM type network. Therefore, a number of literatures have argued the technology which combines a packet-based transmission with a TDM system (such as a STM) [43, 44, 45, 46]. Here, it is efficient to consider the allocation of cell transmitted positions for each call on the ATM network. This means a virtual STM transmission on ATM. We propose this new method named as Q-STM [47, 48, 49].

In this scheme, a time *frame* concept is introduced. The frame is divided into some numbers of *subframes*, all of which are the same length. The subframe is again divided into *slots*, which is a unit of bandwidth allocation. Because the time positions of each call are fixedly allocated with respect to all links on the route, the time switching of slots at each switch is necessary for the flexibility of slot reservation. In the Q-STM method, the basic period of this time switching is not a frame but a subframe, which remarkably reduces storing delay at each intermediate node. Furthermore, this scheme also provides general ATM service class<sup>1</sup>, which is free from a restriction of time frames, in addition to the Q-STM service class. So two kinds of cells (Q-STM and ATM cell) are mixed on one link. Because of the allocation of time positions, Q-STM calls are able to be not only realized the transmission of cell loss free and no intranetwork delay jitter, but also performed UPC structurally. And vacant position in a frame, which may occur due to the rate fluctuation of Q-STM calls or which is not reserved by Q-STM calls, can be utilized by ATM calls. In other words, ATM class cells can use not only non-allocated slots for Q-STM, but also the cell position without a Q-STM cell even if it is in the slot allocated for Q-STM. By the effects of statistical multiplexing of ATM cells, slots not used by Q-STM cells are utilized efficiently.

<sup>1</sup>In this thesis, we simply call this class of cells as "ATM cell".

## 2.2 Problems for Isochronous Services in ATM Networks

In the ATM network, the following four problems exist for isochronous services: (1) a delay jitter, (2) a buffer overflow caused by VBR, (3) a cell collision in ATM switching fabric, and (4) propagation of congestion caused by ABR. In this section, we explain these four problems briefly.

### [1. Delay jitter]

The information of a voice source is encoded at a constant period. For instance, an analog voice source is quantized 8bits digital information in the 125 $\mu$ s interval [21]. Therefore, digital information bits are sent at the constant rate<sup>1</sup> On the other hand, the rate of video sources is variable because of an encoding scheme which reduces required bandwidth. By a technique of a high efficient encoding, e.g. H.261, MPEG1, and MPEG2 [63, 64], required bandwidth is decreased dramatically. In the case of a High Density TeleVision (HDTV), the original analog bandwidth, e.g. several Gbps, is reduced to around 20Mbps by MPEG2 [5]. If a video source is treated as CBR, an estimation of required bandwidth and UPC become simpler. Therefore, some video sources are sent as CBR. As a result, many isochronous services will be accommodated in the ATM network as a CBR service.

The sender of a CBR service transmits cells at a constant interval  $T$ , and the receiver must read arrived cells at the same interval  $T$ . However, a cell experiences a forwarding delay variance (jitter) because of a queueing at an ATM switch. This delay jitter caused one queue is accumulated because each connection passes plural number of ATM nodes. Besides, the estimation of the upper limit of a jitter is difficult. As a result, the recovery of a CBR source timing is one of the important issues in the ATM network.

### [2. Buffer overflow caused by VBR]

If all isochronous services are supported as CBR and the sum of the rate of all CBR services accommodated to a certain link is less than the link capacity, the queue length of cells waiting to be transmitted in the ATM switch does not become long. Although the size of a memory attached to the ATM switch is finite, the amount of memories which are necessary to avoid the buffer overflow completely can be understood. However, accommodating a video source as VBR has some attractive merits. Through a statistical multiplexing, the network can carry more VBR video calls than the case of CBR. Alternatively, users can obtain better delay quality with VBR than CBR video when both sources are accommodated as the same average rate [13]. Therefore, it is reasonable to consider that some VBR calls will be supported in addition to CBR for isochronous services in future.

Provided that all VBR services are allocated bandwidth in a peak rate, buffer overflow at the ATM switch will not occur in this case, too. However, the peak rate allocation degrades the network efficiency and increases a cost. Therefore, it is important to accommodate these VBR sources with the rate which is less than their peak. In this case, it is necessary to introduce a Call Acceptance Control (CAC) at a call setup in order to guarantee the worst cell loss rate caused at passing ATM

<sup>1</sup>In addition to this constant rate encoding, a variable rate encoding has been considered. It stops cell transmission while a silent period and tries to save the network resource. In this case, the cell transmission rate during a talking period is constant. Therefore, we can apply the following discussion to this variable encoding case, too.

nodes. However, CRC must satisfy the most strict requirement for the worst cell loss rate. In other words, the most strict quality level is applied for all isochronous services. As a result, the efficiency of isochronous service accommodation degrades because of the buffer overflow caused by VBR.

### [3. Cell collision in ATM switching fabric]

Many kinds of ATM switch architectures have been studied [94, 95, 96, 97]. The ATM switch falls into one of two broad categories: (i) a multistage, self routing array and (ii) a single stage fabric.

The multistage switch consists of many small switch elements, and each cell passes some elements [65]. In general, the larger the size of a switching fabric becomes, the higher the required switching speed becomes. Therefore, the multistage switch is considered to be an attractive ATM switching architecture for a central office class switch which connects 1000 – 10000 lines [94]. However, there is a possibility that a cell collides another cell at passing switch elements. The cell loss caused by this internal blocking can not be ignored, so some routing techniques avoiding an internal blocking have been considered [66, 67]. These non-blocking self routing arrays can evade a cell collision at passing switch elements, however, they require a complex control which are against the fundamental principle of ATM: *removing a software-based complicated processing from a switching node* in order to realize a high speed capability.

The other category of an ATM switch is the single stage fabric. There is no internal blocking and each cell can be exchanged with a simple processing. This category is again classified into two subcategories: a space division switch and a shared resource switch.

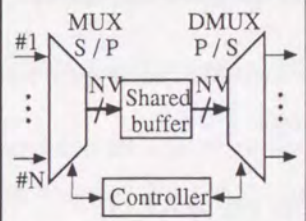
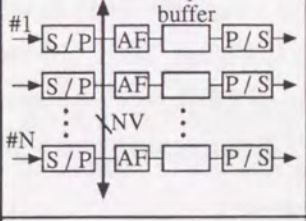
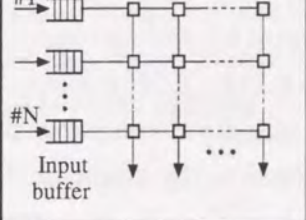
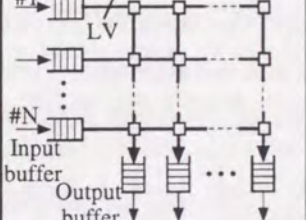
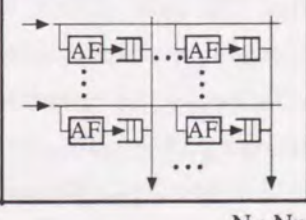
The examples of the space division switch are an input buffer switch [68] and a crossbar switch [69]. Though a high speed memory access is not necessary for the input buffer switch, a Head Of Line (HOL) phenomenon<sup>1</sup> degrades throughput much. Providing a memory for each cross point of input lines and output ones, the crossbar switch realizes a high performance. However, the amount of memories is proportional to the square of the switch size and the efficiency of memories is worse than other architectures.

The final category of ATM switches, i.e. the shared resource switch, can achieve the best performance from the viewpoint of a memory efficiency, a throughput, and a simplicity. A shared memory switch and an output buffer switch [70, 71, 72] exemplify this category. The problem of these switches is a required high speed memory access capability. This difficulty limits a switch scale. Hence, it is efficient to make an upper limit to the number of cells which can be accepted simultaneously at the same output port because the probability that many cells go to the same output link at the same time is little. A knockout switch [73] is one example of this shared resource switch. This switch provides the upper limit on the number of cells simultaneously accepted at an output port of a switching fabric, so it decreases a memory access speed. The knockout switch causes a cell loss at an output port of a switching fabric when cells exceeding the capacity try to go to the same output port simultaneously. An input and output buffer switch [74] is an alternative method to decrease a memory access speed. Though the output port contention can be avoided, an additional scheduling is necessary for each input port. Table 2.1 summarizes the single stage ATM switch architectures.

<sup>1</sup>When a head cell of a queue is waiting, behind cells must wait even if the aimed output ports are available.

For multistage switches, a complex control requires in order to avoid a cell internal blocking at the ATM switch. Therefore, we consider that the shared resource switch is preferable. However, the cell collision at output ports of the ATM switching fabric occurs if we construct a large scale switch. This cell loss also leads the efficiency degradation of isochronous service accommodation.

Table 2.1: Comparison of the single stage ATM switch architecture.

		Switch architecture	Memory access rate	Control rate
Shared resource type	Shared memory		2NV	2NV
	Shared bus (Output buffer)		(N+1)V	V
Space division type	Input buffer		2V	2NV
	Input-output buffer		(L+1)V	V
	Cross-point buffer		2V	V

V : Link capacity  
 AF : Address filter  
 L : Speed up ratio inside switching fabric  
 N : Number of input links  
 S/P : Serial - parallel converter  
 P/S : Parallel - serial converter

#### [4. Propagation of congestion caused by ABR]

An ABR sender starts to transmit cells without a bandwidth allocation and changes a transmission rate depending on the network load [75, 76, 77]. When the network falls a congestion state because of e.g. the increment of number of ABR connections, a rate control method informs senders to decrease the rate. However, the estimations of the control delay and the best threshold value (a trigger of the control) are difficult, so cell loss caused by ABR congestion can not be avoided perfectly. Because isochronous services accommodated as CBR or VBR are multiplexed with ABR services on the same link, the congestion will propagate to CBR(VBR) services. In other words, the bandwidth allocation of isochronous services in the ATM network does not mean the assurance of QOS as the case of the STM network.

### 2.3 Transmission of Isochronous Traffic

In this section, three former methods, which aim to satisfy some requirements among four problems mentioned previous section, are introduced.

#### 2.3.1 Delay Jitter Compensation on AAL 1

In the ATM network, each cell experiences a variable delay in addition to a fixed delay. The fixed delay is caused by a propagation delay and, on the other hand, the variable delay is produced by a queueing at passing ATM nodes. The upper layer of CBR receivers requires AAL 1 to deliver information at a constant interval. The transport of a CBR signal through the ATM network is usually referred as circuit emulation [30, 34].

The one solution to compensate delay jitter caused in the ATM network is an introduction of a buffer which absorbs the delay variance at AAL 1 of receivers. The AAL 1 of a CBR sender transmits cells at the same interval,  $T$ , and the AAL 1 of a CBR receiver delivers cells to the upper layer every  $T$  cycle. As mentioned above, total delay consists of two parts, fixed delay including propagation delay and variable delay. Fixed one can be defined as the minimum delay. To adjust the total delay to fixed value, adequate amount delay which is less than  $D_T$  is wasted in the buffer. This additional delay absorbs the variance of delay. As a result, the variable delay (which is less than  $D_T$ ) is controlled to the same value,  $D_T$ . If a cell experiences the variable delay exceeding  $D_T$ , it is dropped at the receiver AAL 1. This is because that the amount of the delay jitter can not be controlled to  $D_T$  by adding delay in this case.

Figure 2.1 shows the example of a delay distribution between a sender and receiver. Let define  $D_f$  as a fixed delay and  $D_v$  as a variable delay. The ratio of cells whose  $D_v$  is less than  $Q_{max}$  is  $x\%$ . The adjustment of  $D_v$  to  $Q_{max}$  guarantees that  $x\%$  cells experience the same delay  $D_f + Q_{max}$ . These  $x\%$  cells are sure to arrive at the receiver buffer before the instance they should be delivered to the upper layer. Other  $(1-x)\%$  cells will delay exceeding  $D_f + Q_{max}$ , so the adjustment is impossible and they are lost by receivers. Therefore, the cell loss rate  $(1-x)\%$  can be guaranteed if the additional delay is controlled to satisfy

$$D_T \geq Q_{max}. \quad (2.1)$$

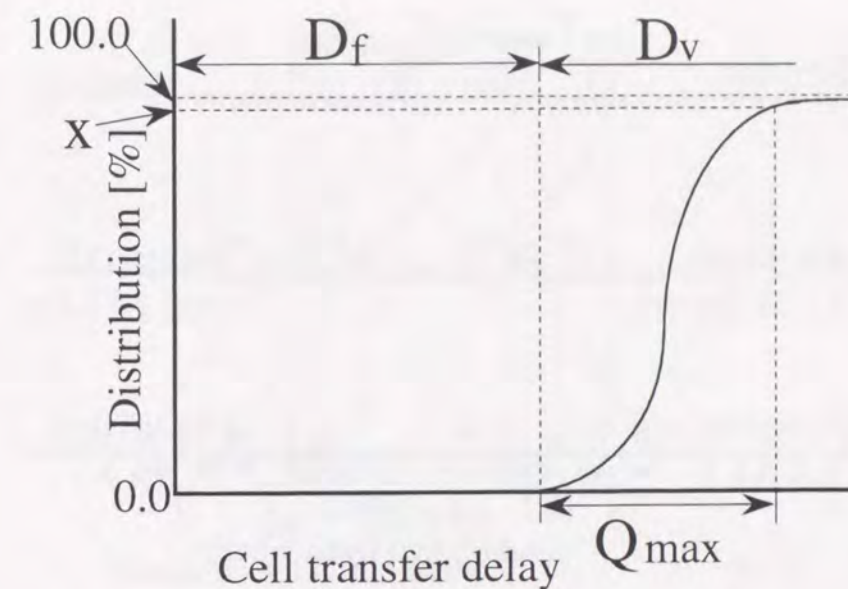


Figure 2.1: Example of the cell delay distribution.

The calculation of  $D_T$  is important issue because  $D_T$  gives the tradeoff between a cell loss quality and a cell delay quality, memory cost. Some ways of  $D_T$  determination have been considered [27, 28, 29]: blind delay, absolute timing, and accumulated variable delay. Next, we explain these methods briefly.

#### Blind Delay

The AAL of a receiver starts to read the first cell at the arrival time of it plus  $Q_{max}$  as shown in Figure 2.2<sup>1</sup>. Let  $d_1$  denote  $D_v$  of the first cell. The following cells are read at the  $T$  interval. For all cells, it is assured that  $D_T = d_1 + Q_{max} \geq Q_{max}$ . Therefore, the condition (2.1) is satisfied. The calculation of  $D_T$  of this method is very simple and any complex facilities are not necessary. However, the obtained  $D_T$  will be longer than the ideal value  $Q_{max}$  because of  $d_1$ . The unnecessary increment of  $D_T$  gives a growth of a cell delay and required memory.

#### Absolute Timing

This method is based on the assumption that both a sender and a receiver use the same global clock and a synchronization of two terminals is established. A sender sets the first cell emission time into the AAL header, then a receiver reads the cell at the tagged time plus  $Q_{max}$  and  $D_f$  as shown in Figure 2.3. Then, all other cells are read at the same interval  $T$ . In this method,  $D_T = Q_{max}$  is guaranteed for all cells and the condition (2.1) is satisfied. From the viewpoint of a delay, a memory cost, and a simplicity of the control, this method is ideal. However, the synchronization of both terminals seems to cost much.

#### Added Variable Delay

This technique is to actually measure the variable delay of the first cell. The variable delay is caused in queueing facilities, so ATM switches or ATM cross connect nodes calculate the queueing delay of the

<sup>1</sup>The fixed delay  $D_f$  is omitted in Figure 2.2-2.4.

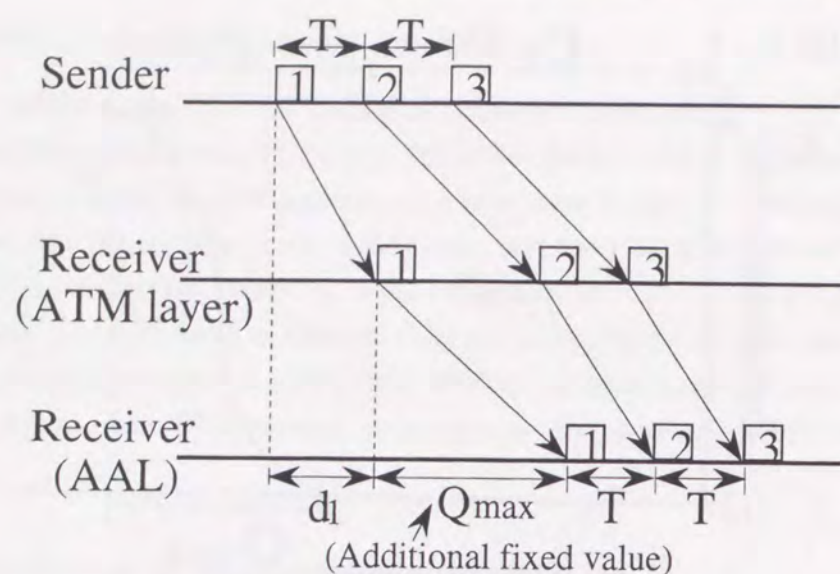


Figure 2.2: Blind delay mechanism.

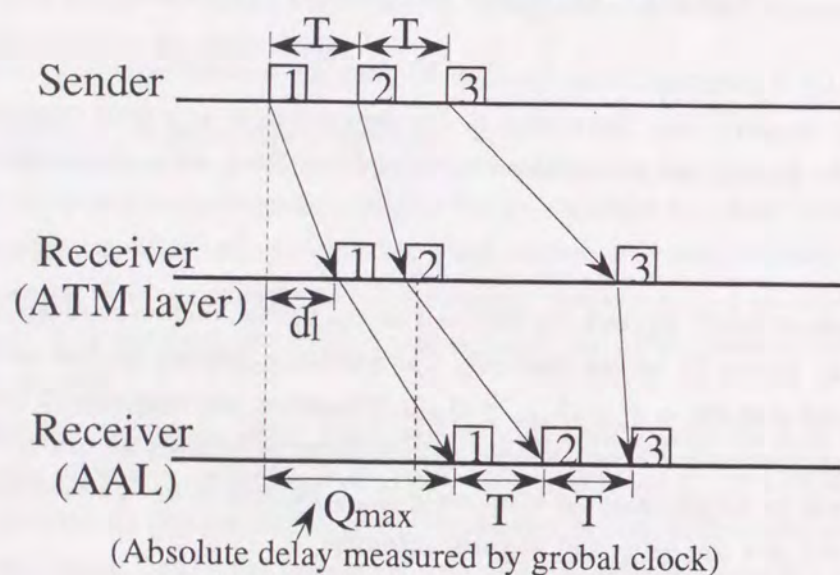


Figure 2.3: Absolute timing mechanism.

first cell and adds the value to a time stamp in the AAL header. As a result, a receiver can understand  $d_1$  correctly and determines the additional delay for the first cell as  $Q_{max} - d_1$  as shown in Figure 2.4. The following cells are read at the  $T$  interval. Like the absolute timing method,  $D_T = Q_{max}$  is assured for all cells. Though this also shows the ideal performance, the complex additional function is necessary for each ATM switch and cross connect.

In order to guarantee the cell loss rate caused at receiver buffers, all of three methods described above require the information for the cell delay distribution exemplified in Figure 2.1 for each connection. However, it is usually difficult to obtain the distribution at any instance. Moreover, the required memory at a receiver will continue to increase rapidly because the number of connections which are simultaneously connected to the same terminal will grow. If the cell delay jitter is bounded like Distributed Queueing Dual Bus (DQDB) [92], these two problems are improved and the delay jitter

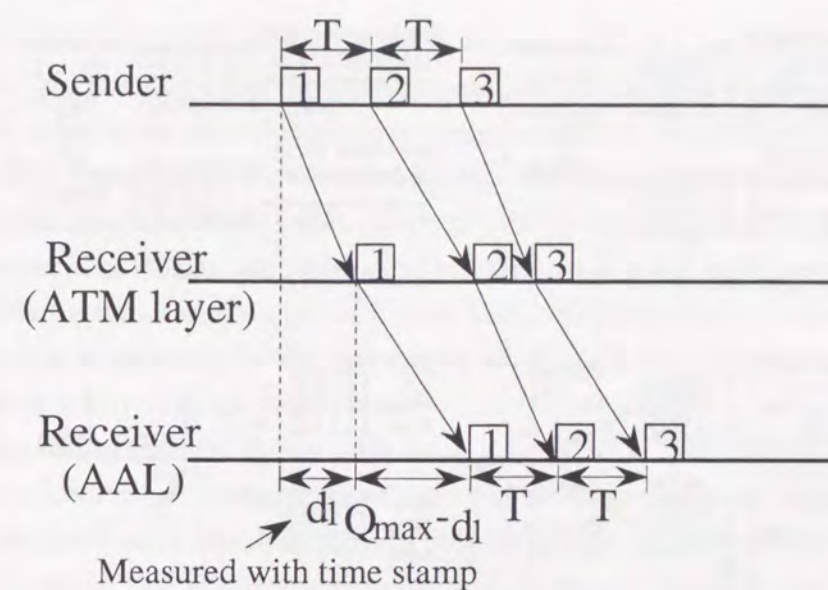


Figure 2.4: Added variable delay mechanism.

compensation on AAL 1 will become reasonable [93].

### 2.3.2 Buffer Priority Control

Isochronous services have various QOS requirements, e.g. an admissible end-to-end cell loss probability is  $10^{-8}$  for video communication and  $10^{-3}$  for telephony [36]. If the cells from all services are handled in the same manner, the resource management of the ATM network must be carried out according to the QOS requirements of the most demanding services (the second problem described in section 2.2). Moreover, congestion caused among ABR services will affect CBR (VBR) services (the fourth problem described in section 2.2). To solve these two problems, a buffer priority control [26, 32, 33, 34, 35, 36, 37] has been considered to be efficient. Buffer priority controls are classified into two categories: a delay priority and a loss priority (space priority). The former mainly gives preferential delay treatment, while the latter provides preferential loss treatment to high priority calls [35]. Next, we describe some buffer priority control schemes.

The delay priority schemes perform a priority control by means of a server scheduling as shown in Figure 2.5(a)-(d). Some delay priority schemes have been proposed, e.g. an absolute priority [78, 79], a Minimum Laxity Threshold (MLT), a Queue Length Threshold (QLT) [32], and a Periodical Bandwidth Allocation (PBA) [34]. The absolute priority gives an absolute priority to the isochronous traffic (corresponding to the high priority class in general). In other words, the error-free traffic (corresponding to the low priority class in general) are served only when there is no cell in the high priority class queue as shown in Figure 2.5(a). Although this scheme is simple, the QOS of the low class cells seem to be more degraded than other schemes.

MLT gives priority to the isochronous traffic when the Minimum Laxity (ML) of the isochronous cells<sup>1</sup> is less than or equal to a threshold,  $L$ ; otherwise priority is given to the error-free traffic as depicted in Figure 2.5(b). QLT gives priority to the error-free traffic when the number of queued

<sup>1</sup>It is defined as the amount of time until the first deadline of all queued isochronous cells expires.

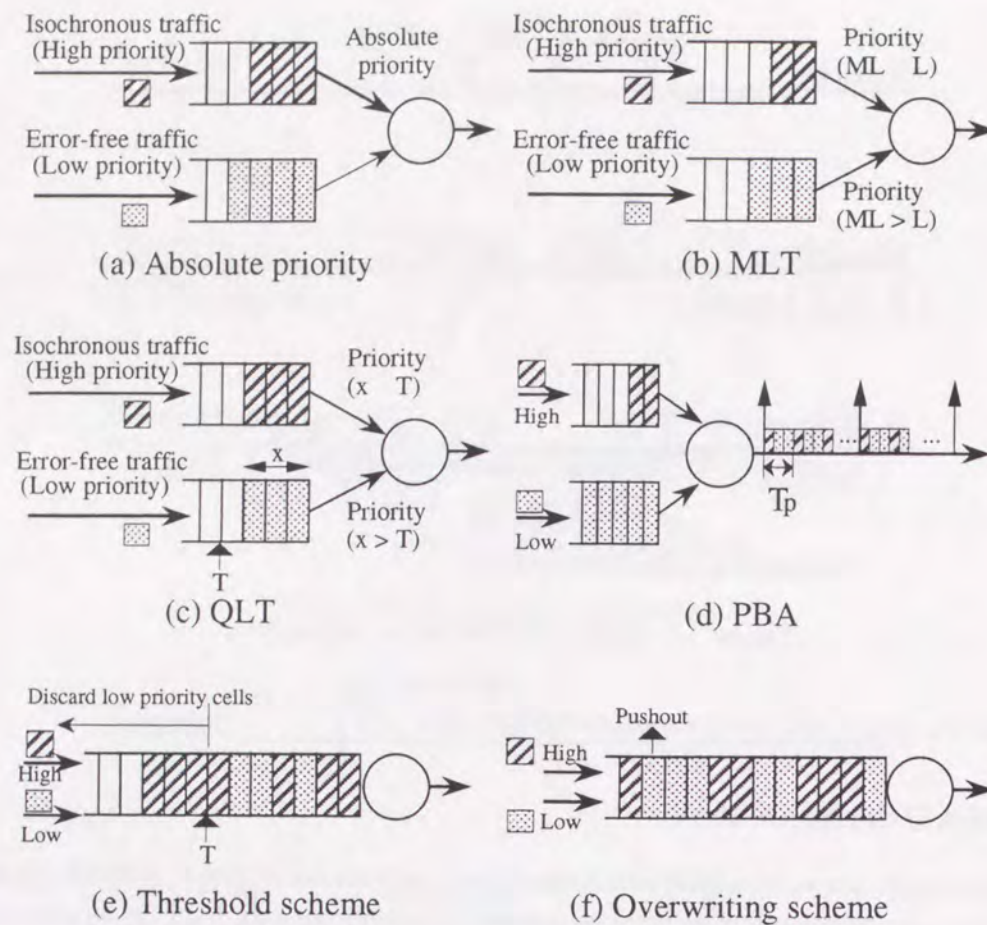


Figure 2.5: Buffer priority control methods.

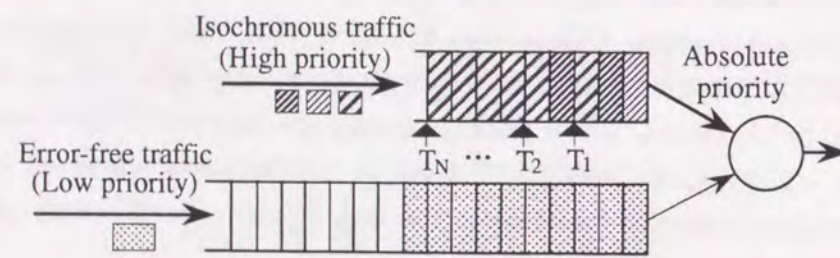


Figure 2.6: Structure of NTCD-MB.

error-free cells is above a threshold,  $T$ ; otherwise isochronous cells are given priority as shown in Figure 2.5(c). Both MLT and QLT achieve essentially the same performance tradeoff which is better than the absolute priority [32]. MLT requires a complex calculation to obtain ML, so QLT seems to be the best method among these three schemes. The upper limit of the delay jitter for an isochronous service can not be guaranteed by the absolute priority, MLT, or QLT.

In order to realize this assurance and decrease the influence on the error-free traffic, PBA selects isochronous cells periodically as depicted in Figure 2.5(d). The transmission period of the isochronous traffic,  $T_p$  is determined dynamically to guarantee all isochronous cells to be transmitted in  $T$ . In other words,  $T_p$  is derived from  $T_p = T/N(T)$ , where  $N(T)$  is the number of isochronous cells arrived during  $T$  period. The difficulty of the scheduling algorithm weakens the attraction of this method.

In the loss priority(space priority), e.g. a threshold scheme [35, 37, 80] and an overwriting scheme [35, 37], an error-free cell is dropped(dropped information can be recovered by retransmission) and its buffer space is given to an isochronous cell to avoid congestion. All cells are queued into the same buffer provided some thresholds in the threshold scheme. When the queue length exceeds the threshold  $T_i$ , all arrived cells of class  $i$  to  $N$  ( $N$  is the number of priority classes) are dropped as shown in Figure 2.5(e). In the overwriting scheme, an isochronous cell arriving at a full buffer can be replaced with an error-free cell arriving earlier as depicted in Figure 2.5(f). Although the threshold scheme is simple, a complex processing is necessary for the overwriting scheme. On the other hand, the performance of the latter scheme is better than the former one.

The loss priority control can not reduce a cell delay jitter of isochronous traffic. If only the delay priority mechanism is introduced, however, the efficiency of isochronous service accommodation becomes worse because the most strict required cell loss rate is applied to all isochronous services. Therefore, a Nested Threshold Cell Discarding with Multiple Buffers(NTCD-MB) has been proposed [33]. NTCD-MB combines the delay priority(absolute priority) and the loss priority(threshold scheme); all isochronous cells which consist of plural priority classes are inserted to the high priority buffer and all error-free cells are queued in the low priority buffer as shown in Figure 2.6. The high priority buffer is always given the priority to the low priority buffer as the absolute priority, and each priority class made in isochronous services are treated as the threshold scheme within the high priority buffer. This scheme satisfies both two purposes of the buffer priority control: the prevention of the congestion propagation from ABR to CBR(VBR) and the increment of the acceptable number of isochronous services.

Though the buffer priority control can solve the second and the fourth problems described in section 2.2, introducing this control is not enough to satisfy the all requirements of isochronous services. The problems are listed as follows.

- The delay jitter is not bounded except for the PBA method.
- The third problem explained in section 2.2, i.e. single stage and large scale ATM switch architectures cause a cell collision at output ports, is out of this control. In order to guarantee the cell loss rate for isochronous services, this contention must be considered.
- A buffer priority control applies the QOS guarantee to whole cells constituting one priority class. For example, when  $10^{-9}$  cell loss rate is guaranteed for one isochronous priority class, one connection of this class may experience  $10^{-8}$  cell loss rate while another connection of the same class experiences  $10^{-10}$  cell loss rate. In order to guarantee QOS for each connection on the buffer priority control, a buffer has to be provided for each connection and connection based priority control is necessary. A fair queueing approach [81] is one example to guarantee QOS for each connection based on the buffer priority control. However, a complex control and large memory is necessary, and the queueing delay increases in this case.

### 2.3.3 Stop-and-Go Queueing

In this section, we explain the stop-and-go queueing [38, 39, 40, 41, 42] which aims at the perfect avoidance of cell loss caused by a buffer overflow and the restriction in an intranetwork delay jitter.

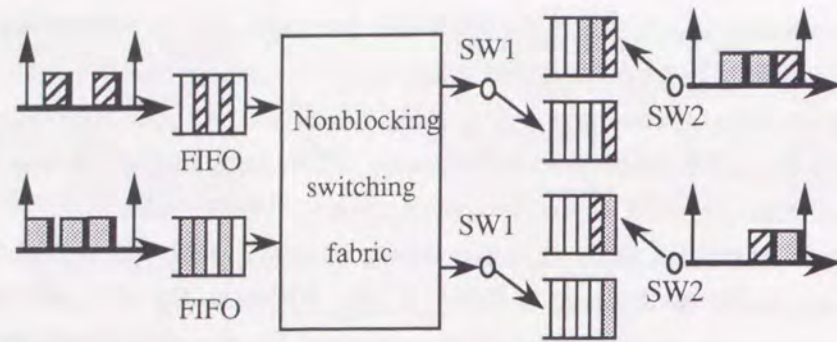


Figure 2.7: Stop-and-Go queueing strategy.

This method resolves the second and the fourth problem mentioned in section 2.2. Moreover, the assurance of the upper limit of a delay variance responds the first problem partially: makes it simple to recover CBR timing at the AAL 1 of receivers(see section 2.3.1).

This scheme consists of two strategies, an admission policy and a stop-and-go queueing. It assumes a frame, whose length is  $T$ , in a time axis. In the admission policy, each call is accepted based on the maximum number of cells which can be transmitted during a frame  $T$  with respect to all links on the route. By only this strategy, it is impossible to guarantee no cell loss at each intermediate node because each source tends to make a burst on random position. To prevent a buffer overflow, the stop-and-go queueing is introduced. In this control, all cells arriving during one frame time are stored at an intermediate node, and then transmitted to the next node. The stop-and-go queueing keeps the number of cells transmitted during the frame less than or equal to the maximum number determined by the admission policy. In order to simplify the frame-based queueing, a switch architecture has been proposed [42]: two buffers are provided for each output link as shown in Figure 2.7. This is the same structure of a double buffer method on a digital switch. Arrived cells are stored into one buffer and cells are transmitted to the output link from the other buffer simultaneously. The roles, i.e. reading and writing, are exchanged at each frame boundary. The stop-and-go queueing assumes a frame-based synchronization, so a buffer is attached in front of a switching fabric to realize this synchronization. The amount of this synchronization buffer is the proper value for each input link and less than the frame length.

By both strategies, cell losses caused by the buffer overflow at each intermediate node are prevented, and all cells are transmitted with bounded intra-network delay jitter within one frame. This scheme, however, can not remove cell loss caused by the output port contention at a switching fabric(the third problem described in section 2.2).

The end-to-end(from the source to the destination) delay,  $D$  is

$$D = Q + \tau + d, \quad (2.2)$$

where  $Q$  is a constant delay caused by a buffering,  $\tau$  is a propagation delay, and  $d$  is a fluctuation of the delay caused by the statistical multiplexing. At all intermediate nodes, additional buffering delay for synchronization of frames from different links is necessary, which is bounded by  $T$ . Thus, we have

$$nT \leq Q \leq 2nT, \quad (2.3)$$

where  $n$  is the number of intermediate nodes on the route of the corresponding call. Since  $Q \gg \tau$  and  $0 \leq d < T$ , the end-to-end delay and the width of intra-network delay jitter are proportional to  $T$ . So, the longer  $T$  leads to the greater network delay. However, the shorter  $T$  is, the worse the flexibility of bandwidth allocation becomes, because each call is allocated the bandwidth by means of the number of cells within one frame. Here, we summarize the demerits of this scheme.

- The queueing delay is much longer than other methods if it preserves the flexibility of bandwidth allocation.
- It is impossible to avoid a delay jitter perfectly in this scheme, so other method which recover CBR timing is necessary.
- The cell collision within the ATM switching fabric can not be avoided, thus non-blocking fabric(e.g. the input-output switch, the output switch, and the shared memory switch) should be introduced if it tries to guarantee a cell loss free transmission.

## 2.4 Quasi-STM Transmission Method

Here, it is efficient to consider the allocation of cell transmitted positions for each isochronous call on the ATM network because a time slot reservation resolves all four problems mentioned in section 2.2 without any complex processing during cell transmission. In other words, the ATM time slot allocation for each call has three merits. First, even if any type of the ATM switching fabric is used, the collision of cells at the output ports have never occurred by means of time scheduling. Second, a cell delay jitter is prevented in a network because the cell transmitted positions are determined exactly whole the network. Thus, a CBR receiver becomes simpler. Third, the distribution of a cell arrival interval is controlled by means of the slot allocation algorithm, so we can moderate burstness of isochronous traffic by using some sophisticated slot allocation algorithms.

We propose the new method named as Q-STM [47, 48, 49]. The main features of the proposal method are summarized as next three items.

- (1) All Q-STM calls are allocated fixed time positions in a frame to transmit cells over all links on the routes. Thus the switching of time slots at each intermediate switch is needed.
- (2) The period of time switching is not the frame which is the period of bandwidth allocation, but the subframe which is composed by splitting a frame into the same time interval.
- (3) In addition to the Q-STM service class, a normal ATM service class without frame concept is composed in order to accommodate high bursty calls efficiently and improve link utilization. Calls with high burst or relative tolerance of a cell loss, i.e. error-free services(data communication), are suitable in this service class. Hence, there are two different types of cells, Q-STM cells and ATM cells, on a link.

In the following four subsections, the frame structure, the ATM service class, the switch architecture, and the call setup procedure are explained respectively. After explaining the fundamental frame concept of the Q-STM method, we describe the aim and meaning of the subframe introduction by



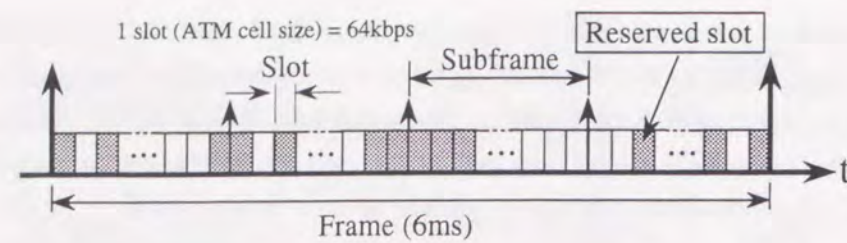


Figure 2.8: Q-STM frame structure.

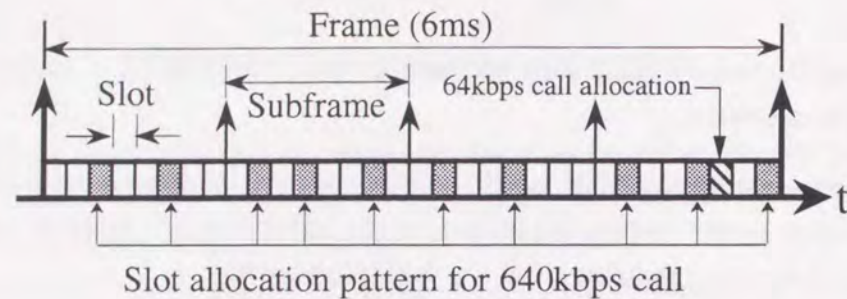


Figure 2.9: Example of the slots allocation.

means of comparing some alternatives in the frame structure subsection. In the ATM service class subsection, the meaning of this service class is explained. We summarize the requirements to realize the Q-STM switch, then compare some switch architectures in the switch architecture subsection. Finally in the call setup subsection, some algorithms are proposed and investigated qualitatively.

### 2.4.1 Frame Structure

#### Fundamental Concept

In order to allocate transmitted cell position on the ATM network, it is necessary to introduce a frame and a slot concept on a time axis: a frame is a period of bandwidth allocation and a slot is a unit of bandwidth allocation. For example, the frame length is  $125\mu\text{s}$ , which corresponds to a sampling period of a voice source, and the slot length is  $8\text{bits}$  in the conventional STM network. It is convenient to set the slot length equal to the amount of information transmitted from the lowest rate service during a frame period. In this case, reserving one slot per one frame just corresponds to the allocation of the lowest rate service. In the ATM network, the time slot synchronization has already established; one time slot is equal to the ATM cell length. Because the Q-STM method is based on the ATM network and cell-based switching, it is efficient to set the slot length as the ATM cell size. Moreover, we assume that the lowest rate isochronous service accommodated into the Q-STM service class is  $64\text{kbps}$  voice service. It takes  $6\text{ms}$  to make one cell from  $64\text{kbps}$  source because the ATM cell payload is  $48\text{bytes}$ <sup>1</sup>. As mentioned later, the queueing which is three times of the frame length is necessary at the maximum for each node. When the call passes several nodes, the queueing delay will be longer than the limit permitted for isochronous services. For example, a per switch cell transfer delay should be below  $500\mu\text{s}$  for services such as DS-1/DS-3 circuit emulation [12].

<sup>1</sup>Actually, one byte of the ATM cell payload is reserved for AAL 1. For the sake of a calculation convenience,  $48\text{bytes}$  cell payload is assumed to be used for user information in this thesis.

The longer a frame is, the better the flexibility of bandwidth allocation becomes because bandwidth of each call is assigned in the form of the number of cells in a frame. From viewpoints of delay performance, the shorter frame size is preferable because a frame is stored for time switching at each node. To satisfy above two conflicting requirements, the Q-STM method introduces a new time frame concept named as "subframe". Therefore, this scheme uses a frame structure consisting of three layers, "the frame", the "subframe", and the "slot", as shown in Figure 2.8. Time switching is executed on the subframe basis, that is composed by splitting one frame into multiple equivalent time intervals. A time table whose period is the subframe length is prepared for each subframe. The referred table is switched at each subframe boundary. The number of subframes within one frame (or the subframe length) is an interesting parameter because it affects many qualities in the Q-STM network. We roughly obtain the most efficient number through some quantitative evaluations in section 3.3.3.

The bandwidth allocation is performed by reserving required number of time slots within the frame. It should be noted that one call can be allocated slots over plural subframes. In Figure 2.9, we show the example of the Q-STM slot allocation where the bandwidth are  $64\text{kbps}$  and  $640\text{kbps}$ . When the link speed is  $156\text{Mbps}$  and one slot is equivalent to  $64\text{kbps}$ , the number of slots in a frame is about 2200 ( $\frac{48 \times 8}{6.4 \times 10^4} \times \frac{1.56 \times 10^8}{53 \times 8} \approx 2200$ ). In this example, the number of subframe is 4, so the number of slots in a subframe is about 550. It is too difficult to show 2200 slots in the figure, so the number of slots in the figure is less than actual frame.  $64\text{kbps}$  is assumed to be the slowest call, so the frame length is  $6\text{ms}$  as mentioned before. For the call of  $640\text{kbps}$ , 10 slots should be allocated. These allocated slots can be placed anywhere in a frame.

Next, we mention how to insert Q-STM cells transmitted from each source. At the entrance point of the Q-STM network, arriving Q-STM cells are queued for each connection, then inserted to the allocated slots. The Q-STM network is defined between the sender end office and the receiver end office. Thus, this entrance point is located at the sender end office. As a result, the Q-STM frame structure is not introduced on the upstream subscriber line (from the sender terminal to the sender end office). On the other hand, the Q-STM frame concept is provided on the downstream subscriber line (from the receiver end office to the receiver terminal) as shown in Figure 2.10. Each Q-STM call can transmit cells in any slots if they are reserved for the call. There is no delay variance within the Q-STM network after the transmitted slot is determined at the sender end office. The Q-STM source terminal can not send cells exceeding its bandwidth. Consequently UPC is realized constructively for Q-STM calls.

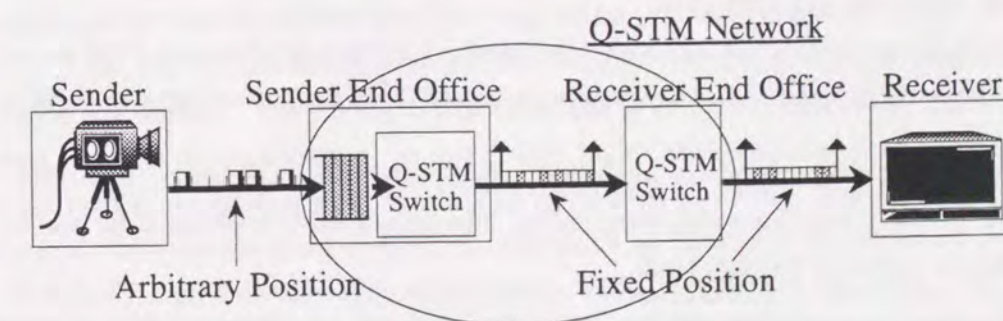


Figure 2.10: Bounds of the Q-STM network.

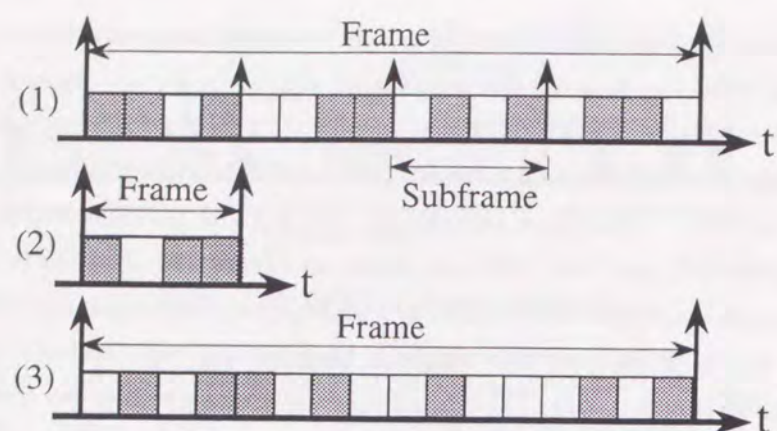


Figure 2.11: Comparison of the frame concept.

### Meaning of Subframe Introduction

We describe the significance of the subframe concept by comparing with two cases without subframes. Here,  $n$  indicates the number of subframes within one frame. As shown in Figure 2.11, the following three models are considered.

- (1) Introducing the subframe concept, and making the subframe a time switching period (proposed Q-STM method corresponds to this case)
- (2) Without the subframe concept, matching the frame length with the subframe length of the first case
- (3) Without the subframe concept, matching the frame length with the frame length of the first case

The three cases are compared from the three viewpoints: (A) a flexibility of bandwidth allocation<sup>1</sup>, (B) a buffering delay caused in a time switch (it is proportional to the amount of required memory), and (C) a required call setup time.

#### [Comparison between (1) and (2)]

The flexibility of bandwidth allocation of (1) is  $n$  times as large as that of (2). The buffering delay and the required time switch size of (1) are same as those of (2). When the same amount of bandwidth is allocated, the number of reserved slots of (1) is  $n$  times as large as that of (2).

#### [Comparison between (1) and (3)]

The flexibility of bandwidth allocation and the required number of allocating slots are same for (1) and (3). The time switching delay and its memory size of (3) is  $n$  times as large as those of (1).

Judging from above comparison, the availability of the subframe introduction is evident. However, there is a fear of the growth of a call setup time. The quantitative evaluation for the Q-STM call setup time will be shown in section 3.4.2.

<sup>1</sup>Bandwidth is allocated by reserving some time slots within one frame. The minimum interval of bandwidth which can be accommodated is *one slot/one frame*. Therefore, the longer the frame length is, the more the flexibility of bandwidth allocation becomes.

### 2.4.2 ATM Service Class

The Q-STM method introduces a normal ATM service class which has no frame concept in addition to the Q-STM service class. Thus, both Q-STM and ATM cells are transmitted on a link in mixed state. By introducing this service class, we obtain following effects.

- (1) The services with very high burstiness or tolerance for cell loss can be accommodated efficiently.
- (2) The slots which are not used by Q-STM calls can be used by ATM class cells, so they are not kept by Q-STM and we can obtain a statistical multiplexing gain from them.

In general, isochronous traffic is accommodated in the Q-STM service class and error-free traffic is supported in the ATM service class. When VBR call is supported as the Q-STM class, the vacant cell position inside the allocated slot may occur because of the rate fluctuation of the source. ATM cells are allowed to be inserted in these spaces in addition to the slots which are not allocated for Q-STM calls. By this strategy, even though time slots are reserved for each Q-STM call, we can obtain the statistical multiplexing gain and improve the utilization of the link. This is not derived from the conventional STM network.

Now, Q-STM cells has a complete priority in assigned slots, so ATM class cells can be regarded as low priority cells. Thus, the QOS of the ATM service class are greatly affected by the distribution of allocated slots and the characteristics of the Q-STM traffic. In the Q-STM method, the distribution of Q-STM cells within a frame can be controlled by means of the slot allocation pattern. The degradation of the ATM service class QOS is moderated by scattering reserved slots position within the frame. Therefore, the Q-STM call setup algorithm is important. We discuss this matter in section 2.4.4.

### 2.4.3 Switch Architecture

A Time switch (T-switch) which executes time switching of slots is necessary in the switch for the Q-STM scheme. In this subsection, we investigate and compare some switch architectures for the Q-STM scheme. Then, the cell switching motion inside the switch is explained briefly.

#### Basic Assumption

In order to realize the virtual STM transmission on the ATM network, it is necessary to introduce the concept of the frame, which is a period of bandwidth allocation, and the slot, which is a unit of it, like the ordinary STM network. When heterogeneous services requiring various bandwidth are accommodated, plural number of slots must be assigned for one call. Therefore, a Time Slot Sequence Integrity (TSSI) [82, 83, 84] becomes a problem like N-ISDN. TSSI is to maintain a cell sequence for a call allocated plural slots. The double buffer structure is useful to resolve this problem, so it has been adapted to many digital switches. In the double buffer structure, two T-switches are provided: information is read from one and written to the other at the same time. The function is switched at the boundary of the time switching period (i.e. the frame in STM and the subframe in the Q-STM method). The Q-STM method also adopts the double buffer structure to maintain TSSI easily.

Although only T-switch can construct the switching facility, it is efficient to combine T-switch with a Space switch (S-switch) to built a large scale switch. Among some combination of both switches,

a TST structure, providing two T-switches at the both sides of S-switch, has been considered to be the best one from the viewpoint of a scalability [85, 86]. The Q-STM method also adopts the TST structure like many digital switches.

When the TST structure is introduced, the call blocking caused by intra-switch congestion must be considered. In the intra-switch congestion state, a call blocking occurs because of an intra-route shortage, even if there is enough available slots on all passing links. Figure 2.12(a) exemplifies the intra-switch congestion. Now, let consider establishing a new connection, whose bandwidth is *one slot per frame*, from the input link 1 to the output link 2. Though there is empty slot on both links, this new call can not be accepted because the intra-route must set at the same time position on both ends. Therefore, the intra-blocking is a major cause of a Q-STM call blocking compared with the outside blocking (the shortage of empty slots on links). In order to avoid the intra-blocking, the following two methods have been investigated [87, 88, 89, 90, 91].

#### (1) Reassignment of Intra-Route

As shown in Figure 2.12(b), a new slot assignment is possible from the input link 1 to the output link 2 if pre-reserved intra-routes are reallocated [88, 89, 90]. The reserved slot positions do not change, so each switch can reallocate intra-routes without any influence to other switches. Although plural trials are necessary in general, it is proved that the reassignment process finishes in the finite frequency [88]. Moreover, the scheme which limits the number of reallocations has been proposed [91] because the reassignment requires plenty processing.

#### (2) Increment of Multiplexing Degree on S-Switch

Let  $n$  and  $m$  denote the number of slots during one frame on T-switch and S-switch respectively. If  $2n - 1 \geq m$  is satisfied, the intra-route blocking must not occur [89]. The worst allocation pattern is depicted in Figure 2.13 when  $m = 2n - 1$ . The worst case is that the reserved intra-route positions of the input-side are perfectly different from those of the output-side. When there is one empty slot on both input and output link, the number of blocked intra-route is  $(n - 1) + (n - 1) = 2n - 2 = m - 1$ ; so there is at least one available intra-route and no intra-route blocking happens. In order to satisfy  $m = 2n - 1$ , it is necessary to double both the amount of T-switches and the cycle speed of S-switch.

As described in section 2.4.1, the growth of the call setup time seems to be problem in the Q-STM

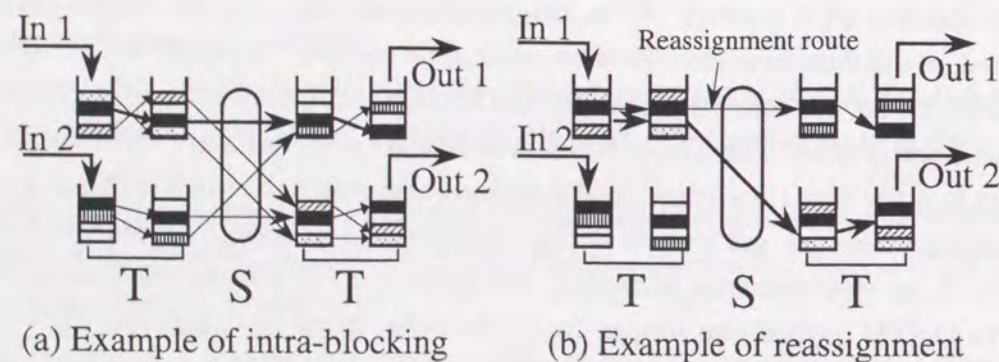


Figure 2.12: Example of the intra-blocking and its reassignment.

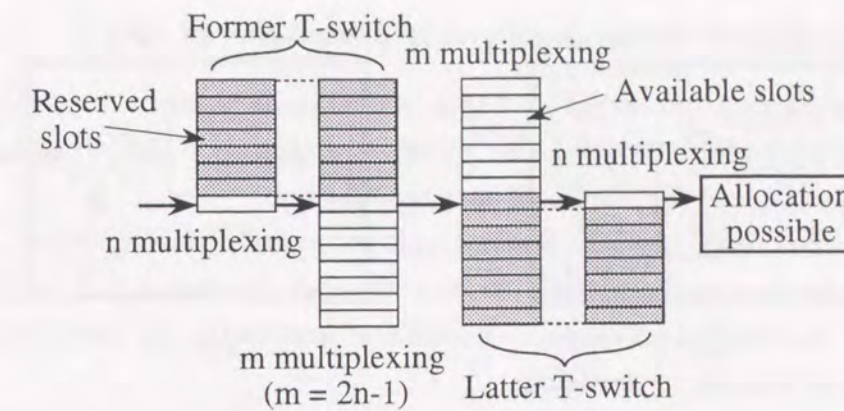


Figure 2.13: Increment of the multiplexing degree on S-switch.

method. The reallocation approach requiring a huge amount of processing will not be suited. On the other hand, the amount of T-switch is decreased by introducing the subframe concept. Moreover, the Q-STM method enables it to use any type of single stage ATM switching fabric because the cell output port collision is avoided by the time scheduling. Consequently, it is relatively easy to increase the switching speed of S-switch, so the Q-STM method assumes to employ the method (2) to avoid the intra-switch blocking. Next, we show one numerical example in order to understand the effect of introducing the method (2) more clearly.

Figure 2.14 shows the effect of the intra-blocking avoidance. The horizontal axis is the Q-STM load and the vertical axis is the Q-STM call blocking probability. The comparison models are

(Normal) the case without any mechanism avoiding the intra-blocking ( $m = n$ ),

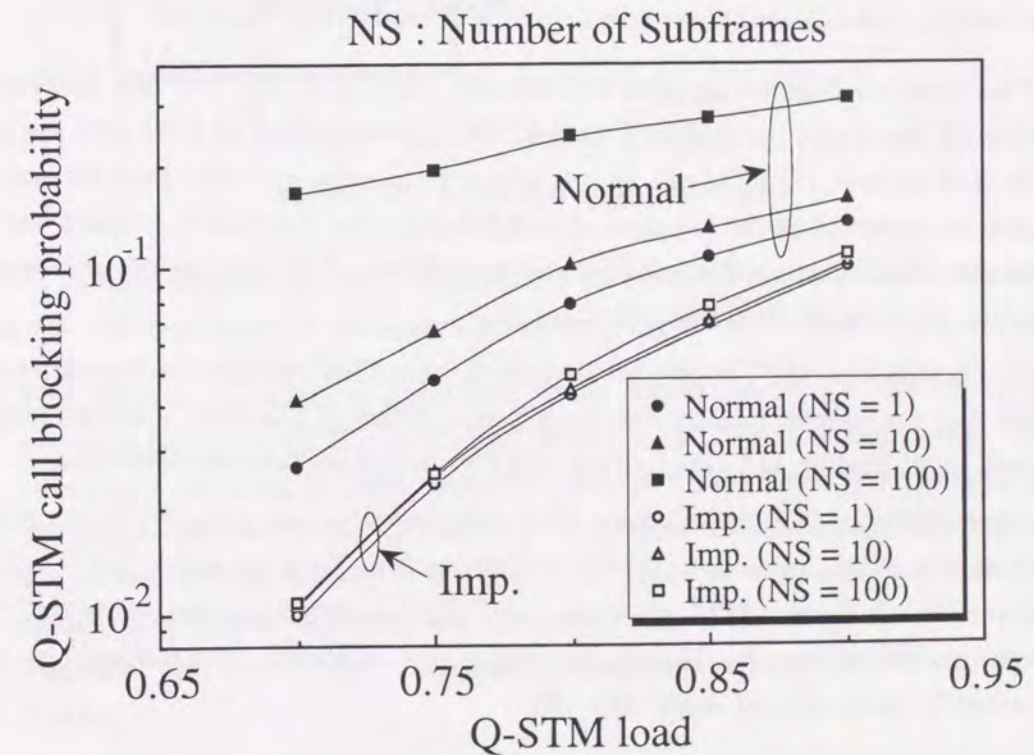


Figure 2.14: Q-STM call blocking probability with or without intra-blocking.

(Imp.) the case increasing the multiplexing degree on S-switch( $m = 2n - 1$ ).

The call level simulation model described in chapter 3 is used. It is assumed that the link capacity is 156Mbps, the frame length is 2200slots, the Q-STM bandwidth is 44slots/frame, the number of input(or output) links is 4, and the number of passing nodes is 3.

In the case of Normal, both the intra-blocking and the outside blocking occur. In the case of Imp., on the other hand, only the outside blocking happens. In Figure 2.14, Imp. shows much better performance than Normal. Therefore, the effect of introducing the intra-blocking avoidance mechanism can be seen strongly in the figure.

In general, the smaller the multiplexing degree on S-switch is, the more the inconsistent position becomes. So the Q-STM call blocking probability of the Normal case degrades with the number of subframes increases as shown in Figure 2.14. As a result, the avoidance of the intra-blocking is important for the Q-STM method which introduces the subframe concept.

Next, we investigate some switch architectures, then explain the cell switching mechanism briefly.

### Comparison of Architecture

It is assumed that the switch consists of three portions, an input module, an output module, and a switching fabric.

#### (1) Input Module

The function of the input module is to receive cells which consist of Q-STM and ATM cells, then to synchronize the subframe period and to exchange a time position for Q-STM cells. A synchronization buffer is necessary to establish the subframe synchronization. For the structure of this module, the following three alternatives are possible(see Figure 2.15(A)-(C)).

- (A) This structure does not separate Q-STM cells from ATM cells. Not only Q-STM cells but also ATM cells are inserted to T-switch. The time switching of ATM cells are performed by slots without a Q-STM cell, so it is necessary to make up a time table for non-allocated slots to maintain the cell sequence of an ATM call. This structure is simplest but the delay quality of ATM cells is degraded because each ATM cell experiences the unnecessary delay in the synchronization buffer and T-switch.
- (B) In this structure, Q-STM cells are separated from ATM cells and the separation continues till they are inserted into the switching fabric. Although two input ports are necessary for each input module, the delay quality of ATM cells shows the best performance.
- (C) After separating Q-STM cells from ATM cells, this structure stores ATM cells in a First-In First-Out(FIFO) queue. The Q-STM cell stream from T-switch is observed; when an empty slot is found, the top ATM cell waiting in FIFO is inserted into the empty slot. The most complex facility requires, however, one input port is enough. The influence on ATM cells is smaller than (A) and larger than (B).

#### (2) Output Module

The function of this module is to execute the time switching for Q-STM cells again(because the

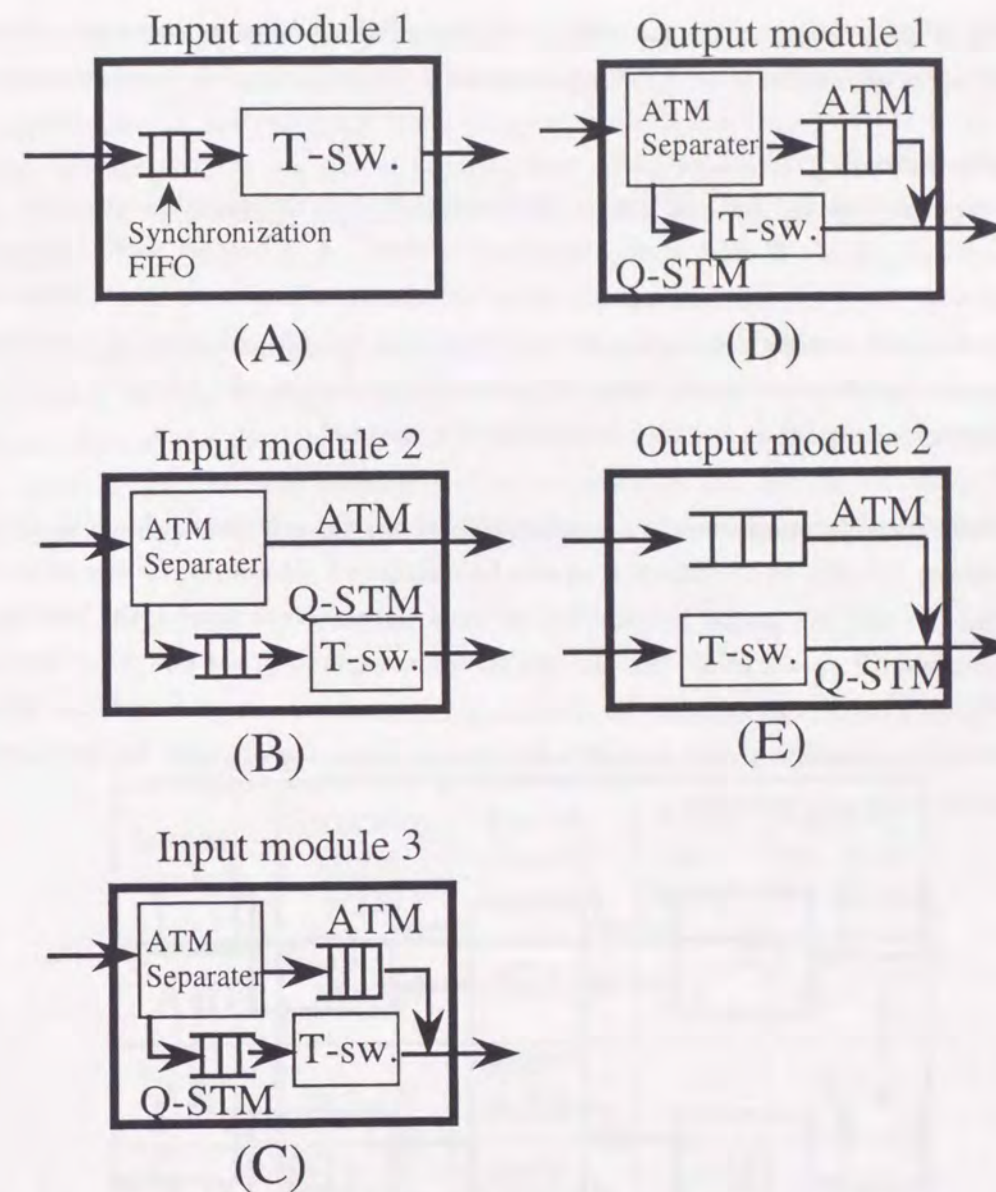


Figure 2.15: Input and output module.

Q-STM method supposes the TST architecture) and insert ATM cells to the slot without a Q-STM cell. The candidates of this module is the following two structures(see Figure 2.15(D),(E)).

- (D) This structure provides one input port to the output module(i.e. the output port of the switching fabric). Q-STM cells are separated from ATM cells in the module. Though this structure is attractive from the viewpoint of the switching fabric scale, some priority mechanism is necessary to avoid the output port collision of Q-STM cells. The time scheduling guarantees that the number of arriving Q-STM cells at the same output port simultaneously is less than or equal to one. Therefore, even if the switching fabric capacity is so small that only one cell can be accepted at the same time, the Q-STM cell collision can be avoided.
- (E) In this structure, two input ports to the module are provided: the one is for Q-STM cells and the other is for ATM cells. The construction is simpler than (D) and the probability

of ATM cell collision at the output port of the switching fabric is decreased. And also, no avoidance mechanism for Q-STM cell collision at the switching fabric output port requires.

(3) Switching Fabric

In order to avoid the Q-STM cell loss, a nonblocking type switching fabric requires. If a multistage switching fabric is used, some scheduling method, i.e. a batcher sorting networks [67], is necessary to avoid the internal cell blocking. On the other hand, any single stage switching fabric can be used because the number of Q-STM cells arriving at the same port simultaneously is less than or equal to one. From the viewpoint of the simplicity and the delay performance, a single stage switching fabric is suited for the Q-STM method.

The Q-STM switch architecture can be constructed from any three input modules(A)-(C) and any two output modules (D),(E), so six alternatives can be considered. Moreover, for the combination of the input module(B) and the output module(E), not only the structure sharing the switching fabric for both service classes(Figure 2.16(a)) but also the structure separating the switching fabric for each service class(Figure 2.16(b)) can be built. In the separating version, the switching fabric attached for the Q-STM service class needs no cell header information. Thus, the ordinary highway switch used for the S-switch of STM can be used.

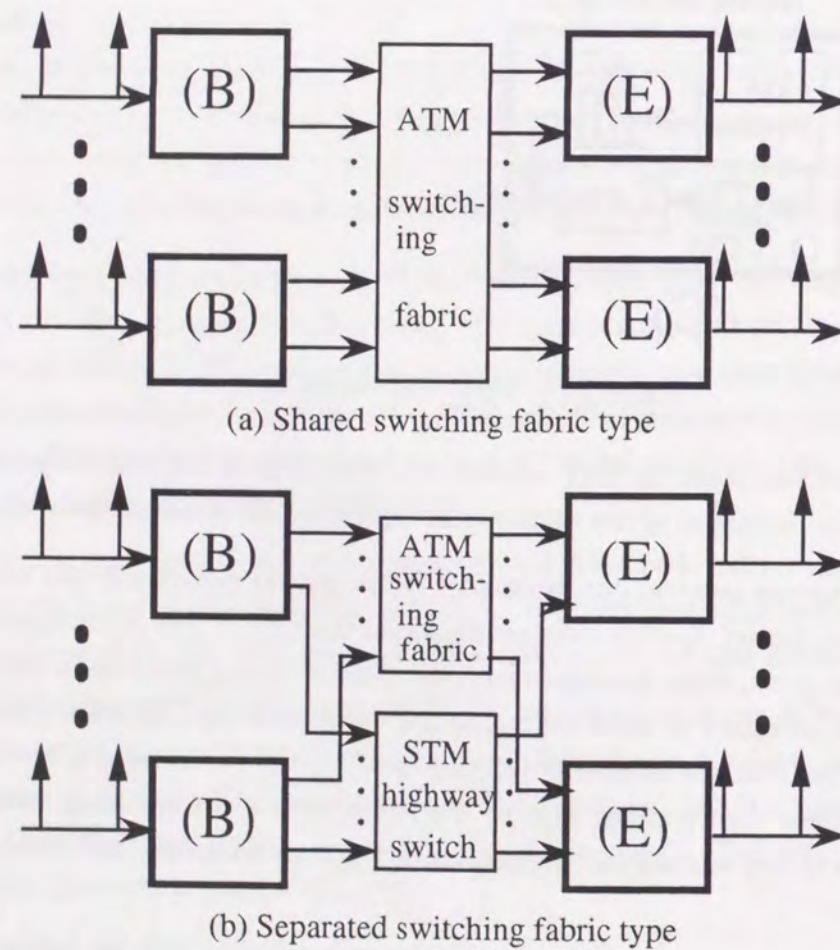


Figure 2.16: Comparison of the switching fabric for (B)-(E) type.

The seven switch architectures are summarized in Table 2.2. The processing speed of the switching fabric is assumed to be  $L$  times as fast as the links capacity. If the number of ATM cells arriving at the same output port of the switching fabric simultaneously is less than or equal to  $L$ , no ATM cell is lost at the output port. In the case of adopting the output module(D), the guaranteed number of ATM cells accepted at the same time decreases just one cell because one Q-STM cell may arrive at the same port.

Though the scale of the switching fabric becomes large, the combination of (B) and (E) gives a simple processing and the best performance for ATM cells. We proceed the following descriptions on the assumption of the (B)-(E) type switch architecture. It is supposed that single stage ATM switching fabric is used, so both sharing type and separating type for the switching fabric are the same structure logically. For the sake of the simple description, we assume the shared type (B)-(E) structure.

Table 2.2: Comparison of the Q-STM switch structure.

In-out module	Switching fabric scale	Priority control on ports	ATM cell delay	Capacity out.-port for ATM
A-D	$M \times N$	Necessay	×	$(L-1)^{*3}$
A-E	$M \times 2N$	Non-necessary	×	L
B-D	$2M \times N$	Necessay	⊙	$(L-1)$
B-E	$2M \times 2N$	Non-necessary	⊙	L
C-D	$M \times N$	Necessay	○	$(L-1)$
C-E	$M \times 2N$	Non-necessary	○	L
B-E <sup>*1</sup>	$2(M \times N)^{*2}$	Non-necessary	⊙	L

M : Number of input links N : Number of output links

L : Speed up ratio of sw. fabric to link capacity

\*1 Separation type of sw. fabric

\*2  $M \times N$  for each Q-STM and ATM

\*3 Number of ATM cells acceptable simultaneously

### Cell Switching Mechanism

Figure 2.17 shows the Q-STM switch architecture when the input module (B), the output module (E), and the shared switching fabric are used. ATM cells and Q-STM cells are separated at the input module and exchanged independently through the switch. These cells are combined on the output link at the output module. Thus, interaction between ATM cells and Q-STM cells is completely avoided.

Incoming cells to the input module are divided into ATM cells and Q-STM ones by the separator. It is assumed that the classification of the service class, i.e. the Q-STM class or the ATM class, is set for each connection. Therefore, the discrimination of cells is executed based on the routing bit in the cell header such as a Virtual Channel Identifier (VCI) or a Virtual Path Identifier (VPI). ATM cells are immediately inserted in the switching fabric and destined for the desired output port. On the other hand, Q-STM cells are queued into the synchronization buffer. Q-STM cells are delayed for a certain time at this synchronization FIFO. This FIFO is introduced to adjust the starting time of subframes for all incoming links by means of adding some synchronization delay, which is fixed value for each input module and less than one subframe length (see Figure 2.18).

Q-STM cells established the subframe synchronization are stored in T-switch, from which cells are read in the order set at the call setup time. The reading order is described in the cell scheduling table and managed by a controller. This method supposes the double buffer structure for T-switch, i.e. double buffers are prepared for the time switching. Arriving cells are stored into one buffer while the stored cells are transmitted from the other buffer. The functions of reading and writing are exchanged at the subframe boundary, that is the switch 1 (SW1) and SW2 in the figure shift at this boundary. The size of these buffers is equal to the subframe length, which is shorter than the one required by the stop-and-go queueing, i.e. the full frame length.

The scale of the switching fabric is  $2M \times 2N$ , where  $M$  is the number of input links and  $N$  is the number of output links. Two input ports are provided for each input link and two output ports are given for each output link. The one is for ATM cells and the other is for Q-STM cells. By means of the switching schedule for Q-STM cells, it is guaranteed that at most only one Q-STM cell can be transferred to a certain output port at a time. So most of single stage ATM switching fabrics, for

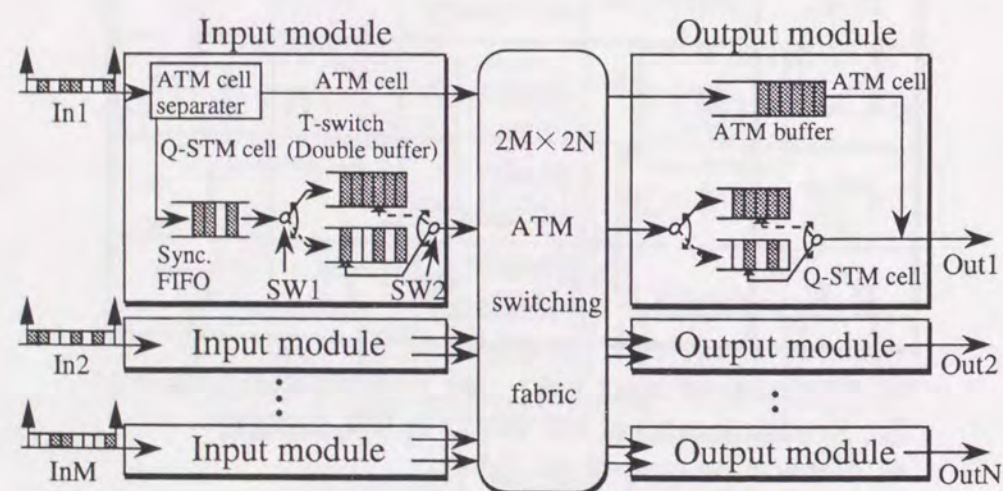


Figure 2.17: Q-STM switch architecture ((B)-(E) type structure).

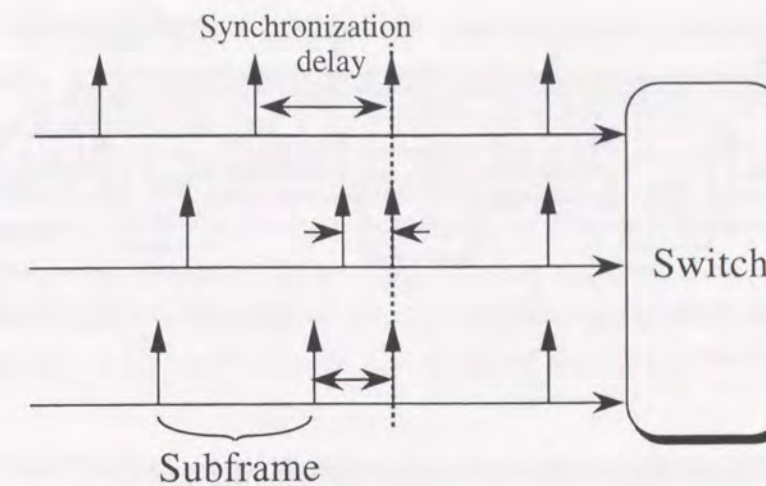


Figure 2.18: Delay to synchronize subframe.

example the knockout switch [73], can be used for this fabric without a Q-STM cell collision at the output port of the switching fabric.

ATM cells switched to the desired output port are stored in the ATM buffer, and Q-STM cells are again entered to T-switch, since the TST structure is assumed. ATM cells are inserted in the cell position which has no Q-STM cell without considering if it is in the allocated slot for Q-STM or not. So ATM cells can also use the vacant cell positions caused by the fluctuation of Q-STM rate. Therefore, a statistical multiplexing gain can be obtained even in the reserved slots; this merit has not been derived from the STM network.

#### 2.4.4 Call Setup

A new procedure of call setup is necessary for the Q-STM service class because time slots are allocated for each Q-STM call. In this subsection, we enumerate required conditions for the Q-STM call setup process and describe one example of the call setup proceeding. Then, some algorithms are proposed.

#### Required Conditions and Example of Call Setup Process

The conditions which must be satisfied to accommodate a Q-STM call are listed as follows.

- The number of slots allocated for a certain Q-STM call inside a certain subframe position must be identical among the subframes located at the same position on the all passing links as shown in Figure 2.19. The reason is that the period of a time switching is each subframe. Figure 2.19 shows an example when the number of subframes is 4, the number of reserved slots for a certain Q-STM call (whose bandwidth is  $22 \text{ cells/frame}$ ) is 6, 5, 5, 6 within the first, second, third, and fourth subframe position respectively.
- To satisfy above condition, a centralized office which determines the number of allocated slots within each subframe position is needed.
- After deciding the positions of reserved slots on each passing link, each office must decide an intra-route, which is a time switching position on the switching fabric for each incoming-outgoing

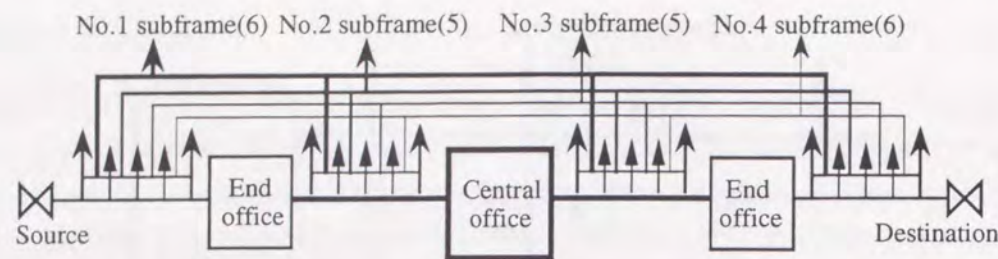


Figure 2.19: Restriction on the number of allocated slots in each subframe.

slots pair.

- Each office must know the positions of allocated slots on the links of both sides in order to determine the intra-route.

To clear the procedure required for Q-STM call setup, we show one example of the call setup process. Here, it is supposed that the centralized office, which determines how many slots allocate in each subframe position for each call, is the end office connecting the sender terminal.

**(i) Decision of the passing route**

A route(virtual path) candidate between source and destination is found by applying both the routing scheme and the connection admission control. If the candidate can not be found at all, this call is rejected.

**(ii) Report of the number of empty slots in each subframe**

As illustrated in Figure 2.20(a), the intermediate offices(namely the offices except for both end ones) report the number of empty slots in each subframe on the lower side link to the source end office(corresponding to the centralized office in this case). And the destination end office reports the same kind of information on the destination subscriber link, too.

**(iii) Recognition of the minimum number of empty slots for each subframe**

The source end office recognizes the minimum number of empty slots in every subframe position by means of the empty slots information which covers all links on the route. The source end office itself searches the information on the link between the source end office and the next intermediate office. The information on other links is obtained by (ii).

**(iv) Determination of the number of allocated slots inside each subframe**

The source end office determines how many slots are allocated to each subframe position in accordance with pre-offered algorithm(defined as *Process1*) by means of the information obtained in (iii). And the result is reported to all relayed intermediate offices and the destination end office.

**(v) Determination of the positions of allocated slots on each link**

As shown in Figure 2.20(b), the source end office and intermediate offices determines the position of allocated slots on the lower side link, in accordance with pre-offered algorithm(defined as *Process2*) according to the information obtained in (iv). The destination end office determines the same kind of position on the destination subscriber link. If another call is accepted during above process, the source end office(recalling this is the centralized office) uses wrong information about empty slots. So it is necessary to introduce some kind of an exclusive control.

**(vi) Cognition of the positions of allocated slots on upper side link**

All offices except for the destination end office report the information of the allocated slot positions to the next lower side office. In this step, each office recognizes the positions of allocated slots on upper side link as well as lower side one.

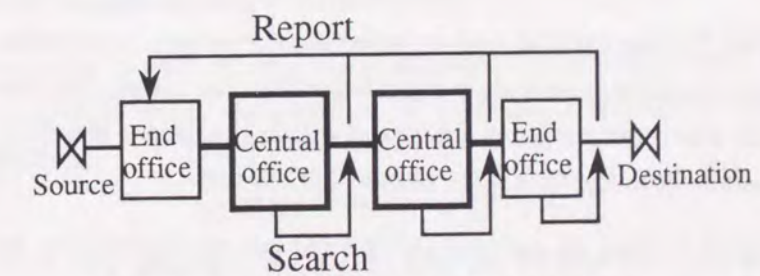
**(vii) Establishment of an intra-route inside each office**

Each office determines an intra-route(the time position on S-switch) independently using the pre-offered algorithm(defined as *Process3*). This transaction does not depend on and affect other offices. The source end office reports a completion of call setup process to source terminals, at once this process has finished even if it has not received a finish signal sent from other offices.

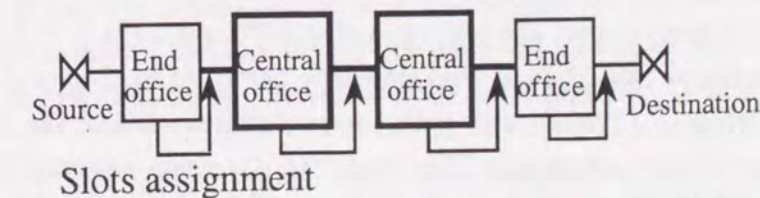
The Q-STM method needs three algorithms for the call setup: the calculation of the number of slots allocated within each subframe(*Process1*), the allocation of time slots for each link(*Process2*), and the assignment of the intra-route of each node(*Process3*). The Q-STM method accommodates the ATM service class traffic in addition to the Q-STM service class one. When we consider each call setup algorithms, therefore, the influence on the QOS of the ATM service class must be considered.

Before considering each call setup process, we roughly investigate the influence of the Q-STM slot reservation pattern on the ATM class QOS. If each Q-STM call is allocated time slots at the same intervals, the ATM class QOS will show the best performance. However, in order to make it possible, a special environment is to be assumed: (1)a homogeneous Q-STM source is accommodated, (2)the number of allocated slots within one frame is the submultiple of the slots number within one frame, and (3)the number of allocated slots within each subframe is the measure of the slots number of the subframe.

Therefore, we assume this special environment to show the general characteristics of the ATM class QOS to the Q-STM slot allocation pattern. The following three algorithms are investigated as the slots allocation pattern(containing the function of *Process1* and *Process2*).



(a) Report of empty slots information



(b) Decision of reservation slots in each subframe

Figure 2.20: Call establishment process.

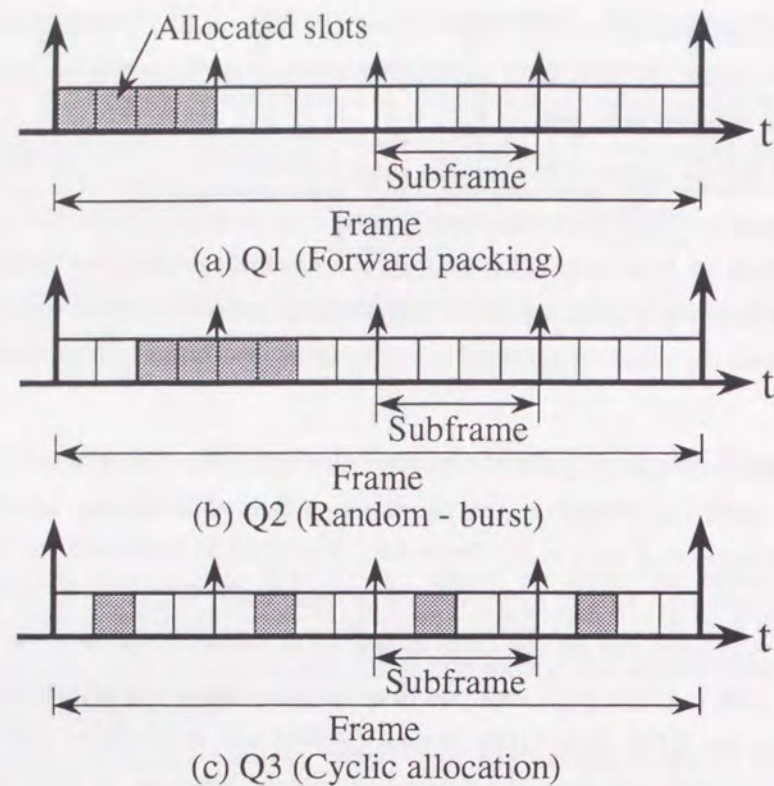


Figure 2.21: Q-STM slot reservation pattern.

(Q1) As shown in Figure 2.21(a), the subframe which locates the earliest position (the left side in the figure) is selected at first. Then, time slots are allocated from the selected subframe as many as possible. If the number of available slots within the subframe is not enough, then the subframe which is in the second earliest position is selected. The third, the fourth, ... subframes are chosen in the same manner. The slot position is randomly allocated within the selected subframe. As a result, allocated slots are centralized in the earlier part of the frame.

(Q2) All reserved slots for one Q-STM call are selected at continuous positions as shown in Figure 2.21(b). The head position is randomly allocated within the integer multiple positions of the Q-STM bandwidth. Allocated positions are spread within the frame. However, they are centralized in a certain position from the viewpoint of one Q-STM call.

(Q3) As shown in Figure 2.21(c), all slots for one Q-STM call are allocated at the same interval. The phase is selected randomly. This is the ideal case.

It is assumed that the number of input (or output) links is 8, the number of subframes is 11, the Q-STM bandwidth is  $44 \text{ slots/frame}$ , the load ratio of Q-STM and ATM is 5 : 3, and the ATM buffer size in the output module is 100. The cell level simulator described in chapter 3 is used.

Figure 2.22 shows the mean ATM cell intra-switch delay characteristics for the total load (Q-STM and ATM). Q3 shows much better performance than other two allocation patterns. Although Q2 scatters Q-STM allocated slot positions within a frame, the reserved positions for one call are centralized into a certain position. The performance of Q2 is worse than Q3, so it is important to decentralize slots allocated for one Q-STM call. The remained part of this subsection investigates three processes

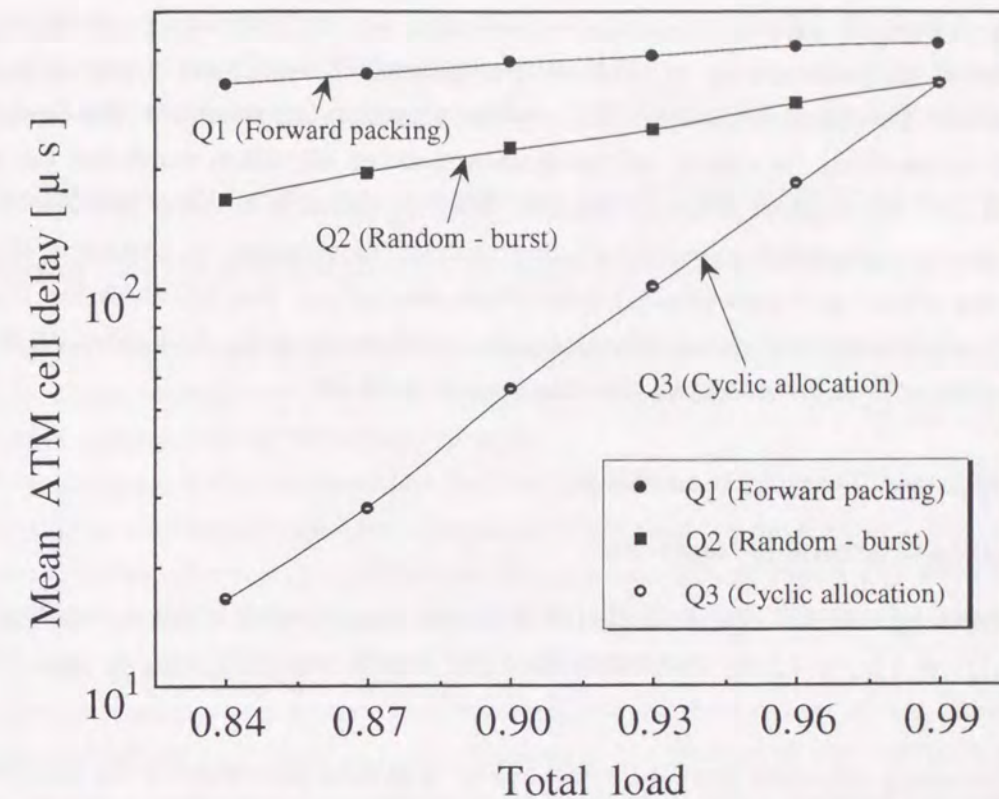


Figure 2.22: QOS of the ATM service class for various Q-STM slot reservation patterns.

considering this result.

#### Calculation of Allocated Slots Number within each Subframe (Process1)

The sender end office (the centralized node) determines the number of slots allocated for each subframe position from the information of the empty slots number for each subframe and each passing link. For *Process1*, following three conditions should be considered.

- (1) The maximum number of slots which can be allocated within subframe  $j$ ,  $avail(j)$ , is equal to the minimum number of empty slots within the subframe  $j$  through all passing links. This is represented as follows,

$$avail(j) = \min_{1 \leq i \leq h} \{emp(i, j)\}. \quad (2.4)$$

Here,  $h$  is the number of passing links,  $emp(i, j)$  is the number of empty slots within subframe  $j$  on the passing link  $i$ .

- (2) The imbalance of number of slots within a subframe reserved for Q-STM calls degrades the call blocking probability of the Q-STM service class and the QOS of the ATM service class. Therefore, it is desirable to balance the load of the accommodated Q-STM service class among subframes.
- (3) For each Q-STM call, it is superior idea to decide the number of allocated slots for each subframe as equally as possible. This is because that the burstiness of the traffic stream is moderated if a VBR source is accommodated as a Q-STM call.



The one straightforward algorithm is a random selection, i.e. the subframe in which one slot is assigned is selected randomly among all subframe positions which have some empty slots; and the selection is repeated for required number. This random algorithm is named as a *RanDom-1(RD-1)* for the sake of convenience. Moreover, we newly show another algorithm which has the possibility to satisfy above requirements in active manner. This algorithm is called a *Subframe Load and Allocated slot location Decentralization(SLAD)*, and basically corresponds to allocate a slot to the subframe position which has bigger  $avail(j)$  than others, one by one. Let  $M$  denote the Number of Subframes(NS),  $\omega(j)$  the number of slots allocated within subframe  $j$ , and  $\omega$  the bandwidth of Q-STM call( $slot/frame$ )( $\omega = \sum_j \omega(j)$ ). Next, we show the process of SLAD.

(SLAD-i) Calculation of  $avail(j)$  from  $emp(i, j)$

(SLAD-ii) Sorting of  $avail(j)$  in bigger order

(SLAD-iii) Denoting  $k = \omega - \lfloor \frac{\omega}{M} \rfloor \times M$  ( $\lfloor x \rfloor$  is a biggest integer which is not in excess of  $x$ ) and setting  $\omega(j) = \lfloor \frac{\omega}{M} \rfloor + 1$  (for  $k$  subframes from the biggest  $avail(j)$ ),  $\omega(j) = \lfloor \frac{\omega}{M} \rfloor$  (for other subframes)

(SLAD-iv) Blocking a call when there is (or are) one or more subframes which is (or are)  $avail(j) < \omega(j)$

Figure 2.23 depicts the example when  $h = 3$ ,  $M = 4$ ,  $\omega = 10$ . The numbers shown in subframes represent the number of empty slots. SLAD satisfies the condition(3), since the difference of  $\omega(j)$  among subframes for one Q-STM call is less than or equal to one. The condition(2) is also filled by means of selecting the subframe which has a bigger  $avail(j)$  to the one allocated one more slots. The efficiency of this algorithm is evaluated in section 3.3.1.

#### Allocation of Time Slots for each Link(Process2)

After being determined the allocated slots number for each subframe position, each passing node reserves time slots on the lower side link. We must consider the situation that the plural slots are allocated within a subframe for one Q-STM call. The literature [98] investigated plural slots allocation considering the accommodation of a  $n \times 64kbps$  call on the STM network. Assuming the single buffer structure, it considered the way of keeping TSSI and evaluated only the call blocking probability.

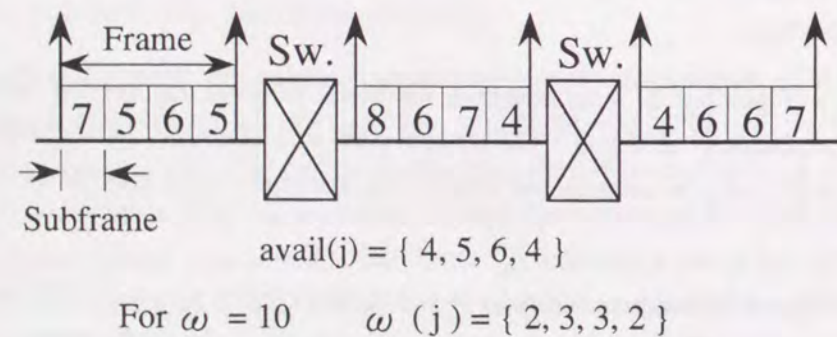


Figure 2.23: Example of SLAD.

On the other hand, the ATM service class which is transmitted without a time frame concept is multiplexed in the Q-STM method. Therefore, it is necessary to consider the QOS of the ATM service class when the way of slot allocation is investigated. Following should be considered for *Process2*.

- (1) Decentralization of time slot positions allocated for one Q-STM call within a subframe
- (2) Scattering time slot positions allocated for whole Q-STM service class within a subframe

When sources accommodated in the Q-STM service class send cells at the almost same interval, the requirement(1) can be neglected. However, algorithm which satisfies item(1) will satisfy item(2), too. Thus, we have only to consider the requirement(1).

A random allocation is also the candidate for *Process2*, we name this algorithm as a *RanDom-2(RD-2)*. Ideally, if time slots are allocated for a certain Q-STM call at the same interval, the requirement(1) will be most satisfied. However, it is difficult to allocate time slots in such a way when heterogeneous Q-STM calls are accommodated because each Q-STM call requires a different slot interval. Here, the algorithm which we call a *Standard Interval(SI)* is newly considered.

SI regards the ideal identical interval as a standard interval. As a matter of fact, the ideal identical interval can be realized only when  $\omega(j)$  is a measure of the number of slots within a subframe,  $H$ . Therefore, we use a table,  $intr(i, m)$ , which keeps information about standard intervals. When the standard position has already allocated for other Q-STM call, time slots around the position are searched. In advance, it is necessary to define the standard interval,  $intr(i, m)$ ,  $m = 1, 2, \dots, i$ , where  $i$  is the number of slots allocated in the subframe  $j$ , i.e.  $i = \omega(j)$ . When  $k = H - \lfloor \frac{H}{i} \rfloor \times i$ , we define for  $i > 1$ ,

- (A)  $intr(i, m) = \lfloor \frac{H}{i} \rfloor + 1$  for  $k$ 's,
- (B)  $intr(i, m) = \lfloor \frac{H}{i} \rfloor$  for  $(i - k)$ 's.

$k$  positions which corresponds to (A) are selected randomly. There is no need to define  $intr(i, m)$  for  $i = 1$ . Next, the process of SI is shown.

- (SI-i) Setting  $l = 0$  ( $l$  is the number of slots which have been already assigned for the tagged call)
- (SI-ii) Selecting one time slot position from subframe  $j$  randomly and setting  $s$  as the selected position
- (SI-iii) When the slot  $s$  is empty, allocating the position and going to (SI-vii), in other case, i.e. when the slot  $s$  has already allocated, setting  $d = s$ ,  $u = s$
- (SI-iv) Setting  $d = d - 1$  (when  $d = -1$ , setting  $d = H - 1$ ), then if the slot  $d$  is empty, allocating the slot and going to (SI-vii)
- (SI-v) Setting  $u = u + 1$  (when  $u = H$ , setting  $u = 0$ ), then if the slot  $u$  is empty, allocating the slot and going to (SI-vii)
- (SI-vi) Repeating (SI-iv) and (SI-v) until an empty slot is found
- (SI-vii) Setting  $l = l + 1$ , then if  $l < \omega(j)$ , setting  $s = s + intr(\omega(j), l)$  (if  $s \geq H$ , setting  $s = s - H$ ) and going to (SI-iii), in other case, i.e.  $l = \omega(j)$ , finishing this algorithm

By *Process1*, it is guaranteed that there is more than or equal to  $\omega(j)$  empty time slots in the subframe  $j$ , thus this algorithm surely stops after selecting  $\omega(j)$  slots. Figure 2.24 shows the example when  $H = 16$ ,  $\omega(j) = 3$ ,  $intr(3,1) = 5$ ,  $intr(3,2) = 6$ ,  $intr(3,3) = 5$ . By applying this algorithm for each  $M$  subframe, all required time slots are allocated. The efficiency of this algorithm is evaluated in section 3.3.2.

### Assignment of Intra-Route(Process3)

In this thesis, the input module (B) is assumed in order to explain the cell switching mechanism and evaluate some performances in the next chapter. Because the intra-route of Q-STM cells is completely separated from that of ATM cells. Thus, it is not necessary to consider the QOS of the ATM service class. The time position must be identical for both input and output sides, so a complex algorithm should be avoided. Therefore, we suppose a random algorithm for *Process3*.

It is assumed that the table registering the intra-route index which can be selected is used, in order to simplify the algorithm. After one available intra-route index is selected, the last available index in the table is moved to the selected position. The available intra-route is different for each combination of an input and output link, so the index table is necessary for each pair. Now, let consider the number of tables required to be revised when a new intra-route between the input link  $X$  and the output link  $Y$  is assigned. In this time, it affects the tables whose input link  $x$  and output link  $y$  are

- $1 \leq x \leq X_{max}$ ,  $x \neq X$  and  $y = Y$ , or
- $x = X$  and  $1 \leq y \leq Y_{max}$ ,  $y \neq Y$ ,

where  $X_{max}$  is the number of input links and  $Y_{max}$  is the number of output links. Therefore, the total number of revised tables is  $X_{max} + Y_{max} - 2$ . Next, we show a random algorithm which can be applied to *Process3*, named as an *Accordance-Type Random(ATR)*. Let  $emp(x,y,j,z)$  denote the available intra-route table where the input link is  $x$ , the output link is  $y$ , the subframe position is  $j$ , and  $z$  is the address in the table. ATR consists of two algorithms, the assignment of an intra-route(selecting one route from the table and the modification of that table) and the modification of other affected tables.

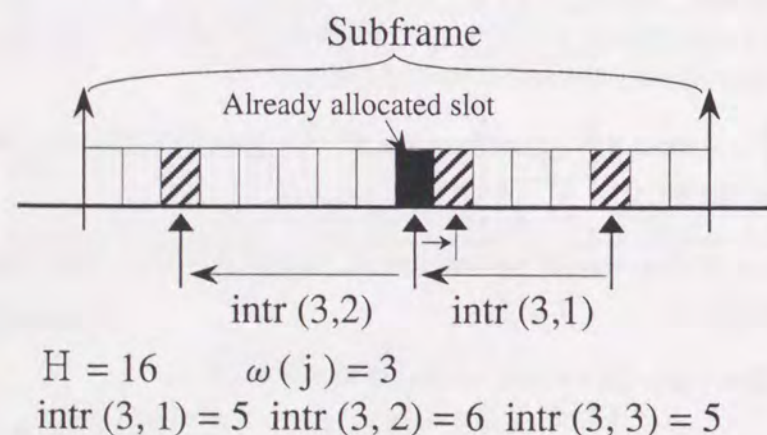


Figure 2.24: Example of SI.

First, we describe the ATR process except for the modification of other  $X_{max} + Y_{max} - 2$  tables.

- (ATR-1-i) Setting  $l = 0$  ( $l$  is the number of intra-route which have been already assigned for the tagged call)
- (ATR-1-ii) Selecting one intra-route among  $emp(X, Y, j, z)$  randomly
- (ATR-1-iii) Modifying the table  $emp(X, Y, j, z)$  (moving the last element to the selected position)
- (ATR-1-iv) Making a time table in the input and output module respectively, using the obtained intra-route index and the time slot position on both links
- (ATR-1-v) Increment  $l$  by one; if  $l < \omega(j)$  then going to (ATR-1-ii), otherwise finishing this algorithm

Applying this algorithm for  $M$  subframes, ATR completes the establishment of all required intra-routes.

Next, the modification process for other  $X_{max} + Y_{max} - 2$  tables affected by the intra-route assignment is explained (the process for the subframe  $j$  is shown as an example).

- (ATR-2-i) Setting  $l = 0$
- (ATR-2-ii) Eliminating the element  $k$  (assuming that the index of the  $l$ th intra-route is  $k$ ) from the table  $emp(x, y, j, z)$
- (ATR-2-iii) Increasing  $l$  by one; if  $l < \omega(j)$  then going to (ATR-2-ii), otherwise finishing this process

Applying this algorithm for each subframe and each combination  $x, y$  satisfying above conditions, the modification process is completed. Though ATR needs plenty of memory, no accordance process between input and output modules is necessary at the call setup time, i.e. the accordance process (modification of the intra-route table) can be performed after the call setup procedure finishes.

## 2.5 Conclusion

In this chapter, the QOS control required for isochronous services was described and three main techniques, the delay jitter absorption in AAL 1, the buffer priority control, and the stop-and-go queueing, were investigated. The time slot allocation on the ATM network is one of the most efficient method to guarantee the QOS of isochronous services. We proposed a virtual STM transmission on the ATM network, named as Q-STM method.

Q-STM introduces two new concepts into the ATM networks; three layered frame structure and time slot reservation. The frame structure of Q-STM consists of "frame", "subframe", and "slot". The frame is a period of bandwidth allocation like the STM network or the stop-and-go queueing. However, the subframe is a new concept that a unit of time switching at intermediate switching nodes. By introducing the subframe, the delay due to time switching is extraordinary reduced without losing the flexibility of bandwidth allocation. By reserving time slots for each Q-STM call, three notable merits are obtained. First, the cell loss at output ports of the ATM switching fabric due to a cell collision is prevented perfectly even if any single stage ATM switching fabric is used. Second, by allocating time

slots in scattered position over the frame, the burstness of Q-STM calls can be moderated. So the degradation of the ATM service class QOS can be moderated. And third, no cell delay jitter in the network can be easily achieved.

We also have showed a new switching architecture which is able to switch both Q-STM cells and ATM cells simultaneously. Moreover, we have collected the conditions which are demanded by the call setup procedure, and suggested one realization. The Q-STM call setup process is organized by three processes, the calculation of the number of slots allocated for each subframe(*Process1*), the slots reservation on each passing link(*Process2*), and the assignment of the intra-route of the switch(*Process3*). The SLAD algorithm was considered for *Process1*, SI for *Process2*, and ATR for *Process3* respectively.

The quantitative evaluations for each call setup algorithm and the investigation of the most efficient number of subframes are treated in chapter 3. The QOS of the ATM service class and the additional call setup time for the Q-STM call are also evaluated in next chapter.

## Chapter 3

# Performance Evaluation of Q-STM Method

### 3.1 Introduction

In the previous chapter, we proposed the Q-STM method which aims for the realization of cell loss free and delay jitter free transmission on the ATM network by allocating time slots for each call. In this chapter, (I)design issues of the Q-STM method are solved, then (II)an availability of this method are evaluated and clarified.

The Q-STM method has two design issues: (1)what Q-STM call setup algorithms are efficient and (2)how many subframes show the best performance.

Because the Q-STM method allocates time slots for each call, some researches for call setup schemes on the STM network serve as good references. In the STM network, objects of performance evaluation for call setup algorithms have been a call blocking probability and a number of processing steps [99]. As mentioned in chapter 2, the Q-STM call setup procedure consists of three processes: *Process1* is the calculation of the number of slots allocated within each subframe position, *Process2* is the slots reservation within each subframe on links, and *Process3* is the assignment of intra-routes in passing nodes. Since the Q-STM call blocking can happen at *Process1*, we must evaluate the call blocking probability for this process. However, this evaluation is not enough because the Q-STM network accommodates the ATM service class as well as the Q-STM service class. Since call setup algorithms affect the ATM class QOS, we must investigate this quality for both *Process1* and *Process2*. *Process3*, i.e. the ATR algorithm, is not evaluated because it gives no influence for any qualities in the assumed switch architecture.

In order to clarify the efficient algorithm of *Process1*, SLAD and RD-1 algorithms are compared for both qualities(the Q-STM call blocking probability and the ATM class QOS). The SI and RD-2 algorithms are also compared for the latter quality(the ATM class QOS) to obtain the available algorithm for *Process2*. The results are that SLAD and RD-2 is more efficient for each process.

The time frame concept of the Q-STM method consists of three layers, the frame, the subframe, and the slot. Though both the frame length and slot size have been already determined in the previous chapter, the subframe length(or Number of Subframes(NS) within one frame) has not been given. The subframe length affects three qualities, the Q-STM cell end-to-end delay, the Q-STM call blocking

probability, and the QOS of the ATM service class. The Q-STM cell delay decreases with the increment of NS. The more NS is, the worse the Q-STM call blocking probability seems to become. By evaluating these three qualities for various NS, we roughly obtain the most efficient NS, as around 100, in the assumed environment.

In general, communication qualities consist of five elements: the information error(or loss) ratio, the mean transmission delay, the transmission delay jitter, the call blocking probability, and the call setup time. The former three qualities are categorized as QOS mentioned before. In order to clarify the availability of the Q-STM method, all five qualities should be evaluated for each Q-STM and ATM service class.

The QOS of the Q-STM service class is guaranteed, hence we have only to investigate the call blocking probability and the call setup time for the Q-STM service class. On the other hand, the Q-STM mechanism gives no influence on these call level qualities for the ATM service class. We can easily reflect the influence of the Q-STM traffic load to the call setup of the ATM service class by means of subtracting the Q-STM load from a link capacity. Therefore, we have only to evaluate QOS for the ATM service class. The Q-STM call blocking probability is evaluated in the section studying the most efficient number of subframes. Consequently, the ATM class QOS and the Q-STM call setup time are matters of concern.

The ATM service class of this method corresponds to a low priority class. In general, a priority control degrades the QOS of a low priority class by improving the QOS of a high priority class [35]. We compare the QOS of the ATM service class with that of the low priority class on a Nested Threshold Cell Discarding with Multiple Buffers(NTCD-MB) method [33]. The number of priority classes in isochronous services is assumed to be one, so this buffer priority control corresponds to the absolute priority scheme [78, 79]. It is clarified that the degradation of the ATM class QOS is much smaller than the low priority class QOS of the absolute priority scheme.

We analyze the additional call setup time caused by introducing the Q-STM method, i.e. the processing time of SLAD, RD-2, and ATR. Each algorithm is fully defined to a machine cycle step level and required steps are calculated. It is obtained that the additional call setup time is negligible. As a result, the availability of the Q-STM method is clarified.

## 3.2 Simulation Model Formulation

Except the investigation of the Q-STM call setup time, we evaluate all qualities by computer simulations. At first, the simulation models are described.

### 3.2.1 Source Model

#### [Q-STM Service Class]

If a  $64\text{kbps}$  voice source, whose bandwidth is  $one\ cell/frame$ , is used, it is difficult to evaluate the efficiency of call setup algorithms. Therefore, the CBR moving picture(Indiana Jones 2 of [64]) source is assumed. The rate is  $6.4\text{Mbps}$  which corresponds to  $90\ cell/frame$  for  $6\text{ms}$  Q-STM frame. Hence, each Q-STM call is allocated 90 time slots within a frame. The sustaining time of each Q-STM call

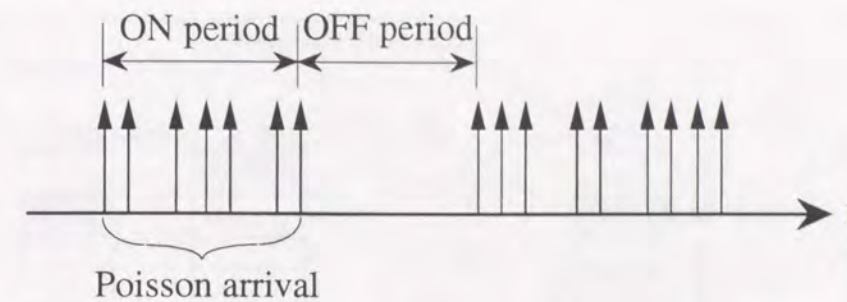


Figure 3.1: IPP model.

obeys the exponential distribution whose average is  $7200\text{s}$ , and the phase of CBR is decided randomly for each source and each Q-STM frame.

#### [ATM Service Class]

An Interrupted Poisson Process(IPP) is assumed as the traffic source model of data communication. Each source repeats two states, ON period and OFF period, as shown in Figure 3.1. The sustaining time of each state obeys the exponential distribution. During ON period, cells arrive as the form of the Poisson process. This model can represent the burstiness of error-free traffic. The average arrival rate during ON period is assumed to be  $10\text{Mbps}(141.5\ cell/frame)$  as the transmission rate of the Ethernet. We can set any value for the other two IPP parameters: the average rate and the average period. Here, it is assumed that the average rate is  $6.4\text{Mbps}(90\ cell/frame)$  which is identical with the Q-STM source, and the average period is  $33.3\text{ms}$ . The ratio of the period length between ON and OFF is  $16 : 9$ .

### 3.2.2 Simulation Model

Computer simulations managed in this chapter are classified into two models, (1)the call level one which mainly investigates the Q-STM call blocking probability and (2)the cell level one which mainly investigates the QOS of the ATM service class. Next, these simulation models are described.

#### [Call Level Simulation]

Many number of connections are multiplexed into one link in the actual network. As a consequence, the size of the simulation becomes huge if we try to emulate this kind of network faithfully. It follows from this that a simple model depicted in Figure 3.2 is assumed. This model generates Q-STM calls according to the Poisson distribution whose average is  $N\lambda$ . Each Q-STM call selects one link from  $N$  for each step. All Q-STM calls pass identical number of links,  $\zeta$ . As a result, each link is offered the identical load  $\lambda$ , so this is the approximated model when the network load is uniform. Now, the ATM service class is not considered because the traffic of this class offers no effect to the Q-STM call blocking probability.

The Q-STM method applies the TST structure for the time switch architecture as mentioned before, so there is a possibility of an intra-blocking at the call setup. The intra-blocking brings a call blocking even when there are enough empty slots on every passing links. In this simulation model, it is assumed

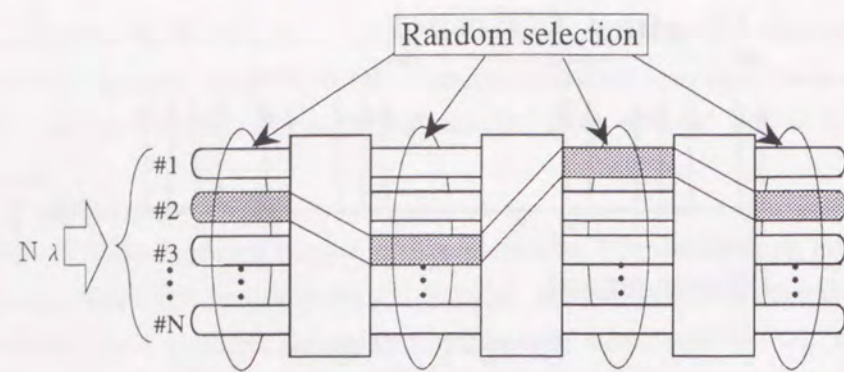


Figure 3.2: Call level simulation model.

that the intra-blocking is perfectly avoided by means of increasing the degree of multiplexing on the space switch as described in section 2.4.3.

#### [Cell Level Simulation]

Figure 3.3 shows the simulation model. The switch architecture is based on the (B)-(E) type and shared switching fabric described in section 2.4.3. The simulator has to produce cell stream arriving to the switch in order to simulate the action of cells inside the switch. The comparison models in section 3.4.1 are the Q-STM method, the absolute buffer priority, and a normal ATM. Hence, pre-offered module is attached for each model as shown in Figure 3.3(a)-(c).

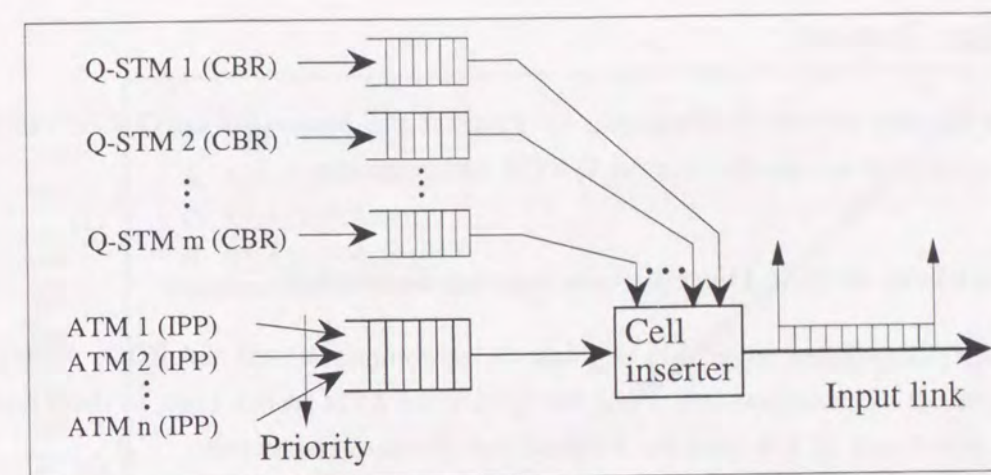
In the Q-STM method, time slots that each Q-STM call is permitted to transmit its cells are fixed for each call. As mentioned before, the Q-STM traffic is assumed to be CBR, so the bandwidth of each Q-STM call is allocated based on the average rate. As a result, Q-STM cells are inserted in all reserved slots in the pre-offered module. A single buffer is provided for ATM traffic, and each ATM cell is inserted into non-allocated slots as shown in Figure 3.3(a). When plural number of cells arrive at the pre-offered module simultaneously, the connection which has the smaller identified number is served faster.

In the case of the buffer priority scheme, one buffer is given for each priority class in the pre-offered module as shown in Figure 3.3(b). Low priority cells are served only when there is no high priority cells. On the other hand, one common FIFO is provided for the normal ATM as shown in Figure 3.3(c). All cells of both kinds of sources are stored in the same manner.

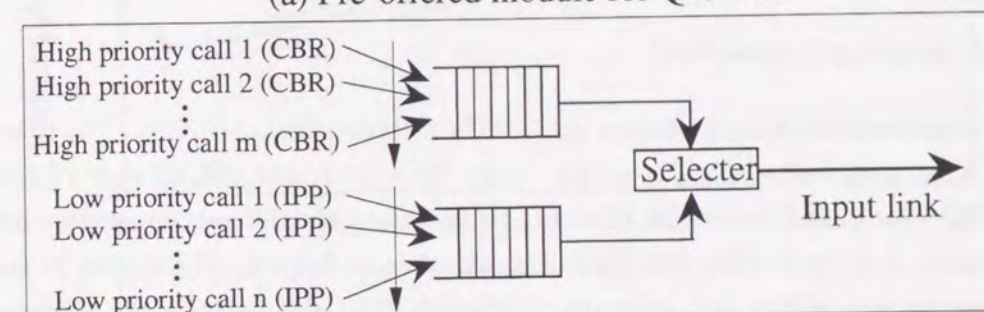
By the way, we apply a momentary slot allocation state of the call level simulator to a condition of reserved slots in this simulator. This condition of the allocated slots pattern is not changed during the cell level simulation. We apply 120 patterns and adopt mean value as the characteristics.

#### [Simulation Parameters]

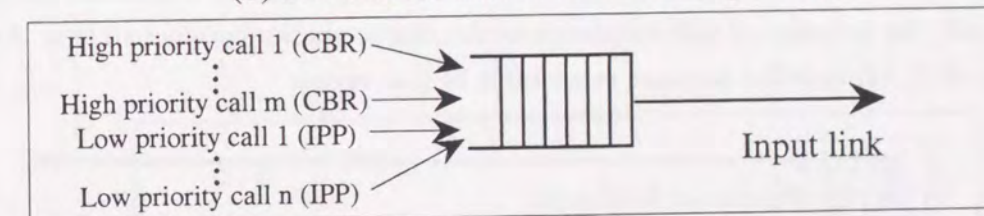
It is assumed that the link capacity is  $156Mbps$ , the frame length is  $6ms(2200\ slots)$ , the number of input(or output) links is 4, and the number of passing nodes is 3(this is applied for the call level simulation). The size of the ATM buffer offered in the output module is  $10000cells$ , and the load ratio between the Q-STM and the ATM is 1 : 1(these are applied for the cell level simulation). Because the



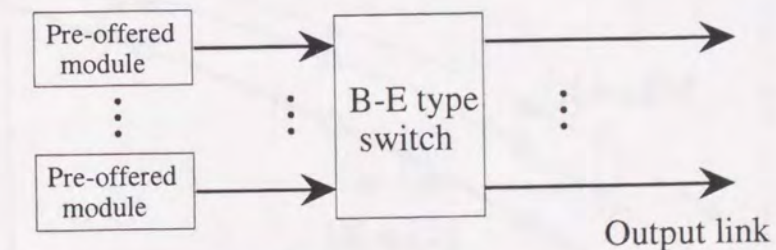
(a) Pre-offered module for Q-STM



(b) Pre-offered module for Buffer priority



(c) Pre-offered module for Normal



(d) Module construction

Figure 3.3: Cell level simulation model.

average rate of the Q-STM source and the ATM source is identical, the number of Q-STM sources multiplexed on one link is equal to that of ATM sources.

### 3.3 Design Issues

In this section, the best efficient (1)algorithms for *Process1* and *Process2* of the Q-STM call setup and (2)number of subframes are clarified for the Q-STM design issues.

#### 3.3.1 Algorithms of Slot Distribution among Subframe

In order to clarify the efficient algorithm of *Process1*, we compare SLAD and RD-1. *Process1* affects both the Q-STM call blocking probability and the QOS of the ATM service class, so these two qualities are evaluated. RD-2 and ATR is used for *Process2* and *Process3* respectively.

#### [Q-STM Call Blocking Probability]

The call level simulator is used to investigate the Q-STM call blocking probability. The characteristics against the Q-STM load is shown in Figure 3.4, when NS is 10 or 440. SLAD shows better characteristics than RD-1 for both NS=10 and NS=440. Furthermore, the difference is small when NS=10. On the other hand, it is large when NS=440. The reason is as follows. SLAD tries to equalize the number of allocated slots within each subframe. Although RD-1 also balances the subframe load on an average, there is some variance on the balance. In the case of large NS, this means the size of the subframe is small, the influence of this imbalance to the characteristics becomes serious. As a result, the superiority of SLAD to RD-1 becomes remarkable in that region.

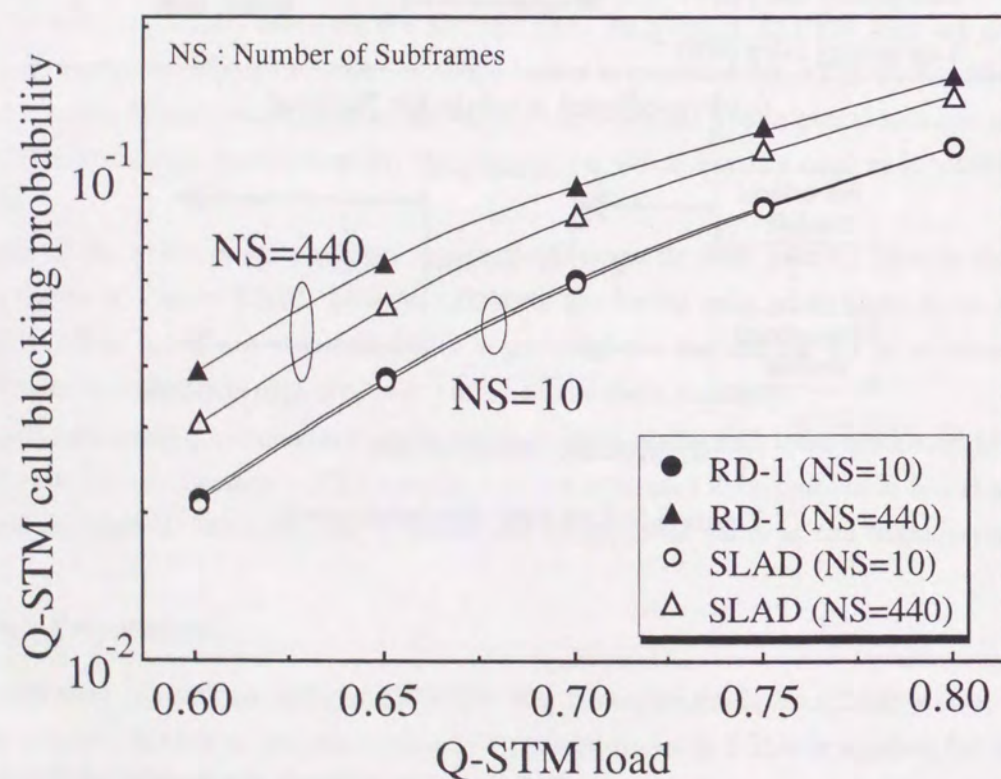


Figure 3.4: Characteristic of the Q-STM call blocking probability [Process1].

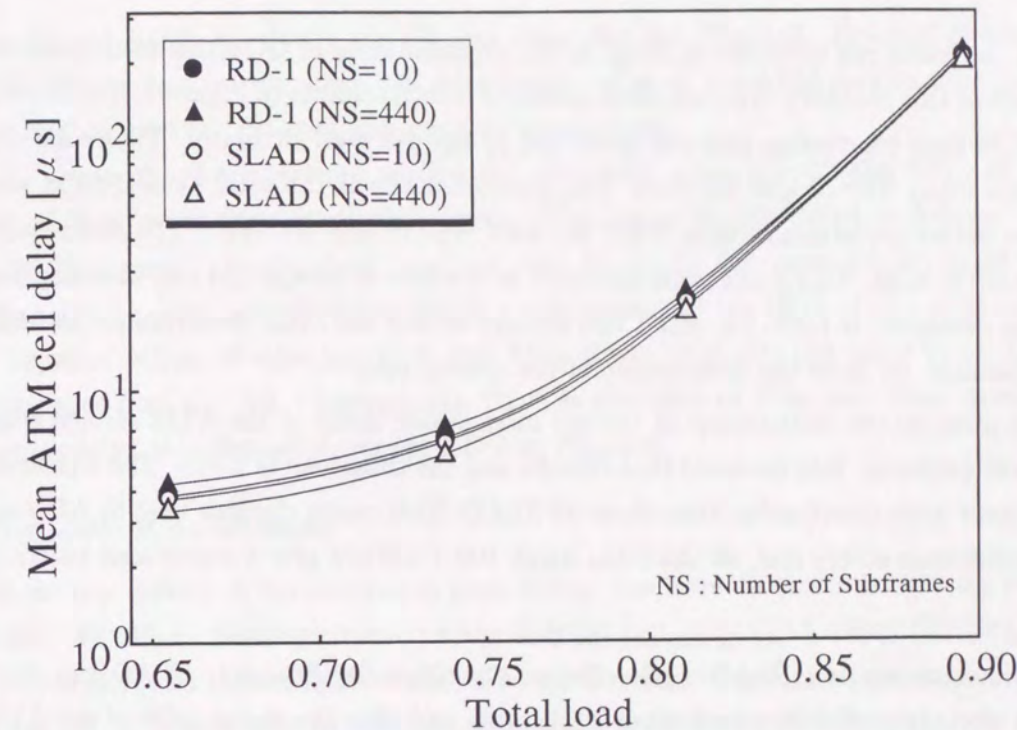


Figure 3.5: Characteristic of the mean ATM cell switching delay [Process1].

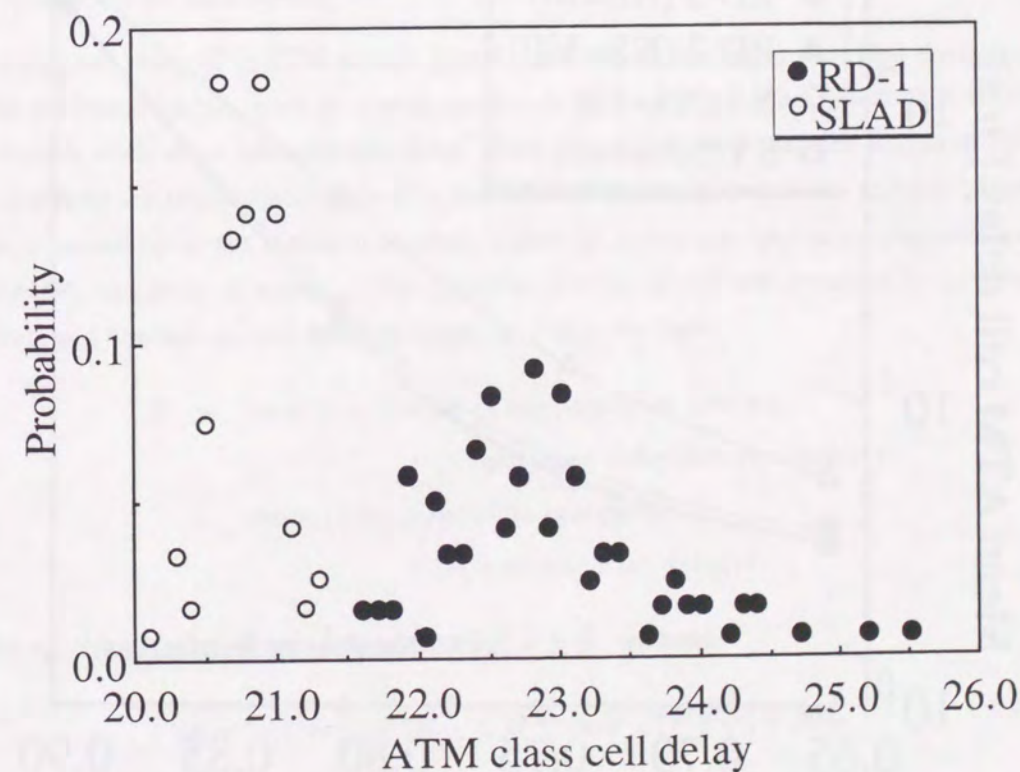


Figure 3.6: Distribution of the ATM cell switching delay [Process1].

## [ATM Service Class QOS]

We evaluate the mean cell intra-switch delay as the representation of QOS (this assumption is applied for whole part of this chapter). The cell level simulator which consists of Figure 3.3(a) and (d) is used for 120 Q-STM slots reservation patterns produced by the call level simulator. Figure 3.5 depicts the characteristics when NS=10 and NS=440. The horizontal axis is the total load (Q-STM and ATM). SLAD shows better performance than RD-1 for both NS=10 and NS=440. The difference becomes bigger when NS is large. This is the same tendency as the case of the Q-STM call blocking probability. However, the difference is little, i.e. RD-1 can achieve almost the same performance as SLAD on an average. Therefore, we show the distribution of the quality next.

Figure 3.6 presents the distribution of the cell intra-switch delay of the ATM service class for 120 evaluated slots patterns. It is assumed that NS=10 and the total load is 0.811. The characteristics of RD-1 have more wide distribution than those of SLAD. This result clarifies that SLAD can balance the load of subframes stably and, on the other hand, RD-1 can not give a stable load balanced status.

From above consideration, SLAD is the efficient algorithm for *Process1*. SLAD can decrease the Q-STM call blocking probability even when NS is large and offer the stable QOS of the ATM service class. Hereafter, we decide to use SLAD as *Process1* for other evaluations.

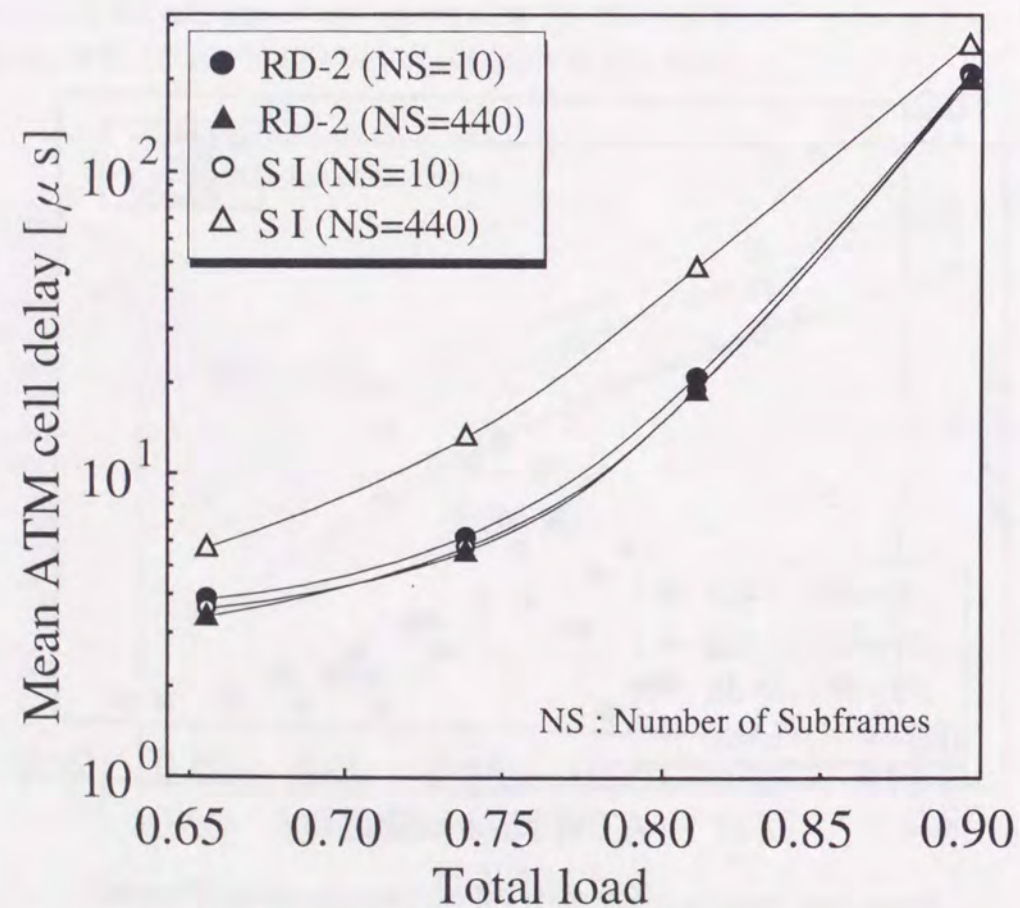


Figure 3.7: Characteristic of the mean ATM cell switching delay [Process2].

## 3.3.2 Algorithms of Slot Arrangement in Subframe

Comparing SI and RD-2, we clarify the efficient algorithm for *Process2*. *Process2* affects the QOS of the ATM service class, so the mean cell intra-switch delay of the ATM service class is evaluated. SLAD and ATR is used for *Process1* and *Process3* respectively.

Figure 3.7 shows the characteristics against the total load when NS=10 and NS=440. The case of NS=440 of SI is worse than other three cases. The reason is considered as follows. When the subframe length is small, the standard positions tend to collide and make stripes in SI. So the Q-STM traffic tends to make a small burst within a subframe, and the QOS of the ATM service class degrades. In other words, SI does not work well when NS is large. On the other hand, RD-2 shows good performance over any NS. Consequently, RD-2 is desirable as *Process2*. This algorithm has a merit of a simplicity, too. Hereafter, we use RD-2 as *Process2*.

## 3.3.3 Number of Subframes

NS can be set any divisor of the number of slots within one frame (if the link capacity is 156 Mbps, this is 2200). NS affects three qualities: (A) the Q-STM cell end-to-end delay, (B) the Q-STM call blocking probability, and (C) the QOS of the ATM service class. In order to obtain the index of the most efficient NS, it is necessary to evaluate these three qualities for NS. By computer simulations using SLAD, RD-2, and ATR, (B) and (C) are investigated. To research the characteristics of (A), simple algebraic formulas are derived.

## [Q-STM Cell End-to-end Delay]

The end-to-end cell delay of Q-STM service class is made up of two parts: the first portion is independent on the subframe length, such as a propagation delay, and the second one is in proportion to the subframe length, such as an intra-switch delay. Here, let  $\xi$  (bits) represent the length of the subframe and  $C$  (bps) denote the transmission rate of a link. And it is assumed that the number of intermediate nodes is represented by  $n$ , the distance between nodes by  $L$  (m), the optical propagation velocity in a fiber by  $\lambda$  (m/s), the delay at a pair of transmission devices, which are arranged at both end sides of link, by  $\tau$  (s), and the end-to-end delay denoted by  $D$  (s). We have

$$D = (n+1) \times \{(\text{delay at transmission devices}) + (\text{propagation delay between nodes})\} + n \times \{(\text{delay for time switching}) + (\text{synchronization delay})\}. \quad (3.1)$$

And as the synchronization delay,  $\bar{d}$ , is within  $0 \leq \bar{d} \leq \frac{\xi}{C}$ , we have

$$(n+1)\left(\tau + \frac{L}{\lambda}\right) + 2n\frac{\xi}{C} \leq D \leq (n+1)\left(\tau + \frac{L}{\lambda}\right) + 3n\frac{\xi}{C}. \quad (3.2)$$

Therefore, the largest value of  $D$ , which is represented as  $D_{max}$ , is

$$D_{max} = (n+1)\left(\tau + \frac{L}{\lambda}\right) + 3n\frac{\xi}{C}. \quad (3.3)$$

The numerical result of  $D_{max}$  is shown in Figure 3.8 when

$$C = 1.5 \times 10^8 \text{bps}, n = 3, \tau = 1.5 \times 10^{-3} \text{s}, L = 4.0 \times 10^4 \text{m}, \lambda = 2.0 \times 10^8 \text{m/s}.$$

The horizontal axis is NS and the figure also contains other characteristics explained later. Because the horizontal axis is plotted in a logarithmic scale, an inverse proportion curve shifted in the direction of the vertical axis is obtained. In consequence, when NS is few, the characteristics improves dramatically with the increment of NS. After NS exceeds about 100, however, the improvement is slight. In conclusion, around 50 to 2200 is efficient as NS from the viewpoint of the Q-STM cell end-to-end delay.

#### [Q-STM Call Blocking Probability]

Using the call level simulator, we evaluate the Q-STM call blocking probability when the Q-STM load is 0.6 and 0.7. The numerical result is also depicted in Figure 3.8. When NS is between one to around 100, we can hardly see any change for the characteristics. When NS exceeds around 100, they become worse rapidly with NS grows.

This can be understood in the following way. If more than or equal to one subframe among all subframes locating at the same position on all passing links has no empty slot, no more slots can be allocated in this subframe position (here, this state is described as a "congestion state"). When the number of slots within one subframe is extremely few, i.e. NS is very large, the number of subframes becoming the *congestion state* increases. As a result, the number of subframes in which anymore slots can not be reserved grows and the Q-STM call blocking probability degrades rapidly. The conclusion of this evaluation is that the efficient NS is one to around 100 as far as the Q-STM call blocking probability is concerned.

#### [ATM Service Class QOS]

Applying 120 Q-STM slots allocation patterns produced by the call level simulator to the cell level simulator (combination of Figure 3.3(a) and (d)), we evaluate the mean ATM cell intra-switch delay. Figure 3.8 also shows the characteristics when the total load is 0.738 and 0.811. Two regions can be seen, one is where NS is small (from one to around 100) and the other is where NS is large (from around 100 to 2200). In the former region, the qualities improves with NS increases. On the other hand, they degrade as NS grows in the latter region.

This can be understood from the next reasons. The smaller NS is, the more *Process2* becomes a dominant factor compared with *Process1*. So *Process2* mainly dominates the QOS of the ATM service class in the first area. SLAD tries to balance the load of subframes positively and, on the other hand, RD-2 has some variation for the stability. Therefore, the more *Process1* (SLAD) becomes dominant in comparison with *Process2* (RD-2), the better the QOS of the ATM service class becomes. This means that we can see improvement of QOS with increasing NS (shortening the length of the subframe). This effect can be seen strongly in the region where *Process2* is a dominant factor, so above tendency is seen in the first area. However, when NS approaches the maximum number "2200", the effect (SLAD becomes dominant factor compared with RD-2) becomes negligible. In the second region, the imbalance of subframe load becomes large. This is caused by the fact that SLAD does not

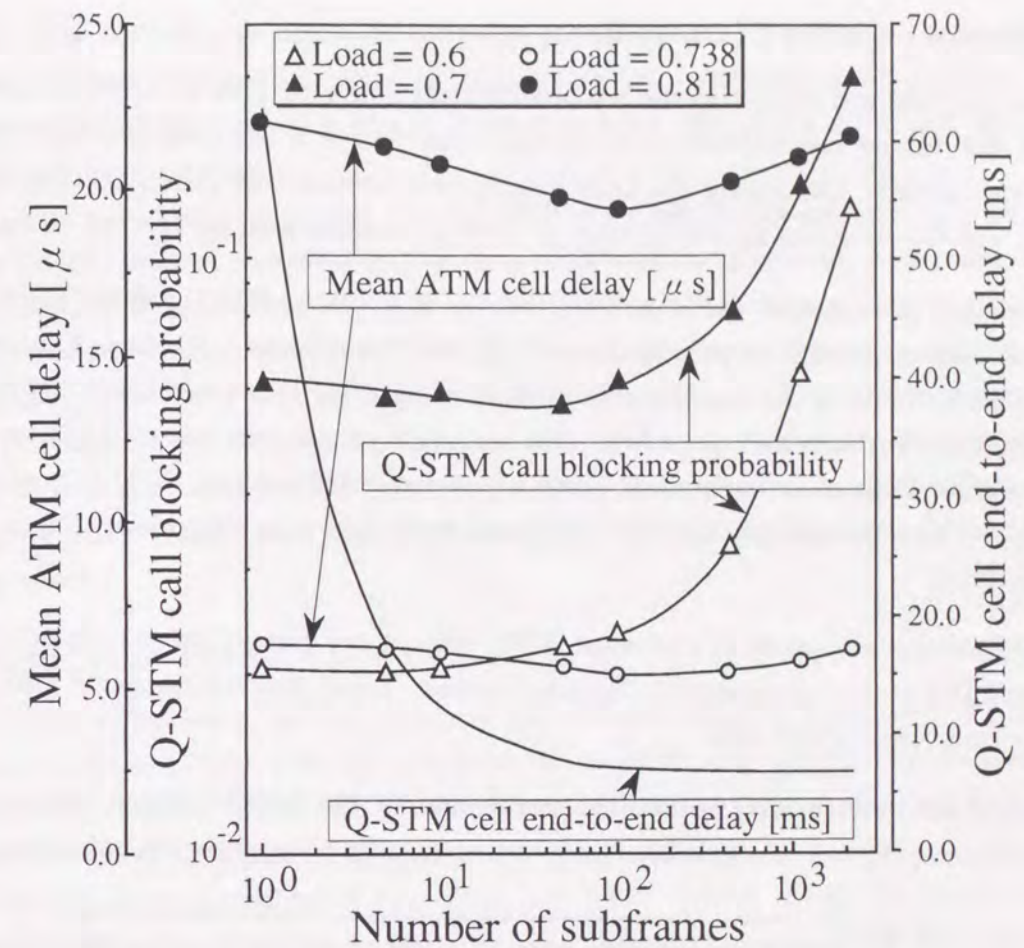


Figure 3.8: Characteristic of three qualities for the number of subframes.

work well when the length of the subframe is around one. In other words, the probability that SLAD selects the subframe, offered higher load than other subframes, to the position in which one more slot is allocated (refer 2.4.4). As a result, the QOS of the ATM service class degrades with NS increases in the second region. We can conclude that the efficient NS is around 100 in case of the ATM class QOS.

Now, we summarize the results about NS. The efficient NS is, around 50 to 2200 for (A) the Q-STM cell end-to-end delay, one to around 100 for (B) the Q-STM call blocking probability, and around 100 for (C) the ATM service class QOS. Thus, the most efficient NS is about 100 in the assumed environment. Hereafter, we set NS as 100.

### 3.4 Evaluation of Availability

In order to clarify the availability of the Q-STM method, we evaluate (1) the QOS of the ATM service class and (2) the additional call setup time caused by introducing the Q-STM method.



### 3.4.1 Influence on ATM Class QOS

The ATM service class corresponds to the low priority class compared with the Q-STM one because each Q-STM call can use reserved slots prior to other calls. Hence, a degradation of the ATM class QOS will be wondered. Comparing the QOS among some schemes, we clarify the degree of the degradation. The following two models are used in order to compare with the Q-STM method.

**(Buffer Priority)** Among some buffer priority controls, we select the NTCD-MB method [33]. It is assumed that the number of priority classes in isochronous services is just one. Therefore, this scheme corresponds to the absolute priority method [78, 79]. It is noted that Q-STM service class sources(CBR) are the high priority class and ATM service class sources(IPP) are the low priority class. Cells of the high priority class are stored in the different FIFO from cells of the low priority one. Low priority cells are only served when there is no high priority cell in the high priority FIFO.

**(Normal)** Every cells are stored in a common FIFO without any priority scheme. In other words, CBR and IPP sources are treated in the same manner. Recall that the number of CBR sources is identical to that of IPP ones.

The mean cell intra-switch delay of the ATM service class for the Q-STM method, the low priority class for Buffer priority, and cells generated from IPP sources for Normal are evaluated respectively.

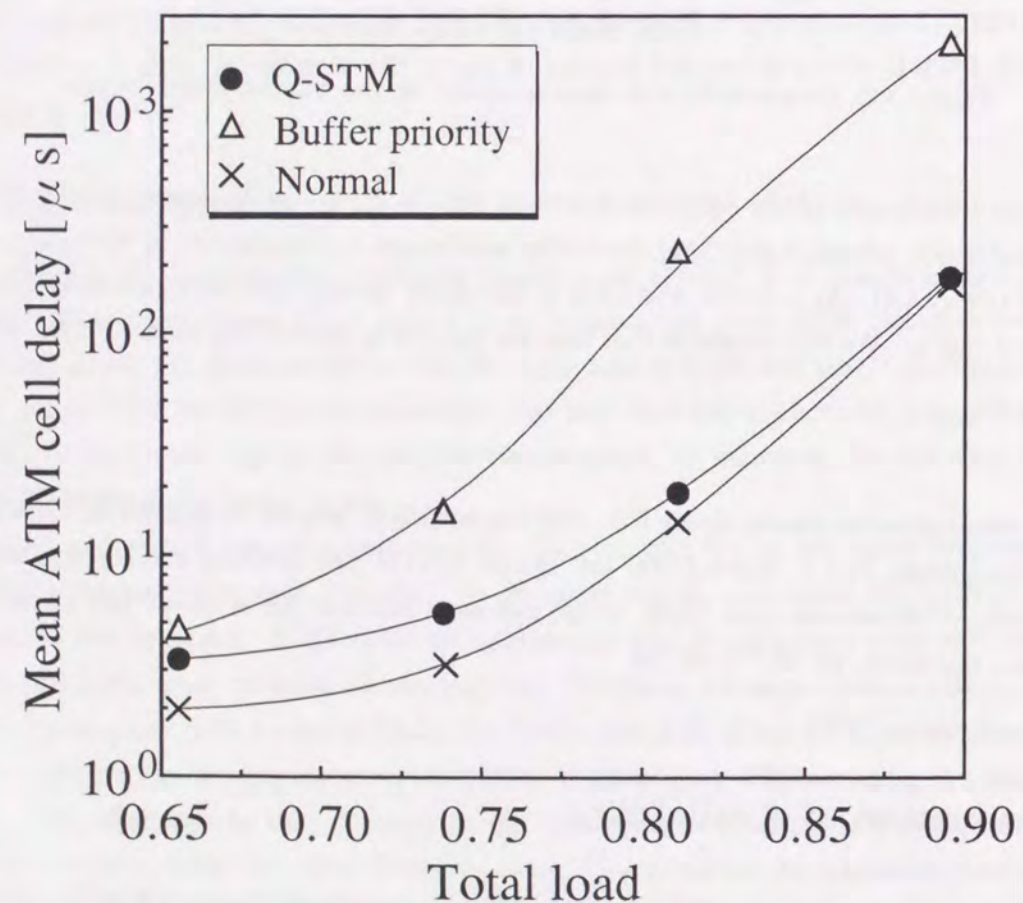


Figure 3.9: Characteristic of the mean ATM cell delay [Method comparison].

For the Q-STM method case, 120 slots allocation patterns provided by the call level simulator are used. The cell level simulators depicted in Figure 3.3(a)-(d) investigate these qualities. Figure 3.9 shows the results where *Process1* is SLAD, *Process2* is RD-2, *Process3* is ATR, and NS is 100. The horizontal axis is the total load.

Although sources of the high priority class are CBR, the traffic stream tends to show a burstiness in the buffer priority method because of multiplexing plural number of sources. As a result, the method degrades the QOS of the low priority class in compensation for the improvement of the QOS of the high priority class. On the other hand, the Q-STM method can avoid making a burstiness of the Q-STM traffic, by means of applying SLAD and RD-2. Therefore, the degradation of the QOS of the ATM service class is a slight degree in comparison with the Normal. Especially, when the total load is high, the effect of scattering Q-STM cells within a frame becomes strong and the difference between them is quite small. It is clarified that the degradation of the ATM service class QOS of the Q-STM method is small.

### 3.4.2 Call Setup Time

In the B-ISDN environment, the network must support wide range of bandwidth. For this reason, a very large number of time slots are sometimes allocated for one Q-STM call, so there is a fear of the call setup time increment. We evaluate the additional Q-STM call setup time caused by the introduction of the Q-STM method through an analytical technique.

We define call setup algorithms(SLAD, RD-2, and ATR) strictly, divide the processes into code steps, then for each step, define the number of required Central Processing Unit(CPU) cycles. Finally, the processing time for each algorithm is obtained by means of summing up its steps.

#### Assumption of Analysis

First, we define the following arguments.

- Number of subframes :  $M$
- Number of slots within a subframe :  $H$
- Number of passing links :  $h$
- CPU cycle time :  $\theta$  (s)
- Bandwidth of a Q-STM call :  $\omega$  (cell/frame)
- Number of slots allocated within subframe  $j$  for tagged call :  $\omega(j)$
- Index table of slots allocated within subframe  $j$  for tagged call( $z$  is table index) :  $res\_slot(j, z)$
- Number of empty slots within subframe  $j$  :  $emp1(j)$
- Number of empty slots within subframe  $j$  on link  $i$  [for SLAD] :  $emp\_sub(i, j)$
- Number of empty slots in the  $j$ th element of the subframe selection priority table [for SLAD] :  $min\_emp(j)$

- Index of subframe in the  $j$ th element of the subframe selection priority table [for SLAD] :  $sub\_n(j)$
- Index table of empty slots for subframe  $j$  [for RD-2] :  $emp\_tab1(j, z)$
- Table of slot position allocated in subframe  $j$  on input side [for ATR] :  $res\_slot\_u(j, z)$
- Table of slot position allocated in subframe  $j$  on output side [for ATR] :  $res\_slot\_d(j, z)$
- Intra-route index matching table for input  $x$ , output  $y$ , and subframe  $j$  [for ATR] :  $match(x, y, j, z)$
- Available intra-route table for input  $x$ , output  $y$ , and subframe  $j$  [for ATR] :  $emp3\_tab(x, y, j, z)$
- Number of available intra-route for input  $x$ , output  $y$ , and subframe  $j$  [for ATR] :  $emp3(x, y, j)$
- Table of assigned intra-route index for subframe  $j$  [for ATR] :  $route\_n(j, z)$
- Time table for input module  $x$  and subframe  $j$  [for ATR] :  $t\_tab\_u(x, j, z)$
- Time table for output module  $y$  and subframe  $j$  [for ATR] :  $t\_tab\_d(y, j, z)$

Table 3.1 shows the number of required CPU cycles for each basic process element cited from [100]. Moreover, combining above basic operations, we define the following processing elements.

Table 3.1: Number of required CPU cycles for basic processes.

Immediate value transfer between registers	1
Load or store	1
Addition, subtraction or comparison(between registers)	2
Addition, subtraction or comparison(through main memory)	4
Multiplication(between registers)	2
Multiplication(through main memory)	4
Division(between registers)	30
Division(through main memory)	32

**(Data transfer between two memory addresses)** : This is a combination of the load and store operation, so the cycle number is 2.

**(Exchanging between two memory addresses)** : It is assumed that read and write two operands finish in one cycle, so the cycle number is 2.

**(Producing random value)** : This operation  $rand(k)$  returns a random integer which satisfies  $0 \leq rand(k) \leq k - 1$ . The cycle number is 66 because of the following reason.

It is assumed the sequence  $x_n$  is obtained from  $x_n = kx_{n-1} \pmod{M}$  and  $rand(x)$  is derived from  $rand(x) = \lfloor x_n \times \frac{x}{M} \rfloor$ . Next, we divide this operation into CPU cycles. When  $x_{n-1}$  is assumed to be stored in the register  $R_r$ , we have

$$(1) k \times R_r \rightarrow R_0 \quad 2,$$

$$(2) R_0 \pmod{M} \rightarrow R_r \quad 30,$$

$$(3) R_r \times x \rightarrow R_2 \quad 2,$$

$$(4) R_2/M \rightarrow rand(x) \quad 32.$$

When we produce the algorithms of SLAD, RD-2, and ATR, we consider following principles.

- Decreasing the required CPU cycles as many as possible
- Removing a memory access from the calculation of the Effective Address(EA)

It is noted that the maximum time is evaluated when the processing time has some variance.

#### Analysis

##### [SLAD]

The SLAD algorithm is depicted in Figure 3.10. The number shown in the right shoulder of each element represents the required number of CPU cycles.  $R_1, R_2, \dots$  are assumed to be registers in CPU.  $R_h$  keeps the number of passing links and  $R_W$  saves the bandwidth of tagged call. The functions of other registers are summarized in Table 3.2.

The function ( $\rightarrow AAL$ ) represents to deliver information to AAL and its cycle is assumed one. For the sake of convenience, we separate the algorithm into three portions:

- (1) Calculation of the minimum number of empty slots for each subframe position,
- (2) Sorting the results obtained by (1) in the bigger order,
- (3) Determination of the number of slots allocated within each subframe position and judgment of the call blocking.

Let  $\Phi$  denote the processing time of the SLAD algorithm. Moreover we define  $\Phi_1, \Phi_2$ , and  $\Phi_3$  as the processing time for each portion.

(1) We have

$$\Phi_1 = \{(9R_h + 4)M + 1\}\theta = \{9Mh + 4M + 1\}\theta. \quad (3.4)$$

(2) Let define  $k_1$  as the number of **A** point passings in Figure 3.10 and  $k_2$  as that of **B** point passings. For a certain  $R_0$ , the bounds of  $k_1$  and  $k_2$  are

$$\begin{aligned} k_1 = 0, k_2 = 0 & \quad \text{for } R_0 = 0, \\ 0 \leq k_1 \leq R_0, k_2 = R_0 - k_1 & \quad \text{for } R_0 \geq 1. \end{aligned} \quad (3.5)$$

Table 3.2: Register functions in the SLAD algorithm.

Register	Functions		
	Portion (1)	Portion (2)	Portion (3)
R0	Subframe index		
R1	Min. num. of empty slots in subframe	Subframe index	Num. of allocated slots in subframe
R2	Link index	Subframe index	NS allocated fraction slot
R3		Subframe index	Subframe index
R4		Subframe index	

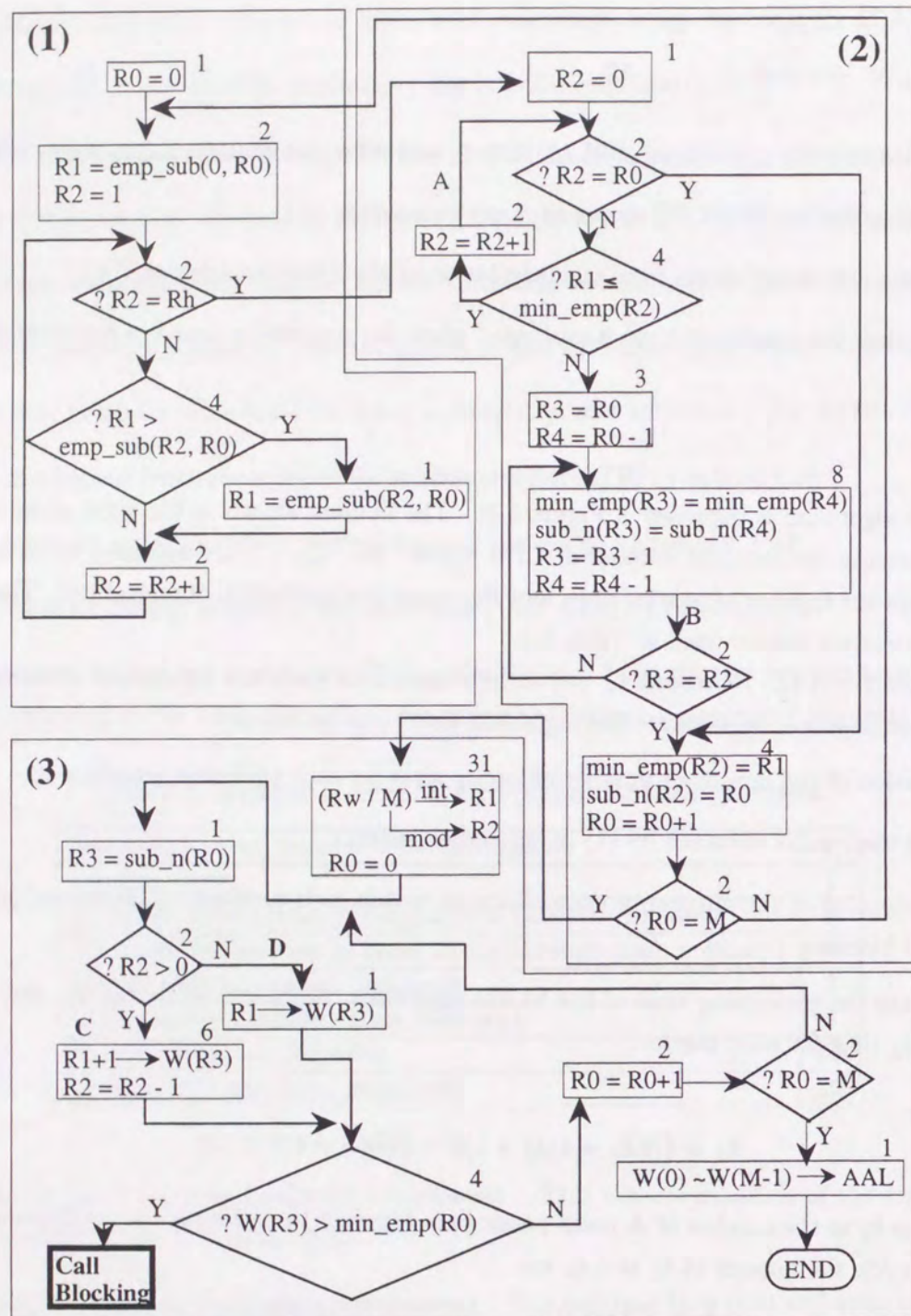


Figure 3.10: SLAD algorithm.

Therefore, let  $f_{\Phi}(R0, k_1)$  denote the number of cycles for  $R0$  and  $k_1$ , then we have

(i) for  $R0 = 0$ ,

$$f_{\Phi}(0, k_1) = 9, \quad (3.6)$$

(ii) for  $R0 \geq 1$ ,

$$f_{\Phi}(R0, k_1) = \begin{cases} 8k_1 + 10(R0 - k_1) + 16 & (0 \leq k_1 \leq R0 - 1), \\ 8R0 + 7 & (k_1 = R0). \end{cases} \quad (3.7)$$

When  $R0 \geq 1$  and  $k_1 = 0$ ,  $f_{\Phi}(R0, k_1)$  becomes the maximum value. The maximum value is derived as follows,

$$f_{\Phi, \max}(R0) = \begin{cases} 9 & (R0 = 0), \\ 10R0 + 16 & (1 \leq R0 \leq M - 1). \end{cases} \quad (3.8)$$

Now, we obtain  $\Phi_2$  as next,

$$\begin{aligned} \Phi_2 &= \left\{ \sum_{R0=0}^{M-1} f_{\Phi, \max}(R0) \right\} \theta \\ &= \left\{ 9 + \sum_{j=1}^{M-1} (10j + 16) \right\} \theta \\ &= (5M^2 + 11M - 7)\theta. \end{aligned} \quad (3.9)$$

(3) For each  $R0$ , either C or D point must be passed. Therefore,  $\Phi_3$  becomes its maximum value when the number of C point passings attains the greatest value. The greatest value is  $M - 1$ , so

$$\Phi_3 = \{6(M - 1) + 1 + 11M + 32\}\theta = (17M + 27)\theta. \quad (3.10)$$

Summing  $\Phi_1, \Phi_2$ , and  $\Phi_3$ , we have

$$\Phi = (9Mh + 5M^2 + 32M + 21)\theta. \quad (3.11)$$

[RD-2]

The algorithm is shown in Figure 3.11 and the register functions are summarized in Table 3.3.

Table 3.3: Register functions in the RD-2 algorithm.

Register	Functions
R0	Subframe index
R1	Allocated slot index
R2	Num. of slots allocated in subframe
R3	Num. of empty slots in subframe
R4	Position of selected slot

Let  $\Omega$  denote the processing time, we have

$$\begin{aligned} \Omega &= \left\{ \sum_{j=1}^M 76w_n(j) + 10M + 1 \right\} \theta \\ &= (76\omega + 10M + 1)\theta. \end{aligned} \quad (3.12)$$

[ATR]

The algorithm of the intra-route assignment is shown in Figure 3.12 and the register functions are summarized in Table 3.4.

Now, let  $X$  and  $Y$  denote the index of the input and output link which the tagged call is passing. The available intra-route table,  $emp3\_tab(x, y, R0, R4)$ , is provided for each pair of input and output

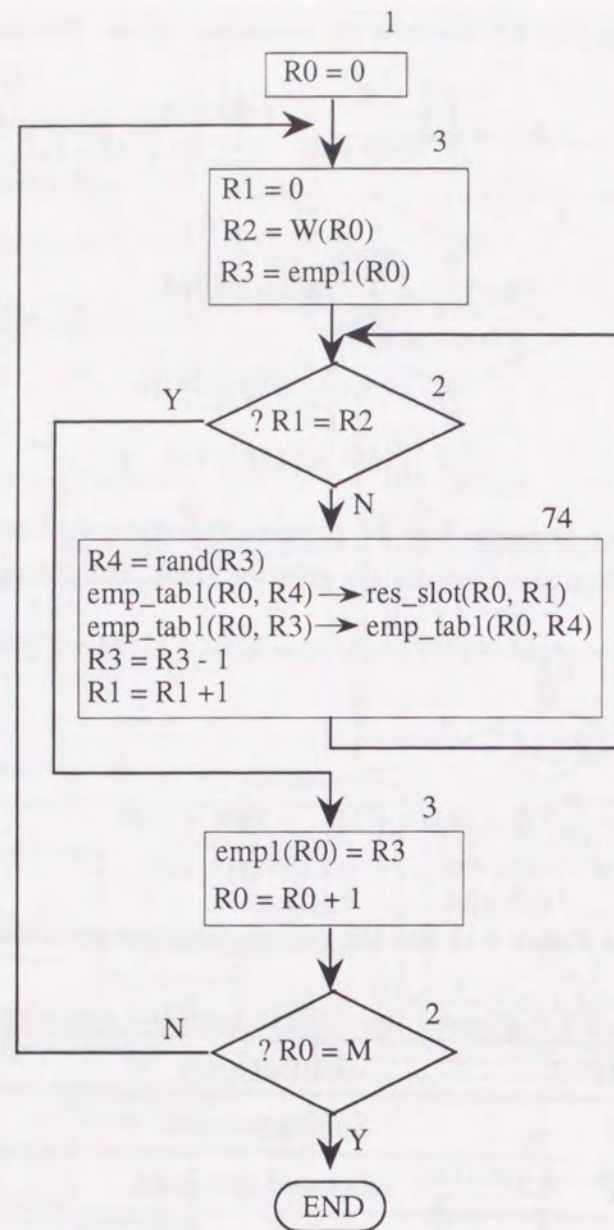


Figure 3.11: RD-2 algorithm.

links. It gives the information of the intra-routes which have already been accorded for both input and output sides. So the assignment of the intra-route between  $x = X$  and  $y = Y$  requires amendment for the tables  $emp3\_tab(x, y, R0, R4)$  which satisfy

- (i)  $1 \leq x \leq X_{max}, x \neq X$  and  $y = Y$ , or
- (ii)  $x = X$  and  $1 \leq y \leq Y_{max}, y \neq Y$ .

The total number of revised table is  $X_{max} + Y_{max} - 2$ .  $X_{max}$  is the number of input links and  $Y_{max}$  is that of output links. This process can be performed after the call setup process completes. Therefore, we do not include this process into the Q-STM call setup time. However, we show the algorithm of the ATR table accordance procedure in Figure 3.13 and the register functions in Table 3.5 for your information. In order to easily find the element which is to be eliminated from the table

$emp3\_tab(x, y, j, z)$ , we provide another table  $match()$ . The table  $match()$  contains the information where each intra-route index is included in  $emp3\_tab(x, y, j, z)$ .

Table 3.4: Register functions in the ATR route assignment algorithm.

Register	Functions
R0	Subframe index
R1	Num. of intra-routes assigned in subframe
R2	Num. of intra-routes to be assigned in subframe
R3	Num. of avail. intra-routes in subframe
R4	Selected index of intra-route table
R5	Selected intra-route index
R6	Position of slot on output link
R7	Work register

Table 3.5: Register functions in the ATR table accordance algorithm.

Register	Functions
R0	Subframe index
R1	Num. of accordanced intra-routes in subframe
R2	Num. of revising intra-routes in subframe
R3	Num. of empty intra-routes
R4	Intra-route index
R5	Introduced position of tagged route in table
R6	For swapping process
R7	Input (or output) link number

From Figure 3.12, the processing time  $\Upsilon$  is derived as

$$\begin{aligned} \Upsilon &= \left\{ \sum_{j=1}^M (83\omega(j) + 10) + 1 \right\} \theta \\ &= (83\omega + 10M + 1)\theta. \end{aligned} \quad (3.13)$$

Although the processing time  $\Xi$  required for the ATR table accordance is not considered for the Q-STM additional call setup time, we describe it for your information. From Figure 3.13, it is obtained as

$$\begin{aligned} \Xi &= \left[ \sum_{j=1}^M \{13\omega(j) + 6(X_{max} - 1) + 8 + 13\omega(j) + 6(Y_{max} - 1) + 11\} + 1 \right] \theta \\ &= \{26\omega + (6X_{max} + 6Y_{max} + 7)M + 1\} \theta. \end{aligned} \quad (3.14)$$

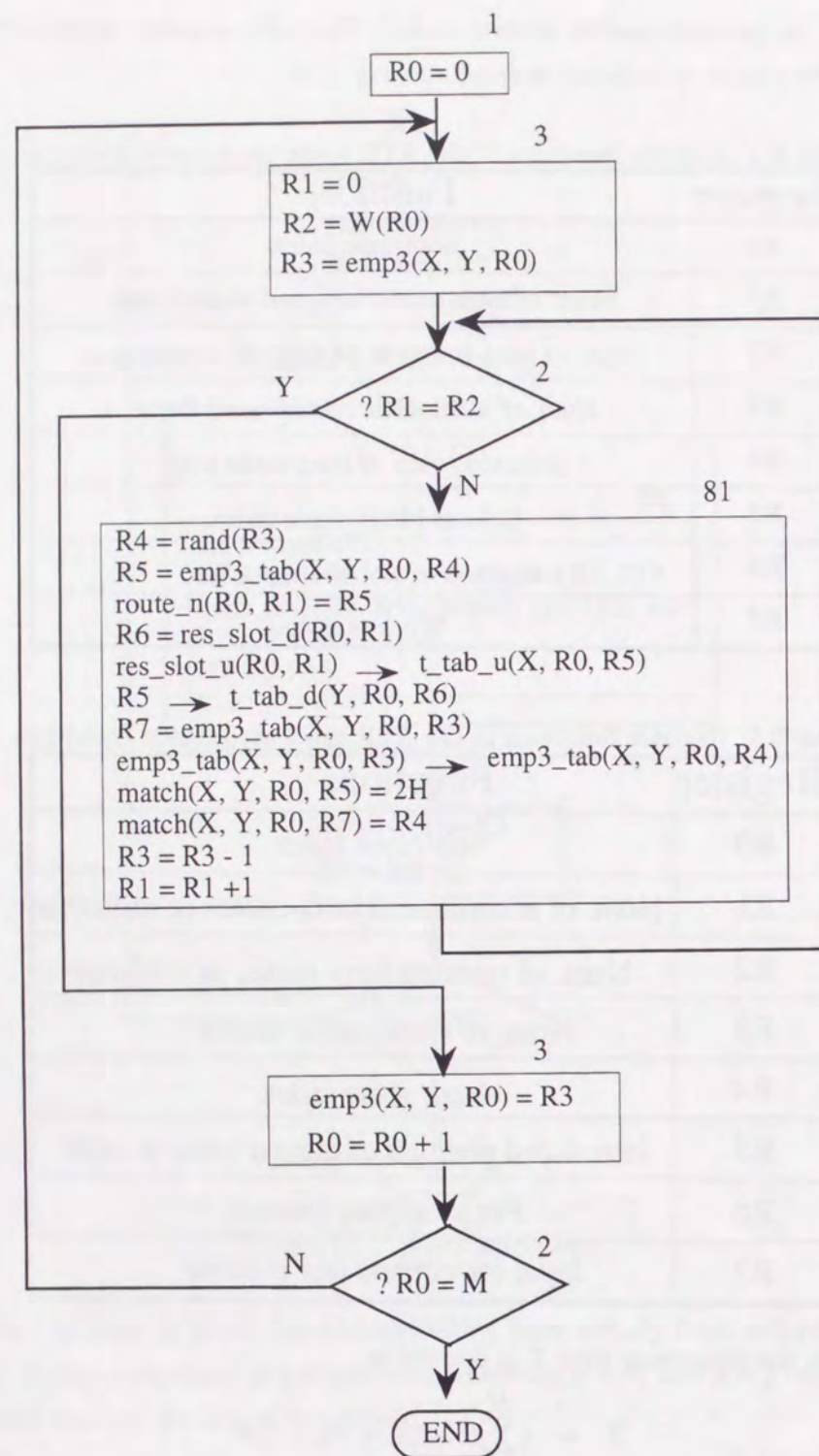


Figure 3.12: ATR intra-route assignment algorithm.

### Numerical Result

The processing time of SLAD, RD-2, and ATR is obtained as follows,

$$\begin{aligned}
 \Phi &= (9Mh + 5M^2 + 32M + 21)\theta \text{ for SLAD,} \\
 \Omega &= (76\omega + 10M + 1)\theta \text{ for RD-2,} \\
 \Upsilon &= (83\omega + 10M + 1)\theta \text{ for ATR.}
 \end{aligned}
 \tag{3.15}$$

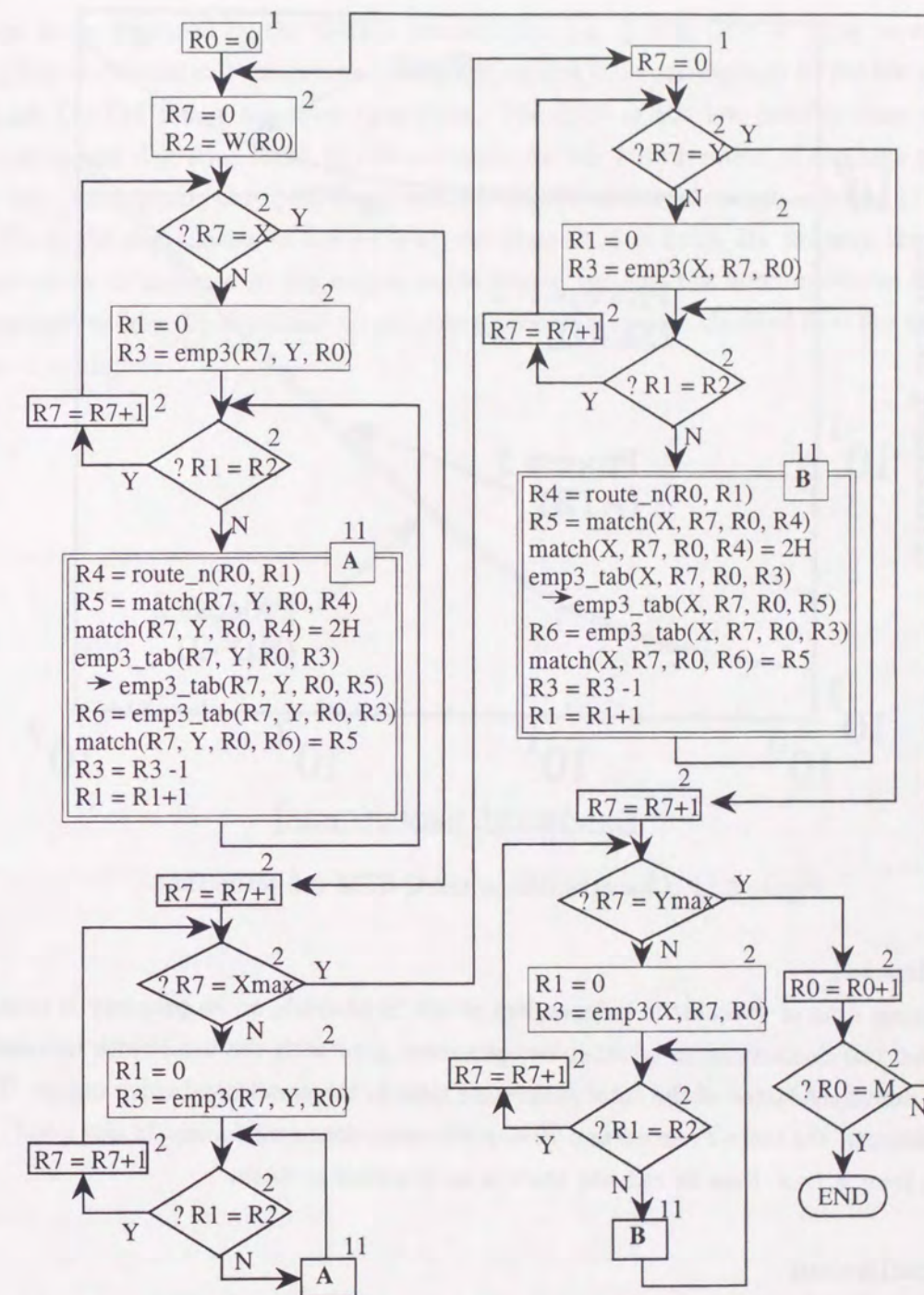


Figure 3.13: ATR table accordance algorithm.

Processing time of *Process1* grows rapidly with increment of  $M$ . This is caused by the calculation and sorting process of *avail(j)*. However, it is independent on  $\omega$ . On the other hand, *Process2* and *Process3* are influenced by  $\omega$ , rather than by  $M$ . This is from the nature of these processes that they allocate slots(or routes) one by one.

The numerical example is shown in Figure 3.14. The horizontal axis is the bandwidth and the vertical axis is the processing time. It is assumed that  $M = 100$ ,  $h = 5$ , and  $\theta = 1.43 \times 10^{-8}s$  [100]. In the figure, the characteristics of *Process1*(SLAD), *Process2*(RD-2), *Process3*(ATR), and the total

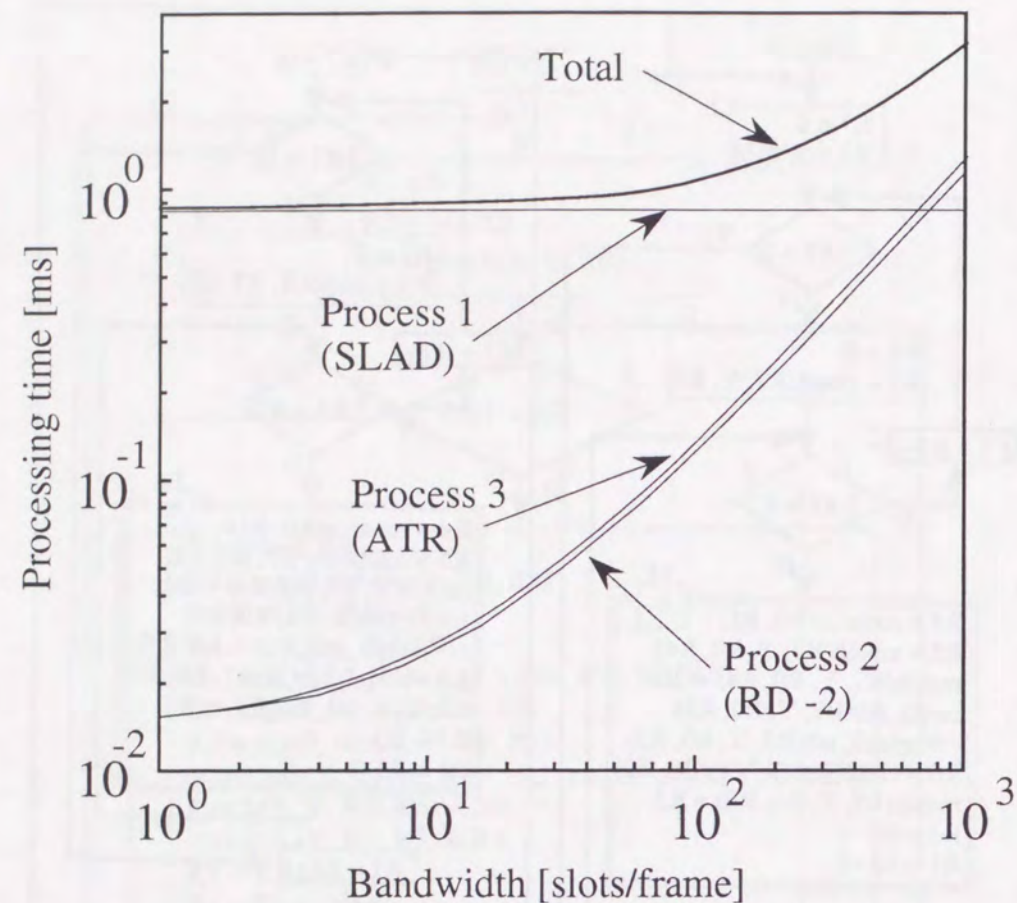


Figure 3.14: Characteristic of the Q-STM call setup time.

of them are depicted.

The processing time of *Process1* is independent of the bandwidth, so its property is constant. On the other hand, the characteristics of other two processes grow with the bandwidth increases. Thus, *Process1* is a dominant factor of the total processing time in the small bandwidth region. The larger bandwidth becomes, the more *Process2* and *Process3* become dominant factor. In any event, the order of processing time is *1ms*, thus we can say there is no practical problem.

### 3.5 Conclusion

In this chapter, the design issues and the availability of the Q-STM method were evaluated.

For the design issues, the efficient call setup algorithms and number of subframes were investigated respectively. We clarified the efficiency of SLAD compared with the random algorithm by means of evaluating the Q-STM call blocking probability and the ATM service class QOS. On the other hand, we got a result that we should use a random algorithm for *Process2* through the evaluation of the ATM class QOS. In order to roughly obtain the most efficient NS, we investigated (1)the Q-STM cell end-to-end delay, (2)the Q-STM call blocking probability, and (3)the QOS of the ATM service class. The conclusion of this evaluation was that the efficient number is around 100 in the assumed environment.

For the sake of evaluating the availability of the Q-STM method, we investigated two qualities

which seem to be degraded by the Q-STM introduction, i.e. (1)the QOS of ATM service class and (2)the Q-STM additional call setup time. The ATM service class corresponds to the low priority class because each Q-STM call is allocated time slots. The QOS of the low priority class of the buffer priority control was degraded much in compensation for the improvement of the high priority class QOS. On the other hand, the Q-STM cell stream can be scattered within a frame in the Q-STM method. Thus, the degradation of the ATM service class QOS is little. By the way, the Q-STM call setup time seems to increase in the unacceptable degree because the accommodated bandwidth in B-ISDN spreads widely. By summing up call setup process steps, we clarified that the additional call setup time is negligible.

## Chapter 4

# Performance Analysis of FEC-SSCS for ABR Class

### 4.1 Introduction

In the previous two chapters, the QOS control method for isochronous services were considered. In this chapter, we note the control method for the other service category, i.e. error-free services. One important example of this service category is data communication between computers or data terminals. Though it is not sensitive to the transfer delay quality, transmission without any error and loss of information require. Therefore, the error control is indispensable for this kind of service. For example, the CRC technique is usually introduced to discover or correct some bit errors [3]. When the receiver can not correct errors, a retransmission technique is necessary to complete the whole data forwarding. In this thesis, a unit of error control is described as "block".

The ATM cell size is so small that the cell-based retransmission costs much [22, 23]. On the other hand, the maximum limit of the block length is set in each network. (In the case of the IP packet transmission on the ATM network, this size is 9180bytes [19, 20].) Therefore, one message which is one volume of transferred data(e.g. one data file) is divided into plural blocks, then one block is divided into plural cells. As a result, three layers exist for the message transmission on the ATM network as shown in Figure 4.1.

Next, we consider some retransmission methods. Three types of retransmission schemes are known as typical conventional techniques: a Stop-And-Wait(SAW), a Go-Back-N(GBN), and a Selective Retransmission(SR) [101, 102]. In the SAW method, each block must wait to be transmitted until the sender receives ACKnowledgement(ACK) or Negative ACK(NACK) for the previous block as shown in Figure 4.2(a). When the receiver accepts the block without any errors, the receiver returns ACK, and the sender sends next block. On the other hand, the receiver returns NACK if some errors are detected and not be corrected, then the sender retransmits the same block. This method is not suited for a high speed network, i.e. ATM, because the throughput is restricted under one block per round trip time.

In the GBN scheme, the sender can send blocks continuously up to  $N$  without waiting a receipt of ACK or NACK for previous sending blocks. When NACK is received at the sender, all blocks following the corrupted block are retransmitted as shown in Figure 4.2(b). The throughput in GBN improves dramatically when the error rate of the network is small [101]. The GBN mechanism is simple as well

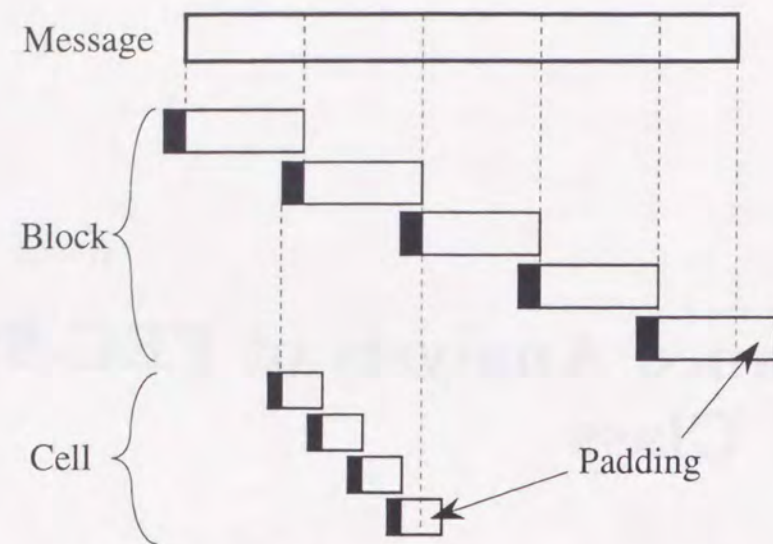


Figure 4.1: Layer structure of data communication on the ATM network.

as more efficient than SAW, so it has been widely applied for several networks.

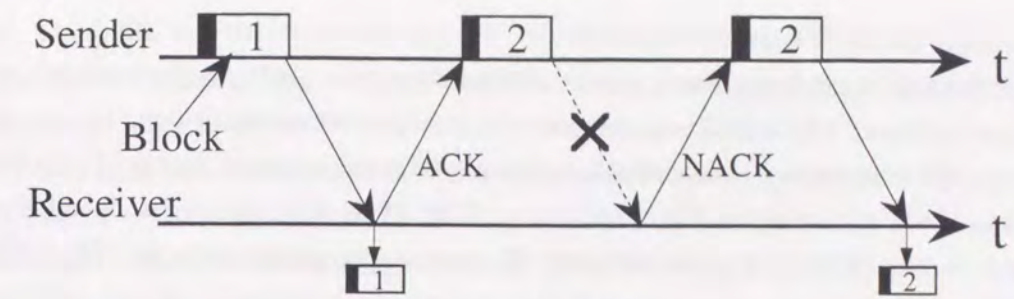
The most efficient retransmission method is SR which retransmits only the corrupted block as shown in Figure 4.2(c). However, plenty of resequence buffer is necessary at the receiver in order to achieve an ideal performance. Therefore, some SR methods have been proposed [107, 108] to limit the required buffer at the receiver. However, the complexity of processing is also problem.

Next, we describe the mechanisms of issues when an error-free service is transmitted on the ATM network.

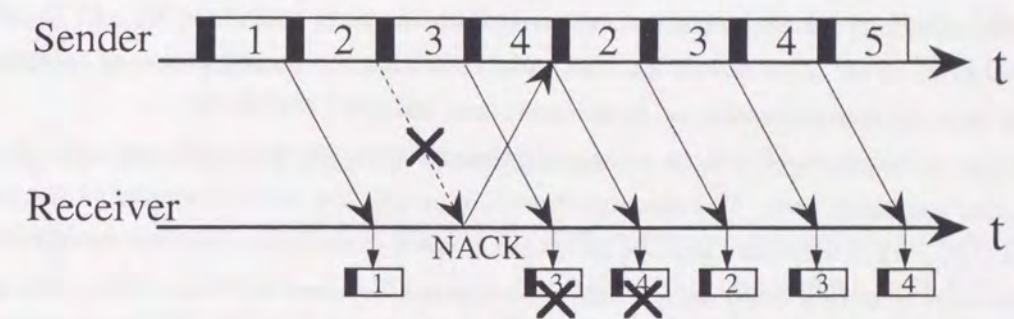
The delay from the instance that the sender starts the first cell transmission to the instance that it receives ACK for the last block is defined as a "message forwarding delay" in this thesis. The message forwarding delay consists of two parts, the transmission delay and the propagation delay as shown in Figure 4.3. The improvement of the interface rate decreases only the transmission delay. Thus, the propagation delay in the high speed network, such as ATM, seems to become more important factor(see Figure 4.3(b)) compared with the conventional networks(see Figure 4.3(a)). The interface rate of the ATM network will continue to increase in future, so this tendency becomes stronger. The retransmission adds one round trip delay, which is not improved by the growth of the interface rate, to the message forwarding delay. Hence, it is important to decrease the number of retransmission in the ATM network. In other words, the decrease of the block loss probability is significant.

Moreover, the cell fragmentation of the block degrades the network throughput. The reason of this is as follows. If at least one cell is lost at one passing ATM node, the block containing the lost cell becomes corrupt. In this time, however, other cells constituting the corrupt block are transmitted to the next passing ATM node, then finally, some of these cells will arrive the receiver. Without any control mechanism, the whole part of the corrupt block is retransmitted at AAL or the transport layer, so these received cells are dropped at the receiver. As a result, these invalid cells waste network resource and increase the network load [18]. Therefore, it is important to decrease the block loss probability for error-free services from the viewpoint of the efficiency of network resource utilization.

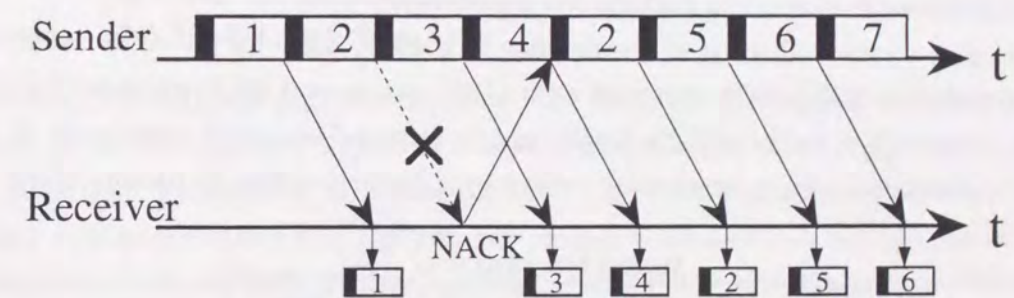
From these two reasons, the improvement of the block loss probability is the main issue for the



(a) Stop-and-wait



(b) Go-back-N



(c) Selective repeat

Figure 4.2: Some retransmission schemes.

QOS control of error-free services. The control methods which aim for the improvement of the block loss rate are listed as follows, the selective cell discarding method [6, 19, 53] and the Forward Error Correction in the Service Specific Convergence Sublayer(FEC-SSCS) [54, 55, 56, 57, 58]. The selective cell discarding method tries to centralize cell loss positions within a certain block. This results in that the block loss rate decreases.

On the other hand, main principle of FEC-SSCS is to recover the block which has some lost cells at the receiver by means of adding some redundant cells at the sender. At the sender, the FEC code is calculated for each symbol(e.g. one byte) over continuous user information cells and obtained FEC codes are packed into a FEC redundant cell. In addition to the user information cells, produced FEC redundant cells are transmitted. The FEC code is produced for each block. If the number of cells lost in the network among block is less than or equal to the number of attached FEC cells, the receiver can correct missing cells, so no retransmission is necessary. In this time, it is not necessary to consider



the positions of the lost cells within a block.

For the selective cell discarding method, a software-based complex processing is necessary at passing nodes. On the other hand, FEC-SSCS requires the additional processing at both end terminals. This is suited for a high speed network because the throughput bottleneck seems to locate at switches rather than end terminals in such a network. In summary, FEC-SSCS is considered to be the attractive control method for the QOS of error-free services. We analyze the performance of FEC-SSCS.

Next, we summarize researches which have been reported up to this time. About FEC-SSCS, the block loss probability in one ATM switch has been evaluated [55]. And the maximum throughput concerning SR has been derived [103]. Moreover, the block forwarding delay (time from the beginning of a block transmission to an acknowledgement reception) has been analyzed [104]. In the literature, a transient behavior of an ATM switch has been analyzed with the consideration of a bursty traffic. The object of performance evaluation on these researches has been the block.

The QOS that subscribers of a data communication network actually feel must be the message level rather than the block level. The message forwarding delay has been evaluated in the literatures [105, 106]. In [105], GBN is treated and the two state Markov chain is used for the block loss process. In [106], a message queueing delay at a sender is compared between GBN and SR when a random block loss is assumed. In these literatures, however, the unit of transmission is a block, so we can not apply these results to the ATM environment. It is noted that the consideration of ATM cell level behavior is indispensable in order to evaluate the performance of the cell level FEC.

This thesis aims at the evaluation of the message forwarding delay on the ATM network for two error control methods: FEC-SSCS combined with GBN and normal GBN (without FEC-SSCS). In this research, three layers, i.e. "a cell", "a block", and "a message" are newly considered. In the ATM network, the information loss is dominantly caused by a buffer overflow in passing nodes owing to

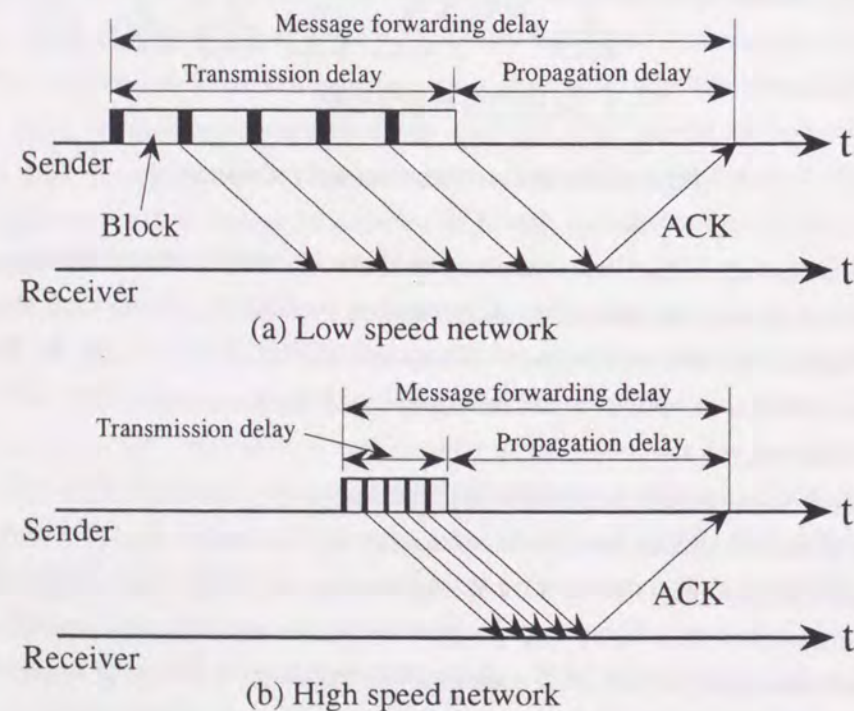


Figure 4.3: Message forwarding delay.

congestion. The buffer overflow tends to occur bursty as described in [109], so the two state Markov chain is used for a cell loss process in this thesis. This model has a good property expressing the cell loss process at the ATM node [110].

Using the two state Markov chain as the cell loss process leads the assumption that a cell loss rate is constant even if retransmission occurs. This assumption may be accurate in the environment that isochronous traffic without a retransmission control occupies a major part of the link capacity. Considering more general situation, it is important to reflect the effect of retransmission to the increment of a cell loss rate. In order to obtain a general tendency of it, an easy queueing model  $M/M/1/K$  is used to calculate the cell loss rate. A block length, an interface rate, and a burstiness of a cell loss process seem to be an important parameter affecting the message forwarding delay. The impact of these parameters are investigated.

## 4.2 Improvement of Block Loss Rate

It is important to decrease the block loss rate for an error-free service as mentioned in previous section. In this section, we explain two major techniques responding this requirement: the selective cell discarding method and FEC-SSCS. Before explaining each method, we briefly describe the configurations of AAL 3/4 and AAL 5 because these AALs are used for data communication.

### (Configuration of AAL 3/4 and AAL 5)

In Figure 4.4(a), the AAL 3/4 format is depicted. The AAL 3/4 SAR uses four bytes in each ATM cell payload. A two-bits Segment Type(ST) field is used to identify what position each cell locates. That is, "10" means a Beginning of Message(BOM), "00" a Continuation of Message(COM), and "01" an End of Message(EOM) [5]. The first cell of each block is BOM, the last cell of each block is EOM, and other cells are COM. Besides, the field becomes "11" (a Single Segment Message(SSM)) if only one cell constitutes a block. In these ways, the recognition of a Common Part Convergence Sublayer(CPCS)-Protocol Data Unit(PDU) boundaries is obtained at AAL.

A Multiplexing Identification(MID) field enables it to multiplex plural calls into the same ATM connection (using the same VCIs and VPIs). Therefore, it saves VCI and VPI resources when many calls communicate simultaneously. A four-bits Sequence Number(SN) field counts sequential cells within a block, modulo 16. A six-bits Length Indicator(LI) field indicates the number of bytes of data in the SAR data field (44 bytes). And CRC is a 10-bits code which is capable of correcting a single bit error in the cell.

Each CPCS-PDU has four bytes header and four bytes trailer. Besides, zero to three bytes padding are attached in order to align the CPCS-PDU payload to 32-bits boundaries. A Common Part Indicator(CPI) is an eight-bits field and the function has not defined yet. A sixteen-bits Buffer Allocation Size(BASize) field indicates the maximum number of bytes required to store the block at the receiver. However, it is not clear how useful the BASize field will be. An eight-bit beginning tag and end tag(Btag and Etag) fields are matching values. By means of these fields, the receiver confirms that the received header and trailer are in the same block. An alignment field is a byte of zeros to ensure that the trailer is 32 bits long. And a length field is the actual number of bytes that were sent in the

block.

In figure 4.4(b), the AAL 5 format is depicted. There is no SAR-PUD header and trailer, so all 48-bytes ATM cell payload can be used for user data. The recognition of CPCS-PDU boundary is obtained by the user signaling bit in the payload type field of the ATM cell header [5]. The indication bit of only the last cell within a block is set to one. A one-byte User-to-User(UU) field and a one-byte CPI field are currently unused and set to zero. A length field is the number of bytes of data in the block. A 32-bit CRC covers over the entire CS layer block, including the pad and the trailer.

The main differences between AAL 3/4 and AAL 5 are summarized as follows.

- In AAL 3/4, the boundary of CPCS-PDU is recognized by the ST field in the SAR-PUD header. On the other hand, it is understood by the signaling bit in the ATM cell header in AAL 5. As a result, when the ATM switch tries to recognize the boundaries, it must perform AAL processing for AAL 3/4. On the other hand, it sees only the ATM layer for AAL 5.
- CRC is executed for each ATM cell in AAL 3/4, however, it is performed for each CPCS-PDU basis in AAL 5. In general, the longer CRC field becomes, the stronger its capability becomes. Therefore, the 32-bits CRC of AAL 5 is preferable to the 10-bits CRC of AAL 3/4.
- The AAL overhead for each ATM cell payload is four bytes in AAL 3/4 and zero in AAL 5. From the viewpoint of the cell payload efficiency, AAL 5 is better than AAL 3/4.

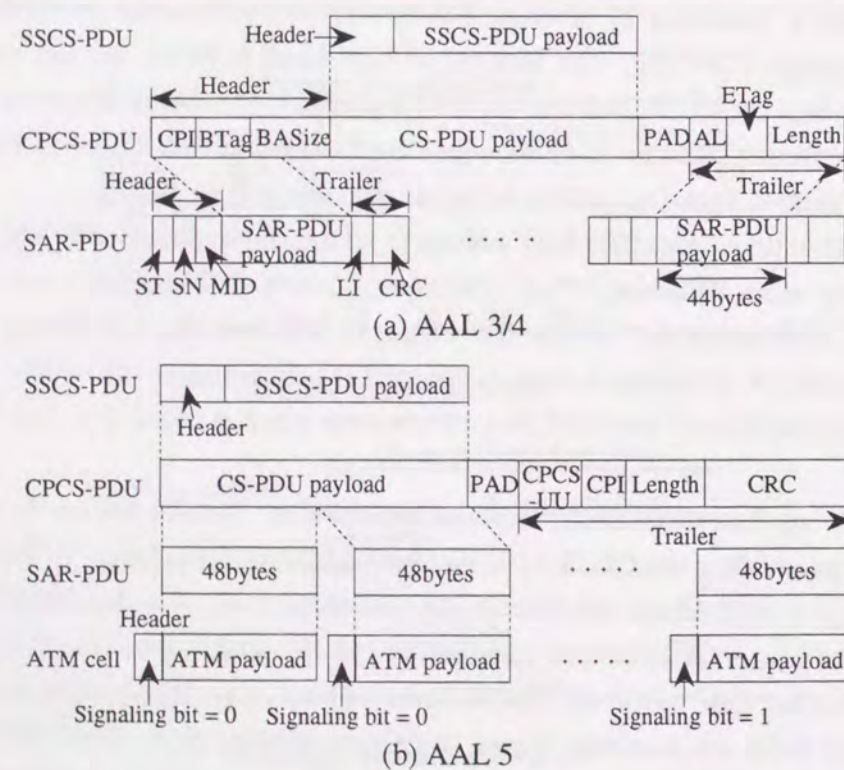


Figure 4.4: Configuration of AAL 3/4 and AAL 5.

- Plural calls can be multiplexed into one ATM connection in AAL 3/4, however, AAL 5 can not do such a multiplexing. Hence, the efficiency of VCI and VPI resources of AAL 3/4 is superior to that of AAL 5.

Next, we explain two control methods which aim at decrease of the block loss probability. The first is the selective cell discarding method, and the second is FEC-SSCS.

#### 4.2.1 Selective Cell Discarding

The main idea of this method is to decrease the transmission of invalid cells caused by one cell loss. In other words, the ATM switch or cross connect node recognizes CPCS-PDU<sup>1</sup> and tries to center dropped cells on a specified block. Mainly, two strategies are proposed: Partial Packet Discard(PPD) and Early Packet Discard(EPD) [19]. Next, each methods are described.

##### [Partial Packet Discard]

Once the switch drops a cell from a VC, it continues to drop cells from the same VC until the boundary of a block is detected. As a result, transmission of invalid cells following the lost cell can be avoided. When AAL3/4 is used, the information of the block boundary exists in the ATM cell payload. So the switch needs to execute processing at AAL. When AAL 5 is used, on the other hand, the identification of the block boundary is obtained in the ATM cell header(the user signaling bit in the payload type field). Therefore, AAL 5 is more attractive to introduce PPD. In the case of AAL 5, the switch does not drop the EOP cell because the missing of the EOP cell means the destruction of the block of both itself and the next.

PPD requires the switch to keep the state of each VC to recognize which VCs are using AAL 5 and want to use PPD. Also, the switch must keep state on which VCs are currently having cells dropped. The throughput improvement is limited because the switch does not drop the cells which have already queued. The cell loss occurs only when the buffer is full, so some cells belonging to the same block may have been already queued when one cell is lost. Thus, the congested link can still transmit a large fraction of cells belonging to corrupted blocks.

##### [Early Packet Discard]

With the EPD method, the switch drops entire blocks prior to the buffer overflow. If the queue length exceeds the threshold when the first cell of a block arrives at the switch, all cells belonging to the block are dropped. So, in terms of the cell-dropping strategy, the ATM switch emulates a block-based switch, dropping complete cells of the block. Because all invalid cells are selectively lost, EPD shows better network throughput than PPD. However, this method has difficulty for the selection of the threshold value. Although a fixed threshold is easily introduced, the performance and flexibility is not good. It may be efficient to move the threshold dynamically according to the network load or traffic characteristics. However, the effective estimation of these conditions are difficult, so the mechanism of setting this threshold is under way.

<sup>1</sup>CPCS-PDU or the transport layer PDU are possible for the block. In this thesis, we assume that the block corresponds to CPCS-PDU.

### 4.2.2 Forward Error Correction in SSCS

Main principle of FEC-SSCS is to recover the block containing some lost cells at the receiver by means of adding some redundant cells at the sender. First, we describe some error correction techniques. There has been a technique which corrects burst bit error, i.e. Reed-Solomon Code(RSC) [54]. When the position in which a burst bit error happens is known, this burst error is called as *burst erasure*. Cell loss is caused by congestion in the switches and an impulse noise. The former case results in the erasure and the latter case results in the error. In the ATM network, the main factor of cell loss is switch congestion. Therefore, it is reasonable to limit the correcting object to the burst erasures. A Reed-Solomon Erasure(RSE) code realizes a simple mechanism by means of this idea.

At the sender, the RSE code is calculated for each symbol(e.g. one byte) over continuous user information cells and obtained RSE codes are packed into a FEC redundant cell. In addition to the user information cells, produced FEC redundant cells are transmitted. The RSE code is produced for each block. Let assume that the number of cells belonging to one block is  $m$  and the number of FEC redundant cells attached for one block is  $n$ . If the number of cells lost in the network among  $m + n$  is less than or equal to  $n$ , the receiver can correct missing cells wherever the lost cells may locate. The same logic circuit can be used for both the encoder and the decoder in RSE.

One realization example of RSE which aims at recover of cell loss is FEC-SSCS. FEC-SSCS is discussed in ATM Forum [57] and its mechanism is introduced in SSCS. In the following sections, we analyze the message level performance of FEC-SSCS combined with GBN.

### 4.3 Analysis Model Formulation

In this section, the analytical model and assumption are described. Three layers are considered as shown in Figure 4.5. Message is one volume of data, whose length is  $L_M(\text{bit})$ , transferred in one communication session. For example, this corresponds to one data file in communication between file server and client terminal. In the analysis, we focus on behavior of one message transmission. One message is divided into some fragments; this fragment is a payload of a block whose length is  $L_B(\text{bit})$ . All blocks are assumed to have the same length payload in order to simplify the analysis. In other words, when the last segment is shorter than  $L_B$ , a padding is used to adjust the length to  $L_B$ . A block is organized by adding a block header, whose length is  $H_B(\text{bit})$ , to a segment.

The block is a unit of an error control: FEC redundant cells are attached for a block and retransmission is performed on a block basis. For instance, this is equivalent to CPCS-PDU or TCP-PDU. Because FEC is assumed to be attached in AAL, the block corresponds to CPCS-PDU in this thesis. Each block is divided into some pieces, the length of each piece is  $L_C(\text{bit})$ . Being added a header whose length is  $H_C(\text{bit})$ , this piece makes up a unit of transmission(i.e. cell). A padding is used for the last cell, if the last piece is shorter than  $L_C$ .

Let  $N_B$  denote the number of blocks constituting one message; it is given by

$$N_B = \lceil \frac{L_M}{L_B} \rceil, \quad (4.1)$$

where  $\lceil x \rceil$  is a smallest integer which is not below of  $x$ . Defining  $N_C$  as the number of cells organizing

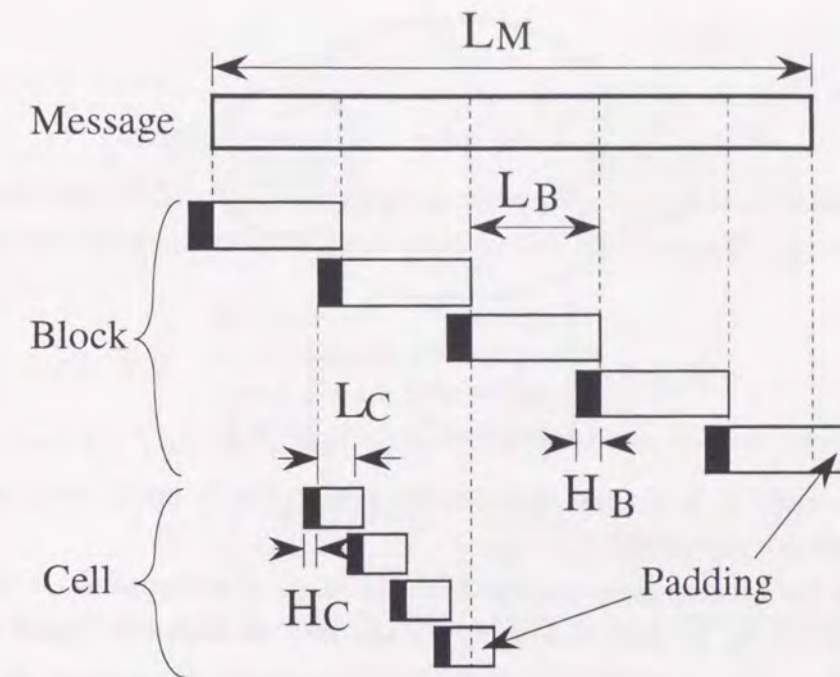


Figure 4.5: Three layers model.

one block, and  $N_r$  as the number of FEC redundant cells per one block, we obtain  $N_C$  as follows,

$$N_C = \lceil \frac{L_B + H_B}{L_C} \rceil + N_r. \quad (4.2)$$

It is noted that  $N_r = 0$  for GBN(without FEC). The block is lost at the receiver when more than  $N_r$  cells are lost among  $N_C$  cells; positions are not cared(see Figure 4.6). In both GBN and FEC+GBN schemes, the all blocks followed the lost block are retransmitted as shown in Figure 4.6. It is assumed that the window size of GBN is large enough not to close in any time.

When NACK is received at the sender during a transmission of other block, there are two ways how to treat the transmitting block(see Figure 4.6). According to one method, the block transmission is immediately interrupted and the retransmission is started: **Interrupted ReTransmission(IRT)**. According to the other method, the retransmission is started after the completion of the block transmission: **Non interrupted ReTransmission(NRT)**. When AAL3/4 is used, each cell contains the sequence number: an interruption of block transmission is possible. Hence, both IRT and NRT can be selected for AAL3/4. When AAL5 is used, on the other hand, a cell has only one bit information indicating whether it is the end of a CPCS-PDU or not. Thus, closing transmission of a block is impossible on AAL5; NRT is the only selection.

A discrete time probability process is considered, where a unit time is the cell length. Hereafter, the time units of all variables are defined as the slot(the cell length), without a notation. The cell loss process obeys the two state Markov chain in which no cell loss occurs in state 0 and cells must be lost in state 1 as shown in Figure 4.7. This model represents the cell loss process at the output buffer of ATM switch when a correlated traffic arrives [110]. We should also notice that this model can not reflect the network load to the cell loss rate directly and the long period congestion, in which the cell loss rate is higher than mean cell loss rate but not zero, can not be considered.

Let  $p_{01}$  and  $p_{10}$  denote one step state transition probability. The equilibrium probability of each

states,  $p_0$  and  $p_1$  are described as

$$(p_0, p_1) = \left( \frac{p_{10}}{p_{01} + p_{10}}, \frac{p_{01}}{p_{01} + p_{10}} \right). \quad (4.3)$$

The mean cell loss rate is equal to  $p_1$ , and the mean sojourn time of state 1 (mean number of consecutive cell losses) is equal to  $\frac{1}{p_{10}}$ . Moreover, the  $m$ -step state transition probability is given as

$$p_{ij}(m) = \begin{cases} p_0 + p_1 \sigma^m, & i = 0, j = 0, \\ p_1(1 - \sigma^m), & i = 0, j = 1, \\ p_0(1 - \sigma^m), & i = 1, j = 0, \\ p_1 + p_0 \sigma^m, & i = 1, j = 1, \end{cases} \quad (4.4)$$

where  $\sigma = 1 - p_{01} - p_{10}$ [111]. It is noted that whether a cell is lost or not is determined by the slot state in which the cell is transmitted.

It is assumed that the cell stream transmitted from one terminal is shaped to a CBR traffic at the User Network Interface (UNI) in order to simplify the analysis. As shown in Figure 4.6, each cell is supposed to be transmitted at intervals of  $D$  slots. Let  $R$  denote the propagation delay between the sender and the receiver, it is obtained as

$$R = \left\lceil \frac{5.0 \times 10^{-9} \psi C}{L_C + H_C} \right\rceil, \quad (4.5)$$

where  $\psi(m)$  is the distance between two terminals, and  $C$  (bps) is the link capacity. Both (i) the delay caused by passing ATM switches and (ii) the processing delay at the receiver between completing a receipt of a block and starting to send ACK or NACK are neglected. Let  $R_T$  denote the round trip delay of a block, we have

$$R_T = D(N_C - 1) + 2R + 2. \quad (4.6)$$

When NACK of the block whose sequence number is less than or equal to  $N_T (\equiv N_B + 1 - \lceil \frac{R_T}{DN_C} \rceil)$  is received at the sender, another block must be on transmission. If NRT is used, the actual round trip

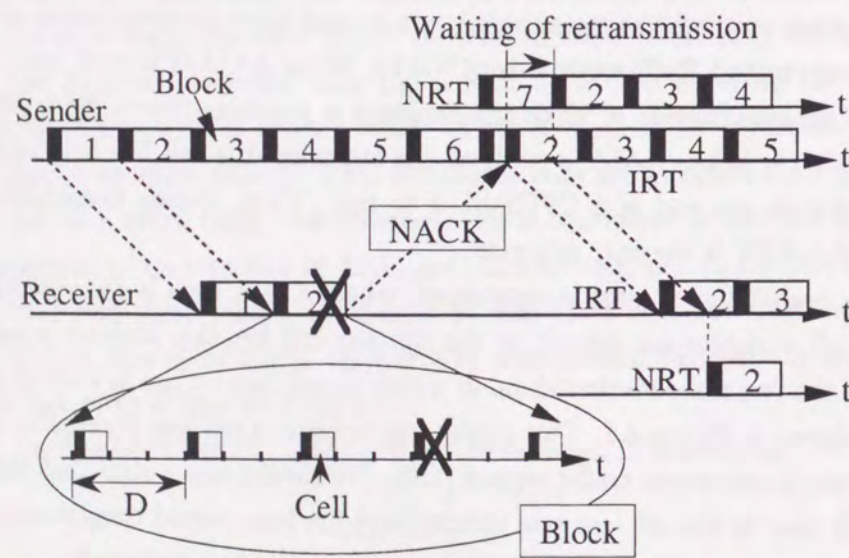


Figure 4.6: Retransmission sequence.

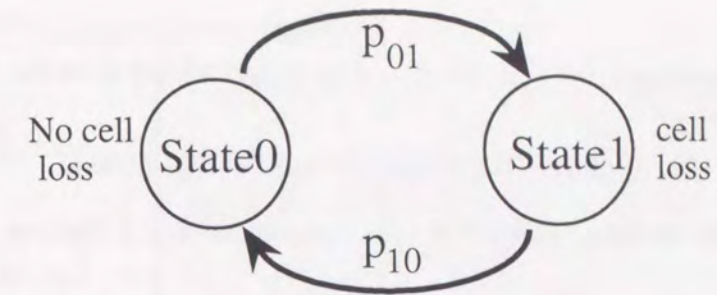


Figure 4.7: Gilbert model.

time is different from  $R_T$ . Thus, let  $r_i$  denote the actual round trip delay, we have

$$r_i = \begin{cases} \lceil \frac{R_T}{DN_C} \rceil \cdot DN_C, & 1 \leq i \leq N_T, \\ R_T, & N_T + 1 \leq i \leq N_P \end{cases} \quad (4.7)$$

for NRT. When IRT is used,  $r_i = R_T$  for all  $i$ . For the sake of convenience, we define  $\hat{R}_T \equiv \lceil \frac{R_T}{DN_C} \rceil \cdot DN_C$ .

## 4.4 Analysis

### 4.4.1 Block Acceptance Probability

Let  $y_i$  denote the random variable representing a slot state, i.e. a cell is transmitted without any loss in  $y_i = 0$  and lost in  $y_i = 1$ . As mentioned in section 4.3,  $y_i$  changes in the unit of slot according to the two state Markov chain.

First, the conditional probability,  $f(j, k, y_j | y_1)$ , is considered:  $k$  cells are lost among consecutive  $j$  cells at intervals of  $D$  slots and the slot state, in which  $j$ th cell is transmitted, becomes  $y_j$ , provided that the slot state, in which the first cell is transmitted, is  $y_1$ . For  $j = 1$ , we have

$$f(1, k, y_1 | y_1) = \begin{cases} 1, & (k, y_1) = (0, 0), (1, 1), \\ 0, & \text{others}, \end{cases} \quad (4.8)$$

and for  $j \geq 2$ ,

$$f(j, k, 0 | y_1) = \begin{cases} p_{00}(D)f(j-1, 0, 0 | y_1), & k = 0, \\ p_{00}(D)f(j-1, k, 0 | y_1) \\ + p_{10}(D)f(j-1, k, 1 | y_1), & 1 \leq k \leq j, \end{cases} \quad (4.9)$$

$$f(j, k, 1 | y_1) = \begin{cases} 0, & k = 0, \\ p_{01}(D)f(j-1, k-1, 0 | y_1) \\ + p_{11}(D)f(j-1, k-1, 1 | y_1), & 1 \leq k \leq j. \end{cases}$$

In order to obtain the general expression of  $f(j, k, y_j | y_1)$ , we consider  $F(z, k, y | y_1)$  which is the probability generating function of  $f(j, k, y_j | y_1)$  for  $j$ . Because  $f(j, k, y_j | y_1) = 0$  for  $j < k$ ,  $F(z, k, y | y_1)$  is defined as

$$F(z, k, y | y_1) \equiv \sum_{j=\max(k,1)}^{\infty} f(j, k, y_j | y_1) z^j. \quad (4.10)$$

Classifying for  $k$ , we derive  $F(z, k, y | y_1)$ .

(i)  $k = 0$ 

Multiplying both sides of equation (4.9) for  $y_j = 0$  by  $z^j$  and adding them for  $j \geq 2$ , we obtain the following equation,

$$F(z, 0, 0|y_1) - f(1, 0, 0|y_1)z = p_{00}(D)zF(z, 0, 0|y_1). \quad (4.11)$$

Taking equation (4.8) into account, we solve above equations for  $F(z, 0, 0|y_1)$  as

$$\begin{aligned} F(z, 0, 0|y_1) &= \frac{zf(1, 0, 0|y_1)}{1 - p_{00}(D)z} \\ &= \begin{cases} \frac{z}{1 - p_{00}(D)z}, & y_1 = 0, \\ 0, & y_1 = 1. \end{cases} \end{aligned} \quad (4.12)$$

In the case of  $y_j = 1$ , it is noted that  $f(j, 0, 1|y_1) = 0$  for any  $j$ . Thus, it is derived as

$$F(z, 0, 1|y_1) = 0. \quad (4.13)$$

(ii)  $k = 1$ 

Multiplying both sides of equations (4.9) by  $z^j$  and adding them for  $j \geq 2$ , we have

$$\begin{aligned} F(z, 1, 0|y_1) - f(1, 1, 0|y_1)z &= p_{00}(D)zF(z, 1, 0|y_1) + p_{10}(D)zF(z, 1, 1|y_1), \\ F(z, 1, 1|y_1) - f(1, 1, 1|y_1)z &= p_{01}(D)zF(z, 0, 0|y_1) + p_{11}(D)zF(z, 0, 1|y_1). \end{aligned} \quad (4.14)$$

By means of substituting equations (4.8), (4.12), and (4.13) into above equations,  $F(z, 1, y|y_1)$  is derived as

$$\begin{aligned} F(z, 1, 0|y_1) &= \begin{cases} \frac{p_{10}(D)p_{01}(D)}{\{1 - p_{00}(D)z\}^2} \cdot z^3, & y_1 = 0, \\ \frac{p_{10}(D)z^2}{1 - p_{00}(D)z}, & y_1 = 1, \end{cases} \\ F(z, 1, 1|y_1) &= \begin{cases} \frac{p_{01}(D)z^2}{1 - p_{00}(D)z}, & y_1 = 0, \\ z, & y_1 = 1. \end{cases} \end{aligned} \quad (4.15)$$

(iii)  $k \geq 2$ 

Multiplying both sides of equations (4.9) by  $z^j$  and adding them for  $j \geq k$ , we obtain

$$\begin{aligned} F(z, k, 0|y_1) &= p_{00}(D)zF(z, k, 0|y_1) + p_{10}(D)zF(z, k, 1|y_1), \\ F(z, k, 1|y_1) &= p_{01}(D)zF(z, k-1, 0|y_1) + p_{11}(D)zF(z, k-1, 1|y_1). \end{aligned} \quad (4.16)$$

From above equations, following recurrence formulas,

$$\begin{aligned} F(z, k, 0|y_1) &= \frac{p_{10}(D)z}{1 - p_{00}(D)z} \cdot F(z, k, 1|y_1), \\ F(z, k, 1|y_1) &= \left[ \frac{p_{01}(D)p_{10}(D)z^2}{1 - p_{00}(D)z} + p_{11}(D)z \right] F(z, k-1, 1|y_1) \end{aligned} \quad (4.17)$$

are derived.

The expressions of  $F(z, k, y|y_1)$  are summarized as

$$\begin{aligned} F(z, k, 0|y_1) &= \begin{cases} \frac{z}{1 - p_{00}(D)z}, & k = 0, y_1 = 0, \\ 0, & k = 0, y_1 = 1, \\ p_{01}(D)p_{10}(D)\{G_{\alpha_1}(z)\}^{k-1}G_{\alpha_2}(z), & k \geq 1, y_1 = 0, \\ p_{10}(D)\{G_{\alpha_1}(z)\}^{k-1}G_{\alpha_3}(z), & k \geq 1, y_1 = 1, \end{cases} \\ F(z, k, 1|y_1) &= \begin{cases} 0, & k = 0, y_1 = 0, 1, \\ p_{01}(D)\{G_{\alpha_1}(z)\}^{k-1}G_{\alpha_3}(z), & k \geq 1, y_1 = 0, \\ z\{G_{\alpha_1}(z)\}^{k-1}, & k \geq 1, y_1 = 1, \end{cases} \end{aligned} \quad (4.18)$$

where  $G_{\alpha_n}(z)$  ( $n = 1, 2, 3$ ) are defined as

$$\begin{aligned} G_{\alpha_1}(z) &\equiv \frac{p_{01}(D)p_{10}(D)z^2}{1 - p_{00}(D)z} + p_{11}(D)z, \\ G_{\alpha_2}(z) &\equiv \frac{z^3}{(1 - p_{00}(D)z)^2}, \\ G_{\alpha_3}(z) &\equiv \frac{z^2}{1 - p_{00}(D)z}. \end{aligned} \quad (4.19)$$

Next, we transform  $G_{\alpha_1}(z)$ ,  $G_{\alpha_2}(z)$ , and  $G_{\alpha_3}(z)$  inversely, then derive distribution  $\alpha_1(i)$ ,  $\alpha_2(i)$ , and  $\alpha_3(i)$  ( $i \geq 0$ ) respectively,

$$\begin{aligned} \alpha_1(i) &= \begin{cases} 0, & i = 0, \\ p_{11}(D), & i = 1, \\ p_{01}(D)p_{10}(D) \cdot \{p_{00}(D)\}^{i-2}, & i \geq 2, \end{cases} \\ \alpha_2(i) &= \begin{cases} 0, & 0 \leq i \leq 2, \\ (i-2)\{p_{00}(D)\}^{i-3}, & i \geq 3, \end{cases} \\ \alpha_3(i) &= \begin{cases} 0, & 0 \leq i \leq 1, \\ \{p_{00}(D)\}^{i-2}, & i \geq 2. \end{cases} \end{aligned} \quad (4.20)$$

By using these distribution functions, we obtain the general forms of  $f(j, k, y_j|y_1)$  as follows ( $j \geq 1$ ),

$$\begin{aligned} f(j, k, 0|y_1) &= \begin{cases} \{p_{00}(D)\}^{j-1}, & k = 0, y_1 = 0, \\ 0, & k = 0, y_1 = 1, \\ p_{01}(D)p_{10}(D) \cdot \underbrace{\alpha_1(j) \otimes \cdots \otimes \alpha_1(j)}_{(k-1)\text{times}} \otimes \alpha_2(j), & k \geq 1, y_1 = 0, \\ p_{10}(D) \underbrace{\alpha_1(j) \otimes \cdots \otimes \alpha_1(j)}_{(k-1)\text{times}} \otimes \alpha_3(j), & k \geq 1, y_1 = 1, \end{cases} \\ f(j, k, 1|y_1) &= \begin{cases} 0, & k = 0, y_1 = 0, 1, \\ p_{01}(D) \underbrace{\alpha_1(j) \otimes \cdots \otimes \alpha_1(j)}_{(k-1)\text{times}} \otimes \alpha_3(j), & k \geq 1, y_1 = 0, \\ \underbrace{\alpha_1(j-1) \otimes \cdots \otimes \alpha_1(j-1)}_{(k-1)\text{times}}, & k \geq 1, y_1 = 1. \end{cases} \end{aligned} \quad (4.21)$$

The symbol  $\otimes$  represents the convolution.

Let  $P_A(N_C, y_E|y_S)$  denote the conditional probability: the block consisting of  $N_C$  cells is accepted at the receiver and the slot state, in which the last cell is transmitted, is  $y_E$ , provided the first cell is transmitted in the slot state  $y_S$ . We have

$$P_A(N_C, y_E|y_S) = \sum_{k=0}^{N_C} f(N_C, k, y_E|y_S). \quad (4.22)$$

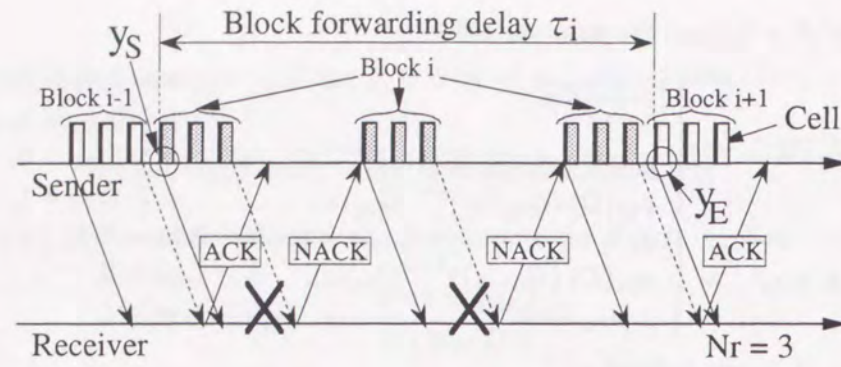


Figure 4.8: Analysis model.

Moreover, let  $P_A(N_C|y_S)$  denote the conditional probability that the block is accepted at the receiver when the first slot state is  $y_S$ ; it is given by

$$P_A(N_C|y_S) = P_A(N_C, 0|y_S) + P_A(N_C, 1|y_S). \quad (4.23)$$

Especially, the probability of the block acceptance when the first cell is transmitted in the equilibrium state is described as follows,

$$P_A(N_C) = p_0 P_A(N_C|0) + p_1 P_A(N_C|1). \quad (4.24)$$

#### 4.4.2 Block Forwarding Delay

Previous to deriving the message forwarding delay, the  $z$ -transformation of the block forwarding delay is considered. It is defined as the time between starting the block transmission and completing the successful block transmission to the link (see Figure 4.8). Let  $\tau_i$  denote the block forwarding delay of block  $i$ , and  $G_{\tau_i}(z)$  denote the  $z$ -transformation of it. Defining  $\tau_i(l)$  as  $\tau_i$  when  $l$  times retransmission occur, we obtain

$$\tau_i(l) = DN_C + r_i l. \quad (4.25)$$

Note that the actual round trip delay depends on the block sequence number  $i$ , not on the number of retransmission.

Let  $P_R(l, y_E|y_S)$  denote the conditional probability: the number of retransmission of block  $i$  is  $l$  and the next block  $i+1$  starts its transmission in slot state  $y_E$ , provided the slot state, in which the first cell of the block  $i$  in the first transmission, is  $y_S$  (see Figure 4.8). This conditional probability is independent on the block sequence number  $i$ , so the subscript  $i$  is eliminated. Let  $G_{\tau_i}(z, y_E|y_S)$  denote the probability generating function of  $P_R(l, y_E|y_S)$  for  $l$ , it is expanded as,

$$\begin{aligned} G_{\tau_i}(z, y_E|y_S) &\equiv \sum_{l=0}^{\infty} z^{\tau_i(l)} P_R(l, y_E|y_S) \\ &= z^{DN_C} \left\{ P_R(0, y_E|y_S) + \sum_{l=1}^{\infty} z^{r_i l} P_R(l, y_E|y_S) \right\} \\ &= z^{DN_C} \left\{ P_R(0, y_E|y_S) + H_i(z, y_E|y_S) \right\}, \end{aligned} \quad (4.26)$$

where  $H_i(z, y_E|y_S) \equiv \sum_{l=1}^{\infty} z^{r_i l} P_R(l, y_E|y_S)$ , and

$$P_R(0, y_E|y_S) = P_A(N_C, 0|y_S) p_{0, y_E}(D) + P_A(N_C, 1|y_S) p_{1, y_E}(D). \quad (4.27)$$

Next,  $H_i(z, y_E|y_S)$  is derived as follows,

$$\begin{aligned} H_i(z, y_E|y_S) &= z^{r_i} \left\{ P_R(1, y_E|y_S) + \sum_{l=2}^{\infty} z^{r_i(l-1)} P_R(l, y_E|y_S) \right\} \\ &= z^{r_i} \left\{ P_R(1, y_E|y_S) + \sum_{l=2}^{\infty} z^{r_i(l-1)} \left\{ 1 - P_A(N_C|y_S) \right\} \right. \\ &\quad \left. \cdot \left\{ p_{y_S, 0}(r_i) P_R(l-1, y_E|0) + p_{y_S, 1}(r_i) P_R(l-1, y_E|1) \right\} \right\} \\ &= z^{r_i} \left\{ P_R(1, y_E|y_S) + \left\{ 1 - P_A(N_C|y_S) \right\} \right. \\ &\quad \left. \cdot \left\{ p_{y_S, 0}(r_i) H_i(z, y_E|0) + p_{y_S, 1}(r_i) H_i(z, y_E|1) \right\} \right\} \\ &= \beta_{i, y_S, y_E} z^{r_i} + \varepsilon_{i, y_S, 0} z^{r_i} H_i(z, y_E|0) + \varepsilon_{i, y_S, 1} z^{r_i} H_i(z, y_E|1), \end{aligned} \quad (4.28)$$

where

$$\begin{aligned} \beta_{i, y_S, y_E} &\equiv P_R(1, y_E|y_S) \\ &= \left\{ 1 - P_A(N_C|y_S) \right\} \sum_{m=0}^1 p_{y_S, m}(r_i) \left\{ \sum_{n=0}^1 P_A(N_C, n|m) p_{n, y_E}(D) \right\}, \\ \varepsilon_{i, y_S, y} &\equiv \left\{ 1 - P_A(N_C|y_S) \right\} p_{y_S, y}(r_i). \end{aligned} \quad (4.29)$$

Inserting  $y_S = 0$  or  $1$  into equation (4.28), we obtain the following equations,

$$\begin{aligned} H_i(z, y_E|0) &= \beta_{i, 0, y_E} z^{r_i} + \varepsilon_{i, 0, 0} z^{r_i} H_i(z, y_E|0) + \varepsilon_{i, 0, 1} z^{r_i} H_i(z, y_E|1), \\ H_i(z, y_E|1) &= \beta_{i, 1, y_E} z^{r_i} + \varepsilon_{i, 1, 0} z^{r_i} H_i(z, y_E|0) + \varepsilon_{i, 1, 1} z^{r_i} H_i(z, y_E|1). \end{aligned} \quad (4.30)$$

By solving these equations,  $H_i(z, y_E|y_S)$  is calculated as follows,

$$\begin{aligned} H_i(z, y_E|0) &= z^{r_i} \left\{ \beta_{i, 0, y_E} (1 - \varepsilon_{i, 1, 1} z^{r_i}) + \beta_{i, 1, y_E} \varepsilon_{i, 0, 1} z^{r_i} \right\} \\ &\quad \cdot \left\{ 1 - (\varepsilon_{i, 0, 0} + \varepsilon_{i, 1, 1}) z^{r_i} + (\varepsilon_{i, 0, 0} \varepsilon_{i, 1, 1} - \varepsilon_{i, 0, 1} \varepsilon_{i, 1, 0}) z^{2r_i} \right\}^{-1}, \\ H_i(z, y_E|1) &= z^{r_i} \left\{ \beta_{i, 1, y_E} (1 - \varepsilon_{i, 0, 0} z^{r_i}) + \beta_{i, 0, y_E} \varepsilon_{i, 1, 0} z^{r_i} \right\} \\ &\quad \cdot \left\{ 1 - (\varepsilon_{i, 0, 0} + \varepsilon_{i, 1, 1}) z^{r_i} + (\varepsilon_{i, 0, 0} \varepsilon_{i, 1, 1} - \varepsilon_{i, 0, 1} \varepsilon_{i, 1, 0}) z^{2r_i} \right\}^{-1}. \end{aligned} \quad (4.31)$$

Since  $r_i$  attains only either  $R_T$  or  $\hat{R}_T$ ,  $H_i(z, y_E|y_S)$  is described as  $H(z, y_E|y_S)$  for  $r_i = R_T$  and  $\hat{H}(z, y_E|y_S)$  for  $r_i = \hat{R}_T$ .

Next, let us consider  $G_{\tau_i}(z, y_E)$ : the probability generating function removing the condition  $y_S$  from  $G_{\tau_i}(z, y_E|y_S)$ . From the assumption that the slot state is equilibrium condition when the first block is started its transmission, it is represented as

$$G_{\tau_i}(z, y_E) = p_0 G_{\tau_i}(z, y_E|0) + p_1 G_{\tau_i}(z, y_E|1), \quad (4.32)$$

for  $i = 1$ . The probability that the first cell of block  $i$  ( $2 \leq i \leq N_B$ ) is transmitted in state  $y$  at the first time is given by  $G_{\tau_{i-1}}(1, y)$ . Therefore,  $G_{\tau_i}(z, y_E)$  for  $2 \leq i \leq N_B$  is expressed as follows,

$$G_{\tau_i}(z, y_E) = G_{\tau_{i-1}}(1, 0) G_{\tau_i}(z, y_E|0) + G_{\tau_{i-1}}(1, 1) G_{\tau_i}(z, y_E|1). \quad (4.33)$$

Substituting  $z = 1$  and  $y_E = 0, 1$  in equations (4.33) and using  $G_{\tau_{N_T}}(z, y_E|y_S) = G_{\tau_{N_T-1}}(z, y_E|y_S) = \dots = G_{\tau_1}(z, y_E|y_S)$ ,  $G_{\tau_{N_B}}(z, y_E|y_S) = G_{\tau_{N_B-1}}(z, y_E|y_S) = \dots = G_{\tau_{N_T+1}}(z, y_E|y_S)$ , we obtain the following simultaneous difference equations,

$$\begin{aligned} G_{\tau_i}(1, 0) &= A_{00}G_{\tau_{i-1}}(1, 0) + A_{01}G_{\tau_{i-1}}(1, 1), \\ G_{\tau_i}(1, 1) &= A_{10}G_{\tau_{i-1}}(1, 0) + A_{11}G_{\tau_{i-1}}(1, 1) \end{aligned} \quad (4.34)$$

for IRT ( $2 \leq i \leq N_B$ ), and

$$\begin{aligned} G_{\tau_i}(1, 0) &= \begin{cases} \hat{A}_{00}G_{\tau_{i-1}}(1, 0) + \hat{A}_{01}G_{\tau_{i-1}}(1, 1), & 2 \leq i \leq N_T, \\ A_{00}G_{\tau_{i-1}}(1, 0) + A_{01}G_{\tau_{i-1}}(1, 1), & N_T + 1 \leq i \leq N_B, \end{cases} \\ G_{\tau_i}(1, 1) &= \begin{cases} \hat{A}_{10}G_{\tau_{i-1}}(1, 0) + \hat{A}_{11}G_{\tau_{i-1}}(1, 1), & 2 \leq i \leq N_T, \\ A_{10}G_{\tau_{i-1}}(1, 0) + A_{11}G_{\tau_{i-1}}(1, 1), & N_T + 1 \leq i \leq N_B, \end{cases} \end{aligned} \quad (4.35)$$

for NRT, where

$$\begin{aligned} A_{jk} &\equiv G_{\tau_1}(1, j|k) \\ &= \sum_{m=0}^1 P_A(N_C, m|k)p_{m,j}(D) + H(1, j|k), \\ \hat{A}_{jk} &\equiv G_{\tau_{N_T+1}}(1, j|k) \\ &= \sum_{m=0}^1 P_A(N_C, m|j)p_{m,j}(D) + \hat{H}(1, j|k). \end{aligned} \quad (4.36)$$

Now, let define two dimensional square matrixes  $\mathbf{A}$  and  $\hat{\mathbf{A}}$  as follows,

$$\begin{aligned} \mathbf{A} &\equiv \begin{bmatrix} A_{00} & A_{01} \\ A_{10} & A_{11} \end{bmatrix} \\ &= \begin{bmatrix} A_{00} & 1 - A_{00} \\ 1 - A_{11} & A_{11} \end{bmatrix}, \\ \hat{\mathbf{A}} &\equiv \begin{bmatrix} \hat{A}_{00} & \hat{A}_{01} \\ \hat{A}_{10} & \hat{A}_{11} \end{bmatrix} \\ &= \begin{bmatrix} \hat{A}_{00} & 1 - \hat{A}_{00} \\ 1 - \hat{A}_{11} & \hat{A}_{11} \end{bmatrix}. \end{aligned} \quad (4.37)$$

Moreover, a two dimensional vector  $\mathbf{g}_i$  is defined as

$$\mathbf{g}_i \equiv [G_{\tau_i}(1, 0), G_{\tau_i}(1, 1)], \quad (4.38)$$

and it is expressed as

$$\begin{aligned} \mathbf{g}_i &= \mathbf{A}\mathbf{g}_{i-1} \\ &= \mathbf{A}^{i-1}\mathbf{g}_1; \quad 2 \leq i \leq N_B \end{aligned} \quad (4.39)$$

for IRT,

$$\mathbf{g}_i = \begin{cases} \hat{\mathbf{A}}^{i-1}\mathbf{g}_1 & ; 2 \leq i \leq N_T, \\ \mathbf{A}^{i-N_T}\hat{\mathbf{A}}^{N_T-1}\mathbf{g}_1 & ; N_T + 1 \leq i \leq N_B \end{cases} \quad (4.40)$$

for NRT. From equation (4.32), we obtain  $\mathbf{g}_1$ . Hence, we have only to derive  $\mathbf{A}^{i-1}$  and  $\hat{\mathbf{A}}^{i-1}$  in order to take the general form of  $\mathbf{g}_i$ .

First, let consider the case of  $\mathbf{A}^{i-1}$ . Eigenvalues of  $\mathbf{A}$  are derived as  $\lambda_1 = 1$  and  $\lambda_2 = A_{00} + A_{11} - 1$  from a characteristic equation  $|\lambda\mathbf{E} - \mathbf{A}| = 0$ . Because both  $A_{00}$  and  $A_{11}$  are less than one,  $\mathbf{A}$  has different two eigenvalues. Therefore, it is possible to diagonalize the matrix  $\mathbf{A}$ . Eigenvectors  $\mathbf{x}_1$  and  $\mathbf{x}_2$  are derived as

$$\begin{aligned} \mathbf{x}_1 &= \left( c_1, \frac{1-A_{00}}{1-A_{11}}c_1 \right), \\ \mathbf{x}_2 &= (c_2, -c_2) \end{aligned} \quad (4.41)$$

where  $c_1$  and  $c_2$  are arbitrary real number. Let  $\mathbf{Q}$  denote a diagonal matrix of  $\mathbf{A}$ , and we select  $\mathbf{Q}$  as follows ( $c_1 = 1 - A_{11}$  and  $c_2 = 1$ ),

$$\mathbf{Q} = \begin{bmatrix} 1 - A_{11} & 1 \\ 1 - A_{00} & -1 \end{bmatrix}. \quad (4.42)$$

In this time, we have

$$\mathbf{Q}^{-1}\mathbf{A}^{i-1}\mathbf{Q} = \begin{bmatrix} 1 & 0 \\ 0 & (A_{00} + A_{11} - 1)^{i-1} \end{bmatrix} \quad (4.43)$$

and

$$\begin{aligned} \mathbf{A}^{i-1} &= \frac{1}{2 - A_{00} - A_{11}} \begin{bmatrix} 1 - A_{11} + (1 - A_{00})(A_{00} + A_{11} - 1)^{i-1} & \\ 1 - A_{00} - (1 - A_{00})(A_{00} + A_{11} - 1)^{i-1} & \\ & 1 - A_{11} - (1 - A_{11})(A_{00} + A_{11} - 1)^{i-1} \\ & 1 - A_{00} + (1 - A_{11})(A_{00} + A_{11} - 1)^{i-1} \end{bmatrix}. \end{aligned} \quad (4.44)$$

It is noted that  $2 - A_{00} - A_{11} > 0$  because  $A_{00} < 1, A_{11} < 1$ .

In the same way,  $\hat{\mathbf{A}}^{i-1}$  is derived as

$$\begin{aligned} \hat{\mathbf{A}}^{i-1} &= \frac{1}{2 - \hat{A}_{00} - \hat{A}_{11}} \begin{bmatrix} 1 - \hat{A}_{11} + (1 - \hat{A}_{00})(\hat{A}_{00} + \hat{A}_{11} - 1)^{i-1} & \\ 1 - \hat{A}_{00} - (1 - \hat{A}_{00})(\hat{A}_{00} + \hat{A}_{11} - 1)^{i-1} & \\ & 1 - \hat{A}_{11} - (1 - \hat{A}_{11})(\hat{A}_{00} + \hat{A}_{11} - 1)^{i-1} \\ & 1 - \hat{A}_{00} + (1 - \hat{A}_{11})(\hat{A}_{00} + \hat{A}_{11} - 1)^{i-1} \end{bmatrix}. \end{aligned} \quad (4.45)$$

Finally, the z-transformation of the block forwarding delay  $G_{\tau_i}(z)$  is derived for  $i = 1$ ,

$$\begin{aligned} G_{\tau_1}(z) &= \sum_{m=0}^1 G_{\tau_1}(z, m) \\ &= z^{DN_C} \left\{ P_A(N_C) + \sum_{n=0}^1 p_n \sum_{m=0}^1 H_1(z, m|n) \right\}, \end{aligned} \quad (4.46)$$

and for  $2 \leq i \leq N_B$ ,

$$G_{\tau_i}(z) = \sum_{n=0}^1 G_{\tau_{i-1}}(1, n) z^{DN_C} \left\{ P_A(N_C|n) + \sum_{m=0}^1 H_i(z, m|n) \right\}. \quad (4.47)$$

#### 4.4.3 Message Forwarding Delay

The message forwarding delay  $\tau$  is defined as the time from starting the transmission of the first cell of the first block to receiving the ACK for the last block at the sender. Let  $G_{\tau}(z)$  denote the z-transformation of  $\tau$ , it is given as

$$G_{\tau}(z) = z^{2R} \prod_{i=1}^{N_B} G_{\tau_i}(z). \quad (4.48)$$

From the property of  $G_{\tau_i}(1) = 1$  for  $1 \leq i \leq N_B$ , the mean message forwarding delay  $m_{\tau}$  is derived as

$$\begin{aligned} m_{\tau} &= \frac{\partial}{\partial z} G_{\tau}(z)|_{z=1} \\ &= N_B D N_C + 2R + \sum_{n=0}^1 \left\{ p_n + \sum_{i=2}^{N_B} G_{\tau_{i-1}}(1, n) \right\} \Gamma(n) \end{aligned} \quad (4.49)$$

for IRT, and

$$\begin{aligned} m_{\tau} &= N_B D N_C + 2R \\ &\quad + \sum_{n=0}^1 \left\{ \left\{ p_n + \sum_{i=2}^{N_T} G_{\tau_{i-1}}(1, n) \right\} \hat{\Gamma}(n) \right. \\ &\quad \left. + \sum_{i=N_T+1}^{N_B} G_{\tau_{i-1}}(1, n) \Gamma(n) \right\}, \end{aligned} \quad (4.50)$$

for NRT, where

$$\begin{aligned} \Gamma(0) &\equiv \frac{\partial}{\partial z} \sum_{m=0}^1 H(z, m|0)|_{z=1} \\ &= R_T \left\{ 1 - P_A(N_C|0) \right\} \left\{ 1 - \sigma^{R_T} + \sigma^{R_T} P_A(N_C|1) \right\} \\ &\quad \cdot \left\{ P_A(N_C) - \sigma^{R_T} P_A(N_C) + \sigma^{R_T} P_A(N_C|0) P_A(N_C|1) \right\}^{-1}, \\ \Gamma(1) &\equiv \frac{\partial}{\partial z} \sum_{m=0}^1 H(z, m|1)|_{z=1} \\ &= R_T \left\{ 1 - P_A(N_C|1) \right\} \left\{ 1 - \sigma^{R_T} + \sigma^{R_T} P_A(N_C|0) \right\} \\ &\quad \cdot \left\{ P_A(N_C) - \sigma^{R_T} P_A(N_C) + \sigma^{R_T} P_A(N_C|0) P_A(N_C|1) \right\}^{-1}. \end{aligned} \quad (4.51)$$

Note that  $\hat{\Gamma}(n)$  is obtained by replacing  $R_T$  with  $\hat{R}_T$  in equations (4.51).

#### 4.4.4 Reflection of Network Load

In this subsection, the network load is reflected to the cell loss rate. First,  $w$  is derived: the mean number of invalid cells accompanied with the message forwarding.

Let  $m_{ret}^{(i)}$  denote the mean number of retransmission of block  $i$ , it is given as

$$m_{ret}^{(i)} = \frac{1}{r_i} \left\{ \frac{\partial}{\partial z} G_{\tau_i}(z)|_{z=1} - D N_C \right\}. \quad (4.52)$$

Defining  $w_i$  as the number of invalid cells caused by one retransmission of block  $i$ , we have

$$w_i = \begin{cases} \lfloor \frac{R_T}{D} \rfloor, & 1 \leq i \leq N_T, \\ (N_B - i + 1) N_C, & N_T + 1 \leq i \leq N_B, \end{cases} \quad (4.53)$$

for IRT, and

$$w_i = \begin{cases} \lceil \frac{R_T}{D N_C} \rceil N_C, & 1 \leq i \leq N_T, \\ (N_B - i + 1) N_C, & N_T + 1 \leq i \leq N_B, \end{cases} \quad (4.54)$$

for NRT. Now,  $w$  is obtained as

$$w = \sum_{i=1}^{N_B} w_i m_{ret}^{(i)}. \quad (4.55)$$

Let  $\rho_0$  denote the available network load concerning only message bits, and  $\rho_S$  denote the network load except for retransmission. It is difficult to analyze the cell loss rate exactly, and the exact analysis of the cell loss rate is not goal of this thesis. So, it is assumed that  $\rho_S$  is simply represented as follows,

$$\rho_S = \rho_0 \times \frac{N_C}{L_B} (L_C + H_C). \quad (4.56)$$

Defining  $\tilde{\rho}_S$  as the network load with the consideration of retransmission, we have

$$\tilde{\rho}_S = \rho_S \left( 1 + \frac{w}{N_B N_C} \right). \quad (4.57)$$

By means of fixing  $\frac{1}{p_{10}}$  and varying  $p_1$ , the network load is reflected to a cell loss rate. It is assumed that  $p_1$  is given from  $M/M/1/K$ , where  $K$  is the buffer size; it is given as follows [112],

$$p_1 = \frac{1 - \tilde{\rho}_S}{1 - \tilde{\rho}_S^{K+1}} \tilde{\rho}_S^K. \quad (4.58)$$

$m_{\tau}$  depends on  $\tilde{\rho}_S$ , and vice versa. Thus,  $m_{\tau}$  is derived through the following procedure.

- (i) Setting  $\rho_S$  to  $\tilde{\rho}_S$  as the initial value
- (ii) Calculating  $p_1$  from the equation (4.58)
- (iii) Calculating  $m_{\tau}$  from equation (4.49) or (4.50)
- (iv) Obtaining  $\tilde{\rho}_S$  from (4.57)
- (v) Repeating (ii)~(iv) up to the convergence of  $\tilde{\rho}_S$

## 4.5 Performance Evaluation

The assumption of ATM environment leads to fix  $L_C = 384$  and  $H_C = 40$ . Supposing that the error control is performed in AAL5, the length of a block header is set as  $H_B = 64$  [26] and NRT is selected. Moreover, it is assumed that  $D = 1$ ,  $\psi = 5.0 \times 10^5$ , and  $K = 100$ . We set  $C = 2.5 \times 10^9$  and  $L_M = 1.0 \times 10^{10}$  when there is no explicit description.

Internet Enforcement Task Force(IETF) has accepted the Maximum Transfer Unit(MTU) size of  $7.344 \times 10^4$ (bit) for IP over AAL5 [20]. For the sake of convenience of treating  $N_r$ , we set  $L_B = 7.65 \times 10^4$ (this length corresponds to 200 cells), except for the impact of the block length. The mean sojourn time of slot state 1, i.e.  $\frac{1}{p_{10}}$ , will affect system performances strongly, and it is investigated that it is greater than around 0.6 [110]. In this section(except for the impact of  $\frac{1}{p_{10}}$ ), two situations are considered: (1) $p_{10} = 0.99$ (the case that cells are lost almost randomly) and (2) $p_{10} = 0.6$ (the case that cells are lost correlatively).

Let  $\chi$  denote the ratio of FEC redundancy, i.e.  $\chi \equiv \frac{N_r}{N_C - N_r}$ . Two cases  $\chi = 0.0$  and  $0.05$ (corresponding to  $N_r = 0$  and  $10$  when  $L_B = 7.65 \times 10^4$ ) are considered except for the impact of  $\frac{1}{p_{10}}$ .



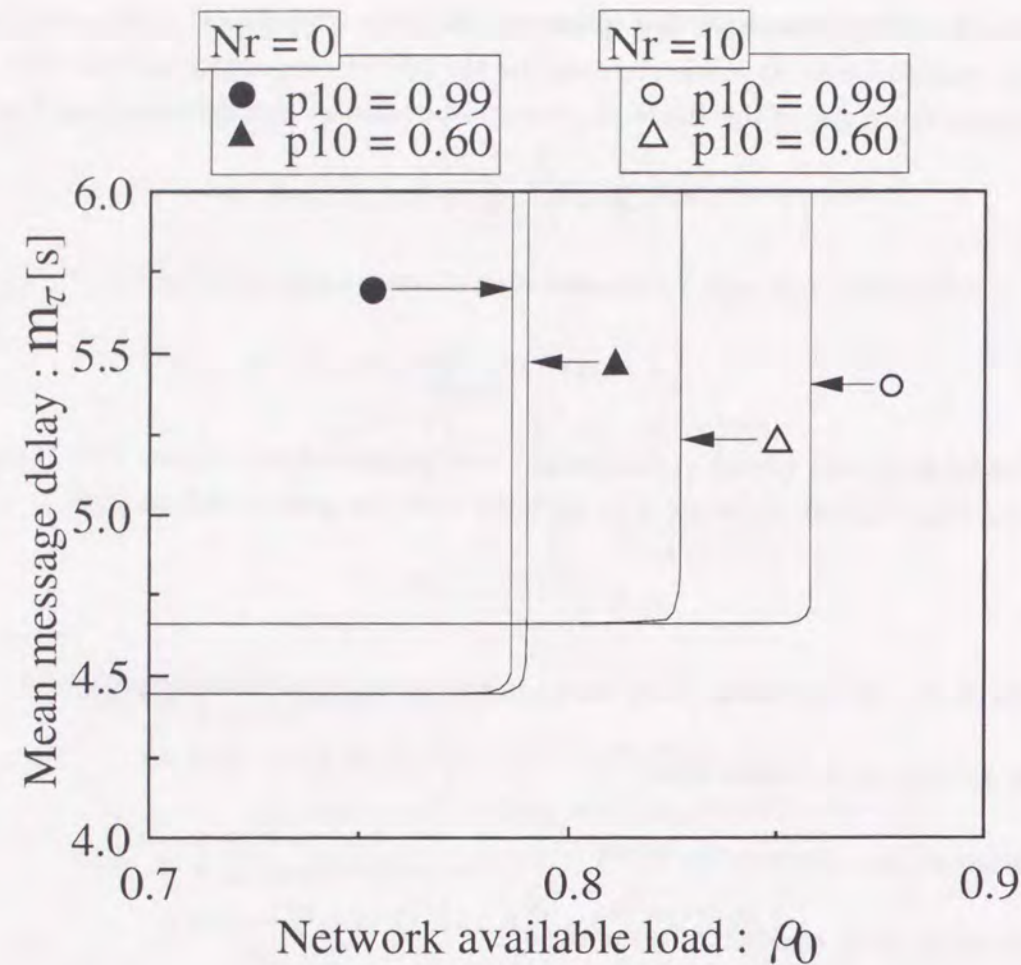


Figure 4.9: Impact of the available load.

#### 4.5.1 Impact for Available Load

Figure 4.9 shows the mean message forwarding delay (hereafter, it is written as the mean message delay)  $m_\tau$  as a function of  $\rho_0$ . When  $\rho_0$  is low, there is few retransmission and little change about  $m_\tau$  is seen. In this region,  $m_\tau$  is dominated by the message transmission delay. So, the less  $N_r$  is, the shorter  $m_\tau$  becomes.

As  $\rho_0$  increases, a cell loss starts to happen often. A cell loss causes retransmission, then retransmission increases the network load and makes more cell losses. In consequence, a number of retransmission grows explosively in a certain  $\rho_0$ . Above this point, it is impossible to increase  $\rho_0$ . This point is different for each comparative parameter. In order to avoid the divergence, we must set  $\rho_0$  low value. However, this makes it difficult to investigate the effect of error controls. Let this point denote the maximum throughput  $S_{max}$ . Describing more precisely,  $S_{max}$  is defined as the available network load that lower within the order of  $10^{-12}$  than the real divergence point.  $S_{max}$  is evaluated in substitution for  $m_\tau$ .

Hereafter, two cases are evaluated about the treatment of  $p_1$ : (1) fixing  $p_1 (= 1.0 \times 10^{-5})$  and (2) reflecting the network load to  $p_1$  (see section 4.4.4). In each case,  $m_\tau$  and  $S_{max}$  is evaluated respectively.

#### 4.5.2 Impact for Block Length

$L_B$  is the important system parameter, so the impact of  $L_B$  is very interesting. Figure 4.10(a) shows  $m_\tau$  and Fig 4.11(b) shows  $S_{max}$  as a function of  $L_B$ .  $\chi$  is fixed in both figures, so  $N_r$  increases with  $L_B$ . If block length is too short, the system performance will be degraded because of an overhead. Therefore, these figures are plotted from  $L_B = 7.616 \times 10^3$ .

Figure 4.10(a) expresses that  $m_\tau$  of  $\chi = 0.0$  increases with increasing  $L_B$  in a large  $L_B$  region. This is because that the more one block contains cells, the bigger the block loss probability becomes. On the other hand, there is few retransmission for  $\chi = 0.05$ , so  $m_\tau$  does not become worse with increasing  $L_B$ . The ratio of the FEC redundant cells in one block is constant, so small  $L_B$  means small  $N_r$  for  $\chi = 0.05$ . Therefore, the ability to correct a block becomes weak and  $m_\tau$  increases when a burst cell loss in a block happens ( $p_{10} = 0.6$ ) and  $L_B$  is small.

Figure 4.10(b) shows the following characteristics for  $\chi = 0.05$ .  $S_{max}$  is improved rapidly around the point that  $N_r$  just exceeds the mean number of cells lost continuously (i.e.  $\frac{1}{p_{10}D}$ ), because FEC-SSCS can not correct missing cells when cells are lost exceeding  $N_r$ . In the region that  $N_r$  is large enough to correct cell losses,  $S_{max}$  shows a gradual increase.

As the general tendency, it is good to make  $L_B$  long enough to correct burst cell loss when FEC-SSCS is used. Unless this is concerned,  $S_{max}$  would be worse compared with the case of  $\chi = 0.0$  because of the redundant cells in the case of  $p_{10} = 0.6$ .

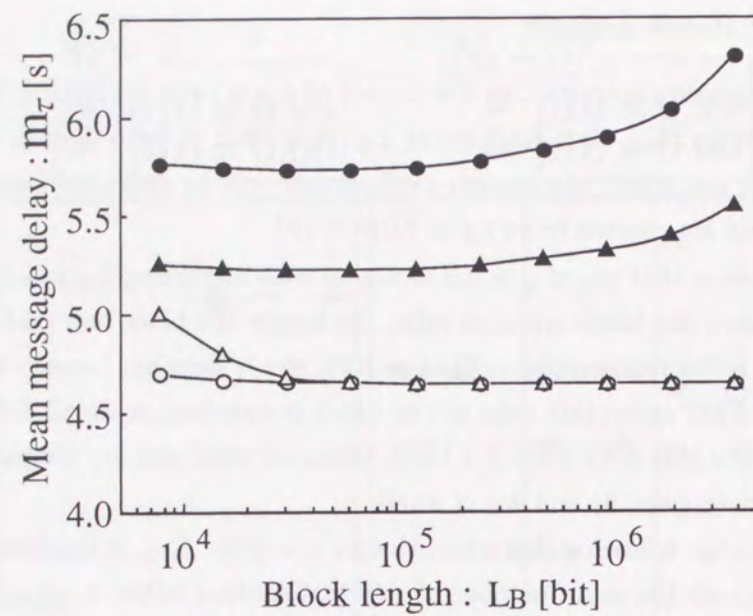
#### 4.5.3 Impact for Interface Rate

Since cells are transmitted at intervals of  $D$  slots, the interface rate  $I$  is defined as  $\frac{C}{D}$ . In order to change  $I$ ,  $D$  is fixed and  $C$  is varied. We set  $L_M = 1.0 \times 10^6$  for Figure 4.11 and  $L_M = 1.0 \times 10^{10}$  for Figure 4.12.

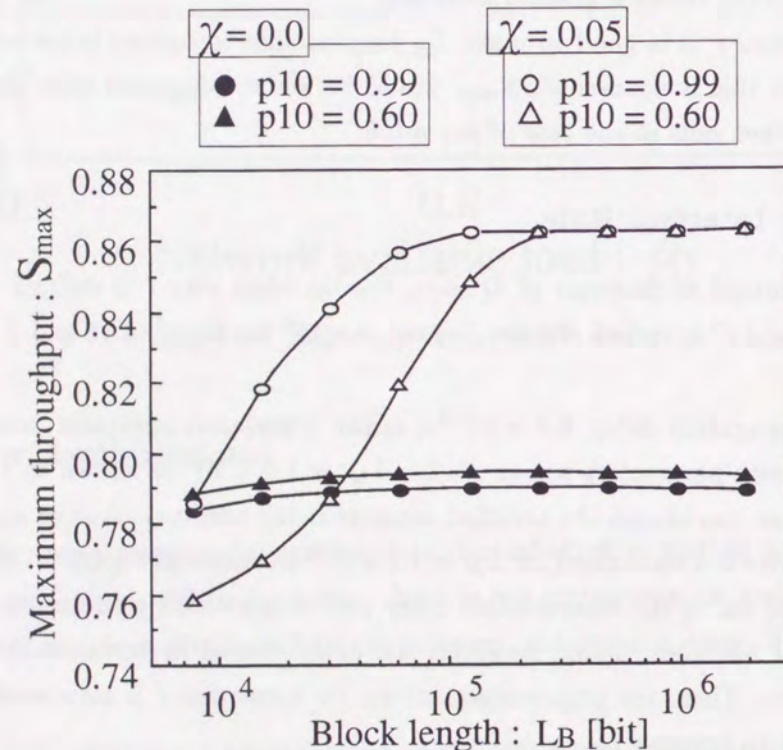
The round trip propagation delay,  $5.0 \times 10^{-3}s$ , is the theoretical minimum message delay. There is little difference among parameters  $p_{10}$  or  $N_r$  for  $L_M = 1.0 \times 10^6$  as shown in Figure 4.11(a). By increasing  $I$  enough, we can obtain the satisfied message delay property close to the theoretical limit. On the other hand, there is a saturation for  $L_M = 1.0 \times 10^{10}$  as shown in Figure 4.12(a). When  $I$  is low, the dominant factor of  $m_\tau$  is the transmission delay and it is possible to decrease  $m_\tau$  monotonously by increasing  $I$ . As  $I$  becomes higher, however, the delay caused by retransmission begins to be a dominant factor to  $m_\tau$ . Thus, the improvement of  $m_\tau$  by increasing  $I$  is saturated, and in this case, FEC-SSCS is efficient to improve  $m_\tau$ .

The reason why the saturation is seen only in Figure 4.12(a) is that the number of total retransmission during one message forwarding is proportional to the length of the message. In this case, the mean delay caused by retransmission is roughly calculated as  $1.39 \times 10^{-4}s$  for  $L_M = 1.0 \times 10^6$  and  $1.30s$  for  $L_M = 1.0 \times 10^{10}$ . When the length of message is small, we can neglect the effect of retransmission to the message forwarding delay even if the interface rate becomes fast.

Next, we consider the maximum throughput  $S_{max}$  in Figure 4.11(b) and 4.12(b). Recall that  $N_T$  indicated the maximum sequence number of the block whose NACK is received at the sender during another block transmission. Therefore, the faster interface rate becomes, the smaller  $N_T$  becomes. As a result, when  $N_T$  is between one and  $N_B - 1$ , the maximum throughput decreases with the interface



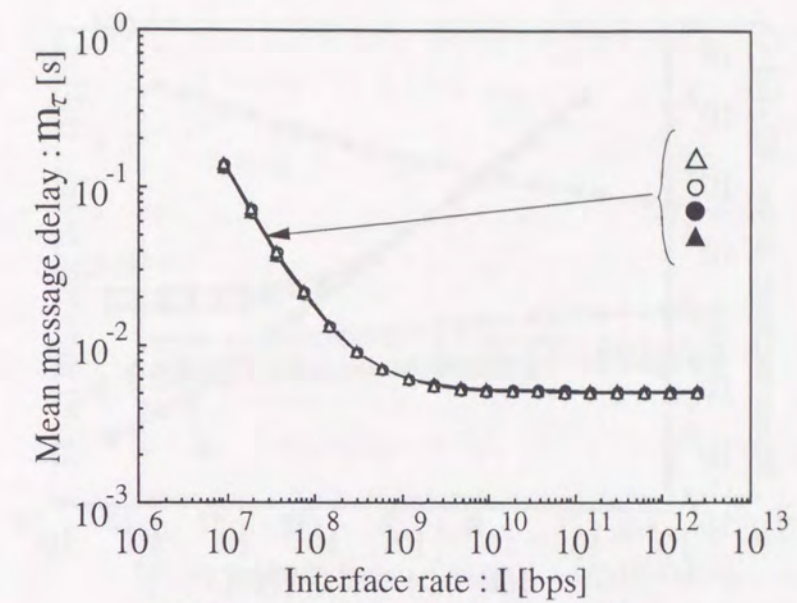
(a) Characteristic of message delay



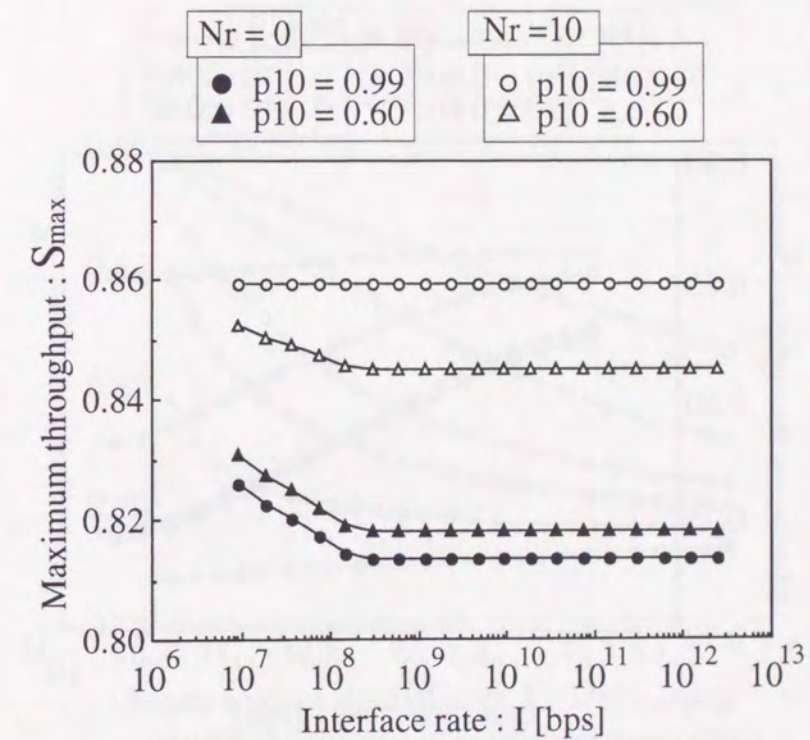
(b) Characteristic of maximum throughput

Figure 4.10: Impact of the block length.

rate increases because the number of invalid cells transferred in one retransmission grows. In the region that  $N_T = 0$ , i.e. there is no other transmission block when NACK for any block arrives at the sender, the increment of the interface rate does not give the growth of the invalid cells. So the maximum throughput in this region keeps a certain value. We can see this tendency in Figure 4.11(b) and Figure 4.12(b). For example, in the case of  $L_M = 1.0 \times 10^6$  and  $N_r = 0$ ,  $N_T$  becomes zero when  $I$  is greater than around  $2.37 \times 10^8$ .



(a) Characteristic of message delay



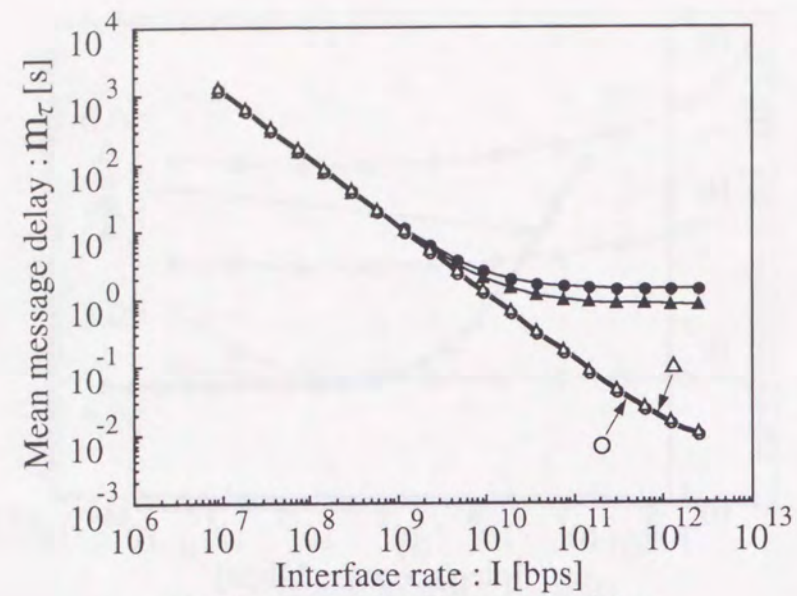
(b) Characteristic of maximum throughput

Figure 4.11: Impact of the interface rate [ $L_M = 1.0 \times 10^6$ ].

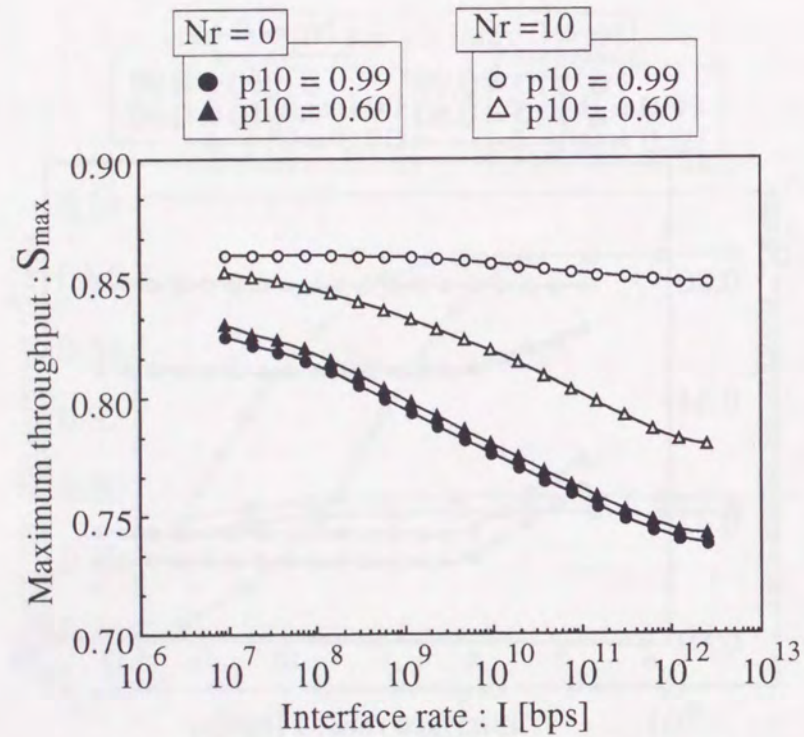
#### 4.5.4 Impact for Mean Number of Consecutive Cell Losses

We set  $C = 2.5 \times 10^9$  for Figure 4.13 and  $C = 2.5 \times 10^{12}$  for Figure 4.14. The difference among some  $N_r$  is relatively small for the mean message delay in  $C = 2.5 \times 10^9$ , so the vertical axis is plotted in linear scale in Figure 4.13(a).

$m_r$  is improved by introducing FEC-SSCS. The improvement can be seen dramatically when  $C$  (i.e.  $I$ ) is large as shown in Figure 4.14(a). If redundant cells are attached exceeding enough amount to



(a) Characteristic of message delay

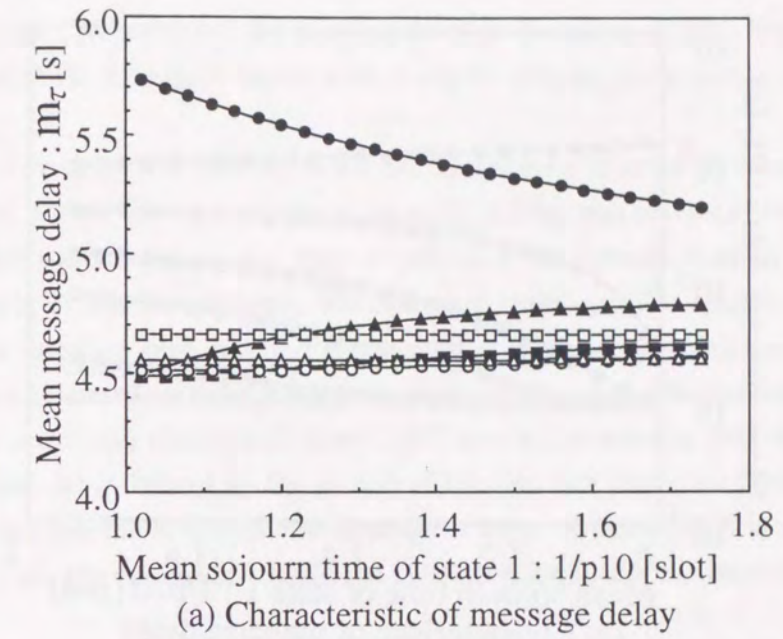


(b) Characteristic of maximum throughput

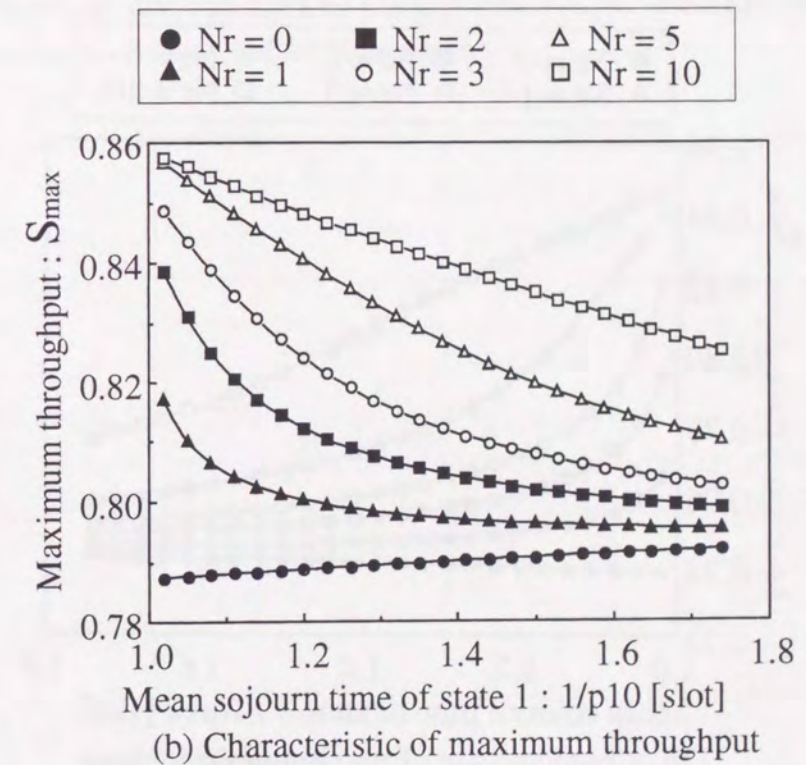
Figure 4.12: Impact of the interface rate [ $L_M = 1.0 \times 10^{10}$ ].

correct lost cells, it leads to grow the message transmission delay. Especially, the large  $N_r$  results in a long  $m_\tau$  in the case of the low  $C$  as shown in Figure 4.13(a), because the transmission delay is more serious than the propagation delay when  $C$  is low.

Since the cells transmitted during one round trip time followed by retransmission become invalid, the growth of  $\frac{1}{p_{10}}$  decreases the number of retransmission. Thus,  $m_\tau$  decreases monotonously as  $\frac{1}{p_{10}}$  increases. We can see this tendency in  $N_r = 0$ . When  $N_r \neq 0$ , however, the growth of  $\frac{1}{p_{10}}$  decreases



(a) Characteristic of message delay



(b) Characteristic of maximum throughput

Figure 4.13: Impact of the  $\frac{1}{p_{10}}$  [ $C = 2.5 \times 10^9$ ].

the ability of FEC-SSCS. For  $N_r \neq 0$ ,  $m_\tau$  increases monotonously as  $\frac{1}{p_{10}}$  increases, so we can say that the second effect is greater than the first one for  $N_r \neq 0$  (FEC-SSCS is used).

The same discussion can be applied for the maximum throughput  $S_{max}$  shown in Figure 4.13(b) and 4.14(b).

From the figures from 4.11 to 4.14, we can obtain the result that FEC-SSCS is efficient when  $I$  is high,  $L_M$  is large, and  $\frac{1}{p_{10}D}$  is small.

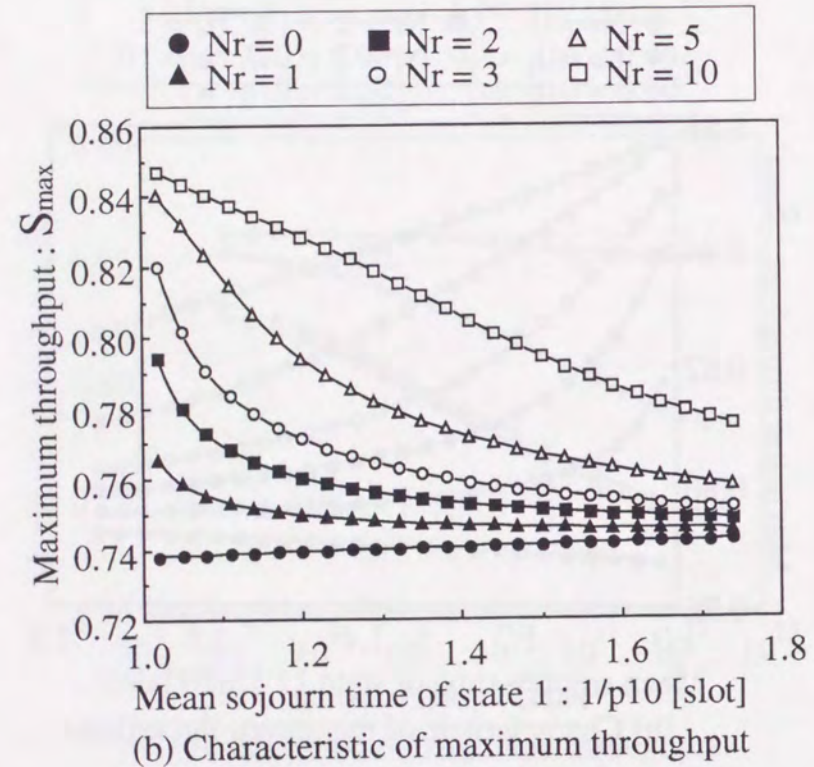
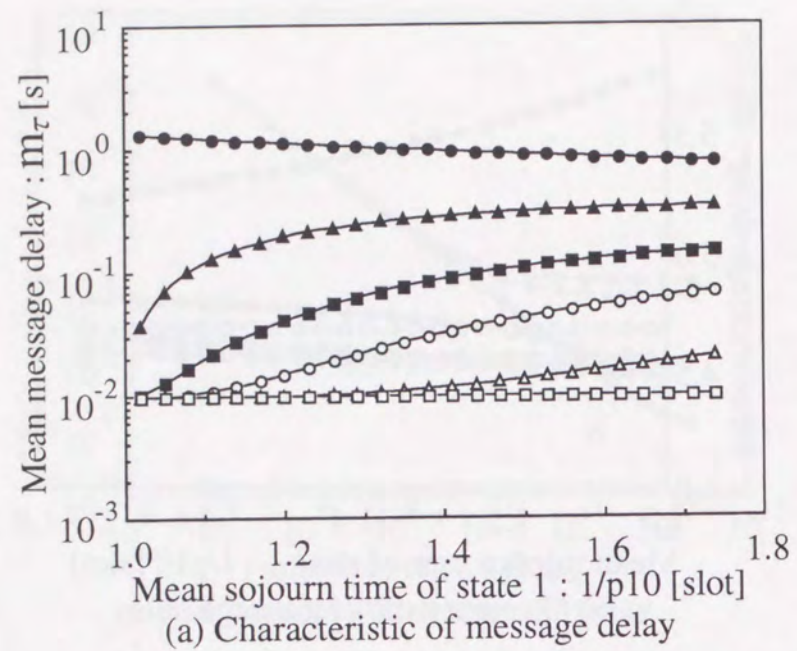


Figure 4.14: Impact of the  $\frac{1}{p_{10}}$  [ $C = 2.5 \times 10^{12}$ ].

## 4.6 Conclusion

The cell fragmentation of a block causes a degradation of the network throughput. Besides, the improvement of the interface rate in the ATM network makes the retransmission delay the main factor of the message forwarding delay. Hence, it is important to decrease the block loss probability for error-free services. The main proposed methods to satisfy this requirement are the selective cell discarding and the FEC-SSCS technique. From the viewpoint of the processing at ATM switches,

FEC-SSCS is attractive. We analyzed the message level performance of FEC-SSCS combined with GBN on the ATM network. The three layers were newly considered, the message, the block, and the cell.

The two state Markov chain was applied to the cell loss process in order to consider the burst cell loss tendency at ATM nodes. The mean message forwarding delay was evaluated for the case of fixing cell loss rate. On the other hand, in the case of reflecting the network load to the cell loss rate, the maximum throughput was investigated. We evaluated these qualities against the network load, the block length, the interface rate, and the mean number of consecutive cell losses. The following three conclusions were obtained. (1) The message forwarding delay explosively increases at the certain network load, so the maximum throughput exists. (2) There is a possibility that the improvement of the message forwarding delay derived by the growth of the interface rate is saturated if FEC-SSCS is not introduced and the volume of transferred message is large. (3) FEC-SSCS is very efficient when the interface rate is high, the volume of transferred message is large, and the burstiness of the cell loss process is small.

Through this analysis, we gave one index for the application region of the FEC-SSCS scheme which is available for error-free services on the ATM network.

## Chapter 5

### Conclusions

The control methods for guaranteeing and improving the quality of services on the ATM network have been investigated in this thesis. Services which are to be supported in B-ISDN are classified into two large categories, isochronous and error-free. Guaranteeing QOS is important for the former category service, and decreasing the block loss probability is significant for the latter one. The purpose of this research was to propose the new scheme assuring QOS for isochronous services efficiently and to analyze the performance of FEC-SSCS which is an available method to improve the requirement of error-free services. The contents and results of each chapter are summarized below.

In chapter 2, the necessity of the QOS control for isochronous services was described and three main techniques, the delay jitter absorption in AAL 1, the buffer priority control, and the stop-and-go queueing, were investigated. The time slot allocation on the ATM network is one of the most efficient method to guarantee the QOS of isochronous services. We proposed a virtual STM transmission on the ATM network, named as Q-STM.

The Q-STM method allocates cell transmitted positions for each call in order to realize cell loss free and delay jitter free transmission on the ATM network. Introducing a new frame concept "subframe", this method decreases the time switching delay with preserving a flexibility of bandwidth allocation. The ATM service class as well as the Q-STM one is introduced. Cells of the ATM service class are transmitted without time frame concepts and time slot reservation, so the statistical multiplexing gain is obtained even for Q-STM reserved slots.

We clarified the requirements for the Q-STM switch and compared some possible contractions for the input and output module respectively, then explained the cell action in one switching architecture. Moreover, the conditions which are demanded for the call setup procedure were described, and one realization was suggested. The Q-STM call setup process is organized by three processes, the calculation of the number of slots allocated for each subframe (*Process1*), the slots reservation on each passing link (*Process2*), and the assignment of the intra-route of the switch (*Process3*). The SLAD algorithm was considered for *Process1*, SI for *Process2*, and ATR for *Process3* respectively.

In chapter 3, the design issues of the Q-STM method were resolved and the availability were evaluated. Two design issues exist on this proposed scheme, (1) what algorithms should be used for the Q-STM call setup and (2) how many subframes show the best performance. Among three stage processes of the Q-STM call setup, we investigated the performance for *Process1* and *Process2* because these processes affect various qualities in the assumed architecture. For *Process1*, the SLAD algorithm

was compared with the random one from the viewpoint of the Q-STM call blocking probability and the QOS of the ATM service class; then we obtained the result that SLAD shows better performance than the random algorithm. For *Process2*, the QOS of the ATM service class using the SI algorithm was contrasted with that using random one; then we reached the result that the random algorithm has better capability than SI. The number of subframes affect three qualities: the Q-STM cell delay, the Q-STM call blocking probability, and the ATM service class QOS. Through the performance evaluations for these three qualities using SLAD, RD-2, and ATR, we roughly got the most efficient number of subframes, i.e. around 100.

In order to clarify the availability of the Q-STM method, it is important to evaluate two apprehended qualities: (1)the QOS of the ATM service class and (2)the Q-STM call setup time. The ATM service class corresponds to a low priority class. In general, the QOS of the low priority class is degraded by improving the QOS of the high priority class. We compared the QOS of the ATM service class to that of the low priority class on the absolute priority scheme. It was clarified that the degradation of the ATM service class QOS is much smaller than that of the low priority class on the absolute priority scheme. We analyzed the additional call setup time caused by introducing the Q-STM method, i.e. the processing time of SLAD, RD-2, and ATR. It was obtained that the additional call setup time is negligible. As a result, the availability of this method was clarified.

In chapter 4, the message level performance of FEC-SSCS on the ATM network was evaluated. Both the cell fragmentation of a block and the increment of the interface rate require the improvement of the block loss probability for error-free services. Therefore, the FEC-SSCS technique which decreases the block loss probability by adding some redundant cells for each block is available. We newly analyzed the message level qualities on the ATM network, i.e. considering three layers: a *message*, a *block*, and a *cell*. In order to take a burst cell loss at the ATM node into account, the two state Markov chain was applied to the cell loss process. For the treatment of the network load, two cases are considered: fixing the mean cell loss rate and reflecting the network load to it. The message forwarding delay was evaluated for the former case and the maximum throughput was investigated for the latter one.

The following three conclusions were obtained. (1)The message forwarding delay explosively increases at a certain network load, so the maximum throughput exists. (2)There is a possibility that the improvement of the message forwarding delay by increasing the interface rate is saturated in some environments. (3)FEC-SSCS is very efficient when the interface rate is high, the volume of transferred message is large, and the burstiness of the cell loss process is small.

Through this research, we have obtained the new scheme, "*Q-STM*" which assures the QOS of isochronous service on the ATM network and clarified the performance of the important QOS control method for error-free service, FEC-SSCS. I hope that this research might make some contributions toward the control methods for quality of service on ATM networks.

## Bibliography

- [1] J.Y.Hui : "SWITCHING AND TRAFFIC THEORY FOR INTEGRATED BROADBAND NETWORKS," *KLUWER ACADEMIC PUBLISHERS*, 1990.
- [2] M.N.Ransom and D.R.Spears : "Applications of Public Gigabit Networks," *IEEE Network Mag.*, pp.30-40, Mar. 1992.
- [3] R.Handel and M.N.Huber : "Integrated Broadband Networks," *ADDISON-WESLEY*, 1991.
- [4] *ITU-TS: Recommendation I.121*. "Broadband Aspects of ISDN," Geneva, 1991.
- [5] C.Partridge : "Gigabit Networking," *ADDISON-WESLEY*, 1993.
- [6] G.J.Armitage and K.M.Adams : "Packet Reassembly During Cell Loss," *IEEE Network Mag.*, Vol.7, 5, pp.26-34, Sep. 1993.
- [7] *ITU-T SGXVIII Draft recommendation I.362* : "B-ISDN ATM Adaptation Layer(AAL) functional description," June 1992.
- [8] *ITU-T SGXVIII Draft recommendation I.363* : "B-ISDN ATM Adaptation Layer(AAL) specification," June 1992.
- [9] ANSI T1S1.5/91-449 : "AAL5-A New High Speed Data Transfer AAL," *ANSI T1S1*, Nov. 1991.
- [10] J.Heinanen : "Multiprotocol Encapsulation over ATM Adaptation Layer 5," *RFC-1483*, July 1993.
- [11] *ITU-T SGXVIII Revised Recommendation I.361* : "B-ISDN ATM Layer specification," June 1992.
- [12] S.I.A.Shah, P.Ashton, and M.Wernik : "Evolution and Service requirements of CBR Applications on ATM Networks," *IEEE ICC '94*, pp.147-153, May 1994.
- [13] A.R.Reibman and A.W.Berger : "Traffic Descriptors for VBR Video Teleconferencing Over ATM Networks," *IEEE/ACM Trans. on Networking*, Vol.3, 3, pp.329-339, June 1995.
- [14] S.Yazid, H.T.Mouftah, and T.Yang : "Fast Reservation Protocol and Statistical Multiplexing: a comparative study," *IEEE ICC '94*, pp.733-737, May 1994.
- [15] *ITU-TS: Recommendation I.371*. "Traffic control and congestion control in B-ISDN," 1992 (revised in 1995).
- [16] W.Fischer, E.Wallweier, T.Worster, S.P.Davis, and A.Hayter : "Data Communications Using ATM : Architectures, Protocols, and Resource Management," *IEEE Commun. Mag.*, pp.24-33, Aug. 1994.

- [17] L.Wojnaroski : "Baseline Text for Traffic Management Sub-Working Group," *ATM Forum/94-0138*, Mar. 1994.
- [18] C.A.Kent and J.C.Mogul : "Fragmentation Considered Harmful," *ACM SIGCOMM '88*, pp.390-401, Aug. 1988.
- [19] A.Romanow and S.Floxd : "Dynamics of TCP Traffic over ATM Networks," *ACM SIGCOMM '94*, pp.79-86, Sep. 1994.
- [20] Draft RFC : "Default IP MTU for use over ATM AAL5," *IETF*, 1993.
- [21] I.Gard and L.-G.Petersen : "Supporting STM Traffic with ATM - A Switch Implementation," *ISS '95*, B1.3, Apr. 1995.
- [22] V.Jacobson, R.Braden, and D.Borman : "TCP Extensions for High Performance; RFC-1323," *Internet Request for Comments*, No.1323, Network Information Center, May 1992.
- [23] A.B.Bondi and W.S.Lai : "The influence of cell loss patterns and overheads on retransmission choices in broadband ISDN," *Computer Networks and ISDN Systems* 26, pp.585-598, 1994.
- [24] A.Bianco : "Performance of the TCP Protocol over ATM Networks," *ICCCN '94*, pp.170-177, Sep. 1994.
- [25] L.Kleinrock : "The Latency/Bandwidth Tradeoff in Gigabit Networks," *IEEE Commun. Mag.*, pp.36-40, Apr. 1992.
- [26] J.J.Bae and T.Suda : "Survey of Traffic Control Schemes and Protocols in ATM Networks," *Proc. IEEE*, Vol.79, 2, Feb. 1991.
- [27] W.A.Montgomery : "Techniques for Packet Voice Synchronization," *IEEE J.Sel.Areas Commun.*, SAC-1, 6, pp.1022-1028, Dec. 1983.
- [28] H.Uematsu and H.Ueda : "Cell Delay Variation Smoothing Methods for ATM-Based SDH Signal Transport System," *IEICE Trans. Commun.*, J76-B-I, 1, pp.48-59, Jan. 1993 (in Japanese).
- [29] K.Unemoto and N.Matsuo : "Voice Synchronization Methods for Packetized Voice Communication," *IEICE Trans. Commun.*, J75-B-I, 9, pp.606-615, Sep. 1992 (in Japanese).
- [30] R.C.Lau and P.E.Fleischer : "Synchronous Techniques for Timing Recovery in BISDN," *IEEE GLOBECOM '92*, pp.814-820, Dec. 1992.
- [31] *ITU-TS SG XVIII US contribution* : "Synchronous Residual Time Stamp: A Combination of SFET/TS," Dec. 1991.
- [32] R.Chipalkatti, J.F.Kurose, and D.Towsley : "Scheduling policies for real-time and nonreal-time traffic in a statistical multiplexer," *IEEE INFOCOM '89*, pp.774-783, Apr. 1989.
- [33] P.Yegani, M.Krunz, and H.Hughes : "Congestion Control Schemes in Prioritized ATM Networks," *IEEE ICC '94*, pp.1169-1173, May 1994.
- [34] C.Oh, M.Murata, and H.Miyahara : "Circuit Emulation Technique in ATM Networks," *IEICE Trans. Commun.*, E76-B, 6, pp.646-657, June 1993.
- [35] A.Y.M.Lin and Silvester J. : "Priority Queueing Strategies and Buffer Allocation Protocols for Traffic Control at an ATM Integrated Broadband Switching System," *IEEE J.Sel.Areas Commun.*, SAC-9, 9, pp.1524-1536, Dec. 1991.

- [36] K.Rothermel : "PRIORITY MECHANISMS IN ATM NETWORKS," *IEEE GLOBECOM '90*, pp.847-851, Dec. 1990.
- [37] G.Gallassi, G.Rigolio, and L.Fratta : "BANDWIDTH ASSIGNMENT IN PRIORITIZED ATM NETWORKS," *IEEE GLOBECOM '90*, pp.852-856, Dec. 1990.
- [38] S.J.Golestani : "A Stop-and-Go Queueing Framework for Congestion Management," *ACM SIGCOMM '90*, Sep. 1990.
- [39] S.J.Golestani : "Congestion-Free Communication in High-Speed Packet Networks," *IEEE Trans. Commun.*, Vol.39, 12, pp.1802-1812, Dec. 1991.
- [40] S.J.Golestani : "Congestion-Free Communication in Broadband Packet Networks," *IEEE ICC '90*, pp.308.3, 1990.
- [41] S.J.Golestani : "Duration-Limited Statistical Multiplexing of Delay-Sensitive Traffic in Packet Networks," *IEEE INFOCOM '91*, pp.323-332, 1991.
- [42] H.Satoh and Y.Ohba : "Switching Algorithm and Network Control in Framed ATM Networks," *IEICE Technical Report*, SSE92-22, May 1992(in Japanese).
- [43] M.J.Fischer and T.C.Harris : "A Model for Evaluating the Performance of an Integrated Circuit- and Packet-Switched Multiplex Structure," *IEEE Trans. Commun.*, COM-24, 2, pp.195-202, Feb. 1976.
- [44] G.F.Williams and A.L.-Garcia : "Performance Analysis of Integrated Voice and Data Hybrid-Switched Links," *IEEE Trans. Commun.*, COM-32, 6, pp.695-706, June 1984.
- [45] S.-Q.Li and J.W.Mark : "Performance of Voice/Data Integration on a TDM System," *IEEE Trans. Commun.*, COM-33, 12, pp.1265-1273, Dec. 1985.
- [46] C.-T.Lea : "What Should Be the Goal for ATM," *IEEE Network Mag.*, pp.60-66, Sep.1992.
- [47] N.Kamiyama, C.Ohta, H.Tode, M.Yamamoto, and H.Okada : "A Virtual STM Transmission Method Based on ATM Network," *IEICE Trans. Commun.*, J77-B-I, 5, pp.353-365, May 1994 (in Japanese).
- [48] H.Tode, N.Kamiyama, C.Ohta, M.Yamamoto, and H.Okada : "A Proposal of Quasi-STM Transmission Method in ATM-Based Network," *IEICE Trans. Commun.*, E76-B, 7, July 1993.
- [49] N.Kamiyama, C.Ohta, H.Tode, M.Yamamoto, and H.Okada : "Quasi-STM Transmission Method Based on ATM Network," *IEEE GLOBECOM '94*, pp.1808-1814, Nov. 1994.
- [50] N.Kamiyama, H.Tode, M.Yamamoto, and H.Okada : "A Quantitative Evaluation for the Introduction of Q-STM Method on the ATM Network," *IEICE Trans. Commun.*, J78-B-I, 9, pp.389-398, Sep. 1995 (in Japanese).
- [51] N.Kamiyama, H.Tode, M.Yamamoto H.Okada, and H.Ikeda : "Performance Evaluation on Applicability of Q-STM method to the ATM network," *APCC '95*, pp.751-755, June 1995.
- [52] J.M.Simmons and R.G.Gallager : "Design of Error Detection Scheme for Class C Service in ATM," *IEEE/ACM Trans. Networking*, Vol.2, 1, pp.80-88, Feb. 1994.
- [53] K.Noritake, S.Ushijima, and M.Hirano : "A Study on Selective Cell Discard Control in ATM-CL Network," *Technical Report of IEICE*, SSE94-77, June 1994 (in Japanese).

- [54] A.J.McAuley : "Reliable Broadband Communication Using a Burst Erasure Correcting Code," *ACM SIGCOMM '90*, pp.297-306, Aug. 1990.
- [55] K.Kawahara, K.Kumazoe, T.Takine, and Y.Oie : "Forward Error Correction in ATM Networks: An Analysis of Cell Loss Distribution in a Block," *IEEE INFOCOM '94*, pp.1150-1159, June 1994.
- [56] E.W.Biersack : "Performance Evaluation of Forward Error Correction in an ATM Environment," *IEEE J.Sel.Areas Commun.*, Vol.11, 4, pp.631-640, May 1993.
- [57] H.Esaki, G.Garle, T.Dwight, A.Guha, K.Tsunoda, and K.Kanai : "Draft Proposal for Specification of FEC-SSCS for AAL Type 5," *ATM-Forum Technical Contributions/95-326 R2*, Sep. 1995.
- [58] M.Murata, Y.Kikuchi, and H.Miyahara : "Performance of High Speed Data Transfer using a FEC Method in a Multimedia Network Environment," *IEICE Trans. Commun.*, J78-B-I, 8, pp.325-334, Aug. 1995 (in Japanese).
- [59] N.Kamiyama, M.Yamamoto, and H.Ikeda : "Message Forwarding Delay Analysis for Error Control of Data Transmission on ATM Network," will be published in *IEICE Trans. Commun.*, 1996.
- [60] L.D.Giovanni, A.M.Langellotti, L.M.Patitucci, and L.Petrini : "Dimensioning of Hierarchical Storage for Video on Demand Services," *IEEE ICC '94*, pp.1739-1743, May 1994.
- [61] Y.-H.Chang, D.Coggins, D.Pitt, D.Skellern, M.Thapar, and C.Venkatraman : "An Open-Systems Approach to Video on Demand," *IEEE Commun. Mag.*, Vol.32, 5, pp.68-80, May 1994.
- [62] D.Deloddere, W.Verbiest, and H.Verhille : "Interactive Video On Demand," *IEEE Commun. Mag.*, Vol.32, 5, pp.82-88, May 1994.
- [63] T.Chiang and D.Anastassiou : "Hierarchical Coding of Digital Television," *IEEE Commun. Mag.*, Vol.32, 5, pp.38-45, May 1994.
- [64] P.Pancha and M.E.Zarki : "MPEG Coding For Variable Bit Rate Video Transmission," *IEEE Commun. Mag.*, Vol.32, 5, pp.54-66, May 1994.
- [65] K.L.E.Law and A.L.-Garcia : "A Merging Network Scheme that Builds Large Sorting Networks," *IEEE GLOBECOM '94*, pp.105-110, Nov. 1994.
- [66] A.Huang and S.Knauer : "Starlite: A wideband digital switch," *IEEE GLOBECOM '84*, pp.121-125, 1984.
- [67] T.T.Lee : "Nonblocking Copy Networks for Multicast Packet Switching," *IEEE Trans. Commun.*, Vol.6, 9, pp.1455-1467, Dec. 1988.
- [68] M.J.Karol, M.G.Hluchyj, and S.P.Morgan : "Input Versus Output Queueing on a Space-Division Packet Switch," *IEEE Trans. Commun.*, COM-35, 12, pp.1347-1356, Dec. 1987.
- [69] S.W.Fuhrmann : "Performance of a Packet Switch with Crossbar Architecture," *IEEE Trans. Commun.*, Vol.41, 3, pp.486-491, Mar. 1993.
- [70] T.Aramaki, H.Suzuki, S.Hayano, and T.Takeuchi : "Parallel "ATOM" Switch Architecture for High-Speed ATM Networks," *IEEE ICC '92*, pp.250-254, June 1992.
- [71] M.G.Hluchyj and M.J.Karol : "Queueing in High-Performance Packet Switching," *IEEE J.Sel.Areas Commun.*, Vol.6, 9, pp.1587-1597, Dec. 1988.

- [72] H.Suzuki, H.Nagano, T.Suzuki, T.Takeuchi, and S.Iwasaki : "Output-Buffer Switch Architecture for Asynchronous Transfer Mode," *IEEE ICC '89*, pp.99-103, June 1989.
- [73] Y.-S.Yeh, M.G.Hluchyj, and A.S.Acampora : "The Knockout Switch: A Simple Modular Architecture for High-Performance Packet Switching," *IEEE J.Sel.Areas Commun.*, SAC-5, 8, pp.1274-1283, Oct. 1987.
- [74] Y.Doi, K.Endo, H.Yamada, T.Takahashi, and M.Suzuki : "A Very High-Speed ATM Switch With Input and Output Buffers," *ISS '92*, Oct. 1992.
- [75] J.-C.Bolot and A.U.Shankar : "Dynamical Behavior of Rate-Based Flow Control Mechanisms," *Computer Communication Review*, Vol.20, 2, pp.35-49, Apr. 1990.
- [76] H.Inai, Y.Kamichika, M.Murata, and H.Miyahara : "Rate-Based Congestion Control in High Speed Packet-Switching Networks," *IEICE Trans. Commun.*, E75-B, 11, pp.1199-1207, Nov. 1992.
- [77] H.Ohsaki, M.Murata, H.Suzuki, C.Ikeda, and H.Miyahara : "Performance of Rate-Based Control Method Using EPRCA - Steady State Analysis of EFCI Switch -," *Technical Report of IEICE*, IN94-147, Jan. 1995.
- [78] T.Hou and A.K.Wong : "Queueing Analysis for ATM Switching of Mixed Continuous-Bit-Rate and Bursty Traffic," *IEEE INFOCOM '90*, pp.660-667, 1990.
- [79] M.Wernik, O.A.-Magd, and H.Gilbert : "Traffic Management for B-ISDN Services," *IEEE Network Mag.*, pp.10-19, Sep. 1992.
- [80] H.Kroner : "Comparative performance study of space priority mechanisms for ATM channels," *IEEE INFOCOM '90*, pp.1136-1143, 1990.
- [81] J.Nagle : "On Packet Switches with Infinite Storage," *IEEE Trans. Commun.*, Vol.35, 4, pp.435-438, Apr. 1987.
- [82] E.Masuda : "Evaluation of Traffic Characteristics of  $n \times 64Kbit/s$  Calls in a Time Division Switching Network Satisfying the Sequence Integrity between  $n$  Time-Slots," *IEICE Trans. Commun.*, J70-B, 8, pp.919-927, Aug. 1987 (in Japanese).
- [83] S.K.Roh, K.H.Kook, J.S.Lee, M.Y.Chung, and D.K.Sung : "Performance of a Time Slot Searching Mechanism in Multi-Rate Circuit Switching Systems," *IEICE Trans. Commun.*, E77-B, 5, pp.650-655, May 1994.
- [84] T.Takahashi : "Time-Slot Sequence Integrity for  $(N \times 64)Kb/s$  Connection," *IEICE Trans. Commun.*, J69-B, 10, pp.1038-1045, Oct. 1986 (in Japanese).
- [85] R.A.Bruce, P.K.Giloth, and E.H.Siegel JR. : "No.4 ESS-Evolution of a Digital Switching System," *IEEE Trans. Commun.*, COM-27, 7, pp.1001-1011, July 1979.
- [86] T.J.Cieslak and P.J.Hickson : "Analysis and Simulation of No.4 ESS Network Performance," *IEEE Trans. Commun.*, COM-27, 1, pp.1-9, Jan. 1979.
- [87] V.E.Benes : "Mathematical theory of connecting networks and telephone traffic," *Academic Press*, 1963.
- [88] K.Gotoh : "Rearrangement Characteristics on Time Division T-S-T Networks," *IEICE Trans. Commun.*, J61-B, 3, pp.182-188, Mar. 1978 (in Japanese).



- [89] S.Ohta and H.Ueda : "A Rearrangement Algorithm for Three-Stage Switching Networks," *IEICE Trans. Commun.*, J69-B, 2, pp.139-146, Feb. 1986 (in Japanese).
- [90] H.Ueda : "Rearrangement Characteristics of Three-Stage Switching Networks," *IEICE Trans. Commun.*, J74-B-I, 7, pp.547-560, July 1991 (in Japanese).
- [91] N.Hujii : "Digital Cross-Connect System Control Algorithm Reducing Rearrangement Needs," *IEICE Trans. Commun.*, J74-B-I, 9, pp.666-674, Sep. 1991 (in Japanese).
- [92] IEEE Standard 802.6-1990 : "DQDB Subnetwork of a MAN," *IEEE Publications*, July 1991.
- [93] G.Mercankosk and A.Cantoni : "Characterization of a CBR Connection over a Channel with Known Bounded Delay Variation," *IEEE INFOCOM '93*, pp.1170-1177, Mar. 1993.
- [94] R.J.Simcoe and T.-B. Pei : "Perspectives on ATM Switch Architecture and the Influence of Traffic Pattern Assumptions on Switch Design," *ACM Computer Communication Review*, pp.93-105, Apr. 1995.
- [95] H.Ahmadi and W.E.Denzel : "A Survey of Modern High- Performance Switching Techniques," *IEEE J.Sel.Areas Commun.*, Vol.7, 7, pp.1091-1103, Sep. 1989.
- [96] F.A.Tobagi : "Fast Packet Switch Architectures for Broadband Integrated Services Digital Networks," *Proceedings of the IEEE*, Vol.78, 1, pp.133-167, Jan. 1990.
- [97] H.Yamada, S.Yamada, H.Kai, and T.Takahashi : "A Multi- Purpose Memory Switch LSI for ATM-Based Systems," *IEEE GLOBECOM '90*, pp.1602-1608, 1990.
- [98] G.Hetbuterne and A.Gravey : "A Space Priority Queueing Mechanism for Multiplexing ATM Channels," *Computer Networks and ISDN System*, No.20, pp.37-43, 1990.
- [99] N.Ogino, T.Saito, and H.Inose : "Evaluation of Large Scale T-S-T Types of Networks Controlled by Homing-Type Path Hunting Strategies," *IEICE Trans. Commun.*, J65-B, 5, pp.531-538, May 1982 (in Japanese).
- [100] H.Iino : "A Single Chip Supercomputer," *T.IEE Japan*, Vol.113-C, 9, pp.664-668, Sep. 1993 (in Japanese).
- [101] D.Toesley and J.K.Wolf : "On the Statistical Analysis of Queueing Lengths and Waiting Times for Statistical Multiplexers with ARQ Retransmission Schemes," *IEEE Trans. Commun.*, COM-27, 4, pp.693-702, Apr. 1979.
- [102] Z.Rosberg and N.Shacham : "Resequencing Delay and Buffer Occupancy Under the Selective-Repeat ARQ," *IEEE Trans. Commun.*, Vol.35, 1, pp.166-173, Jan. 1989.
- [103] K.Kumazoe, K.Kawahara, T.Takine, and Y.Oie : "Analysis of Packet loss Probability in ATM Networks," *Technical Report of IEICE*, SSE94-206, Feb. 1995 (in Japanese).
- [104] Y.Kikuchi, H.Inai, M.Murata, and H.Miyahara : "Comparative Evaluation of Error Recovery Schemes for High Bandwidth-Delay Product Networks," *Technical Report of IEICE*, SSE92-199, Mar. 1993(in Japanese).
- [105] G.R.Pieris and G.H.sasaki : "Performance of the Go-Back- $\infty$  Protocol Under Correlated Packet Losses," *IEEE Trans. Commun.*, Vol.41, 5, pp.660-663, May 1993.

- [106] M.Yoshimoto, T.Takine, Y.Takahashi, and T.Hasegawa : "Waiting Time and Queue Length Distributions for Go-Back-N and Selective-Repeat ARQ Protocols," *IEEE Trans. Commun.*, Vol.41, 11, pp.1687-1693, Nov. 1993.
- [107] M.J.Miller, and S.Lin : "The Analysis of Some Selective-Repeat ARQ Schemes with Finite Receiver Buffer," *IEEE Trans. Commun.*, COM-29, 9, pp.1307-1315, Sep. 1981.
- [108] M.J.Miller : "Error Control Techniques for Integrated Services Packet Networks," *IEEE J.Sel.Areas Commun.*, Vol.7, 5, pp.690-697, June 1989.
- [109] H.Suzuki and S.Sato : "Temporal Cell Loss Behavior in an ATM Multiplexer with Heterogeneous Burst Input," *IEICE Trans. Commun.*, E75-B, 12, pp.1346-1353, Dec. 1992.
- [110] H.Ohta and T.Kitami : "Simulation Study of the Cell Discard Process and the Effect of Cell Loss Compensation in ATM Networks," *IEICE Trans. Commun.*, E73, 10, pp.1704-1711, Oct. 1990.
- [111] D.R.Cox and H.D.Miller : "The Theory of Stochastic Processes," *London:Chapman and Hall*, 1965.
- [112] L.Kleinrock : "Queueing Systems, Volume I : Theory," *Wiley-Interscience*, New York, 1974.

