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Synopsis of Thesis

Title: Process development of ultra-fine pitch assembly for system-in-package devices (SiPデバイス用の超微細ピッチアセンブリープロセス開発)

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The goal of this thesis is to develop a robust assembly processes for system–in–package (SiP) module packaging with ultra fine–pitch solder interconnected devices, and propose a solution procedure to minimize/eliminate lead–free soldering defects in the assembly of high–density SiP modules.

Chapter 1 is the introduction, which presents the background and motivation for this research.

The literature relevant to the research objectives is reviewed in Chapter 2. In addition, this chapter briefly reviews the current status of research on the high–density solder interconnection and assembly of miniature chip components.

In Chapter 3, the assembly of 01005 miniature chip component was investigated. A detail study was carried out various experiments to optimize surface mount technology (SMT) process parameters, particularly focusing on solder paste type, stencil type, stencil design, vision camera type, and vacuum pick up nozzle type. The results of the study indicated that both electroformed and electropolished laser–cut stencils had a comparable print quality with respect to the solder volume delivered to the component pads. In terms of assembly yield performance, type 4 (size range : 20–38 μm) solder paste with a smaller sphere size gave a better overall yield and better paste deposition on the component pad, if used on a 0.08 mm–thick electroformed stencil with a 90 percent aperture. Temperature cycling between – 65 to 150°C, with up to 1,500 cycles, showed that no cracks were observed at the solder joints due to temperature cycling. The process and design change required for achieving a robust manufacturing process have been indicated and reported.

In Chapter 4, the effect of acid electrolyte and electropolishing conditions on the stencil printing performance of the small apertures was investigated. The results demonstrated that the acid solution for the electrolyte as well as the electropolishing time had a significant effect on the small stencil's aperture quality and the solder paste's stencil printing performance. In particular, a 95 wt.% phosphoric acid–based electrolyte showed encouraging results in terms of SMT assembly yields.

In Chapter 5, the effect of electropolishing on the printing performance of the small apertures was investigated. The results demonstrated that the deposited solder paste thickness was significantly better for the enhanced laser–cut stencil with electropolishing compared to the conventional electroformed stencils. Due to important improvements in the quality of the electropolished laser–cut stencil, and based on the results of this experiment, the electropolished laser–cut stencil is strongly recommended for the solder paste printing of fine–pitch and miniature components, especially in comparison to the typical laser–cut stencil.

In the Chapter 6, the effect of fine–grained structure on stencil printing performance was investigated. The fine–grained metallic material exhibited superior performance, indicating that the grain size of metallic materials has a significant effect on aperture dimensional tolerance, surface roughness of small aperture walls, and stencil printing performances. For a 150 μm pitch flip–chip assembly, type 7 (size range: 1–12 μm) solder paste with a smaller sphere size was observed to produce good results in terms of a better solder paste deposition on the component pads. Solder paste deposit volumes can also be controlled by optimizing appropriate printer parameters, such as stencil speed and print force.

In the Chapter 7, the effect of micro via–in–pad designs on tombstoning defect was investigated. In total, four different micro via–in–pad designs were compared (via–hole diameter): ultra small via–in–pads (10 μm),

small via–in–pads (20 μm) and large via–in–pads (60 μm), as well as designs with no via–in–pads and capped via–in–pads. The results indicated that capped via–in–pads exhibited the best results in preventing tombstoning, and provided a wide process window for the selection of process parameters. It is also indicated that tombstoning was found to rapidly reduced with both increasing stencil opening size and use of reflow profile with long preheat conditions.

In the Chapter 8, the effect of micro via–in–pad designs on voiding and spattering defects were investigated. The results indicate via–holes were seen to create bigger voiding than smaller via–holes. For smaller via–holes, spattering is a greater problem than voiding in solder joints. Capped via–in–pads exhibited the best results in preventing voiding and flux spattering, and provided a wide process window for the selection of process parameters. The findings provide certain process guidelines for surface mount assembly with via–in–pad substrate design. The strategy is to prevent voiding and spattering by adopting capped via–in–pads, if possible, when applying micro via–in–pads with the 95wt.%Sn–5wt.%Sb solder alloy system.

In the Chapter 9, the effects of reworked board assemblies with lead–free BGA packages was investigated. The results of the study indicated that the use of retrofit board fixture has proven to be most efficient method of controlling the temperature of board and bottom side of rework equipment and thermal uniformity during rework process. The reworked BGAs passed through thermal cycling of up to 1,180 cycles without failures. However, the reworked BGA components showed an approximate 36 percent reduction in the drop reliability over the non–reworked BGA components. The adjacent passive component was also degraded the shear strength after the rework process, resulting in a joining reliability reduction of approximately 24 percent.

From the knowledge gathered, process guidelines are developed for the assemblies of high–density SiP module platform with miniature components and ultra fine–pitch solder interconnected devices.

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論文審査の結果の要旨及び担当者

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論文審査の結果の要旨

近年の携帯機器デバイスの実装においては、超微細部品の鉛フリーはんだ付け技術による超高密度実装を如何に高いスループットで信頼性高く行うかが、技術開発に強く求められている。本論文は、信頼性の高いシステム・イン・パッケージ（SiP）鉛フリーはんだ高密度実装のための、設計要素の選択、設計指針の確立、および、実験手法の開発に取り組むものである。一連の評価において、極小チップ部品を用いた高信頼性実装パラメータを評価し、以下の成果を得た。

微細部品の代表として01005チップ部品を用い、スクリーン印刷におけるクリームはんだタイプ、スクリーン版タイプ、スクリーン版開口率、部品マウントにおけるカメラによる可視化法と真空吸引ノズルなどの影響を詳細に調べ、生産性へ与える影響を明にした。

超微細部品のサイズをパラメータとし、基板表面実装における生産性評価、欠陥評価、温度サイクル試験前後の強度試験による信頼性評価を行った。その結果、はんだ粒子径が小さいほど実装強度のばらつきが少なく、スクリーン印刷におけるメタルマスクの孔表面をエッチングにより粗さを小さくすることで生産性が改善されることが明らかになった。また、メタルマスクの材質やエッチング方法も、生産性へ大きな影響を与えた。

微細部品の表面実装において問題となるツームストーン、ボイド、はんだはじき等の欠陥形成を抑制する策として、基板上の電極部に形成するマイクロビアの大きさを設計パラメータとし、その生産性へ与える効果を評価した。マイクロビアの存在はボイド形成を促進し、極微少ビアにおいてはんだはじきが生じやすいことが明らかになった。

BGA部品のリワークはんだ付けとその信頼性へ与える影響を、特に、せん断強度および落下衝撃試験を用いて評価したところ、電極に非接触状態ではんだ鏝を操作する手法の優位性が確認された。リワークしたBGAの実装強度が低下することに加え、隣接する微細受動部品の実装強度も低下することが明らかになった。BGAのリワーク後は、アンダーフィルの採用が望ましいことが示された。

以上のように、本論文では最新の超微細部品を鉛フリーはんだにより高密度表面実装する場合の諸問題に取り組み、各種プロセスパラメータが実装に与える生産性や信頼性へ与える影響を明らかにした。本研究により得られた結果は、今後の01005サイズ等の超微細部品、CSP、BGA、あるいは、高密度SiPなどの様々な超微細実装技術の展開において、多大の貢献が期待されるものである。

よって本論文は博士論文として価値あるものと認める。