Doctoral Dissertation

Process development of ultra-fine pitch assembly for system-in-package devices

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Abstract

This dissertation describes the development of robust assembly processes for a high-density system-in-package (SiP) with lead-free solder interconnected devices, including various elemental selection criteria, design strategies, and experimental techniques. A comprehensive study was undertaken to evaluate various assembly parameters of 01005s as they relate to highly reliable products. The study evaluated solder printing-related parameters, such as types of solder paste, stencil, and stencil design, and pick-and-place machine-related parameters, such as types of vision camera, and vacuum pick-up nozzle. This study identifies and evaluates the key parameters affecting solder paste printing. These include stencil-related parameters, such as laser machine type, laser-cutting time, electrolyte type and electro-polishing time, and metallic stencil material type, and printing process-related parameters, such as solder paste type, print speed, and print pressure. In addition, three types of stencils (laser-cut stainless steel with coarse-grained SUS304 microstructure, laser-cut stainless steel with fine-grained SUS301 microstructure, and electroformed nickel) were investigated by measuring transfer efficiency as a function of the area ratio of the stencil apertures. This study proposes a solution to assembly problem by minimizing or eliminating soldering defects, such as tombstoning, voiding, and spattering in the assembly of 0201 chip components using micro via-in-pads of 95 wt.%Sn-5 wt.%Sb solder alloy. Four different micro via-in-pad designs were compared: 1) ultra-small via-in-pads; 2) small via-in-pads; 3) large via-in-pads; 4) capped via-in-pads, and no via-in-pads. Furthermore, this study designed experiments to evaluate multiple alternatives for several steps in the reworking process. Two commonly used techniques for cleaning pads were evaluated: the manual soldering iron and the semi-automatic system. Boards with and without retrofit fixtures were evaluated. Because the reliability of the reworked solder joint was also a concern, a reliability study consisting of cross-sectional analysis, scanning electron microscopy (SEM), thermal cycling, drop shock, and shear

test was conducted to determine the reliability of the reworked solder joints. In summary, based on the results of this study, recommendations are made for mass production and implementation of emerging packages, such as 01005s, flip-chips, CSPs, and BGAs. In addition, the findings provide process guidelines for a high-density SiP module with ultra-fine pitch solder interconnected devices and lead-free solder alloys.

Preface

This dissertation is submitted for the degree of Doctor of Philosophy at Osaka University. The doctoral dissertation work was carried out under the supervision of Professor Dr. Katsuaki Suganuma in the Department of Adaptive Machine Systems at Osaka University between the years of 2007 and 2013. This dissertation is written based on author's over twelve years experience in advanced microelectronics packaging and in the development of interconnection technology, especially soldering and surface mount technology for various applications. Except where acknowledgement and reference to previous work is made, this work is, to the best of my knowledge, original, and has been carried out without collaboration. Neither this, nor any substantially similar dissertation has been, or is being, submitted for any other degree, diploma or qualification at any other university. This dissertation contains fewer than 60,000 words, and is identical to that which was examined, except for corrections as required by the examiners. The dissertation consists of ten chapters, which are grouped into six parts for convenience. Chapter 3 through 9 is the core parts of this study which cover the objective and overview, experimental procedures, results and discussions, and summary. These chapters were written for publication as research articles.

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Abbreviations

BGA	Ball Grid Array
BT	Bis-maleimide Triazine
CPU	Central Process Unit
CrN	Chromium Nitride
CRT	Cathode Ray Tubes
CSP	Chip Scale Package
CTE	Coefficient of Thermal Expansion
DC	Direct Current
DCA	Direct Chip Attach
DIC	Digital Image Correlation
EDX	Energy Dispersive X-Ray
EMC	Epoxy Mold Compound
ENIG	Eletronics Nickel and Immersion Gold
EP	Electropolishing
EPA	Environmental Protection Agency
FC	Flip Chip
FCOB	Flip Chip on Board
IC	Integrated Circuit
IMC	Intermetallic Compound
IPC	Institute for Interconnecting and Packaging Electronic Circuits
IEEE	Institute of Electrical and Electronics Engineers
IMC	Intermetallic Compound
ITRS	International Technology Roadmap for Semiconductor
JEIDA	Japan Electronic Industry Development Association
JEITA	Japan Electronics and Information Technology Industries Association
LSL	Lower Specification Limit
MCM	Multi Chip Module
MTTF	Mean Time to Failure
MUF	Molded Underfill
NSMD	Non Solder Mask Defined
PA	Power Amplifier
PBA	Printed Circuit Board Assembly
PCB	Printed Circuit Board
PDA	Personal Data Assistant
PIP	Package in Package
POP	Package on Package
PPM	Parts Per Million

PWB	Printed Wiring Board
RF	Radio Frequency
ROHS	Restriction of Hazardous Substances
SE	Standard Error
SEM	Scanning Electron Microscope
SD	Standard Deviation
SiP	System in Package
SMD	Solder Mask Defined
SMD	Surface Mount Device
SMT	Surface Mount Technology
SoC	System on Chip
TiN	Titanium Nitride
TSV	Through Silicon Via
UFP	Ultra Fine Pitch
USL	Upper Specification Limit
YAG	Yttrium Aluminum Garnet
WEEE	Waste of Electrical and Electronic Equipment

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This doctoral dissertation would not have been possible without the support of many people. First, I am most grateful to my advisor Professor Dr. Katsuaki Suganuma for his guidance, advice, and encouragement throughout my pursuit of this degree. His advice has been invaluable, and he has supported my motivation and encouraged my determination at the highest level. I have learnt valuable lessons under his guidance.

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I would like to thank the current members and Korean alumni of the Suganuma Laboratory of ISIR at Osaka University. I want to thank Dr. Jung-Lae Cho for helping with the administrative procedure for doctoral dissertation evaluation. I also thank Ms. Keiko Suzuki, Secretary for her helpful assistance and kindness. Among the alumni, I thank Dr. Sung-Joon Kim and Dr. Chang-Jae Kim of Samsung Electronics Co., Dr. Jae-Ean Lee of Samsung Electro-Mechanics Co., Dr. Do-Seop Kim of Hyundai Motor Co., and other former members.

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PART I: AN INTRODUCTION AND OVERVIEW

Chapter 1

Introduction

The first chapter of this dissertation will introduce the motivation and historical background for the current study. System-on-chip (SoC) technology has historically brought challenges to engineers, from design to final test. So, the industry has been searching for solutions that can implement SoCs with relatively less difficulty. In the packaging industry, system-in-package (SiP) technology is a potential solution for reducing or eliminating SoC bottlenecks. Therefore, the trend of system products toward integration and shrinking profiles not only drives design demand for SoCs but also places the spotlight on new SiP packaging technology. Solders have been commonly used as interconnecting material for electronic packaging and interconnection assembly, providing electrical, thermal, and mechanical functions. With the implementation of surface mount technology (SMT), solder paste and soldering, which are the most practical and viable material and process system, respectively, in mass production, continue to play a crucial role to the overall performance and reliability of electronic circuit assemblies. The goal of this dissertation was to develop a robust assembly processes for SiP devices, and propose a solution procedure to minimize/eliminate lead-free soldering defects in the assembly of 01005 chip components. The organizations of this dissertation are given at the end of this chapter.

1.1 Motivations

The five basic options available for the assembly and joining of engineering components are as follows [1]:

- Mechanical fastening
- Adhesive bonding
- Welding
- Solid-state joining
- Soldering and brazing

The schematics of these joining methods are shown in Figure 1.1. Although the five methods have a number of features in common, they also have significant differences. Mechanical fastening involves the clamping together of components without fusing the joint surfaces. This method often, but not always, relies on the use of clamping members, such as screws and rivets. Adhesive bonding involves the use of a polymeric material, which often contains various additives, to "stick" the components together. The process involves a chemical reaction, which may simply comprise the exposure of the adhesive to air, leading to the formation of a hydrogen-type bond between the cured adhesive and the respective components. Welding involves the fusion of the joint surfaces by controlled melting, in which heat is directed toward a particular joint. Commonly used heating sources are plasma arcs, electron beams, lasers, and electrical current, which are applied through the components and across the joints (electrical resistance). The term, solid-state joining, covers a very wide range of joining processes. The two extremes are pressure welding and diffusion bonding. Pressure welding, at its simplest, involves the physical deformation of two abutting, faying surfaces to disrupt any intervening surface films and enable direct metal-to-metal contact. Diffusion bonding in its purest form merely requires placing two faying surfaces in contact and heating the assembly until the voids at the interface have been removed by diffusion. In soldering and brazing, a molten filler metal is used to wet the mating surfaces of a joint, with or without the aid of a fluxing agent, leading to the formation of metallurgical bonds between the filler and the respective components. Soldering may be defined as "a process by which metals may be joined via a molten metallic adhesive (the solder),

which on solidification forms strong bonds [usually intermetallic compounds (IMC)] with the adherents". Soldering is generally restricted to alloys with a liquidus temperature below 450 °C. This differs from brazing, in which the added metal generally has a melting range above 450 °C, but below the metals to be joined [1].

Solders are typically classified as either soft or hard. Some confusion often results from this convention because, if the melting temperature criterion is applied, some hard solders are really brazing materials. Soft solders typically consist of alloys containing lead and tin, but they often contain In, Bi, Sb, or Ag. In practice, most soft alloys melt at temperatures lower than 450 °C, usually between 180 °C and 300 °C. High-Sn solders, typical of Pb-free solders, tend to be stiffer, harder, and less ductile compared to high-Pb solders. Hard solders often contain metals such as Au, Zn, Al, and Si [2].

Although the soldering technique has been used since Roman times, it is only in the last few decades that the performance of soldered joints in electrical and electronic devices has received detailed attention. Now, because electronic technology is shortly to become the largest industrial sector, with an estimated output of some 10^{13} joints per annum [3], solders and soldered joints are regarded as pivotal to future developments in electronics. Furthermore, because of continuing miniaturization and ever-increasing performance demands, their reliability in service has become subject to severe testing.

Previously, it was sufficient to prescribe solders based on their processability (i.e., flow, wetting, and chemical characteristics). However, the structural integrity of the joint, and hence the mechanical behavior of solders, has become equally important. In addition, from the environmental perspective, it is necessary to eliminate lead from solders and pollutants emitted into the atmosphere by the cleaning and fluxing processes [4].

In the electronics industry, soldering is the preferred method for attaching components to printed circuit boards (PCB) or chips to substrates. On traditional boards, the integrated circuit is built in a dual-in-line package and solder is attached to the holes in the board.

A surface mount assembly is the composite structure of the printed circuit board, the solder joint, and the surface mount component. Unlike traditional through-hole technology (THT), SMT has smaller components that are soldered directly to the pad surface of the PCB.

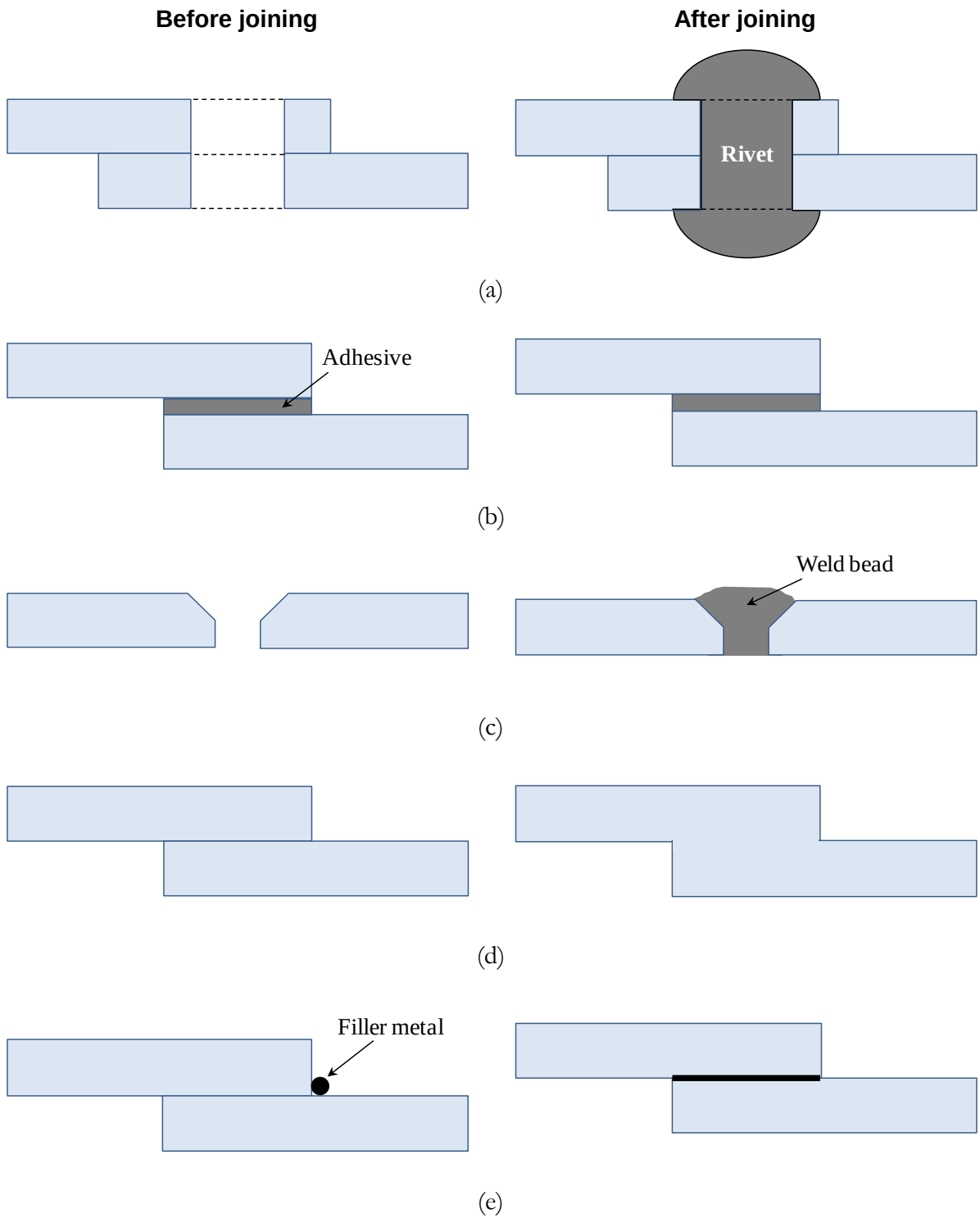


FIGURE 1.1 Principal methods for joining engineering materials [1].

Notes: (a) mechanical fastening; (b) adhesive bonding; (c) welding; (d) diffusion bonding; (e) soldering and brazing.

Thus, the solder joint is the sole mechanical means of attaching the component to the PCB, in addition to acting as the electrical connection and the means of heat dissipation [4]. Schematic examples of common joint geometries used for attaching components to boards are shown in Figure 1.2. With the trend towards greater interfacial areas, a layered structure may be used to accommodate thermal strain. Leadless (i.e., without leads, *not* lead, or Pb) chip carriers are most vulnerable to thermal strains because of their structural rigidity. However, this problem is reduced by the incorporation of compliant leads in leaded chip carriers. In particular, the large mismatch of the coefficients of thermal expansion (CTE) of heterogeneous components has a decisive influence on interconnect reliability. The process is shown schematically in Figure 1.3. Solders are usually much softer than the other joint components are, and the majority of the strain generated is connected within the thin layer of solder adhesive, as shown in Table 1.1. Hence, materials, interfaces, and interconnect technologies must combine to minimize the mechanical stresses in interconnects.

1.1.1 Implementing lead-free electronics [2,7]

Pb has been widely used in the industry for a long time. Of the approximately 5 million tons of lead consumed globally every year, 81 percent is used in storage batteries, with ammunition and lead oxides together accounting for about 10 percent, as shown in Table 1.2 [8]. However, despite the long-term acceptance of lead by human society, lead poisoning is now well recognized as a health threat.

The environmental impact of lead dates back to 1887 when U.S. medical authorities diagnosed lead poisoning in children and later, (1904), linked this poisoning to lead-based paint. In 1921, Thomas Midgley discovered that tetraethyl lead curbs engine knock when added to gasoline. The following year the public health service warned of the dangers of leaded gasoline. In spite of that warning, leaded gasoline went on sale in 1923 [9] and continued to be sold in the USA until the late 1990s when it was banned.

With the Clean Air Act of 1970, the U.S. Environmental Protection Agency (EPA) proposed the phase-out of lead in gasoline in 1972. Eleven years later, the EPA reported that the

amount of lead in gasoline had dropped 50 percent and lead levels in blood dropped 37 percent between 1976 and 1980. By 1991, there was a 78 percent reduction in lead-levels in blood [9].

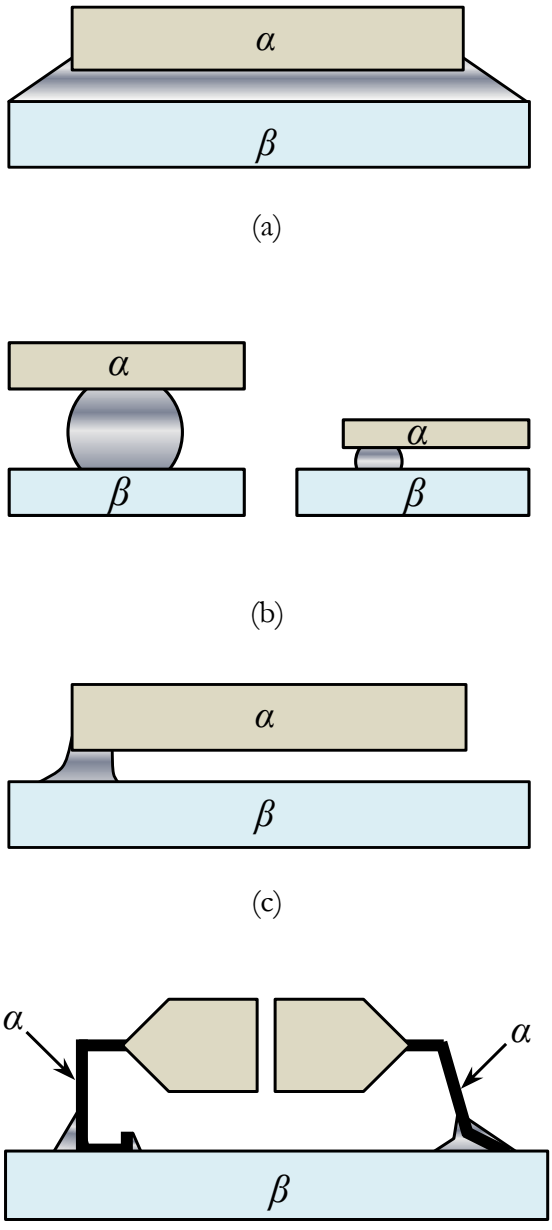


FIGURE 1.2 Some common solder joint configurations. Shaded area is solder and *a*, *β* are different materials [5].

Notes: (a) die or substrate bonding; (b) solder bump; (c) leadless chip carrier; (d) leaded chip carrier.

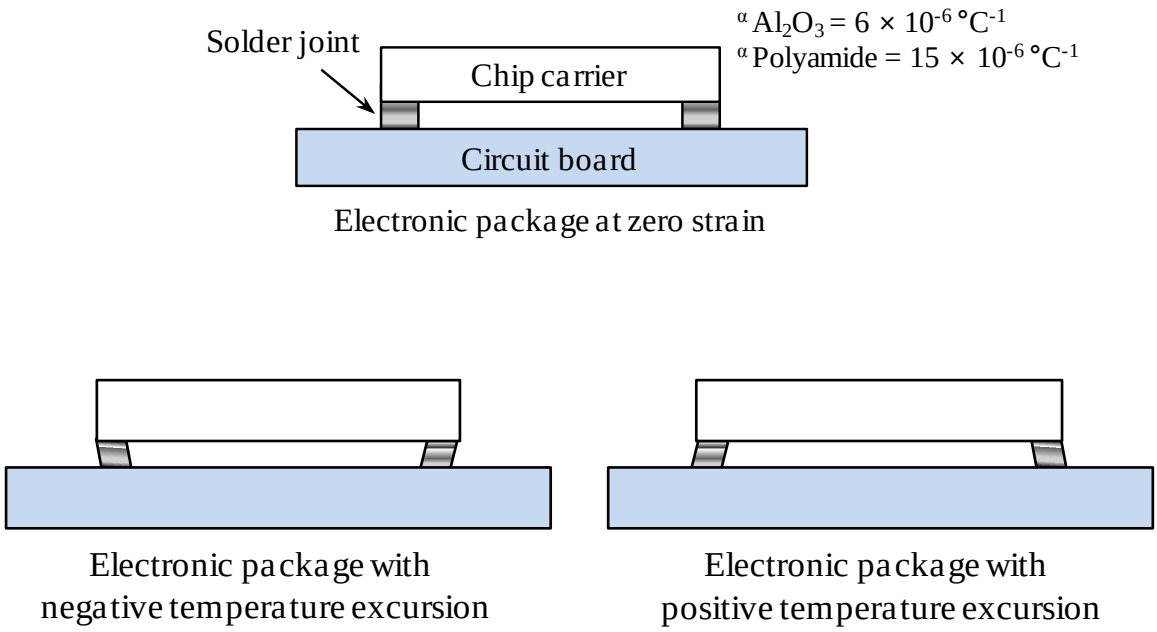


FIGURE 1.3 Development of strains in an electronic device [6].

TABLE 1.1 Coefficient of thermal expansion for materials used in electronic assemblies [4]

Material	**Expansion coefficient ($\times 10^{-6} K^{-1}$)**
Solder (63Sn-37Pb)	22
Solder (95Pb-5Sn)	28.7
Solder (96.5Sn-3.5Ag)	22
Alumina	6.5
Aluminum nitride	2.7
Copper	16.7
Silicon	2.5
Epoxy resin	26

TABLE 1.2 Lead consumption by product [8]

Product	Consumption (%)
Storage batteries	80.81
Other oxides (paint, glass and ceramic products, pigments, and chemicals)	4.78
Ammunition	4.69
Sheet lead	1.79
Cable covering	1.40
Casting metals	1.13
Brass and bronze billets and ingots	0.72
Pipes, traps, other extruded products	0.72
Solder (excluding electronic solder)	0.70
Electronic solder	0.49
Miscellaneous	2.77

In the United States, the Clean Water Act of 1986 banned the use of lead alloy solders for portable water systems, and lead in household paint has been prohibited since before 1970. The dramatic decline in blood lead levels in adults and children since 1970 has been the result of regulatory and voluntary elimination of lead in gasoline, drinking water plumbing connections and fittings, and paint.

In the past, the health and safety concerns with lead poisoning have focused on lead-based paint and lead in gasoline. However, the increasing quantity of scrap electronic products disposed into landfills has raised the question of the environmental impact of this source of lead. Studies in 1991 by Allenby *et al.* [10] examined the potential for replacing lead-based solder and concluded that there were no viable alternatives at that time. They also suggested that the total

environmental impact of lead and its alternatives, from mining, through manufacture, use, and end-of-life should be considered.

In the early 1990s, legislation was proposed in the U.S., but no regulatory action was taken. The movement toward lead-free electronics emerged into concrete legislation in Europe on June 13, 2000 when the European Commission adopted two proposals: A Directive on Waste of Electrical and Electronic Equipment (WEEE), and a Directive on the Restriction of Hazardous Substances (ROHS). The WEEE requires Member States to set up take-back centers for end-of-life recovery at no cost to the consumer. The initial WEEE included the ROHS requirements and set 2004 as the date for lead-free electronics [lead in cathode ray tubes (CRTs) is exempt]. Since then the deadline was established as July 01, 2006. In Japan, the Japan Electronic Industry Development Association (JEIDA) developed the roadmap 2000 for commercialization of lead-free solder. Thus, the environmental impact of lead from electronics and lead-free alternatives is an important issue to explore.

Lead-free electronics is now a worldwide trend. By 2003, approximately 70–80 percent of Japanese electronics companies had introduced lead-free products [11]. Their current goal is to remove lead from all electronic products by the end of 2005. In South Korea, the major consumer electronics export country, approximately 340 electronics companies, representing 95 percent of South Korea's electronics production, have participated in a voluntary program to phase out all the lead banned under the European RoHS directive, making an effort to ensure its electronic products have access to the European market. As time goes by, more and more original equipment manufacturers and their subassembly supplier are joining in lead-free production. Lead-free is becoming a global trend in the electronics industry.

1.1.2 Miniaturized electronics assembly

Miniaturization continuous to accelerate for portable consumer electronics, particularly for consumer electronic products like mobile phones, personal data assistants (PDA), camcorders, laptops, cameras and MP3 players. In fact, another driving force in product miniaturization is the increasing complexity of features and functions, accompanied by a lower cost. This market dynamic has accelerated the development and use of finer pitch and smaller passive components with high density, both in design and assembly technologies [12].

Small and thin packages with high function density are key for competitiveness in mobile and handheld applications. The need for smaller size, lighter weight, high function density and higher performance has driven the increase in the pin count number, as shown in Figure 1.4. This increase in pin count number not only directly drives the evolution of packaging types, but also indirectly drives the trend toward miniaturization [14].

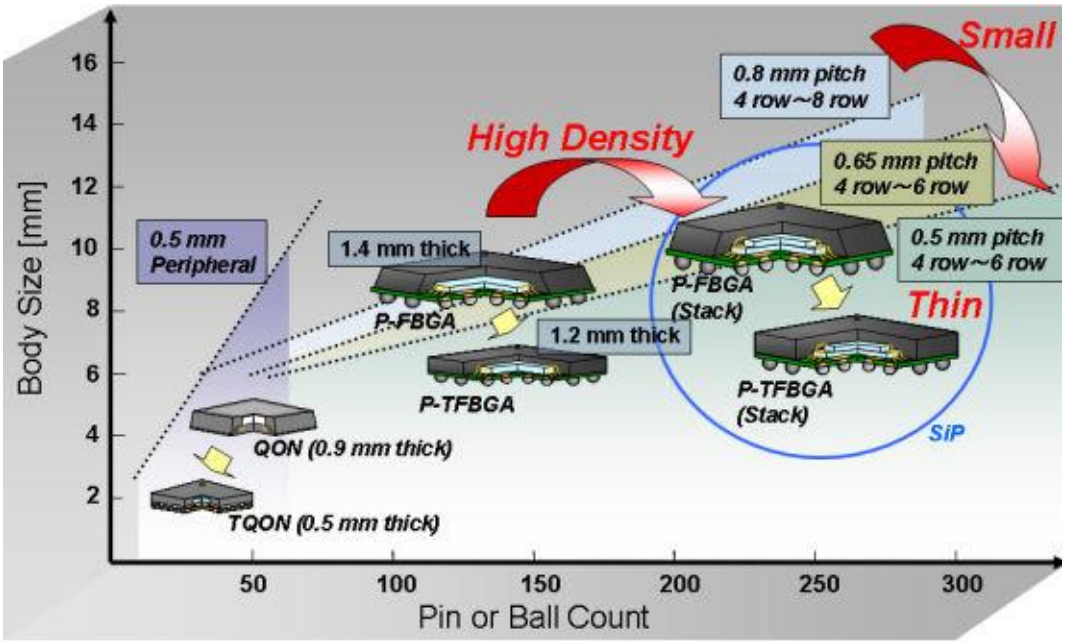


FIGURE 1.4 Package technology trends [13]. (SOURCE: Toshiba Electronics Europe)

Area array packages are devices with I/Os interconnection distributed across the bottom side of components in an area array pattern [14]. The interconnections often are composed of metal or polymer bumps, and the area array packages are mounted onto substrates through

soldering or adhesives. In SMT, area array package evolved further to the peripheral fine-pitch lead approach. This development ran into limitations quickly at approximately 0.3–0.4 mm pitch applications. To address this challenge the area array packaging technology emerged, offering almost a quantum leap over the peripheral packaging technology. From flip-chips (FC) and chip scale packages (CSP) to BGAs, area array packaging now provides great benefits at both the IC and component levels [14].

Extensive research and development continues to reduce the size of active packages. Passive components have also been reduced size to enable designers to use smaller printed circuit boards to perform a given task. The miniaturization of passive components can be exemplified by the size evolution of multilayer ceramic chip capacitors [15], as shown in Figure 1.5.

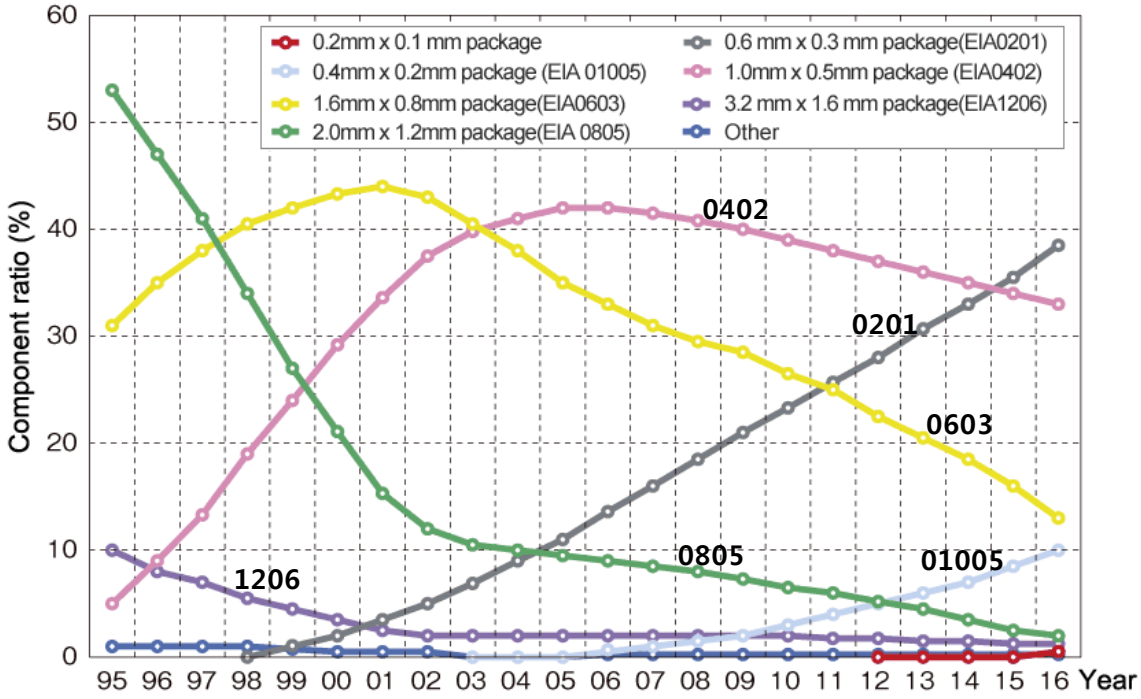


FIGURE 1.5 Trends in the shares of various component sizes. The 1.0 × 0.5 mm chip (0402) type has the highest component ratio as of 2009, but it has passed its shipment peak. The 0.6 × 0.3 mm chip (0201) type is rapidly increasing in place of the 1.0 × 0.5 mm chip (0402). In 2015, the ratio of the 0.6 × 0.3 mm chip (0201) type is expected to exceed that of the 0402 chip. The graph is based on Murata's projections [15].

The chip size of the most commonly used passive components gradually decreased from 0805 (2012 metric, 2.0 mm × 1.2 mm) chip in 1995, to 0603 (1608 metric, 1.6 mm × 0.8 mm) chip in 1998. With the increasing adoption of ultra-small capacitors for mobile phones, digital cameras and digital camcorders and other compact portable products, set makers have begun to adopt 0402 (1005 metric, 1.0 mm × 0.5 mm) chip, format products as general-purpose capacitors, so 0402 chip was projected to be the most popular size in 2003. 0201 (0603 metric, 0.6 mm × 0.3 mm) chip emerged in 1998 and is rapidly gaining market acceptance.

In 2004, Murata Manufacturing Co., Ltd. has developed the tiny 01005 (0402 metric, 0.4 mm × 0.2 mm) chip capacitor a first in the industry [15]. The volume of this new chip capacitor is approximately 44 percent of the 0201 chip, the predominant chip capacitor presently used in market leading Smartphone. Figure 1.6 shows 01005 chip components relative size different 0201 sized components. Difficulty in handling the small chips such as 01005 may result in a change in technology toward further miniaturization. A potential candidate technology may integrate passives [14].

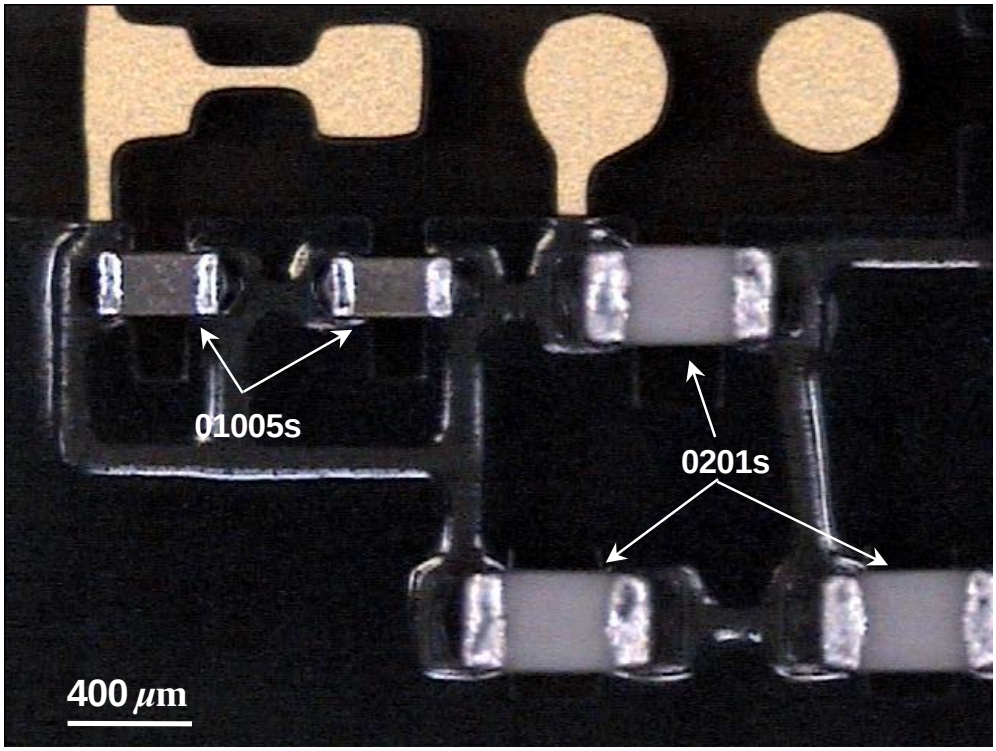


FIGURE 1.6 Size comparisons of tiny 01005 chip components with 0201 size chip components.

1.1.3 System-in-package technologies

System products continually move toward light, thin, short, small, and shrinking packages. The industry typically used two approaches to achieve this target: a SoC solution based on IC front-end process technology, or a SiP solution based on IC back-end packaging process technology.

SiP is a combination of multiple active electronic components of different functionality, assembled in a single unit that provides multiple functions associated with a system or sub-system. SiP may optionally contain passives, micro-electro-mechanical-systems (MEMS), optical components and other packages and devices [16].

In comparison to SoC technologies, SiP technology offers the following advantages [17,18]:

- High flexibility of package architectures allowing designers to combine active and passive components from a variety of semiconductor technologies without impacting the IC design and chip fabrication.
- High performance by providing high-level integration for digital, logic and RF functions and passive elements; short interconnection to minimize the parasitic effects both in the chip / substrate interconnection and the package / system board connection.
- Low system costs by eliminating multiple packages for individual chips while leveraging the existing packaging and SMT assembly manufacturing infrastructure.
- Small size factor by providing a platform for the integration of active devices integrated and embedded passives.
- Short time-to-market. The system design, tuning and debugging are done at the substrate level, minimizing IC mask set redesign and wafer fabrication cycle times. This reduces new product time to market.
- Suitable for a wide variety of devices and materials.

Today's wireless market is largely driven by the cell phone industry where cost, size, performance and time-to-market are the primary driving factors. Examples of current SiPs include RF modules, which enjoy wide use in cell phones, and direct current (DC) power

conditioning blocks. The 2009 ITRS has described the future SiP growth model under the title "more than Moore" [19]. In this vision, adding functionality with SiP technology leapfrogs traditional scaling approaches to accelerate time to market for tomorrow's products (Figure 1.7).

To address the need for greater functionality quickly, a number of companies have already shifted away from single-die SiP innovations typical of those illustrated in Figure 1.8. A market report prepared by Prismark identifies four categories of SiP [20,21]:

- **Modules:** including low temperature co-fired ceramic (LTCC) and PCB-based modules that combine one or more uncased die and integrated and /or discrete passive components in a BGA, land grid array (LGA), or castellated joint package. The majority of high volume module designs are for RF applications, such as mobile phone power amplifier (PA) modules and Bluetooth modules.

- **Multi-chip modules (MCM):** with multiple uncased die and optional passives in side-by-side and stacked die configurations with standard package outlines. Examples include graphics processor and memory MCMs as well as central process unit (CPU) and memory MCMs.

- **3D stacked-die packages:** including any standard package outline with two to five (or more) vertically stacked devices with a lead-frame, PCB, or flex circuit base. The primary application is memory for mobile phones.

- **3D stacked package-on-package (PoP) and stacked package-in-package (PiP):** PoP includes pre-packages devices that are stacked on top of each other using lead-frame, PCB, and flex-based solutions. PiP includes stacked package configurations where one of the die stacks includes an over-molded package.

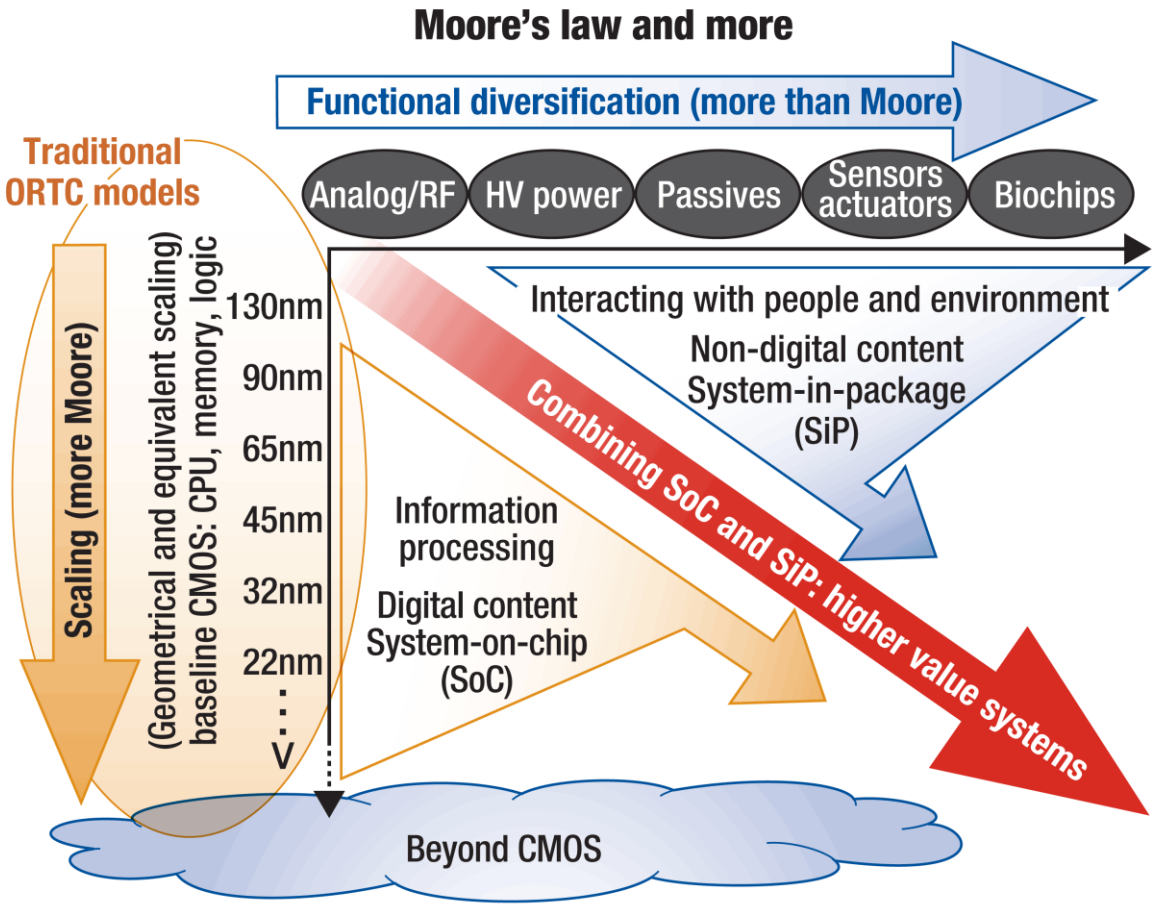


FIGURE 1.7 System-in-package integration leapfrogs traditional scaling approaches, providing "more than Moore" functionality [19]. (SOURCE: Semiconductor Industry Association. The International Technology Roadmap for Semiconductors, 2009 Edition, SEMATECH, Austin, TX, 2009)

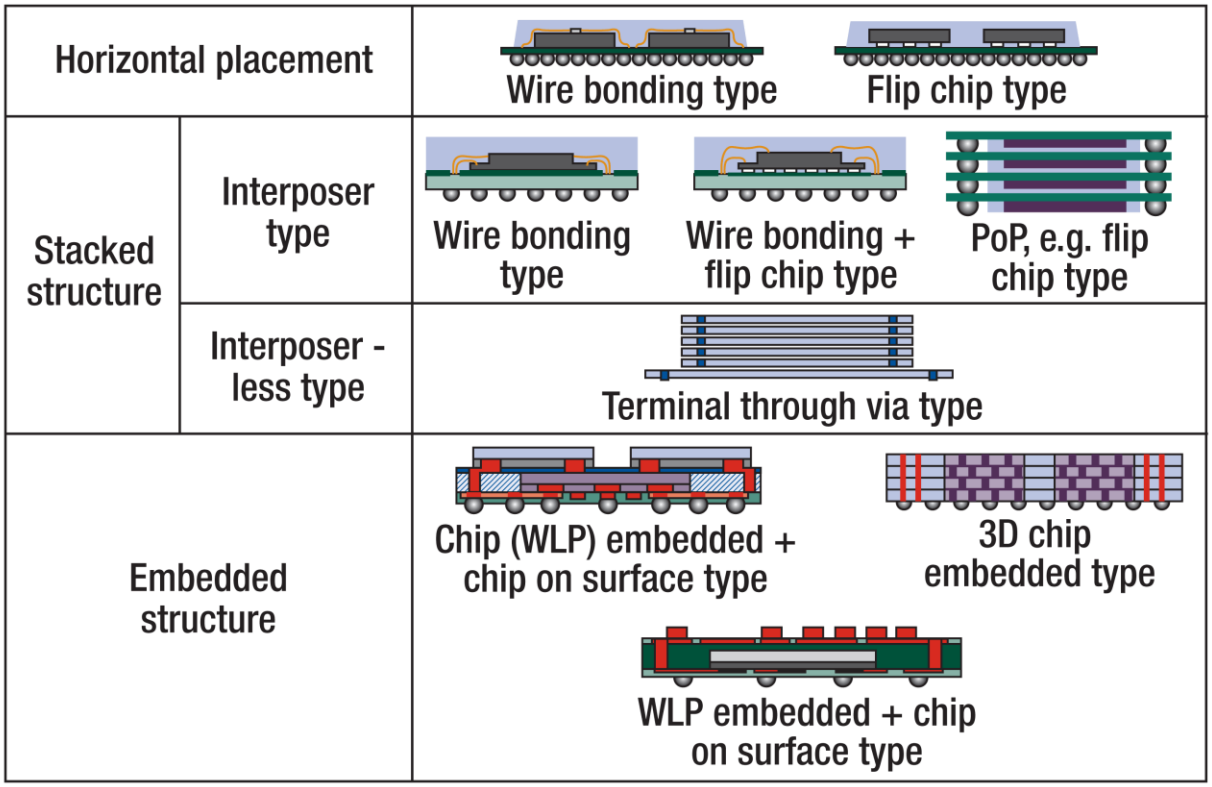


FIGURE 1.8 Variations of current system-in-package methodologies [20,21].
(SOURCE: iNEMI 2009 Industry Roadmap)

1.2 Historical background

1.2.1 Technological driving force

An emerging trend in electronic packaging technology is the "convergence system" or a system that is characterized by the integration of diverse product functions into one package or product [22].

In recent years, SiP technologies are more and more penetrating products of the mentioned market segments due to their benefits of a rapid time to market and lower overall costs. These technologies enable systems with high functional density by use of a wide range of chip technologies.

Starting with a side-by-side placement of devices, SiP is now going to use 3D-integration to shorter circuit-to-circuit interconnect lengths and to enlarge interconnect densities. In this way 3D-integration offers a higher bandwidth and lower power consumption of interconnects. 3D-integration can be realized by 3D-packaging like PoP or by die stacking with high efficiency by use of through-silicon-vias (TSV) [23].

SiP and especially 3D-integration technologies will be the basic technologies for realizing smaller portable and hand-held products, for faster networking and communications, for medical and bioengineering applications as well as for miniaturized sensors and actuators. These products will be achieved by so-called hetero system integration. They can be realized as autarkic systems with energy harvesting and wireless communications.

SiP can be made based on existing technologies (rigid and flexible interposer, lead-frames, PoP, and die stacking). Assembly technologies which are used cover through-hole assembly, surface mount assembly, direct chip attach and wafer level technologies. Interconnections between circuits and devices can be realized by well-known first-level interconnection technologies like wire bonding (Table 1.3) and flip-chip techniques by using solder bumps [25].

TABLE 1.3 Chip-to-package pitches [24]

Year of production	2010 (μm)	2013 (μm)	2015 (μm)
Wire bond single in line	35	30	25
Wire bond-wedge pitch	20	20	20
Flip-chip area array (organic and ceramic substrate)	130	110	100
Flip-chip on tape or film	10	10	10

1.2.2 Problem description

Because of the diversity of applications, device structure, and requirement for SiP modules, a variety of packaging and interconnect techniques have to be developed to meet the requirements of these applications. There are several key process challenges in assembly of SiP modules. The four major problems are described below.

(1) Miniature chip component assembly

Trend for miniaturization and higher functionality has fostered the introduction of many fine-pitch surface mount packages with lead pitches under 0.4 mm (15 mils) are classified as ultra-fine pitch (UFP) components [26]. Aside from the newer 01005 chip components that are starting to receive attention, the aforementioned components are widely used in Smartphone, where reliability is of main concern. Although 01005 chip components, enable the effective use of the limited real estate to form complex circuitry, their introduction has posed new challenges during the SMT assembly processes. The quality of solder joints affects the reliability of these packages, especially where they are subjected to very harsh conditions. These challenges must be solved in order for miniature-sized components to gain acceptance as an option for high-speed and high-yield assembly. Extensive research, particularly focusing on stencil design, PCB pad design, component placement clearance, and solder paste selection, has been carried out to develop assembly processes for 01005 chip components. However, current published results do not

provide sufficient guidelines for the assembly of 01005 chip components and also do not cover reliability data that can be applied for mass production of these devices.

(2) Fine-pitch devices and solder stencil printing process

The use of ultra-fine pitch packages makes the stencil printing process more critical to produce a reliable solder joint. For fine-pitch packages, solder paste volume and consistency are critical to solder joint reliability. The process becomes more challenging when the combination of paste rheology and stencil geometry causes inadequate or inconsistent solder paste transfer [27]. However, the solder paste stencil printing process is still not completely understood, as indicated by the fact that industry reports 60–70% of fine-pitch SMT defect are related to the solder paste stencil printing process [28–30]. In addition, the various stencil design elements that affect the solder paste release are the aperture size, aperture shape, aperture wall taper, and wall finish of the apertures. Stencil fabrication technology plays a major role in the amount of solder paste released from the apertures during stencil printing process [27]. However, little work has been reported on the effects on stencil fabrication process factors, particularly those of aperture quality and stencil printing performance.

(3) High-density substrate and assembly defects

For the substrate technique of SiP modules, they may contain wire-bonded and/or flip-chip interconnects, 3D stacked die, and use high-density interconnect (HDI)/micro via layers in addition to classical substrate layers. HDI is defined as circuit boards that have vias smaller than 150 μm in diameter, which qualifies them to be called micro vias, and copper trace features smaller than 100 μm in diameter [31]. Micro via-in-pad in SMT applications allows realization of low cost, high density, high speed, and miniaturization for electronic devices. However, along with all of the advantages described above is the observation of a high occurrence rate of voiding in the solder joints involving micro vias. The trouble is getting worse with the prevalence of BGAs and CSPs, particularly in the presence of micro vias. In general, the presence of voiding in solder joints will affect the mechanical properties of the joints and degrade the reliability [32,33].

The current literature offers a significant amount of information on evaluating the impact of micro vias on void formation. However, most of the earlier research findings were based on the assembly of BGA or CSP and do not provide sufficient guidelines for the assembly of tiny passive components such as 0201s and 01005s.

(4) Lead-free assembly and BGA rework

Rework is an important aspect of manufacturing that helps meet required yields to achieve economic viability – another aspect that is anticipated to be substantially affected by a change to lead-free technology [2]. Several studies focusing on rework practices for solders have been reported [34–36]. The rework of lead-free solder joints has been shown to be technically feasible. Concerns associated with locally heating printing circuit boards or attachments at high temperature are mostly associated with the need to reflow heavy and complex components such as BGAs that require a high level of heat to effectively achieve removal and reflow. The effects of higher process temperatures on various microelectronics board assemblies when utilizing most lead-free solders are listed in Table 1.4 [2], and other issues related to higher process temperature will be discussed in this dissertation. Higher reflow temperatures increase dissolution rates, which may result in an increase concentration of termination pads and surface finish elements in solder joints. This high temperature may also influence the components that are adjacent to the reworked area [37]. Several rework studies were reported to help develop the capability to manufacture lead-free printed circuit board assemblies (PBAs). However, the rework processes still represented a major technical challenge in industry due to the narrow process window.

All of these challenges must be solved in order for SiP module packaging to gain acceptance as an option for high-speed and high-yield assembly. Many techniques and approaches are being pursued by the research community, and many more will surely be tried in the future. It is not practical to review all of these approaches here, but some of the most relevant and practical approaches will be discussed in this dissertation.

TABLE 1.4 Effect of higher process temperatures on various microelectronic board assemblies [2]

Board assembly items	Effects
Components	
Ceramic chip carriers	Little to none
Organic chip carriers	Degradation can be substantial, depends on T_g of material
Specials: electrolytic capacitors,	Increased moisture sensitivity level
wound components, etc.	Susceptible to damage, typically designed for 230°
	Maximum temperature, some up to 260°C
Printed circuit board material	Standard FR-4, T_g ~140°C
	Subject to degradation
	Higher T_g materials
	Will service proposed ~240°C
	Typically will not survive ≥260°C
Plastic over-mold material	Thermal plastics may undergo shrinking or warping or cause critical features to move (creep)
	Thermal setting compounds, typically not affected by MSL-related effects
Fluxes	Must be formulated to be active near and at the alloy melt point temperature
	Must not create charred masses that hinder soldering, or allow surface reoxidation

1.3 The goal and outline of this dissertation

The goal of this research is twofold: to develop a robust assembly process for SiP devices with 01005 chip components and to propose a procedure to minimize or eliminate lead-free soldering defects in the assembly of high-density SiP devices. The dissertation consists of ten chapters, which are grouped into six parts for convenience, as shown in Figure 1.9.

The first part of this dissertation (Chapters 1 and 2) is the introduction, which presents the motivation, historical background and recent progresses for this research.

Chapter 1 introduces the dissertation by presenting the motivation for this research and the research objectives. Chapter 2 provides a review of the literature relevant to the research objectives. In addition, this chapter briefly reviews the status of research on the high-density solder interconnection and assembly of miniature chip components such as 01005s. Chapters 3 through 9 are the core parts of this study. They cover the experimental procedures, results, and discussion and the process guidelines for the assembly of a high density SiP module with lead-free solder alloys. These chapters were written for publication as research articles on the above topics.

In Part II (Chapter 3), the assembly of miniature chip components is investigated.

Chapter 3, entitled "The Effect of Selected Process Parameters on Defects in the Assembly of 01005 Chips", deals with the investigation of assembly processes for the components of 01005 chips. Data on assembly yield, defects, quality, reliability assessments of component shear strength, and temperature cycling are included in this chapter. The subject of this chapter is the basis of a journal paper entitled "Process Characterization and Reliability for the Assembly of 01005 Chip Components", which has been published in *Soldering & Surface Mount Technology* (2012) (Highly Commended Paper Award).

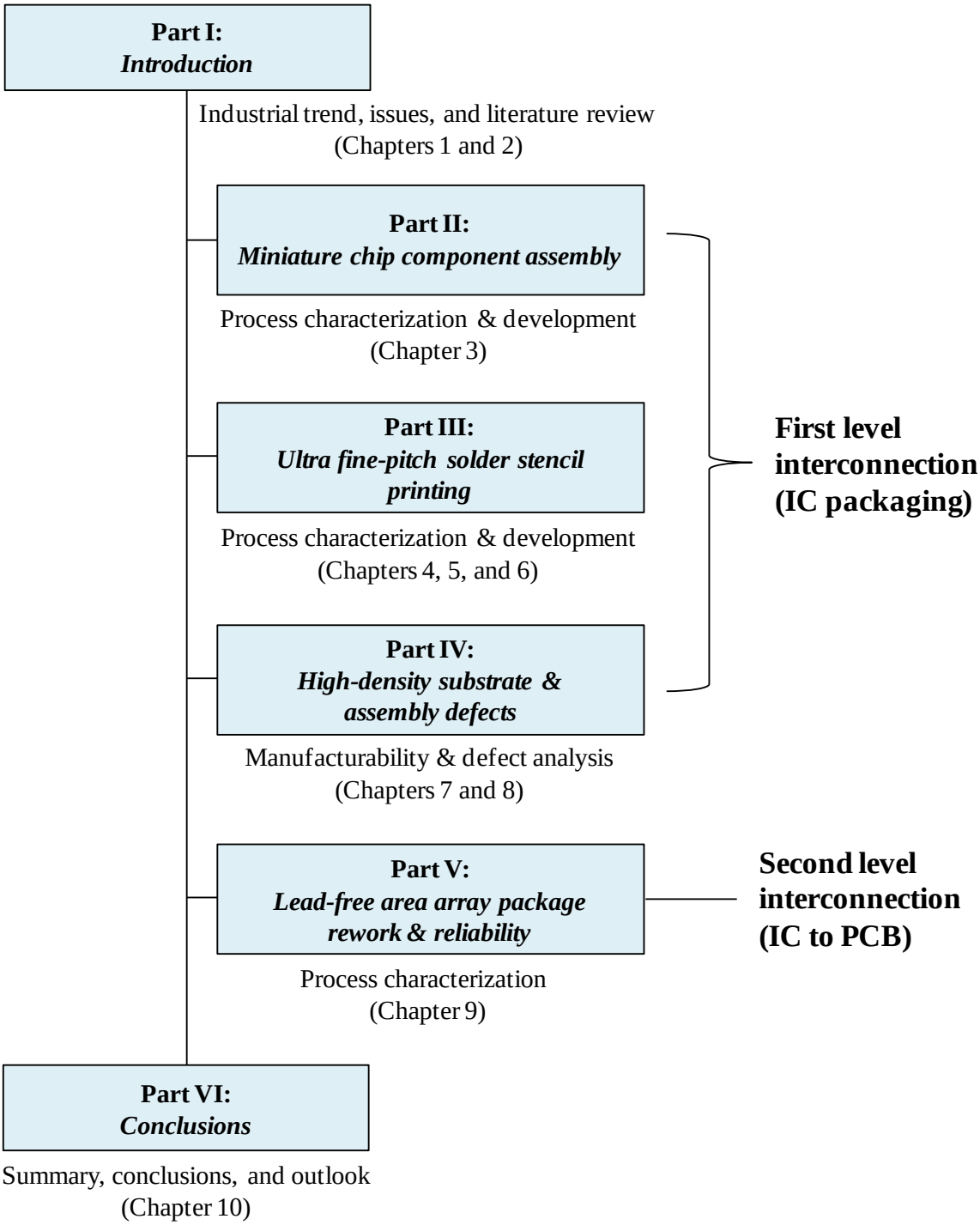


FIGURE 1.9 Organization of the present dissertation.

In Part III (Chapters 4, 5, and 6), the ultra-fine pitch solder stencil printing process are investigated.

Chapter 4 is entitled "The Effects of Acid Electrolyte and Electro-polishing Conditions on the Printing Performance of Small Apertures." This chapter discusses the effect of potential factors, such as electrolyte compositions and electro-polishing time, which may affect the performance of laser-cut stencil printing in the finishing of the stencil apertures. The results of the work reported in this chapter are the basis for a paper entitled "Effects of Acid Electrolyte and Electro-polishing Conditions on Laser-Stencil Printing Performance", which has been published in *IEEE Transactions on Components, Packaging and Manufacturing Technologies* (2011).

Chapter 5 is entitled "The Effect of Electro-polishing on the Printing Performance of Small Apertures." This chapter discusses the effect of selected electro-polishing process parameters on the performance of laser-cut stencil printing. The results of the work reported in this chapter are the basis for two papers. One is entitled "The Behavior of Solder Pastes in Stencil Printing with the Electro-polishing Process", which has been published in *Soldering & Surface Mount Technology* (2013). The second paper is entitled "Developing the Stencil Printing Process for 01005 Lead-Free Assemblies", which was presented and published in the proceedings of the IEEE International Conference on Electronic Packaging Technology & High Density Packaging – ICEPT & HDP (2008) (NXP Semiconductor Best Paper Award).

Chapter 6 is entitled "The Effect of Fine-Grained Structure on Stencil Printing Performance." This chapter discusses the effect of grain size and stencil manufacturing parameters on the performance of laser-cut stencil printing on a 150 μm pitch flip-chip-on-board (FCOB) assembly. A stencil with a fine-grained microstructure is tested for ultra-fine pitch printing performance with very fine solder pastes, which contributes to defining the narrow process windows of type 6 and type 7 pastes for ultra-fine pitch, flip-chip applications. The results of the work reported in this chapter are the basis for a paper entitled "A Novel Process Results in Ultra-Fine Pitch Stencil Printing and Improved Properties", which has been submitted for publication in *Soldering & Surface Mount Technology*.

In Part IV (Chapters 7 and 8), the high-density substrate and assembly defects are investigated.

Chapter 7 is entitled "The Effect of Micro Via-in-Pad Designs on Tombstoning." This chapter discusses the effect of potential factors, such as micro via-in-pad design, stencil opening ratio, and reflow profile, which may affect soldering defects in the assembly of 0201 small chip components. The results of the tombstoning mechanism are discussed, and optimized conditions are recommended. The results of the work reported in this chapter are the basis for two papers. One is entitled "The Effect of Micro Via-in-Pad Designs on Surface Mount Assembly Defects: Part I – Tombstoning", which has been published in *Soldering & Surface Mount Technology* (2012). The second paper is entitled "The Effect of Micro Via-in-Pad Designs on SMT Defects in Ultra-Small Component Assembly", which was presented and published in the proceedings of the IEEE International Conference on Electronic Packaging Technology & High Density Packaging – ICEPT & HDP (2010).

Chapter 8 is entitled "The Effect of Micro Via-in-Pad Designs on Voiding and Spattering." A micro via-in-pad design is proposed in this chapter. The issue of via-hole design and the soldering process of the 0201 chip components on the SiP module are discussed. This chapter also determines defect mechanisms. The results of the work reported in this chapter are the basis of a paper entitled "The Effect of Micro Via-in-Pad Designs on Surface Mount Assembly Defects: Part II – Voiding and Spattering", which has been published in *Soldering & Surface Mount Technology* (2013).

In Part V (Chapter 9), lead-free reworking and reliability are investigated.

Chapter 9 is entitled "The Effects of Reworked Board Assemblies with Lead-Free BGA Packages." This chapter characterizes the reworking process with BGA packages and discusses the effects of the reworking process on the reliability of printed circuit board assembly, particularly the reliability of drop shock. The results of the work reported in this chapter are the basis for a paper entitled "Process Characterization and Reliability for the Rework Assemblies with Lead-Free BGA Packages", which has been submitted for publication in *Soldering & Surface Mount Technology* (in press).

Part VI (Chapter 10) provides conclusion remarks and recommendations for future research.

Chapter 10, "Conclusions and Outlook", summarizes the key achievements and findings of Chapters 3 through 9, and recommends directions for future work in this area.

Chapter 2

Recent progresses

Many of today's consumer electronic products require miniaturization of components and high-density solder interconnections on printed circuit boards. With these demands, advanced packages, such as flip-chips, CSPs, BGAs, and 01005 passive chip components, have become an interesting topic to study in electronics manufacturing. Surface mount assembly is primarily a process of reflow soldering, as shown in Chapter 1. It involves deposition of solder paste, component pick-and-place, and reflow soldering. Therefore, to achieve a high quality and high yield soldering process, it is essential to understand the fundamentals of surface mount assembly. The following sections review the diverse processing techniques related to this study.

2.1 Passive chips in modern system-in-packages

System-in-package (SiP) modules are becoming increasingly popular due to their ability to integrate functionality in a very small amount of space and in a very cost-competitive manner. SiP modules take active and discrete passive components and integrate them within the same package. Discrete passive components, in the form of surface-mountable-devices (SMD), can be mounted into packages using solder attachment assembly processes [38]. A common SiP module example, shown in Figure 2.1.

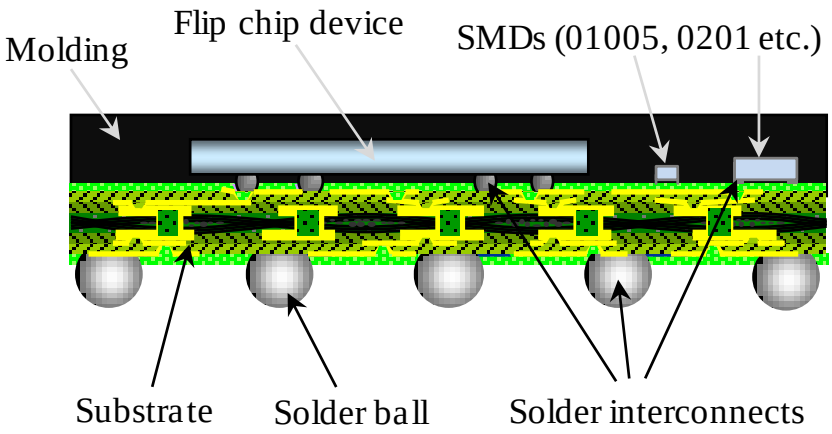


FIGURE 2.1 Typical RF SiP platform.

Reducing both the size of the passive components and the spacing between them increases the package density and this is an efficient way to miniaturize many electronic products. The industry has witnessed the introduction of a variety of chip sizes, including 0402 (1005 metric, 1.0 mm × 0.5 mm), 0201 (0603 metric, 0.6 mm × 0.3 mm), and 01005 (0402 metric, 0.4 mm × 0.2 mm) [39].

The 01005 size is the smallest discrete passives available today. Passives tend to move down a case size every 4 years while, following Moore's law; ICs double their transistors/cm^2 about every 1.5 years. Figure 2.2 shows the dimensions of dominant passive components [40]. Figure 2.3 shows a cell phone RF section that utilizes 01005 and 0201 resistors and capacitors surrounding a 10 × 10 mm packaged integrated circuit.

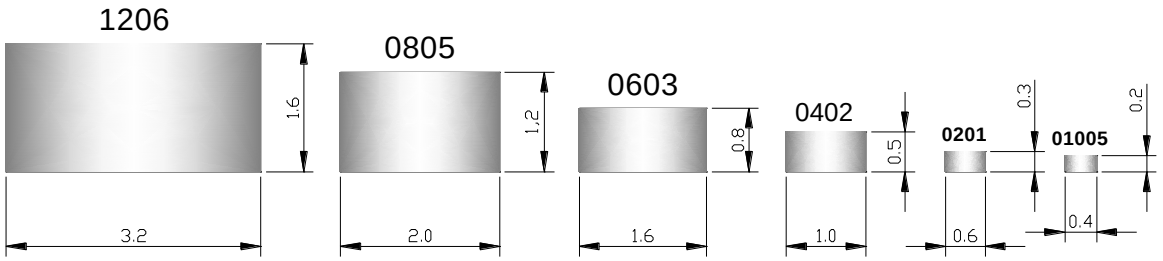
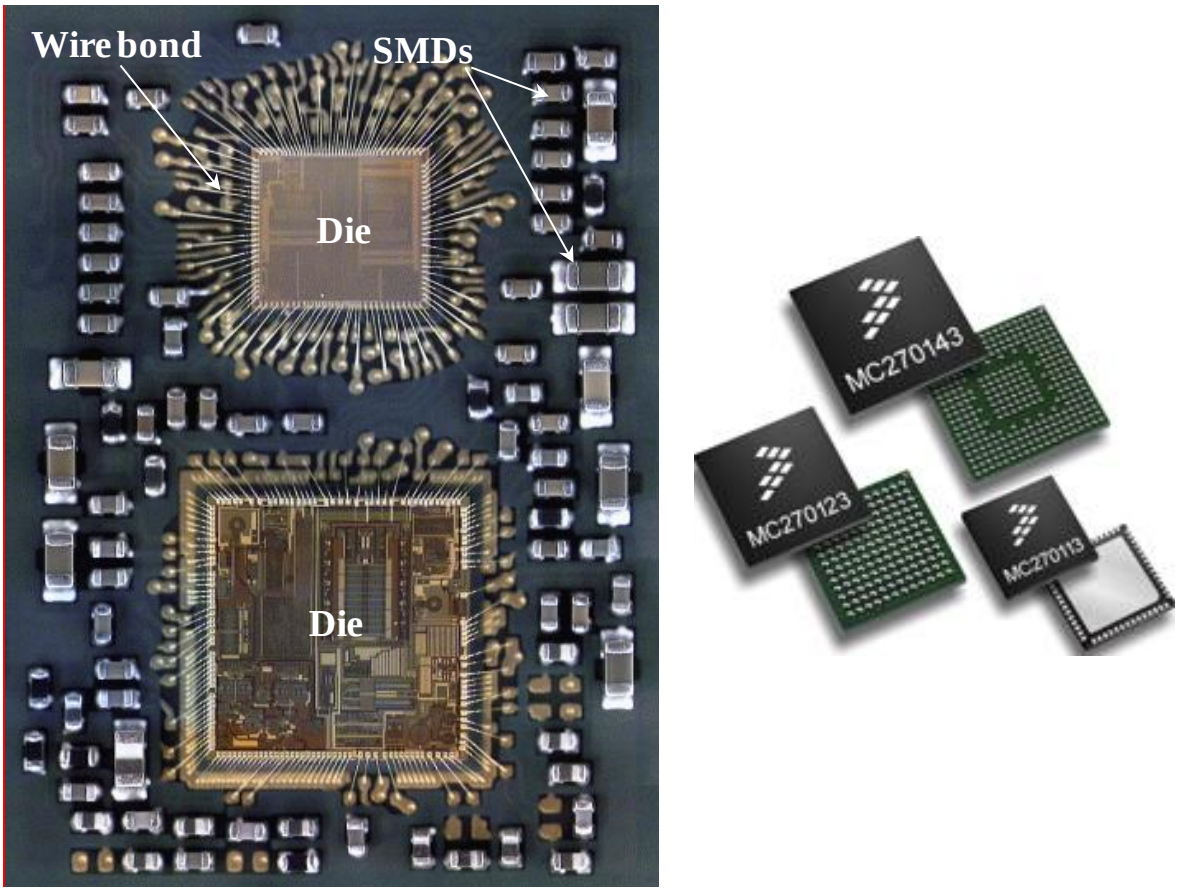


FIGURE 2.2 Dominant passive component dimensions (mm) [40].



(a) (b)

FIGURE 2.3 Cell phone RF section utilizing surface-mount passives by (a) assembled RF module; (b) over-molded RF module package. (SOURCE: Freescale Semiconductor, Inc.)

2.1.1 Impact of 01005 chips in electronics manufacturing

Being in the initial stages of deployment, 01005s are not as popular as its precursor, the 0201. There are many reasons for this. First and foremost, there is the assembly issues associated with 01005s. Secondly, there is the cost of these components; 01005 chip components are currently very expensive and cost between 20–60 cents U.S. each in medium to low volume range [41].

Manufacturing process changes include changes in printing parameters, stencils equipment changes like nozzles, feeders, and changes in the reflow profile. These changes are mainly due to the size of the component which reduces the pad size and ultimately requires smaller solder paste deposits. Good solder paste deposits for these components can be achieved by using thinner stencils. However, this will led to insufficient solder paste for large components. Incorporating 01005 chip components with larger components is hence challenging [42]. Some prefer to use a step stencil to alleviate this problem. However, in some cases, the location and distribution of these passive components across the board and its proximity to larger components may not permit the use of a step stencil. For example, the PCBs used for memory modules and handheld devices are densely populated. The spacing between the active and the passive components does not permit the use of a step stencil [43].

2.1.2 Assembly processes for 01005 chip components

Recently, 01005 chip components have been implemented in very high density applications, such as mobile phones, Bluetooth modules, and wireless LANs after extensive process optimization [44–47]. Resistors and capacitors are now being produced in the extremely miniaturized 01005 chip size. However, the use of such tiny components poses great challenges for SMT assembly. The main factors affecting the 01005 assembly process can be divided into the following categories: PCB design [48], stencil design [49], solder paste [50], pick-and-place [39], reflow, and inspection [43]. A number of investigators have conducted various experiments to optimize SMT process parameters, particularly focusing on stencil design, PCB pad design, component placement clearance, and solder paste selection, in order to develop assembly processes for 01005 chip components [48,49,51,52]. It has been demonstrated that thinner stencils (0.08 – 0.10 mm thicknesses) combined with finer solder paste types (types 4 or 5) are necessary in order to

guarantee sufficient and consistent paste deposition. Their findings are very useful in enabling an understanding of the various process issues involved and the factors impacting assembly yield.

2.1.3 Assembly critical parameters for high process yield

As noted chapter 1, the continuing demand for smaller, lighter, high-density products has resulted in the increased use of miniature components. Emerging package types include fine-pitch ICs (0.3 mm pitch), *µ*BGAs, CSPs and flip-chips. The impact of these new package types on equipment requirements and printed circuit board assembly technology is significant. For printed circuit boards, the trend is towards smaller line widths and spacing and more accurate solder-resist positioning. This trend is not only limited to integrated chips and printed circuit boards but also towards passive components like resistors and capacitors. Recently, one of the miniature components that are being used for resistors and capacitors is the 01005 chip components.

Typically, current surface mount devices and area array package assembly processes rely on solder paste deposition through stencil printing, component pick-and-place, and mass reflow soldering as shown in Figure 2.4. In order to ensure high process yields during assembly the process parameters of the various assembly operations must be evaluated. Factors that affect the assembly process yield can be divided into four categories; human factors, environment, materials, and process methods. Figure 2.5 is a so-called fish bone diagram that illustrates the interrelationship among the various factors and their influence on assembly yields [2]. The factors considered were chosen based on the literature review and the problems faced during the study.

Surface mount quality can be influenced by a range of SMT process parameters. For small components, the requirements for these process parameters become much more critical. First of all, a sufficient volume of solder paste must be deposited onto the printed circuit board pads and the distribution should be as uniform as possible. To achieve this goal, a variable screen printing process is necessary. There are many variables that influence the quality of the stencil printing process, which is measured by the amount and position of solder paste deposited. Figure 2.6 gives a list of important process variables. Pan [53] reviewed the work on investigating

the effects of the process variables. Since there are more than 45 variables, to identify the critical variables is necessary.

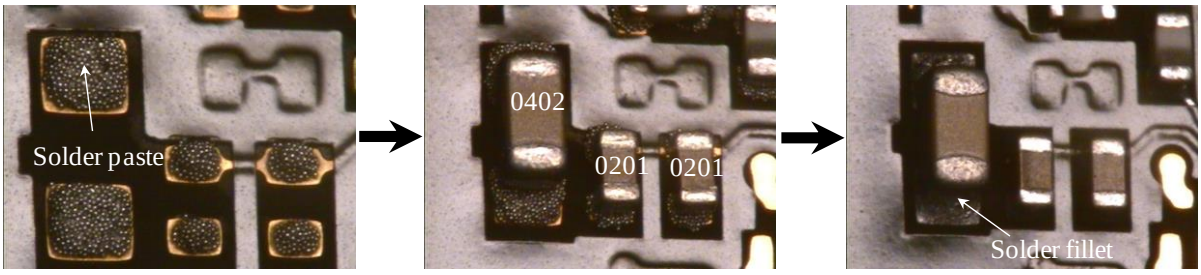


FIGURE 2.4 Process mapping for SMT line.

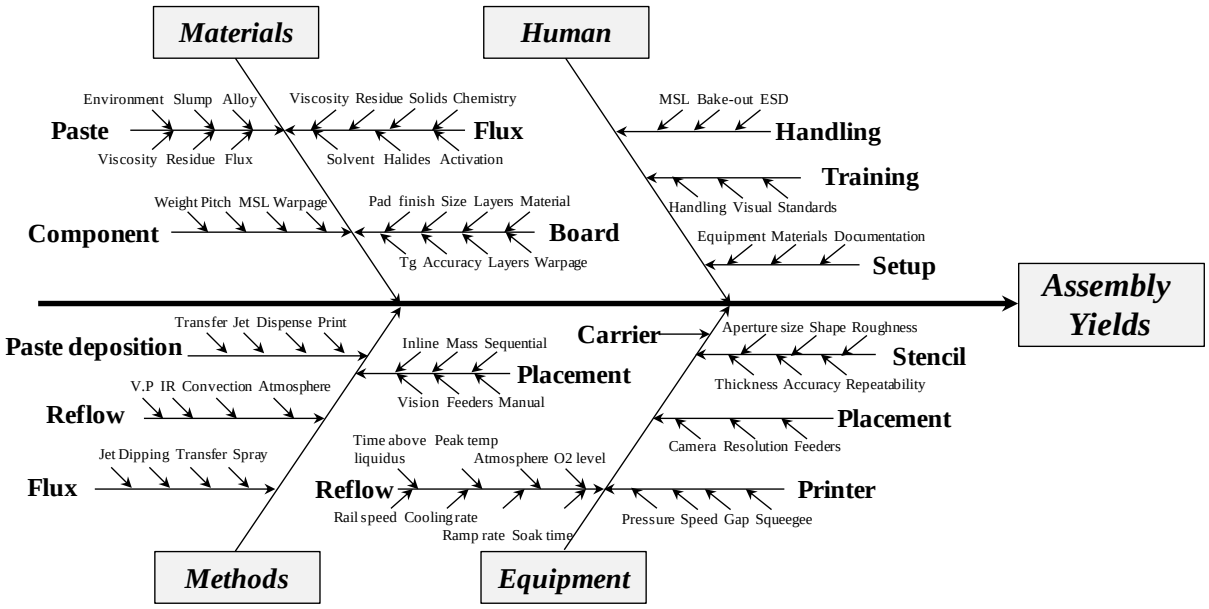


FIGURE 2.5 Cause and effect diagram of factors that influence lead-free assembly [2].

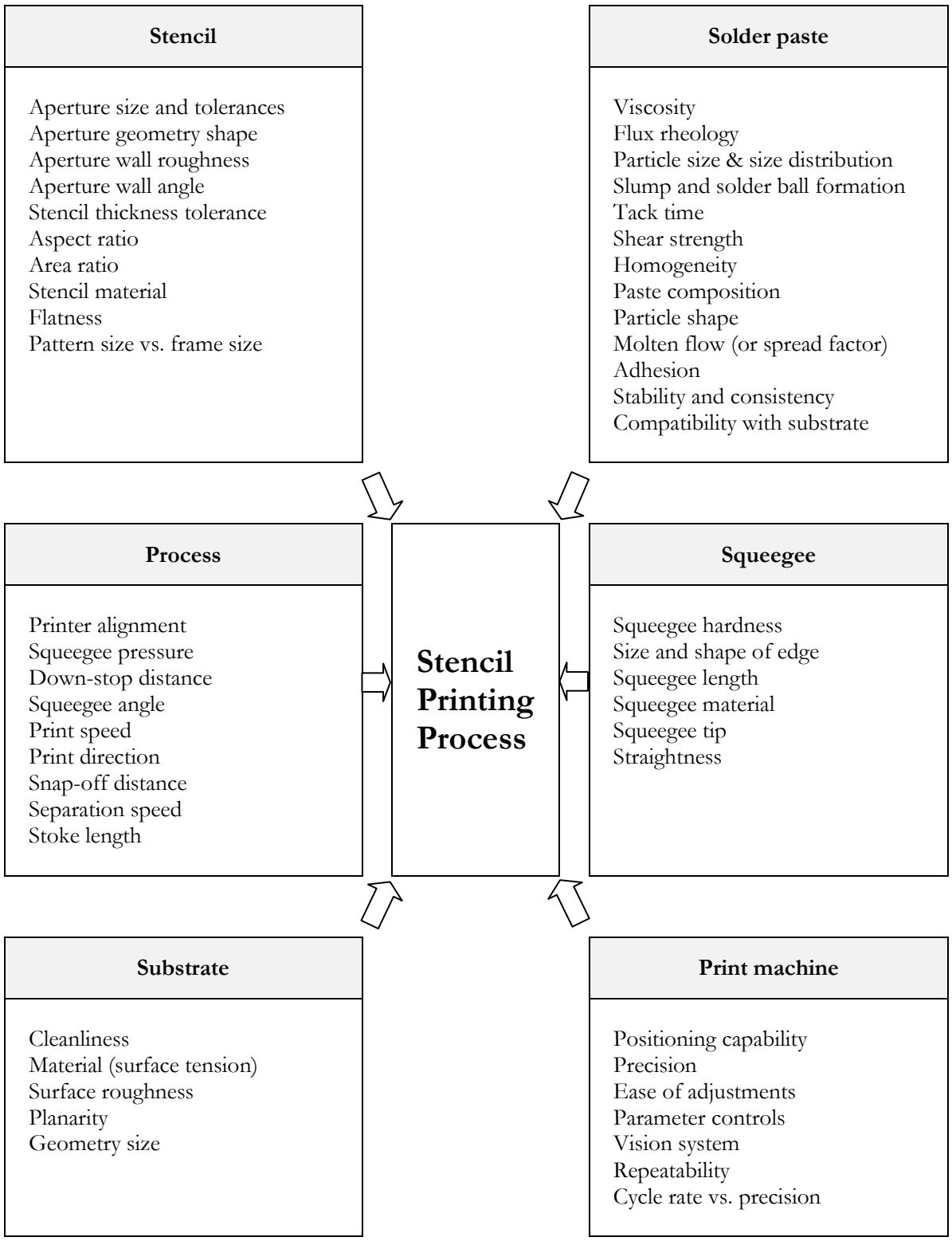


FIGURE 2.6 Factors that influence the stencil printing process [54].

2.2 Printing fine-pitch solder paste

The trend for miniaturization and higher functionality has fostered the introduction of many fine-pitch surface mount packages with lead pitches under 0.4 mm (15 mils) are classified as ultra-fine pitch components [26]. The assembly processes most dramatically affected by the fine-pitch packages are solder paste printing and component placement. The most commonly used solder paste printing process is stencil printing, although other technologies are also used, including dispensing, pin-transferring, and roller coating [14].

2.2.1 Process characterization of the stencil printing

Stencil printing is one of the most important processes in the SMT assembly process. It has been pointed out that 60–70% of the defects encountered in SMT assembly are related in some way to the printing process [28–30]. Stencil printing is a dynamic and multifactor process. The function of a stencil is to deliver a controlled, known volume of solder paste to pads on the PCB substrate. The printing process involves two steps (Figure 2.7) [55]:

(1) the aperture fill process, in which solder paste fills the stencil aperture; and,
(2) the paste release process, in which solder paste is released from the stencil aperture to the pads on the PCB substrate.

The fill process depends largely on the solder paste, squeegee blade, solder paste roll, print speed, and aperture orientation with respect to the print direction [56].

Riemer [57] and Hanrahan *et al.* [58] have developed a hydrodynamic model to predict the effect of squeegee angle and squeegee speed on rolling of the paste and filling of the apertures. Riemer developed a hydrodynamic model for screen printing (that utilizes the same principle of stencil printing) based on Taylor solutions by solving the Navier-Stroke differential equation. Taylor's solution generated a stream function ψ, which describes the ink movement in front of the squeegee. Riemer analytically proved that a squeegee angle of 45° helps in better rolling of the ink and filling of the apertures. Riemer also modeled the effect of the squeegee speed and squeegee pressure on ink rolling over the mesh. Hanrahan *et al.* developed the free surface modeling of the roll of the solder paste in the stencil printing process and compared the

model results with the infinite model. They are able to identify that the rolling of the paste takes place approximately 0.7 mm after the stencil-squeegee contact point. These models illustrate the complex flow characteristics of the paste during rolling and illustrate the rolling of apertures filling.

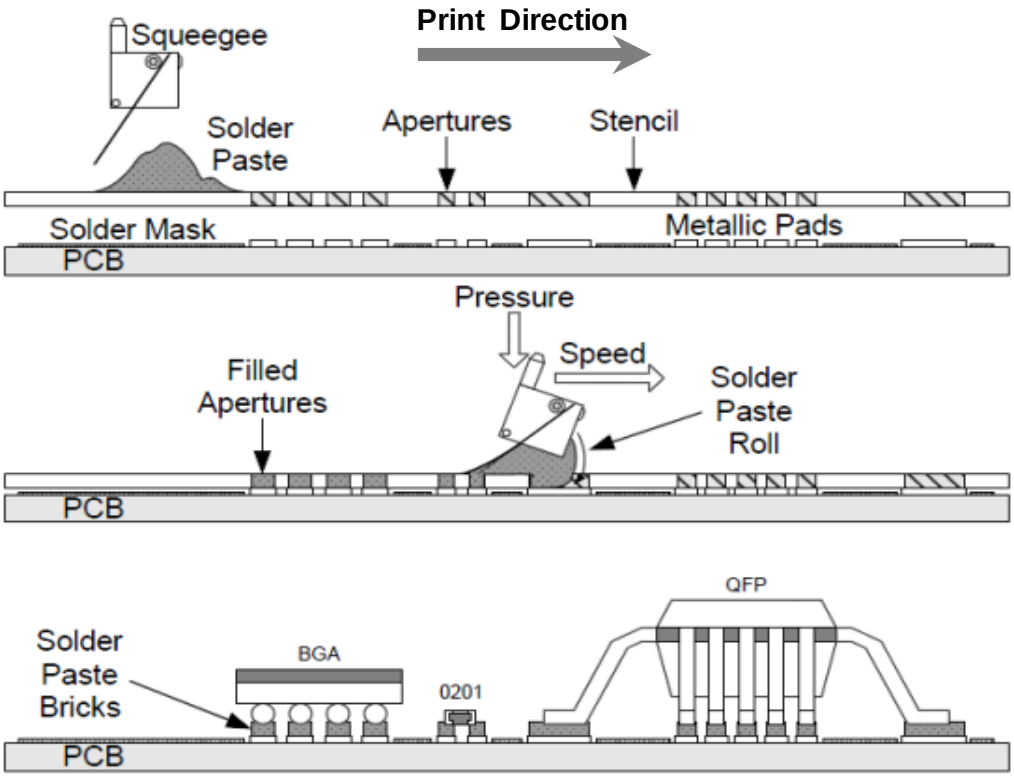


FIGURE 2.7 Stencil printing operation illustrations [55].

The filling of the aperture is one of the critical processes of the stencil printing process. If the apertures are not filled properly, then proper amount of paste will not be transfer from the apertures. Ekere *et al.* [59] used interrupted printing and observation to study the aperture filling process and identify the moment when the paste begins to flow into the apertures. It is seen that flow into the apertures occurs about 1 cm in from of the squeegee tip. Pham-Van-Diep *et al.* [60] developed a visualization technique to understand the filling of the apertures during printing. During the experimentation, they observed that flow of paste into the apertures starts about 1.143 cm (0.45 inch) upstream of the point where the squeegee contacts the stencil. The result of the filling process is validated with the computational fluid dynamic simulation.

The paste release process during a stencil printing operation also forms a critical part in determining the amount of paste transferred onto the pads. Riemer [57] first analyzed the stencil release or aperture emptying process for the screen printing process. For the ink screening case, Riemer estimated the stress at the substrate separation point, which is assumed to be the point of maximum stress. Then, using the stress at the separation point, he estimated the amount of ink that is released onto the fabric. Sahay *et al.* [61] proposed a model for the release process treating the solder paste as a single phase Newtonian fluid entering a circular duct. They reported good agreement between the model prediction and experimental results for coarse pitch apertures. Rodriguez *et al.* [62] developed a model for the release process based on shear release of the paste from the small stencil apertures. The shear release model assumes the existence of a yield point in the solder paste and models the solid-like and viscoelastic behavior of the paste based on the observations from his work.

Meanwhile, the various stencil design elements that affect the solder paste release are the aperture size, aperture shape, aperture wall taper, and wall finish of the apertures [63]. From these, it can be taken that the aperture size and shape are related to the stencil design, while the aperture wall taper and aperture wall finish are related to the stencil fabrication technology. Stencil fabrication technology plays a major role in the amount of solder paste released from the apertures during stencil printing [27]. They will be briefly discussed in the following text.

2.2.2 Stencil fabrication technology

Depending on cost considerations and the stencil forming technology chosen, the metallic materials used for stencil include brass, stainless steel, molybdenum, nickel, and Alloy 42 as shown in Table 2.1 [64]. Stainless steel and brass are the most commonly used materials for the chemical etching process. Molybdenum stencil is produced by similar processes to chemically etched brass and stainless steel with a different and more hazardous etchant solution. Molybdenum has been promoted as an alternative metal to stainless steel or brass due to its denser grain structure which reportedly will improve solder paste release from the stencil [65-66].

Nickel is the material of choice for electroforming technology, due to chemistry requirements. For laser-cut technology, stainless steel is the primary choice. Recently a plastics

material, KEPOCH, has been introduced for the laser-cut process [67]. The primary advantages claimed for the KEPOCH stencil system are low cost, 6 hours' turnaround time, easy stencil cleanability, better stencil release, and better resistance against stencil deformation or denting [14].

TABLE 2.1 Comparison of stencil materials in key performance areas [64]

Performance	Brass	Stainless Steel	Molybdenum	Alloy 42	Nickel (Electroform)
Mechanical strength	Unfavorable	Favorable	Favorable	Favorable	Favorable
Chemical resistance	Unfavorable	Favorable	Unfavorable	Favorable	Favorable
Etchability	Favorable	Less favorable	Favorable	Favorable	N/A
Sheet stock availability	Favorable	Favorable	Unfavorable	Favorable	N/A
Cost	Favorable	Less favorable	Unfavorable	Less favorable	N/A
Fine-pitch (opening)	Favorable	May need electropolishing	Favorable	May need electropolishing	Most favorable
Unique feature	Lowest cost	Durable	Self-lubricating; smooth wall	—	Finest opening

Note: N/A = not applicable.

Currently, three conventional stencil fabrication methods are used for solder paste printing in SMT processes: electroforming, chemical etching, and laser-cutting. Each type of fabrication method possesses inherent merits and limitations. The key performance of a stencil is assessed by the straight vertical wall, wall smoothness, and dimensional precision. In addition, durability, chemical resistance, fine opening capability, and cost are also important factors [64].

For many years, electroformed stencils have been the premier solution for fine-pitch, challenging assemblies. Electroforming is an additive process [14]. A mandrel is used as a base for the photo-resist application and for resolution of the image. The mandrel is then placed in a bath where Ni is plated. The opening will be formed around the photo-resist until the desired thickness of the stencil has been achieved. Figure 2.8 illustrates the stencil apertures made by electroforming and laser-cut [68]. The definition and tolerance of electroforming are better than the other techniques, such as chemical etching and laser-cutting process. However, it should be noted that nickel is soft and more prone to damage. A smooth wall, presumably plus low surface tension of Ni may favor paste release from the aperture. The surface tension effect may be questionable in the paste release process. The surface may also be too smooth to allow for a proper paste rolling action. The permanent gasket formed is expected to reduce paste bleed-out. The stencil thickness ranges from 25 to 300 μm, with minimum aperture width being 1.1 × thicknesses. Tapered side walls are also possible.

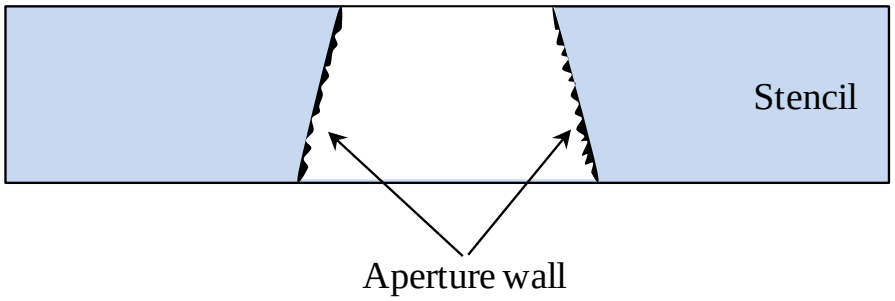
Electroformed stencils provide a much smoother wall than chemical etch and laser-cut stencils. However, nickel stencils, whether or not they are fully electroformed, are more expansive than typical laser-cut stencils. In most cases, the turnaround time is three-to-five days, but this technology is limited to only a few stencil manufactures that have knowledge about and expertise in, plating very thin nickel foils. Reduction of the manufacturing cost is necessary in order to apply this method to the stencil printing process to achieve an inexpensive assembly process.

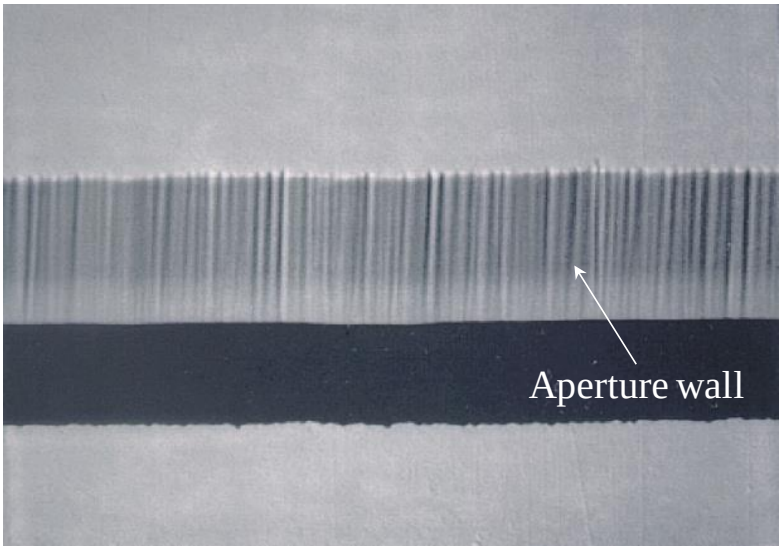
Chemical etching has been successful for making stencil apertures for many years. Chemically etching involves the photolithographic patterning of a metal foil and then the placement of the patterned mandrel into an etching solution. The unmasked regions are etched away, thereby creating the apertures. The problem with chemical etching is that the foil material is polycrystalline and hence etches isotropically. This artifact causes undercutting below the resist

mask, which is difficult to control. This taper limits the spacing between apertures, called the web, which must have a sufficient degree of metal to hold the stencil together while being subjected to tensile forces occurring during the framing and printing processes. In addition, the etching solution etches faster along specific crystal grains, hence creating a rough, porous inner sidewall that is conductive to clogging of the apertures by the paste material. Double sided etching minimizes the amount that the etching solution can eat into the stencil; however this process involves more complicated processes which involve double sided photolithography. In practice, the minimum pitch achievable through chemical etching is around 250 μm, however in most applications other types of stencils are used for pitch below 500 μm [69].

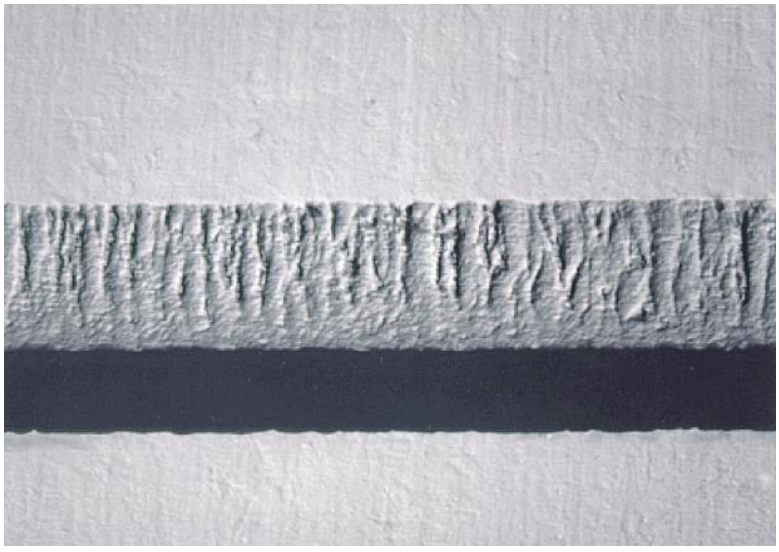
Laser-cut stencils are one-to-eight times less expensive than electroformed stencils. This cost advantage, coupled with the ability to deposit solder paste, makes it the most attractive option for high volume, low cost SiP module assembly. However, laser-cut stencil fabrication techniques do not allow for generation of stencil stencils capable of printing reliable deposits below 0201 chip size, because the quality of each aperture surface varies too significantly to produce a similar volume of print deposits.

Laser-cut stencil process involves (1) processing Gerber data, and (2) cutting image [14]. Typically stainless steel or other low zinc content materials are used. Common problems exhibited are a saw-toothed edge or dross buildup on the stencil surface. Post-cutting processing such as electropolishing (EP) is able to remove the dross buildup. The minimum feature size and tolerances for laser are a function of the beam configuration and machine parameters. Typical minimum feature size is 50 to 100 μm, with a tolerance of $\pm$ 6 to 8 μm. Both straight and tapered (25 μm) apertures are easily achievable. This incompatibility seriously limits the available materials that can be printed. In practice, the minimum pitch achievable for reliable and reproducible stencil printing is currently limited to around 150 μm pitch [69].





(a)



(b)

FIGURE 2.8 Stencil apertures made by (a) electroforming; (b) laser-cut [68]. (SOURCE: Photo Stencil, Inc.)

2.2.3 Post surface finish of stencil aperture walls

The surface finish of the aperture walls of a stencil has a significant impact on the paste release phenomenon [27]. In laser-cut stencil fabrication processes, EP is a secondary micro-etching procedure applied to the stainless steel after the primary aperture forming process has been completed [65]. EP will remove the high points and rough points from the stencil surface, thereby creating a shiny surface. The process has been promoted as being able to improve the solder paste release from the fine-pitch stencil openings.

The current literature offers a significant amount of information on evaluating the primary stencil technologies, including the effect of post-surfacing finish on small apertures produced by laser-cut stencils, which is done to improve the solder paste printing performance. Clouthier [70] carried out a detailed study to compare the printing performance of three primary stencil technologies: chemical etch as well as laser-cut and electroformed stencils. In addition, the effects of EP and nickel plating on chemically etched and laser-cut stencils have been studied. Similar work was also reported by Coleman [71], who compared the solder paste printing performance of the laser-cut and electroformed stencils and the effect of post-surfacing finish on the laser-cut stencil's quality. All the stencils were printed at the same printing parameters and a type 3 no-clean paste was used to evaluate the print performance of the stencils. To evaluate the print performance of these stencils, relative solder paste volume was used as the response parameter. The study indicated that electroformed stencils provided better print performance and provided acceptable printing performance down to an area ratio of 0.5. Another study by Coleman and Richter [72] evaluated stencils coated with thin films of titanium nitride (TiN) and chromium nitride (CrN), which could achieve the smooth release of the solder paste from stencil apertures. These coatings may be provided on the squeegee blades to ensure were resistance and provide a low coefficient of friction. The degree of EP is defined by the time for which the stencil is kept submerged in the electrolytic bath. During the process, the high points on the aperture wall are attacked and they leave the walls to give it a smooth and shiny appearance. But if sufficient time is not provided for the rough points to separate from the walls, they could hang out from the walls, making the walls even rougher. A very high time for EP will make the walls more shiny and smooth but also make the edges round, which can affect the gasketting of the

stencil to the pads. So, a balance has to be achieved between the wall smoothness and the edge roundness to achieve good prints. Painaik [63] conducted a study to compare the print performance of laser-cut and chemical etched stencils in a single print stroke. Additionally, the effect of different levels of aperture taper and EP are studied in a single stroke. Specially designed stencil, with all the possible combinations of taper and EP, are utilized. It is found that apertures having area ratio greater than 0.66 behaved differently when compared to apertures having area ratio less than 0.66. The experiment provided the best possible combination of taper and EP for apertures greater than 0.3 mm aperture sizes. These studies have analyzed the effects on the small apertures of various stencil fabrication practices and laser-cut stencil post-surfacing treatments. However, little work has been reported on the effects of EP factors, particularly those of aperture quality and stencil printing performance.

2.2.4 Characteristics of solder powder

With the growing demands for increasing the package density, the performance and quality required for the solder paste are becoming critical. The importance of solder paste in the production process cannot be understated, as it significantly affects the entire soldering line from solder paste printing, through reflow and beyond.

The important characteristics of solder paste that need to be considered from a process perspective include the following: solder powder particle size, metallurgy, slump, temperature and humidity sensitivity, solid contents, type of flux residue, viscosity and the propensity of solder balling [73]. The particle size is dependent on the component pitch. It is desired to have the aperture width greater than or equal to 4-5 times the particle diameter [74]. The use of ultra-fine pitch packages decreases the aperture sizes, which advocates the use of smaller particle size.

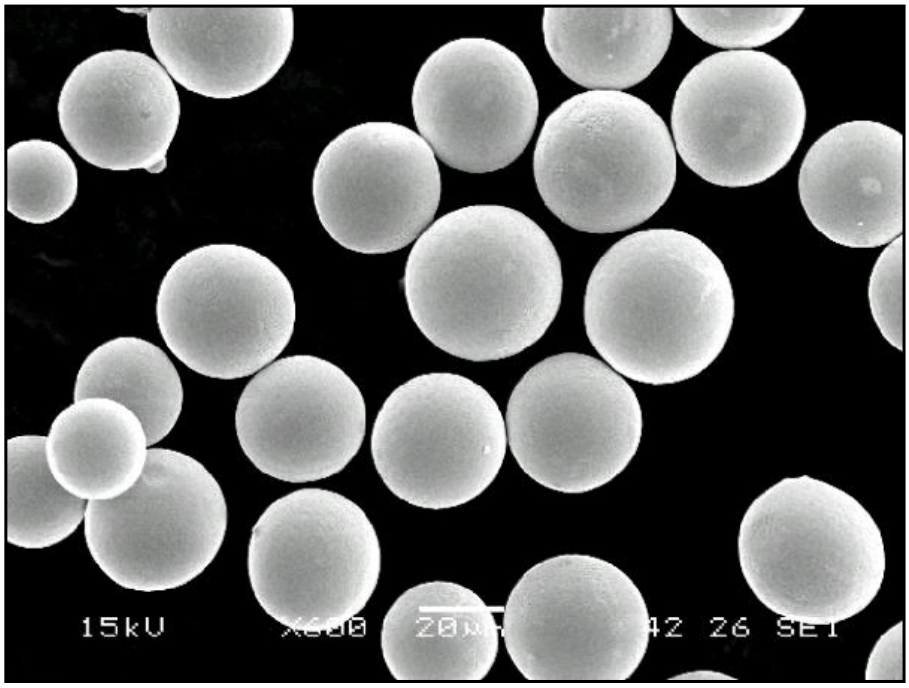
For the electronics industry, the solder powder used can be categorized into the dimensions shown is Table 2.2 [75]. Due to the miniaturization trend of the surface mount industry, the prevailing solder powder size also reduced with time. Type 2 solder powder was used prior to the early 1990s. Type 3 solder paste is more widely used by most manufacturers in the assembly of standard SMT components and fine-pitch components. Consequently, it would save a lot of time for the manufacturer if type 3 pastes could be used for the assembly of BGAs,

CSPs and 0201s, which would otherwise be spent in characterizing the entire assembly process for a type 4 paste. Additionally type 3 pastes are much cheaper type 4 and type 5 pastes. Figures 2.9 and 2.10 shows an example of a type 3 and type 4 solder powders.

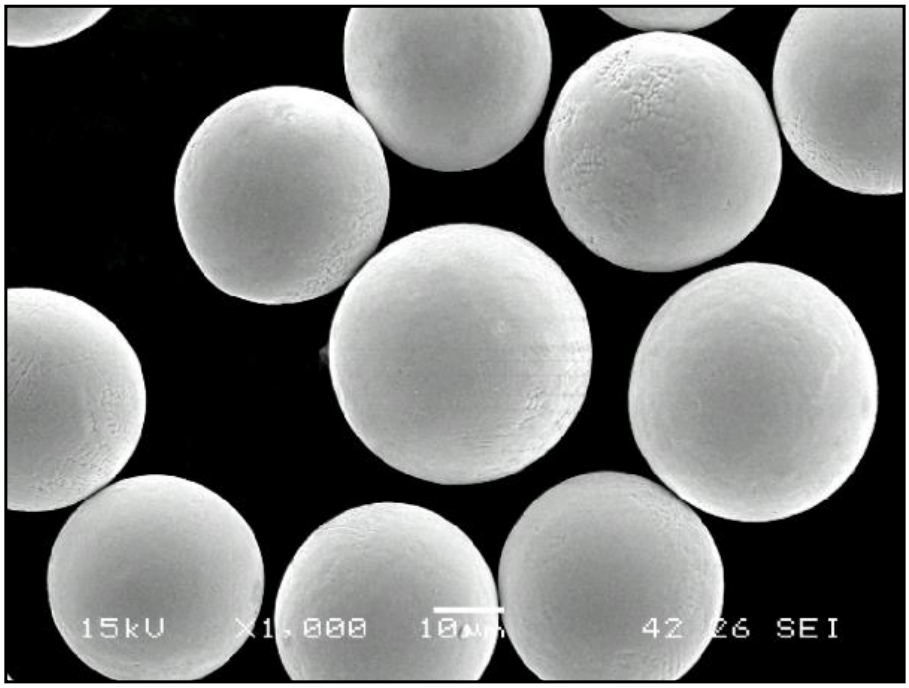
Lead-free solder alloy powders are now being developed exhibiting type 6 and type 7. Although powder sizes of type 6 and type 7 are not common, there is already a demand for those powders. Currently, these fine powders are primarily intended for use in either ultra-fine pitch applications or wafer solder paste bumping [76].

TABLE 2.2 Classification of solder powder size, expressed as percent of sample by weight – nominal sizes [75]

Category	None larger than	Less than 1% larger than	80% minimum between	10% maximum less than
Type 1	160 μm	150 μm	150 – 75 μm	20 μm
Type 2	80 μm	75 μm	75 – 45 μm	20 μm
Type 3	50 μm	45 μm	45 – 25 μm	20 μm
Type 4	40 μm	38 μm	38 – 20 μm	20 μm
Type 5	30 μm	25 μm	25 – 15 μm	15 μm
Type 6	20 μm	15 μm	15 – 5 μm	5 μm



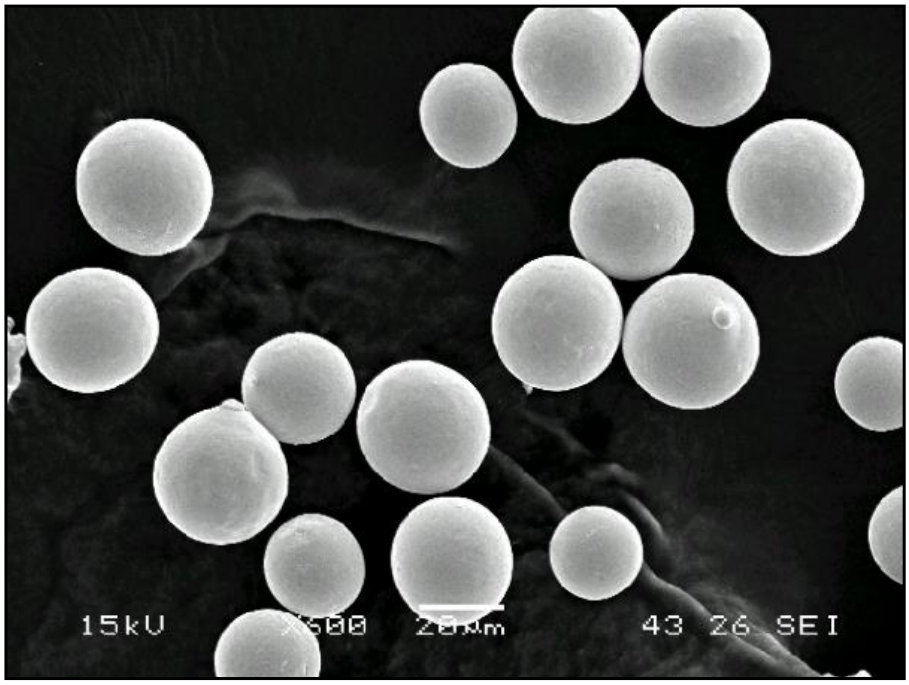
(a)



(b)

FIGURE 2.9 SEM pictures of type 3 95wt.%Sn–5wt.%Sb solder powder.

Notes: (a) X600; (b) X1,000. (SOURCE: Tamura Co.)



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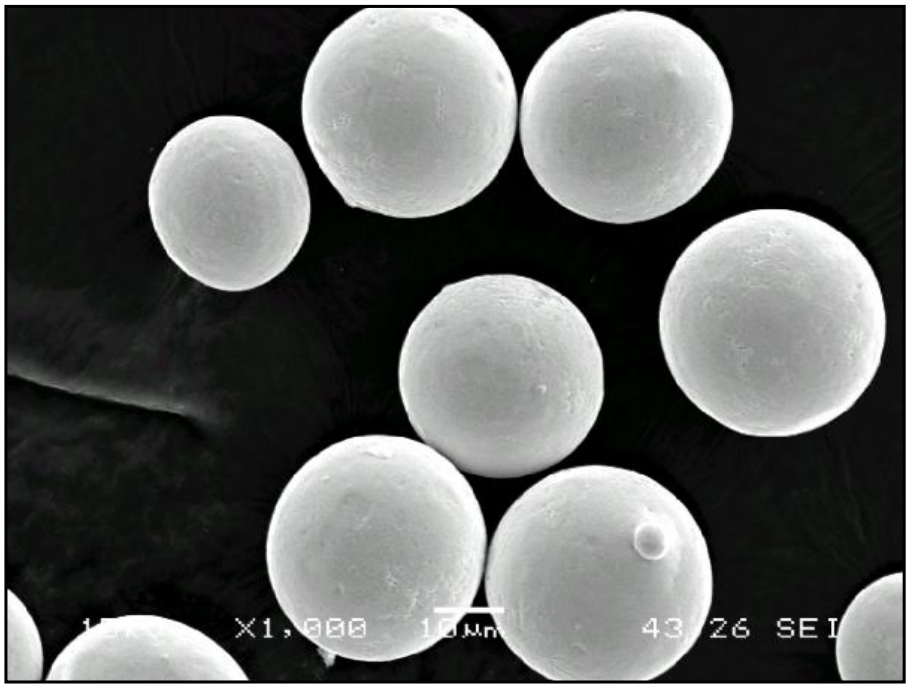


(b)

FIGURE 2.10 SEM pictures of type 4 95wt.%Sn–5wt.%Sb solder powder.

Notes: (a) X600; (b) X1,000. (SOURCE: Tamura Co.)

2.3 High-density substrate and assembly defects

2.3.1 Micro via-in-pads

The electronics manufacturing industry is continuously facing demands for smaller, lighter and more powerful devices [49]. This demand has led to the introduction of PCB with micro via-in-pad technology, which allows more space between pads for trace routing, thus enabling a higher I/O density design [14].

Micro via-in-pads are defined by IPC-02315 and IPC-6012A standards as blind and buried vias that are equal to or less than 152 μm in diameter with a target pad equal to or less than 356 μm in diameter. The target pad is defined as the land on which a micro-via ends and makes a connection [77].

Micro via-in-pads in SMT applications allow the realization of low costs, high densities, high speeds and miniaturization for electronic devices. However, along with all of the advantages described above is the observation of a high occurrence rate of voiding in the solder joints involving micro via. The trouble is getting worse with the prevalence of BGAs and CSPs, particularly in the presence of micro via. In this text, the micro via-in-pad-related defects, such as voiding, spattering, and tombstoning will be briefly discussed in more detail.

2.3.2 Voiding and spattering defects

Voiding is defined as cavities and bubbles in solidified solder, which may deteriorate electrical, thermal and mechanical properties of the solder joint [78]. In some cases, the cavities may be filled with flux due to surface roughness and low temperature soldering process [79]. Furthermore, void volumes add to the thickness of the joint volume, thus increasing the joint thickness, resulting in higher thermal resistance. Over the years, researchers have identified several parameters that can be attributed to void formation. These factors can be distributed into four categories – materials, methods and machine, environment and human factors [80]. Each of these categories can be further subdivided into several sub-categories. In the following schematic, all of the factors and their sub-factors leading toward void formation are illustrated (Figure 2.11).

Voiding is caused by outgassing which in turn is the result of fluxing reactions or flux volatiles. When a solder paste is used for BGA attachment onto the card with via-in-pads, the

paste filled within the via-hole will melt, coalesce, and wet to the parts at the same time. During this coalescence process, some flux will inevitably be temporarily entrapped within the molten solder. At this stage, any outgassing from the entrapped flux will result in voiding. Coalescence of small voids plus the effect of buoyancy plus the low standoff eventually result in a large void stuck at the top of the solder joint. An example of a via-in-pad solder joint with a trapped void is depicted in Figure 2.12.

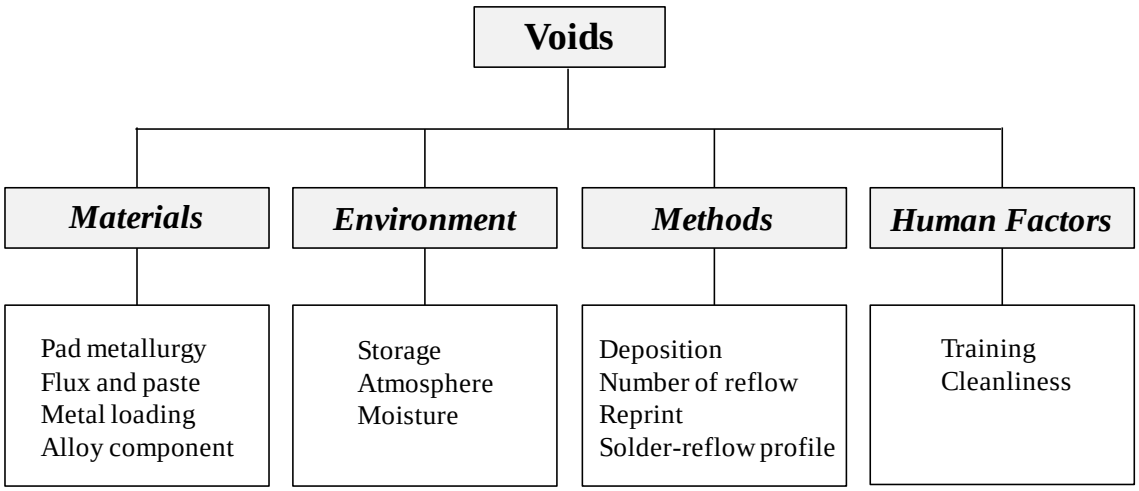


FIGURE 2.11 Factors contributing to void formation [80].

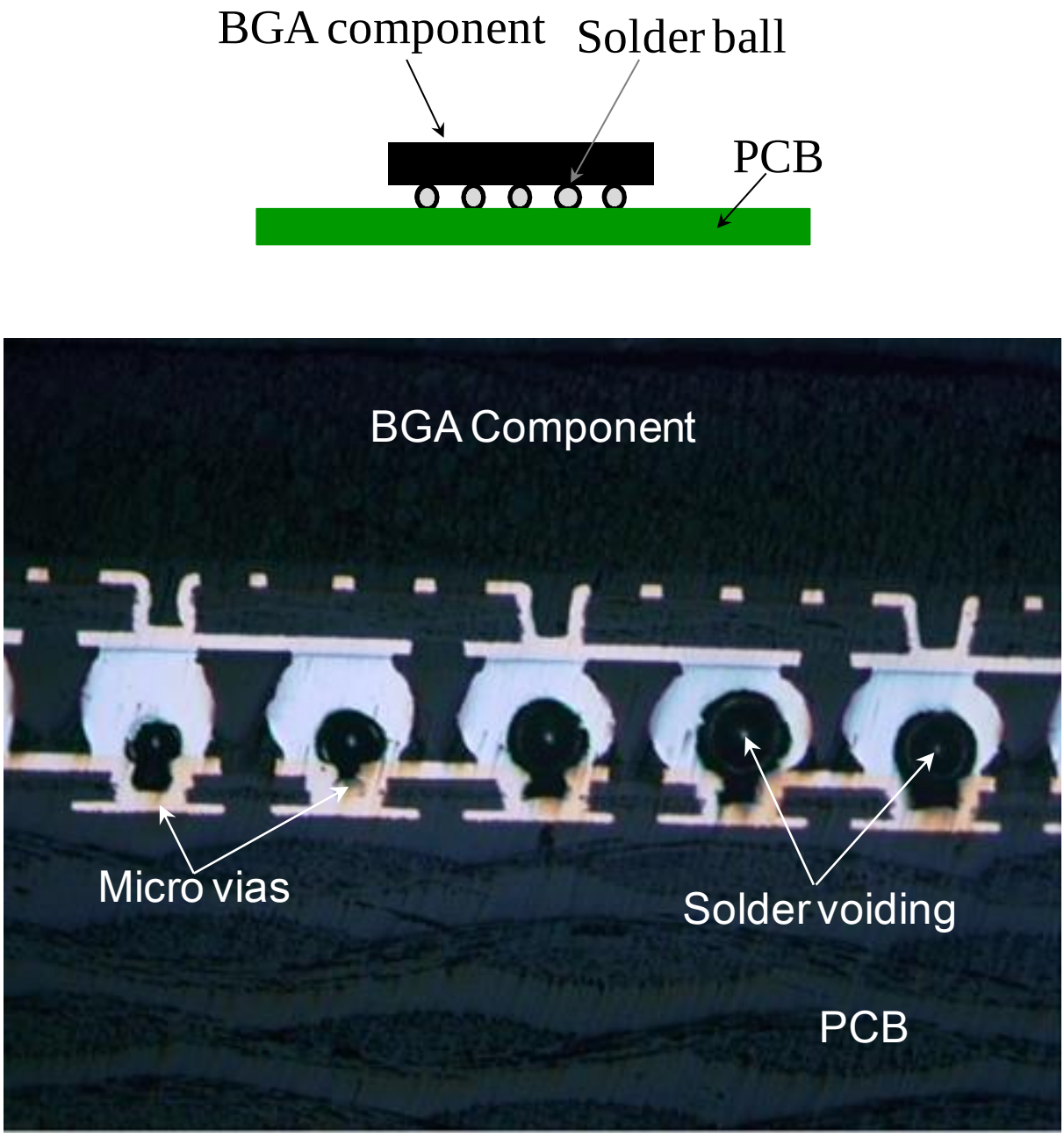


FIGURE 2.12 Cross-section of BGA solder joints formed on micro via. Voids tend to form at the opening of micro via [81].

The current literature offers a significant amount of information on evaluating the impact of micro vias on void formation [82-84]. Jo *et al.* [84] have studied voiding mechanisms in micro via board for CSP assembly using SnAgCu lead-free solder paste. In their results, voiding was found to decrease with increasing number of solder paste printing, increasing flux activity, decreasing solder powder size, decreasing metal content, decreasing peak temperature, and use of linear ramp profile instead of profile with a soaking zone. In addition, the effect of reflow profile on voiding at micro via for lead-free soldering was dependent on the flux chemistry.

Grano *et al.* [83] presented the soldarability results for different via-in-pad locations and sizes based on assembly criteria. In their study, the location of the via-hole had an effect on void formation. With the via-hole located in the center of the pad was an increase in voiding.

Their findings are very useful in enabling an understanding of the voiding mechanism and the factors impacting void formation at micro via and lead-free solder conditions. However, most of the earlier research findings were based on the assembly of BGA or CSP packages and do not provided sufficient guidelines for the assembly of tiny discrete components such as 0201 and 01005 chip components.

In general, the solder composition and structure of solder pastes have the most significant effect on void formation [85]. Huang *et al.* [86] studied the effect of solder composition on voiding. They evaluated the soldering performance of five SnAgCu and one eutectic SnPb solder alloy systems. The voiding was found to decrease with increasing Ag content for SnAgCu solder alloy.

The 95wt.%Sn–5wt.%Sb solder is a solid solution of antimony in a tin matrix. The relatively high melting point of this alloy makes it suitable for high temperature applications [87]. However, this alloys used for the assembly of SiP module introduce new process challenges. The wettability of lead-free alloys, especially Sn-Sb alloys, is lower than the eutectic Sn-Pb alloy [3,88,89]. In order to improve the wettability of lead-free solder pastes, they are formulated with a very active flux. These fluxes have a tendency to explode (or burst) during the reflow operation and create flux spatters on the PCBs. As the solder melts and coalesces, surface tension of the molten material exerts pressure on the entrapped flux. When the pressure exerted is high enough, flux is expelled violently [90]. This is commonly referred to as the coalescence theory [91].

Spattering is the spitting of flux or solder around solder joints at reflow, and it may reach more than several millimeters [14]. Spattering causes many process problems with sensitive electronic components. For example, if the spattered solder lands on nearby wire bond fingers, it can form slight bumps that may create a disruption of the planar surface of wire bond fingers and hinder contact with the connector. An example of the solder spattering is depicted in Figure 2.13.

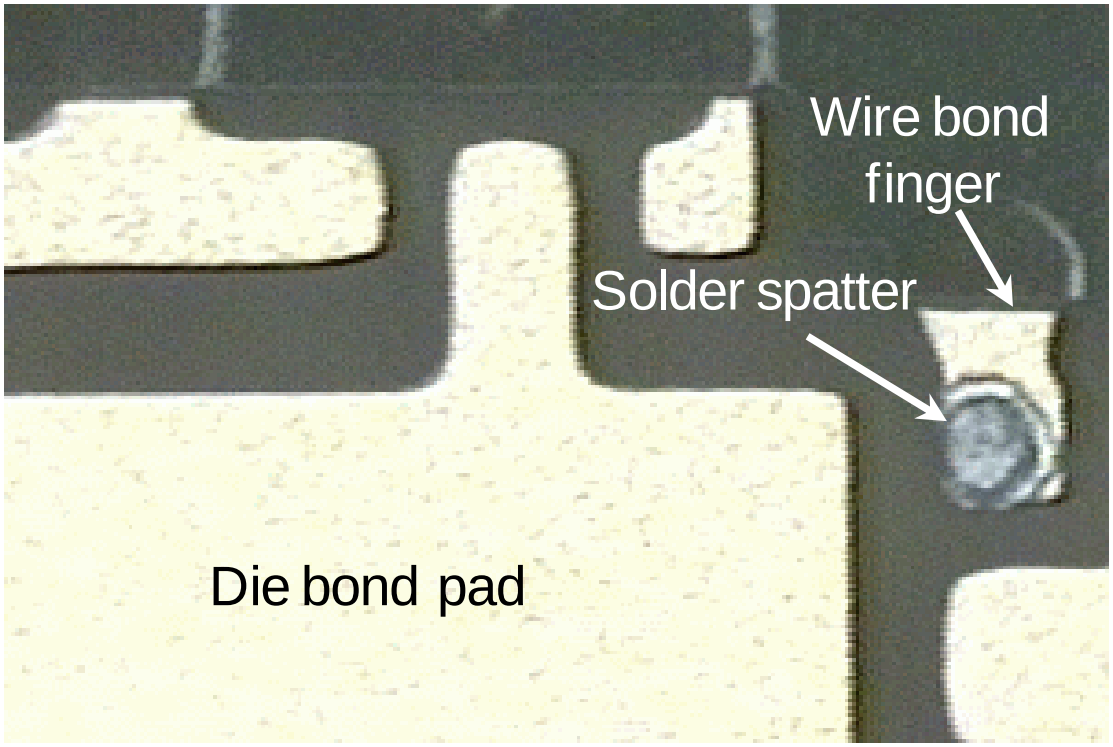


FIGURE 2.13 Picture of solder spattered at reflow. Note the tiny solder droplets on the wire bond finger.

2.3.3 Tombstoning defect

Tombstoning is the lifting of one end of a leadless component, such as a capacitor or a resistor, and the standing on another of its ends, as shown in Figure 2.14. It is caused directly by an unbalanced wetting of the two ends of the component at reflow, and accordingly, the unbalanced surface tension pulling force of the molten solder is exerted onto the two ends, as illustrated in Figure 2.15. Here, there are three forces exerted onto the chip:

(1) the weight *F1* of the chip;
(2) the surface tension vertical vector *F2* of the molten solder surface beneath the chip; and,
(3) the surface tension vertical vector *F3* of the molten solder surface on the right side of the chip.

Forces *F1* and *F2* pull downward and tend to keep the component in place, whereas force *F3* presses onto the chip corner and tends to tilt the component into a vertical position. Tombstoning occurs when force *F3* overrides the sum of forces *F1* and *F2* [14]. In addition, tombstoning is also sensitive to other factors, including the pad spacing, pad size, chip termination dimension [14,92], solder alloy compositions [93,94], paste type, preheat slope, and surface finish condition [95]. Lee and Evans [92] have reported that unbalanced wetting can be aggravated by the use of a flux with a short wetting time during the reflow process. Thus, a short wetting time is found to result in a greater occurrence of tombstoning.

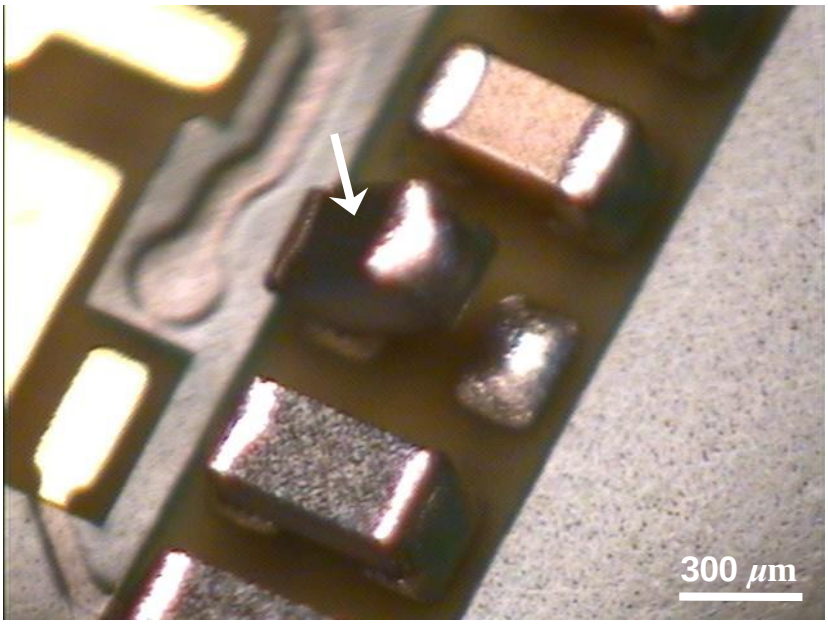
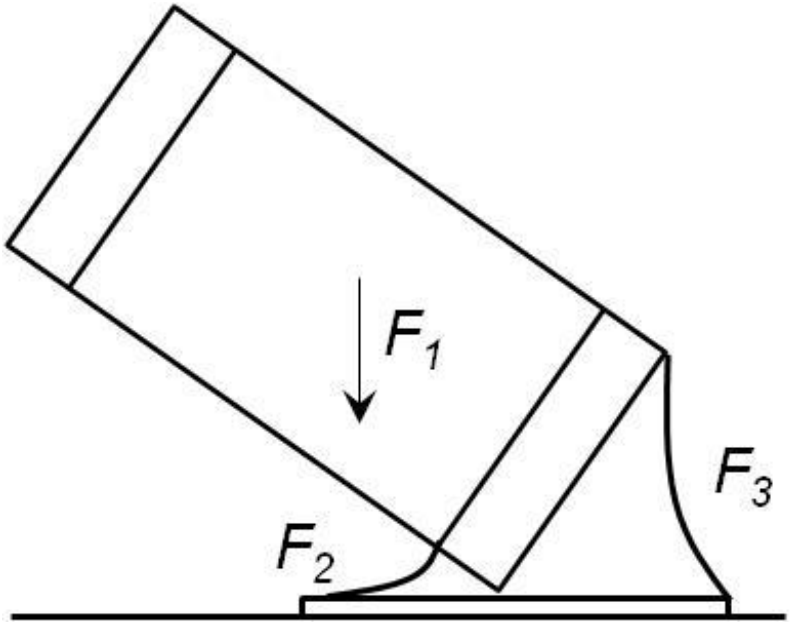


FIGURE 2.14 Example of tombstone, indicated by the arrow: 0201 chip resistor stands on one of its ends.



Note: Tilting will occur if *F*1 + *F*2 < *F*3

FIGURE 2.15 Schematic representation of the forces acting on a chip as it tombstones [14].

2.4 Lead-free assembly and rework

Rework is the term in the electronics industry that pertains to removing and subsequently replacing one or more of the components or other attachments on a PWB, as depicted in Figure 2.16 [2]. The procedure typically consists of locally heating the solder joints of peripheral or area array packages. When the solder joints melt, the component is lifted away from the board either by mechanical means or by a vacuum-activated device. A replacement component is locally reflowed to the same site. Sometimes the board is also heated from the underside to lower the thermal gradient and to help eliminate warping.

Rework is an important aspect of manufacturing that helps meet required yields to achieve economic viability– another aspect that is anticipated to be substantially affected by a change to lead-free technology. Rework operators, such as inspectors, will require additional training, and development will be necessary because the properties and melting points of the solders can be significantly altered from component to component across an assembly because of elemental additions introduced to the solder from the PWB and terminal pad metallization systems [2].

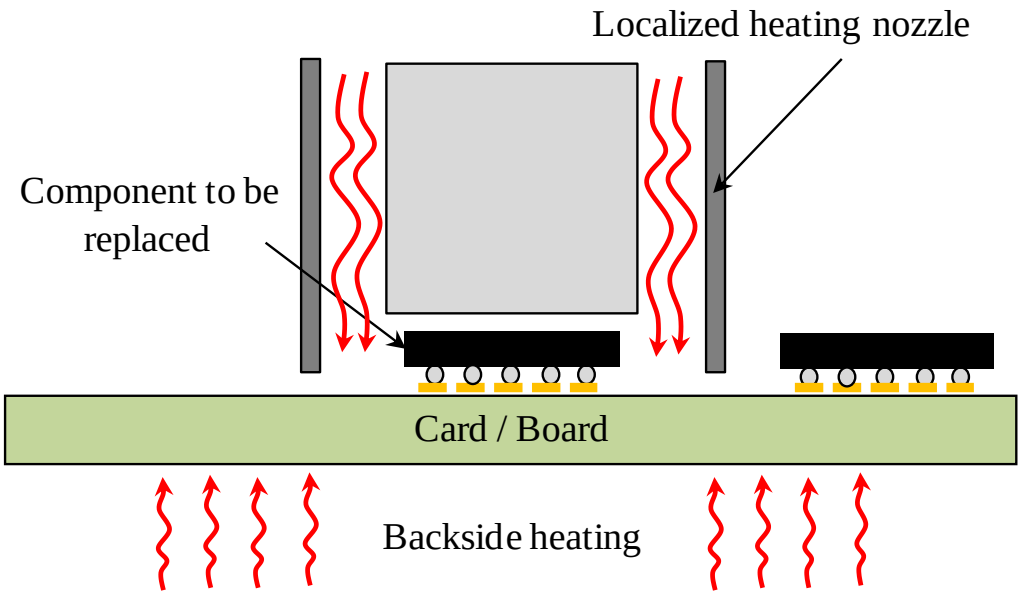


FIGURE 2.16 Illustration depicting the replacement of a component attached to a printed circuit board (PCB) utilizing a localized heating technique [2].

2.4.1 Lead-free rework assembly for BGA and CSP packages

The trend by the electronics industry toward the miniaturization of electronic assemblies resulted in the development of BGA packages [96]. Although BGAs provide density and yield advantage, they also provide the assembler with rework obstacles. With solder bumps hidden from view, reflow cannot be visually verified.

Rework refers to the general technical problem of removing and replacing defective circuit components on a printed circuit board [97]. Area array package rework includes the process of reworking BGA and/or CSP components. Area array package rework typically comprises of five major steps: component removal, site cleaning, solder paste/flux replenishment, component replacement, and reflow. The flow chart in Figure 2.17 summarizes the process steps involved in area array rework [98].

Two methods are currently used to rework BGA components. One approach uses the solder paste deposition method and the other uses a flux-only application method. Metal stencil is the most common method used to selectively apply solder paste in BGAs reworking. Plastic film stencil can be used on a one-time only basis. The selective solder paste printing process requires more skill and more attempts to produce an acceptable paste deposition than the flux application methods. The flux-only method is usually selected for a BGA rework process, due to its simplicity. From the viewpoint of reliability, selective solder paste printing is a more reliable rework process compared to the flux-only attachment method [99]. Using the flux-only application decreases the long-term reliability of a solder joint because excessive flux residue may residue the surface resistivity of the PCB surface [100,101]. However, the solder paste deposition method requires more skill, and more attempts, to produce an acceptable paste deposit than the flux-only application method.

2.4.2 Challenges in lead-free BGA and CSP rework assembly

As noted previously, the preliminary challenge that lead-free solders presents to IC and component manufacturers, and electronic assemblers is the higher temperature typically required of lead-free solders. The generally accepted limit that IC packages can withstand is approximately 235–240°C and the lower limit to reliably reflow eutectic Sn-Pb solders is about 200–205°C. This

provides approximately a 30°C process window, which is sufficient in a properly monitored line to produce a low-defect-rate, high yield product with little concern for creating process drift-related defects. However, with lead-free assemblies, the process window shrinks dramatically, as illustrated in Figure 2.18. With bismuth-containing alloys, whose liquidus temperatures typically range between 206°C and 213°C, the window shrinks by one third, to approximately a 20°C operating range. For Sn–Ag–Cu alloys, whose liquidus is 217°C, the window is reduced by two thirds, with an operating range of only 10°C. Given that assemblers desire to remain within 5°C of their control limits, the true process window is very small. However, it has been determined that the soldering process can be significantly optimized by obtaining and analyzing data on a real-time basis in a reflow oven. Process control can be aided by utilizing prediction software that customizes a profile for a specific solder paste, product type, and user-defined input process limit [102].

The main technical challenges during lead-free BGA rework process are component body temperature and limitation of the maximum allowable component temperature because of the relatively high temperature applied to the printed circuit board assembly (PBA) and components [103]. Due to the narrow process window available for lead-free BGA components rework, it is essential to conduct a comprehensive study researching various alternatives for each rework process step in order to arrive at a reliable and repeatable rework process.

Several rework studies were reported to help develop the capability to manufacture lead-free PBAs. Gowda *et al.* [36] discussed the challenges in lead-free rework process focusing on several surface mount devices, such as CSPs, micro-lead devices, and passive components. In a previous paper by Gowda and Srihari [104] process guidelines for fine-pitch components and CSP in particular were developed and were presented. Nguty *et al.* [35] has demonstrated the rework techniques available for CSP and pads clean-up and deposition methods have been evaluated. Manjunath *et al.* [98] recently have reported a detailed study on lead-free rework process development and reliability. In the reliability testing results, all test samples subjected to thermal shock and thermal cycling passed through 200 and 1,000 cycles, respectively. Although most of the earlier research findings a good level of confidence regarding the process developments and the reliability assessments of the reworked components, the rework processes

still represent a major technical challenge in printed board assembly industry due to the narrow process window. These challenges must be solved in order for area array packages to gain acceptance as an option for high-speed and high-yield assembly.

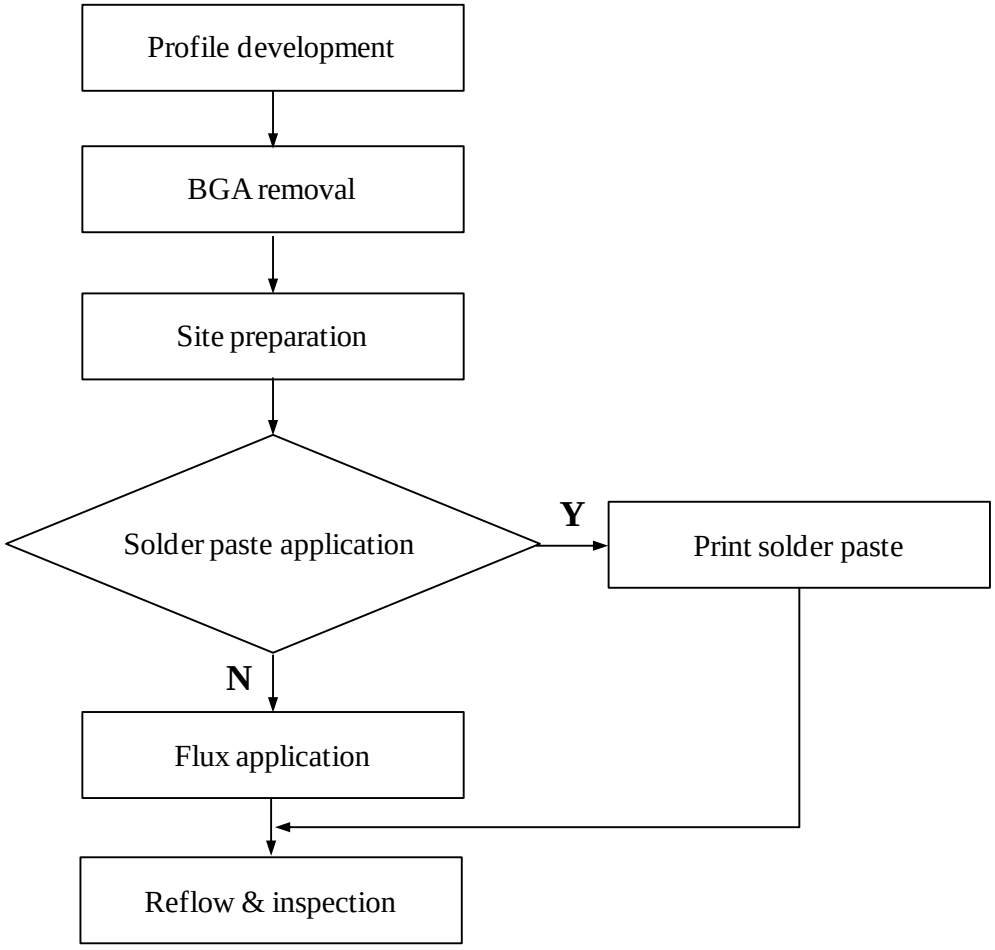


FIGURE 2.17 Area array package rework process [98].

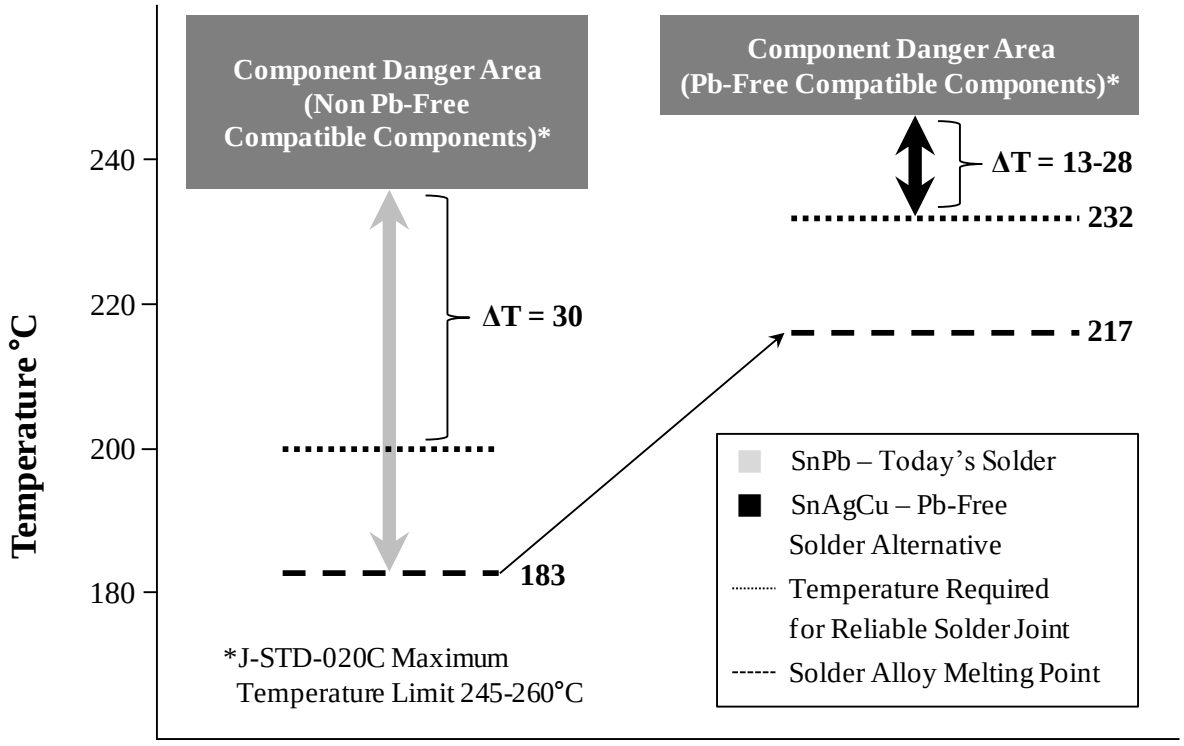


FIGURE 2.18 Lead-free tighter process window. The diagrams show a significant reduction in the Pb-free process window compared to SnPb assembly; this is caused by the difference in melting temperatures and component survival ability [105].

In practice, the PCB is subjected to multiple reflow cycles during the BGA rework process of removing the components, cleaning the site, and soldering the new components. The high processing temperature and the multiple reflow may result in the degradation of the reliability of the solder joint and the quality of the solder joint. This high temperature may also influence the components that are adjacent to the reworked area. Gleason *et al.* [37] have reported that the reliability performance of adjacent components resulted in significant reduction in thermal fatigue resistance. With careful optimization, it appears that rework can be accomplished without damaging temperature-sensitive parts with minimal board warpage. The same issues apply to rework of general assembly operations, soldering temperatures and other parameters must be tightly controlled [12].

2.5 Summary

The continuing demand for smaller, lighter, portable products has driven the use of 01005 chip components. The use of this tiny component presents several significant challenges to the SMT assembly process. Significant process issues include solder powder selection, determining the optimum printed circuit board pad design, the optimum stencil aperture design, and component placement nozzle selection, solder paste printing and stencil selection, and reflow profile. One particularly significant issue is designing a stencil that will optimize the printing of the 01005 chip component and the surface finish of the aperture walls has a significant impact on the paste release phenomenon.

On the other hand, BGA and CSP are taking center stage now for producing miniaturized high density electronic devices. Although the leadless feature allows them to be processes easily without the need of ultra-fine pitch equipment capability, the two-dimensional area array I/O feature imposes a great challenge on the assembly and rework due to the temperature gradient factor and the hidden joint formation process. The challenges discussed in this chapter show that additional considerations should be given in order to have a high yield process.

PART II: MINIATURE-SIZED CHIP COMPONENT ASSEMBLY

Chapter 3

The effect of selected process parameters on defects in the assembly of 01005 chips[1]

Packaging trends throughout the history of electronics manufacturing have moved progressively toward the characteristics of being smaller, faster, lighter, and cheaper, as discussed in Chapter 1. The purpose of this study is to optimize the surface mount assembly processes to minimize defects in the assembly of 01005 chip components. During the study, solder paste printing process-related variables, such as solder paste types, stencil types, and stencil opening ratio, and pick and place process-related methods, such as vision camera types and vacuum pickup nozzle types were evaluated with the goal of achieving a high yield assembly solution for 01005 chip components. Temperature cycling between – 65 to 150°C, with up to 1,500 cycles, show that no cracks were observed at the solder joints due to temperature cycling. The process and design change required for achieving a robust manufacturing process have been indicated and reported. The results of this work provide assembly process recommendations for the implementation of 01005 sized chip component assembly in mass production processes.

[1] Based on Yong-Won Lee, Keun-Soo Kim, and Katsuaki Suganuma (2011), "Process characterization and reliability for the assembly of 01005 chip components", *Soldering & Surface Mount Technology*, Vol.23 No.4, pp. 235–243.

3.1 Objective and overview

The increasing functionality of ever-smaller wireless products, in particular, is driving the evolution to thinner PCBs and parts, the use of smaller electrical parts in greater numbers, and narrow and adjacent mounting technologies. The size of the smallest components used extensively in products for today's mobile electronics sector is 0201, but 01005 parts are already beginning to appear in higher frequency modules [106], as shown in Chapter 1.

Although miniature-sized components, such as 01005, enable the effective use of the limited real estate to form complex circuitry, their introduction has posed new challenges during the SMT assembly processes. These challenges must be solved in order to for miniature-sized components to gain acceptance as an option for high-speed and high-yield assembly.

This chapter summarizes previous assembly and reliability issues encountered in developing and implementing 01005 components for the high volume manufacturing of high-density system-in-package modules using lead-free solder alloy. Assembly yield (e.g. pickup rate and SMT yield), defects (e.g. insufficient fillet, tombstoning, misalignment and missing), quality (e.g. joint shape, coverage, and solder height) and reliability assessment data of component shear strength, and temperature cycling are included in this chapter.

3.2 Experimental

A four-layer BT board test vehicle with a nickel/gold finish was used in the study. The test vehicle was a 10 mm × 10 mm laminated module, composed of a 5 × 5 × 3 matrix and consisting of 3,000 pad layouts for 01005 chip components, and 1,950 pad layouts for 0201 chip components. The solder pads were semi-solder-mask-defined (SMD) pads for the 01005 and 0201 chip components. All pad shapes were also distributed equally in the horizontal orientation and the vertical orientation (Figure 3.1). Details of pad dimensions are shown in Table 3.1.

The solder paste used in this experiment was water soluble 95wt.% Sn–5wt.% Sb, the metal content was 90 percent, and the solder melting point was approximately 232–240 °C, as specified in the supplier's specification (Alpha Metal WS609).

The test vehicles were assembled for each experimental group with lead-free passive components, such as resistors, inductors, and capacitors. The lead-free finish on the component terminal was 100 percent pure tin. Figure 3.2 shows the actual dimensions for the 01005 chip capacitor components used in the experiment. (The metric dimensions of the chip components were 0.4 mm × 0.2 mm and the imperial dimensional equivalents are converted values, i.e. mm divided by 25.4). Table 3.2 summarizes the component dimensional tolerances.

The stencil printing process was carried out using an MPM AP Excel printer with metal squeegee angled at 60° fitted to the printer. The following stencil printing parameters were used for all stencil printing: printing speed = 8 mm/s, print force = 5.3 kg, balance = 50:50 and print gap = 0. The solder deposited PCB substrate was inspected using a microscope equipped with a digital camera and documented photographically. The solder paste height measurement data were analyzed with the data obtained from the semi-SMD pads.

After obtaining the measurements of the solder paste bricks, the component placement was performed using a Siemens HS60 Pick-and-Place machine. A placement force of 1 N was used. Next, populated PCBs were soldered in a nine zone Heller 1800 convection oven with a nitrogen atmosphere. The nitrogen environment was controlled at an oxygen level of less than 400 ppm. The peak temperature was 251 °C, the time above 232 °C (the solder melting point) was 39 s, and the belt speed was 16"/min.

The following five variables were selected for this study: stencil type, solder paste type, stencil opening ratio, camera type, and vacuum pickup nozzle. The response variables were the height of the deposited solder paste, the component shear, tombstoning, solder bridging, misalignment, and missing components. In order to accomplish this, a designed experiment was conducted using various factors and levels as described below. For an experimental run, a total of 30 test vehicles were fabricated.

Stencil type

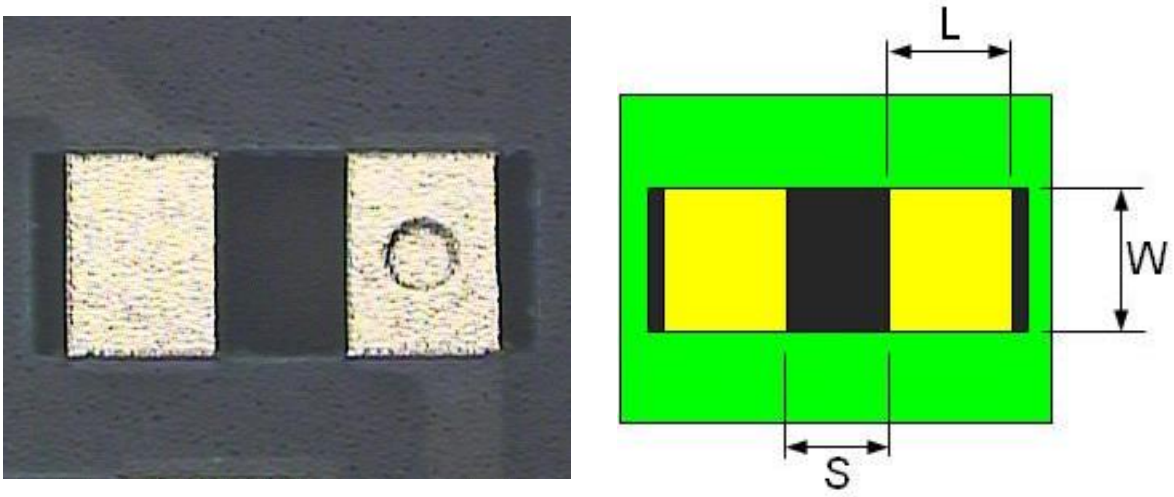
An experiment was designed to compare the solder paste printing behavior with different stencil types, such as electroformed stencil and electropolished laser-cut stencil with a solder paste type 4 (size range: 20–38 μm). The aperture shape was the same as the pad shape and the stencil opening ratio was set at 90 percent with a 0.08 mm stencil thickness.

TABLE 3.1 Pad dimension in the test vehicle

Components	L (mm)	W (mm)	S (mm)
01005	0.17	0.25	0.15
0201	0.30	0.36	0.22

TABLE 3.2 Dimensional tolerances for chip capacitors

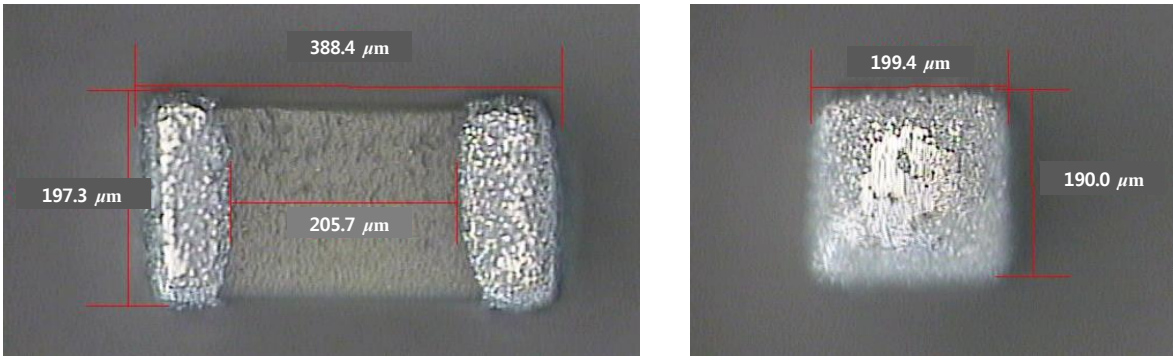
		Length (mm)		Width (mm)		Termination Width (mm)	
English	**Metric**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
01005	0402	0.38	0.42	0.18	0.22	0.07	0.14
0201	0603	0.57	0.63	0.27	0.33	0.08	0.20



(a) (b)

FIGURE 3.1 Schematic of component pad design for 01005 chip components.

Notes: (a) Photograph of pad and solder mask; (b) pad geometry.



(a) (b)

FIGURE 3.2 01005 chip capacitor components, metrics (mm).

Notes: (a) Top view; (b) side view.

Solder paste type

This study evaluated two types of solder paste particle sizes, namely type 3 (size range: 25–45 μm) and type 4 (size range: 20–38 μm). The stencil opening ratio was set at 90 percent with a 0.08 mm thick electroformed stencil.

Stencil opening ratio

To define the optimum stencil aperture, variants of the stencil opening ratio for the solder pads were set at 80, 90, and 100 percent. Furthermore, the evaluation was combined with two print offset conditions of the solder printer machine to investigate the self-alignment effect. Print offset conditions were set as 0 and 100 μm. A simulation of the print offset scenario is shown in Figure 3.3 and the experiment matrix is shown in Table 3.3. Type 4 solder paste with a 0.08 mm thick electroformed stencil was used in this work.

Camera

The pickup rate was recorded on a standard camera and a direct-chip-attach (DCA) camera from the Pick-and-Place machine. The DCA camera (pixel size: 27 μm) had a higher pixel size compared to the standard camera (pixel size: 50 μm). Standard cameras are currently used for 0201 components. Table 3.4 summarizes the different types of camera used to evaluate the pickup performance. A total of 18,000 components were evaluated. The stencil opening ratio was set at 90 percent with a 0.08 mm thick electroformed stencil.

Vacuum pick-up nozzle

Pickup rate and placement accuracy were recorded using a 906 vacuum nozzle and a 926 nozzle from an HS60 Pick-and-Place machine (Siemens). The 926 nozzles had a smaller nozzle vacuum hole size compared to the 906 nozzle (Figure 3.4). The 906 nozzles are currently used in 0201 components.

The reliability of the 01005 components was evaluated using temperature cycle testing and shear testing. These two tests were chosen to serve as basic metrics to indicate joint strength and reliability. Shear testing of the 01005 component was also performed using a Dage 4000 bond tester. All shear testing was conducted at room temperature with a shear height of 50 μm and a

pulling speed of 200 μm/s. For each experimental run, shear testing was conducted on ten or 20 randomly chosen components.

Fully assembled and defect-free boards were chosen for the temperature cycling. The temperature was cycled from – 65 °C to 150 °C with a frequency of two cycles per hour. The boards were subjected to temperature cycling for 0–1,500 cycles, with a 10° C/min ramp time and a 10 min dwell time. Measurements of the shear strength of the 01005 components were conducted at time zero (after assembly) and after 500, 1,000, and 1,500 cycles, respectively for both the 01005 and the 0201 components. An optical microscope and a scanning electron microscope (SEM, JEOL JEM-2000) were employed to observe the microstructure.

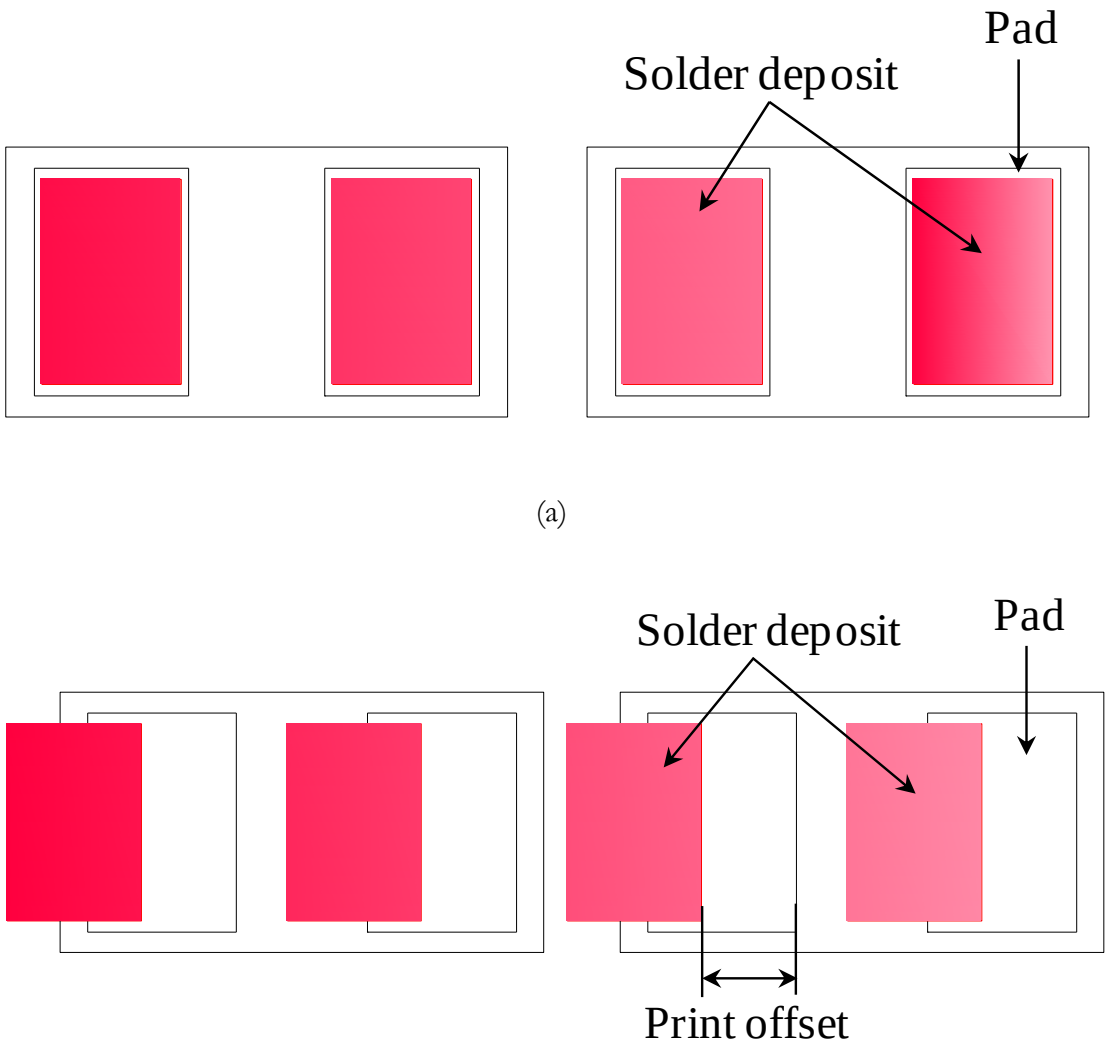


FIGURE 3.3 Print offset scenario for 01005 chip components.

Notes: (a) 0 μm; (b) 100 μm.

TABLE 3.3 Design of the experiment matrix

Test number	Stencil opening ratio (%)	Print offsets (*μ*m)
1	80	0
2	90	0
3	100	0
4	80	100
5	90	100
6	100	100

TABLE 3.4 Types of vision camera used

Items	Standard camera	DCA camera
Pixel size (*μ*m)	50	27
Field of view (mm)	24 × 24	15.6 × 15.6
Max. comp. (mm)	18.7 × 18.7	13 × 13

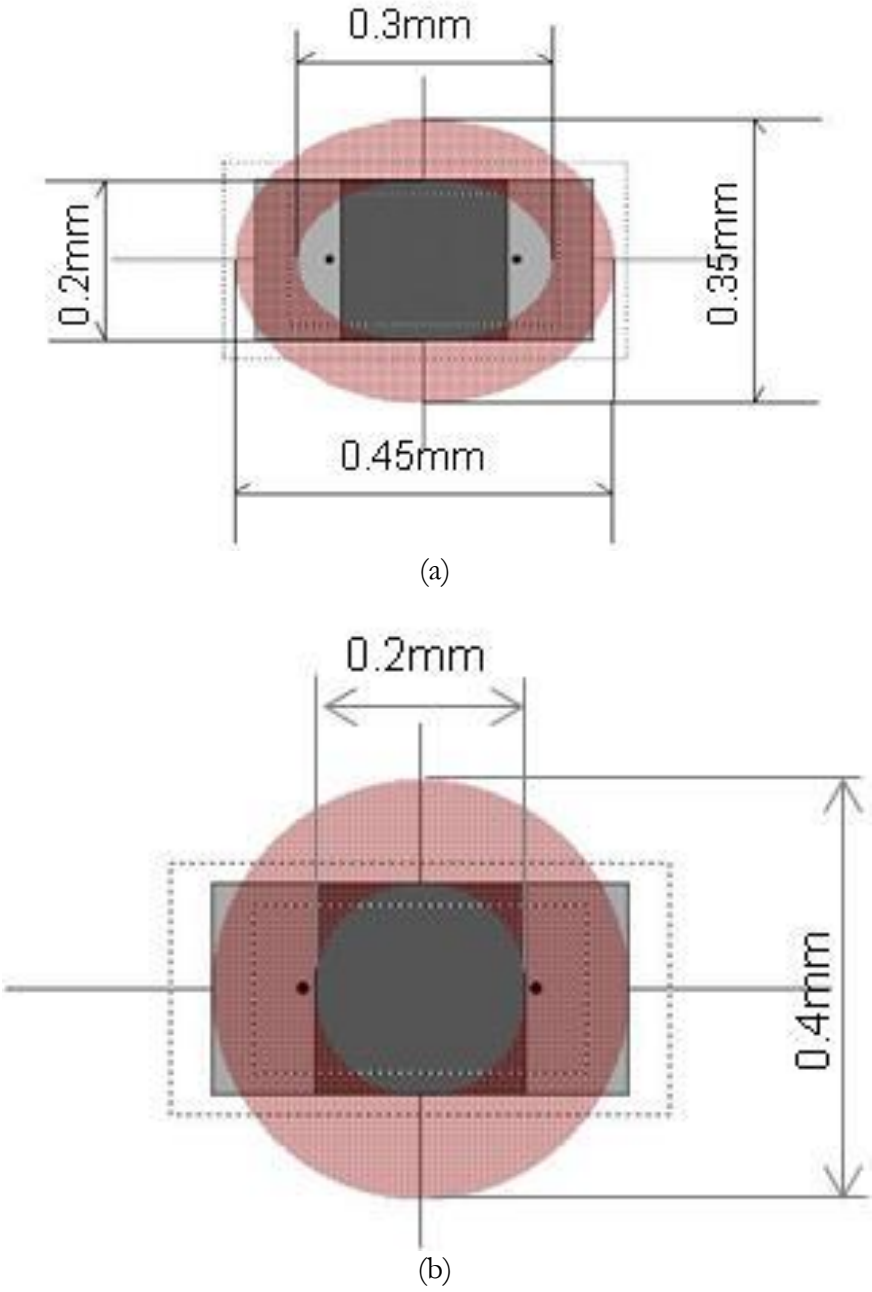


FIGURE 3.4 Nozzle types used in this experiment.

Notes: (a) 906 nozzle; (b) 926 nozzle.

3.3 Results and discussion

3.3.1 Assembly process analysis

The solder paste release behaviors, with different stencils, were compared, based on the thickness of the deposited solder paste. The box plot of the thickness of the deposited solder paste versus each stencil type is shown in Figure 3.5 and Figure 3.6, respectively, for the 01005 components and the 0201 components. The box plot shows the smallest value, the first quartile (Q1), the median, the third quartile (Q3), the largest value, and the outlier. From the Figure 3.5, the box plot reveals that the mean height of solder paste in the electroformed stencil was higher than that of the electropolished laser-cut stencil. It was necessary to determine if the difference observed was statically significant. This was done using the two sample-*t* test and the results are shown in Table 3.5. The results show that the *p*-value was 0.836 for each stencil type. This value of the two sample-*t* test indicates that the two stencils were not statically different (*p*-value > 0.05). Meanwhile, Figure 3.6 shows that the thickness of solder paste, deposited in the electropolished laser-cut stencil, was higher than that of the electroformed stencil for the 0201 chip components (*p*-value < 0.05).

TABLE 3.5 Two-sample *t*-test results for solder paste thickness comparison

Components	**Stencils**	*n*	**Mean**	**SD**	**SE mean**	***P*-Value**
01005	Electroformed	10	0.1011	0.0126	0.0040	0.836 ($p > 0.05$)
	Laser-cut	10	0.1000	0.0109	0.0035	
0201	Electroformed	10	0.1018	0.0076	0.0024	0.039 ($p < 0.05$)
	Laser-cut	10	0.1101	0.0087	0.0027	

Notes: SD - standard deviation; SE mean - standard error mean

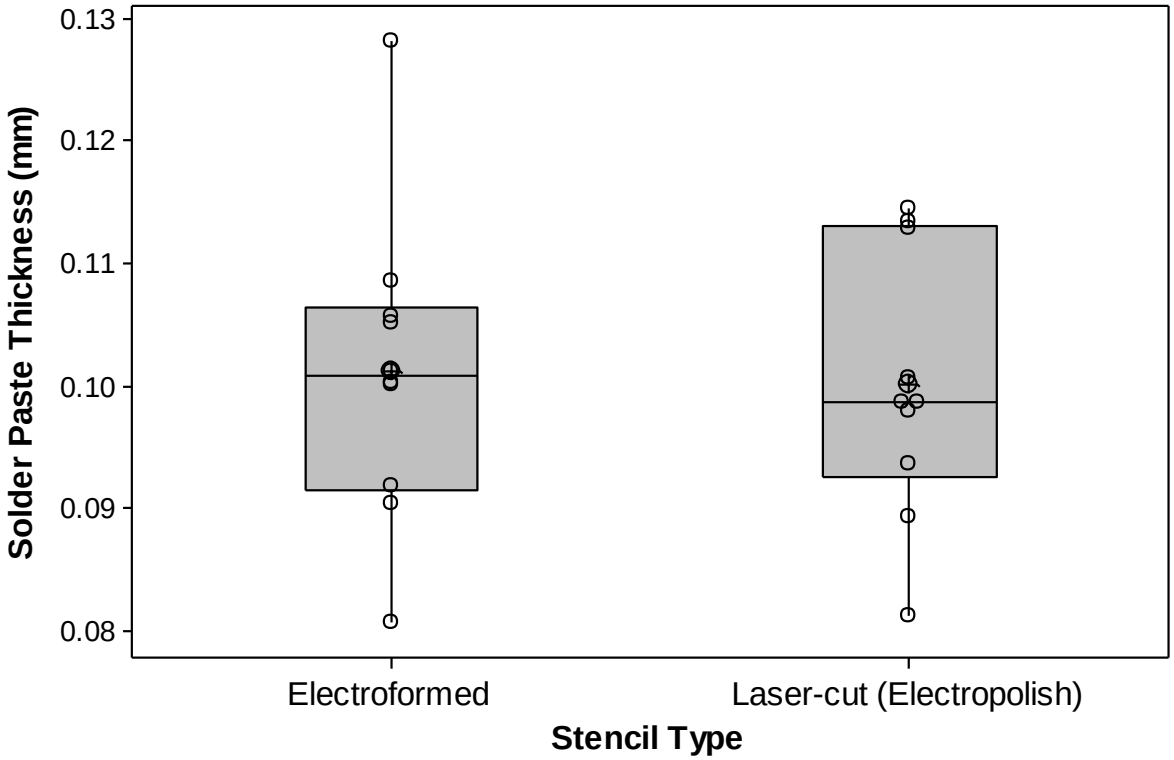


FIGURE 3.5 Solder paste thickness comparisons for 01005 chip components.

Note: The box plot shows the smallest value, the first quartile, the median, the third quartile, and the largest value.

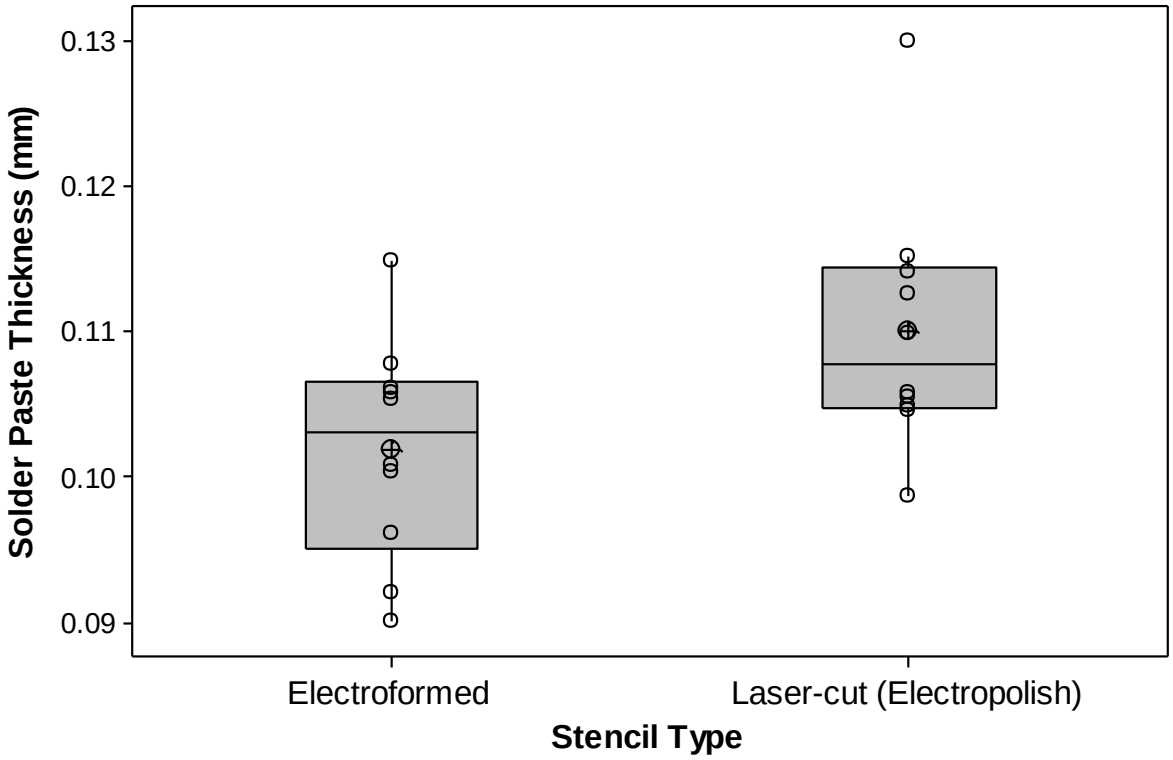


FIGURE 3.6 Solder paste thickness comparisons for 0201 chip components.

Note: The box plot shows the smallest value, the first quartile, the median, the third quartile, the largest value, and the outlier.

Figure 3.7 is a box plot comparing the component shear strength for each stencil type. The lower specification limit (LSL) was 1.47 N for the shear strength of the 01005 chip components. From the box plot, it can be seen that the shear strength in the electroformed stencil was approximately 25 percent higher than that of the electropolished laser-cut stencil.

The graph in Figure 3.8 contains process yield information. The graph shows that the electroformed stencil's process yield (97.9 percent) is slightly higher than the electropolished laser-cut stencil's process yield (97.5 percent). A total of five defects were also generated. One tombstoning and four misalignments were generated at the assembly with the electroformed stencil and six defects, including two tombstoning and four misalignments, were generated at the assembly with the electropolished laser-cut stencil.

Until now, the use of an electroformed stencil, rather than a laser-cut stencil, has been recommended to improve solder paste release in a high-density module assembly process to which the 01005-sized chip components are applied. Even though the electroformed stencil can implement high-quality solder paste printing, it has a shortcoming in that it requires a more complex manufacturing process that results in increased production costs. In this study, a general laser-cut stencil was electropolished to achieve high-quality 01005 module assembly at a low production cost. Consequently, a further detailed study is necessary that can help achieve a low-cost solution.

The solder paste release behavior for different types of paste particle sizes was studied for the 01005 components. Figure 3.9 shows some representative photographs from solder deposition on the 01005 and the 0201 pads for different paste types, such as types 3 and 4. Solder powder size had a significant effect on paste release and, hence, paste volume and coverage. The type 4 solder paste released better than the type 3 pastes. When a type 3 solder paste was used, several release defects, such as insufficient solder, were generated. This is in agreement with the information presented in several published articles about 01005 solder paste printing studies [39,51]. A type 4 paste has a smaller particle size, which will give a better paste release performance and aid in depositing more solder volume onto the pads. Therefore, to obtain the best and more repeatable volume of solder paste in a 01005 stencil printing, the particles required a smaller mesh paste, as can be found in type 4 solder paste, although a type 3 solder paste is typically used for more SMT applications.

After all boards had completed the reflow soldering, shear testing was performed for each type of solder paste. It should be noted that two failure modes were observed during the testing. They are fracture at the solder joint and component failure. Most of the components were fractured at the solder joint interface. The results of shear testing are shown in Figure 3.10. The type 4 paste exhibits an approximately 10 percent higher shear force than the type 3 paste. This is because the type 4 paste has a better paste release performance. It is clear from the print images (Figure 3.9) that a type 4 paste gave a more consistent, higher volume print than a type 3 paste.

The visual inspection of the test coupons was performed manually using a low-power optical microscope. The graph in Figure 3.11 contains process yield information. The yield comparison between type 3 and type 4 pastes shows that type 4 paste had a better yield performance. The graph notes that the process yield for type 4 paste (98 percent) was greater than the process yield for type 3 paste (95 percent).

Three types of stencil opening sizes were chosen to evaluate the soldering quality. Figure 3.12 shows the relationship between the stencil opening ratio and the height of the deposited solder paste. The graph notes that an increase in stencil opening ratio dramatically improves the height of the deposited solder paste. Figure 3.13 shows some representative images of the solder paste deposited for each stencil opening ratio.

Shear testing was performed to determine the integrity of each stencil opening ratio after the reflow process. The result of the shear test is shown in Figure 3.14. In general, an increase in stencil opening ratio improved the shear strength. Because the large stencil opening ratio was bigger, it provided more solder volume and, thus, higher shear strength. Comparing the shear strength per stencil opening ratio variants shows that the100 percent stencil opening ratio had stronger shear strength than the 80 percent stencil opening ratio.

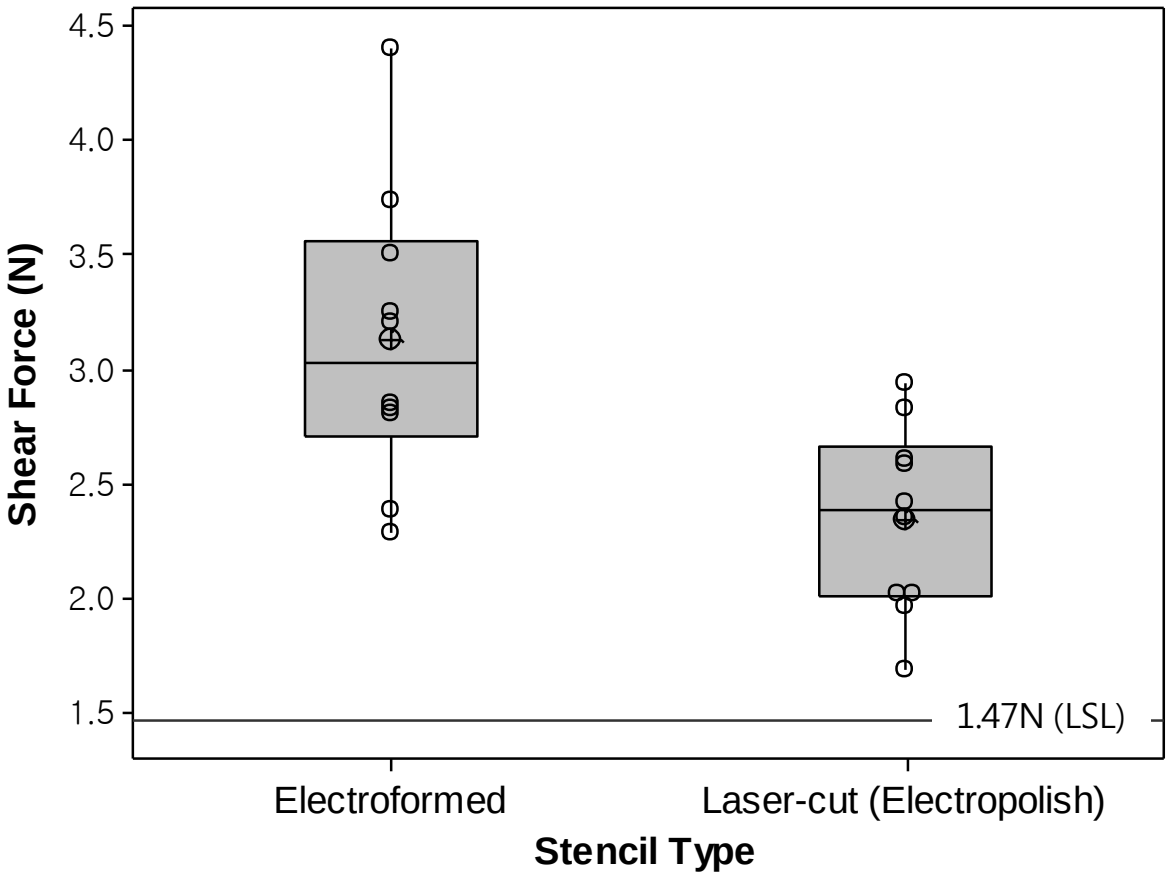


FIGURE 3.7 Shear force comparisons on 01005 chip components for each stencil type.

Note: The box plot shows the smallest value, the first quartile, the median, the third quartile, and the largest value.

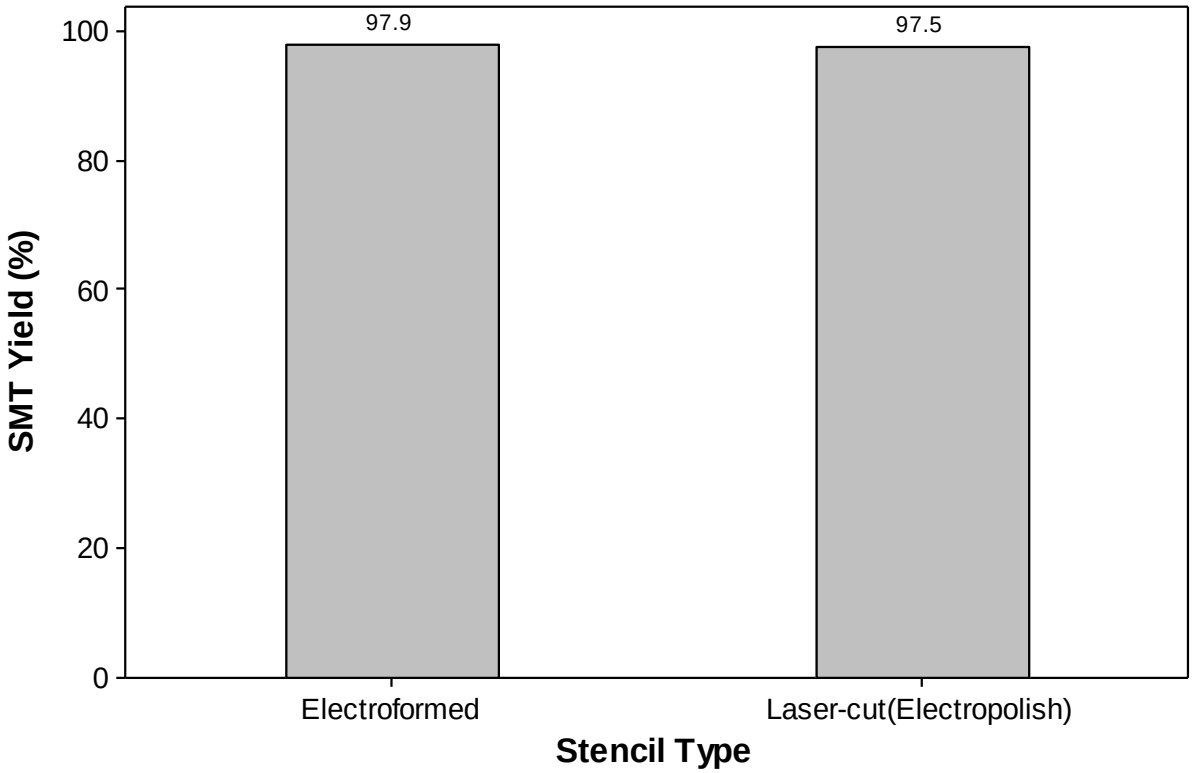
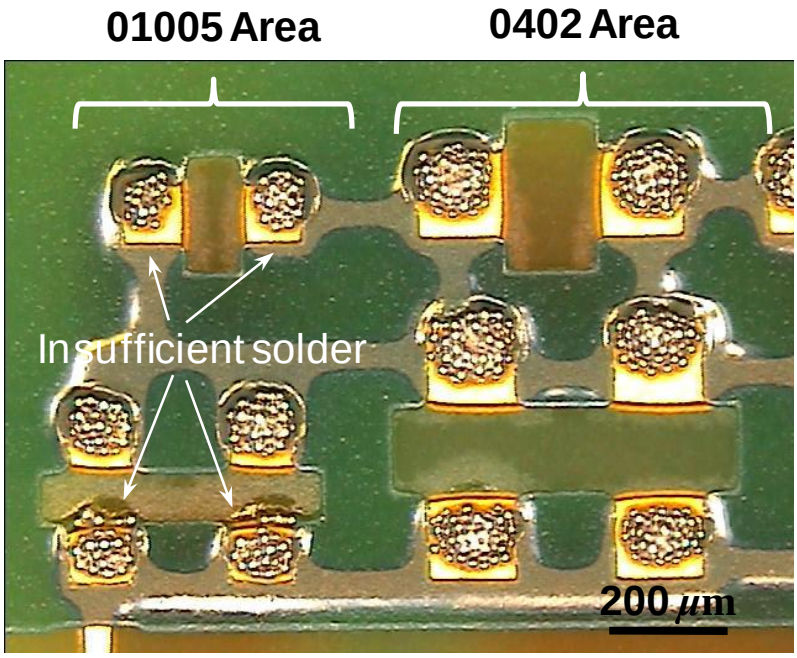
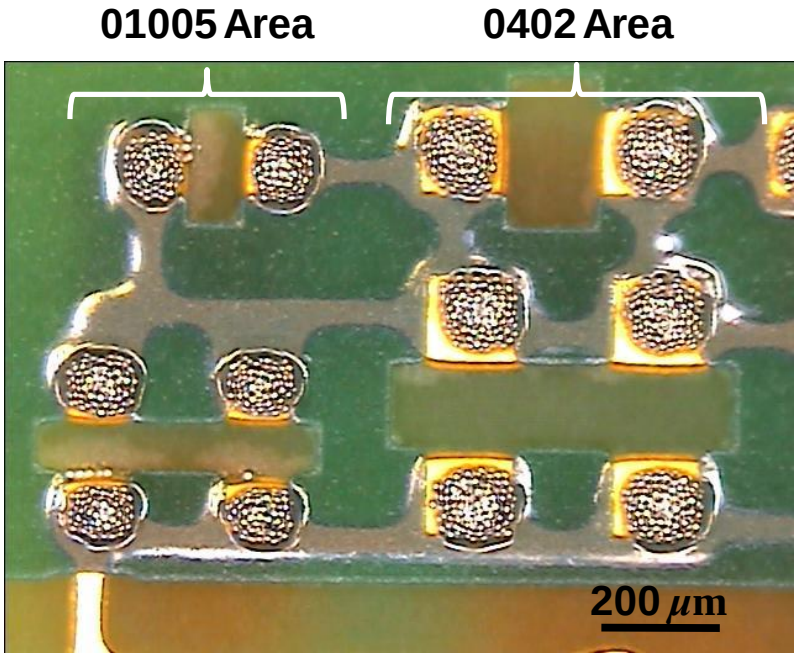


FIGURE 3.8 Yield comparisons on 01005 chip components for each stencil type.



(a)



(b)

FIGURE 3.9 Solder deposition on 01005 pads for each solder paste type.

Notes: (a) Type 3; (b) type 4.

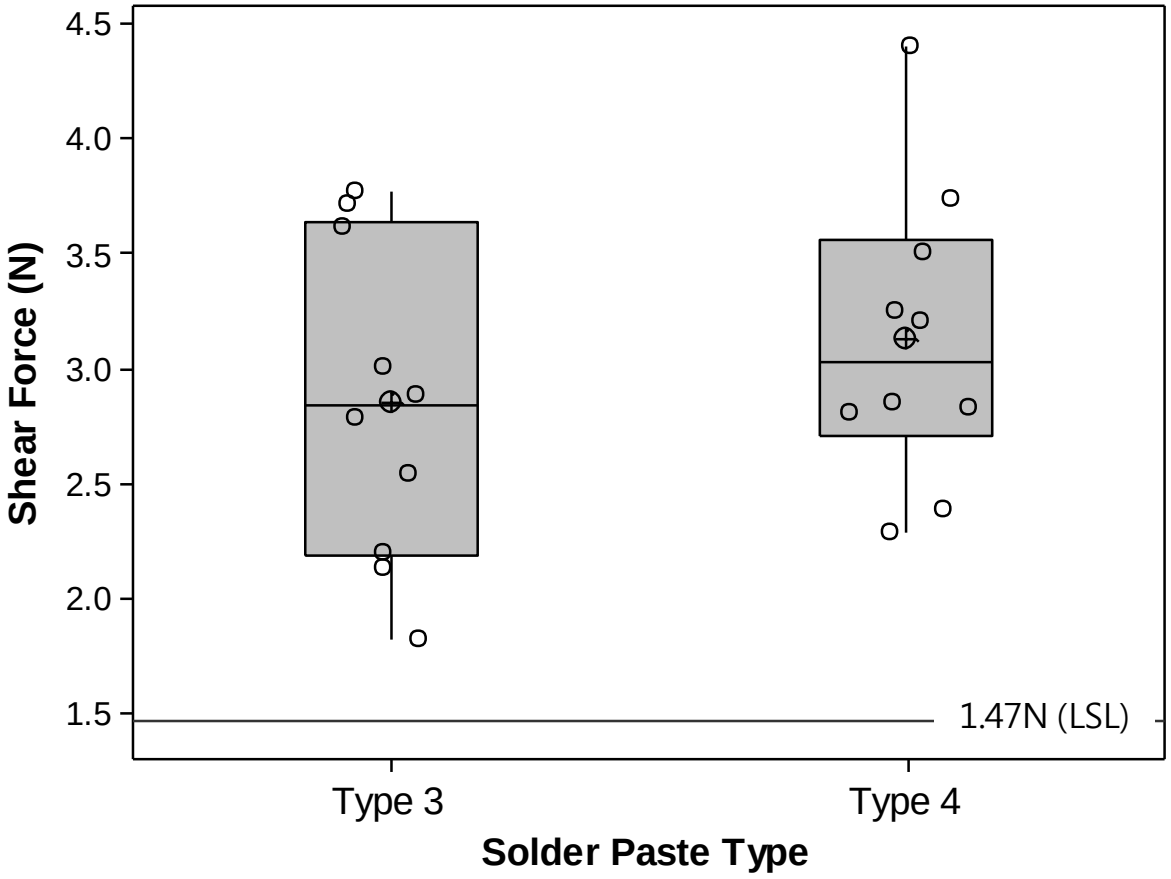


FIGURE 3.10 Shear force comparisons on 01005 chip components for each solder paste type.

Note: The box plot shows the smallest value, the first quartile, the median, the third quartile, and the largest value.

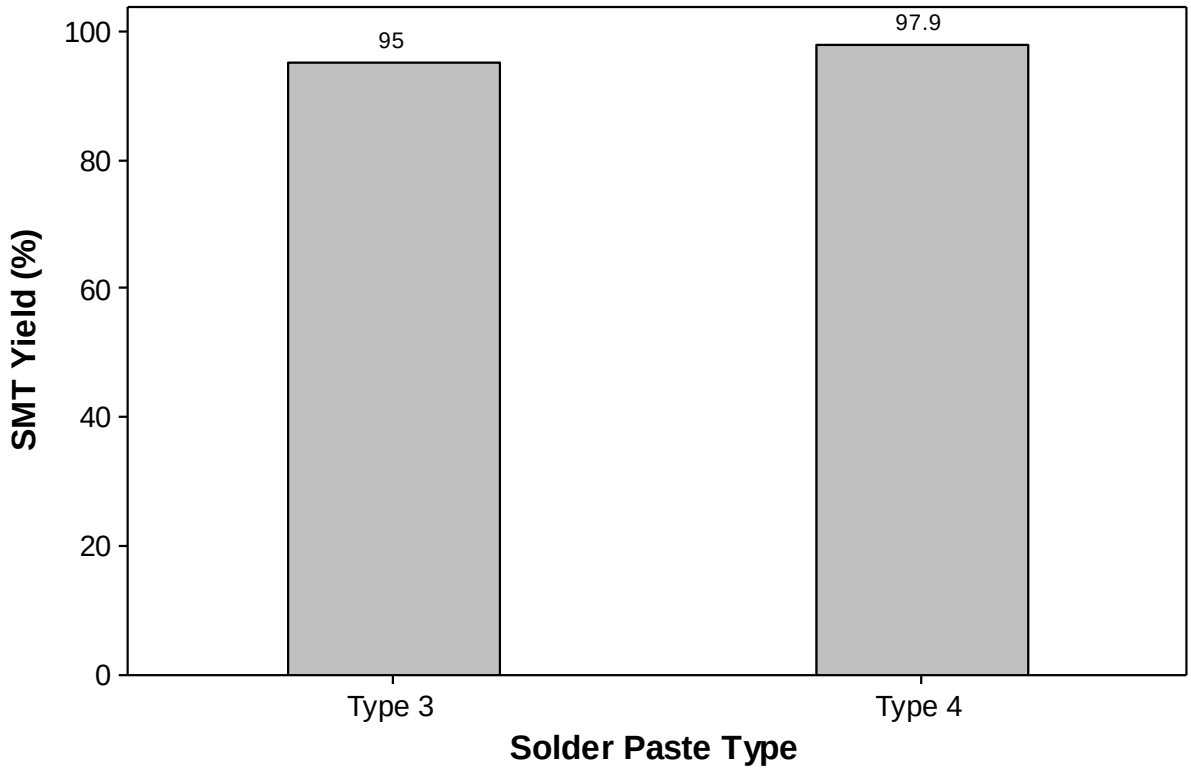


FIGURE 3.11 Yield comparisons on 01005 chip components for each solder paste type.

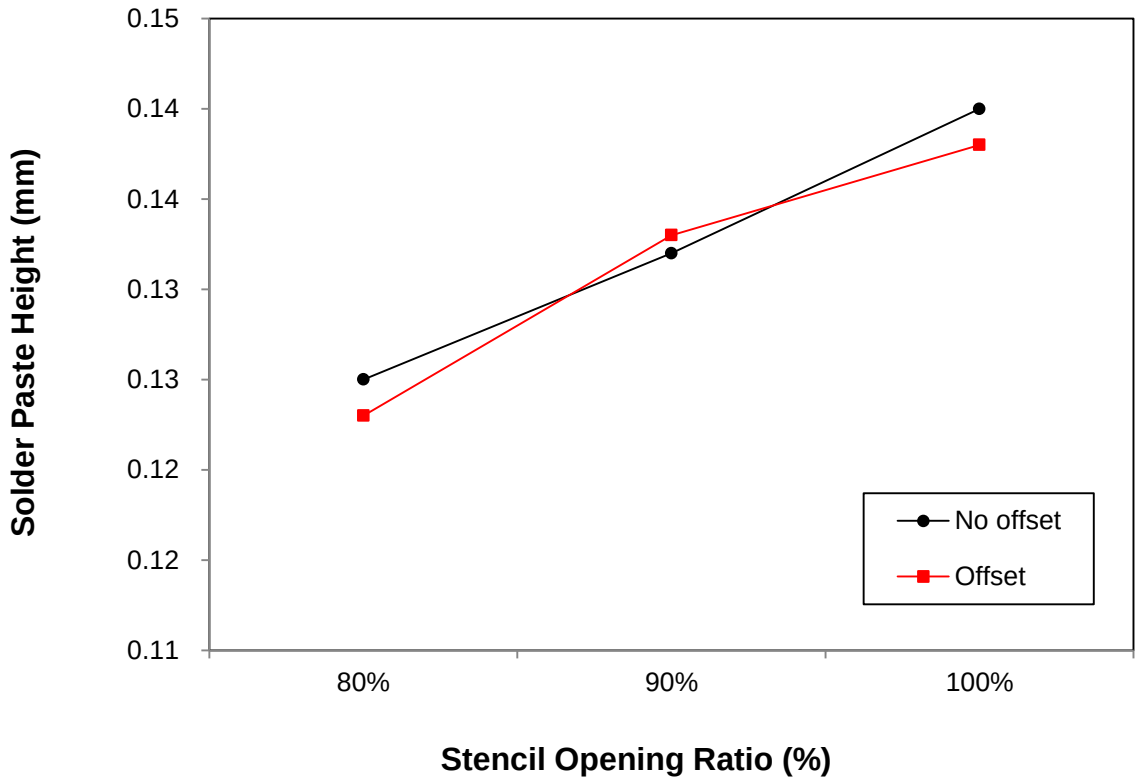
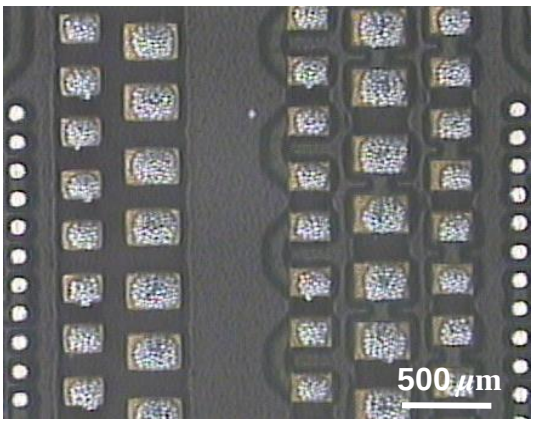
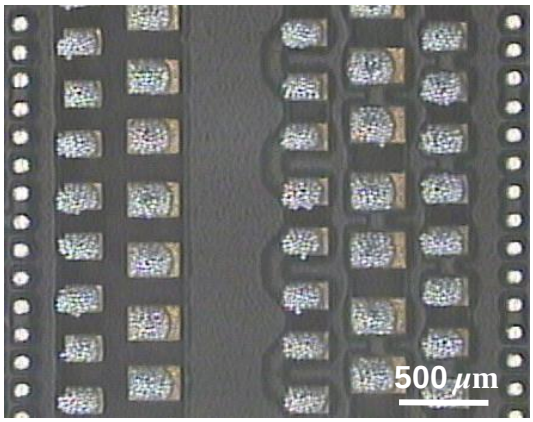


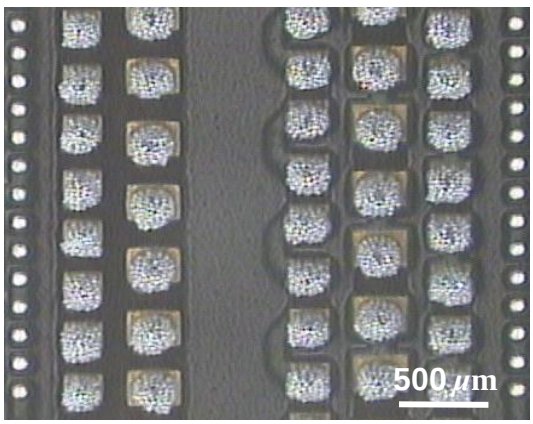
FIGURE 3.12 Solder paste height comparison on 01005 chip components for each stencil opening ratio.



(a)



(b)



(c)

FIGURE 3.13 Solder deposition on 01005 pads with each stencil opening ratio.

Notes: (a) 80 percent; (b) 90 percent; (c) 100 percent.

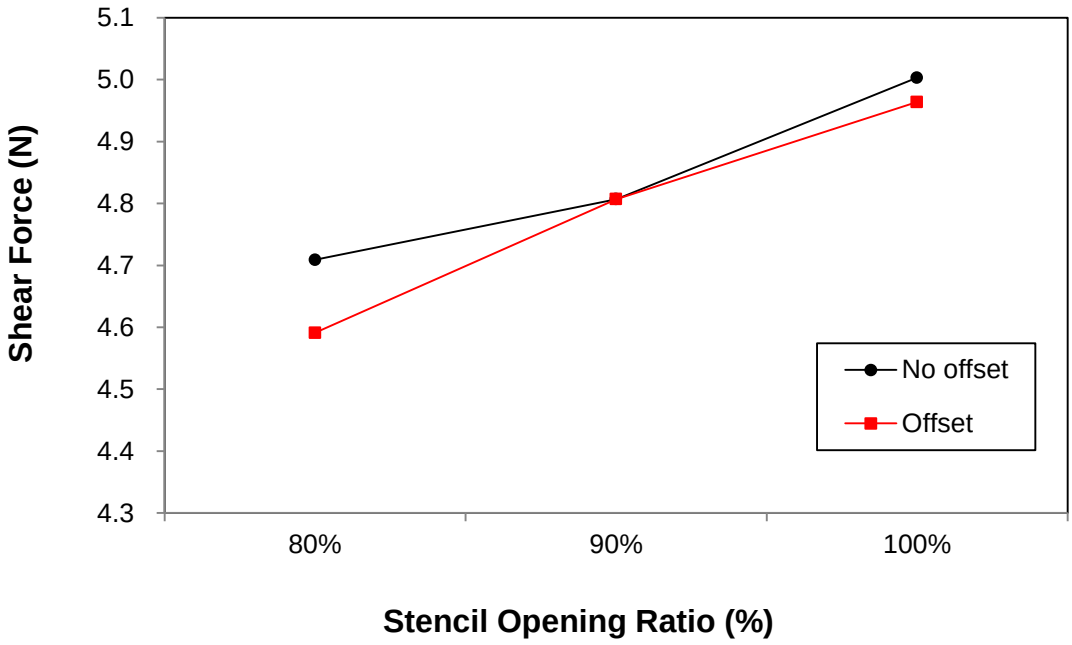


FIGURE 3.14 Shear force comparison on 01005 chip components for each stencil opening ratio.

Additionally, the evaluation was combined with two offset conditions of the solder printer machine to investigate the self-alignment effect for the 01005 chip components. Figure 3.15 shows process yield information for each stencil opening ratio and for the offset conditions. From the graph it can be concluded that the 0 μm offset performed much better than the 100 μm offsets. When print offset equaled zero, the defects were generated 14 and 16 percent, respectively, for 80 and 100 percent stencil opening ratios. No defect was generated for the 90 percent stencil opening ratio, which indicated that this stencil design provided the best self-alignment ability. When print offset equaled 100 μm, an 80 percent stencil opening ratio showed 36 percent defects and stencil opening ratios of 90 percent and 100 percent generated 20 percent defects. The largest solder volume of 100 percent stencil opening offered the most tolerance to print offset and decreased defects rate. The smallest solder volume, with an 80 percent stencil opening ratio, was the most sensitive to print registration on defects.

The study revealed that, generally, as the stencil opening ratio increased the number of defects also decreased and the number of defects that were generated depends upon the solder volume delivered. Additionally, sufficient post-print paste and coverage conditions, such as stencil opening ratios of 90 and 100 percent, performed much better than the stencil opening ratio of 80 percent, even at the 100 μm print offset level.

For the placement of 01005 components, it is important to look at both the pickup and placement of the components. Figure 3.16 compares the pickup rates of a standard camera and a DCA camera for the 01005 components. The pickup rate of the DCA camera was 99.95 percent, and that of the standard camera was 87.08 percent. A comparison of performance between the standard camera and the DCA camera shows that the DCA camera was better in terms of fewer missing components. This result appears to be due to the difference in the resolutions of the two cameras. The DCA camera had a pixel size that was 50 percent smaller and a higher resolution than the standard camera.

Figure 3.17 shows the defect rates of the two cameras after the reflow process. The standard camera, with a lower resolution, produced four times more defects than the DCA camera. With regard to defect modes, the misalignment and tombstoning of the standard camera were 7.1 and 1.3 percent, respectively, whereas those of the DCA camera were 1.7 and 0.4 percent, respectively. The higher the placement accuracy, the lower the defect rate became and

the DCA camera, with better resolution, showed a lower defect rate than did the standard camera.

The vacuum nozzle is another factor that has a great effect on the pickup reliability of components. In this study, the component pickup rates of 906 and 926 nozzles, with different nozzle shapes, were compared. The results are shown in Figure 3.18. The pickup rate of the 906 nozzle was 99.76 percent, whereas the 926 nozzle was slightly higher at 99.94 percent.

Figure 3.19 shows the defect rates of the two nozzles after the reflow process. As shown in this graph, the 906 nozzle had a high-defect rate of 37.3 percent, whereas the 926 nozzle had a defect rate of 7.3 percent. The reason for this result appears to be that the vacuum hole size of the 926 nozzle is smaller than that of the 906 nozzle and, thus, has a better component adsorption property.

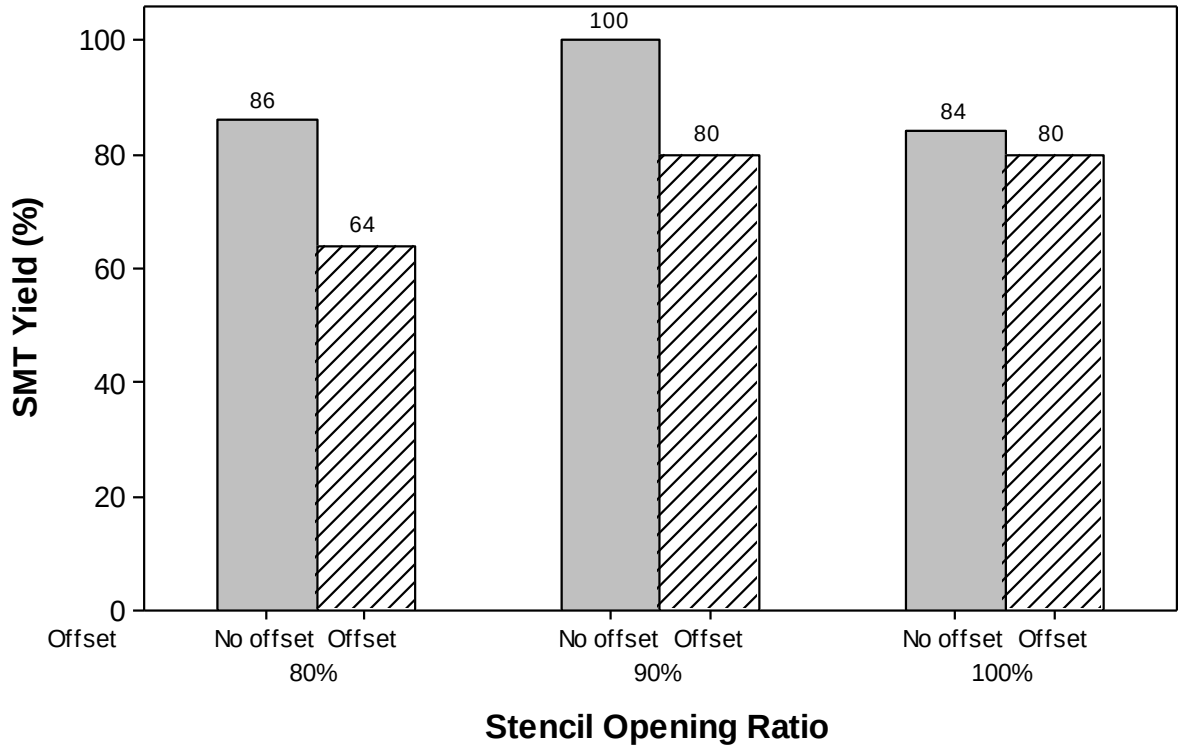


FIGURE 3.15 Yield comparisons on 01005 chip components for each stencil opening ratio.

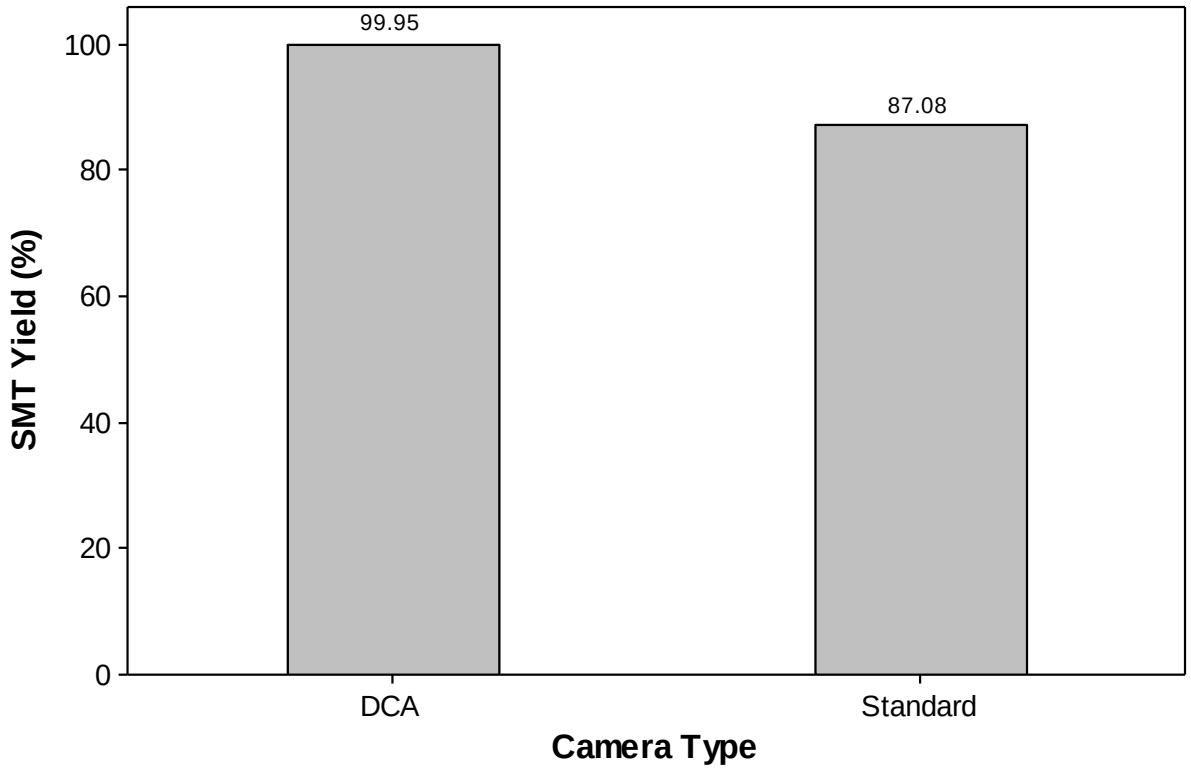


FIGURE 3.16 Pickup rate comparisons on 01005 chip components for each camera type.

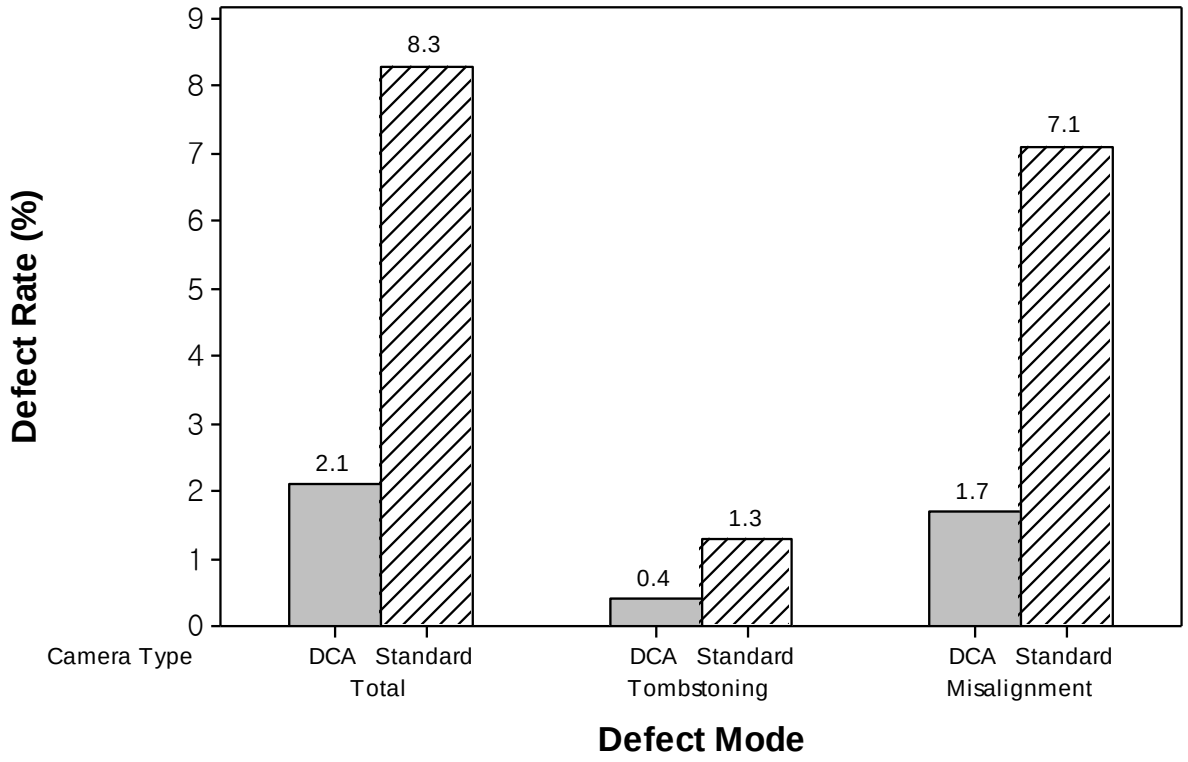


FIGURE 3.17 Defect rate comparisons on 01005 chip components for each camera type.

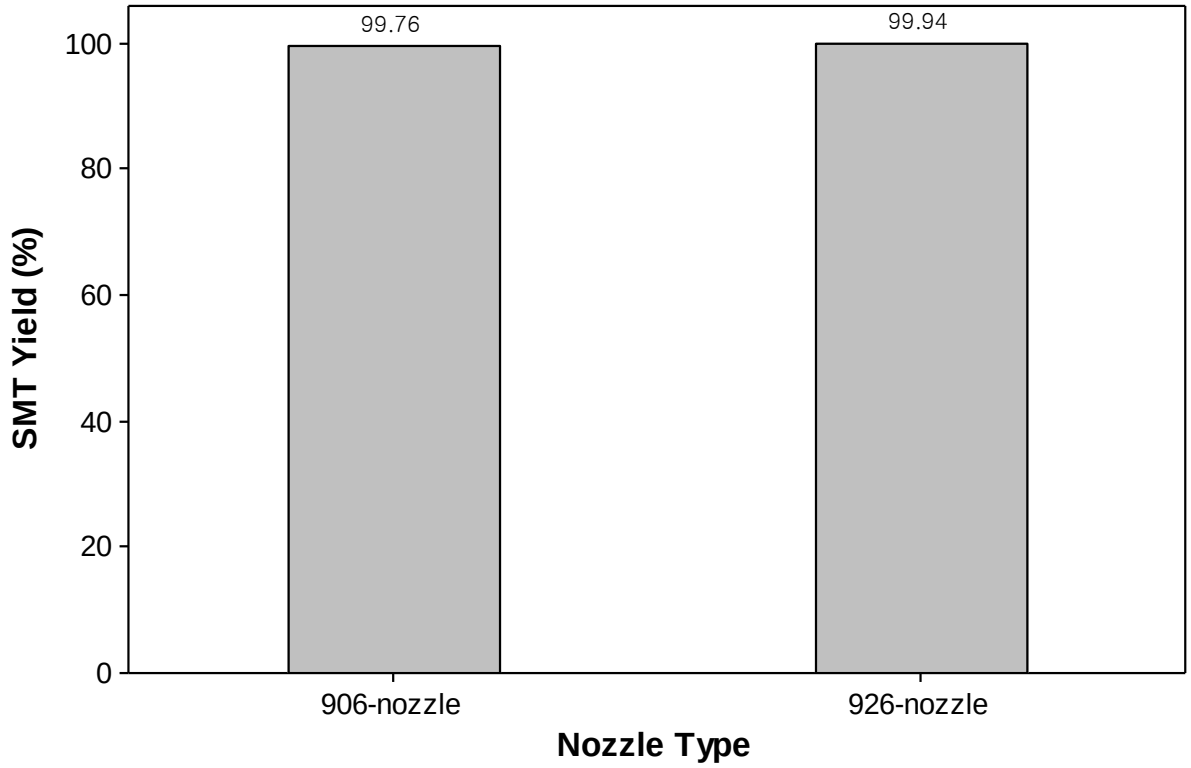


FIGURE 3.18 Pickup rate comparisons on 01005 chip components for each nozzle type.

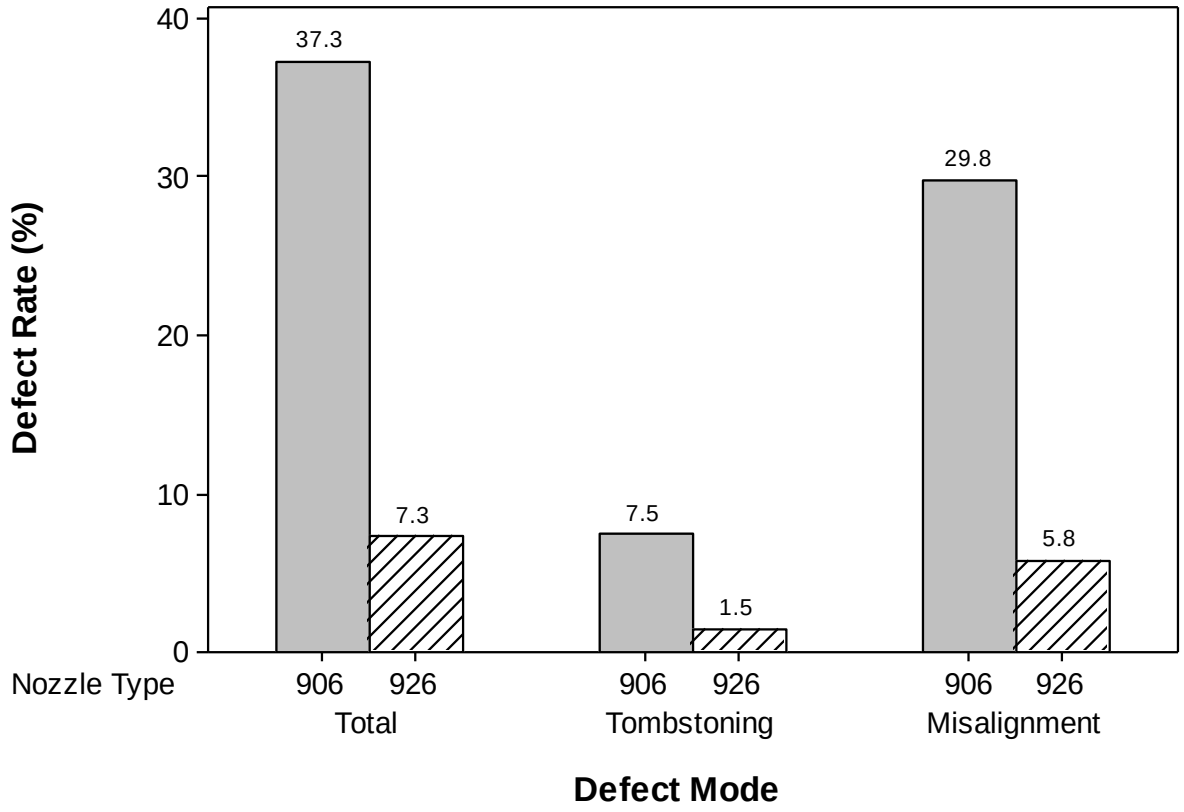


FIGURE 3.19 Defect rate comparisons on 01005 chip components for each nozzle type.

3.3.2 Reliability results

The temperature cycle dependence of shear strength is shown in Figure 3.20. The 0201 components were also shear tested as a benchmark. After 500 cycles, the shear strengths decreased 14 and 23 percent, respectively, for the 0201 and the 01005 components. After 1,000 cycles, the decrease was 17 and 22 percent, respectively, and after 1,500 cycles, the decrease was further amplified to 22 percent and 32 percent, respectively. Basically, the reduction in shear strength also follows an approximately linear relationship with the number of cycles.

Meanwhile, as the temperature cycle progressed, the fall rate of the shear strength of the 01005 components was greater than that of the 0201 components. Furthermore, after 500 cycles, the shear force of the 01005 components did not even reach LSL 1.47 N. The reason for this is that the 01005 components are very small, compared to the general components, and they have a weak bonding strength. Therefore, the stabilization of the assembly process is very important in order to achieve high reliability for the 01005 components.

Cross-sections of the 01005 components were performed after each cycle. No cracks were observed due to temperature cycling. Figure 3.21 shows the cross-sections of the 01005 capacitor components for each of the temperature cycles. The solder joints showed severe microstructures damage with increasing temperature cycling. Grain coarsening was also observed in the cross-sections due to temperature cycling as shown in Figure 3.22.

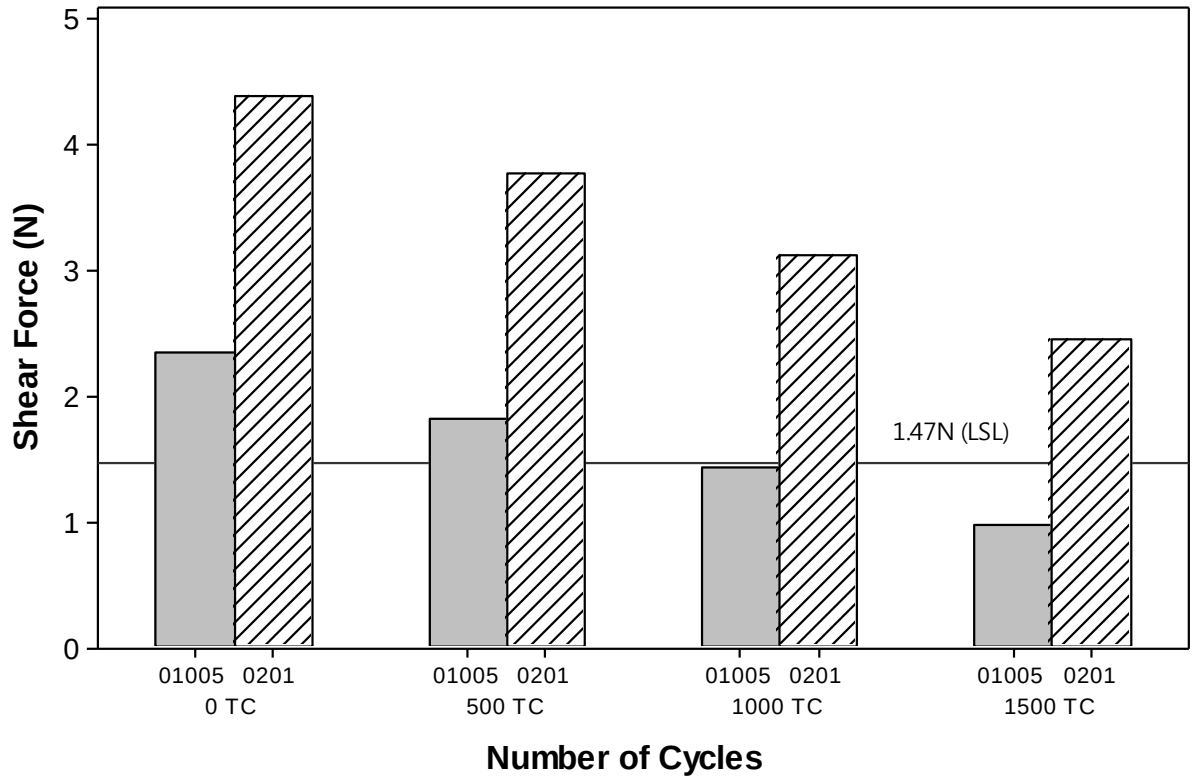


FIGURE 3.20 Shear strength after temperature cycling test.

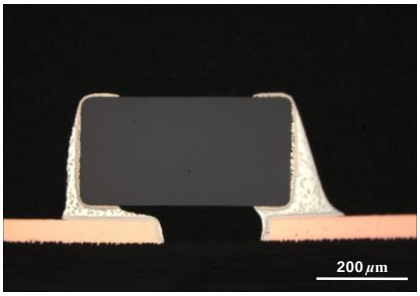
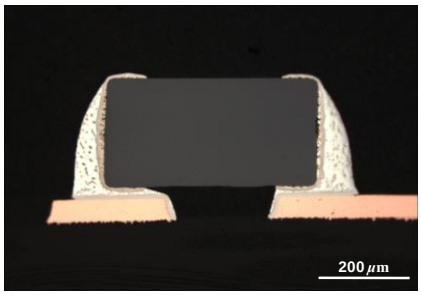
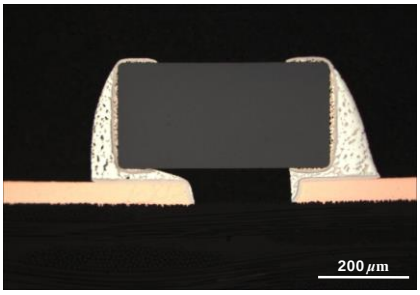
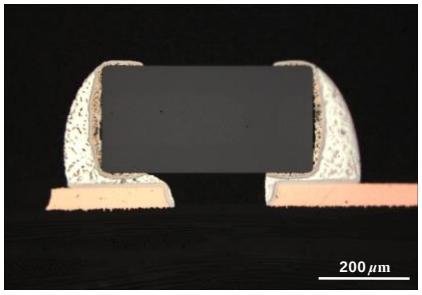
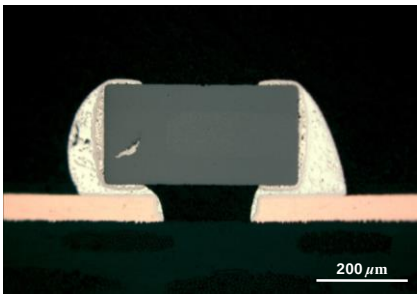
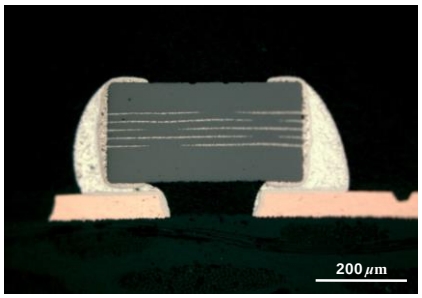
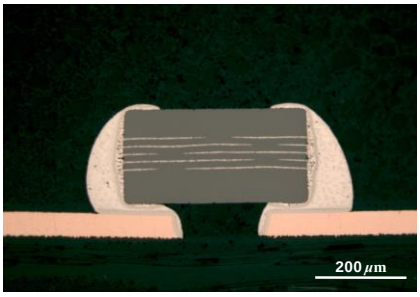
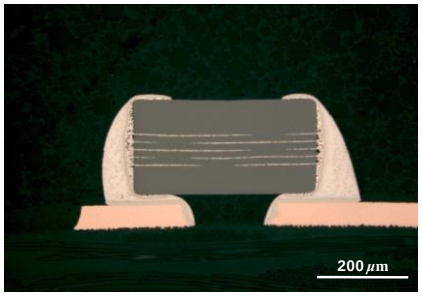
Temperature Cycle	Capacitor	Resistor
0 cycle		
500 cycle		
1,000 cycle		
1,500 cycle		

FIGURE 3.21 Cross-sections of the 01005 chip components for each temperature cycle.

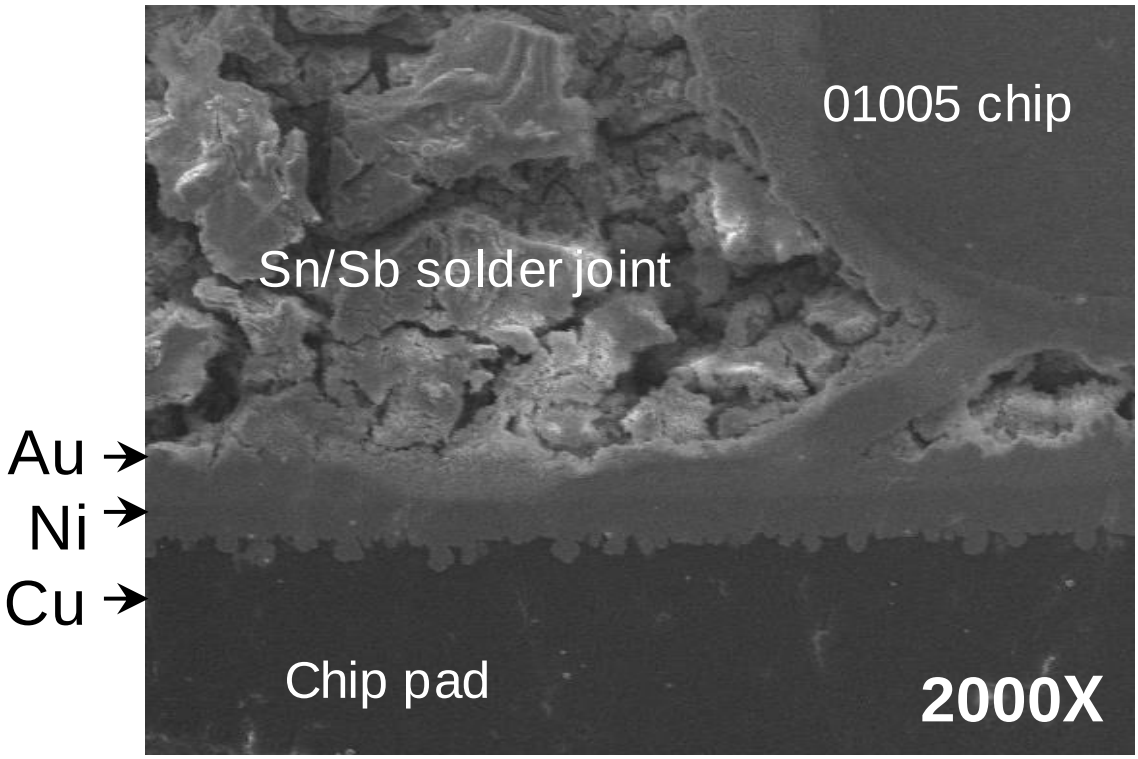


FIGURE 3.22 Cross-section of the 01005 chip components after 1,500 temperature cycles.

3.4 Summary

In this chapter, the results of experimental study provide the operating process window for assembling lead-free 01005 packages. For the stencil fabricating techniques, both electroformed and electropolished laser-cut stencils have a comparable print quality that is solder volume delivered to the pads, but the shear strength in the electroformed stencil is somewhat higher than it is in the electropolished laser-cut stencil. If an electroformed stencil is used, the type 4 solder paste, with a smaller sphere size, will give a better overall yield and better paste depositions on the pads. Tombstoning and misalignment defects are minimized using this type of solder paste.

A 0.08 mm-thick electroformed stencil with a 90 percent aperture opening was observed to produce good results. Based on the findings and on the observation of zero defects after assembly, this stencil design provided the best self-alignment ability.

Characterizing the performance of the vision camera and the vacuum pickup nozzles, for the 01005 components Pick-and-Place process, both the DCA camera and the 926 nozzle were observed to produce good results in terms of having fewer missing components and a better overall yield.

For the reliability studies, temperature cycle testing of the solder joints showed no failure after 1,500 cycles. However, the shear strength significantly decreased 32 percent after 1,000 cycles.

PART III: ULTRA-FINE PITCH SOLDER STENCIL PRINTING

Chapter 4

The effects of acid electrolytes and electropolishing conditions on the printing performance of the small apertures[2]

In this chapter, the EP process has shown promising results for improving the surface finish of small apertures in laser-cut stencils. I report on the results of the investigations of the parameters that control the EP process using a highly concentrated phosphoric acid. The effect of the phosphoric acid solution on the finish of the polished small apertures and the effect of EP time were investigated. An optimized process was established through inspection of the polished stencil apertures of the laser stencil. The results demonstrated that the acid solution for the electrolyte and EP times had a significant effect on the small stencil's aperture quality and the solder paste's stencil-printing performance. In particular, a 95 wt.% phosphoric acid-based electrolyte showed encouraging results in terms of surface smoothness, improved solder-paste printing and surface mount technology yields.

[2] Based on Yong-Won Lee, Keun-Soo Kim, and Katsuaki Suganuma (2011), "Effects of acid electrolytes and electropolishing conditions on laser-stencil printing performance", *IEEE Transactions on Components and Manufacturing Technology*, Vol.1 No.5, pp. 641– 646.

4.1 Objective and overview

Stencil printing is one of the most important processes in the SMT assembly process. It has been said that 60 percent to 70 percent of the defects encountered in SMT assembly are related in some way to the printing process [28–30]. The various stencil design elements that affect the solder-paste release are the aperture size, aperture shape, aperture wall taper, and wall finish of the apertures [63]. From these, the aperture size and shape is stencil design-related, while the aperture wall taper and aperture wall finish are stencil fabrication technology-related. Stencil fabrication technology plays a major role in the amount of solder paste released from the apertures during stencil printing [27].

In Section 3.3.1 of Chapter 3, I discussed the effect of electropolished laser-cut stencil on small apertures for the assembly of 01005 chip components. The results showed comparable solder paste performance with electroformed stencils when type 4 (38–20 μm) solder paste was used. In this chapter, primarily EP process variable was studied, and potential factors such as electrolyte compositions and EP time, which may affect small apertures' quality and laser-cut stencil printing performance, were investigated. The results will be discussed below, along with recommended optimal conditions.

4.2 Experimental

The solder paste used in this study was a water-soluble 95 wt.%Sn–5 wt.%Sb of type 3 particle size (size range: 45–25 μm), which is widely used in the assembly industry due to its low-cost. The metal content was 90 wt.% and the melting point of the solder was approximately 232–240 °C, as specified by the supplier (Alpha Metal WS609).

The test vehicle used in the work reported in this paper was a four-layer BT board with a nickel/gold finish. The test vehicle contained sixty 8 mm × 8 mm laminate modules, arranged in a 5 × 6 × 2 matrix (Figure 4.1). There was a total of 1,500 locations for 0201 (0603 metric, 0.6 mm × 0.3 mm) components, and 240 locations for 0402 (1005 metric, 1.0 mm × 0.5 mm) components. All solder pads were solder-mask-defined pads on three sides for the 0201 and 0402 components. The pad shapes were also distributed equally in the horizontal and vertical

orientations (Figure 4.2). The pad dimension details are shown in Table 4.1. The test vehicles were assembled for experimental runs using lead-free passive components such as resistors, inductors, and capacitors. The lead-free finish on the component terminal was 100 percent pure tin.

Stencils were produced using standard laser-cut stencil fabrication techniques. In Figure 4.3, the production steps of the laser-cut stencil fabrication process are shown. For the fabrication of the stencils, a matrix of small apertures must be formed in the SUS304 3/4H TA stainless steel sheet. The laser-cutting was carried out using an LPKF Micro-cut F stencil laser-cutting system.

The next step was the EP process. The important process parameters in EP are electrolyte temperature, polishing time, current density, and the electrolyte used. At the beginning of the EP process, the cathode and anode work-piece were electrically connected by the conductive electrolyte that filled the gap between the cathode and anode. The anode was a metallic stencil foil (stainless steel), and the cathode was the stainless steel (SUS304) plate. The electropolish bath consisted of a solution of H_2SO_4 and H_3PO_4 containing water. Most mixtures studied were made without additional water. The EP process parameters are shown in Table 4.2.

TABLE 4.1 Pad dimension in the test vehicle

Components	L (mm)	W (mm)	S (mm)
0201	0.30	0.36	0.22
0402	0.45	0.56	0.38

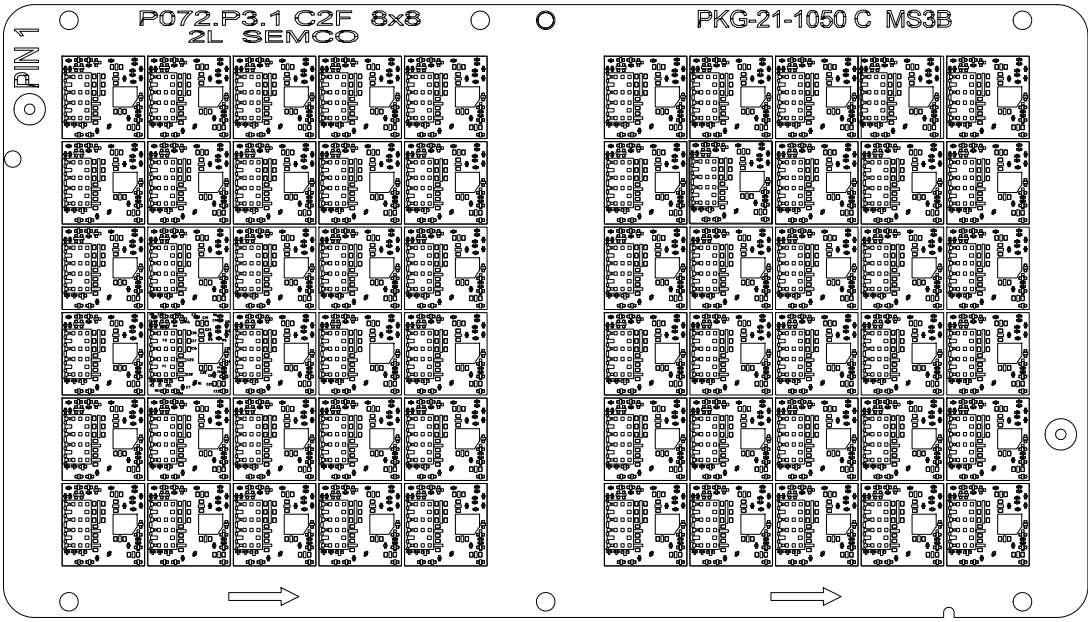


FIGURE 4.1 Schematic diagram of the topside of board on the test vehicle.

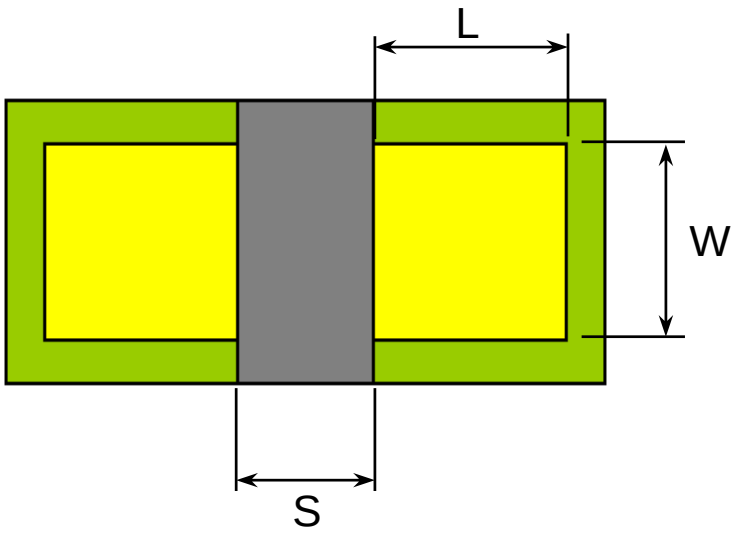


FIGURE 4.2 Schematic of component pad design.

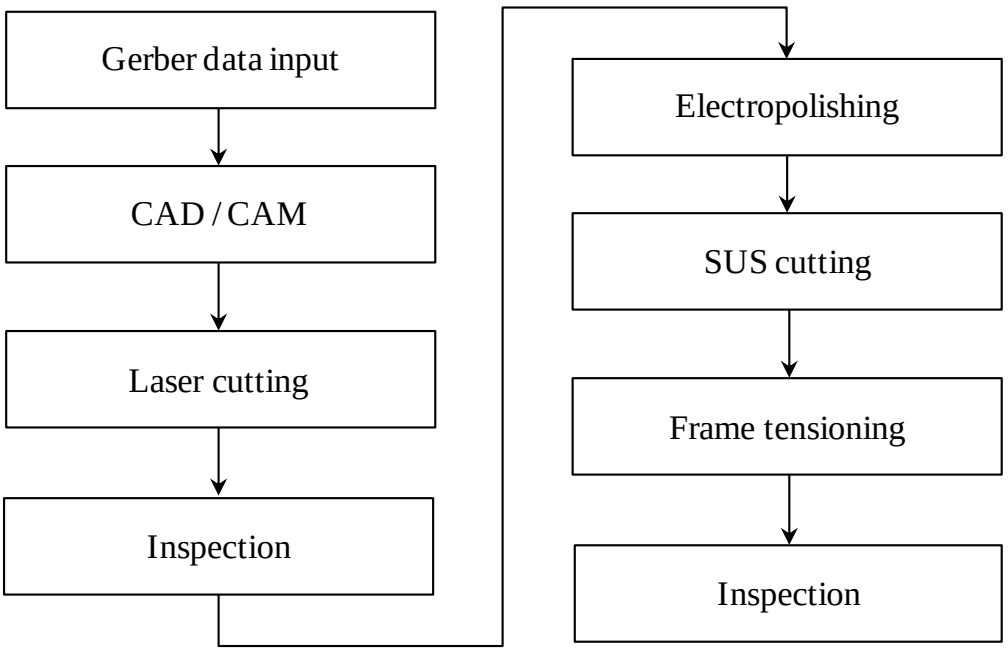


FIGURE 4.3 Manufacturing steps of the laser-cut stencil.

TABLE 4.2 Parameters of EP

Items	Parameters
Power output (DC)	380
Current (mA)	400 – 500
Voltage (V)	13
Temperature (°C)	40 – 50
EP time (s)	0 - 20
Electrolyte	H_3PO_4 : H_2SO_4
Electrode gap (mm)	175
Tool material	SUS304 stainless steel

A complete stencil consists of a square rigid frame to which the stencil is attached. The frame design is specific to the printer to be used, and is most commonly fabricated from square aluminum tubing for the optimum combination of rigidity and lightness, although cast aluminum frames are used in small printers. The frame size used was 736 mm × 736 mm, and the metal stencil was 530 mm × 530 mm. Tensioning was required to ensure a taut and flat surface. A summary of the laser-cut stencil fabrication process used for these experiments is shown in Table 4.3. The apertures obtained were inspected using a SEM (JEOL JEM-2000).

The screen-printing process was carried out using an MPM AP Excel printer (Speedline Technologies, Inc.) with metal squeegees angled at 60°. The stencil was cleaned before each use. The stencil was placed on the PCB substrate and, after vision alignment, a squeegee traveled at a certain pressure and speed to push the solder paste through the stencil apertures. The following stencil printing parameters were used for all stencil printing: print speed = 8 mm/sec; print force = 5.3 kg; balance = 50:50 and print gap = 0 mm. The solder paste deposits were inspected in a microscope equipped with a digital camera and documented photographically. After measurements of the solder paste thickness on the pads, the components were placed and soldered in a reflow oven with nitrogen atmosphere. Table 4.4 provides details pertaining to the oven profile for this experiment, and the actual profile used is shown in Figure 4.4.

All boards were visually inspected using a stereoscopic microscope (Olympus SMT 6). Shear testing of the 0201 chip component was also performed using a Dage 4000 bond tester. All shear testing was conducted at room temperature with a shear height of 50 μm and a pulling speed of 200 μm/s.

To investigate the EP characteristics of the small apertures of laser-cut stencils, an experiment was designed and conducted using the various factors and levels shown in Table 4.5. The first part of this paper focused on the effect of the acid electrolyte bath conditions on the smoothness of the aperture walls and solder paste printing performance. Two EP phosphoric-sulfuric acid solutions were tested: 85 wt.% and 95 wt.%. The bath was prepared by adding sulfuric acid to the phosphoric acid slowly and mixing the solution thoroughly. The aperture shape was the same as the pad shape, while the ratio of aperture to pad size was 80 percent. In this experimental run, 0.1-mm-thick laser-cut stencils were used. The other SMT process parameters were kept constant for all the experimental runs. The response variable used for the

qualitative analysis for both acid solutions was the smoothness of the aperture wall. The quantitative response variables were the printed solder paste thickness, shear force, and SMT yield in parts per million (ppm). The experimental data was analyzed using the Minitab data statistical software.

The second part of the paper examined the effect of the EP time on the surface smoothness of the small apertures in various thicknesses of laser-cut stencils. To compare the effect of EP time, 25 stainless steel sheets were tested with various EP times, from 5 s to 20 s, for three stencil thicknesses: 0.05, 0.08, and 0.10 mm. All 75 laser-cut stencils were cut on the same laser cutter with the same setup parameters.

TABLE 4.3 Laser-cut stencil fabrication parameters

Items	Parameters
Laser system model	LPKF Micro-cut F
Laser type	YAG
Laser beam size (*μ*m)	20
Laser diameter (*μ*m)	30–35
Machine accuracy (*μ*m)	±5
Stencil frame tension (mm)	0.55–0.70

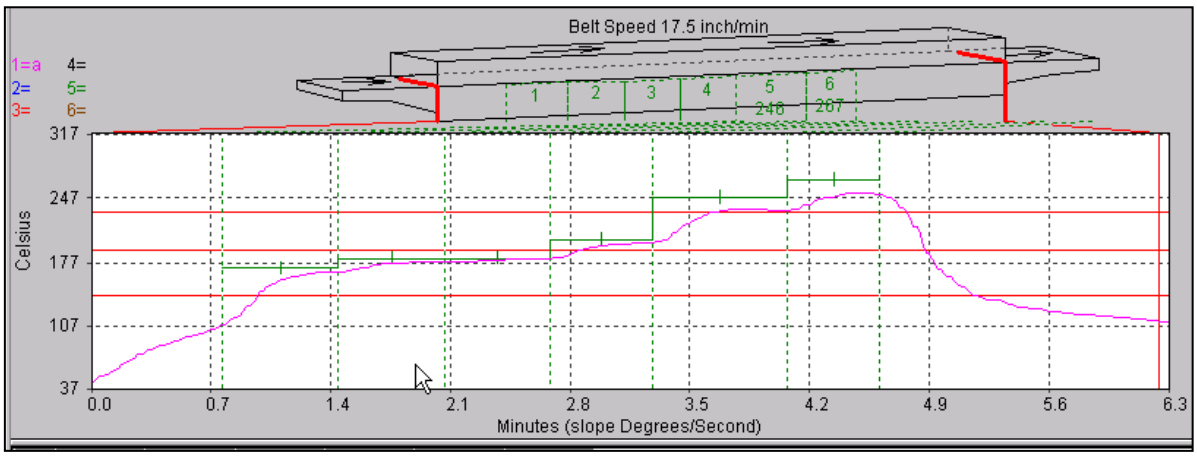


FIGURE 4.4 Reflow actual profile for experiment run.

TABLE 4.4 Reflow process parameters

Peak temperature	Total time between 190/232 °C	Total time above 232 °C
251.2 °C	53.97 s	66.41 s

TABLE 4.5 Factors for experiments

Factors	**Levels**			
Acid solution (wt.%)	85		95	
Stencil thickness (mm)	0.05	0.08	0.10	
EP time (s)	0	5	10	20

4.3 Results and discussion

4.3.1 The effect of the acid solution as electrolyte

The surface finish of the aperture walls of a laser stencil has a significant effect on the solder paste release performance, and stencils that have been electropolished have smoother inside aperture walls than a non-electropolished stencil [68, 71]. The effect of the phosphoric acid solution on the quality of the stencil aperture's surface polish was investigated. The electric current used for the EP was 400 mA, the temperature of the electrolyte was 40 °C, the electrode gap was 175 mm, and the EP time was 20 s.

Figure 4.5 shows the SEM images of the aperture walls in the laser-cut stencil made after EP. Two stencil coupons were treated with EP for 20 s, the only difference between them being the percentage of phosphoric acid in the electrolyte solution. After EP process, the two differently treated apertures were examined by the SEM. As shown in the images in Figure 4.5, surface waviness is clearly seen in both electrolyte types due to excessive EP. However, when a 95 wt.% phosphoric acid solution was used, the aperture wall was smoother than when a 85 wt.% phosphoric acid solution was used.

The solder paste printing performances resulting from each acid solution were characterized and evaluated using several methods of data analysis. The first method used was capability analysis, which is a method used to determine whether a process is meeting the specification limits and producing good parts. Capability is determined by comparing the width of the specification limits with the width of the process variation. The measure of this is called the process capability index, or *Cpk*. Values greater than 1.0 are acceptable, and 1.33 is a common target [107]. Typically, in electronics assembly, a process is deemed capable if this ratio is 1.67 or greater [108]. *Cpk* is defined as

$$Cpk = \min\left(\frac{\mu - LSL}{3\sigma}, \frac{USL - \mu}{3\sigma}\right)$$

where *LSL* is lower specification limit, μ is the mean, *USL* is the upper specification limit, and σ is the standard deviation of the process. Figure 4.6 shows capability plots generated by each acid solution treatment. The target value was a solder paste thickness of 0.113 mm, with an *LSL* of

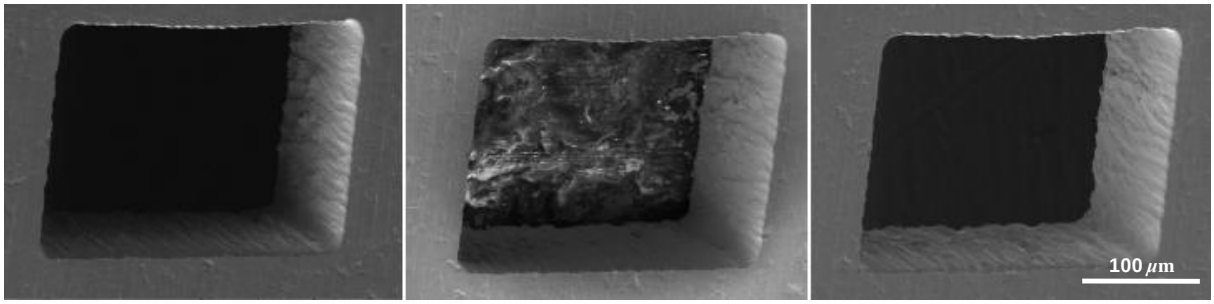
0.076 mm and a *USL* of 0.150 mm. The solder paste thickness (*Cpk*) was 1.18 for the 85 wt.% phosphoric solution and 1.35 for the 95 wt.% phosphoric solution. The mean performance of the 85 wt.% phosphoric solution shifted, and its *Cpk* value was slightly smaller than that of the 95 wt.% phosphoric solution. The cause of this performance difference was the difference in the aperture wall quality, with the aperture wall smoothness with 85 wt.% phosphoric solution being much less than that resulting from the 95 wt.% phosphoric solution (Figure 4.5).

A box plot of the solder paste thickness versus each acid solution is shown in Figure 4.7. The box plot reveals that the mean thickness of solder paste in the 95 wt.% phosphoric acid condition was higher than that of the 85 wt.% phosphoric acid condition. It was necessary to determine whether the difference observed was statistically significant. This was done using the two-sample *t*-test results shown in Table 4.6. The results show that the *p*-value was 0.039 for each acid solution condition. This value of the two-sample *t*-test indicates that the solder paste thicknesses resulting from the two phosphoric acid solutions were statistically different (*p*-value < 0.05).

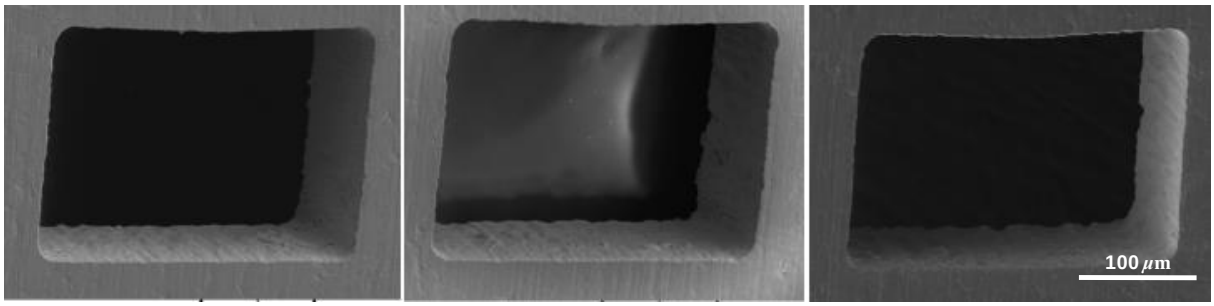
Figure 4.8 is a box plot of the component shear force versus the phosphoric acid solution. Table 4.7 shows the results of the two-sample *t*-test for shear force comparison. From the statistical result, it can be observed that two acid solution conditions were not statically different (*p*-value > 0.05). However, it can be seen that the 95 wt.% phosphoric acid solution has the standard deviation of a distribution of means is smaller than that for the 85 wt.% phosphoric acid solution from the box plot.

Defect rates for each bath condition were recorded. One important measurement of performance was the number of defective parts produced per million. The most common types of assembly defects that are observed were tombstoning, insufficient solder, and misalignment. Tombstoning defects are caused by differences in the initial wetting of the joints of a component by the solder during soldering. They are mainly due to unequal amounts of printed solder paste on the pads. Tombstoning and insufficient solder were the focus of this paper.

The 85 wt.% phosphoric solution exhibited a defect rate of 1,643 and 381 ppm, while the 95 wt.% phosphoric solution exhibited defect rates of 1,039 ppm and 289 ppm for tombstoning and insufficient solder, respectively. The total defect rates were 2,050 and 1,394 ppm for the 85 wt.% phosphoric and 95 wt.% phosphoric solutions, respectively.



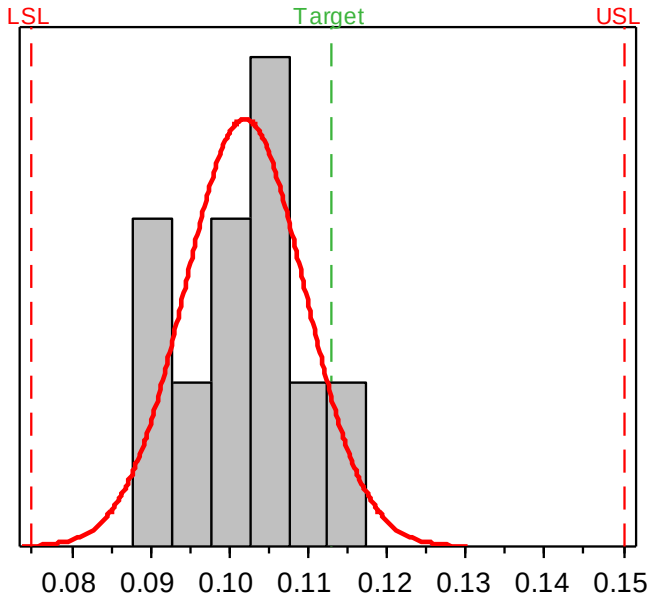
(a)



(b)

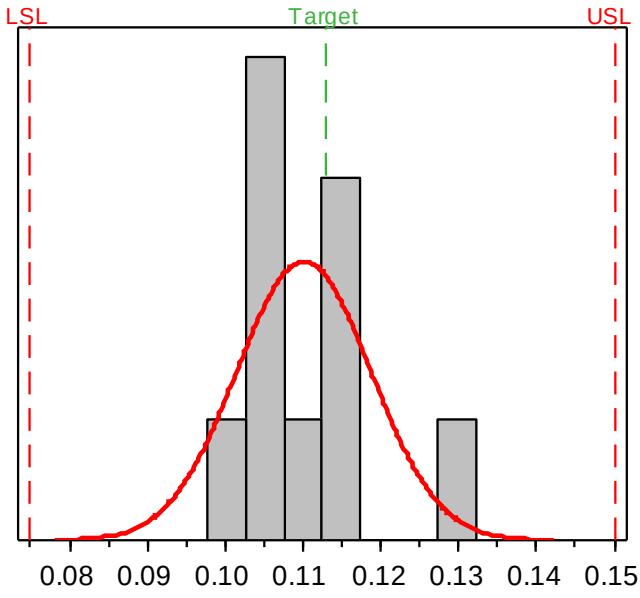
FIGURE 4.5 SEM pictures taken from electropolished laser-cut stencils.

Notes: (a) 85 wt.% phosphoric acid solution; (b) 95 wt.% of phosphoric acid solutions.



MEAN = 0.10188, STDEV = 0.00762, *Cpk* = 1.18

(a)



MEAN = 0.1106, STDEV = 0.00866, *Cpk* = 1.35

(b)

FIGURE 4.6 Process capability plot of (a) 85 wt.% of phosphoric acid solution and (b) 95 wt.% of phosphoric acid solution.

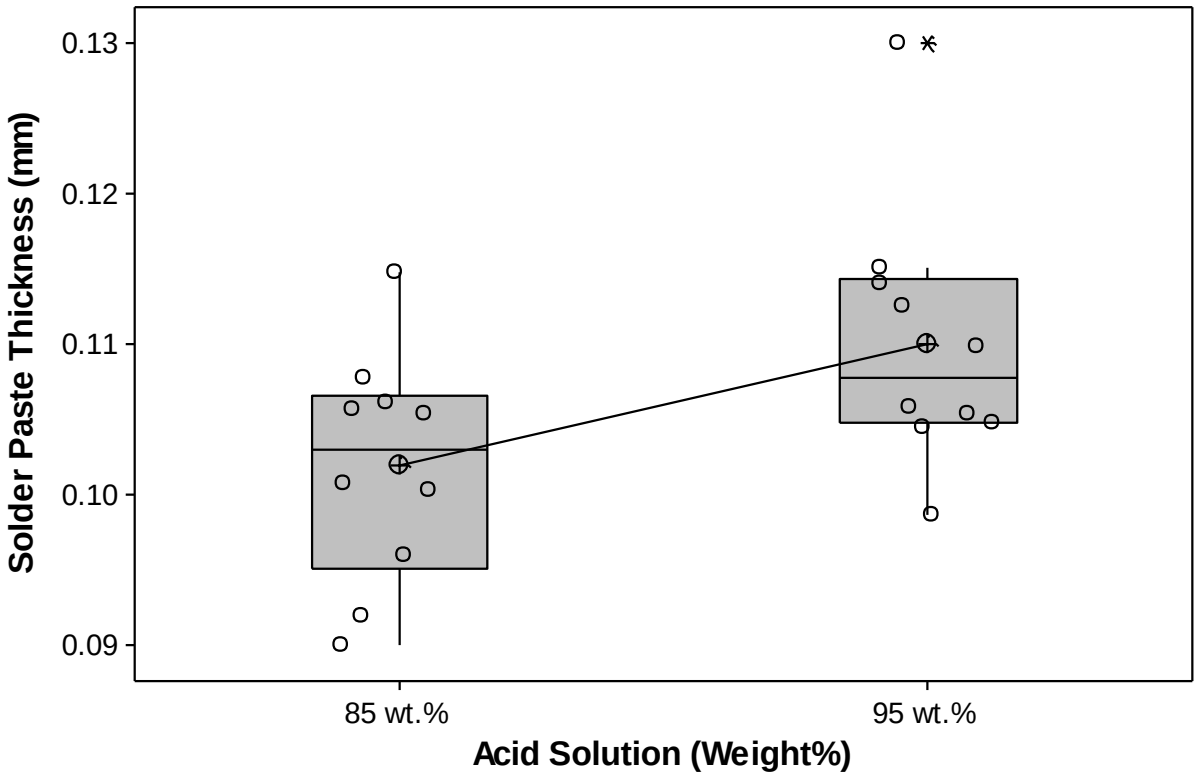


FIGURE 4.7 Solder paste thickness measurement results for two phosphoric acid solutions.

Note: The box plot showing the smallest value, the first quartile, the median, the third quartile, the largest value, and the outlier.

TABLE 4.6 Two-sample *t*-test results for solder paste thickness

Acid solution	*n*	Mean	SD	SE mean	*p*-value
85 wt.%	10	0.10188	0.00762	0.0024	0.039 ($p < 0.05$)
95 wt.%	10	0.11006	0.00866	0.0027	

Notes: SD - standard deviation; SE mean - standard error mean

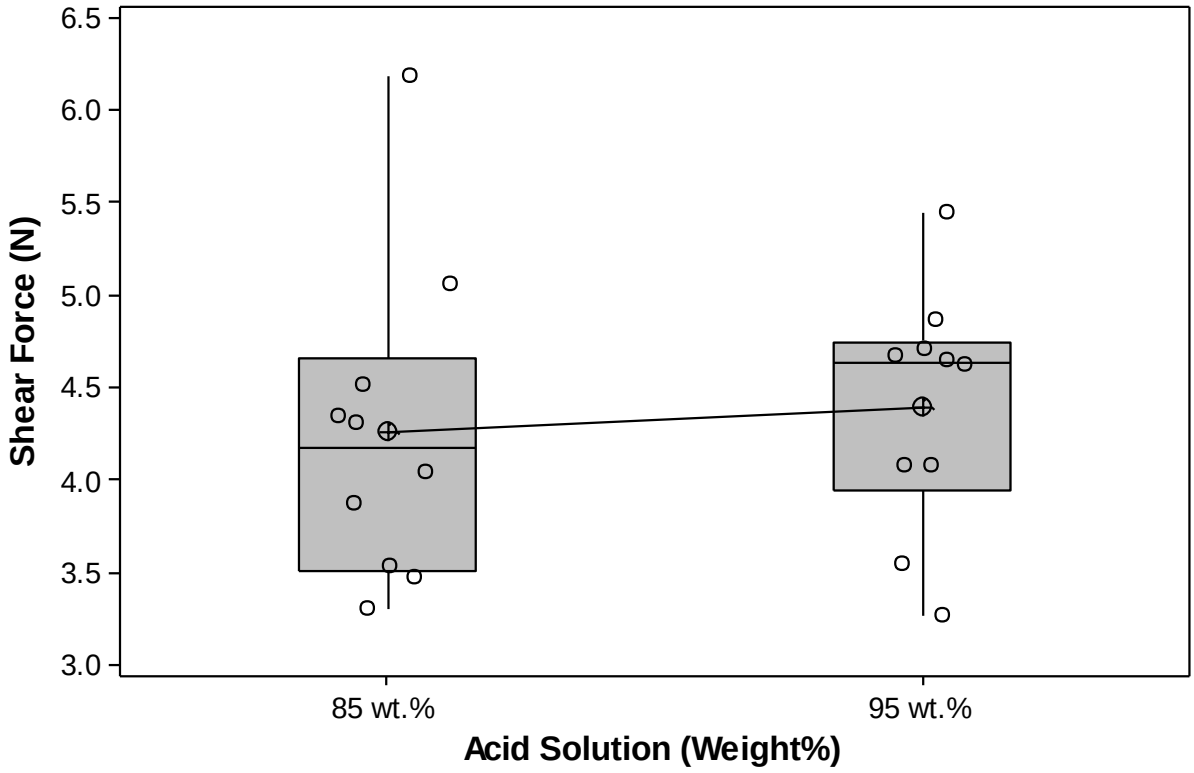


FIGURE 4.8 Component shear test results for each acid solution.

Note: The box plot showing the smallest value, the first quartile, the median, the third quartile, and the largest value.

TABLE 4.7 Two-sample *t*-test results for shear force

Acid solution	*n*	Mean	SD	SE mean	*p*-value
85 wt.%	10	4.262	0.862	0.27	0.704 ($p > 0.05$)
95 wt.%	10	4.394	0.649	0.21	

Notes: SD - standard deviation; SE mean - standard error mean

The total defect rates were 2,050 and 1,394 ppm for the 85 wt.% phosphoric and 95 wt.% phosphoric solutions, respectively. The dramatic drop in all defect rates is shown in Figure 4.9. The 95 wt.% phosphoric solution with 1,394 ppm defects gives a defect rate of 0.1%. This represented a 32 percent decrease from 85 wt.% phosphoric solution rate of 2,050 ppm. It was noted that the overall solder paste print quality produced by laser-cut stencils treated in the 95 wt.% phosphoric solution was superior to that of stencil treated in 85 wt.% phosphoric solution. Based on the above results; it was decided to use the 95 wt.% phosphoric solution for further study.

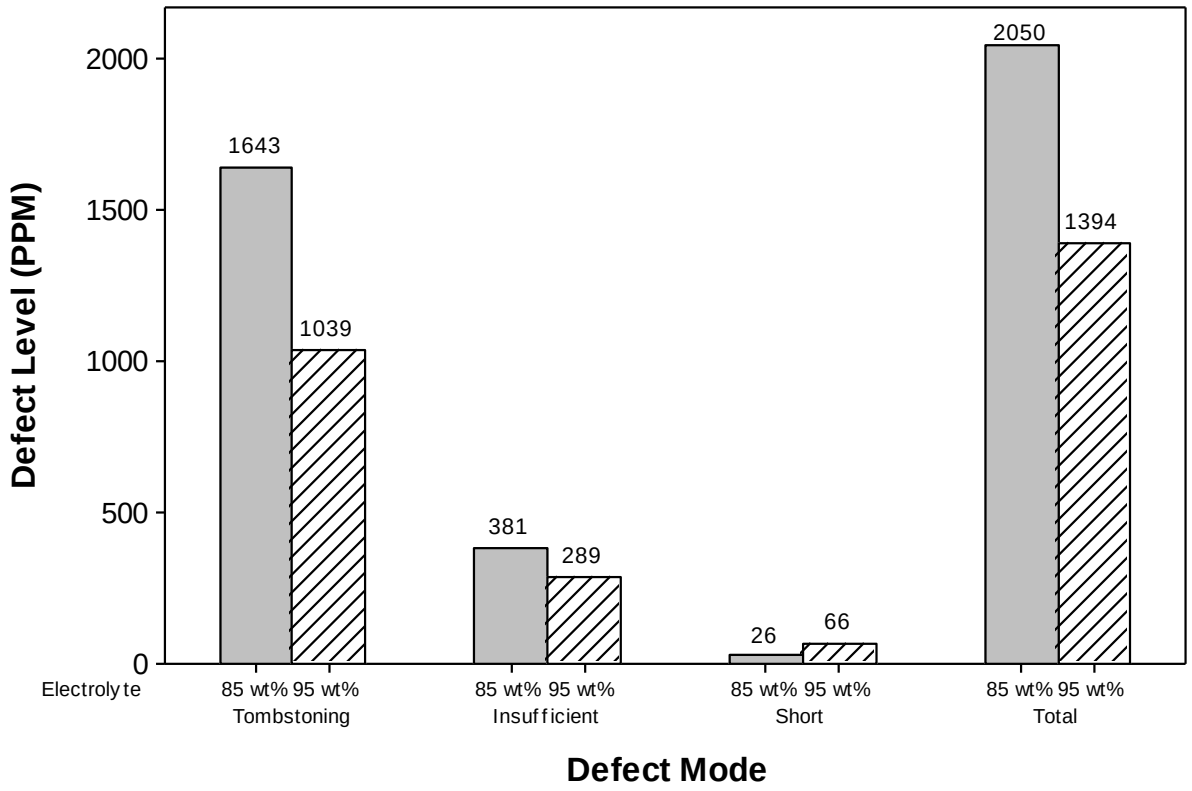


FIGURE 4.9 Total number of SMT defects by two phosphoric acid solutions.

4.3.2 The effect of EP time

For comparison, we also investigated the EP on stencil apertures using the 95 wt.% phosphoric solution. Figure 4.10 shows the SEM images of the apertures surfaces for various stencil thicknesses and EP times. The electric current used for the EP was 400 mA. The electrolyte temperature was 40 °C, and the electrode gap was 175 mm. The samples were electropolished for 5, 10, 15, or 20 s. In the case of the 0.05-mm-thick laser-cut stencil [Figure 4.10 (a)], the surface gloss and roughness of the aperture generally showed an improvement as the processing time increased. The surface quality rapidly improved at around 5 s, and the surface roughness was improved after 5 s but not significantly.

The 0.08-mm-thick laser-cut stencil gave excellent surface quality after 10 s, as shown in Figure 4.10 (b). The small fragments in the aperture seen in the photograph are remnants from processing, which were all removed by washing. The stencil was not properly polished in times less than 10 s. When processing time was relatively short, there were many small fragments left on the surface. In addition, in the 15–20 s range, the numerous small fragments were removed to some extent. However, the surface quality was worse than that obtained after 10 s, and greater surface waviness was observed. On the other hand, many small fragments were found around the aperture wall but were effectively removed through the EP process of the 0.10 mm thick laser-cut stencil, which was the thickest stencil used in this experiment [Figure 4.10 (c)]. The small fragments were completely removed after approximately 20 s of EP, and a highly glossy and satisfactory surface was obtained.

Based on the results of this experiment, it can be concluded that the surface quality would not be improved much if processing time were increased further; thus, it is desirable to select an optimum length of time when considering the efficiency of processing. In addition, because thicker stencils require longer EP time, stencils with different thicknesses must be processed under their respective optimal conditions.

In the case of recent miniature components in the sizes of 0201 and 01005, stencil printing is a great challenge. Since it is fundamentally difficult to obtain a good surface quality with existing laser processing due solely to processing traces such as small fragments on the

surfaces of the apertures of stencils, this EP post-treatment is important for good solder paste release from apertures.

However, it is true that there are limitations to improving the quality of high-quality stencils with EP treatments alone because, as mentioned earlier, processing will not improve the surface quality much after a certain limit is reached. In addition, excessive EP may cause adverse effects due to changes in the size of the aperture and decreases in the thickness of the stencil [27,71]. Therefore, it can be said that, to obtain a fundamentally good surface quality, the quality of the initial laser-processed surface should be good. Given the appropriate selection of stencil materials with excellent properties for laser processing and the appropriate optimization of laser processing conditions, we believe that even better surface qualities can be obtained.

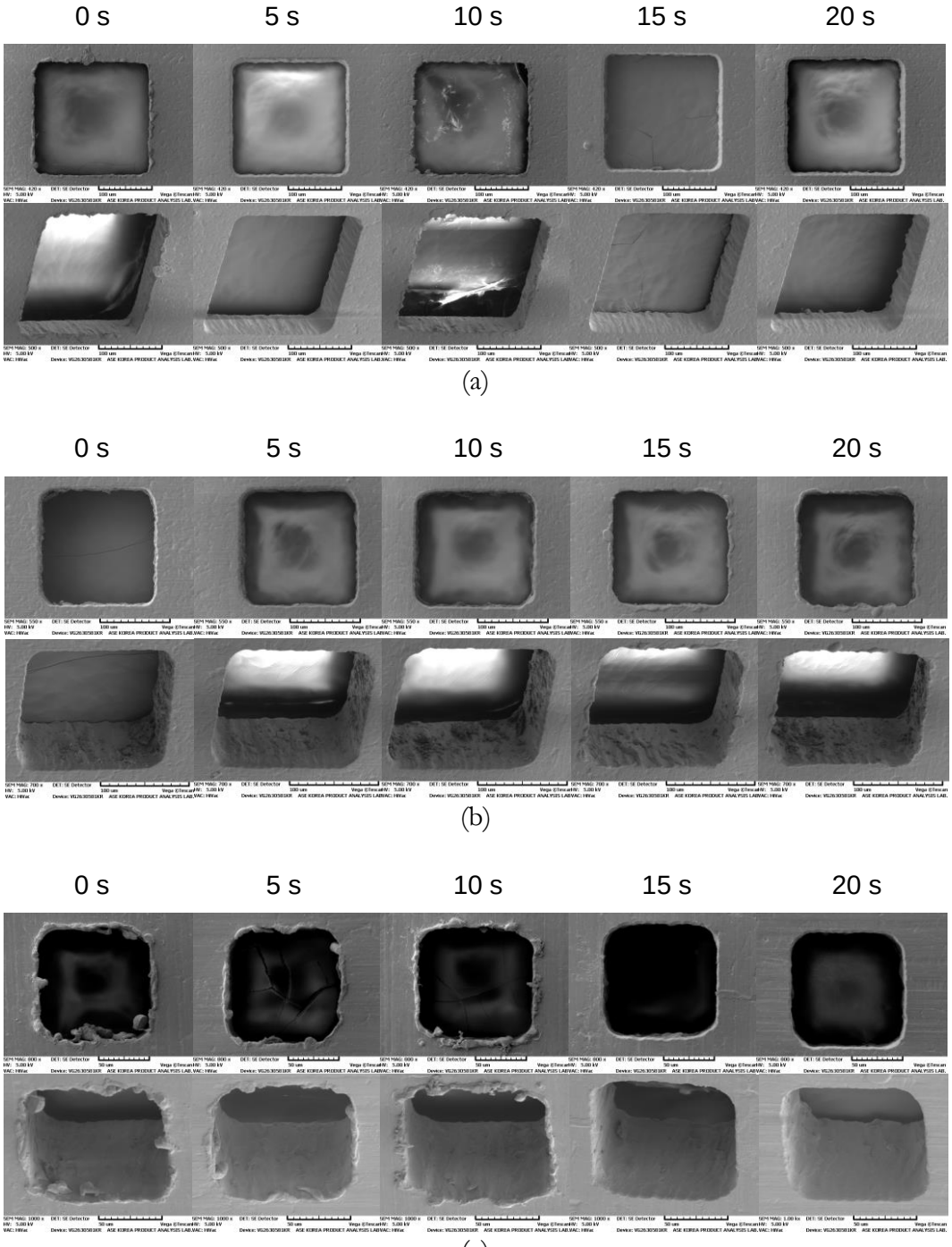


FIGURE 4.10 SEM pictures taken from laser-cut stencil apertures by different EP time.

Notes: (a) 0.05 mm thick; (b) 0.08 mm thick; (c) 0.10 mm thick.

4.4 Summary

This chapter has shown that the phosphoric acid solution concentration and EP time are important conditions in the EP process used for the surface finishing of laser-cut stencil apertures. The optimum concentration of phosphoric acid solution for electropolished laser-cut stencils was determined. The smoothness of the stencil aperture and solder paste printing performance are best when the electrolyte solution concentrations are 95 wt.% phosphoric acid and 5 wt.% sulfuric acid. These bath conditions also yielded better performance when compared to the 85 wt.% phosphoric acid solution.

The surface gloss and roughness of the stencil aperture generally showed improvement as processing time was increased. Thicker stencils were also shown to require a longer EP time. However, the surface quality will not be significantly improved if the processing time is increased further, thus, it is desirable to select appropriate times considering the efficiency of processing.

The quality of the initial laser-processed surface is also important for obtaining good aperture surface quality. Better surface quality can be obtained by selecting stencil materials with excellent properties for laser processing and by optimizing of laser processing conditions.

Chapter 5

The effect of electropolishing on the printing performance of the small apertures[3,4]

This chapter is intended as an expansion of the work of Chapter 4, where we have described the effect of EP process on the laser-cut stencil printing performance. The purpose of this paper is to study the effect of the EP time of stencil manufacturing parameters and solder-mask definition methods of PCB pad design parameters on the performance of solder paste stencil printing process for the assembly of 01005 chip components. During the study, two types of stencils were manufactured for the evaluations: electroformed stencils and electropolished laser-cut stencils. The deposited solder paste thickness was significantly better for the enhanced laser-cut stencil with EP compared to the conventional electroformed stencils. Due to important improvements in the quality of the electropolished laser-cut stencil, and based on the results of this experiment, the electropolished laser-cut stencil is strongly recommended for the solder paste printing of fine-pitch and miniature components, especially in comparison to the typical laser-cut stencil. The advantages of implementing a 01005 chip component mass production assembly process include excellent solder paste release, increased solder volume, good manufacture-ability, fast turnaround time, and greater cost saving opportunities.

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[3] Based on Yong-Won Lee, Keun-Soo Kim, and Katsuaki Suganuma (2013), "The behavior of solder pastes in stencil printing with electropolishing process", *Soldering & Surface Mount Technology*, Vol. 25 No.3, pp. 164-174, and

[4] Yong-Won Lee, Keun-Soo Kim, and Katsuaki Suganuma (2008), "Developing the stencil printing process for 01005 lead-free assemblies", *IEEE International Conference on Electronic Packaging Technology & High Density Packaging, Shanghai, China*, July.

5.1 Objective and overview

Recently, 01005 chip components have been implemented in very high density applications, such as mobile phones, Bluetooth modules, and wireless LANs after extensive process optimization [44,45,47]. Resistors and capacitors are now being produced in the extremely miniaturized 01005 chip size. However, the use of such tiny components poses great challenges for SMT assembly. The main factors affecting the 01005 assembly process can be divided into the following categories: PCB design [48], stencil design [49], solder paste [50], pick-and-place [39], reflow, and inspection [43].

In Chapter 4, I discussed the effects of acid electrolytes and EP times on laser-cut stencil printing performance for the small stencil apertures. The results demonstrate that both the electrolyte and the EP process showed encouraging results in terms of surface smoothness, improved solder paste printing, and assembly yields.

The purpose of this study was to determine the effect of stencil printing variables on solder paste printing. The present study investigated potential factors, such as EP time, and solder-mask definition methods, which may affect solder paste printing performance in the assembly of 01005 chip components with 95wt.%Sn–5wt.%Sb solder paste. The results and printing mechanisms are discussed below and optimized conditions are recommended.

5.2 EP process analysis

5.2.1 Materials and methods

The experimental material was conventional SUS304 stainless steel. The chemical composition of the test steel investigated in this paper is presented in Table 5.1. Specimens of SUS304 stainless steel (50 mm × 50 mm) were cut and their sides were ground to remove burrs. There were a total of 640 apertures for the 01005 chip components. The size of all the apertures was fixed at 0.184 mm (width) × 0.200 mm (length) × 0.080 mm (thickness).

A standard YAG laser (LPKF SL600), with oxygen as its gas medium, was used in the laser-cutting test. The laser-cutting speed was 4 mm/s. Table 5.2 summarizes the laser-cutting machine used to evaluate the laser-cutting performance.

After the laser-cutting process was completed, the EP test was conducted. The EP process includes the following major operations (Figure 5.1):

1. metal preparation to remove surface oils, grease, oxides, and other contaminants that interfere with the uniformity of EP;
2. EP to smooth, brighten, and/or deburr the metal; and
3. post-treatment to remove residual electrolytes and the by-products of the EP reaction, and dry the metal to prevent staining.

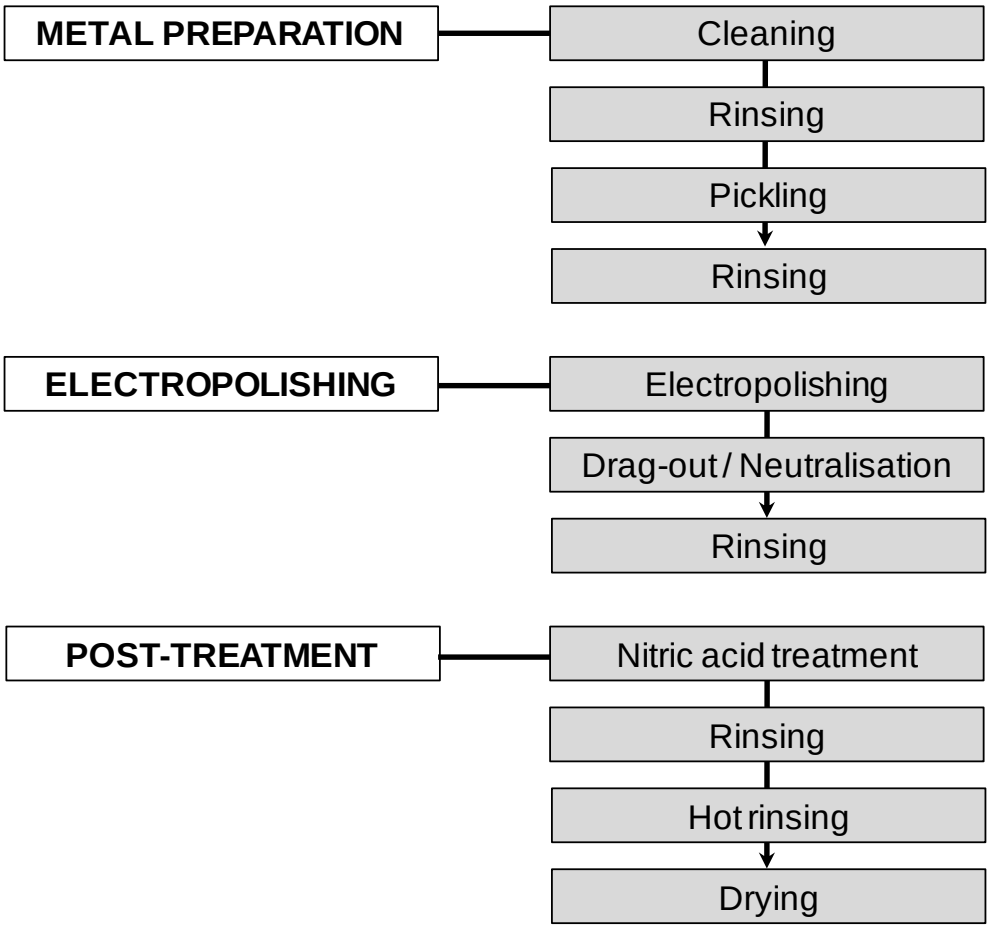


FIGURE 5.1 Schematic diagram of the typical process flow chart.

TABLE 5.1 Chemical composition of the SUS304 stainless steel (wt.%)

SUS304 stainless steel	Composition (%)
Carbon (C)	0.080
Silicon (Si)	1.000
Manganese (Mn)	2.000
Phosphorus (P)	0.045
Sulfur (S)	0.030
Nickel (Ni)	8.000
Chromium (Cr)	18.000
Ferrum (Fe)	Rem

TABLE 5.2 Laser-cutting system used

System specifications	
Laser type	YAG
Model	LPKF SL600
Laser beam size (*μ*m)	40
Laser cutting area (X/Y) (mm)	600 × 600
Laser repetition rate (kHz)	Up to five
Accuracy (*μ*m)	± 10
Repeatability (*μ*m)	± 1

The following important factors were considered: the presence of residual electrolytes, current density, temperature, polishing time and electrode gap. Given the number of factors that influence the EP process, the main challenge of this experiment was to isolate the effect of the EP time. An acid based EP solution (95 wt.% H_3PO_4 : 5 wt.% H_2SO_4) has been used in our laboratory in previous studies of acid electrolytes on stainless steel foils for the laser-cut stencil as shown in Chapter 4. The EP process parameters are shown in Table 5.3.

The stencil apertures that were obtained were inspected using a JEOL JEM-2000 scanning electron microscope (SEM) to determine the surface structures. The stencil aperture size was measured using an optical microscope (Olympus SMT6). The area ratio is the area beneath the stencil aperture opening divided by the area of the inside aperture wall (Figure 5.2). For a rectangular aperture, the area ratio was determined by the following equation:

$$AR = \frac{L \cdot W}{2(L + W) \cdot T}$$

Where L and W are the aperture length and width, respectively, and T is the stencil thickness. The generally accepted rule is to achieve area ratios of > 0.66 for paste transfer [109].

A 3D surface roughness measuring instrument (Keyence VK-9710) was used to obtain the surface roughness of the aperture walls of the stencil. Each test piece was measured five times and the average value calculated. The sliding speed was 0.1 mm/s, and the sliding distance was 0.150 mm. The surface roughness of the cut edge was characterized by the formation of striation lines that were left by the cutting process. Surface roughness (*Ra*) values were measured from the centre line of the cut edge (Figure 5.3).

5.2.2 Design of the experiments

The EP time was selected as an input variable (Table 5.4). The response variables used for the qualitative analysis were the dimension tolerance, the area ratio, the stencil thickness and the surface roughness of aperture wall. For an experimental run, a total of three test specimens were fabricated using the exact same aperture data. All the stencil specimens had a thickness of 0.08 mm.

TABLE 5.3 Parameters of EP

Process parameters	
Power output (DC)	380
Current (mA)	400-500
Voltage (V)	13
Temperature (°C)	40-50
Electrolyte (wt.%)	95 : 5 (H_3PO_4 : H_2SO_4)
Electro gap (mm)	175
Tool material	SUS304 stainless steel

TABLE 5.4 EP variable factors

	Level		
Factor	**No EP**	**Low EP**	**High EP**
EP time (s)	0	100	150

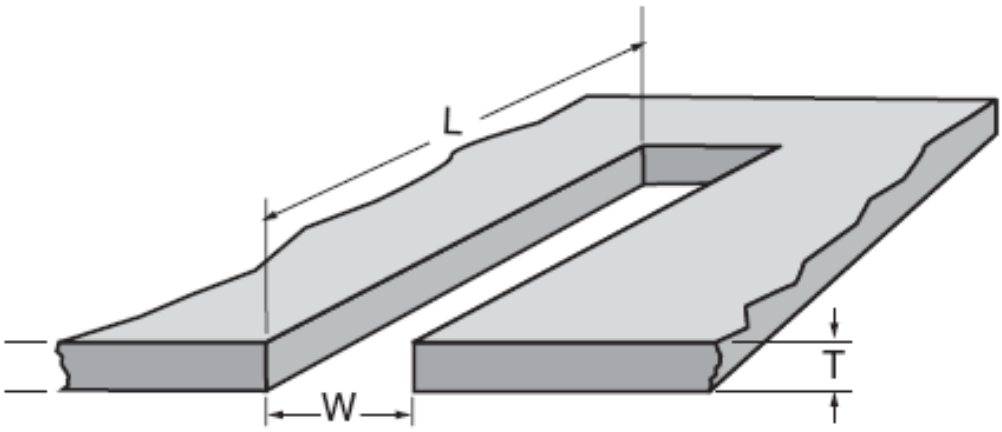
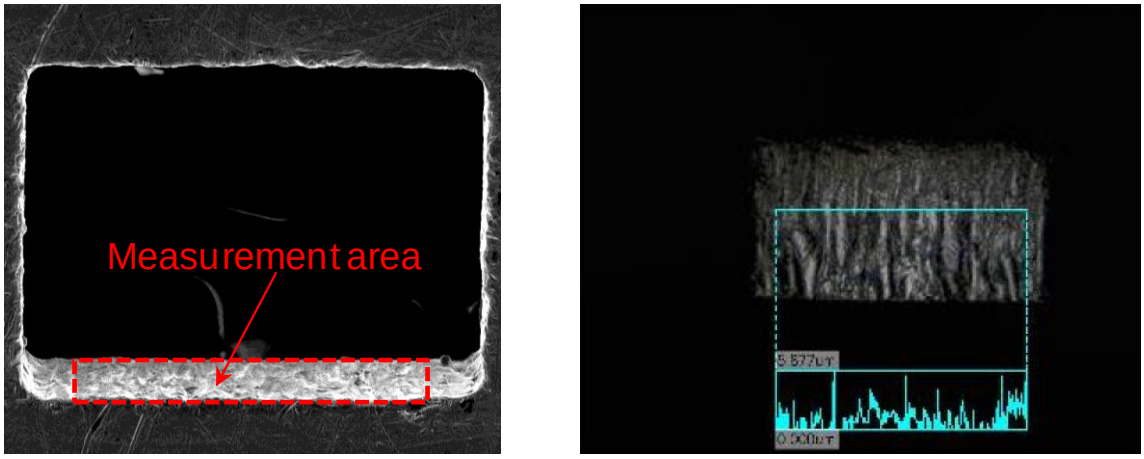


FIGURE 5.2 Dimensions of the stencil aperture [109].



(a) (b)

FIGURE 5.3 Measurement of surface roughness: (a) measurement area of aperture wall; (b) surface roughness profile.

Note: Surface roughness (*Ra*) was measured through center of the material; original magnification: 500X.

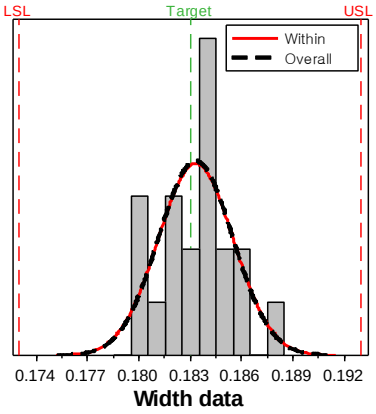
5.2.3 Results and discussion

In this study, the effect of EP time on laser-cut stencil performance was examined by comparing different times. For each time variable, the current density was set at 500 mA and the temperature was 50°C.

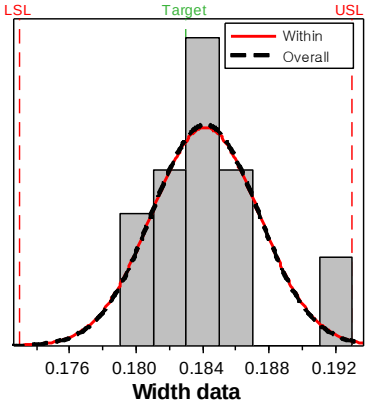
First, the stencil aperture size was analyzed using the statistical process capability analysis method for the characterization of laser-cut dimensional tolerance. All three stencil foils were measured for this test. Figure 5.4 shows histograms of the width distribution of the aperture dimension with a target value of 0.185 mm, lower tolerance limits of 0.175 mm, and upper tolerance limits of 0.195 mm for the specification. Histograms of the length distribution of the aperture dimension with a target value of 0.200 mm, lower tolerance limits of 0.190 mm, and upper tolerance limits of 0.210 mm are shown in Figure 5.5. The results show that most of the electropolished apertures were slightly larger than their specified size, and it was observed that an increase in EP time increases the aperture sizes.

The calculated process capability index (*Cpk*) for each set of parameter settings is provided in Table 5.5. Values greater than 1.0 are acceptable, and a value of 1.33 is a common target [107]. Typically, in electronics assembly, a process is deemed capable if this *Cpk* ratio is 1.67 or greater [108]. Based on the calculated *Cpk* data in Table 5.5, the best settings for dimensional tolerance were low EP (100 s), for both aperture sizes, although all of the measured apertures were well within the specification. The cause of this discrepancy in process capability was due to differences in the quality of the surface polish. The application of the optimized stencil with EP resulted in much smoother aperture walls.

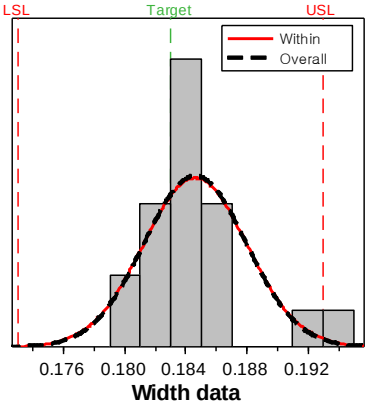
The effect of EP time on stencil thickness was evaluated. Figure 5.6 shows the variations in stencil thickness according to different EP times. Generally, the stencil thickness gradually decreased as the EP time increased. In this experiment, the thickness of the stencil foils decreased to 0.070 mm after high EP (150 s).



(a)



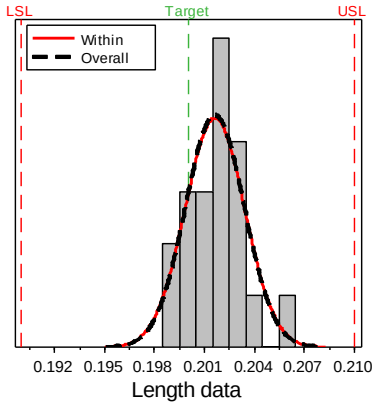
(b)



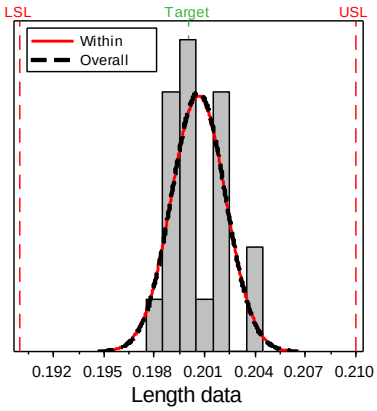
(c)

FIGURE 5.4 Histograms of aperture width distribution for the laser-cut stencil for each EP time.

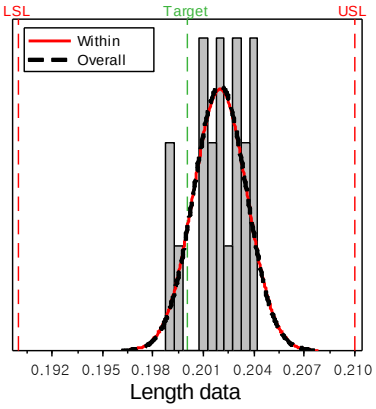
Notes: (a) No EP; (b) low EP; (c) high EP.



(a)



(b)



(c)

FIGURE 5.5 Histograms of aperture length distribution for the laser-cut stencil for each EP time.

Notes: (a) No EP; (b) low EP; (c) high EP.

TABLE 5.5 Measured aperture sizes for each EP time (PCB side)

				Standard deviation		
Dimension	**EP time (s)**	*n*	**Mean**	**Within**	**Overall**	*Cpk*
Width (X)	No EP (0)	20	0.1832	0.002198	0.002169	1.47
	Low EP (100)	20	0.1841	0.003218	0.003176	0.92
	High EP (150)	20	0.1845	0.003390	0.003345	0.83
Length (Y)	No EP (0)	20	0.2016	0.001793	0.001770	1.55
	Low EP (100)	20	0.2006	0.001622	0.001601	1.92
	High EP (150)	20	0.2020	0.001590	0.001569	1.68

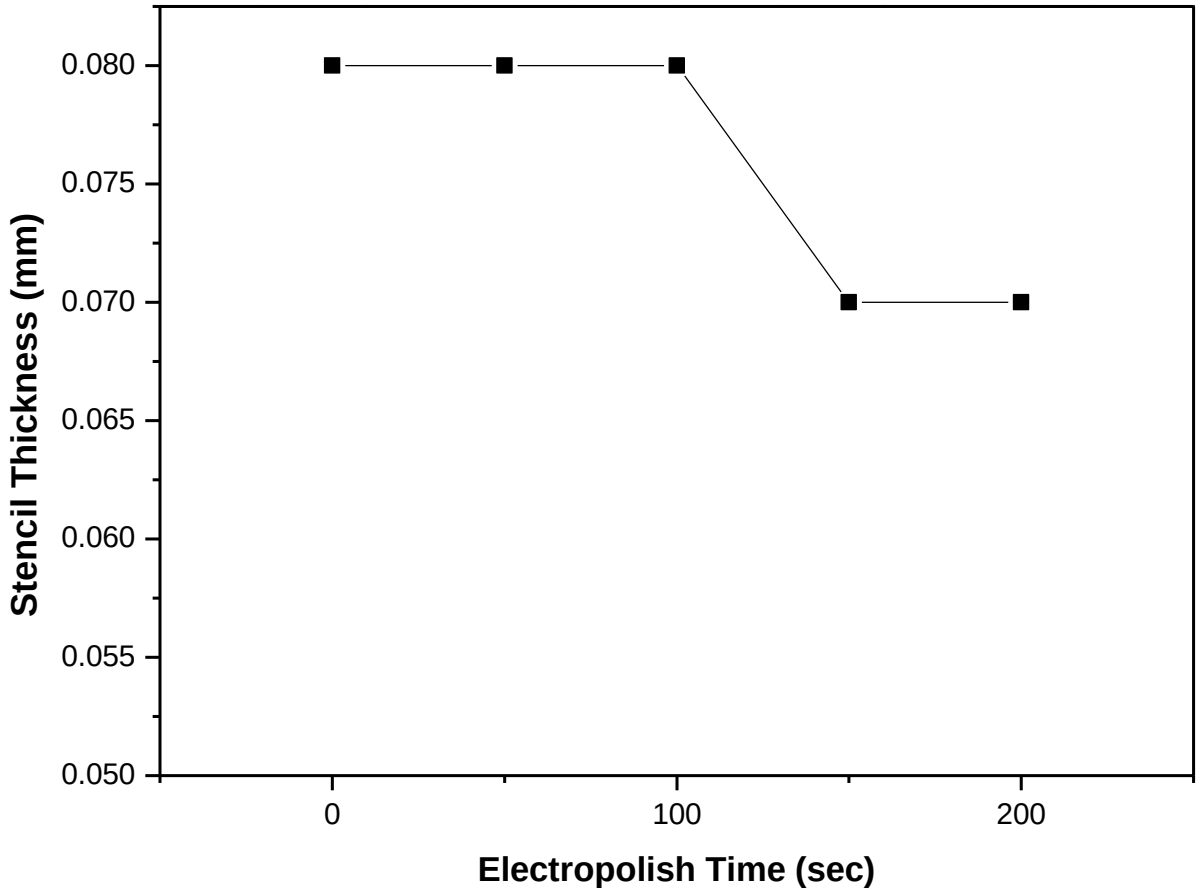


FIGURE 5.6 Relationship between EP time and stencil thickness.

The effect of EP time on area ratio was also evaluated. Figure 5.7 shows the relationship between EP time and area ratio. The area ratio increased after the EP time was increased beyond low EP (100 s). In this experiment, the area ratio was at maximum when the EP time was high EP (150 s).

The smoothness of the metal surface is one of the primary and most advantageous effects of EP. The effect of EP time on the surface roughness of the stencil apertures was examined. Figure 5.8 shows the relationship between average surface roughness and EP times. In this set of experiments, the highest roughness (*Ra*) was found in the work pieces that did not undergo EP. The surface roughness decreased rapidly after the EP times were increased beyond low EP (100 s). In cases where smoother surfaces are needed, longer polishing times are required. The smallest roughness value *Ra* within this set of experiments was achieved after 150 s of EP at an average current density of 500 mA. The *Ra* value was less than 0.72 μm. In EP, it is commonly known that lower roughness can be achieved at longer EP times with higher current densities [110]. The longest EP time will make the aperture wall shinier and smoother, which helps release more paste from the apertures; however, a longer time will also make the edges more round. In addition, it was observed that an increase in the length of EP time caused a decrease in the stencil thickness and an increase in the aperture size during the course of experimentation (Figures 5.6 and 5.7). Based on the above results, it was decided that the low EP condition (100 s) would be used for further study.

The aperture walls were examined with a SEM at 600 X magnification. A comparison of aperture walls before and after EP is shown in Figure 5.9. From the figure it can be seen that the laser-cut stencil has tapered apertures, and it was exactly 2.5 degrees by cross-section. The degree of taper depends upon the laser parameters, which should be controlled tightly during the manufacturing process for these types of stencils. Figure 5.9 (b) shows how successive EP can smooth out the aperture side wall to improve paste release for the electropolished laser-cut stencil.

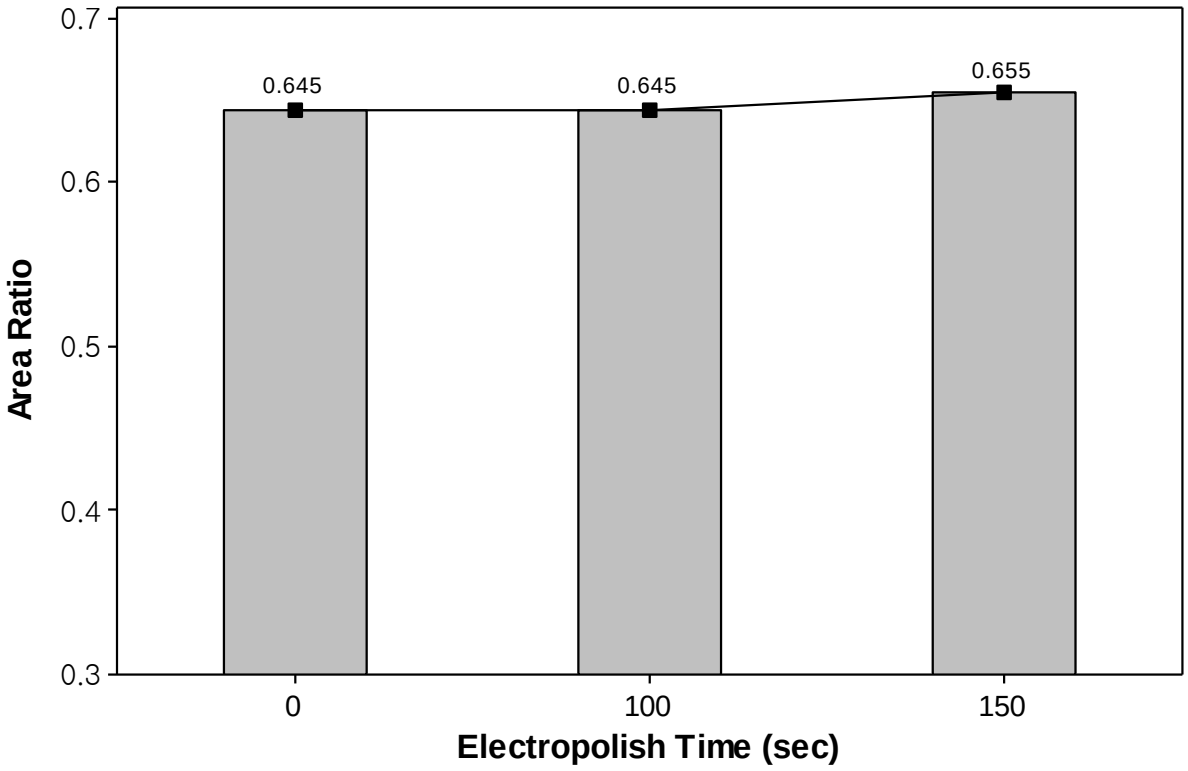


FIGURE 5.7 Relationship between EP time and area ratio.

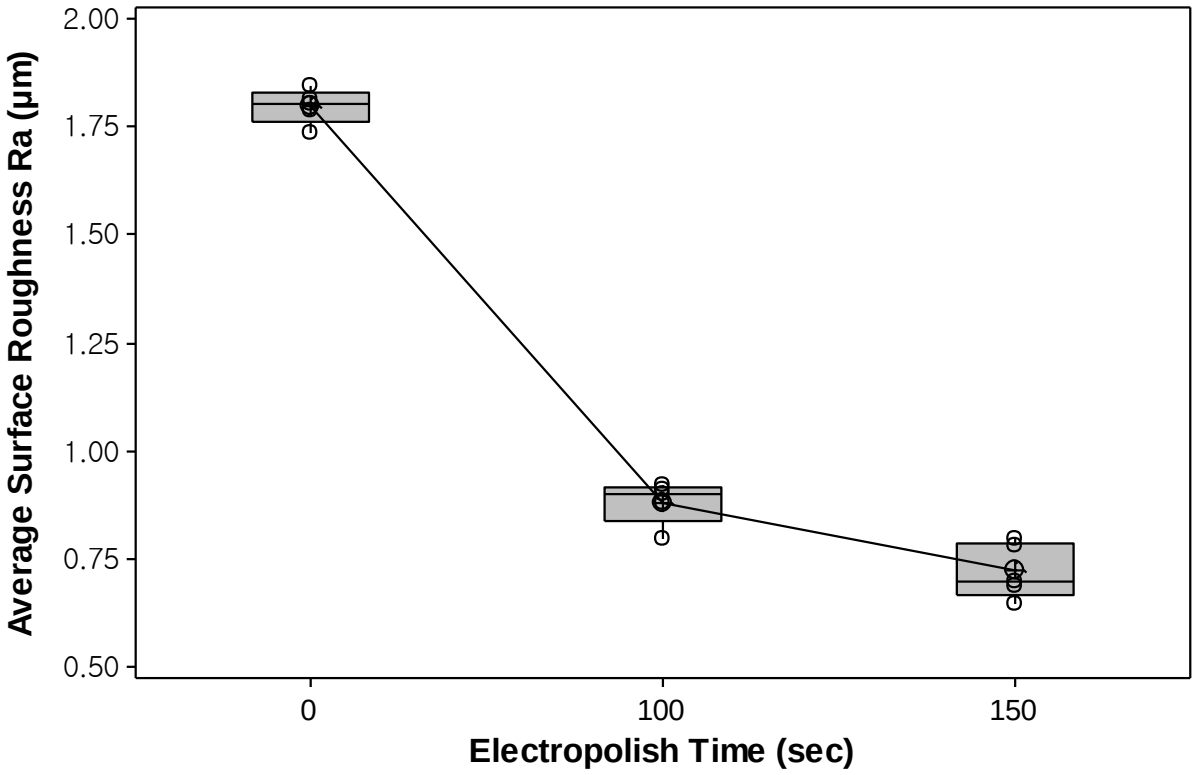
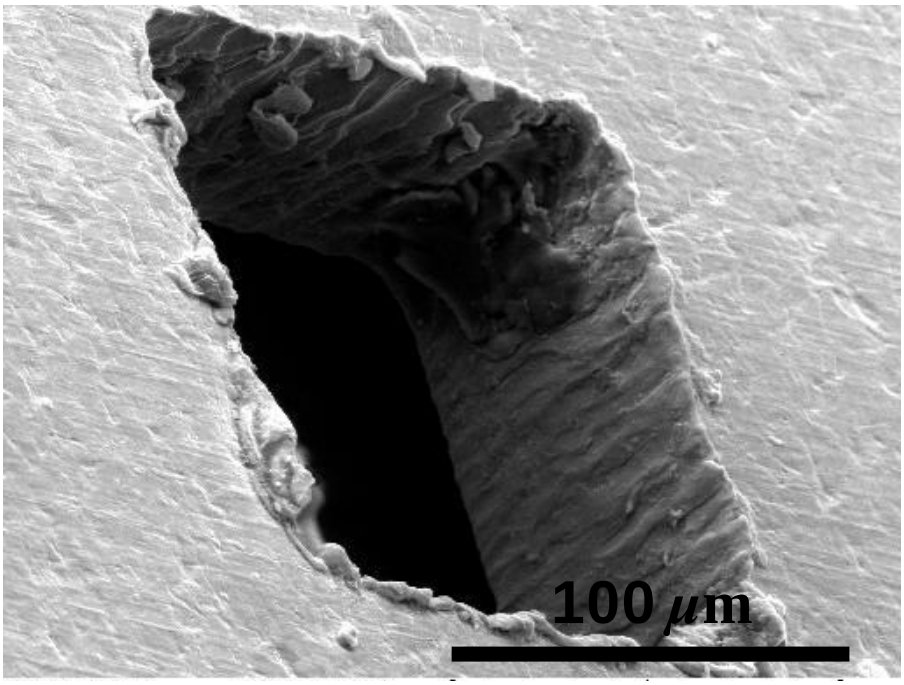
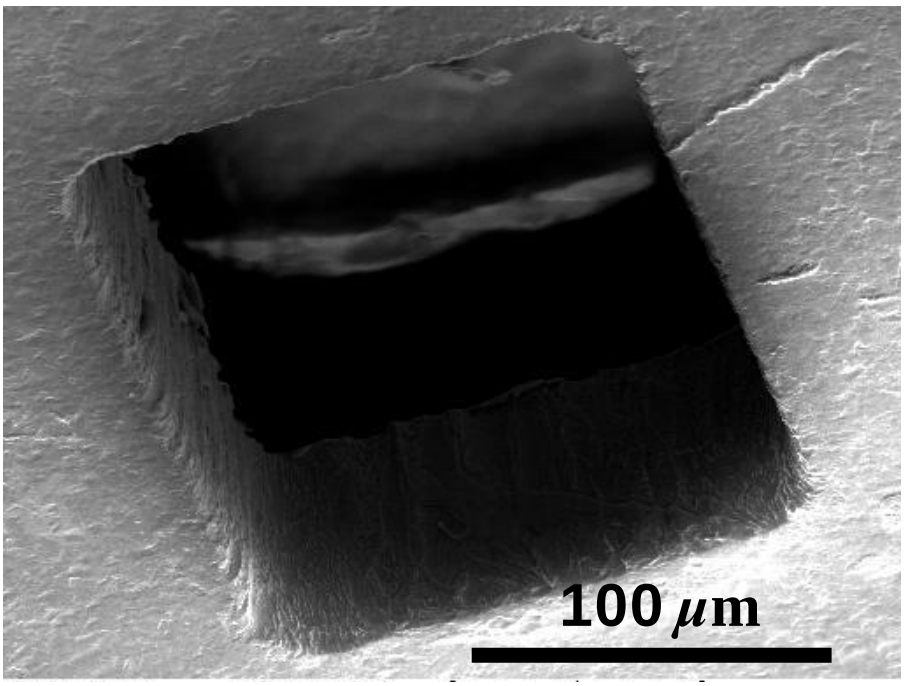


FIGURE 5.8 Relationship between EP time and aperture surface roughness (*Ra*).

Note: The box plot showing the smallest value, the first quartile, the median, the third quartile, and the largest value.



(a)



(b)

FIGURE 5.9 (a) SEM images of square aperture wall geometry after laser-cutting; (b) after EP.

Note: A microscopic view of the same surface before and after EP shows that the process produces clean metallic surfaces; material: SUS304 stainless steel; laser-cutting speed: 4 mm/s; EP time: 100 s (Low EP); original magnification: 600X.

5.3 Solder printing behavior

5.3.1 Materials and methods

The test vehicle used in this experiment is shown in Figure 5.10. A test vehicle, four-layer BT boards with a nickel/gold finish using 01005 and 0201 chip components, was designed for the stencil printing process evaluation. The test vehicle was a 10 mm × 10 mm laminated module, composed of a 5 × 5 × 3 matrix and consisting of 3,000 pad layouts for the 01005 chip components and 1,950 pad layouts for the 0201 chip components. All 01005 passive component pads in this design were fixed at 0.184 mm (length) × 0.200 mm (width) × 0.150 mm (space), and all the 0201 components pads were fixed at 0.300 mm (length) × 0.360 mm (width) × 0.220 mm (space). The solder-mask definition methods for all chip components were solder-mask-defined (SMD) pads and non-solder-mask-defined (NSMD) pads.

The solder paste used in this experiment was a water soluble 95wt.%Sn–5wt.%Sb paste with a type 4 (size range: 20–38 μm) particle size (Alpha Metal WS609). The solder content was 90 wt.% and the melting point was approximately 232–240°C, as noted in the supplier's specification. Since the solder paste was stored at 4°C, it had to be brought to room temperature before being used in the screen printer for the experiments.

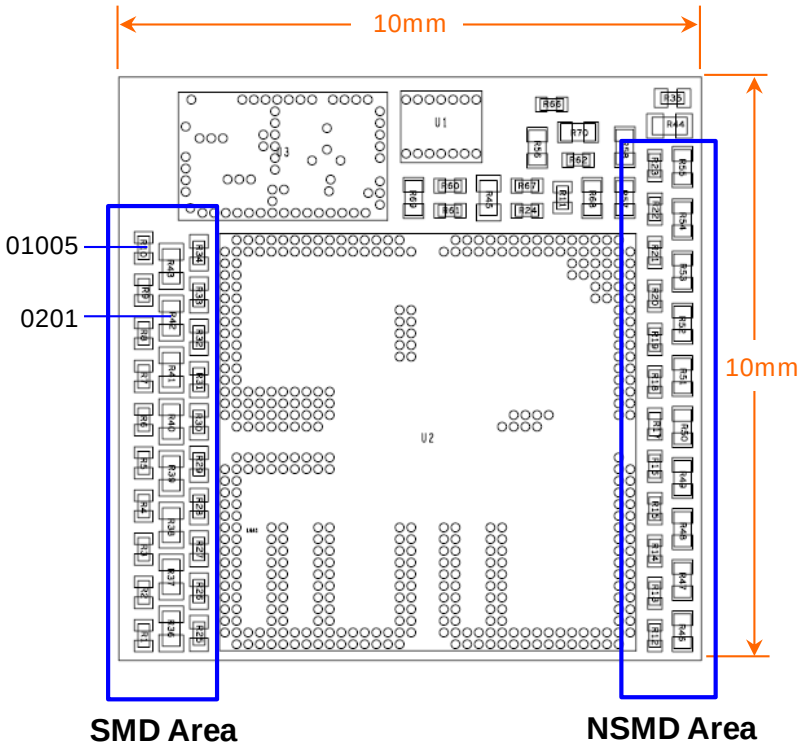
5.3.2 Design of the experiments

Two kinds of stencils—electroformed and laser-cut with EP—were tested in the experiments. The stencils were manufactured using the exact same aperture data, while the opening ratio of aperture-to-pad-size was 100 percent for the 01005 chip components. The stencil geometry is summarized in Table 5.6. Note that the area ratios listed in the table are lower than the industry recommended 0.66 for both the laser-cut stencil and the electroformed stencil apertures; this was done in order to achieve acceptable volume control according to the IPC stencil design guideline [109].

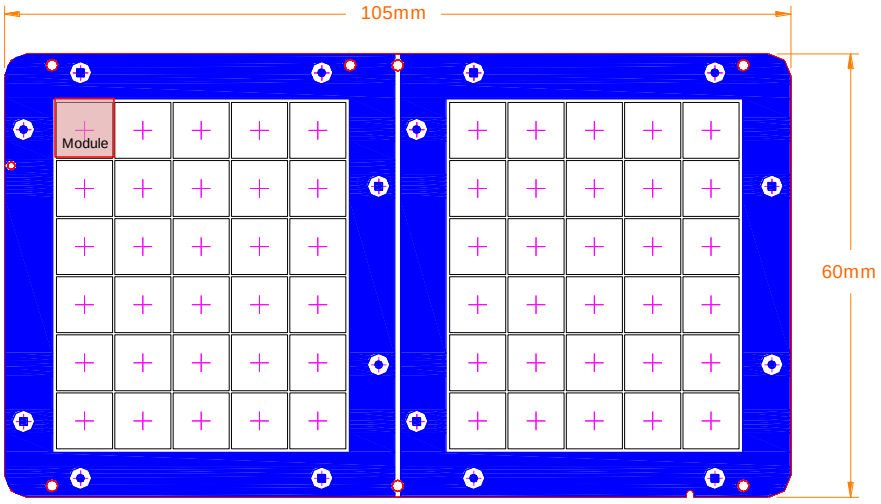
Two solder-mask definition methods were tested in the experiment: SMD pads and NSMD pads. Solder paste thickness and shear strength were used to determine performance. For an experimental run, a total of 30 test vehicles were fabricated for each stencil.

TABLE 5.6 Stencil geometry

Stencil type	Aperture ratio (%)	Aperture design	Stencil thickness (mm)	Area ratio
Electroformed	100	Square	0.08	0.63
Laser-cut (EP)	100	Square	0.08	0.64



(a)



(b)

FIGURE 5.10 Test vehicle design for printing experiments: (a) module design; (b) top-side view that shows entire PCB substrate strip outline.

Note: SMD refers to solder-mask-defined pad; NSMD refers to non-solder-mask-defined pad.

5.3.3 Results and discussion

5.3.3.1 Electropolished laser-cut stencil vs. electroformed stencil

Figure 5.11 shows a box plot of the solder paste thickness for the 01005 chip components. The range is defined as the highest solder paste thickness minus the lowest solder paste thickness. The bottom of the box represents the first quartile (Q1) and the top of the box represents the third quartile (Q3). The whiskers extend to the furthest data point within 1.5 times the width of the box. Figure 5.11 shows that, for the 01005 chip components, the thickness of the solder paste that was deposited in the laser-cut stencil with EP was higher than the thickness of the solder paste of the electroformed stencil.

It was necessary to determine whether the difference observed was statistically significant. This was done using the two-sample *t*-test results shown in Table 5.7. The results show that the *p*-value was 0.001 for each stencil type. This value of the two-sample *t*-test indicates that the solder paste thickness resulting from the two stencil types were statistically different (*p*-value < 0.05).

As can be seen from the graph, the values plotted are often referred to as the stencil printed release values. Release is defined as the volume of the stencil printed deposit divided by the volume of the apertures [111]. The graph shows that the electropolished laser-cut stencil demonstrates better paste release on the 01005 apertures. The better performance of the electropolished laser-cut stencil could be due to the improved surface quality of the aperture wall, resulting from the EP process.

Second, a repeat printing experiment was performed on 30 boards for each stencil type. The objective of this experiment was to determine the print frequency and stencil cleaning interval for each stencil type. Figure 5.12 shows the solder paste thickness for each stencil type, by repeat printing, without wiping the 01005 chip components. From the graphs, it can be seen that no significant drop occurred in the repeat printing for both the electroformed stencils and the electropolished laser-cut stencils. However, the paste thickness and print stability for the electropolished laser stencil was better than it is for the electroformed stencil. Visual inspection was performed on seven of the 30 boards printed for each stencil. Figure 5.13 and Figure 5.14 show the conditions of repeat printing on sections of the 01005 chip component pads. An

excellent printability is shown for both stencil types, with no bleeding from the beginning sheet to the 30th sheet.

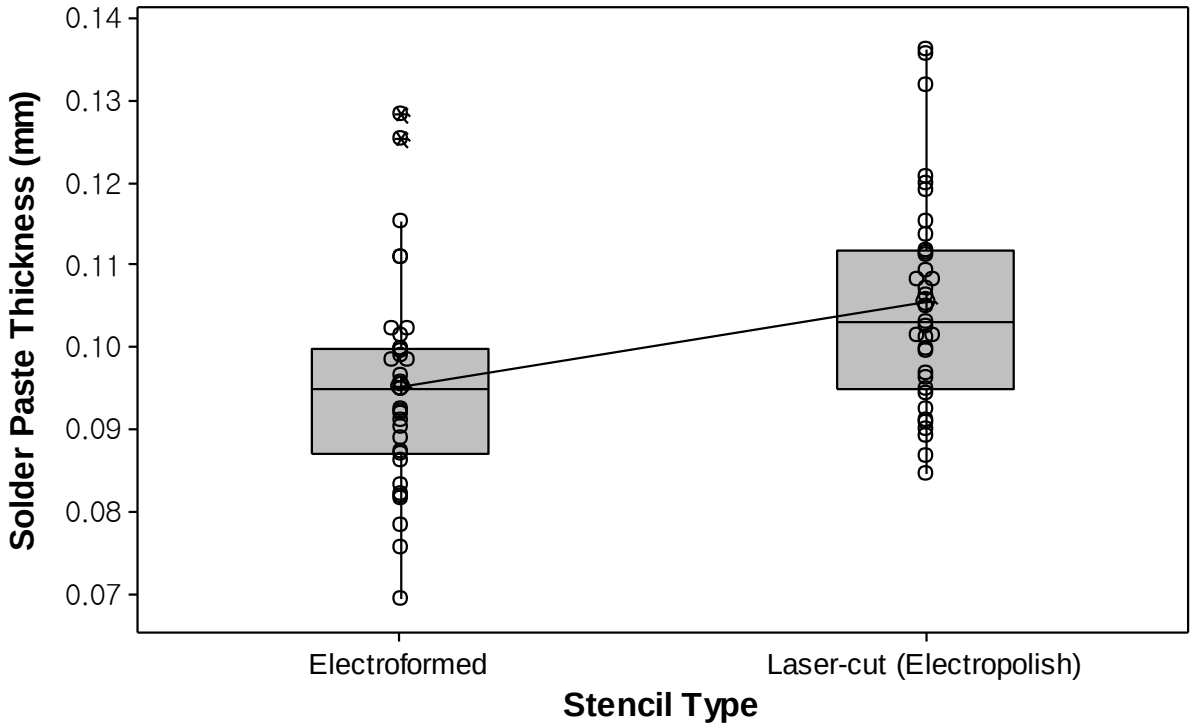


FIGURE 5.11 Solder paste thickness comparisons for each stencil type.

TABLE 5.7 Two-sample *t*-test results for each stencil type

Stencil type	*n*	**Mean**	**SD**	**SE mean**	*p*-**value**
Electroformed	35	0.0951	0.0127	0.0021	0.001 ($p < 0.05$)
Laser-cut (EP)	35	0.1054	0.0132	0.0022	

Notes: SD - standard deviation; SE mean - standard error mean

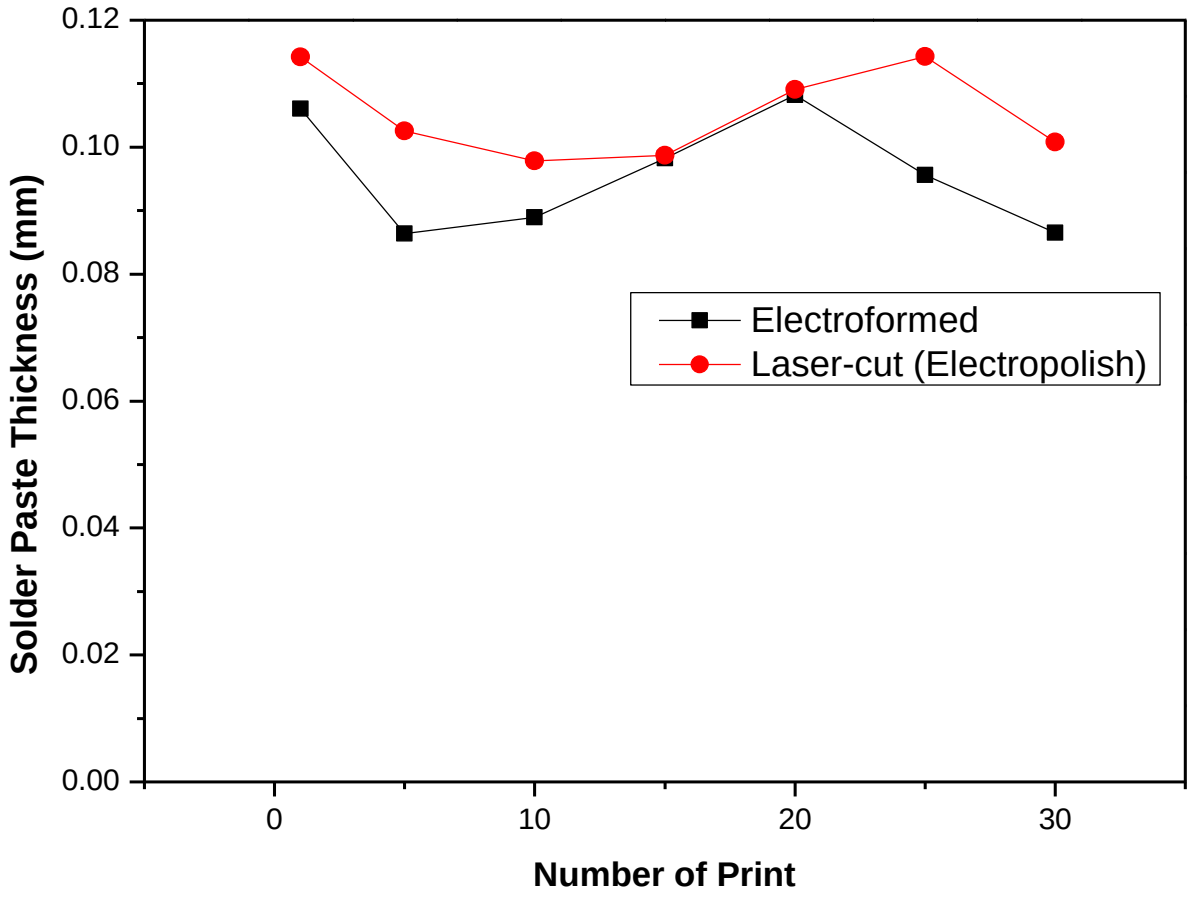
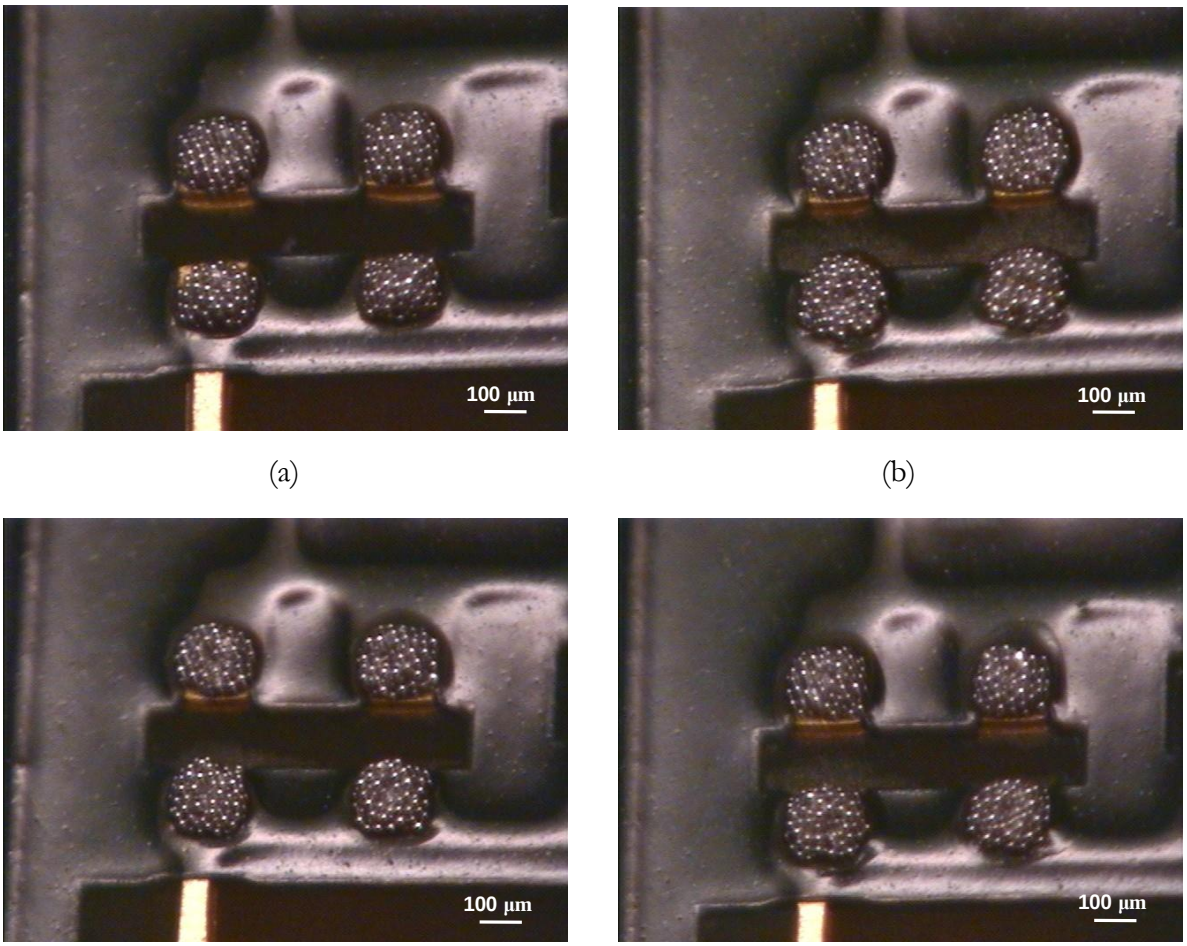


FIGURE 5.12 Effect of repeat paste printing without wiping for each of the stencils.

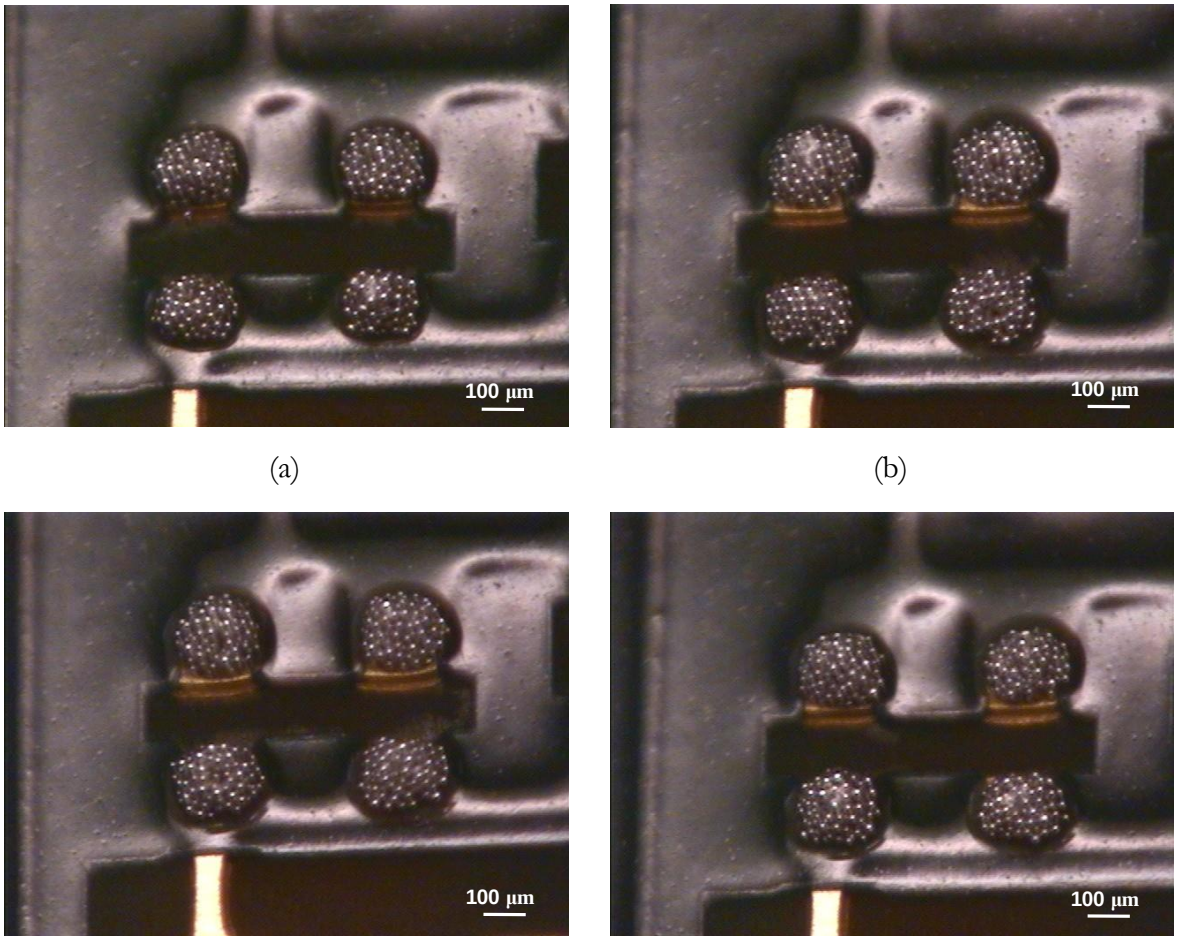


(a) (b)

(c) (d)

FIGURE 5.13 OM images showing the solder deposition results of repeat printing for the electroformed stencils.

Notes: (a) First print; (b) tenth print; (c) 20th print; (d) 30th print.



(a) (b)

(c) (d)

FIGURE 5.14 OM images showing the solder deposition results of repeat printing for the electropolished laser-cut stencils.

Notes: (a) First print; (b) tenth print; (c) 20th print; (d) 30th print.

5.3.3.2 SMD pads vs. NSMD pads

The solder paste thickness measurement data were analyzed, and the data obtained from the SMD pads and the NSMD pads were analyzed separately. Laser-cut stencils with EP and type 4 (size range: 20–38 μm) solder paste were used for this test.

Figure 5.15 shows the box plot of the thickness of the deposited solder paste versus each solder-mask definition method for the 01005 chip components. The box plot reveals that the average solder paste thickness in the SMD solder pad was higher than the average solder paste thickness in the NSMD solder pad. The results of the two-sample *t*-test show that the *p*-value was 0.000 for each solder-mask definition method, as shown in Table 5.8. This two-sample *t*-test value indicates that the two solder pads were statistically different (p-value < 0.05).

Several fine feature studies have shown that SMD pads generally have higher print volumes than NSMD pads [112,113]. This is because the paste thickness of the solder-mask adds an extra amount of volume to the print area (Figure 5.16). As can be seen, since the solder-mask was under the stencil, more solder paste was printed on the SMD solder pad than on the NSMD solder pad; therefore, the solder paste volume on the SMD solder pad is higher than it is on the NSMD solder pad.

Figure 5.17 shows a box plot comparing the component shear strength for each solder-mask definition method. The lower specification limit (*LSL*) was 1.47 N for the shear strength of the 01005 chip components. From the box plot it can be seen that the shear strength in the SMD pad was approximately 22 percent higher than the shear strength of the NSMD solder pad. The results of the two-sample *t*-test show that the *p*-value was 0.000 for each solder-mask definition method, as shown in Table 5.9. This two-sample *t*-test value indicates that the component shear force resulting from the two solder-mask definition methods was statistically different (p-value < 0.05). This is because the SMD pads have higher print paste volumes than the NSMD pads. This is considered to be a benefit, as the extra solder volume will increase the reliability of the package. Thus, pad definition methods should be considered when generating stencil apertures for fine feature devices.

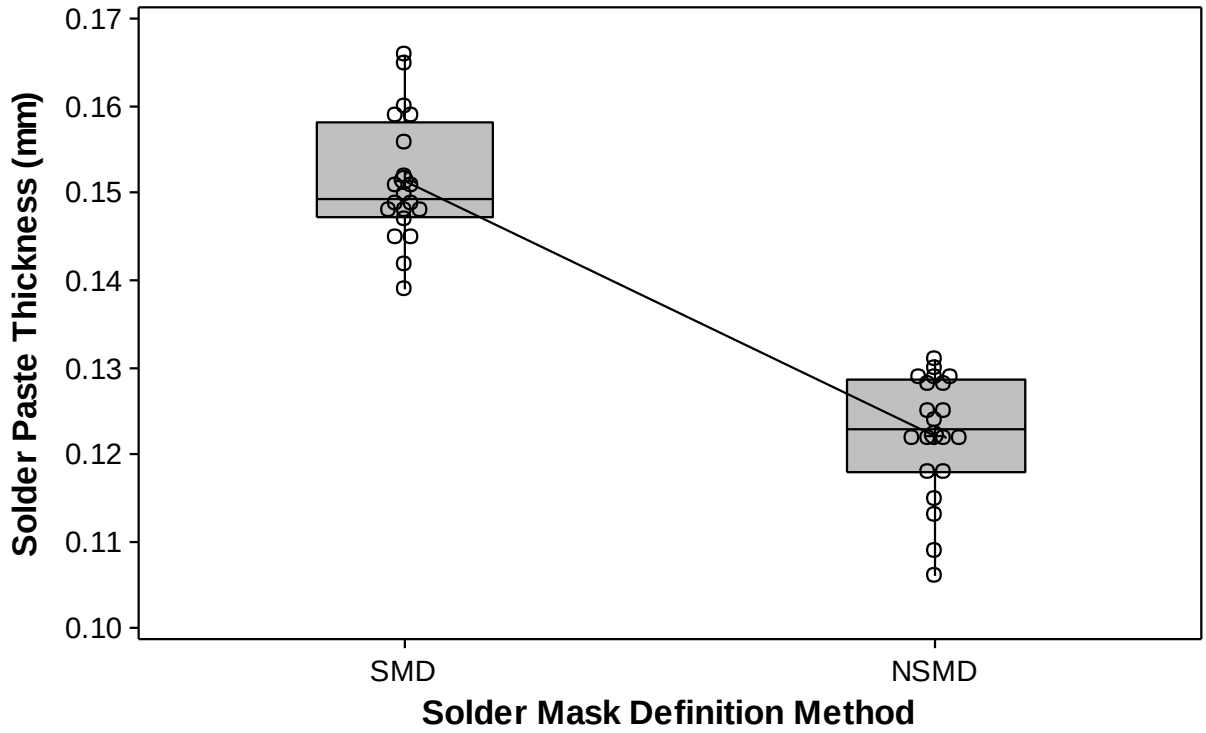


FIGURE 5.15 Solder paste thickness comparisons for each solder-mask-definition method.

Note: The box plot shows the smallest value, the first quartile, the median, the third quartile, and the largest value.

TABLE 5.8 Two-sample *t*-test results of solder paste thickness for each solder-mask definition

Solder-mask definition method	*n*	Mean	SD	SE mean	*p*-value
SMD	20	0.15145	0.00726	0.0016	0.000 ($p < 0.05$)
NSMD	20	0.12250	0.00715	0.0016	

Notes: SD - standard deviation; SE mean - standard error mean

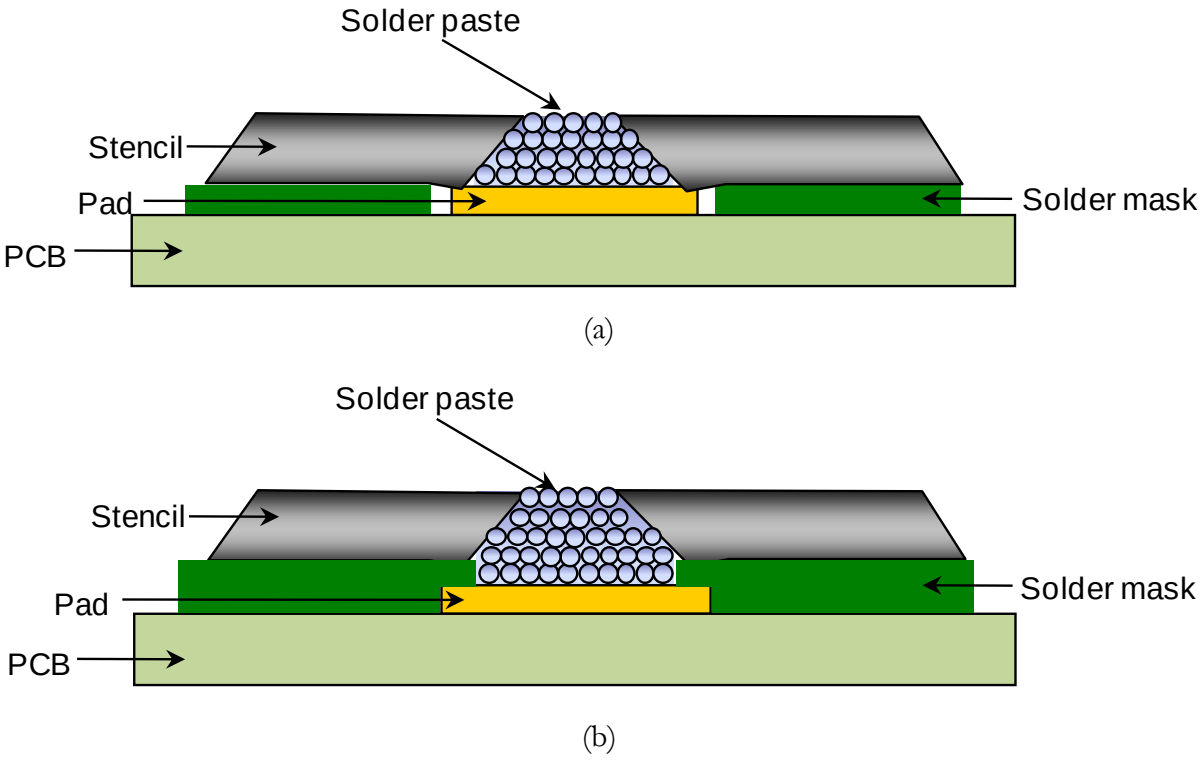


FIGURE 5.16 Structure of the solder pads using different solder-mask definition methods.

Notes: (a) non-solder-mask-defined pad; (b) solder-mask-defined pad.

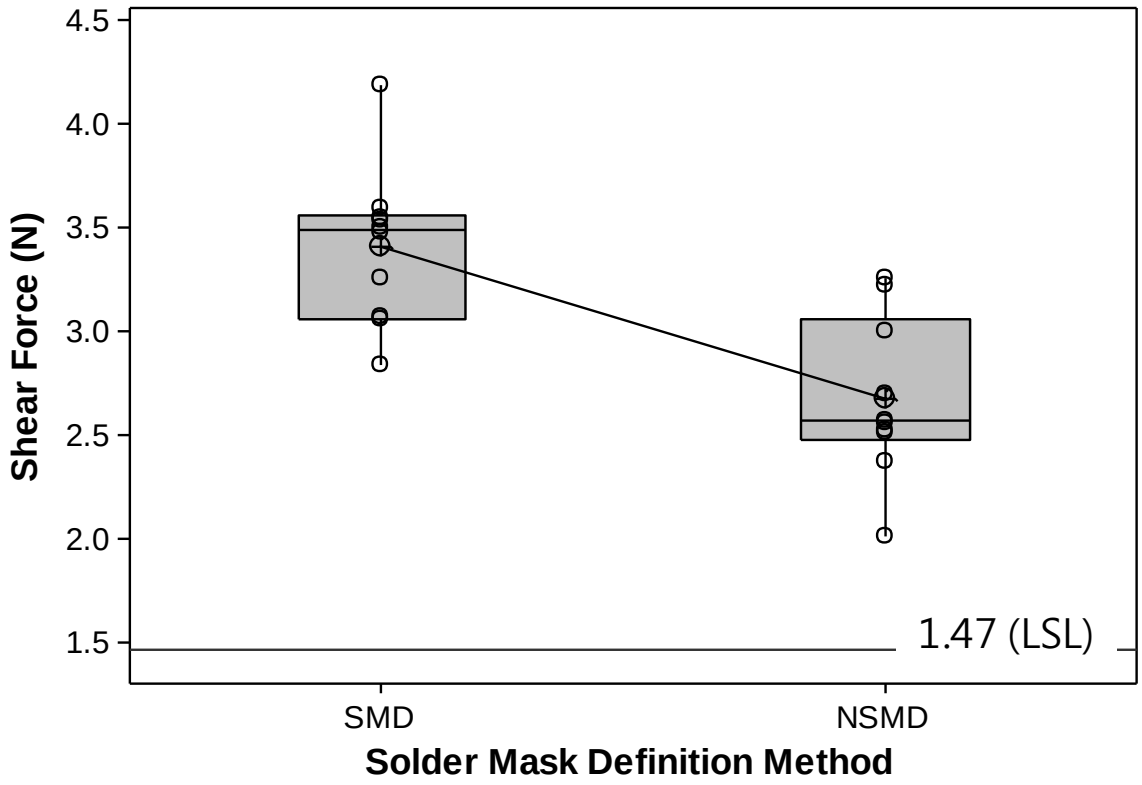


FIGURE 5.17 Shear force comparisons for each solder-mask definition method.

TABLE 5.9 Two-sample *t*-test results of shear force for each solder-mask definition method

Solder-mask definition method	*n*	Mean	SD	SE mean	*p*-value
SMD	10	3.411	0.376	0.12	0.000 ($p < 0.05$)
NSMD	10	2.679	0.386	0.12	

Notes: SD - standard deviation; SE mean - standard error mean

5.4 Summary

The results of this work provide the operating process window for a stencil printing process that can be used for the mass production assembly of lead-free 01005 chip components. Stencil aperture wall quality has a direct influence on solder paste release and, as a result, a post-finishing process, such as EP for laser-cut stencil manufacturing, is necessary in order to achieve a smoother surface. In this experiment, the surface roughness of the stencil aperture wall generally showed improvement as the EP time was increased. However, the longest EP time also resulted in a decrease in the stencil thickness and an increase in the aperture size, which may affect bridging problems, such as the spacing between the pads. Thus, it is desirable to select appropriate EP times in order to take the efficiency of the processing into consideration.

Stencil printing transfer efficiency was significantly better for the laser-cut stencils with EP, as compared to the typical electroformed stencils. This study's findings have shown that laser-cut stencils with EP can be used for the mass production assembly of 01005 chip components.

In this study, print paste thickness measurements were found to vary across different solder-mask definition methods with no change in the stencil aperture size. The highest paste value transfer consistently occurred with the SMD pads, when the laser-cut stencil with EP method was used.

Chapter 6

The effect of stencil materials on stencil printing performance[5]

This chapter is intended as an expansion of the work of Chapters 4 and 5, where we have described the effect of EP process-related variables, such as electrolyte, and EP time, on the laser-cut stencil printing performance of the small apertures. In this chapter, the effect of the stencil material and stencil manufacturing parameters were investigated for a 150 μm pitch flip-chip assembly application. The current state of the art for metallic stencil printing of solder paste is limited to pitches between 400 μm and 500 μm. In this study, the flip-chip device was successfully stencil-printed down to a pitch of 150 μm at an aperture size of 100 μm. This advancement in the stencil printing process was possible by utilizing both a smaller solder sphere size and a novel fine-grained metallic stencil technology. The study evaluated solder paste printing process-related variables, such as solder paste type, print speed, and print force to achieve a high-yield assembly solution for fine pitch structures. A silicon PCB substrate was used in a series of experiments designed to optimize the solder paste printing process.

[5] Based on Yong-Won Lee (2013), "A novel process results in ultra fine-pitch stencil printing and improved properties", *Soldering & Surface Mount Technology* (in review).

6.1 Objective and overview

The attractiveness of flip-chip technologies includes superior electrical performance, higher thermal conductivity, smaller size and higher I/O counts, which are mandatory requirements for advanced semiconductor applications. However, a substantive shift towards flip-chip interconnection technologies will be accomplished only by the development of cost-efficient high-density substrate technologies [114].

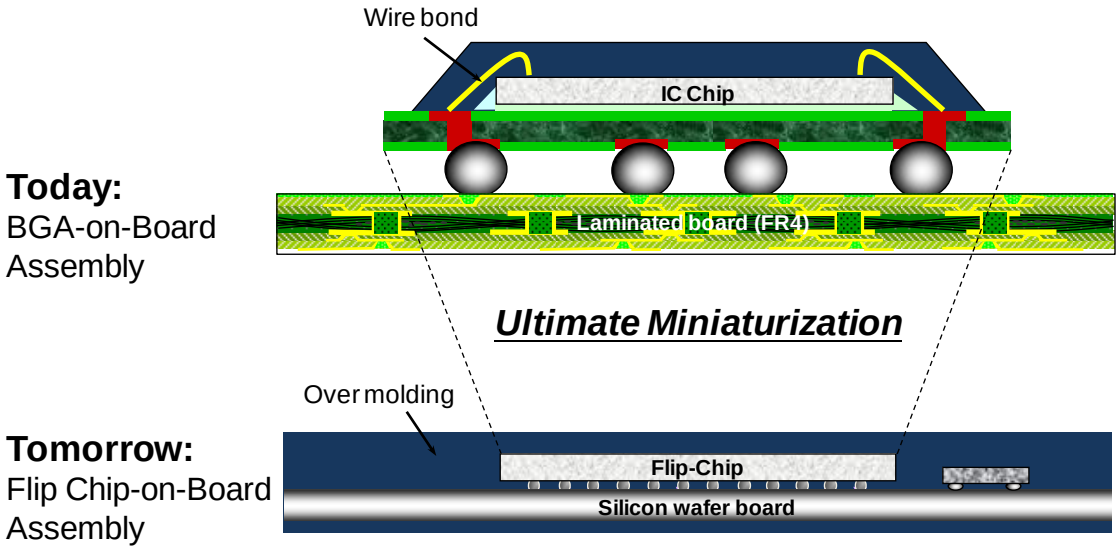


FIGURE 6.1 Schematic diagram of the flip chip-on board (FCOB) assembly with silicon wafer substrate.

In the present study, next generation silicon substrates were used as a potential alternative for the fabrication of organic laminate PCB substrates that are able to support high-density interconnect, as illustrated in Figure 6.1. In the assembly concept of the flip chip-on-board (FCOB) assembly, the over-mold printed board assembly consists of a silicon wafer substrate. This patented process eliminates many of the assembly processes that use conventional packaging, resulting in a dramatic reduction in board size and manufacturing cost [115].

For current pitches from 150 μm to 200 μm, flip-chip bumps are the most commonly used technology. However, the creation of solder interconnects at pitches below these values

must overcome a number of process and design-related challenges. A major challenge is the solder interconnection process, which includes solder bumping and paste deposition on PCB substrates.

In solder bumping technologies, metal stencil printing has been shown to be 2 to 10 times less expensive than evaporation and electroplating [116]. In a single print stroke, stencil printing can deposit millions of interconnects onto a variety of different substrates (i.e., die, wafer, and PCB). This cost advantage, coupled with the ability to deposit solder alloys, makes it the most attractive option for high volume, low cost flip-chip assembly.

In this chapter, we report the development of a novel stencil technology for a low cost and high throughput flip-chip assembly process using silicon substrates. The fine-grained stencil is tested for print performance with very fine pastes, which contributes to defining the narrow process windows of type 6 and type 7 pastes for ultra-fine pitch flip-chip applications. The assembly of a FCOB based on silicon substrates and solder paste deposits stencil printed at a pitch of sub-150 μm is described.

6.2 Noble stencil technology development

6.2.1 Experimental

The experimental materials were commercialized SUS304 stainless steel with coarse grain sizes from 20 to 30 μm and a fine-grained SUS301 stainless steel with grain sizes from 1 to 2 μm. The chemical composition of the test materials investigated here is presented in Table 6.1. All steels were in hot-rolled condition. Their mechanical properties are shown in Table 6.2.

Some test specimens were prepared to examine the microstructure and grain sizes of both materials. These were grounded, polished with diamond paste, and etched by standard procedures suitable for stainless steel microstructures.

TABLE 6.1 Chemical composition of stainless steels used in this study (Weight %)

	Composition%	
Element	**Coarse grain**	**Fine grain**
Carbon (C)	0.080	0.013
Silicon (Si)	1.000	0.430
Manganese (Mn)	2.000	1.360
Phosphorus (P)	0.045	0.030
Sulfur (S)	0.030	0.005
Nickel (Ni)	8.000	6.680
Chromium (Cr)	18.000	17.280
Nitrogen (N)	-	0.130
Niobium (Nb)	-	0.050
Ferrum (Fe)	Rem	Rem

TABLE 6.2 Mechanical properties of stainless steel

Sample index	**Coarse grain**	**Fine grain**
Material (Stainless steel)	SUS304	SUS301
Finish	H-TA	H-TA
Vickers hardness (Hv)	370	421
Tensile strength (N/mm²)	1,130	1,230
Yield strength (N/mm²)	931	1,173
Elongation (%)	3	9
Average grain size (*μ*m)	25	2

A high-speed microscope (Keyence VW-9000) was used in a slow motion analysis of the board-stencil interactions during stencil separation. The stencil apertures obtained were inspected using scanning electron microscopy (FEI, Quanta-600) to photograph the surface structures. The stencil aperture size was measured by optical microscope (Olympus SMT6).

For characterization of the wetting state, contact angle measurement was carried out on a portable contact angle analyzer. A measure for wettability is contact angle α, which identifies the hydrophobic properties of the surface (Figure 6.2). The concept of the contact angle is most commonly illustrated by letting a droplet of water fall upon a solid surface and then observing the boundary of the droplet.

A 3D surface roughness measuring instrument (Keyence VK-9710) was used to obtain the surface roughness of the aperture walls of the stencil. Each test piece was measured 5 times and the average value was used for a more accurate reading. The surface roughness of the cut edge was characterized by the formation of striation lines that were left by the cutting process. *Ra* values were measured from the center line of the cut edge (Figure 6.3). A few samples were also examined under the optical microscope so that a visual inspection of the respective striation patterns could be done.

Two sources of laser beams—a conventional LPKF YAG laser and the new LPKF multi-cut fiber laser—were tested in the experiments. Figure 6.4 shows an overview of the machines, and Table 6.3 summarizes the different types of laser-cut machines used to evaluate the laser cutting performance.

The next step was the EP process. The important process parameters in EP are electrolyte temperature, polishing time, current density, and the electrolyte used. At the beginning of the EP process, the cathode and anode workpiece were electrically connected by the conductive electrolyte that filled the gap between the cathode and anode. The anode was a workpiece (metallic stencil foils), and the cathode was the stainless steel (SUS304) plate. The electropolish bath consisted of a solution of H_2SO_4 and H_3PO_4 containing water. Test specimen size was 530 cm × 530 cm and EP was treated on whole surface. The EP process parameters are shown in Table 6.4.

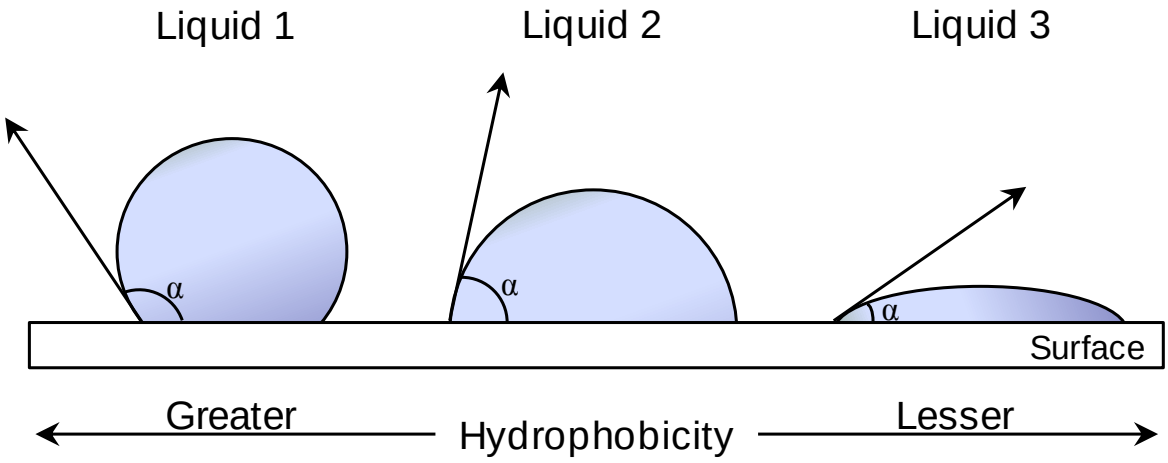


FIGURE 6.2 A schematic illustration of a various contact angles.

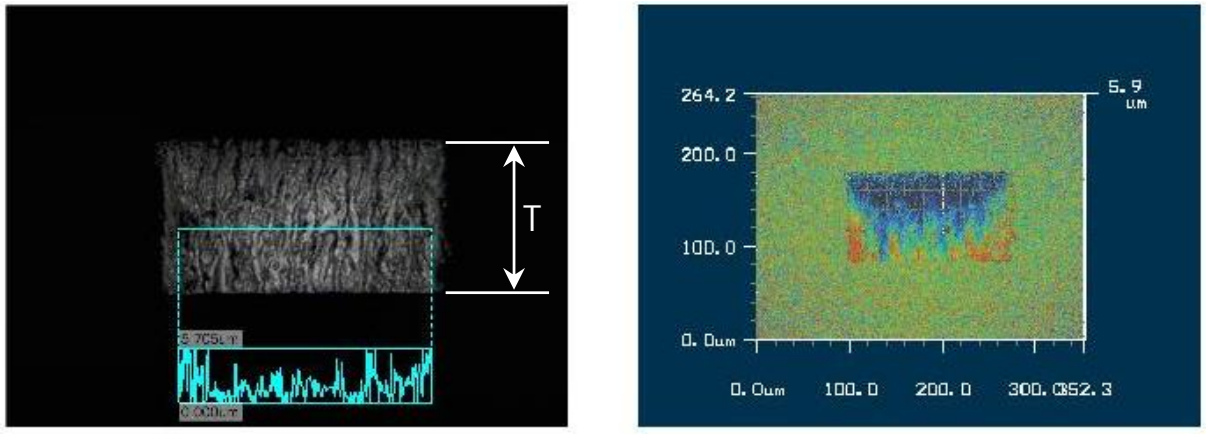


FIGURE 6.3 Measurement of surface roughness.
Note that surface roughness (*Ra*) is measured through center of material.

TABLE 6.3 Types of laser cutting system used

Laser system type	YAG laser	Fiber laser
Model	LPKF SL600	LPKF G6080
Laser beam size (*μ*m)	40	20
Cutting area (X/Y) (mm)	600 × 600	600 × 800
Laser repetition rate (kHz)	Up to 5	Up to 45
Accuracy	±10	±2
Repeatability (*μ*m)	±1	±2

FIGURE 6.4 Photographs of laser-cut system used.

TABLE 6.4 Parameters of EP

Process parameters	
Power output (DC)	380
Current (mA)	400 - 500
Voltage (V)	13
Temperature (°C)	40 - 50
EP time (s)	90 - 150
Electrolyte (wt.%)	H_3PO_4 : H_2SO_4 (95 : 5)
Electro gap (mm)	175
Tool material	SUS304 Stainless steel

6.2.2 Results and discussion

6.2.2.1 Stencil material characterizations

For many years, laser-cut stencils used 300 series stainless steel for the stencil foil material, which is a good solution for the majority of assemblies, but their paste release performance reduces considerably when printing apertures have surface area ratios below 0.66 [109]. Figure 6.5 (a) shows an example of a standard SUS304 stainless steel microstructure. The grain size of common stainless steels generally ranges from 20 to 30 μm. It was found that when SUS304 stainless steel is used, the solder would stick to the aperture walls in the stencil. This occurred because the typical size of solder powder is from 25 to 45 μm (type 3). Furthermore, because the grain size of SUS304 stainless steel was as much as 20 μm, the solder paste easily adhered to the stencil walls.

Figure 6.5 (b) shows an example of a fine-grained SUS301 stainless steel consisting of grains less than 2 μm. This fine-grained SUS301 stainless steel contains smaller and fewer voids in the material. With smaller and fewer voids, the solder paste does not adhere as easily to the stencil aperture walls. This is primarily due to the micro size of the voids that makes it more difficult for the solder paste particles to get a grip on the stencil walls. It is commonly known in both material science and technology that fine-grained stainless steels improve material properties, such as mechanical strength and uniformity [117,118]. The Hall-Petch Law states that the material strengthens as the grain size decreases [119].

In this study, the effect of stencil material on laser-cut performance was examined by comparing two microstructure grain sizes. I analyzed the stencil aperture size using the statistical process capability analysis method for characterization of laser-cut dimensional tolerance. Figure 6.6 shows histograms of the distribution of aperture dimension with a target value of 100 μm, lower tolerance limits of 90 μm, and upper tolerance limits of 110 μm for the specifications. The figure shows that the distribution is much tighter when a fine-grained SUS301 stainless steel is used than when coarse-grained SUS304 stainless steel is used. The comparison of process capability between fine-grained SUS301 and coarse-grained SUS304 stainless steels shows that the fine-grained SUS301 stainless steel had much better capability performance. The process capability (*Cpk*) values of the fine-grained SUS301 stainless steels were 1.94, whereas those of the

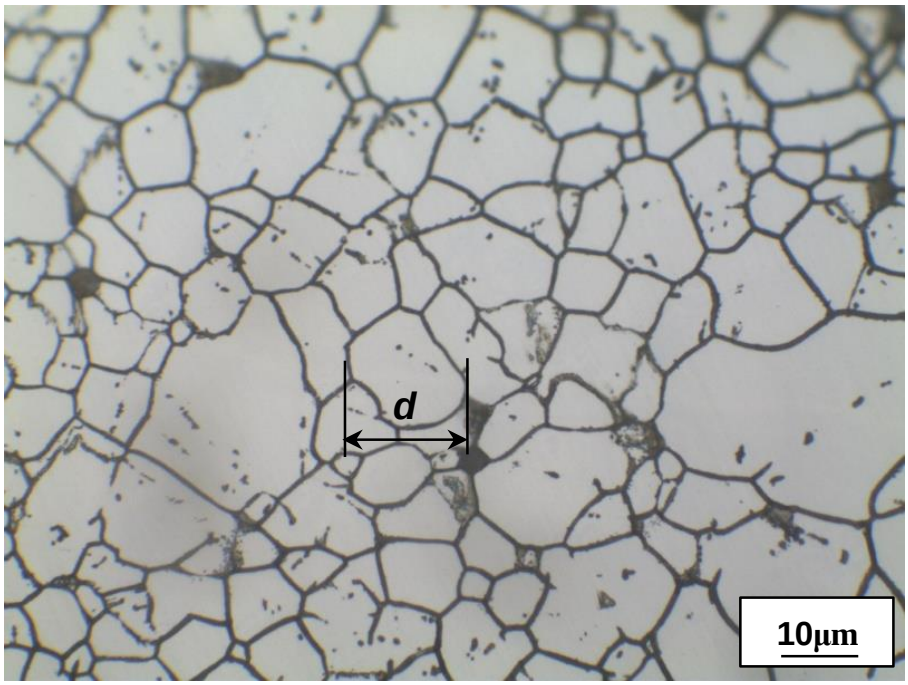
coarse-grained SUS304 stainless steels were much lower at 0.05. The cause of this discrepancy in process capability was due to the difference in the quality of the laser cut. The application of the fine-grained SUS301 stainless steel resulted in much smoother aperture walls. Thus, a more controlled printing process is achieved by using fine-grained SUS301 stainless steel for ultra-fine pitch flip-chip printing applications.

Previous researches have investigated micro cutting and the microstructure of metals [120,121]. Grum and Kisin [122] investigated the influence of the microstructure of work-piece materials on static and dynamic cutting forces. They associated the size of the soft phase in a microstructure with the dynamic component in the cutting force. The performance of mechanical machining processes is influenced by components of this microstructure, such as anisotropy, crystalline orientation, grain size, and boundaries [123,124]. Thus, the grain size of the work material plays an important role in the laser-cutting process.

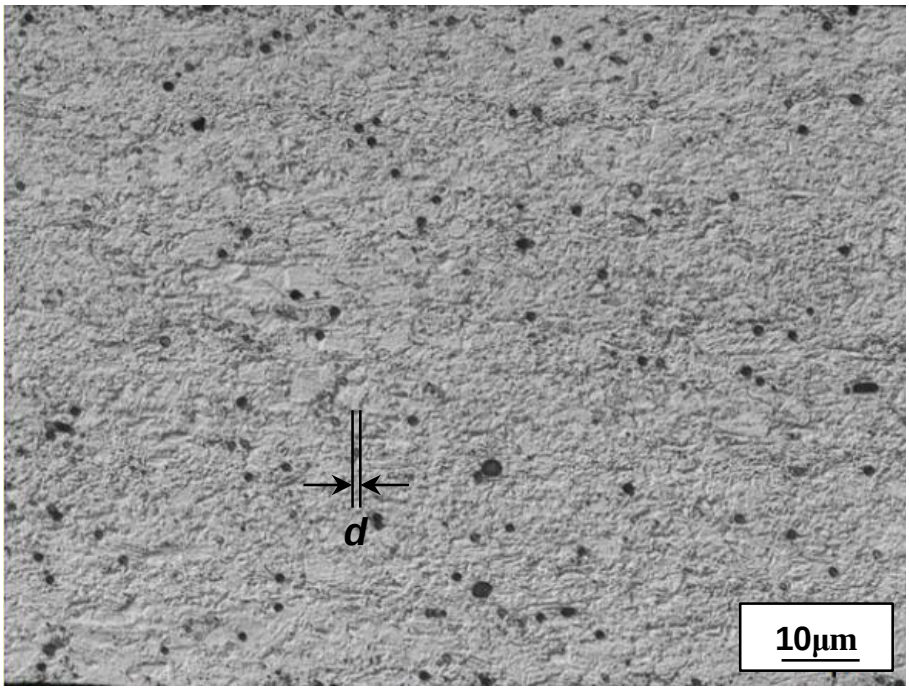
The wettability in the material surface was evaluated by measuring the contact angles. A number of tests can be applied, one being the contact angle test using a goniometer. Contact angles larger than 90° corresponded to the hydrophobic surfaces, while the hydrophilic surfaces were measured according to material grain size. The box plot shows that the fine-grained SUS301 stainless steel's contact angle (α = 83.5°) was higher than that of the coarse-grained SUS304 stainless steel (α = 60.9°), as shown in Figure 6.7. This result appears to be due to the different in the surface roughness of the two materials. The surface energy and surface tension of fine-grained SUS301 stainless steel was much lower than those of the coarse-grain SUS304 stainless steels that is, the higher the contact angle, the more hydrophobic the solid surface. The impact of surface roughness on the contact angle is given by the Wenzel equation [125], and the heterogeneous contact angle is given by the Cassie-Baxter equation [126].

For real-time observation of the fluxphobic behavior in the stencil underside, the substrate/stencil separation process was observed *in situ* with a high-speed microscope, as shown in Figure 6.8. Because water is not used as a printing medium, more viscous materials, such as flux in solder paste (flux-phobic) need to be tested and verified. The results show that the volume of flux remains on PCB pads is significantly better for the fine-grained SUS301 metallic stencil, with smaller flux residue on the stencil underside, as shown in Figure 6.8 (b). In addition, a uniform release was achieved in the stencil of the fine-grained SUS301 stainless steel. The flux

volume increase was strongly related to the contact angles between the different surface characteristics of the two materials. In addition, there might be a difference in surface tension between the PCB pads and the fine-grained SUS301 metallic stencil, which might have higher surface tension. Therefore, the fine-grained SUS301 metallic stencil foil with the higher contact angle is highly desirable for ultra-fine pitch structures.



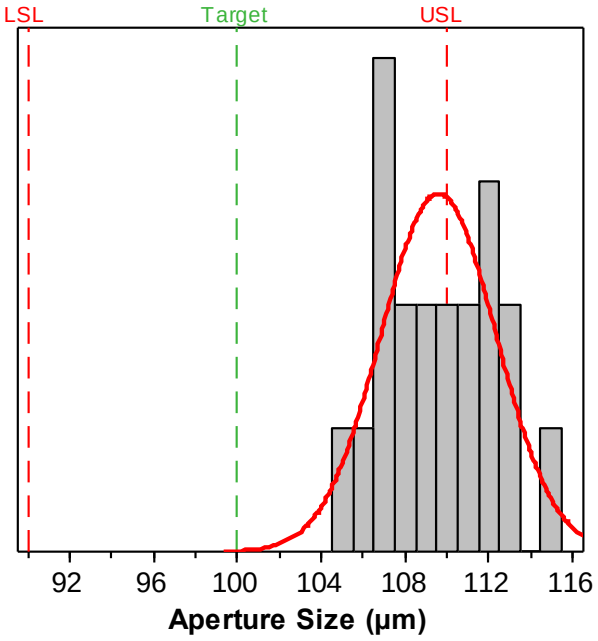
(a)



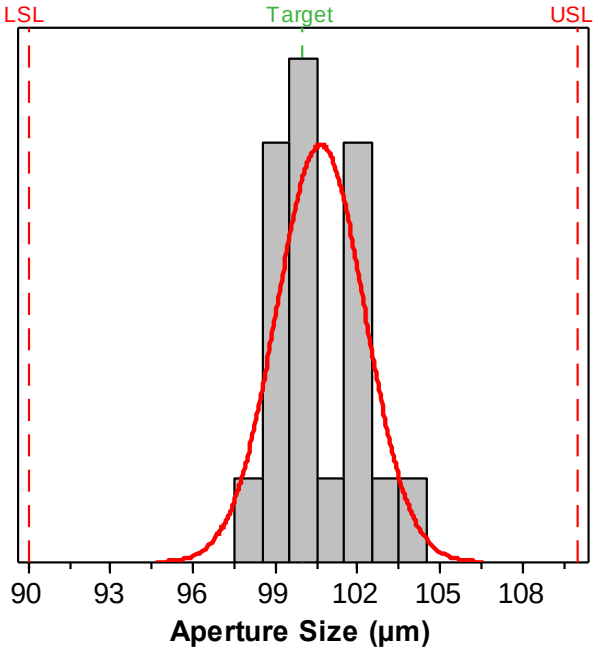
(b)

FIGURE 6.5 Microstructure of stainless steel used.

Notes: (a) Coarse-grained SUS304 stainless steel; (b) fine-grained SUS301 stainless steel.



(a)



(b)

FIGURE 6.6 Process capability plot.

Notes: (a) Coarse-grained SUS304 stainless steel (*Cpk* = 0.05); (b) fine-grained SUS301 stainless steel (*Cpk* = 1.95).

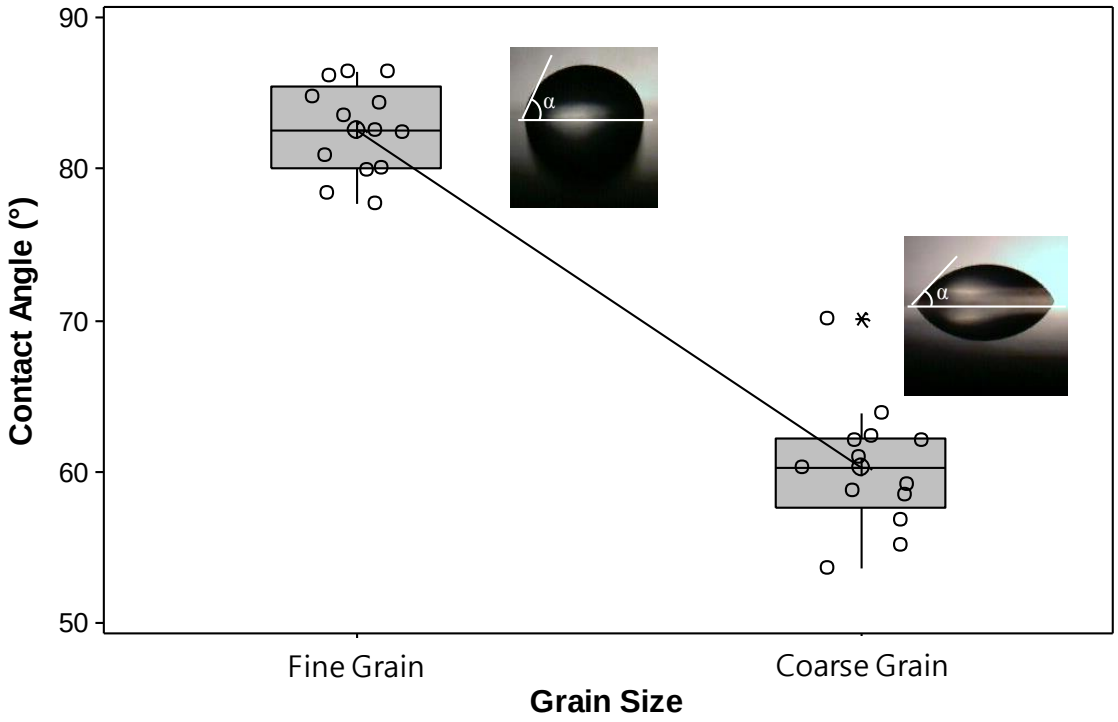


FIGURE 6.7 Relationship between grain size of stainless steel and contact angle.

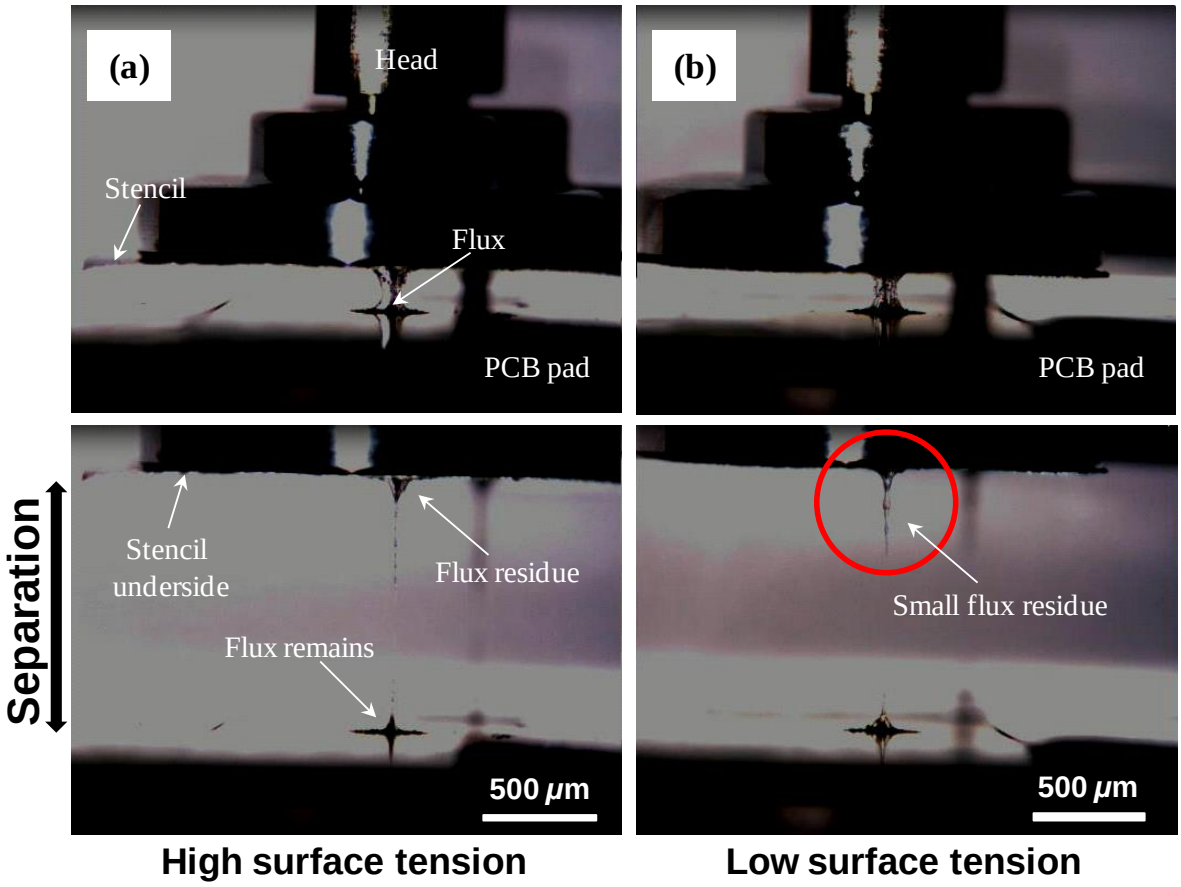


FIGURE 6.8 High-speed microscope images of substrate/stencil separation process.

Notes: (a) Coarse-grained SUS304 stainless steel; (b) fine-grained SUS301 stainless steel.

6.2.2.2 Stencil fabrication process analysis

Experiments were conducted using various material types, laser types, cutting speeds, and EP time. The output parameter, such as surface roughness, was measured. The experimental results were analyzed to study the influence of different factors on laser-cutting performance.

The effect of material type was evaluated. The laser-cutting speed was 15 mm/s and all samples were electropolished for 120 s. Figure 6.9 shows the stencil aperture wall with conventional SUS304 stainless steel and fine-grained SUS301 stainless steels after the laser-cutting. Remarkable difference was observed in the surface texture. The wall texture of fine-grained SUS301 stainless steel is extremely smooth compared to the conventional SUS304 stainless steel. In addition to improved paste release for smaller apertures and much cleaner paste release through the entire stencil, the finer grained structure of these materials also produces a more highly defined aperture edge when cut with a properly turned laser beam. Figure 6.10 shows the box plot of the average surface roughness versus each stencil material type. The box plot of the performance of the novel SUS301 stainless steel with fine grain size shows that the *Ra* value was lower than that of the conventional SUS304 stainless steel with coarse grain size. This may be due to the fine-grained microstructure structure can be reduced cutting defects of the laser process, the sharp cut edge of the aperture, uniform surface microstructure, dimensional consistency and is conducive to mass production. For a solder stencil printing process, the smoothness of the stencil aperture wall is a vital component of a high performance stencil allowing printing of smaller apertures without reducing the foil thickness.

Figure 6.11 shows the box plot of the average surface roughness versus each laser system type. The box plot of the performance of the new fiber laser system shows that the *Ra* value was lower than that of the conventional YAG laser system. The YAG laser system has the advantages of high flexibility and high speed; moreover, it is able to cut very small apertures. However, its disadvantage is edge quality. In the YAG laser system, the smallest diameter laser beam possible was approximately 40 μm. While this diameter laser beam is fine for the majority of stencil designs, the energy density with a 40 μm beam diameter is not high enough to produce the smoothest aperture walls possible in cutting stencil apertures for fine pitch structures ($\leq$ 200 μm pitches).

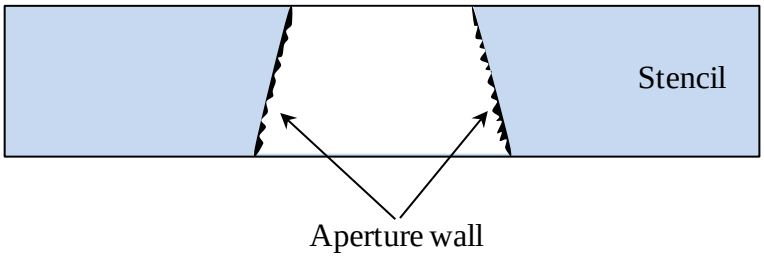
Recently, diode-pumped fiber lasers were developed [127]. These lasers are doped plastic or glass fibers that are end- or side-pumped by diode lasers. Fiber lasers produce shorter pulse widths and higher frequencies. They produce a smaller laser beam diameter of 20 μm with a corresponding four-fold increase in energy density. This increase in energy density significantly increases the ability of the laser beam to cut through the metal, and the result is a much smoother aperture wall (Figure 6.9). The diode pumped new fiber laser has a beam quality 10 times better than that of the standard YAG laser. Finally, the edges obtained with this new laser process are almost perfect, producing the lowest taper angle yet (Figure 6.12). The results showed that the tapered angles were 2.5° and 0.7° for the standard YAG laser and the diode-pumped fiber laser, respectively. The tapered angle was determined by the following equation:

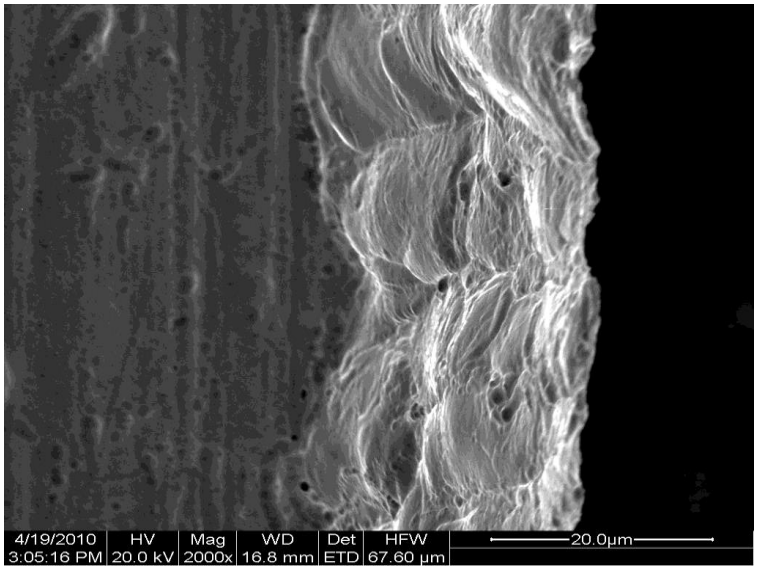
$$A = \tan^{-1} ((d1-d2) / 2 \times t)$$

where *d1* and *d2* are the aperture sizes at the entrance and exit, respectively, and *t* is the stencil thickness.

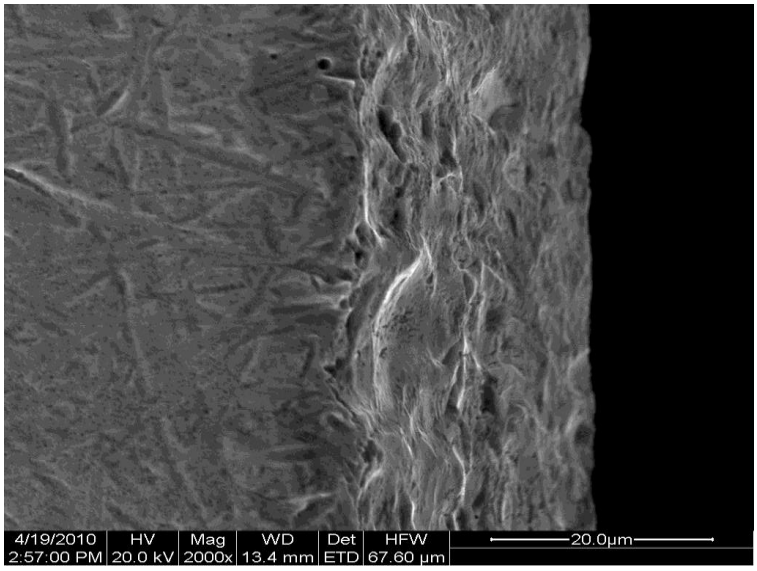
The effect of cutting speed was also evaluated. Figure 6.13 shows the variations in average surface roughness according to different cutting speeds. Generally, the average surface roughness of fine-grained SUS301 stainless steel decreases as the cutting speed increases. In this experiment, the surface roughness of the fine-grained SUS301 stainless steel is at maximum when the cutting speed is 3 mm/s. Conversely, the surface roughness gradually decreases when the cutting speed increases to 10 mm/s. It attains minimum roughness as the cutting speed increases to maximum at 15 mm/s. A correlation has been established between surface roughness (or smoothness) of the aperture cut edge with laser-cutting speed. From the figure the surface roughness can be seen to be inversely proportional to the cutting speed. At very low speed (3 mm/s), the cut edge of aperture wall is rougher than that shown at high speed (15 mm/s). This may be due to overheating caused by the metal-oxygen reaction when the reaction may propagate beyond the area which is already heated by the laser beam. These results are consistent with the results of Neimeyer *et al.* [150] who have reported that at low speeds, the oxidation reaction front moves more quickly than the laser traversed cutting speed. As cutting speed is increased, the laser moves faster than the oxidation front, providing more continuous heat and a smother surface.

This study also evaluated the effect of the surface finish. Previous research indicated that EP is usually provided to smoothen the surface finish of the stencil aperture walls [71]. For comparison, I investigated the EP on stencil apertures using an acid based solution (95 wt% H_3PO_4: 5 wt% H_2SO_4), as described in Chapter 4. Figure 6.14 shows the relationship between average surface roughness and EP time. The electric current used for the EP was 400 mA. The electrolyte temperature was 40°C, and the samples were electropolished for 90, 120, or 150 s. The laser-cutting speed was 15 mm/s. The surface roughness decreased sharply after the EP time was increased beyond 90 s. The results showed that aperture smoothness is improved by increasing the EP time, and 120 s of polishing time resulted in minimal surface roughness. Hence, the graphs shown in Figures 6.11 to 6.14 clearly show that when the diode-pumped new fiber laser system was used, higher cutting speed and longer EP times reduced the surface roughness of the fine-grained SUS301 stainless steel.





(a)



(b)

FIGURE 6.9 SEM images of stencil aperture wall for each material type.

Notes: (a) Coarse-grained SUS304 stainless steel; (b) fine-grained SUS301 stainless steel.

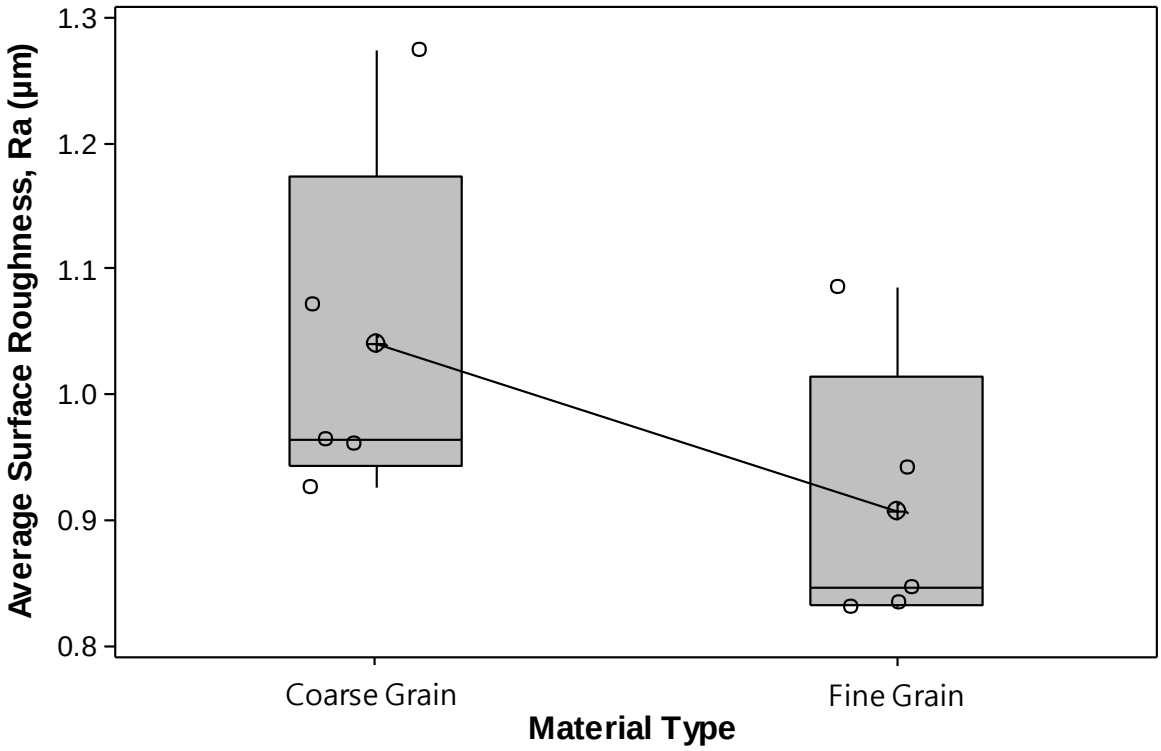


FIGURE 6.10 Relationship between grain size of stainless steel and surface roughness (*Ra*).

Note: The box plot shows the smallest value, the first quartile, the median, the third quartile, and the largest value.

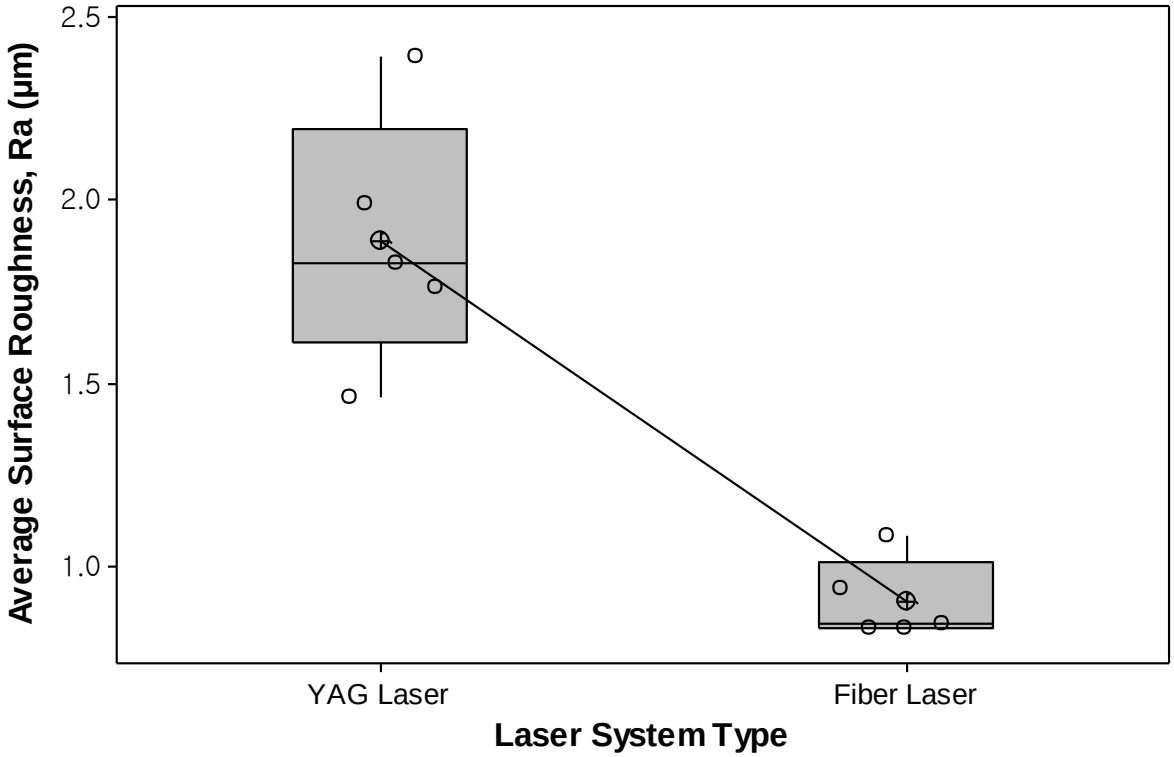
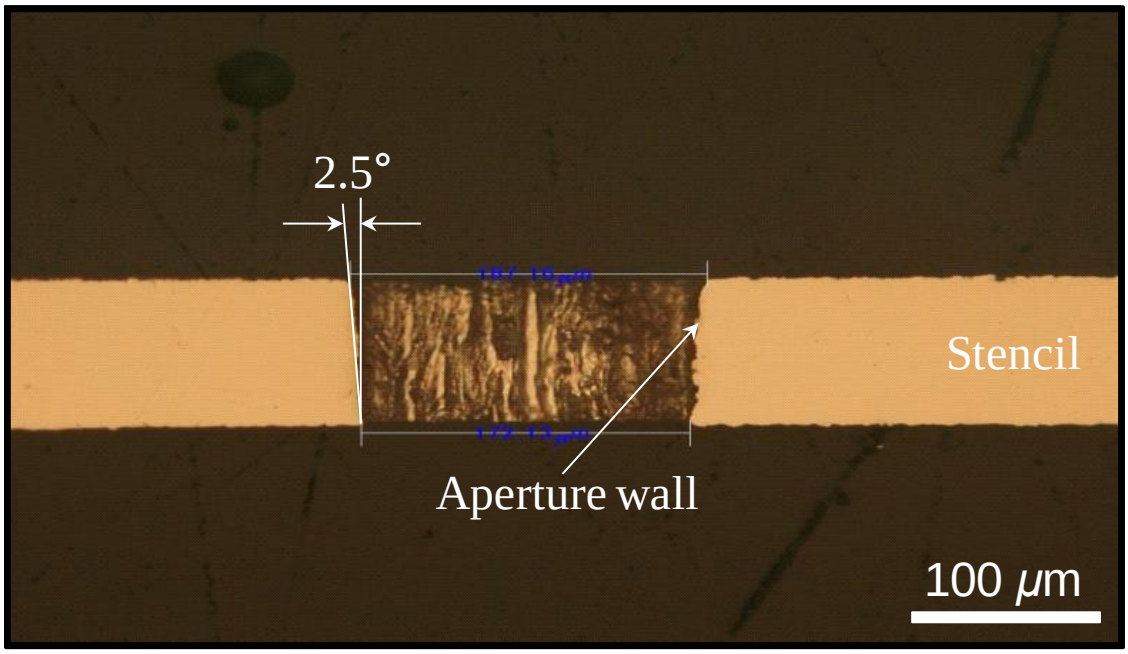
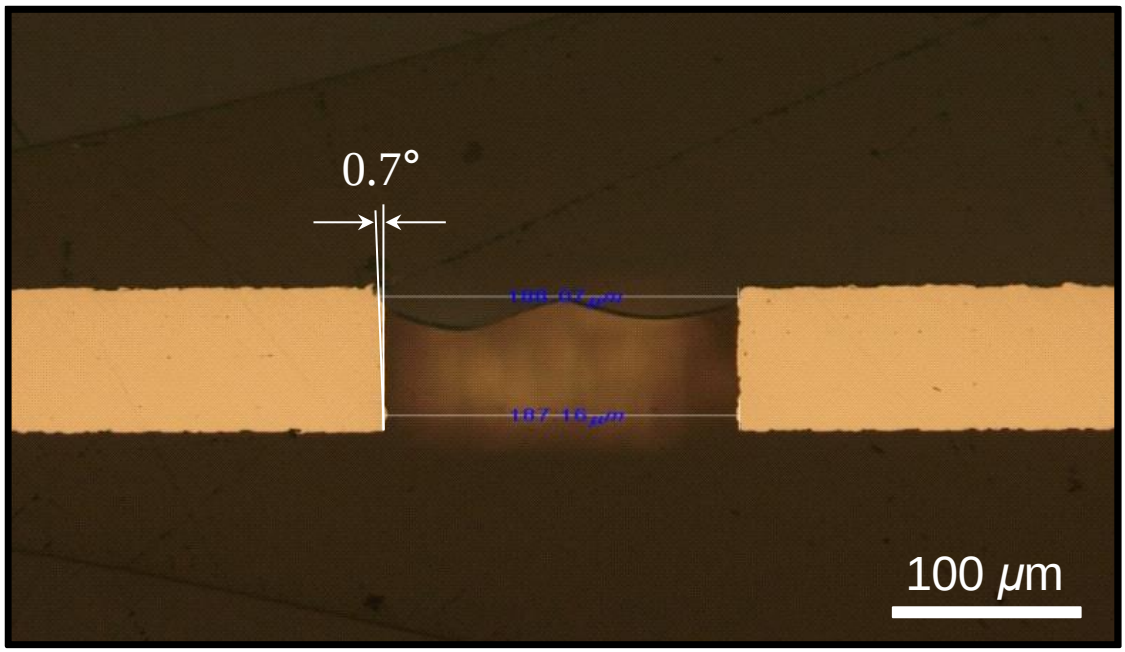


FIGURE 6.11 Relationship between laser system type and surface roughness (*Ra*).

Note: The box plot shows the smallest value, the first quartile, the median, the third quartile, and the largest value.



(a)



(b)

FIGURE 6.12 Comparison of tapered stencil wall apertures.

Notes: (a) The standard YAG laser; (b) the diode-pumped new fiber laser.

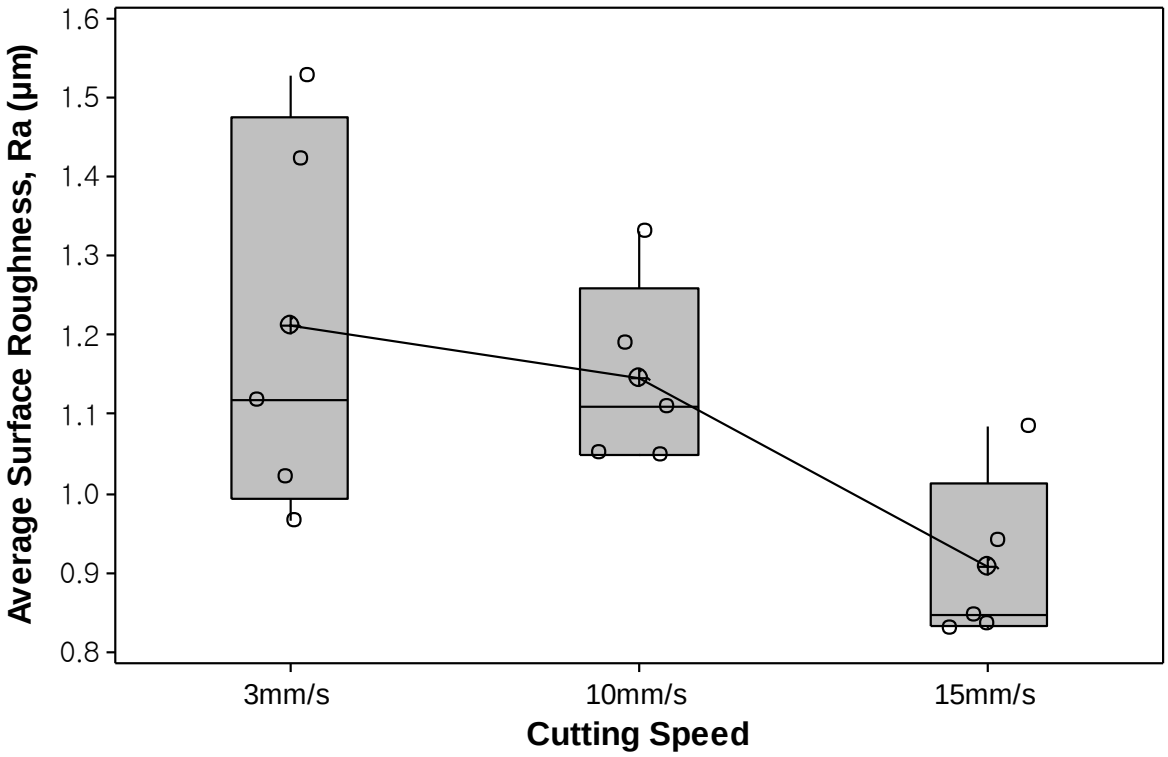


FIGURE 6.13 Relationship between laser cutting speed and surface roughness (*Ra*).

Note: The box plot shows the smallest value, the first quartile, the median, the third quartile, and the largest value.

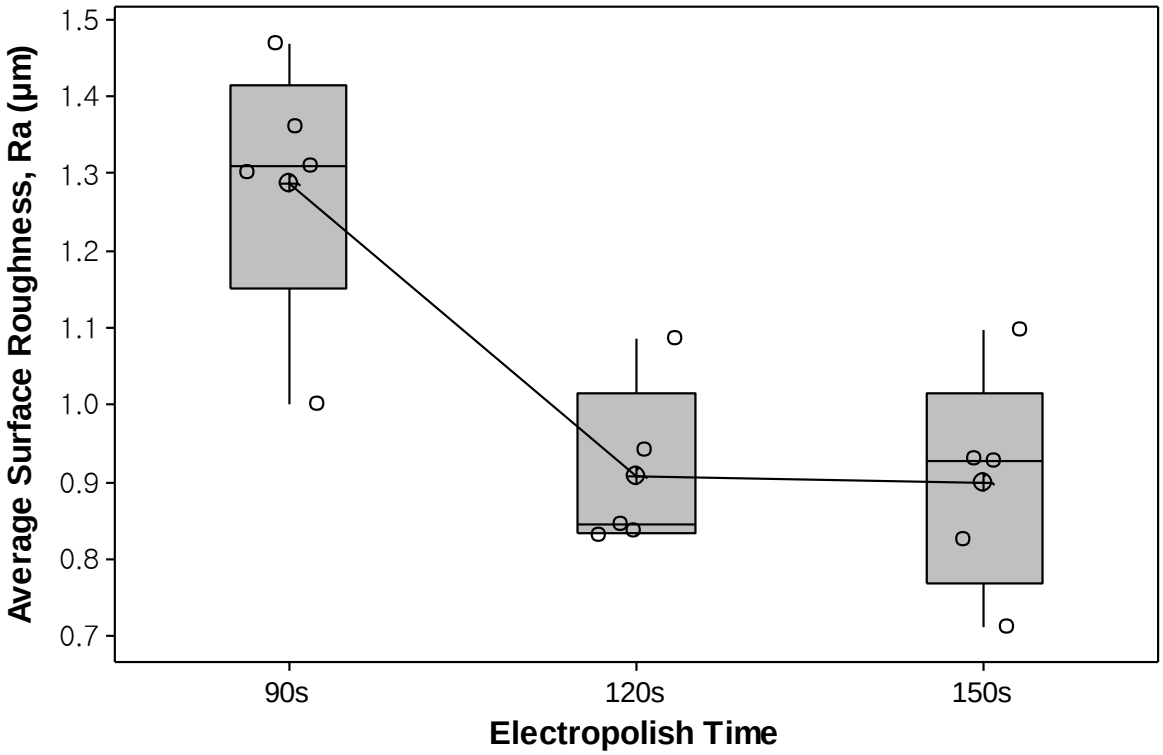


FIGURE 6.14 Relationship between EP time and surface roughness (*Ra*).

Note: The box plot shows the smallest value, the first quartile, the median, the third quartile, and the largest value.

6.3 Flip-chip assembly and SMT process

When developing the low cost flip chip-on-board assembly process, I focused on SMT process compatibility. Indeed, this process fits smoothly in a standard SMT assembly line, as shown in Figure 6.15.

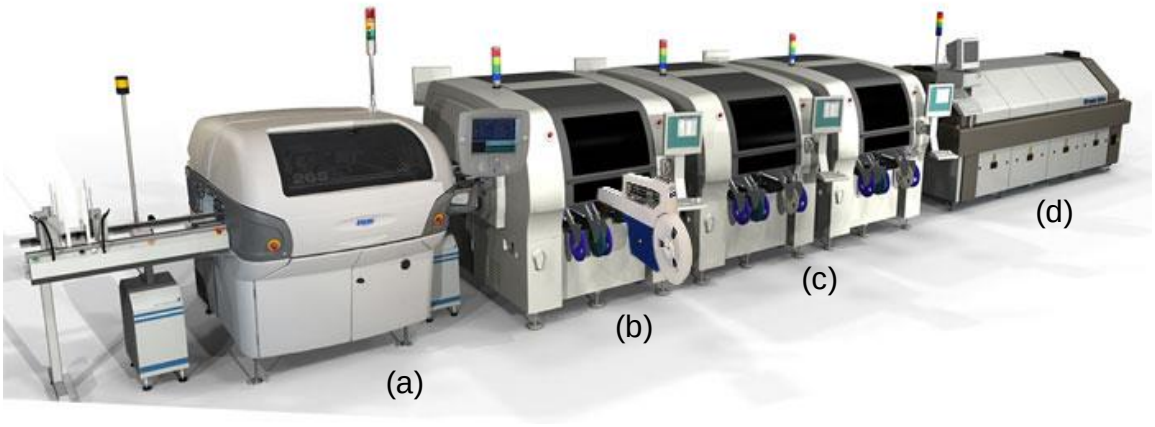


FIGURE 6.15 Investigation of flip-chip assembly in the SMT process. The tools depicted in the photograph are: (a) screen printer, (b) pick-and-place machine #1, (c) fine-pitch pick-and-place machine #2, and (d) reflow oven. (SOURCE: Universal Instrument Corporation)

6.3.1 Experimental

6.3.1.1 Test vehicle

This study used the silicon wafer substrate with standard wafer-level packaging manufacturing techniques. The test vehicle was a 25 mm × 25 mm module 0.3 mm in thickness. The test vehicle incorporated the standard SMT components, mainly BGA, QFN, WLP, and flip-chip. The pitch varied from 150 μm to 800 μm. Detailed information about the flip-chip device is given in Table 6.5. The top-layer design of the test vehicle is shown in Figure 6.16. The solder pads were solder-mask-defined for the flip-chip pads and the pad dimensions are shown in Figure 6.17. The other components dimensions are presented in Table 6.6.

6.3.1.2 Materials and methods

Both type 6 and type 7 water-soluble 96.5wt.%Sn–3.0wt.%Ag–0.5wt.%Cu (SAC305) solder pastes were used in the present study (Tamura Co.). The metal content in both pastes was 89 percent. According to the vendor specifications, the solder powder size in type 6 was in the range of 5 μm to 20 μm in diameter, whereas the corresponding powder size in type 7 was in the range of 1 μm to 12 μm. Figure 6.18 shows the appearance of the solder powder taken by SEM photography. The stencil printing process was carried out using an MPM Excel printer with a metal squeegee angled at 60° fitted to the printer. The solder-deposited silicon substrate was inspected using a microscope equipped with a digital camera to provide photographical documentation.

A nine-zone Heller 1800 convection oven was used to reflow the devices with a typical lead-free reflow profile and a nitrogen atmosphere. The peak temperature was 239 °C; the time above 220 °C (the solder melting point) was 46 s. Due to the thin silicon substrate, all process steps were performed on specially designed carrier follow the silicon substrate through all steps of the process [128].

After the components were assembled, a flexible-printed-circuit (FPC) interconnection was performed using the semi-auto hot bar soldering method. Deflux cleaning of the residue was then performed with an ultrasonic cleaner.

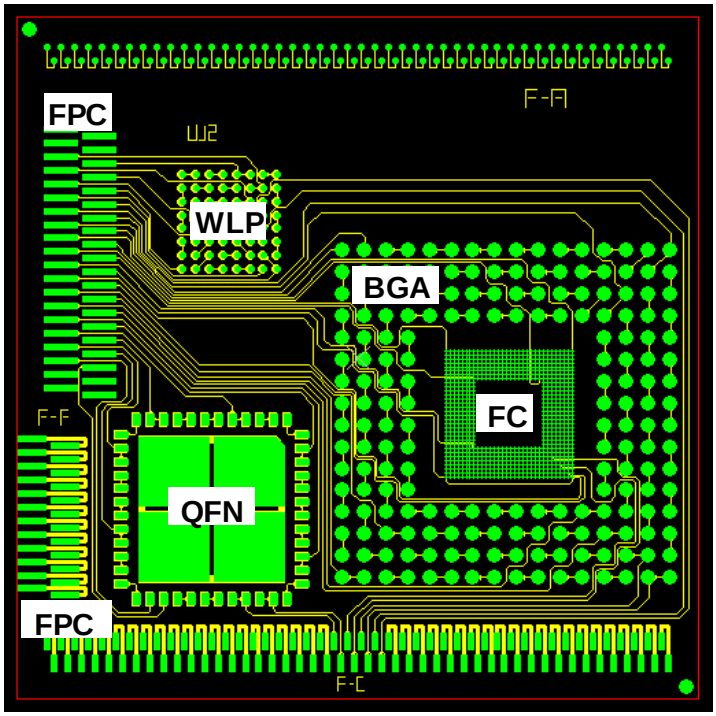
After all SMT processes and electrical testing, a Hanmi HP-120 transfer mold system was used with a molded-underfill (MUF) epoxy mold compound (Cheil Industries, SG-8500UBX). Epoxy mold compound (EMC) was prepared with the maximum particle size below 20 μm cut and 78wt.% content. The standard post mold cure temperature of 175 °C was applied to all strips. Bump pitches for the test vehicle ranged from 150 μm to 800 μm, which shrank rapidly in the majority of products. Hence, MUF material should be capable of filling fine gaps without trapping voids under the flip-chip die, which otherwise could result in an assembly yield loss, or worse, a latent failure during board assembly or in the market. All the completed assemblies were inspected using an x-ray inspection system. Figure 6.19 shows the process flow chart for the silicon substrate assembly with the FCOB attachment.

TABLE 6.5 Flip-chip device information

Items	Dimension
Die size (mm)	5 × 5
Bump pitch (*μ*m)	150
Bump height (*μ*m)	20-30
Bump diameter (*μ*m)	110
No of bumps	768
Bump composition	96.5wt.%Sn-3wt.%Ag-0.5wt.%Cu (SAC305)
UBM diameter (*μ*m)	100

TABLE 6.6 Component dimension in test vehicle

Items	BGA	QFN	WLP
Pitch (*μ*m)	800	500	500
Pad pitch (*μ*m)	480	270 × 470	270
SR opening (*μ*m)	460	250 × 450	250



(a)

(b)

FIGURE 6.16 Test board layout showing schematic with mounted components.

Notes: (a) Test vehicle design; (b) assembled silicon substrate.

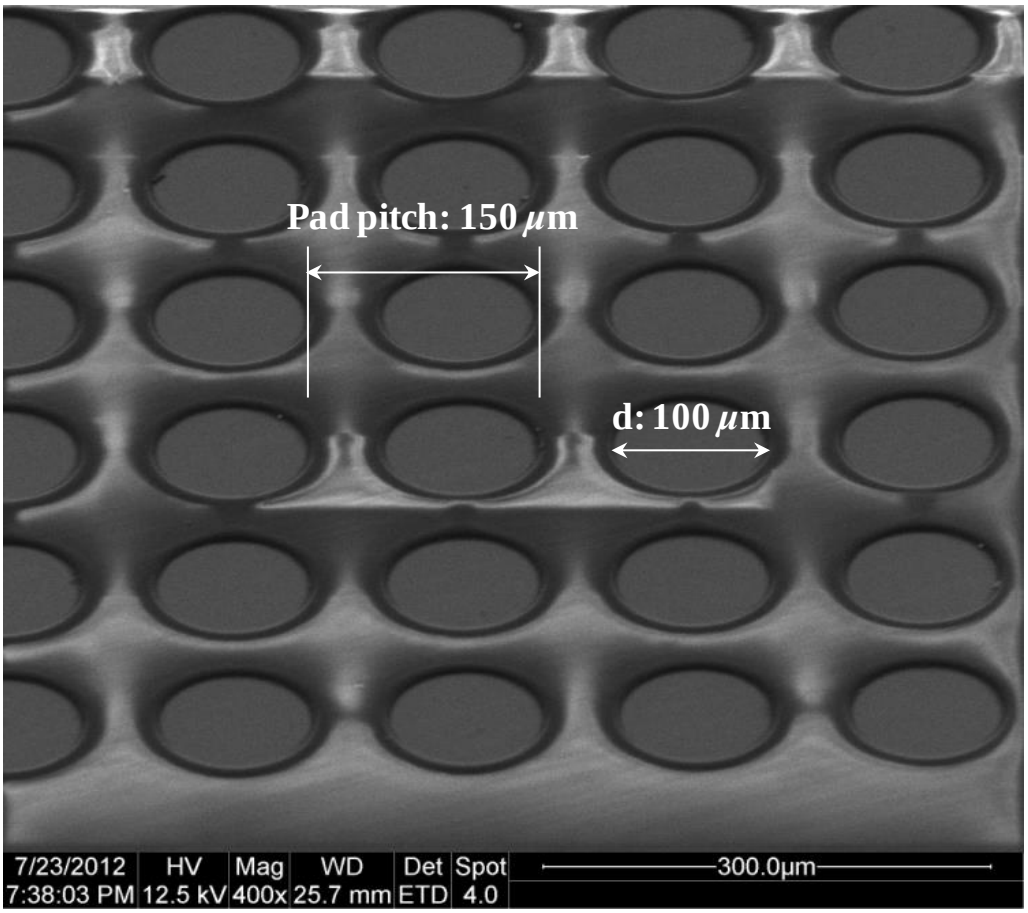
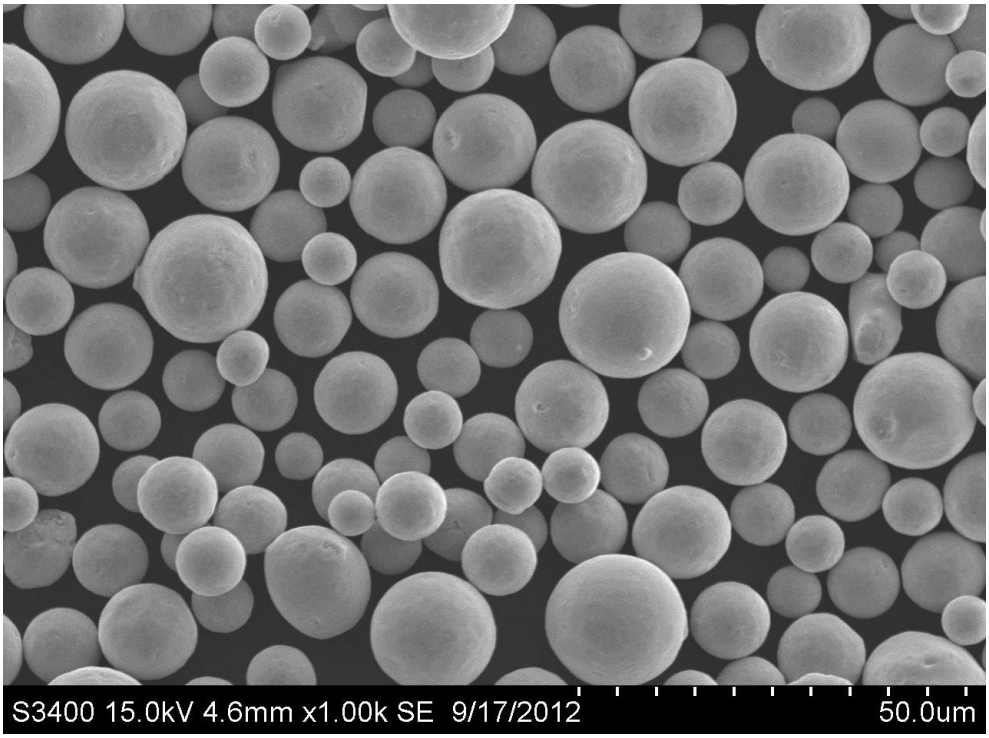
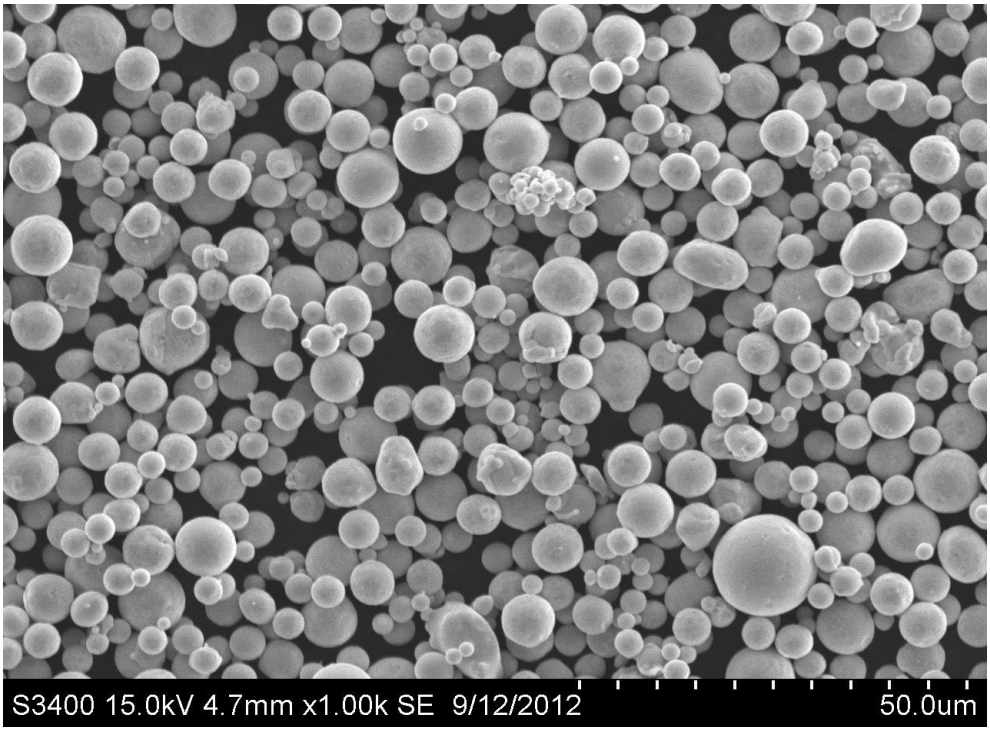


FIGURE 6.17 SEM image of flip-chip pads on silicon substrate.



(a)



(b)

FIGURE 6.18 SEM photograph of solder powder.

Notes: (a) Type 6; (b) type 7.

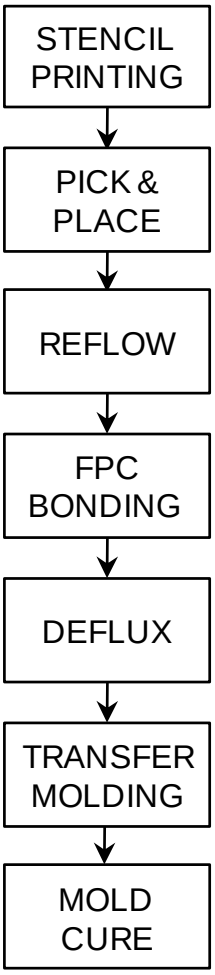


FIGURE 6.19 Process flow for the assembly of silicon substrate.

6.3.1.3 Design of the experiments

An experimental design approach was followed to determine the optimum solder paste printing process. The factors considered were the solder paste type, print speed, and print force. A full factorial design required 18 experimental runs (2 levels of solder types × 3 levels of print speeds × 3 levels of stencil forces). Two replicates were carried out for each experimental run. Thus, 36 test vehicles were fabricated in this study. The response variables were the volume of the deposited solder paste. The factors and their levels are shown in Table 6.7.

TABLE 6.7 Factors and levels for experiments

	Level		
Factor	**Low**	**Middle**	**High**
Solder paste type	-	Type 6	Type 7
Print speed (mm/s)	40	60	80
Print pressure (MPa)	0.8	1.2	1.6

6.3.2 Results and discussion

The results of the design of experiment (DOE) factors of solder paste type, print speed and print force are discussed in this section. An inline inspection machine was used to measure the print volume of the solder paste deposited for each experimental run.

The main effect of the three factors on the solder volume is shown in Figure 6.20, which shows that the volume of the solder paste deposited is maximized when type 7 solder paste is printed at a print speed of 40 mm/s with a print force of 1.6 MPa. The plots show that the average solder print volume increases with the increase in print pressure and decrease in print speed. Thus, the solder sphere size and print pressure are the most important factor.

The paste release behavior for the different types of paste size was studied in 150 μm pitch flip-chips. Figure 6.21 shows some representative SEM images from the solder deposition on the substrate pads for different paste types, such as type 6 and type 7. Paste size had a significant effect on paste release and, hence, paste volume and coverage. Type 7 solder paste released more quickly than type 6 pastes. When a type 6 solder paste was used, printing defect, such as insufficient solder, was generated [Figure 6.21 (a)]. Type 7 paste has a smaller particle size, which gives better paste release performance and aids in depositing more solder volume onto the pads. Therefore, to obtain the best and most repeatable volume of solder paste in a stencil printing of 150 μm pitch flip-chips, the particles required a smaller mesh paste, which is found in type 7 solder paste, although type 6 solder paste is typically used in wafer bumping applications.

In addition, solder paste printing with type 7 paste yielded good print deposits for all test fields in the stencil. Specifically, paste rolling was adversely affected by the relatively high viscosity and tackiness of the paste but the selected higher squeegee angle (60°) and adjustments of the print speed and force improved the printability of the paste.

Pads printed with both type 6 and type 7 pastes were reflowed in order to derive comparative information about paste performance. Bump height measurement was performed by the cross-section method. Figure 6.22 shows a box plot of the bump height for each solder paste type. Type 7 paste exhibits bump height that is approximately 35 percent higher than that by type 6 paste. This result is because type 7 paste has a better paste release performance. The paste print image (Figure 21) clearly shows that type 7 paste gave a more consistent, higher

volume print than did type 6 paste. The typical average height of reflowed solder bumps was 95 μm at pitches lowered to 150 μm (Figure 23).

All units were subsequently subjected to thermal cycling between -40°C and 85°C. A ramp rate of 10°C/min was used, and the dwell time at each extreme was 30 min. Electrical testing and visual inspections were performed at room temperature in intervals of 200 cycles. No additional failures were observed, even after 1,000 cycles. As shown in Figure 6.24, the mean and the range of the resistance of solder joints on the flip-chip device indicate that solder interconnects did not show significant changes in joint resistance. The failure of an assembled flip-chip die was defined as its resistance increased by 10 percent over its initial resistance. Cross-section analysis was used to determine whether cracks occur in solder joints with an increase of more than 2 Ω. Figure 6.25 presents the cross section of an assembly for a 150 μm pitch flip-chip device.

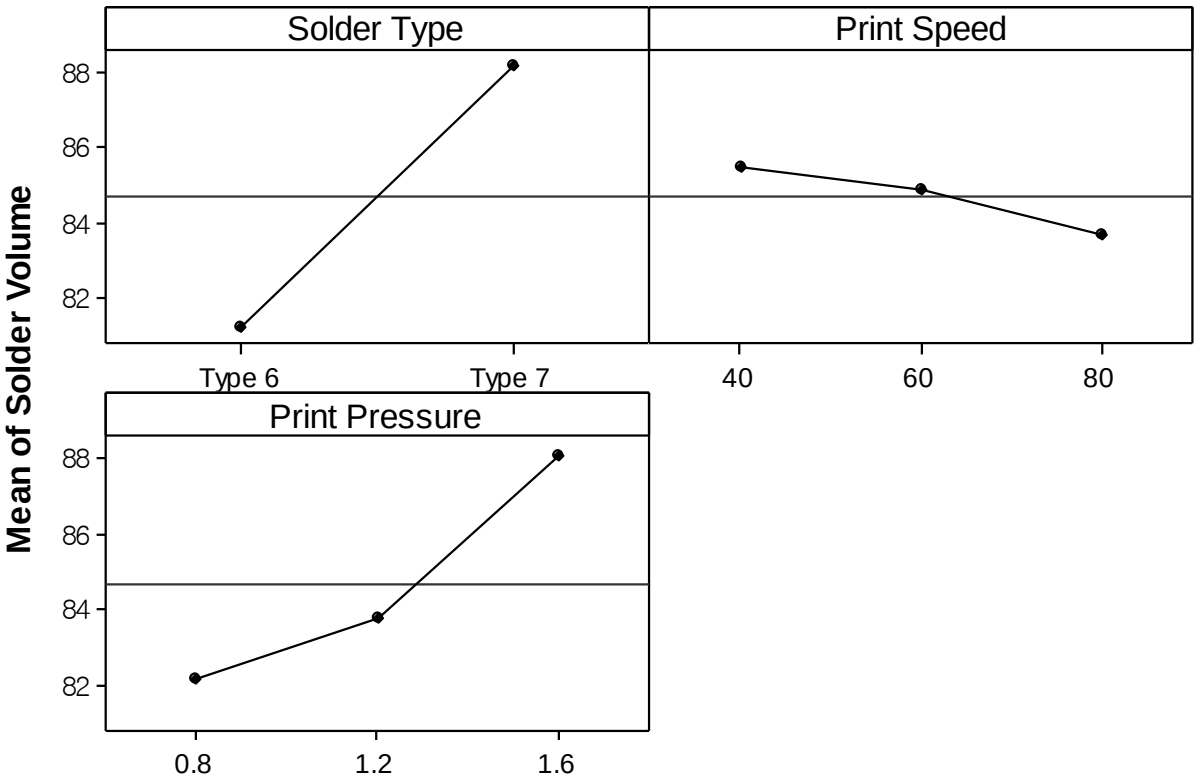
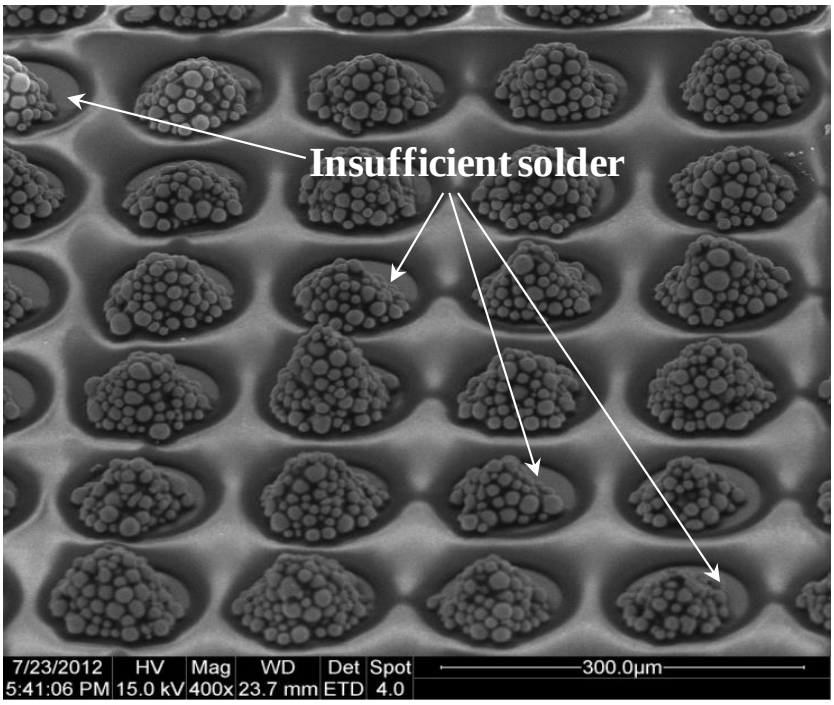
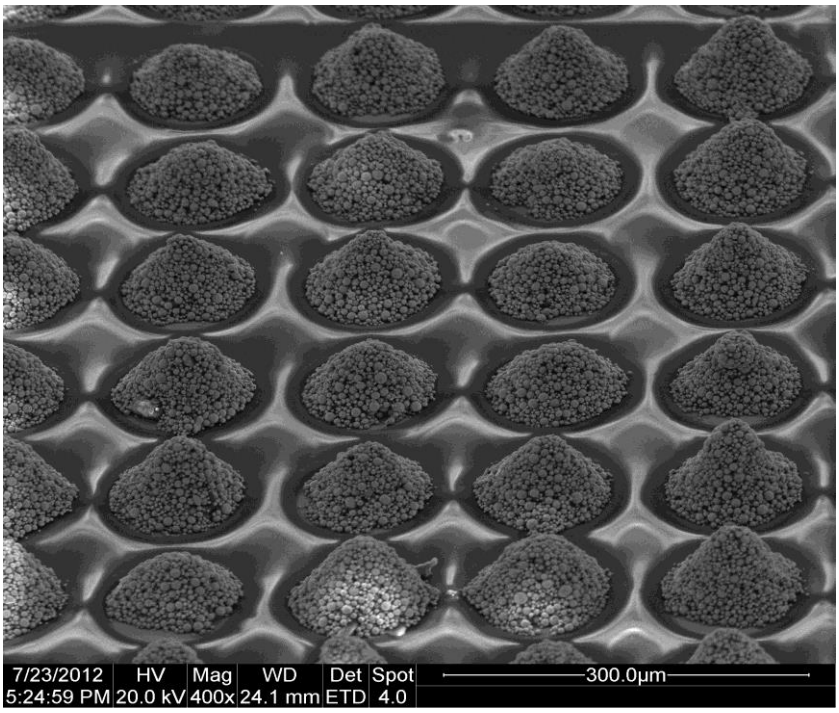


FIGURE 6.20 Main effects plot for solder volume.



(a)



(b)

FIGURE 6.21 SEM images of solder deposition on 150 μm pitch flip-chip pads for each solder paste type. Insufficient solder paste deposit, indicated by the arrows.

Notes: (a) Type 6; (b) type 7.

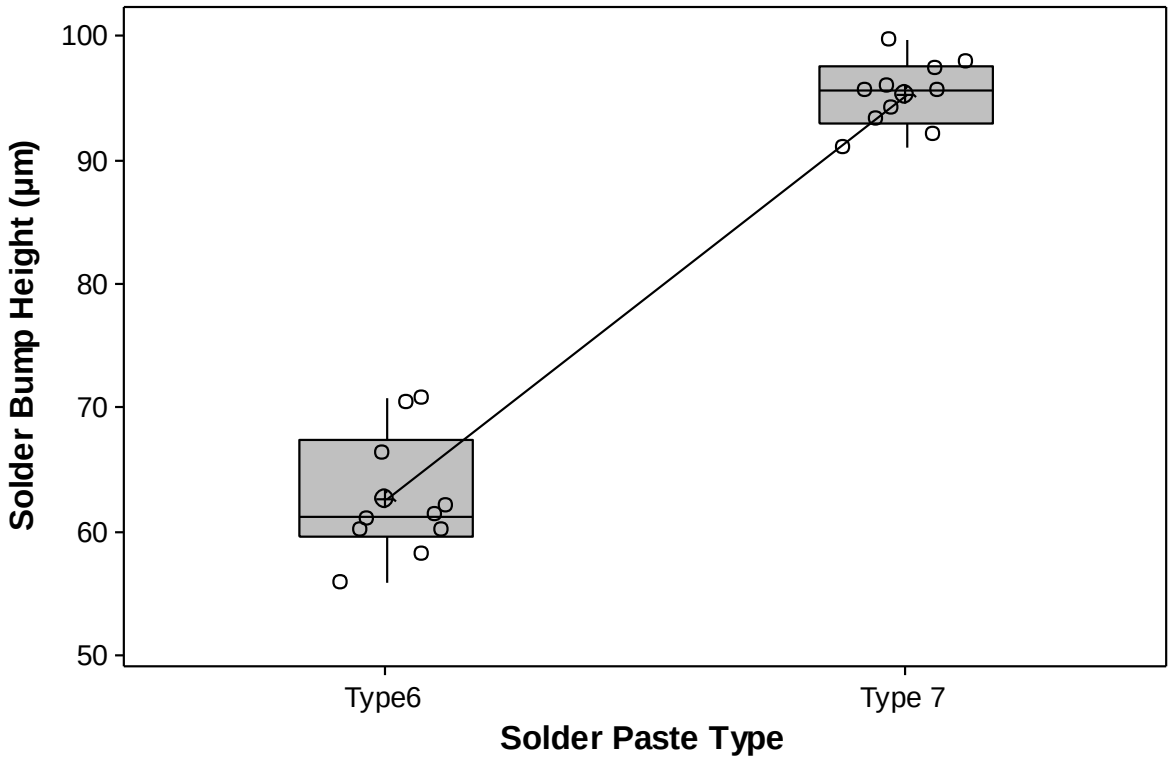


FIGURE 6.22 Solder bump height comparison for each solder type.

Note: The box plot shows the smallest value, the first quartile, the median, the third quartile, and the largest value.

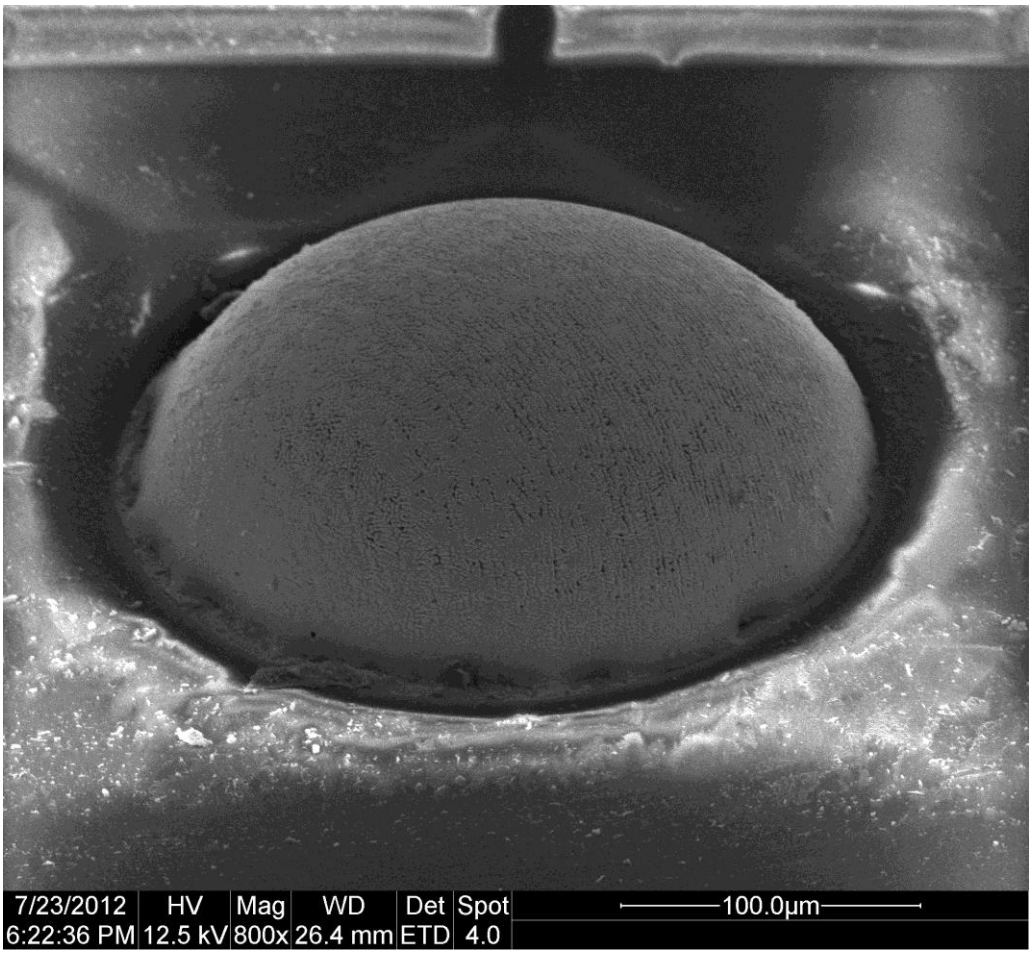


FIGURE 6.23 SEM image of solder bump on silicon substrate pad, average bump height 95 μm, pitch 150 μm.

Note: Print of type 7 paste on pads. Original magnification X800.

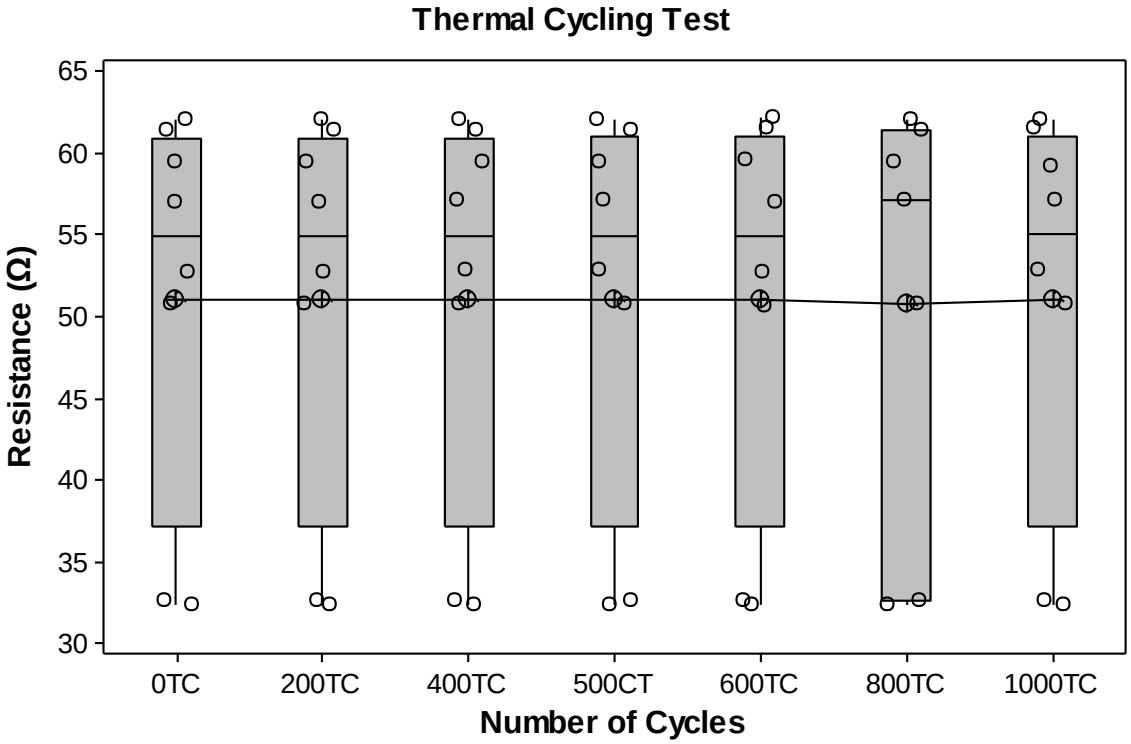


FIGURE 6.24 Resistance changes throughout the thermal cycling test.

Note: Flip-chip device with type 7 paste.

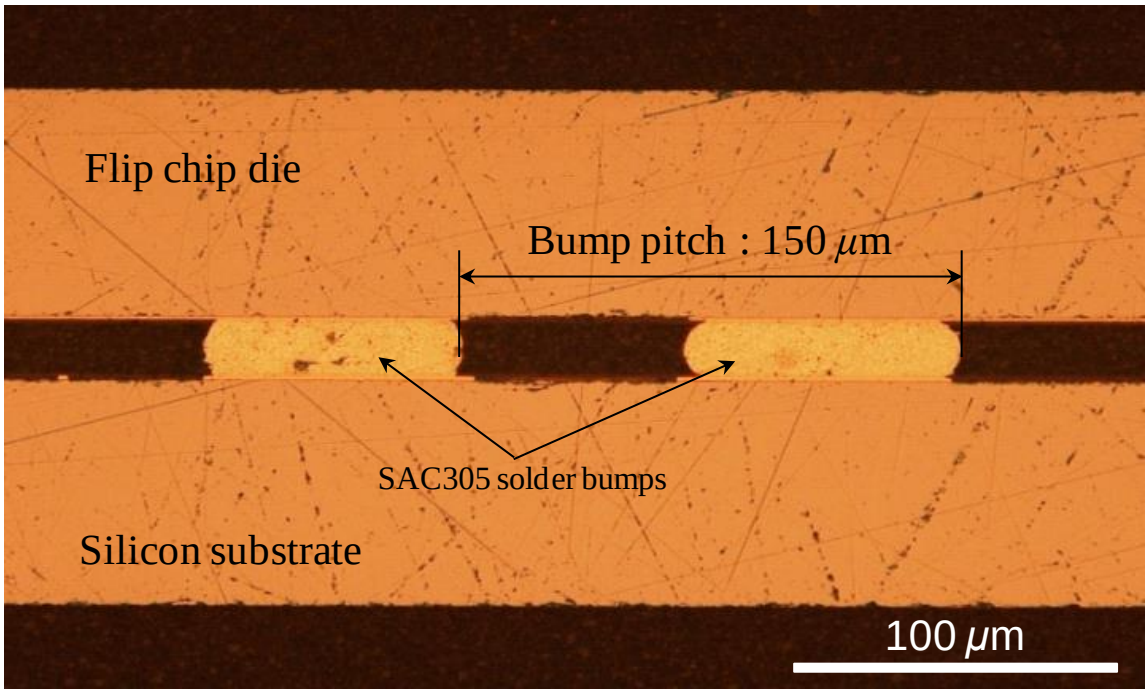


FIGURE 6.25 Cross-section of MUF and over molded FCOB assembly. Note that cross-sectioning picture showing good solder joint formation.

6.4 Summary

In light of the rising demands for finer pitch interconnection, coupled with the need for more cost-effective processing, existing SMT infrastructure and associated materials are extended to provide next generation solutions.

This study investigates the influence of stencil manufacturing parameters on the surface roughness of aperture walls. The fine-grained SUS301 stainless steel exhibited superior performance, indicating that the grain size of stainless steels has a significant effect on aperture dimensional tolerance.

Results of the novel stencil technology showed that the fine-grained SUS301 metallic stencil indicated a substantially less contaminated assessment in comparison to the alternative stencils. Finer stencil structures over a higher number of print cycles are reproducible and remain printable without cleaning the stencil, which results in a high throughput of PCBs in the printing process. In this study, the fine-grained SUS301 metallic stencil had an acceptable paste volume at a surface area ratio of 0.45. In contrast, the surface area ratio limits are 0.5 and 0.66 for electroformed stencils and laser-cut stencils, respectively.

Type 7 solder paste with a smaller sphere size was observed to produce good results in terms of a better solder paste deposition on the pads. Solder paste deposit volumes can also be controlled by optimizing appropriate printer parameters, such as stencil speed and print force.

This study demonstrated that fine-grained metallic stencil printing is a strong alternative to electroformed stencil technology for fine-pitch flip-chip packaging applications.

PART IV: HIGH-DENSITY SUBSTRATE AND ASSEMBLY DEFECTS

Chapter 7

The effect of micro via-in-pad designs on tombstoning defect[6,7]

The purpose of this work is to propose a solution procedure to minimize/eliminate tombstoning defects in small chip components with different micro via-in-pad designs for high density module assembly. Four different micro via-in pad designs were compared (via-hole diameter): ultra-small via-in-pads (10 μm), small via-in-pads (20 μm) and large via-in-pads (60 μm), as well as designs with no via-in-pads and capped via-in-pads. The results indicated that the micro via-in-pad design significantly increased the tombstoning; thus, tombstoning did not occur in components with both no via-in-pads and capped via-in-pads. Capped via-in-pads exhibited the best results in preventing tombstoning and provided a wide process window for the selection of process parameters. The results showed that tombstoning was found decreased with both increasing stencil opening ratio and use of reflow profile with long-preheat condition.

[6] Based on Yong-Won Lee, Keun-Soo Kim, and Katsuaki Suganuma (2012), "The effect of micro via-in pad design on surface-mount defects: part I – tombstoning", *Soldering & Surface Mount Technology*, Vol.24 No.3, pp. 197–205, and

[7] Yong-Won Lee, Keun-Soo Kim, and Katsuaki Suganuma (2010), "The effect of micro via-in-pad designs on SMT defects in ultra-small component assembly", *IEEE International Conference on Electronic Packaging Technology & High Density Packaging, Shanghai, China*, August.

7.1 Objective and overview

The electronics manufacturing industry is continuously facing demands for smaller, lighter and more powerful devices [49]. This demand has led to the introduction of PCB with micro via-in-pad technology, which allows more space between pads for trace routing, thus enabling a higher I/O density design [14]. Micro via-in-pads are defined by IPC-02315 and IPC-6012A standards as blind and buried vias that are equal to or less than 152 μm in diameter with a target pad equal to or less than 356 μm in diameter. The target pad is defined as the land on which a micro-via ends and makes a connection [77].

Micro via-in-pads in SMT applications allow the realization of low costs, high densities, high speeds and miniaturization for electronic devices. However, accompanying all of the advantages described above is a high occurrence rate of soldering defects, such as voids [81,82,83,129,130,131] and extreme cases of tombstoning in the assembly of tiny passive components [12]. Tombstoning is the lifting of one end of a leadless component, such as a capacitor or a resistor, and the standing on another of its ends [14]. It is caused directly by an unbalanced wetting of the two ends of the component at reflow, and accordingly, the unbalanced surface tension pulling force of the molten solder is exerted onto the two ends, as shown in Section 2.3.3 of Chapter 2.

In the present study, potential factors such as micro via-in-pad design, stencil opening ratio and reflow profile, which might affect tombstoning in 0201 chip components, were investigated. The results and tombstoning mechanism are discussed below, and optimized conditions are recommended.

7.2 Experimental

7.2.1 Materials and methods

The test vehicle used in the study was a four-layer BT board with a nickel-gold finish. The test vehicle contained 60 8 mm × 8 mm laminated modules arranged in a 5 × 6 × 2 matrix. There were a total of 1,560 pad layouts for 0201 (0603 metric, 0.6 mm × 0.3 mm) chip components. Figures 7.1 and 7.2 shows the micro via-in-pads' locations and examples of them. The test board

design groups were the different micro via-in-pad designs and solder pads. The pads were NSMD pads for all chip components. All pad shapes were distributed equally across the horizontal and vertical orientations. The pad dimensions in this design were fixed at 0.30 mm (length) × 0.36 mm (width) × 0.22 mm (space).

The test vehicle was assembled for lead-free 0201 passive components, such as resistors, inductors, ferrite beads and capacitors. The lead-free finish on the component termination was 100 percent pure tin.

The solder used in this study was a water soluble paste with a metal composition of 95wt.%Sn–5wt.%Sb. The metal content was 90 percent, and the solder melting range was approximately 232–240°C, as specified in the supplier's specifications (Alpha Metal WS 609). The solder powder used in this study had a particle size of 25–45 μm (Type 3).

The stencil printing process was carried out using an MPM AP Excel printer with metal squeegee angles at 60°, which were fitted to the printer. The following stencil printing parameters were used for all stencil printing: printing speed = 8 mm/s, print force = 5.3 kg, balance = 50:50 and print gap = 0.

After the solder paste stencil printing process, the component placement was performed using a Siemens HS 60 pick and place machine. A placement force of 1 N was used. Next, a Heller 1800 convection reflow oven was used to reflow an assembled board from a good solder joint between the PCB and the chip components with a nitrogen atmosphere. The nitrogen environment was controlled at an oxygen level of less than 400 ppm. The reflow section included six heating zones and two cooling zones. Each heating zone was equipped with two convectional heaters on both top and bottom, which were programmed appropriately into the following temperature sections: preheating, soak, reflow, peak and cooling. All boards were visually inspected using a microscope, and solder behavior was observed using a Sanyo Seiko SK-5000 SMT scope.

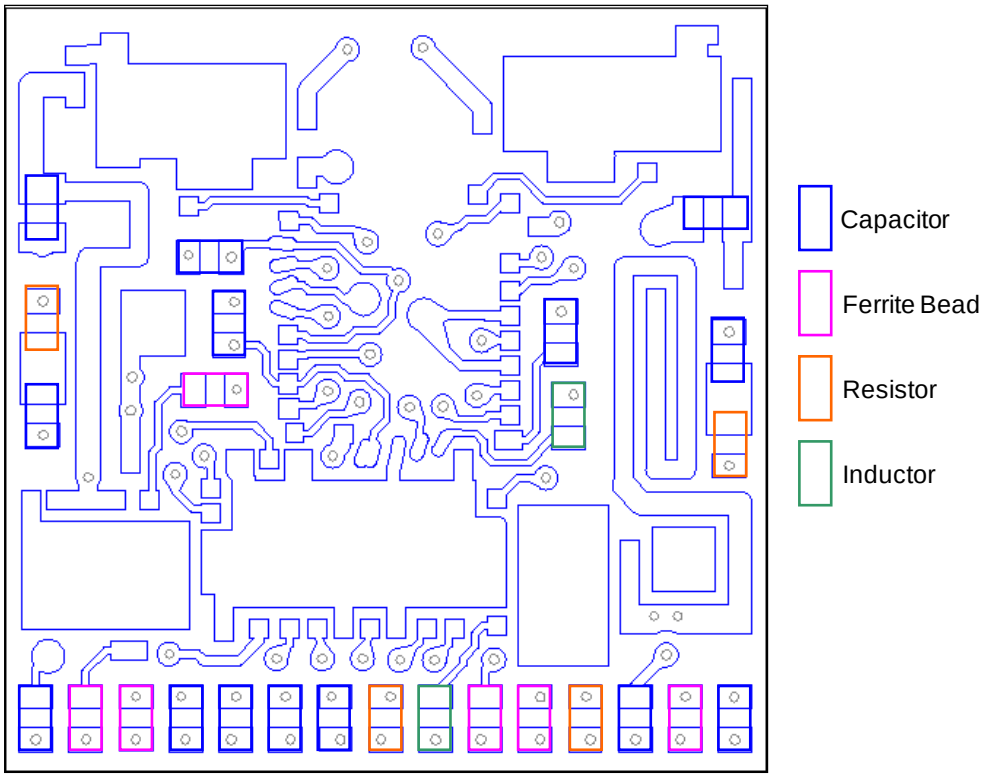


FIGURE 7.1 Test vehicle design.

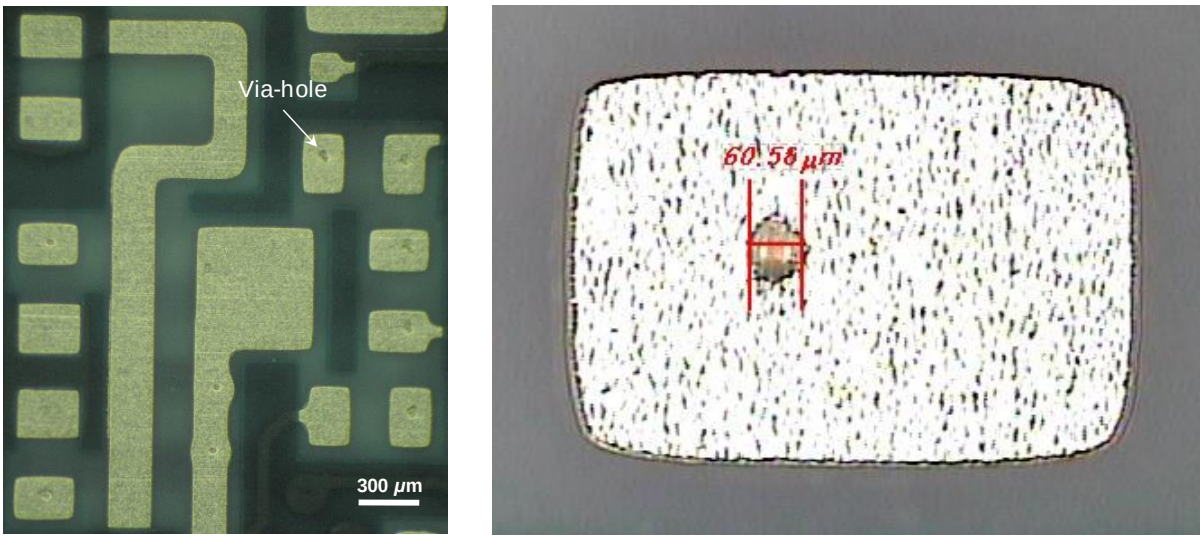


FIGURE 7.2 Example of micro via-in-pads: the via-hole is 60 μm in diameter.

7.2.2 Design of the experiments

A designed experiments approach was followed to determine the micro via-in-pads' design and process parameters. An experiment was designed and conducted using the various factors and levels shown in Table 7.1. The different types of micro via-in-pad are shown in Figure 7.3. Micro via-in-pad types tested included ultra-small via-in-pads, small via-in-pads, large via-in-pads, no via-in-pads and capped via-in-pads. Via-hole diameters were 10 μm, 20 μm, and 60 μm for ultra-small via-in-pads, small via-in-pads, and large via-in-pads, respectively.

Three different experiments were completed to evaluate the impact of micro via-in-pad design, stencil aperture size and reflow profile on tombstoning in small chip components with micro via-in-pads. Two different reflow profiles were set. Table 7.2 summarizes the key reflow profile parameters for this experiment. The actual reflow profiles used are shown in Figure 7.4. The profile with the long-preheat condition was used as the standard reflow profile in the present study.

TABLE 7.1 Factors for experiments

Factors	**Levels**				
Micro via type (Via-hole size)	Ultra-small vias (10 μm)	Small vias (20 μm)	Large vias (60 μm)	No vias	Capped vias
Stencil aperture (Opening ratio)	80%		90%	100%	
Reflow profile	Long-preheat (84 s)		Short-preheat (71 s)		

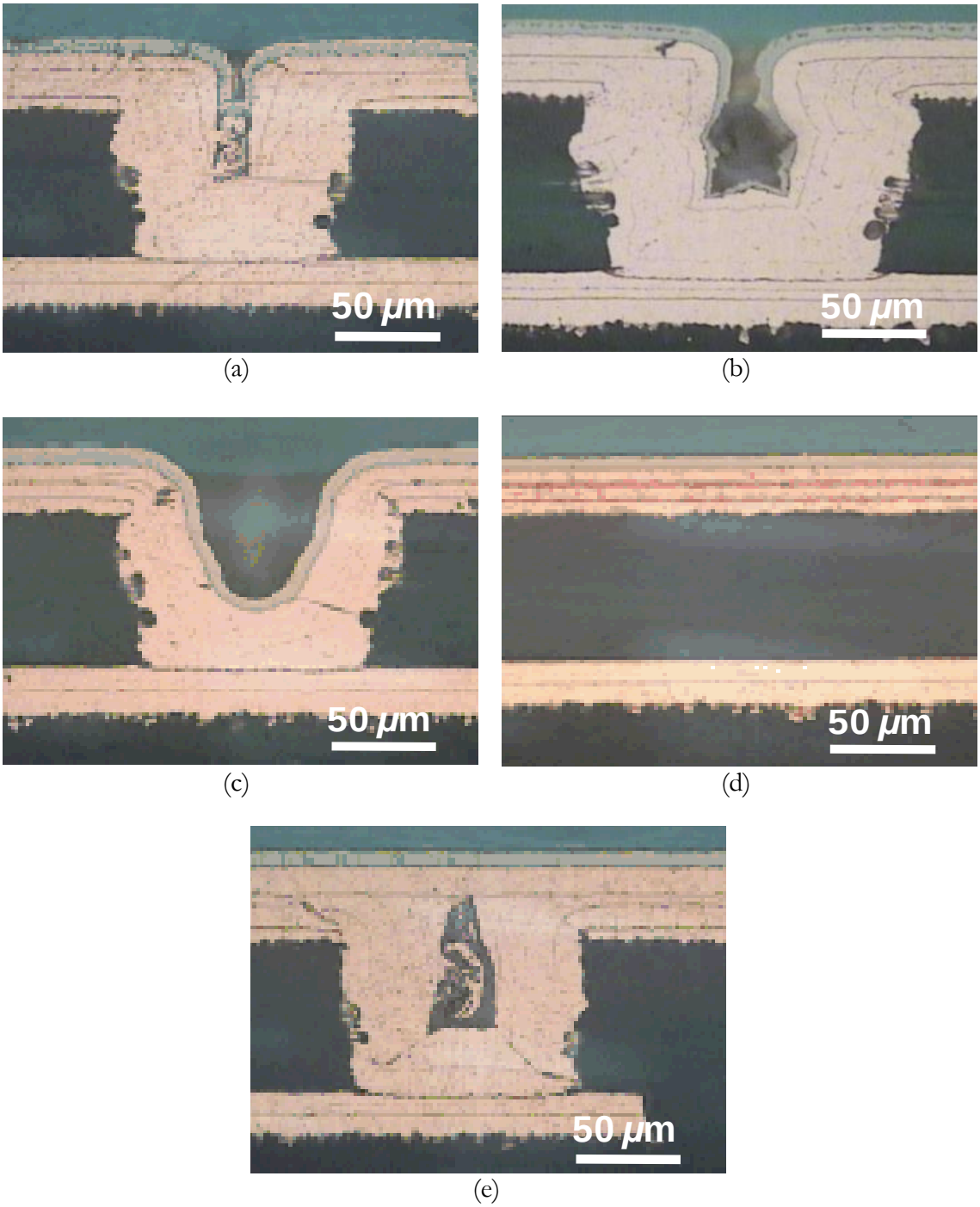
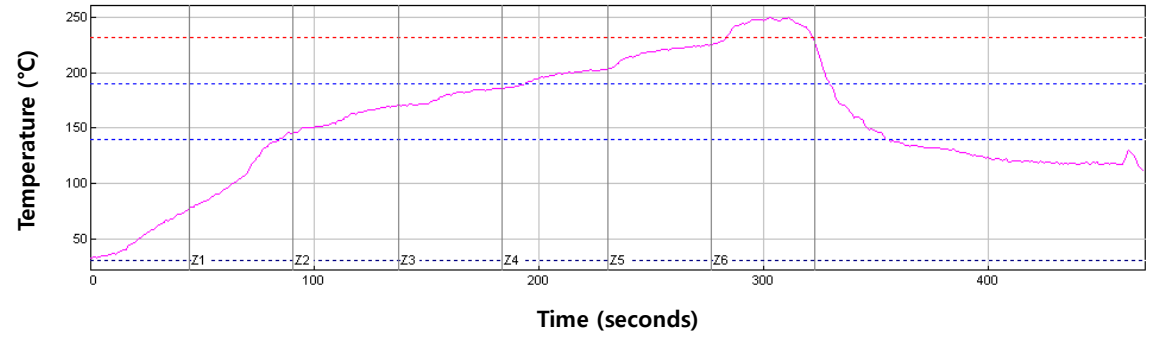
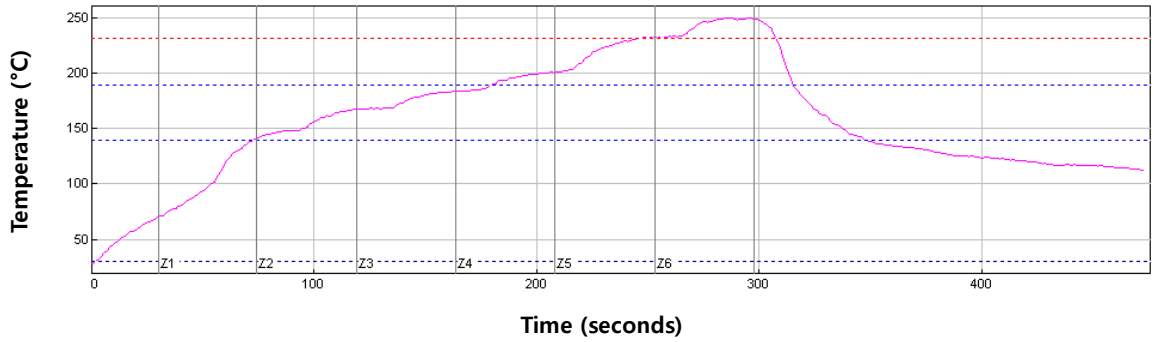


FIGURE 7.3 Micro via-in-pad designs.

Notes: (a) Ultra-small via-in-pads; (b) small via-in-pads; (c) large via-in-pads; (d) no via-in-pads; (e) capped via-in-pads.



(a)



(b)

FIGURE 7.4 Actual reflow profile.

Notes: (a) Long-preheat condition; (b) short-preheat condition.

TABLE 7.2 Key thermal profile parameters

Profiles	Preheat 30-140°C	Soak time 140-190°C	Reflow time-above-liquidus (232°C)	Peak temperature
Long-preheat	84 s	109 s	39 s	251°C
Short-preheat	71 s	107 s	60 s	251°C

7.2.3 FEM thermal simulation

In order to verify thermal behavior and to clarify the mechanism of tombstoning, the thermal simulation was conducted by means of the finite element method (FEM). Figures 7.5 and 7.6 show a two-dimensional thermal simulation model for the reflow process. The following assumptions were made regarding the simulation analysis: in the simulation, the peak solder joint temperature was 251°C, while the maximum top of the board temperature was 268°C and bottom of board temperature was 258°C. The reflow time (time-above-liquidus) was 45 s. Analyses were made of two micro via-in-pad designs: small micro via-in-pads (20 μm) and large micro via-in-pads (60 μm). The dimensions used for calculation are listed in Table 7.3.

TABLE 7.3 Thermal simulation model

Items	Material	Dimension (mm)
Total substrate thickness	–	0.49
Outer metal layer	Copper	0.03
Inner metal layer	Copper	0.03
Prepreg material	Prepreg resin material	0.06
Core material	BT	0.10
Large via-hole	Copper	0.06
Small via-hole	Copper	0.02
0201 chip component size	–	0.6 × 0.3 × 0.3
Package body size	–	9.9 × 9.0 × 1.5

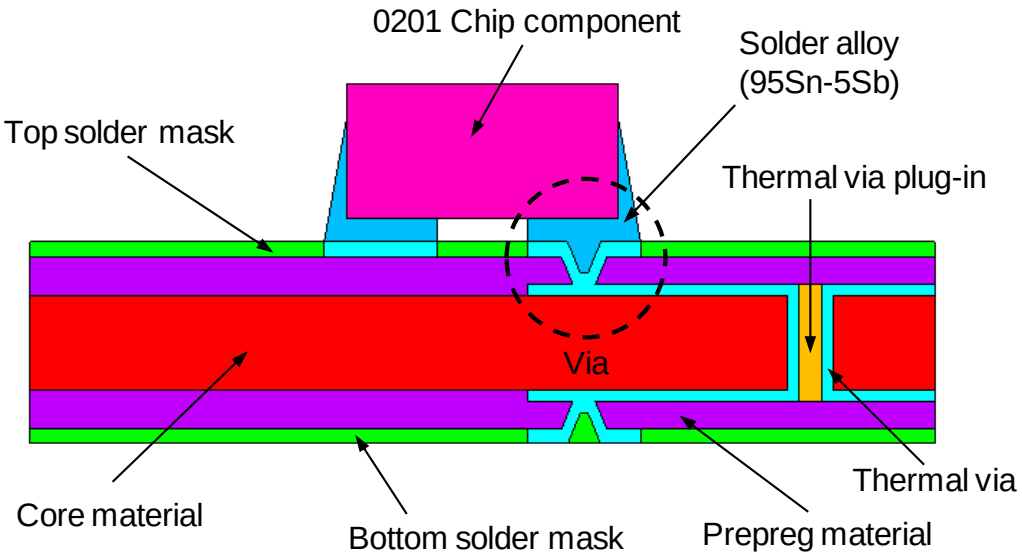


FIGURE 7.5 Schematic of micro via-in-pad structure for thermal simulation.

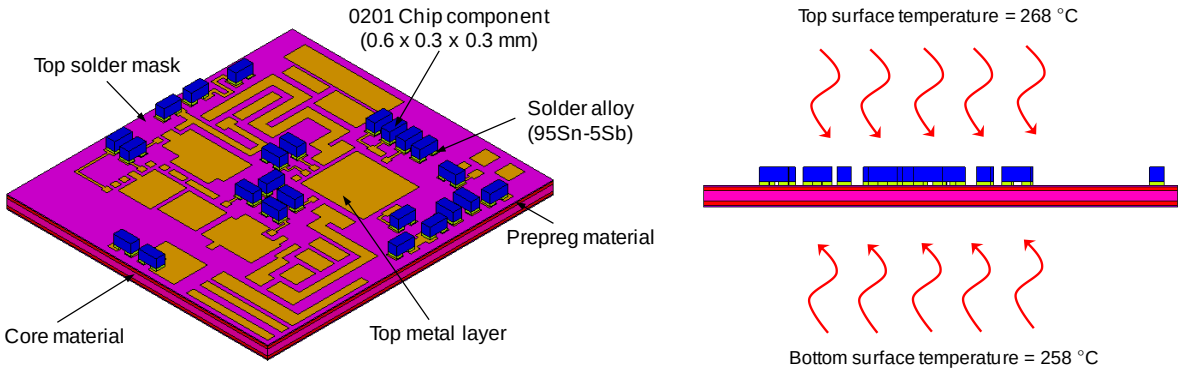


FIGURE 7.6 3D thermal simulation models.
Notes: (a) Assembled package; (b) board temperature setting.

7.3 Results and discussion

7.3.1 The effect of micro via-in-pad designs on tombstoning

A tombstoning test was carried out with different micro via-in-pad designs. Figure 7.7 shows the relationships between micro via-in pad design and tombstoning. As shown in Figure 7.7, tombstoning was not observed in large via-in-pads (60 μm), no via-in-pads and capped via-in-pads. However, ultra-small via-in-pads (10 μm) and small via-in-pads (20 μm), whose via-hole sizes were the smallest, showed tombstoning rates of 5.4 and 3.5 percent, respectively.

In this study, micro via-in-pads' designs also greatly affected the occurrence of tombstoning in the assembly of small chip components. For example, the micro via-in-pads will be easily covered by solder flux and become a fully sealed space during the solder paste printing process. If the gas remaining inside the via-in-pad is fully or partially blocked, when the flow is suddenly cut off by the heat of the reflow process, the remaining gas will inevitably be ejected. Degassing will be easy if the flux viscosity is low; however, degassing will be difficult and the gas accumulates to a high pressure if the flux viscosity is high. In this case, the spurting force of the gas will depend on the via-hole size. The smaller the via-hole size, the greater the spurting force becomes. As the results in Figure 7.7 show, the highest tombstoning rate occurred with use of the small via-in-pads (20 μm).

The shape of the via-hole is another factor affecting tombstoning in components with micro via-in-pads. Figure 7 a schematic comparison of three representative via-hole shapes in micro via-in-pads:

(a) cup-like via-hole;
(b) funnel-like via-hole, and
(c) bowl-like via-hole.

The outgassing force of entrapped flux will be higher with (b) the funnel-like via-hole than with (a) the cup-like via-hole and (c) the bowl-like via-hole. This phenomenon can be explained by the equation of continuity of fluid [133]. According to the equation of continuity, the smaller the area, the faster the flow becomes, and the greater the area, the slower the flow becomes. Therefore, in the case of the funnel shaped via-hole, as the via-hole opening becomes

narrower, the gas flow becomes faster, and its outgassing force will be greater than that of a large via-hole opening.

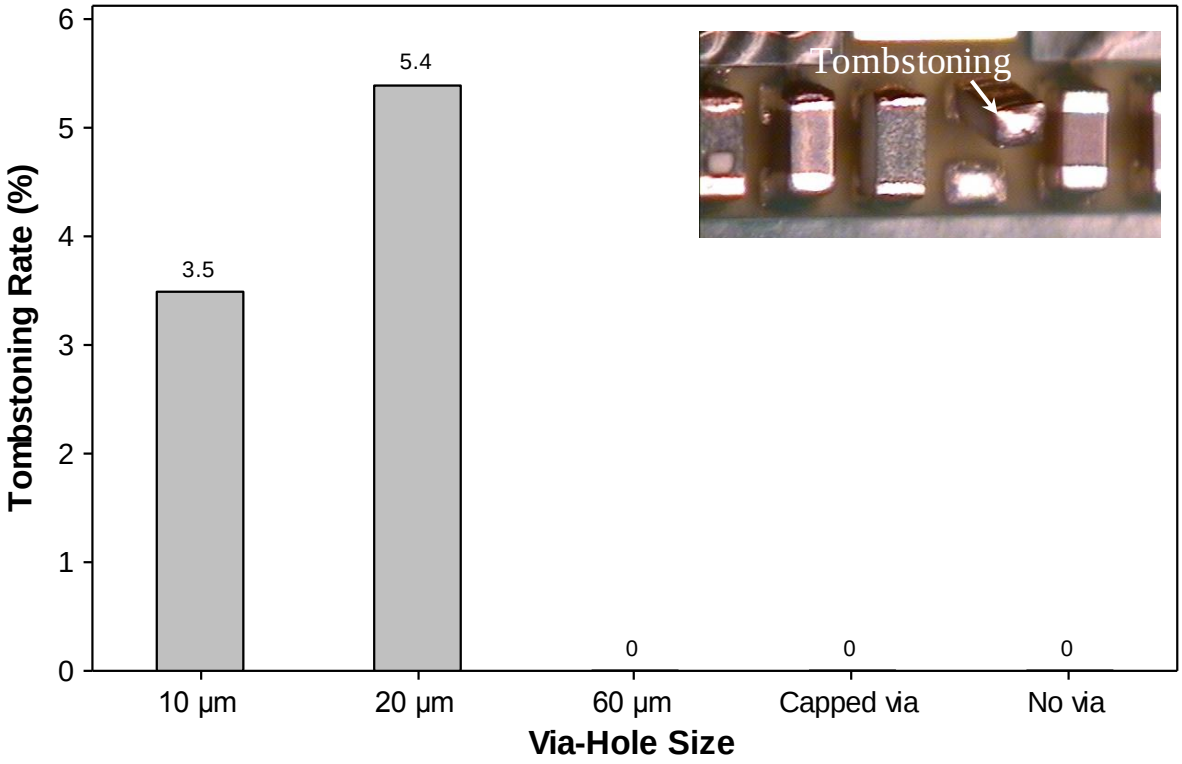
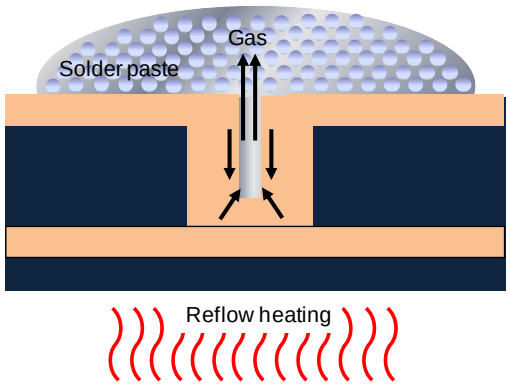
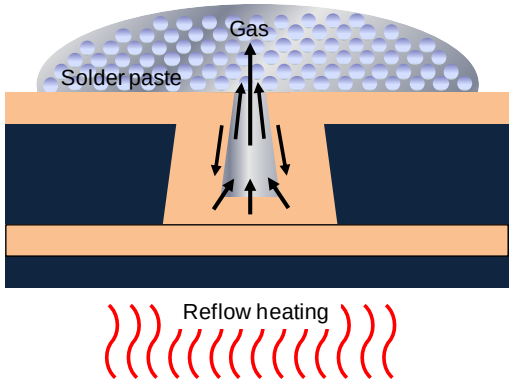


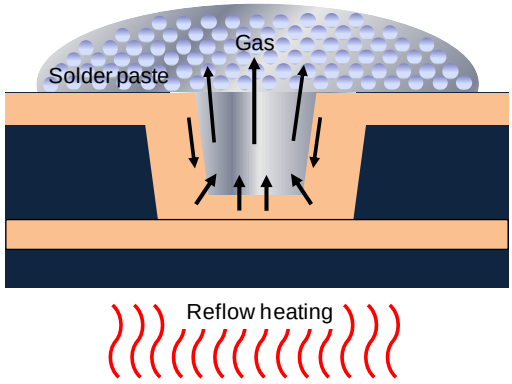
FIGURE 7.7 Relationship between micro via-in-pad design and tombstoning.



(a)



(b)



(c)

FIGURE 7.8 Schematic diagrams of (a) cup-like via-hole, (b) funnel-like via-hole, and (c) bowl-like via-hole.

7.3.2 The effect of stencil aperture size on tombstoning

Figure 7.9 shows the relationship between stencil opening ratio and micro via-in-pads' tombstoning rate. No tombstoning defect was observed in components with no via-in-pads and capped via-in-pads for any stencil opening ratio. The large via-in-pads (60 μm) showed a tombstoning rate of only 1.1 percent at an 80 percent stencil opening ratio, and no tombstoning was observed at 90 or 100 percent stencil opening ratios. The small via-in-pads (20 μm) showed tombstoning at all three stencil opening ratios. The tombstoning rate was 5.8 percent at an 80 percent opening ratio, and it reduced as the stencil opening ratio increased. The tombstoning rates were the highest when the ultra-small via-in-pads (10 μm) were used, which was as high as 13 percent. The tombstoning rate was dramatically reduced when the stencil opening ratio was 90 and 100 percent, to 3.6 and 2.9 percent, respectively. This result indicates that the larger solder volume performed much better than the smaller solder volume in reducing the occurrence of tombstoning in the micro via-in-pads.

Since ultra-small components, such as 01005s (0402 metric, 0.4 mm × 0.2 mm × 0.2 mm) and 0201s (0603 metric, 0.6 mm × 0.3 mm × 0.3 mm), are very small and light, the small solder volume will not endure the flux spurting from the via-hole. Increasing the solder volume can be helpful, presumably because it blocks expelled gas from the via-hole.

7.3.3 The effect of reflow profile on tombstoning

The effect of reflow profile on tombstoning rate was studied by comparing the two preheat conditions with the results shown in Figure 7.10. As expected, no tombstoning occurred in both no via-in-pads and capped via-in-pads. Tombstoning was observed in only 0.4 percent in the profile with the short-preheat conditions for the large via-in-pads (60 μm), and it was not observed in the profile with the long-preheat conditions. The ultra-small via-in-pads (10 μm) showed the highest tombstoning rate in the profile with the short-preheat conditions, but it rapidly decreased to approximately 3.5 percent when the long-preheat conditions were applied. The overall tendency was that the long-preheat condition of the reflow profile was somewhat effective in reducing the occurrence of tombstoning, but it could not completely remove the defects in the use of micro via-in-pads with lead-free solder.

The tombstoning behavior in the reflow process was observed *in situ* with an SMT scope. Figure 7.11 shows the representative images. As the reflow temperature became elevated above 227°C, one side of the chip component near the pad with a via-hole reacted and made a motion [Figure 7.11 (b)]. It may be an early stage of a version of tombstoning. Then, the melting solder was elevated along the opposite side of the component at the pad with no via-hole simultaneously when the temperature became elevated above 232°C. At composition 95wt.%Sn–5wt.%Sb, the solder begins to melt at the solidus temperature of 232°C, but will not turn completely to liquid before reaching the liquidus temperature of 240°C, according to the tin-antimony phase diagram [134]. Above 240°C, the solder fillet rapidly formed at the pad with no via-hole and chip component, which were being soldered to the pad with a via-hole side; they were suddenly lifted vertically.

The primary cause of this tombstoning defect is the unbalanced force acting on the component, which arises from the surface tension of the molten solder alloy. To understand the origin of tombstoning, it is necessary to consider all process and material factors. Figure 7.12 shows the forces acting on a chip component when it is in contact with molten solder during the reflow process. There may be a difference in moment between the melting solder side and the non-melting solder sides of the chip electrode area which may have different temperatures during the reflow process. Tombstoning defects may occur when the force of moment *F4* (surface tension at one side of the chip electrode area) and *F6* (flux spurting force from the via-hole) are larger than the sum of moment *F3* (self weight), moment *F5* (surface tension under the chip component) and moment *F2* (tack force power at the opposite side of chip electrode area). Thus, it is easy to demonstrate the conditions under which surface tension and flux spurting force will be large enough to lift a small chip component.

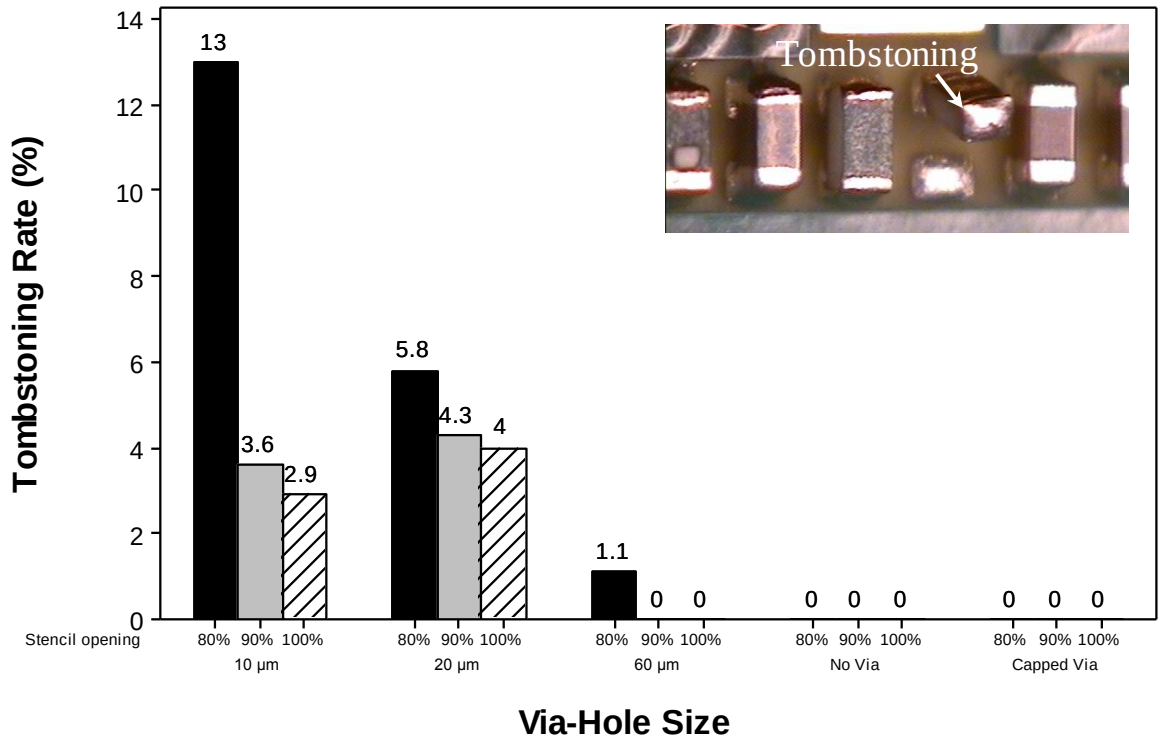


FIGURE 7.9 Relationship between stencil opening ratio and tombstoning rate at micro via-in-pads.

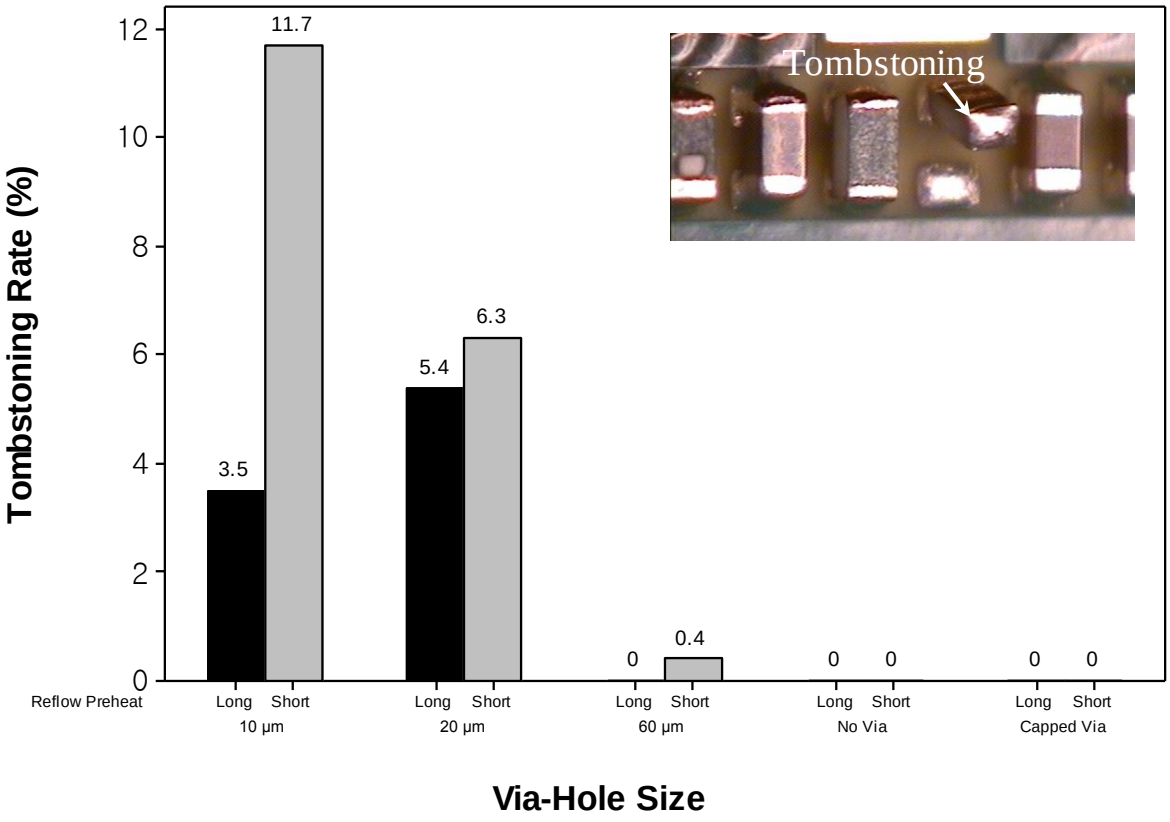
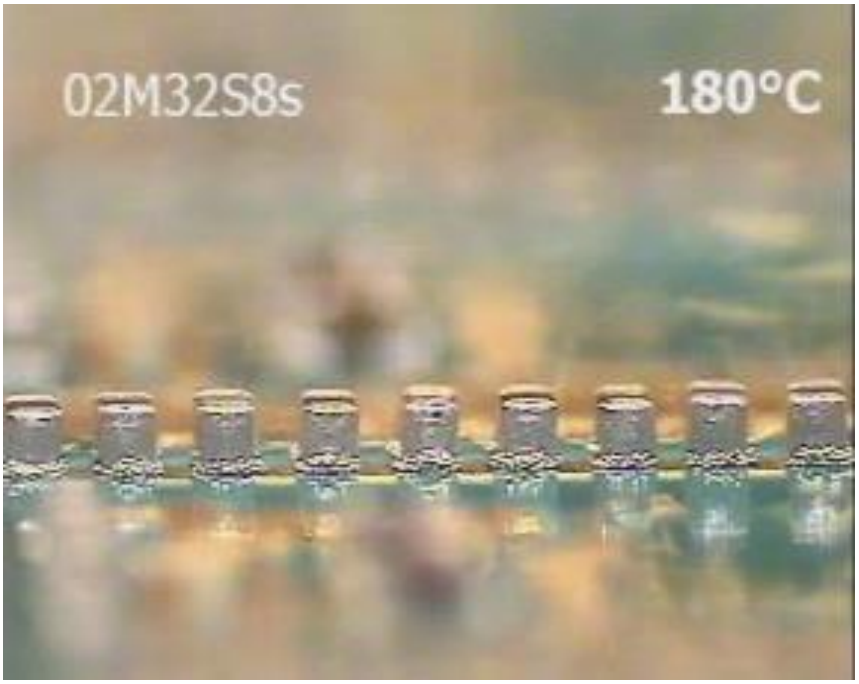
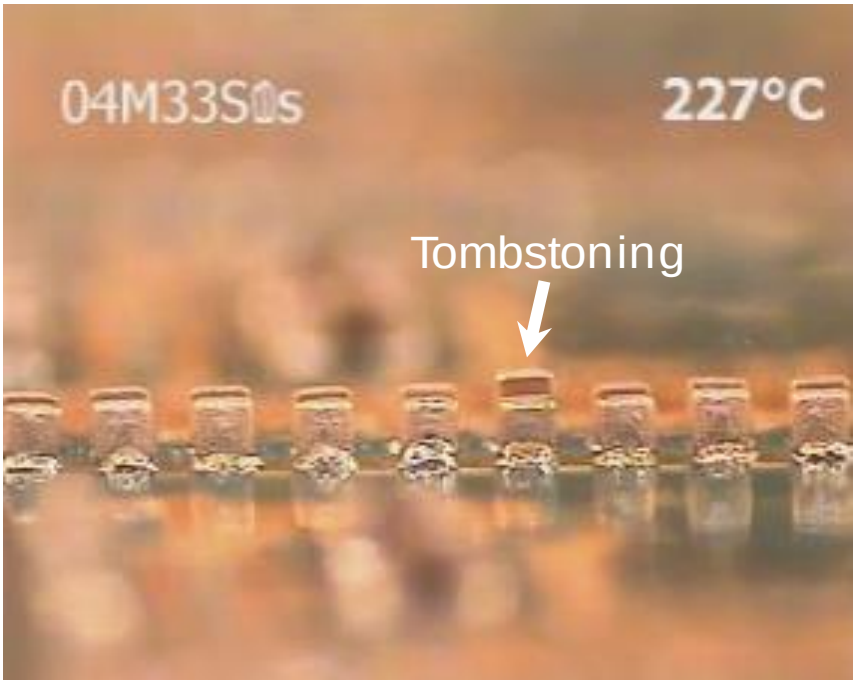


FIGURE 7.10 Relationship between reflow preheat condition and tombstoning rate in micro via-in-pads.



(a)



(b)

FIGURE 7.11 SMT scope images of (a) reflow soak zone (180°C) and (b) reflow zone (227°C).

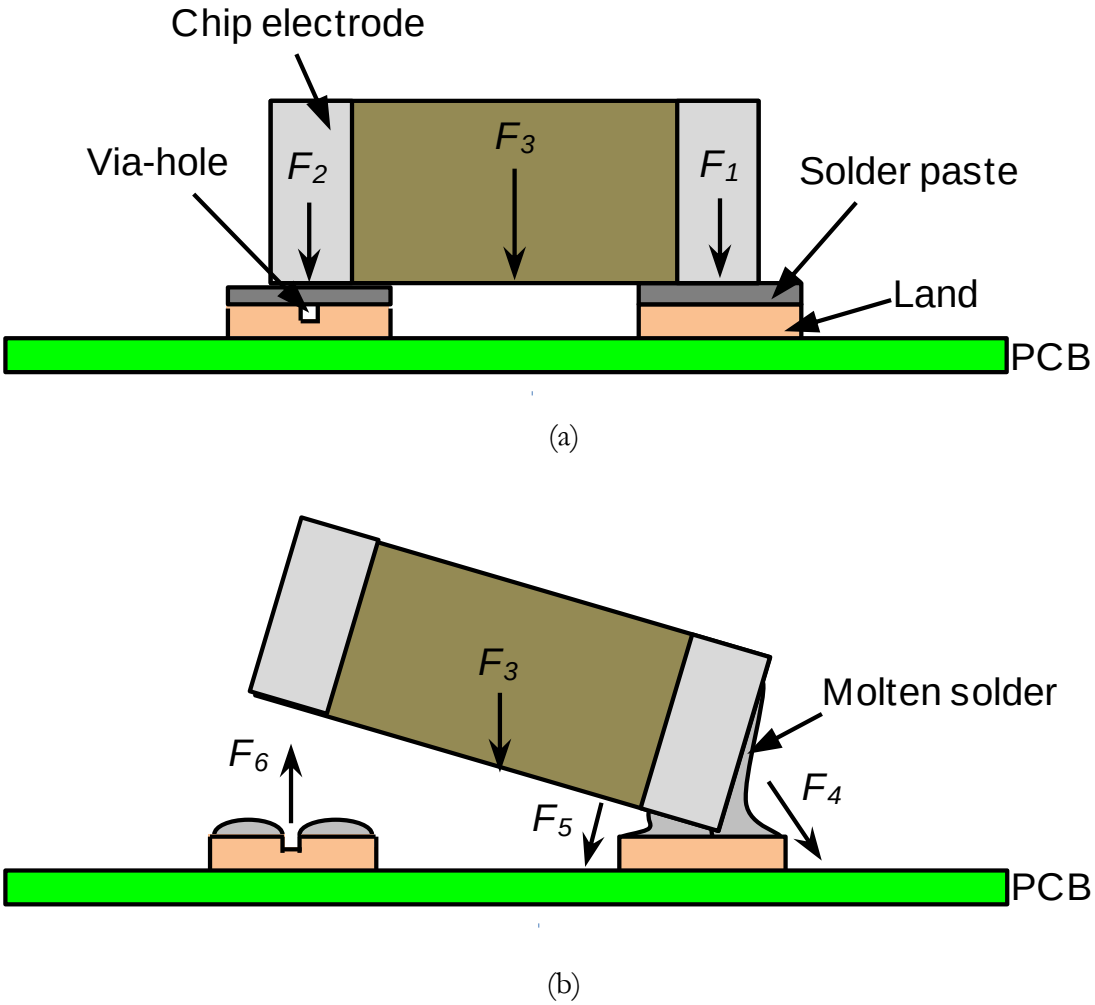


FIGURE 7.12 Schematic representations of the forces acting on a chip as it is tombstoning.

Notes: (a) solder paste conditions before melting during the reflow process; (b) conditions of melting solder at only one side of the electrode when the temperatures are different at both sides of the electrode with a chip component; tombstoning will occur if: *F4+F6 > F2+F3+F5*; *F1*, *F2*: moment of tack force power with solder paste; *F3*: moment of weight of self weight with chip component; *F4*: moment of melting solder surface tension at chip electrode area; *F5*: moment of melting solder surface tension under the chip component and *F6*: moment of flux spurting force at the via-hole.

7.3.4 FEM simulation results

Figures 7.13 and 7.14 show the temperature distributions within the solder joint in micro via-in-pad designs for the pad with a small via-hole (20 μm) and the pad with a large via-holes (60 μm). Simulation results for both the small via-in-pad and large via-in-pad are summarized in Table. 7.4.

Based on the simulation results, temperature differences between the pad with a no via-hole side (268°C) and the pad with a small via-hole side (266.75°C) were within 2°C, as shown in Figure 7.13. The same result appeared in the pad with a no via-hole side (268°C) and the pad with a large via-hole side (266.70°C), as shown in Figure 7.14. The results showed that it was impossible to differentiate the thermal mass distribution between the pad with a small via-hole and the pad with a large via-hole, regardless of micro via-in-pad types.

However, the result shows that the maximum temperature difference is about 2°C between the pad with no a via-hole side and the pad with any via-hole side during the reflow process. The reason for this temperature difference is due to heat release behavior from the via-hole side. 0201 chip components are very small and, accordingly, soldering progresses much faster on the pad with a no via side than on the pad with a via side. Therefore, a moment difference may be seen between the melting solder side (no via side) and the non-melting solder side (via side) because both sides of the chip component have a different temperature during the reflow process.

TABLE 7.4 FEM simulation results summary.

	Small via-in-pads		**Large via-in-pads**	
Via-in-pad type	**No via side**	**Via side**	**No via side**	**Via side**
Temperature (°C)	268.0	266.75	268.0	266.70

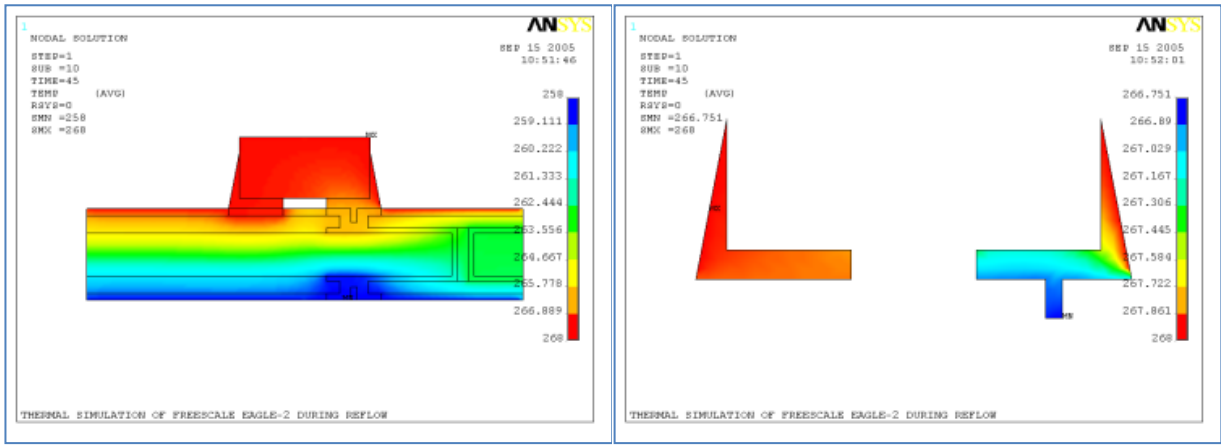


FIGURE 7.13 FEM simulation results for solder joint with a small via-in-pad.

Note: The via-hole is 20 μm in diameter.

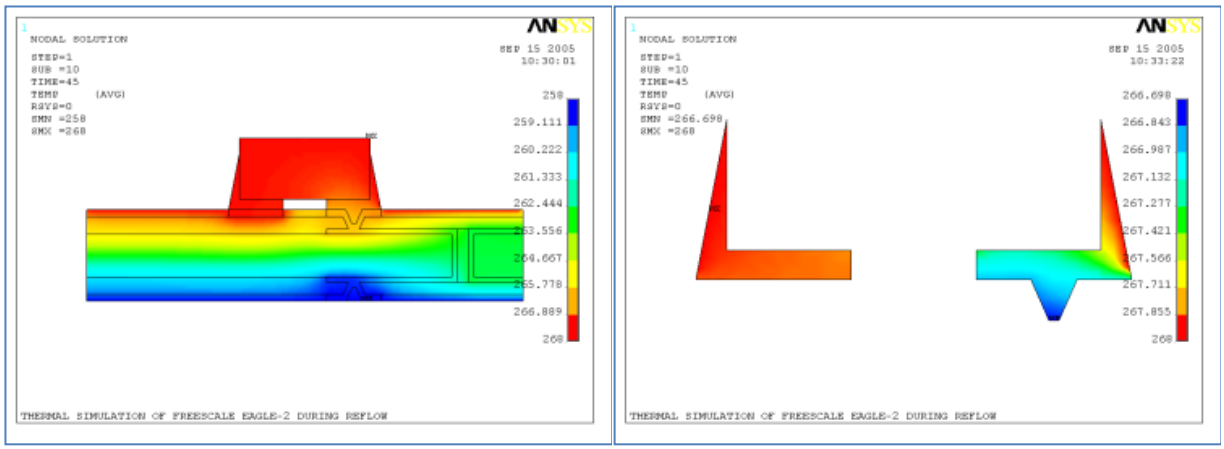


FIGURE 7.14 FEM simulation results for solder joint with a small via-in-pad.

Note: The via-hole is 60 μm in diameter.

7.4 Summary

In this work, the following test results were obtained regarding the relationship between micro via-in-pad design and tombstoning problems in the SMT process:

1. The design of micro via-in-pads greatly affects on the occurrence of tombstoning in the assembly of small chip components. In a word, the smaller the via-hole size, the greater the occurrence of tombstoning. The highest tombstoning rate occurred during use of the ultra-small via-in-pad design (10 μm). A capped via-in-pad was effective in reducing the occurrence of tombstoning.

2. The larger solder volume performed much better than the small solder volume in reducing the occurrence of tombstoning in the micro via-in-pad conditions. Tombstoning occurred in about 1.1 percent of components with large via-in-pads (60 μm) at an 80 percent stencil opening. Defects ramped up to about 5.8 percent with small via-in-pads (20 μm) and to 13 percent with ultra-small via-in-pads (10 μm) at 80 percent stencil openings, and they dramatically reduced as the stencil opening size increased.

3. The long-preheat conditions of the reflow profile were effective in reducing the occurrence of tombstoning, but it could not completely remove the defects.

4. In the simulation results, temperature differences between the pad with no via side and the pad with a large via side were within 2°C and consequently resulted in unbalanced wetting. Thus, unbalanced wetting was found to result in a greater tombstoning rate.

Therefore, from the above, capped via-in-pads, larger stencil opening size and the use of a reflow profile with long-preheat conditions are highly desirable if the micro via-in-pad and lead-free solder technology is considered in the SiP module assembly process.

Chapter 8

The effect of micro via-in-pad designs on voiding and spattering defects[8]

This chapter is intended as an expansion of the work of Chapter 7, where we have described the effect of micro via-in-pad design on tombstoning defects. The purpose of this paper is to propose a solution procedure to minimize/eliminate voiding and spattering defects in the assembly of 0201 chip components with micro via-in-pads and 95wt.%Sn–5wt.%Sb solder alloy. In total, four different micro via-in-pad designs were compared (via-hole opening size): ultra-small via-in-pads (d: 10 μm), small via-in-pads (d: 20 μm), and large via-in-pads (d: 60 μm), as well as designs with no via-in-pads and capped via-in-pads. The results indicate that larger via-holes were seen to create bigger voiding than smaller via-holes. For smaller via-holes, spattering is a greater problem than voiding in solder joints. Capped via-in-pads exhibited the best results in preventing voiding and flux spattering, and provided a wide process window for the selection of process parameters. The findings provide certain process guidelines for surface mount assembly with via-in-pad substrate design. The strategy is to prevent voiding and spattering by adopting capped via-in-pads, if possible, when applying micro via-in-pads with the 95wt.%Sn–5wt.%Sb solder alloy system.

[8] Based on Yong-Won Lee, Keun-Soo Kim, Katsuaki Suganuma (2012), "The effect of micro via-in pad design on surface-mount defects: part II – voiding and spattering", *Soldering & Surface Mount Technology*, Vol.25 No.1, pp. 4–14.

8.1 Objective and overview

The 95wt.%Sn–5wt.%Sb solder is a solid solution of antimony in a tin matrix. The relatively high melting point of this alloy makes it suitable for high temperature applications [87]. However, this alloys used for the assembly of SiP modules and it introduces new process challenges. The wettability of lead-free alloys, especially Sn-Sb alloys, is lower than the eutectic Sn-Pb alloy [3,88,89]. In order to improve the wettability of lead-free solder pastes, they are formulated with a very active flux. These fluxes have a tendency to explode (or burst) during the reflow operation and create flux spatters on the PCBs. As the solder melts and coalesces, surface tension of the molten material exerts pressure on the entrapped flux. When the pressure exerted is high enough, flux is expelled violently [90]. This is commonly referred to as the coalescence theory [91].

As shown in Chapter 7, the design of micro via-in-pads greatly affects on the occurrence of tombstoning defect in the assembly of small chip components. In a word, the smaller the via-hole size, the greater the occurrence of tombstoning. The highest tombstoning rate occurred during use of the ultra-small via-in-pad design (via-hole size: 10 μm). A capped via-in-pad was effective in reducing the occurrence of tombstoning. In this chapter, effects of micro via-in-pad designs on voiding and spattering defects. The results and defects mechanism will be discussed below, and optimized conditions will be recommended.

8.2 Experimental

8.2.1 Materials and methods

The test vehicle used in this study was a SiP module, as shown in Figure 8.1. The PCB substrate was a four-layer BT board with a nickel-gold finish. The test vehicle contained 60 8.0 mm × 8.0 mm laminated modules arranged in a 5 × 6 × 2 matrix. There were a total of 1,560 pad layouts for 0201 chip components. The test board design groups were the different micro via-in-pads. The pads were NSMD pads for all chip components. All pad shapes were distributed equally across the horizontal and vertical orientations. The via-hole design for the passive components is shown in Figure 8.2. The figure depicts a laser via-hole. Details of pad dimensions are shown in Table 8.1.

The test vehicle was assembled for experimental run lead-free 0201 chip components, such as resistors, inductors, ferrite bead, and capacitors. The lead-free finish on the component terminal was 100 percent tin.

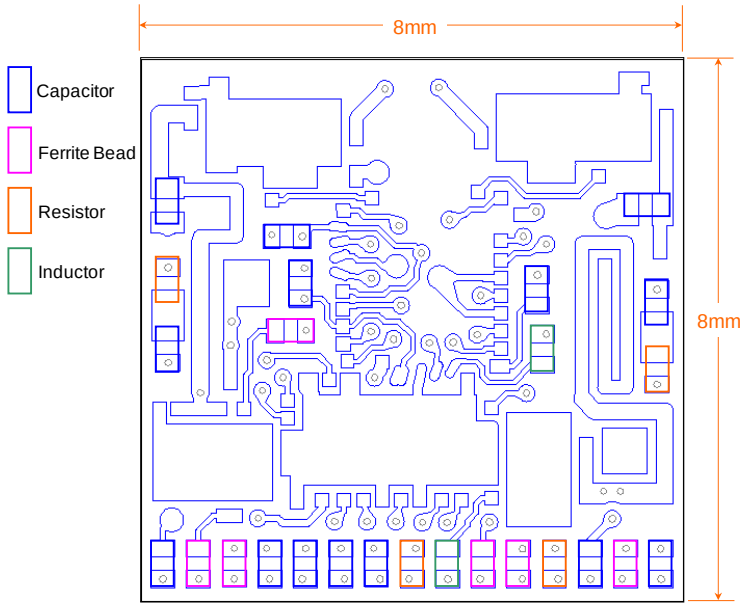
The solder paste alloy used in this study was a water soluble 95wt.%Sn–5wt.%Sb. The metal content was 90 percent, and the solder melting point was approximately 232-240°C as specified in the supplier's specification (Alpha Metal WS609). The solder powder used in this study had a particle size of 25–45 μm (Type 3).

The stencil printing process was carried out using an MPM AP Excel printer with metal squeegee angles at 60°, which were fitted to the printer. The following stencil printing parameters were used for all stencil printing: printing speed = 8 mm/s, print force = 5.3 kg, balance = 50:50 and print gap = 0. The solder paste deposited PCB substrate was inspected using a microscope equipped with a digital camera and documented photographically.

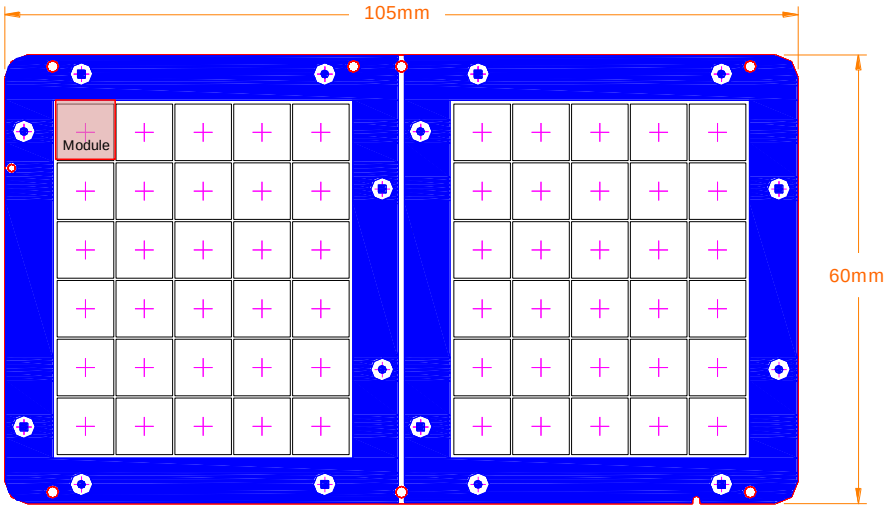
After the stencil printing process, the component placement process was performed using a Siemens HS 60 pick-and-placement machine. A placement force of 1 N was used. Next, populated PCBs were soldered in an eight zone Heller 1800 convection oven with a nitrogen atmosphere. The nitrogen environment was controlled at an oxygen level of less than 400 ppm. Two different profiles were set and determined by thermal profiler (DATAPAQ^{TM}).

The assembled boards were examined for voids using X-ray inspection system (Nikon XT V 160). All measurements were taken at the same Z-level, frame size, voltage, current, resolution brightness, contrast, color, filter etc. to measure the effective area of void for each type of PCB substrate. The average data of 20 samples for each via-in-pad was derived. The void content is expressed as percentage of solder joint area. Too much voiding is unacceptable and 15 percent was set as a maximum allowable voiding extent. Figure 8.3 shows representative X-ray images of the test vehicle. A cross-sectional study was conducted on three randomly selected samples.

Optical microscope and SEM were employed to observe the soldered pads for flux spattering behavior. *In-situ* soldering behavior was also observed using a Sanyo Seiko SK-5000 SMT scope.



(a)



(b)

FIGURE 8.1 Test vehicle design.

Notes: (a) Module design; (b) top side view that shows whole PCB substrate strip outline.

TABLE 8.1 Pad dimension in the test vehicle

Component	L	W	S	A
0201	0.30 mm	0.36 mm	0.22 mm	0.15 mm

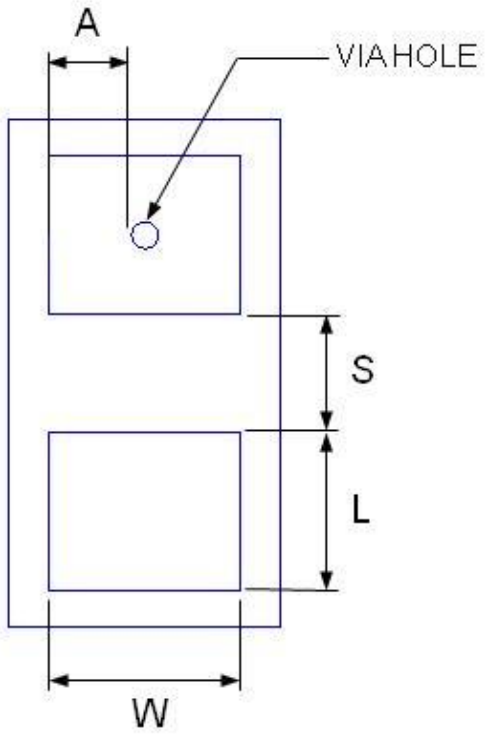


FIGURE 8.2 Schematic of passive chip component pad design and via-hole location.

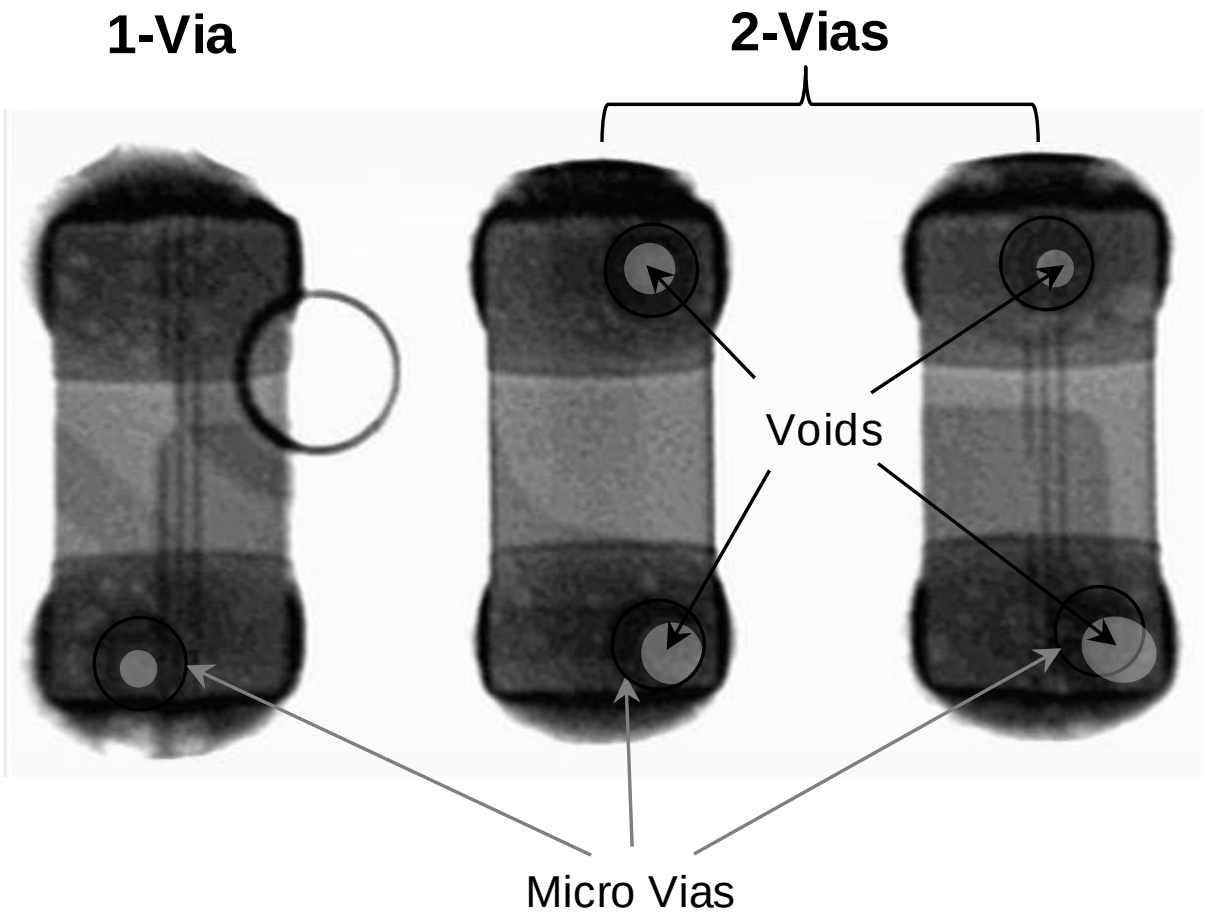


FIGURE 8.3 Example of X-ray image of test vehicles with voids and voiding area evaluation using computer software.

8.2.2 Design of the experiments

A designed experiments approach was followed to determine the micro via-in-pads' design and processes parameters. An experiment was designed and conducted using the various factors and levels shown in Table 8.2. The different micro via-in-pad designs for the 0201 chip components are shown in Figure 8.4. The micro via-in-pad types that were tested include ultra-small via-in-pad, small via-in-pad, large via-in-pad, no via-in-pad, and capped via-in-pad. Their via-hole opening sizes were 10 μm, 20 μm, and 60 μm in diameter for ultra- small via-in-pads, small via-in-pads, and large via-in-pads, respectively.

Three different experiments were completed to evaluate the impact of micro via-in-pad type, stencil aperture size, and reflow profile on voiding and flux spattering in components with micro via-in-pads. Two different reflow profiles were set. Table 8.3 summarizes the key reflow profile parameters for this experiment. The profile with the long-preheat condition was used as the standard reflow profile in the present study (Figure 8.5). For an experimental run, a total of 30 test vehicles were fabricated.

The first response factor used for the qualitative analysis was the ratio of the volume of void to the actual volume of solder joints. The void content was measured using the X-ray system. The response factor obtained for the various runs was checked for normality, using a 95 percent confidence interval. The normality test revealed that the data was normality distributed. The second response factor was the occurrence of flux spatters.

TABLE 8.2 Factors for experiments

Factors	**Levels**				
Micro via type (Via-hole size)	Ultra-small vias (10 μm)	Small vias (20 μm)	Large vias (60 μm)	No vias	Capped vias
Stencil aperture (Opening ratio)	80%		90%		100%
Reflow profile	Long-preheat (84 s)			Short-preheat (71 s)	

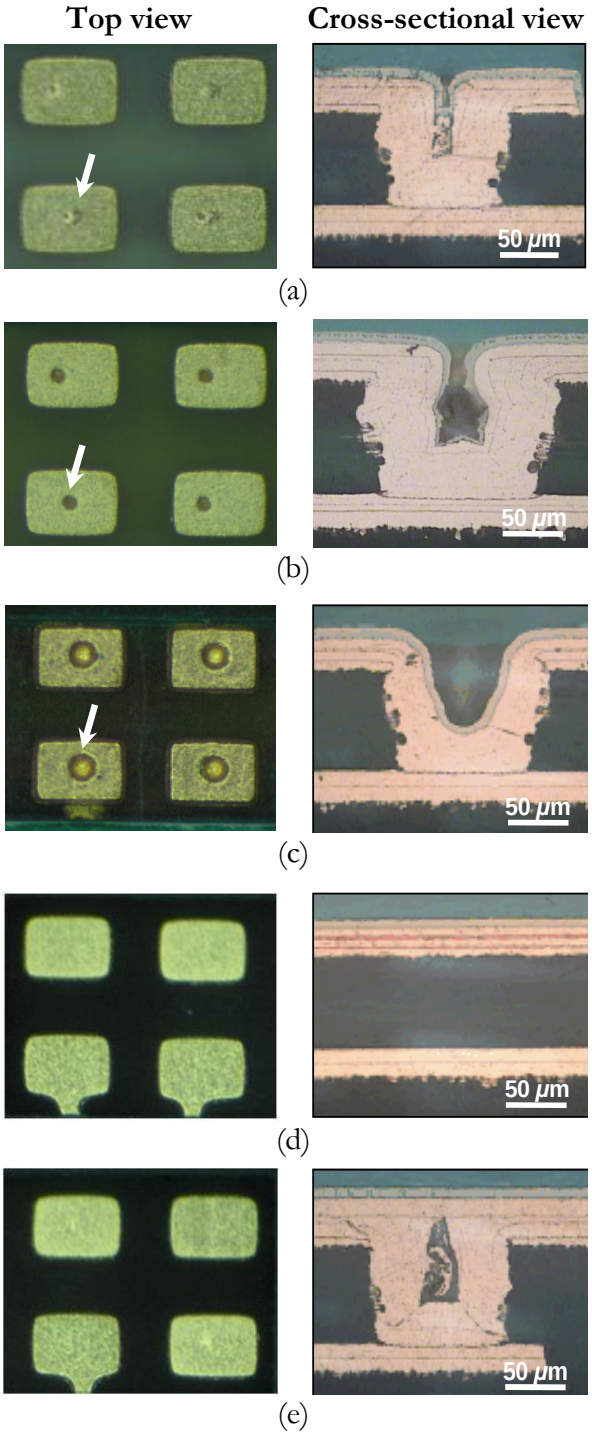


FIGURE 8.4 Optical images of each micro via-in-pad, with the via-hole indicated by arrows.

Notes: (a) ultra-small via-in-pad; (b) small via-in-pad; (c) large via-in-pad; (d) no via-in- pad; (e) capped via-in-pad.

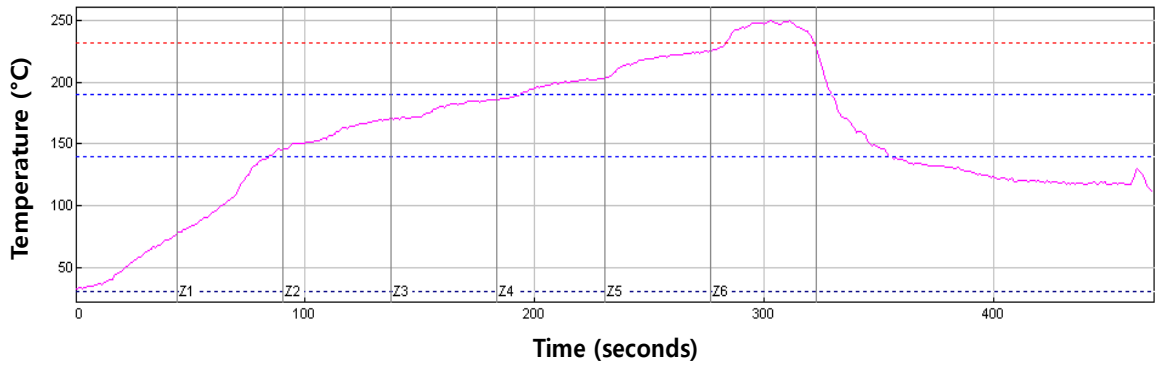


FIGURE 8.5 A representative of reflow profile: long-preheat condition (84 s).

TABLE 8.3 Key thermal profile parameters

Profiles	Preheat 30-140°C	Soak time 140-190°C	Reflow time-above-liquidus (232°C)	Peak temperature
Long-preheat	84 s	109 s	39 s	251°C
Short-preheat	71 s	107 s	60 s	251°C

8.3 Results and discussion

8.3.1 The effect of micro via-hole size on voiding

A voiding test was carried out with different micro via-in-pad designs. The effect of micro via-hole opening size on voiding at solder joints is shown in Table 8.4. The ultra-small via-hole (d: 10 μm) joints showed a void content of 5.0 percent, and it rapidly increased as the via-hole size increased. The void contents were the highest when the via-hole (d: 60 μm) joints were used, which was as high as 23.7 percent. However, the results indicate that the voids content of no via and capped via-hole joints were very comparable, regardless of the existence of via-holes, as shown in Figure 8.6. From the statistical result of two sample *t*-tests, it can be observed that two via-hole types were not statistically different (*p*-value > 0.05). This suggests that the micro via voiding performance of both no via and capped via-hole joints should be comparable, at least in the case of using 95wt.%Sn–5wt.%Sb solder alloy system.

Comparing the percentage of opened via-hole joint groups versus the percentage of capped via-hole joint groups; there was an apparent inverse correlation, as shown in Figure 8.7. It was necessary to determine if the difference observed was statistically significant. The statistical results are shown in Table 8.4. The results show that the *p*-value was 0.000 for each via-hole joint group. This value of the two sample *t*-test indicates that the two via-hole joint groups were statistically different (*p*-value < 0.05), and the capped via-hole joint groups clearly had a role in reducing voiding at solder joints.

For the three representative cross-sectional view of voiding in the solder joint, as shown in Figure 8.8, (a) small via-in-pads generated voiding in solder joint, but these were smaller than the voiding in the (b) large via-in-pads. In the case of (b) large via-in-pads, it was found that the largest voids were located between the chip component and the opening of via-hole, while the voiding was connected to the inside of the via-hole. No voiding was observed in the (c) capped via-in-pads.

In this study, the via-hole size had a dramatic effect on void formation. This is in agreement with the information presented by Grano *et al.* [83] about the effect of via-hole size on void formation. Voiding is a phenomenon commonly associated with solder joints involving micro via [82]. Figure 8.9 shows a schematic view of void formation for the large via-holes and

the small via-holes. If via-holes are unfilled, the entrapped flux will result in void formation in solder joints. From Figure 8.9, larger space in the (a) large via-holes will generate more entrapped flux than (b) small via-holes, and the higher void content associated with larger entrapped flux. In other words, the outgassing of entrapped flux is directly responsible for the voiding formation in the solder joints with micro via-holes, and lower voiding content means a smaller amount of entrapped flux [14].

TABLE 8.4 Void measurement results for each via-hole size

			Voiding (area %)			
Micro via-in-pad type		***n***	**Mean**	**SD**	**SE mean**	***p*-value**
Opened via-hole (via-hole size)	d: 10 μm	20	5.090	1.567	0.350	0.000 ($p < 0.05$)
	d: 20 μm	20	13.115	5.281	1.180	
	d: 60 μm	20	23.725	3.683	0.824	
Capped via-hole	No via	20	1.935	0.844	0.190	0.430 ($p > 0.05$)
	Capped via	20	1.745	0.646	0.140	

Notes: SD - standard deviation; SE mean - standard error mean

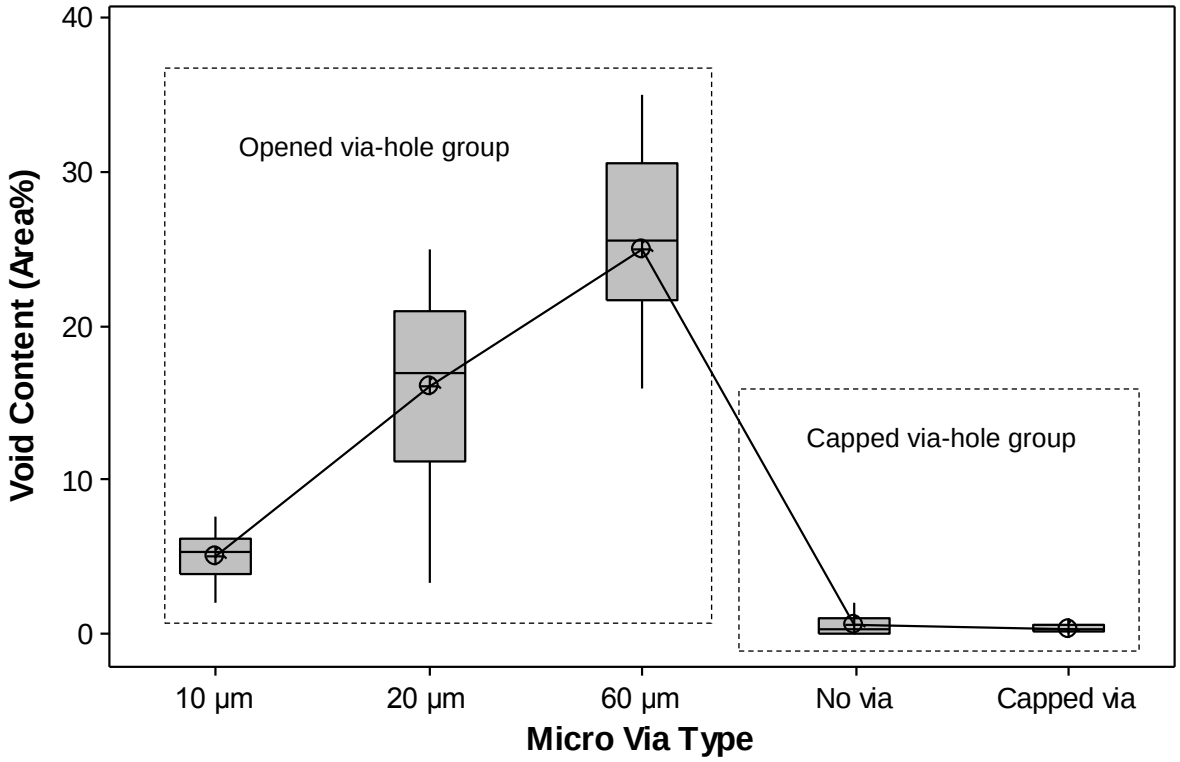


FIGURE 8.6 Relationship between micro via-hole size and voiding.

Note: The box plot shows the smallest value, the first quartile (Q1), the median, the third quartile (Q3), and the largest value.

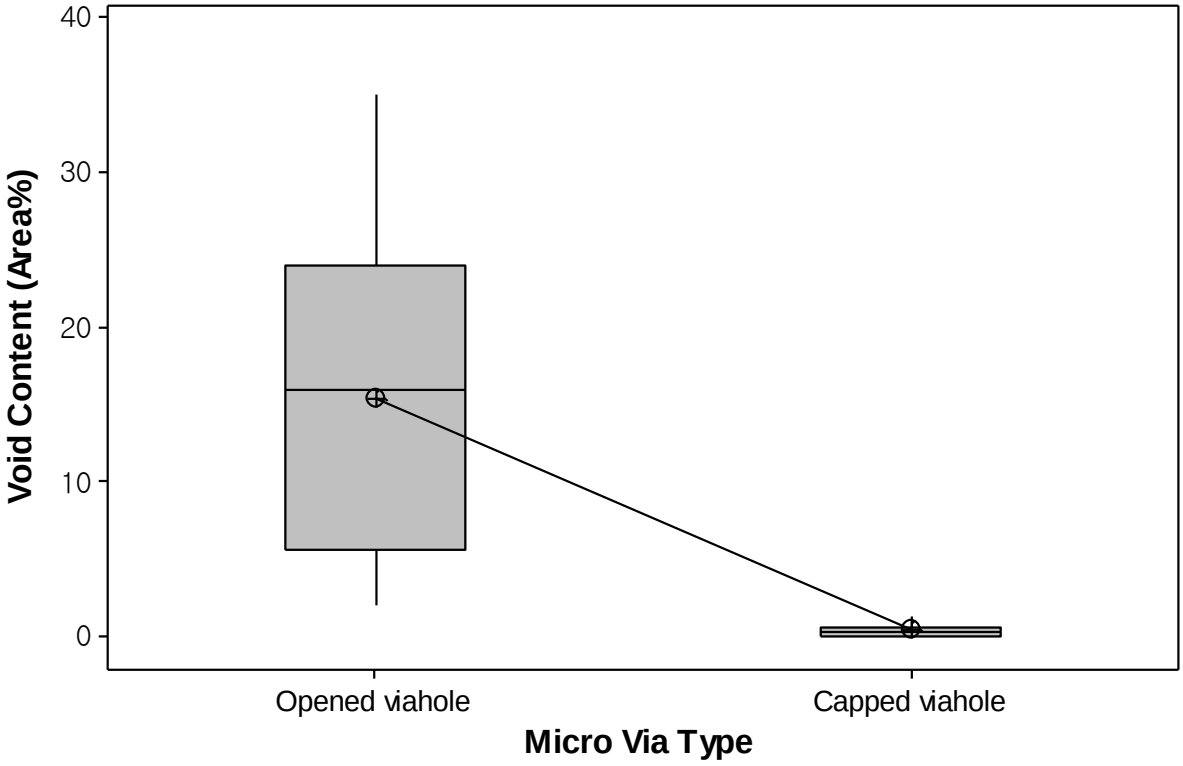
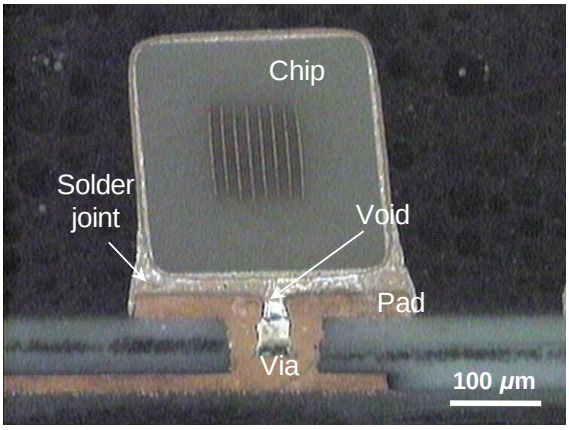
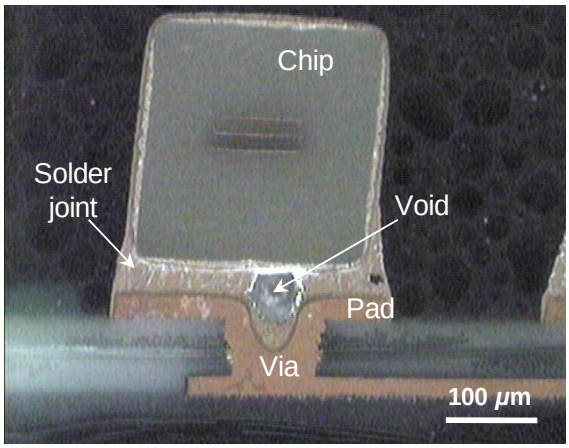


FIGURE 8.7 Void content comparisons for each via-hole group.

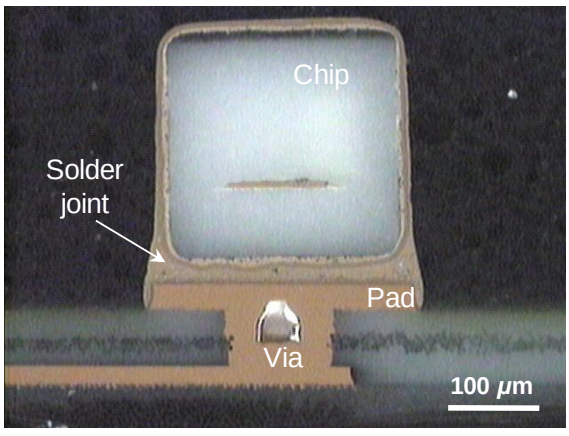
Note: The box plot shows the smallest value, the first quartile (Q1), the median, the third quartile (Q3), and the largest value.



(a)



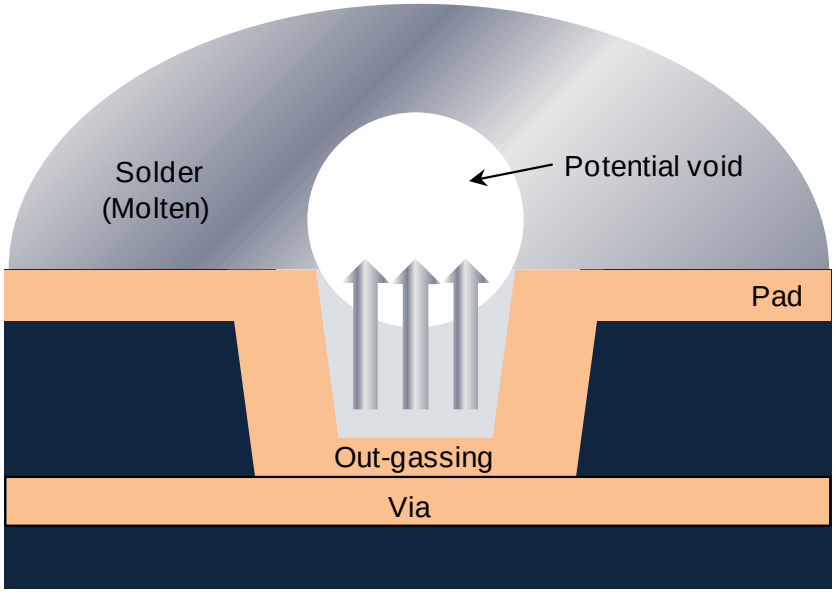
(b)



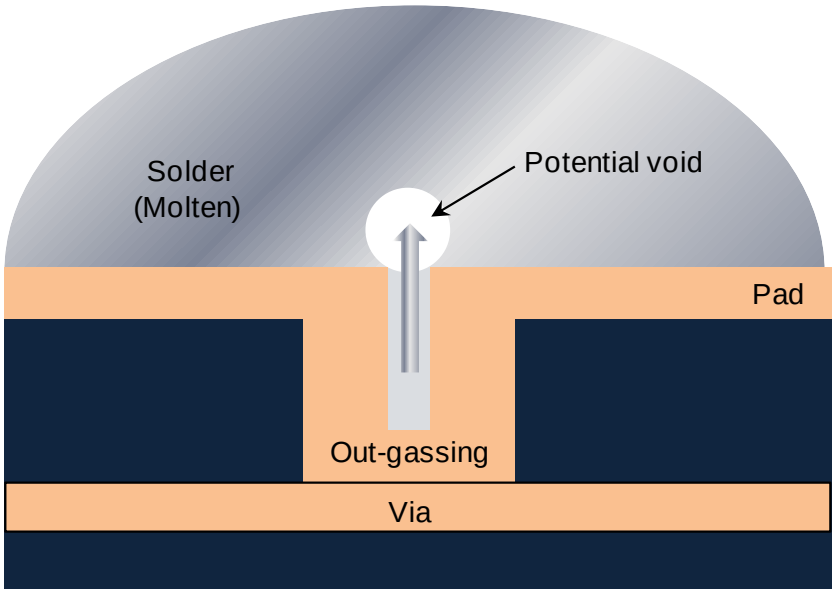
(c)

FIGURE 8.8 Representative cross-sectional view of voiding in the solder joint at micro via-in-pads.

Notes: (a) Small via-in-pad; (b) large via-in-pad; (c) capped via-in-pad.



(a)



(b)

FIGURE 8.9 Schematic diagram of voiding formation in the solder joints with different micro vias.

Notes: (a) Large via-in-pad; (b) small via-in-pad.

8.3.2 The effect of micro via-in-pad designs on spattering

The effect of micro via-in-pads on the occurrence of spattering was studied as shown in Figure 8.10. Ultra-small via-in-pads (d: 10 ㎛) produced the worst results, with 1.7 percent, and spattering rate was reduced by 1.2 percent with the small via-in-pads (d: 20 ㎛). No spattering was observed in large via-in-pads (d: 60 ㎛), no via-in-pads, and capped via-in-pads.

The spattering rate decreases rapidly with increasing via-hole size in micro via-in- pads, as indicated by Figure 8.10. This can be explained by the equation of continuity of fluid [133]. With the smaller the tube opening area, the faster the flow becomes, and the larger the tube opening area, the slower the flow becomes. In other words, in the case of the ultra- small via-in-pads (d: 10 ㎛), as the via-hole opening gets narrower the flux flow gets faster, and the outgassing force of entrapped flux can be stronger than that of large via-in-pads (d: 60 ㎛).

To confirm this phenomenon, a solder reflow test was performed with the same test vehicles in which no components were placed, and only solder paste was printed on the pads. For example, the components were found to decrease the impact of spatters, presumably by blocking expelled flux from the via-hole. The same 95wt.%Sn–5wt.%Sb solder paste and reflow profile were used as the baseline performance. The results for the entire test vehicle are shown in Figures 8.11 and 8.12. In the large via-in-pads in Figure 8.11, the via-hole is exposed on the soldered pads. In contrast, in the small via-in-pads in Figure 8.12, the shape of the via-hole is not identified, as the soldered pads were severely ruptured. This can be explained by the mechanism discussed above. The outgassing of entrapped flux spurred out more strongly through the small via-in-pads (d: 10 ㎛) than through the large via-in-pads (d: 60 ㎛).

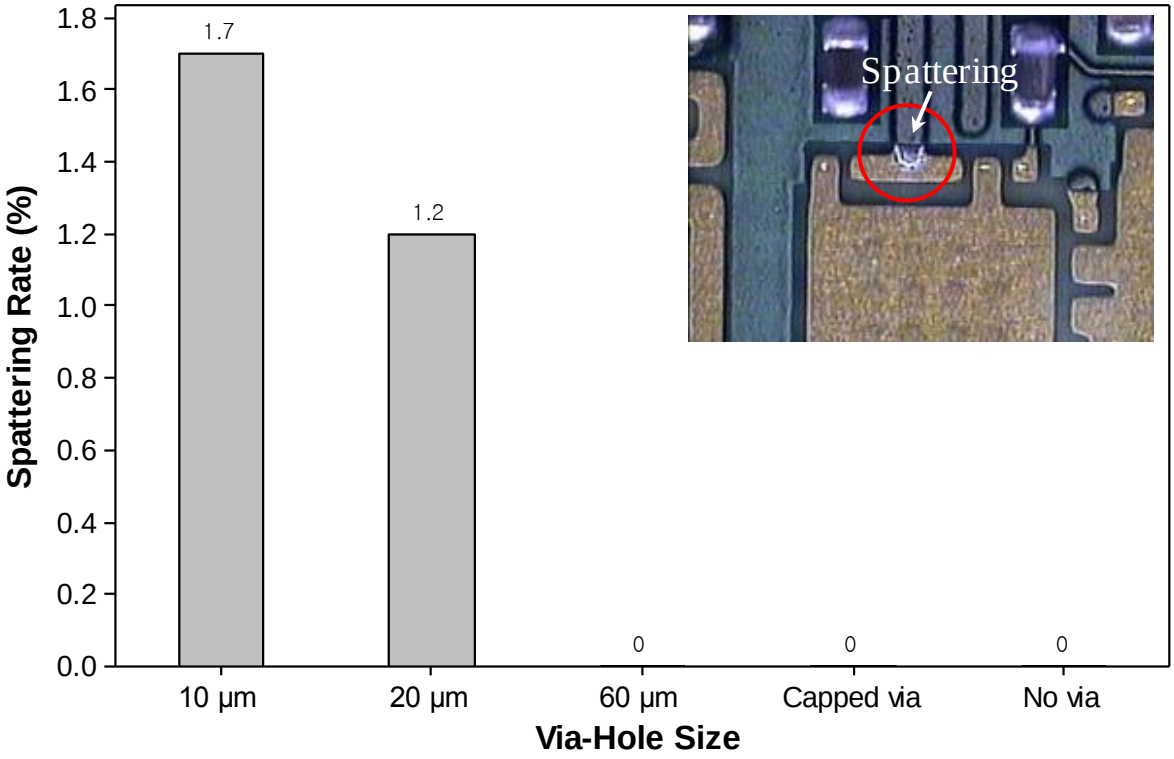


FIGURE 8.10 Relationship between micro via-hole size and spattering rate.

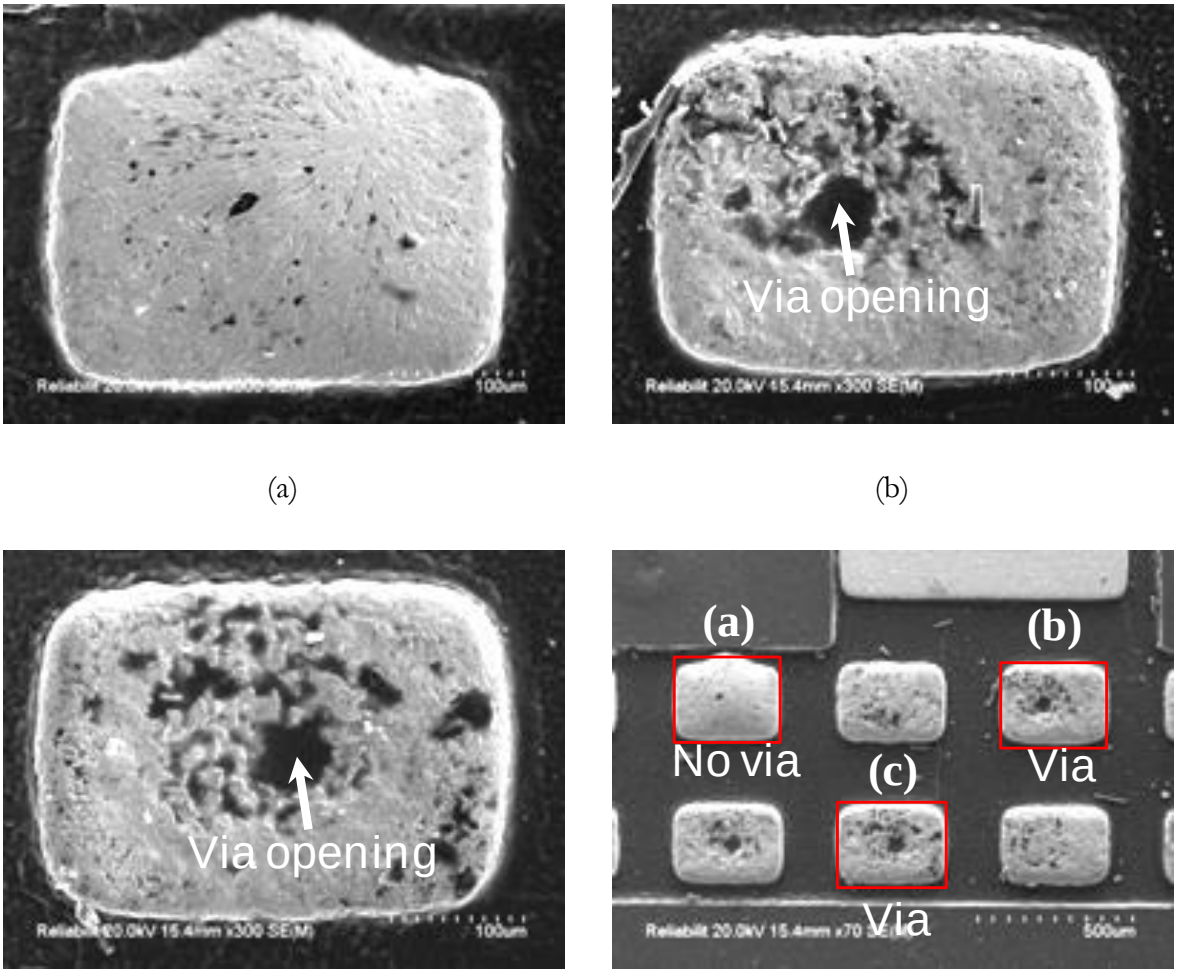


FIGURE 8.11 The results of a solder reflow test with large via-in pads (d: 60 μm).
Notes: (a) No via-in-pad; (b), (c) via-in-pads.

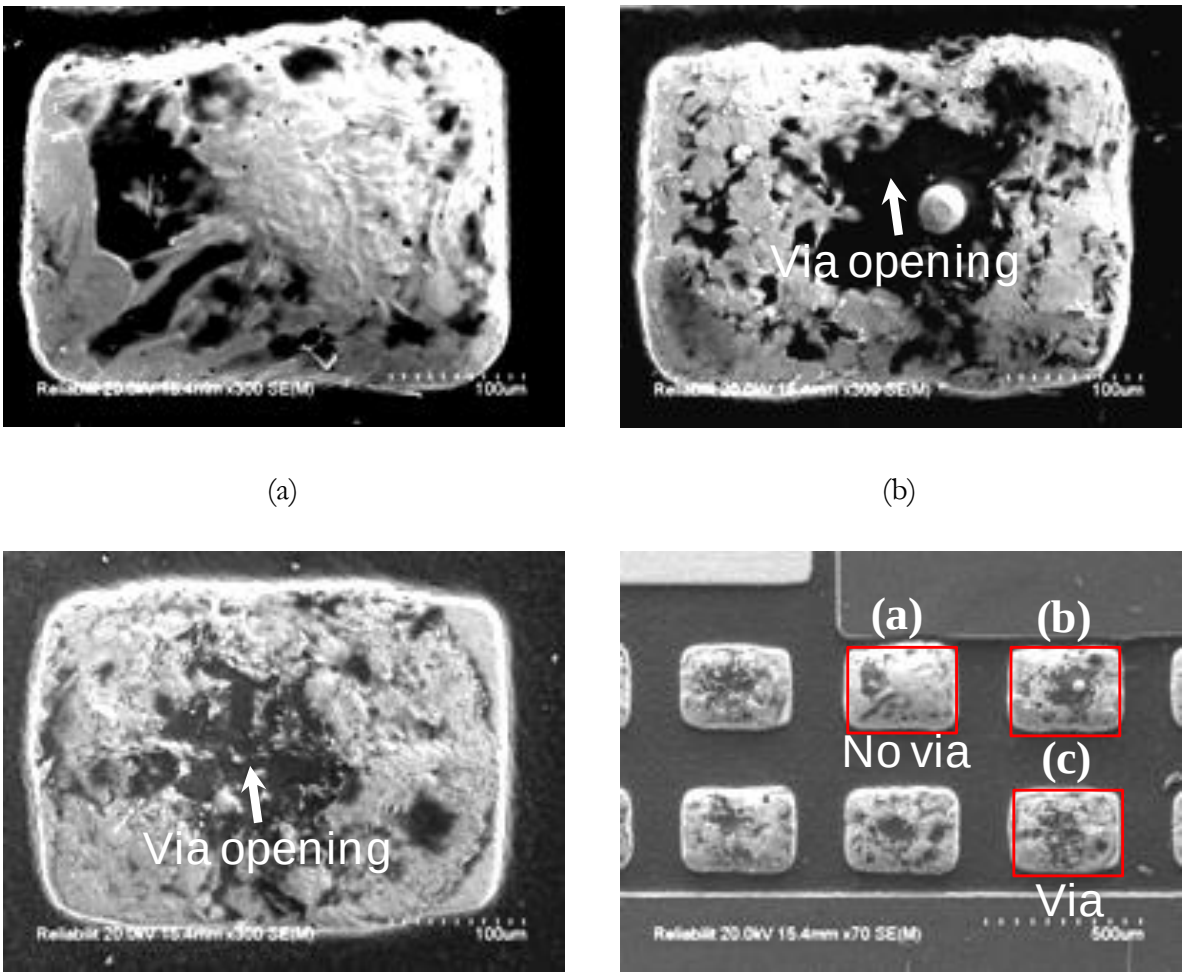


FIGURE 8.12 The results of a solder reflow test with small via-in pads (d: 20 μm).
Notes: (a) No via-in-pad; (b), (c) via-in-pads.

8.3.3 The effect of stencil opening size on spattering

The effect of the stencil opening size on spattering rate was studied by comparing the solder paste volume, as shown in Figure 8.13. The stencil opening ratio was 80, 90, and 100 percent.

The spattering rate was the highest when the ultra-small via-in-pads (d: 10 μm) were used at 80 percent stencil opening ratio, which was as high as 8.0 percent, and the spattering rate reduced rapidly with increasing stencil opening ratio. In the case of small via-in-pads (d: 20 μm), the spattering rate was 2.7 percent at 80 percent and 1.4 percent at 90 percent stencil opening ratios, and no spattering occurred at 100 percent stencil opening ratio. No spattering was observed in large via-in-pads (d: 60 μm), no via-in-pads, and capped via-in-pads for all stencil opening ratios.

The study revealed that, generally, as the stencil opening ratio increased, the amount of spattering reduced, and the amount of spattering that was generated was dependent on solder volume delivered. This result suggests that it is important to maximize solder paste volume to prevent spattering in use of micro-via substrates. This can be explained by the fact that the larger solder paste volume can be helpful, presumably by blocking expelled outgassing of entrapped flux from the via-in-pads.

8.3.4 The effect of reflow profile on spattering

The effect of reflow profile on spattering rate was studied by comparing the two preheat reflow conditions with the results shown in Figure 8.14. As expected, no spattering occurred in both no via-in-pads and capped via-in-pads. Spattering was observed in only 0.4 percent in the reflow profile with the short-preheat condition for the large via-in-pads (d: 60 μm), and no spattering was observed for the reflow profile with the long-preheat condition. For the small via-in pads (d: 20 μm), the spattering rate was 1.7 percent in the reflow profile with a short-preheat condition, but it was slightly reduced to 1.3 percent in the reflow profile with the long-preheat condition. The ultra-small via-in-pads (d: 10 μm) showed the highest spattering rates (2.9 percent) in the profile with the short-preheat condition, but it rapidly reduced to 1.3 percent when the reflow profiles with the long-preheat condition was applied. The overall tendency was that the reflow profile with the long-preheat condition was somewhat effective in reducing the occurrence of

spattering, but it could not completely remove the spattering defect in the use of ultra-small micro via-in-pads with the 95wt.%Sn–5wt.%Sb solder alloy system.

For real-time observation of the spattering behavior, the entire reflow process was observed *in-situ* with an SMT scope (Figure 8.15). The preheat zone, 0-140°C, was where the flux was activated, but no spattering was observed in this zone. Also, no spattering was observed in the soak zone, 140-190°C, either. Spattering began to be evident when the temperature became elevated above 232°C. At a composition of 95 wt.%Sn–5wt.%Sb, the solder begins to melt at the solidus temperature of 232°C [134]. As the solder melting started, the flux accumulated in the via-hole pushed the solder out. Therefore, the flux can be spattered around the metal pads with melting solders. This result indicates that control of the duration of the preheat zone at 140°C to evaporate all solvents.

In general, spattering decreases with either increasing drying time or increasing drying temperature [91]. The positive effect of drying on spattering could be attributed to the following reasons:

- The moisture pickup is dried out.
- More oxide buildup during drying, thus showing downs the coalescence process.
- The flux is becoming more viscous due to loss of volatiles, therefore reacting more slowly with solder oxide.
- The solder powder coalesces more slowly due to a more viscous flux medium.

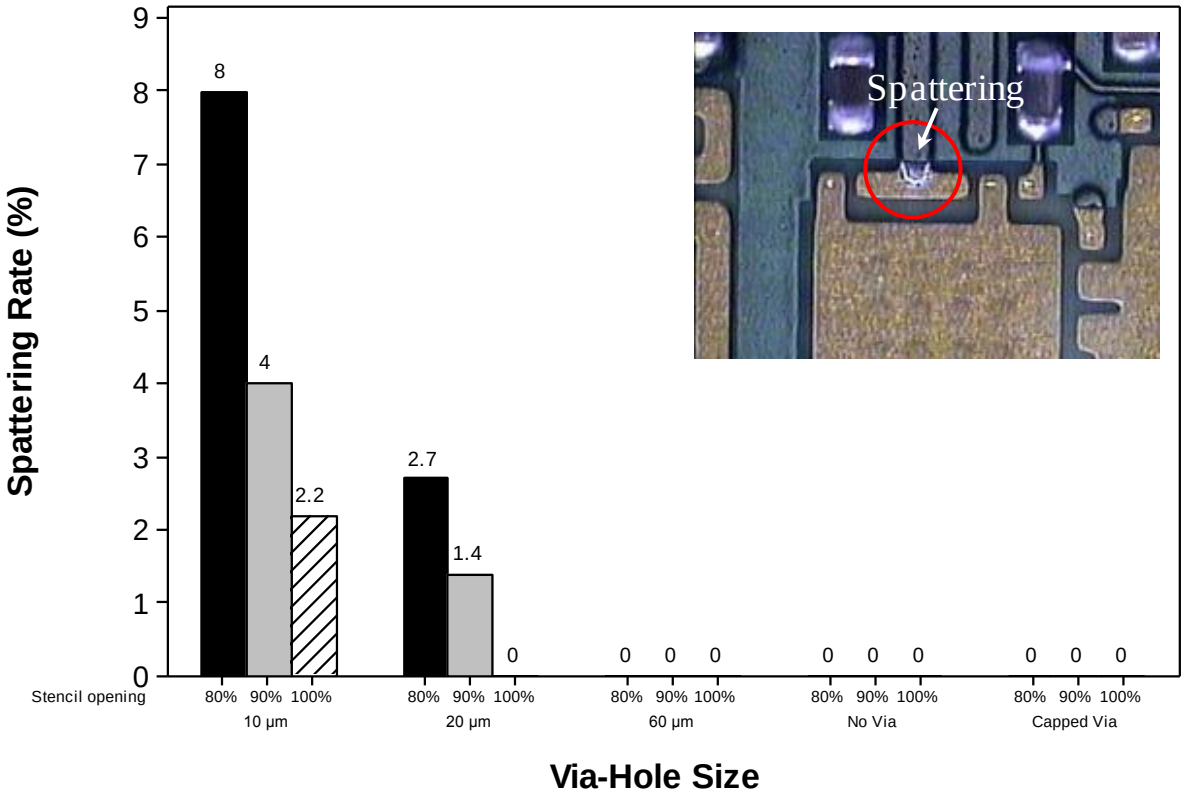


FIGURE 8.13 Relationship between stencil opening ratio and spattering rate in micro via-in-pads.

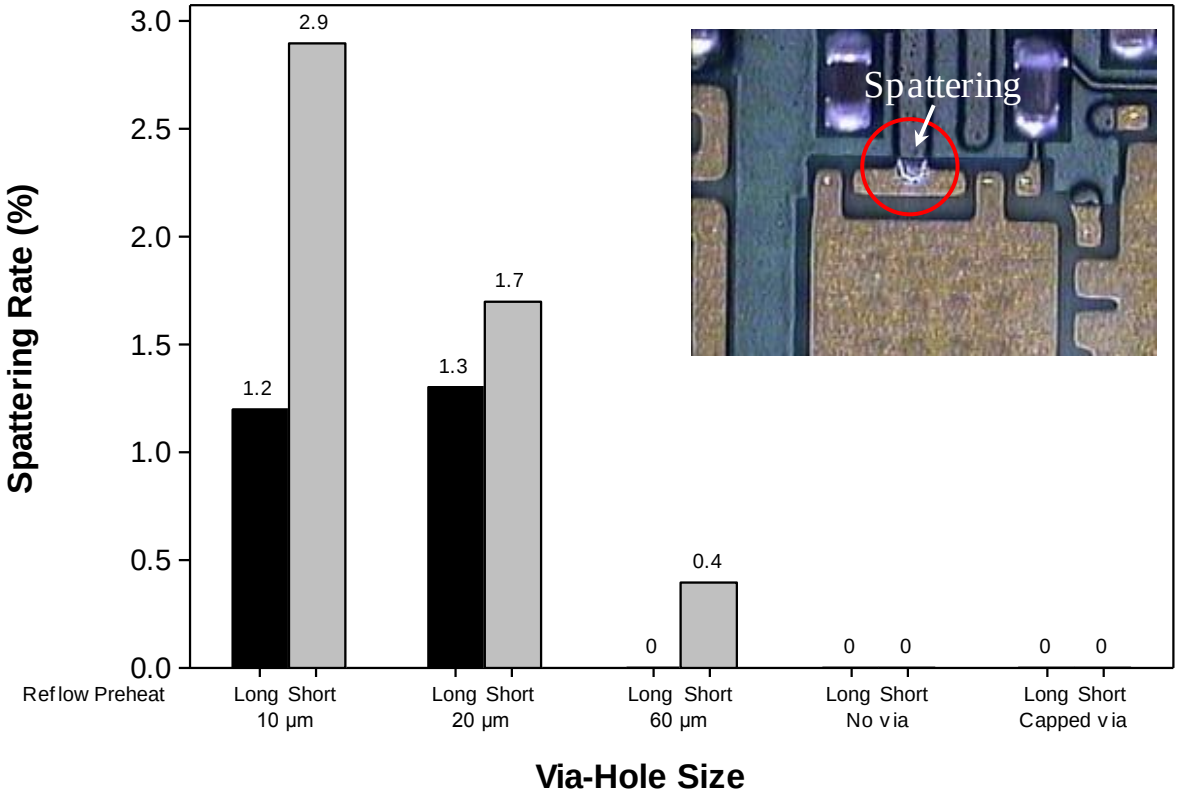


FIGURE 8.14 Relationship between reflow preheat condition and spattering rate in micro via-in-pads.

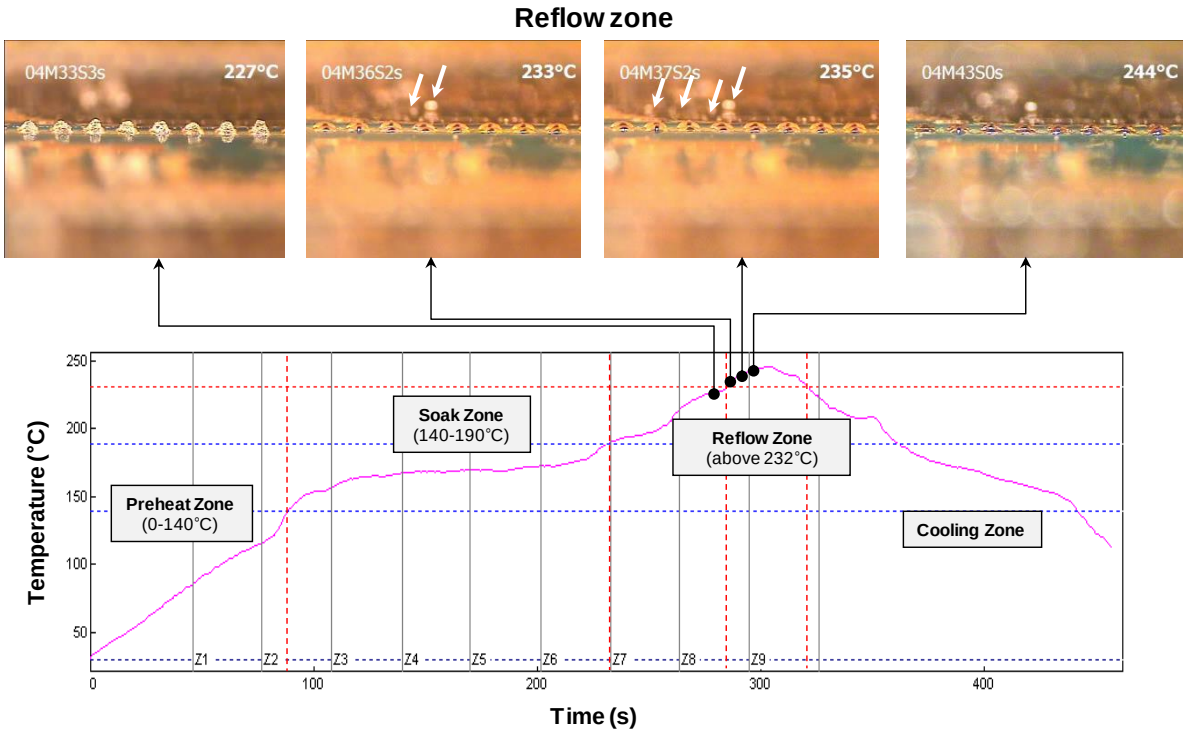


FIGURE 8.15 SMT scope images of reflow process for spattering phenomenon.

Note: The solder droplet on the pad, indicated by the arrow.

8.4 Summary

In this work, we obtained the following test results were observed regarding the relationship between micro via-in-pad design and SMT defects, such as voiding and flux spattering:

1. Micro via-in-pads greatly affected the occurrence of voiding in the assembly of 0201 chip components. In the small via-in-pad design, the possibility of voiding becomes lower and for the larger the via-hole size, the greater the occurrence of voiding. A capped via-in-pad and no via-in-pad were effective in reducing the occurrence of voiding.

2. In the via-in-pad design, it was shown that the smaller the via-in-pad designs, the greater the possibility of spattering becomes. The highest spattering rate occurred during use of ultra-small via-in-pad design (d: 10 μm). A capped via-in-pad and no via-in-pad were effective in reducing the occurrence of spattering.

3. The long-preheat conditions of the reflow profile were effective in reducing the occurrence of spattering, but it could not completely remove the defects in the use of ultra-small via-in-pads and 95wt.%Sn–5wt.%Sb solder paste.

Therefore, from the above, capped via-in-pads, larger stencil opening size, and the use of a reflow profile with long-preheat conditions are highly desirable, if the micro via-in-pad design and lead-free soldering is considered in the SiP module assembly process.

PART V: LEAD-FREE REWORK AND RELIABILITY

Chapter 9

The effects of reworked board assemblies with lead-free BGA packages[9]

The purpose of this chapter is to evaluate rework assembly processes in order to minimize defects and the present work is to study the effect of the reworked board assemblies with lead-free BGA packages. This study focuses on reworked BGA components (208 balls) using flux-only application method without the addition of the semi permanent metal stencil printing process. As process evaluations, two pads clean-up methods have been compared and conclusions drawn from the resultant pads clean-up. A suitable reflow profile was developed for component removal and replacement. Thermal cycling and drop impact testing was conducted for board level reliability of the package sample. The reworked BGAs passed through thermal cycling of up to 1,180 cycles without failures. However, the reworked BGA components show an approximate 36 percent reduction in the drop reliability over the non-reworked BGA components. The adjacent passive component was also degraded the shear strength after the rework process, resulting in a joining reliability reduction of approximately 24 percent.

[9] Based on Yong-Won Lee (2013), "Process characterization and reliability for the reworked assemblies with lead-free BGA packages", *Soldering & Surface Mount Technology* (in press).

9.1 Objective and overview

The trend by the electronics industry toward the miniaturization of electronic assemblies resulted in the development of BGA packages [96]. Although BGAs provide density and yield advantage, they also provide the assembler with rework obstacles. With solder bumps hidden from view, reflow cannot be visually verified.

Due to the narrow process window available for lead-free BGA components rework, it is essential to conduct a comprehensive study researching various alternatives for each rework process step in order to arrive at a reliable and repeatable rework process. Issue associated with rework assembly process, using lead-free Sn-Ag-Cu solder alloys, is the comparatively high melting temperatures of these alloys when they are compared to the eutectic Sn-Pb alloys [135,136]. Additionally, the PCB is subjected to multiple reflow cycles during the BGA rework process of removing the components, cleaning the site, and soldering the new components. The high processing temperature and the multiple reflow may result in the degradation of the reliability of the solder joint and the quality of the solder joint. This high temperature may also influence the components that are adjacent to the reworked area. Gleason *et al.* [37] have reported that the reliability performance of adjacent components resulted in significant reduction in thermal fatigue resistance.

This study on the effects of rework board assemblies with lead-free BGA packages is divided into two main parts. The first part of the study examines the effect of the potential process factors such as pads clean-up methods and thermal profile on rework performance. Another part concerns how the flux-only application method without the addition of the application of solder paste in the BGA rework process affects joint reliability and this part of the study examines the effect of the rework process on adjacent components. The results are discussed below, along with the recommended optimal conditions.

9.2 Experimental

The BGA component selected for this experiment was a 208 I/O, 0.8 mm pitch, 4-row perimeter and 15 mm body size, with 95.5wt.%Sn–4.0wt.%Ag–0.5wt.%Cu (SAC405) lead-free solder balls. Mechanical drawings of BGA package are shown in Figure 9.1. The BGA components that contained the actual active die were daisy-chained, but the electrical path was routed through the solder balls and the BGA substrate. The substrate daisy chain layout is shown in Figure 9.2.

The primary test vehicle, with BGAs and 0201R (0603 metric, 0.6 mm × 0.3 mm) passive components, was designed and the study used a 100 mm × 50 mm × 1.0 mm FR-4 board with an electroless nickel and immersion gold (ENIG) surface finish and NSMD pads. Test boards were custom-fabricated 8-layer printed wring boards (PWBs), designed to accommodate three test units per panel. Included in the test matrix were samples that had undergone a rework process. The test vehicle was designed as shown in Figure 9.3. The BGA-to-0201R chips placement gaps were set as 0.5 mm and 1.0 mm. Figure 9.4 presents a photograph of the test board with mounted components.

In first step of assembly process, the lead-free components were assembled using commercially available 96.5wt.%Sn–3.0wt.%Ag–0.5wt.%Cu (SAC305) solder alloy. The SMT process yield for all assemblies was 100 percent.

The original BGA assemblies were reworked using a manual and semi-automated hot gas system, the ZEVAC Onyx 29 machine. The independent pick-up tube is used for removing and replacing the components. The hot gas nozzle completely covers the BGA component and the nozzle size used was 16 mm × 16 mm. The nozzle-to-PCB clearance was approximately 2.0 mm. In Figure 9.5, the process flow of the rework process is shown. Rework requires a multiple reflow cycle to achieve removal and replacement. The component removal profile was considerably hotter than the rework soldering profile [98]. BGA components at the site to be reworked are heated, typically using a local convective hot gas nozzle, to raise solder joints above the melting point.

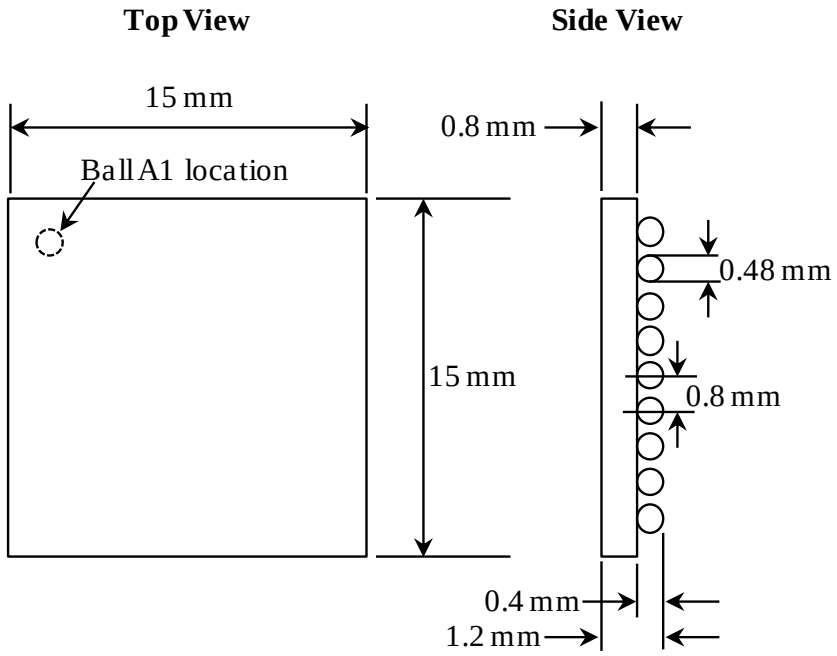


FIGURE 9.1 BGA mechanical outlines.

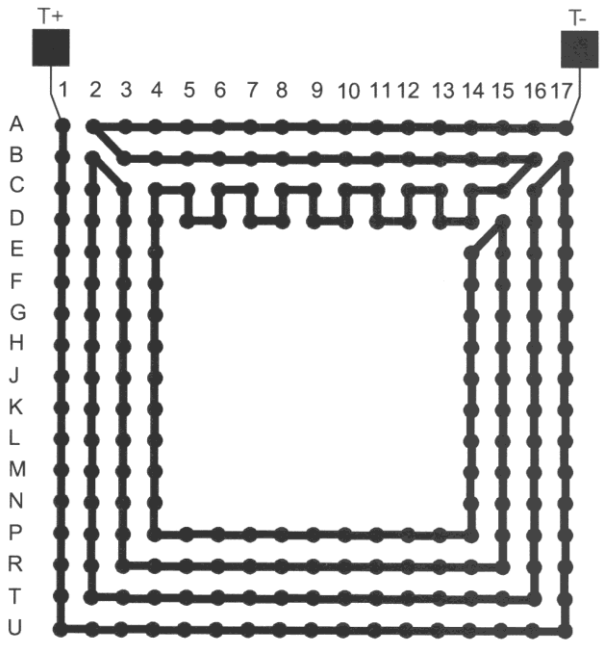


FIGURE 9.2 BGA208 test vehicle substrate daisy chains.

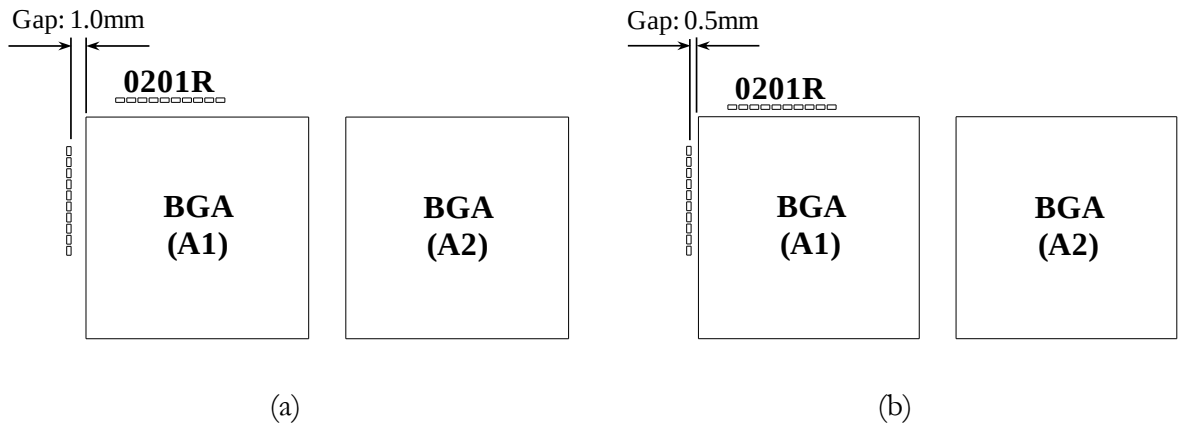


FIGURE 9.3 BGA-to-0201R chip placement gap scenario: (a) 1.0 mm; (b) 0.5 mm.

Note that A1 is BGA site to be rework and A2 is adjacent BGA site.

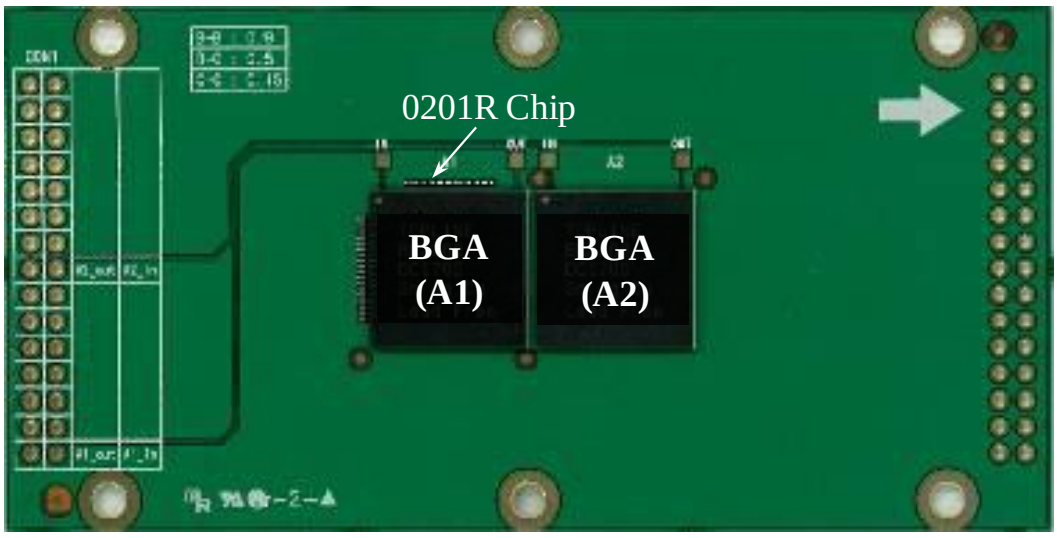


FIGURE 9.4 Photograph of the rework assembled test board.

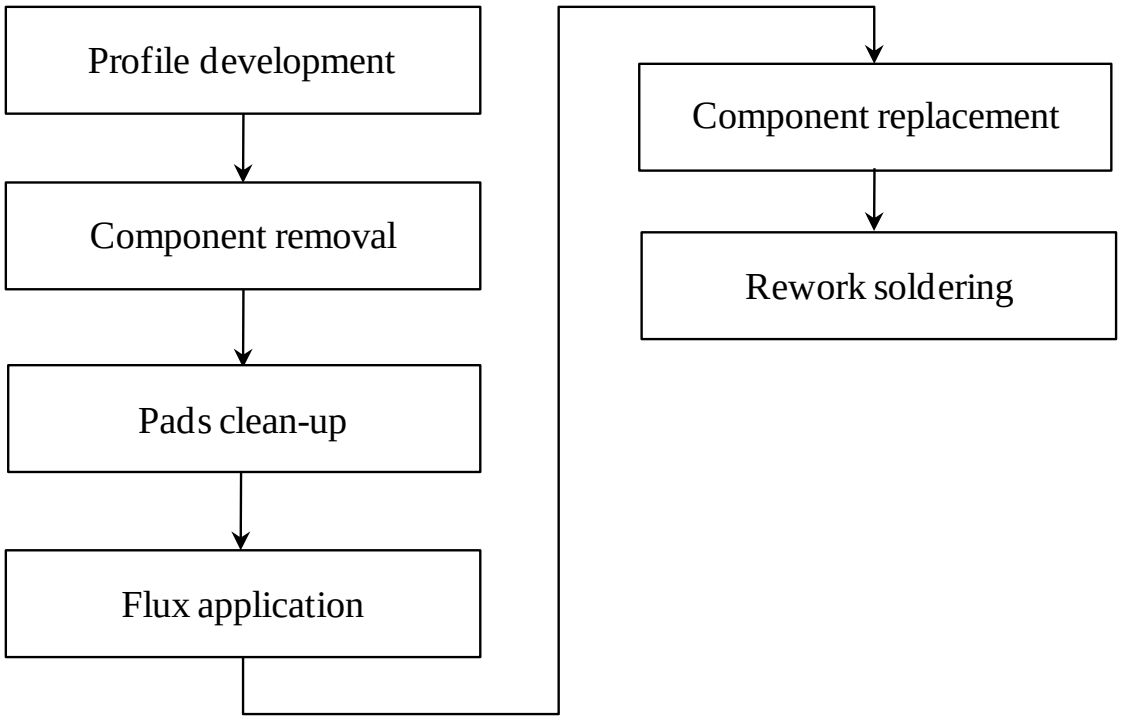


FIGURE 9.5 General BGA rework process flow.

After BGA components removal, the rework site must be dressed and cleaned for the attachment of a new component. This process is termed pads clean-up, and its purpose is to return the component site to as close to its original state as possible. In this study, two commonly used techniques for pads clean-up were evaluated: (1) manual soldering with iron and solder wick, and (2) semi-automatic system methods. In the manual soldering iron and solder wick method, contact clearance between soldering iron tip and pads were verified: (1) off-contact and (2) on-contact methods.

After pads clean-up, the site was cleaned with alcohol to remove any flux residues. And then a flux-only application method was used without the use of a semi-permanent stencil printing. The study used an OL107 flux, manufactured by Alpha Metals. A flux-applied pad is ready for the new BGA replacement step. The pick-and-place capability of a rework system is used to align and place the new BGA onto the pad of the rework site. Because the joints of the BGA components are hidden beneath the components.

Hot-gas rework profiles were created for removal and replacement. The time above melting point was calculated from the material's solder paste melting point of 220°C. Three thermocouples were used for thermo profiling. Figure 9.6 shows the locations of the three thermo couples and the rework setup. The major locations at which the temperatures were measured are: top of the BGA component (*ch1*), solder joint of the BGA component (*ch2*), and bottom-side of the BGA component (*ch3*).

After the rework process was completed, the outer rows of the solder joints were visually checked for misalignment, board delamination and damage of adjacent components.

For the warpage analysis, the high-speed imaging system was used with a digital image correlation (DIC) system to analyze the full-field image series captured by the cameras. DIC is a full-field optical measurement technique by which both in-plane and out-of-plane deformations can be computed by comparing the pictures of the target object at initial and deformed stages.

Thermal shock testing was conducted for board-level reliability of the package sample. 30 boards (90 BGAs) from each group (as-reflowed and as-reworked samples) were tested in a liquid-to-liquid thermal shock chamber. The cycle was heated from – 40 °C to 85 °C with 5 min. at each extreme and a 1 min. transition time. In this series of tests, the resistance of daisy chain

circuit patterns running between the BGA and test board after exposure to thermal shock was measured.

Drop impact testing was conducted for board level reliability of the package sample. 30 boards (90 BGAs) from each group were tested according to the JEDEC standard [137], which is a common test platform for handheld electronics products. The drop test was carried out at 1,500 G, for 0.5 ms duration time. The Lansmount model-30 drop test system was used for this work. A voltage-type accelerometer was mounted on a shock table to measure input acceleration. The bottom of the board was instrumented with a resistance wire strain gauge. The accelerometers measured the accelerations in the direction of the drop. The strain gauge measured the in-plane strain during the post-impact sessions. Three BGA components were mounted on a test board. This study used a double-sided board assembly. This board was connected to a fixture and a drop table with four corner screws. It fell from a height of 24 inches. After every drop, failure was measured and assessed against the following criterion: 100 ohm, with a data acquisition frequency of 20 kHz.

Shear testing of the 0201 passive component was also performed using a Dage 4000 Bond Tester. All shear testing was conducted at room temperature with a shear height of 50 μm and a pulling speed of 200 μm/s.

Determination of the failure mode for the test PBA subjected to thermal shock testing was conducted using two separated methods. The first technique involved cross-section analysis and preparing them using standard metallographic techniques to reveal the presence of cracks or other features such as voids. The second method was dye and pry analysis. In this case, test PBA that had been subjected to thermal shock cycling was immersed in a bath of machinist marking fluid, subjected to ultrasonic vibration, and then dried. The presence of cracks in the solder joints was then determined by visual inspection under a high-power microscope: pre-existing cracks caused by thermal shock testing were indicated by the bright red color of the dye on the fracture surface.

The microstructure and the fracture mode of the test PBA after the board-level reliability tests were observed with both the optical microscope and the scanning electron microscope (SEM). Interfacial intermetallic compound (IMC) formation was also observed, and the IMC thickness measurements using optical images were verified using a SEM. One as-reflowed BGA

component was also analyzed as a control to compare the IMC thickness before and after the rework processing. The data gathered from this experimentation was arranged, and the numerical time-to-failure data was analyzed statistically, using Minitab data statistical software.

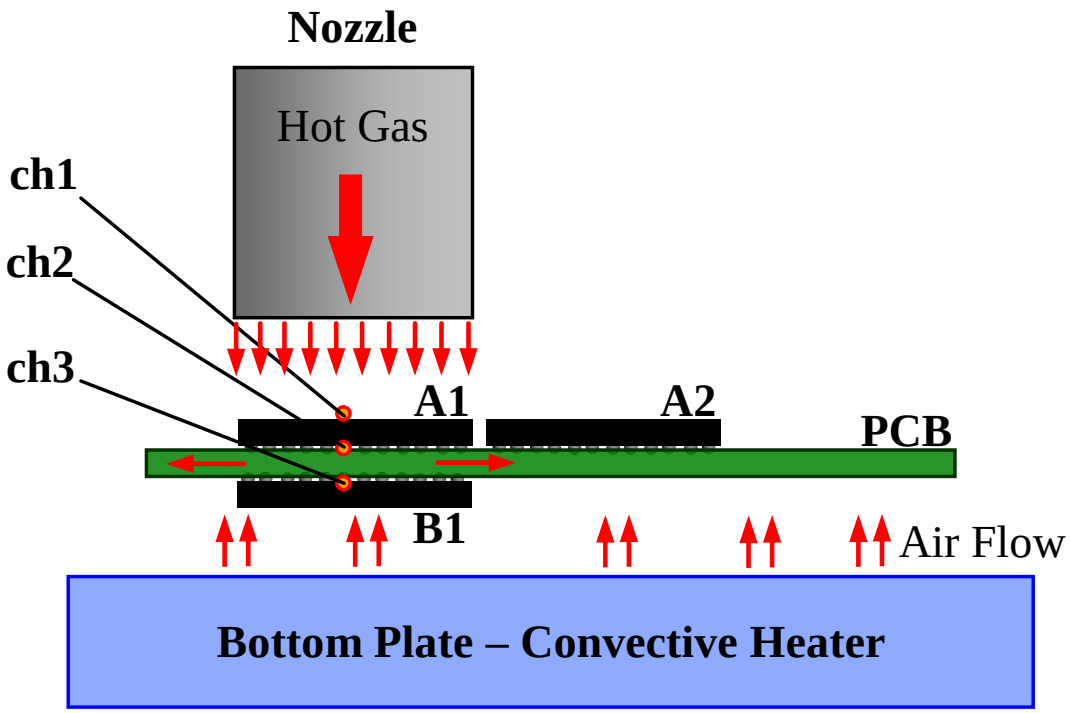


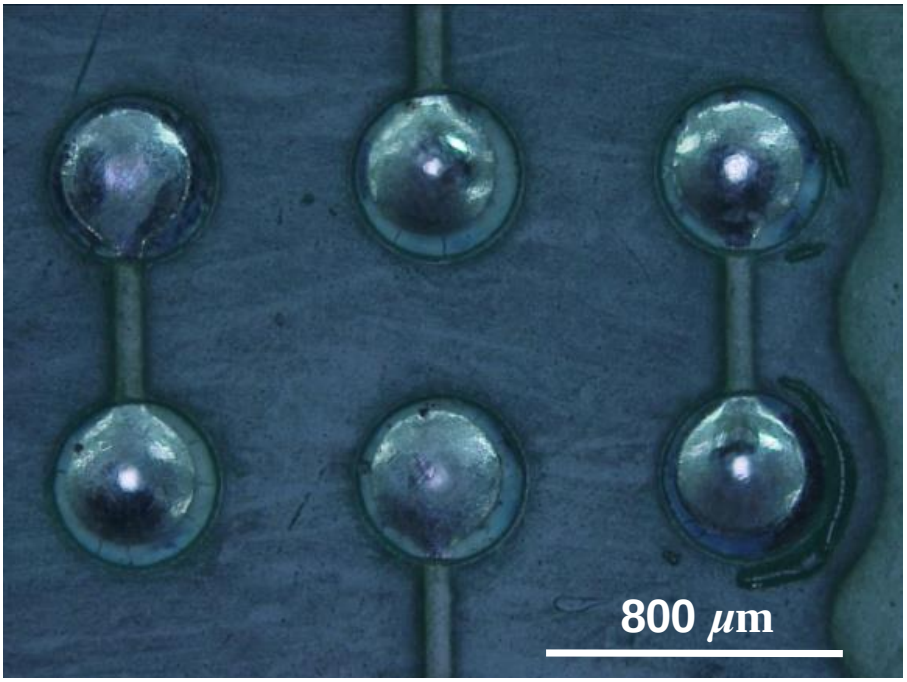
FIGURE 9.6 Illustration of thermocouple locations and heating system for BGA rework. Note that *ch1*, *ch2* and *ch3* are thermocouple locations.

9.3 Results and discussion

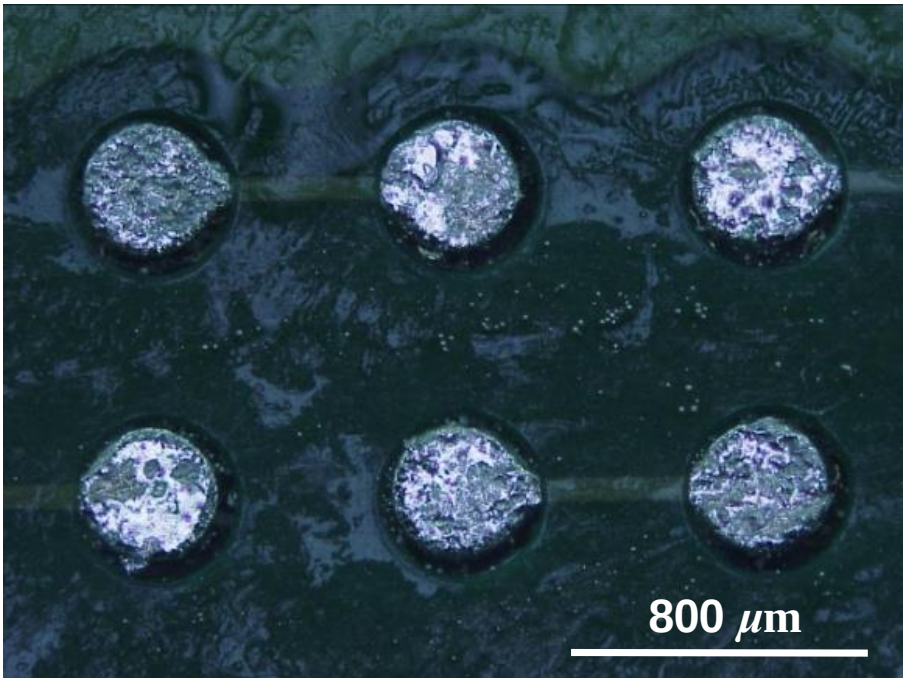
9.3.1 Pads clean-up process results

Pads clean-up is one of the most important stages of the rework process, and the purpose is to remove residual solder left by removal of the defective component and to return the pads on the component site to their original state as much as possible.

In this work, two different pads clean-up technique approaches were evaluated: (1) manual soldering iron and solder wick, and (2) semi-automatic system. The soldering iron and solder wick technique require the operator to be highly proficient to avoid any damage to the PCB. The pads were cleaned using a solder wick applied with an activated flux with a soldering tip temperature of 350°C. The semi-automatic system used a vacuum desoldering system that sucked up the residual solder leaving behind jagged pads for excess solder deposited. After ensuring that the pads were perfectly cleaned by both techniques, the pads clean-up quality was then inspected and compared with that of a new board as a reference. Figure 9.7 shows some representative photographs from pads cleaned with different techniques. Comparing soldering iron and solder wick versus a semi-automatic system for pads clean-up quality, soldering iron and solder wick showed significantly better quality than the semi-automatic system by the vacuum desoldering machine. However, many of the pads cleaned using soldering iron and the solder wick technique showed some signs of damage. This technique was highly operator-dependent, and the pads and solder mask were easily damaged. The important factors for the manual pads clean-up technique were found to be the soldering iron tip, the iron tip to pad clearance, the amount of flux application, the width of the solder wick and the operator's proficiency [98]. Meanwhile, the semiautomatic system technique of pads clean-up was found to be more repeatable and did not result in any solder mask and pads damage. In this work, no pads lift-off damage was observed since a highly skilled operator was prepared with a soldering iron and solder wick technique from the board.



(a)



(b)

FIGURE 9.7 A close-up view of the pads cleaned for each pads clean-up method.

Notes: (a) Manual soldering iron and solder wick; (b) semi-automatic system using a vacuum desoldering machine.

Minimum contact clearance between soldering iron tip and pads was verified by different methods before employing the manual soldering iron technique for this study. Figure 9.8 shows the schematic diagram of two methods. The on-contact method was a typical technique that requires a soldering iron making contact with the pads. Another technique used an off-contact, and the soldering iron to pads clearance was approximately 2.0 mm in this study. Comparing the process yield, the off-contact method appeared to have much more yield adequate than the on-contact methods during pads clean-up process. Some pads damage has arisen in the on-contact method, and special care must be taken to avoid damaging the solder mask and prepared pads. To clarify the cause, a cross-section was observed for units selected from both samples. The shapes of the pads cleaned were analyzed. The principle surface shapes identified included flat, convex, concave and inclined, as seen in Figure 9.9. In this work, all prepared pads were convexly shaped. Flat, convex and concave are deemed desirable for good pads clean-up quality, as inclined pads tend to be irregular and open interconnects between pads may also occur.

Heights of solder on pads were measured with a high-power microscope and compared with an original SMT solder reflowed pads as a reference. The average deposited heights obtained for 10 pads prepared using an off-contact method are shown below in Figures 9.10 and 9.11. The box plot reveals that the height of solder deposited pads in the as-reflowed sample was higher than that of the as-reworked sample. It could be due to the original SMT reflow pads having produced larger deposit volumes for solder paste than rework pads prepared.

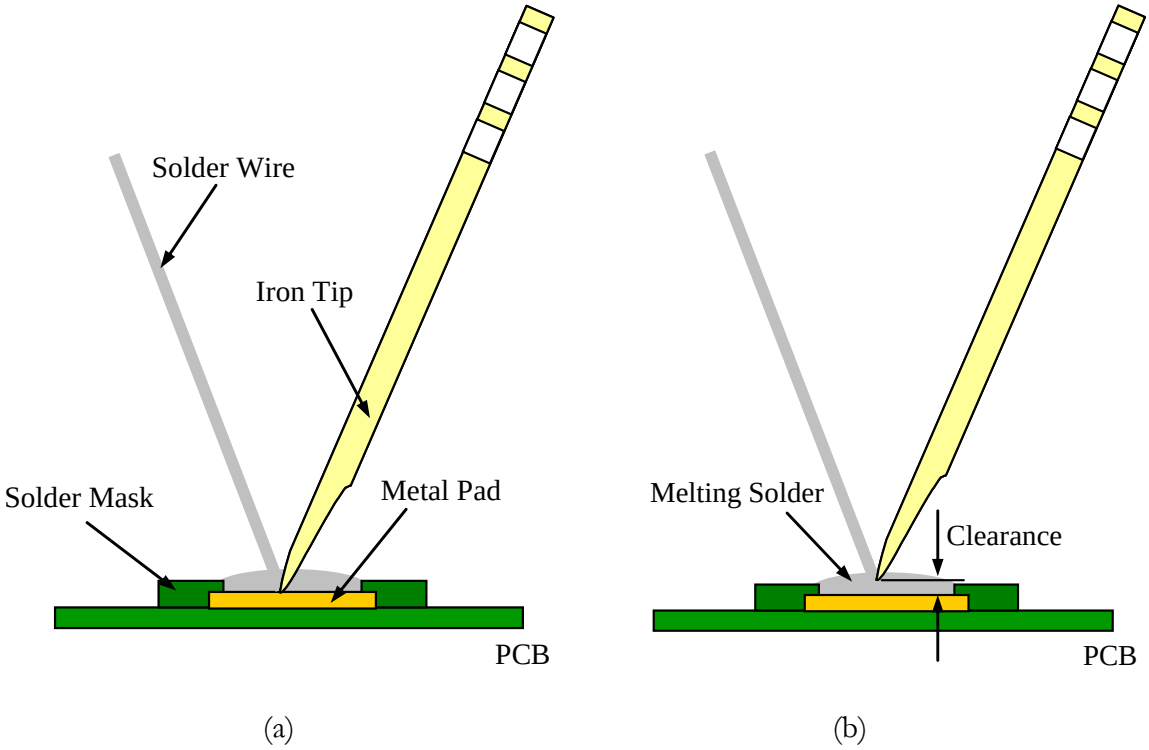
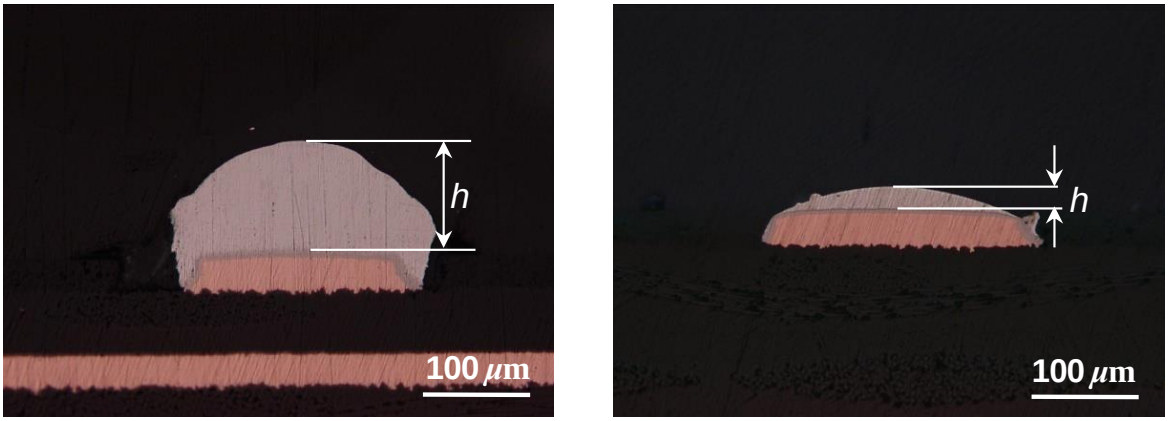


FIGURE 9.8 Schematic diagram of pads clean-up methods by manual soldering iron technique.

Notes: (a) On-contact; (b) off-contact.

FIGURE 9.9 Schematic diagram of solder deposited pads displaying surface shapes identified [28].

Notes: (a) Flat; (b) convex; (c) concave; (d) inclined.



(a) (b)

FIGURE 9.10 Cross-section of soldered on pads.

Notes: (a) As-reflowed soldered pad; (b) as-reworked soldered pad.

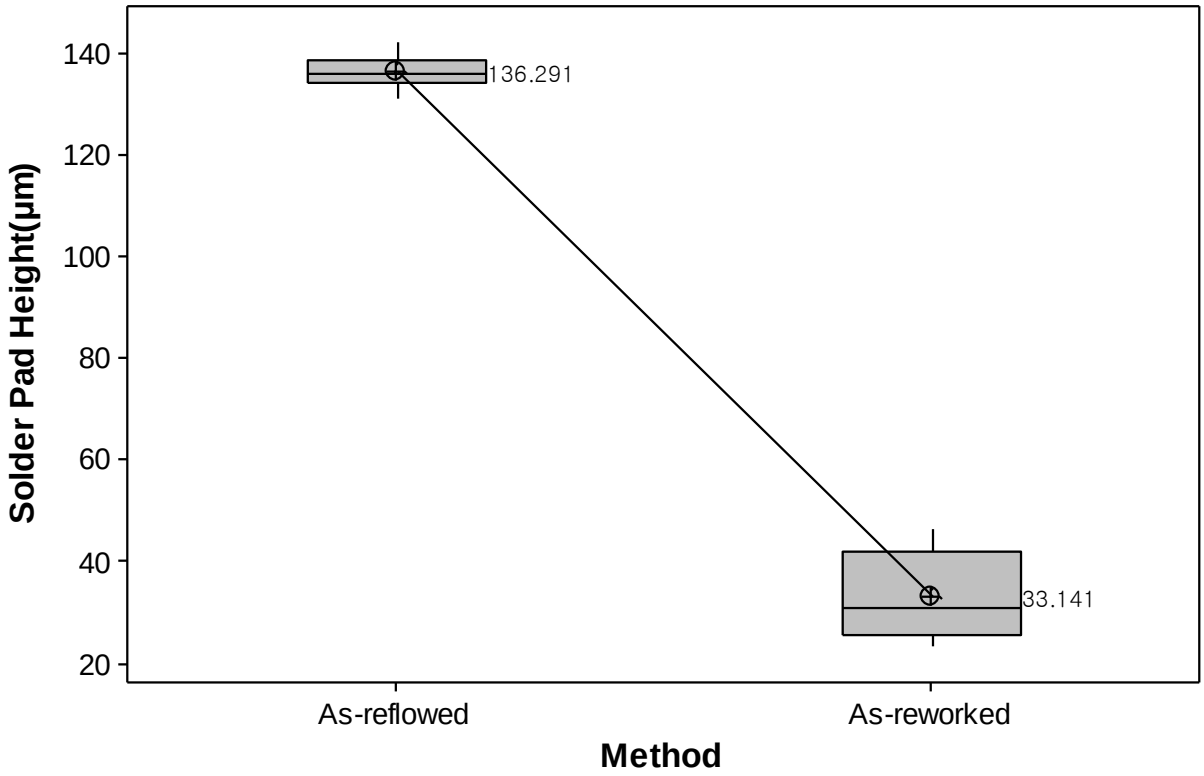


FIGURE 9.11 Resultant averages solder pad height.

Note that the box plot shows the smallest value, the first quartile (Q1), the median, the third quartile (Q3) and the largest value.

9.3.2 Thermal profile development

The thermal profiling work is a very challenging task in the lead-free BGA rework process. The most likely lead-free representative solder alloys, SAC305 or SAC405, have melting points in the range of 217-220°C. Since the same fluidity and wetting considerations will apply, it is reasonable to suggest that peak rework temperatures may reach the 235-245°C range. Thermal profiles were developed for component removal and replacement steps. The measuring profile is shown below in Figure 9.12.

For a better overview, just three representative measurements are depicted. The minimum solder joint temperature was approximately 231°C, while the maximum top of the component temperature was approximately 255°C and bottom component temperature was approximately 220°C.

The lead-free BGA rework temperature is near the limits of component specifications. So, it is very important that the thermal delta should be minimal while allowing sufficient heat to from form solder joints, which is very critical. However, one of the most difficult problems of proper BGA rework is board stability during the reflow process. In this experiment, the utility of the retrofit board fixture was evaluated to help establish better thermal control. Figure 9.13 shows a photograph of a retrofit board fixture between the rails of equipment. As a result, it was found that the retrofit board fixture played a significant role in the thermal profiling work and was very efficient in minimizing the thermal delta and shock to the PCB. This is shown explicitly in Figure 9.14 as results of IR imaging analysis during the rework heating process. The following Table 9.1 summarizes the thermal profiling parameters and results. As the results of measured temperatures, ΔT1 – temperature difference between the package top and solder joint – was 29°C, and ΔT2 – temperature difference between the package top and package bottom – was 48°C in no retrofit board fixture application. However, ΔT1 was 24°C and ΔT2 was 35°C in the retrofit board fixture application. When the use of the retrofit board fixture, thermal delta was slightly reduced. The preheating time was also shortening from 600 s to 300 s in the retrofit board fixture application. Therefore, preliminary tests suggest that the retrofit board fixture has proven to be the most efficient method of controlling the temperature of the PCB and thermal

uniformity during the rework heating process. More thermal profile development work is needed to support the elevated lead-free rework process.

TABLE 9.1 Thermal profile parameters

Thermal profile		**Peak temp. / Time above liquidus**			**ΔT1**	**ΔT2**
		Top (ch1)	**Solder joint (ch2)**	**PCB bottom (ch3)**		
Reflow		248°C / 47s	249°C / 48s	251°C / 50s	1°C	3°C
Rework	Without board fixture	257°C / 64s	228°C / 37s	209°C / 0s	48°C	48°C
	With board fixture	255°C / 63s	231°C / 41s	220°C / 0s	35°C	35°C

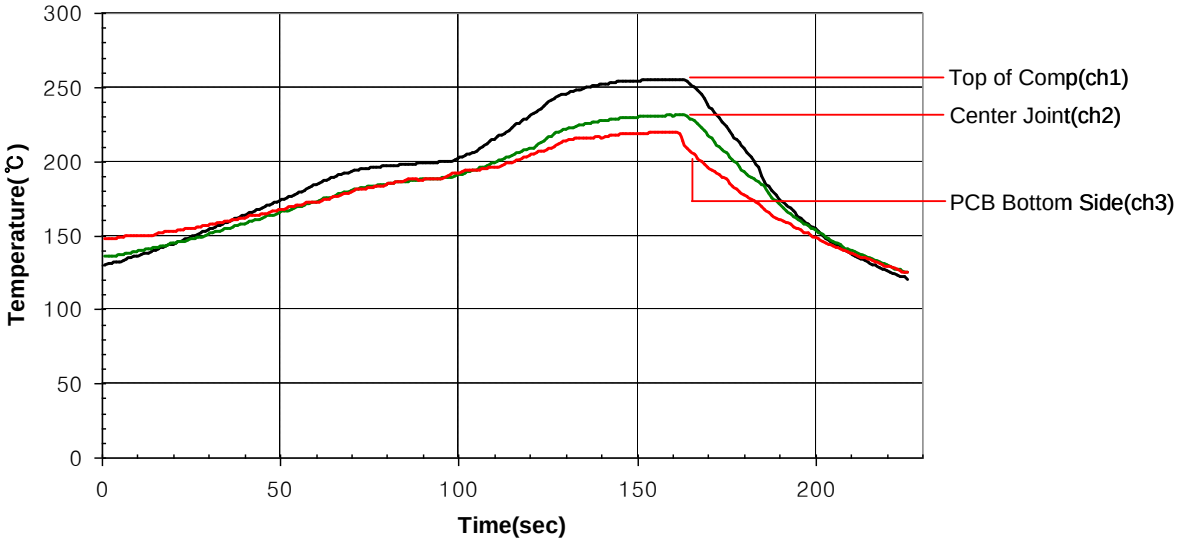


FIGURE 9.12 Thermal profile for lead-free BGA rework.

Notes: (ch1) Top of the BGA component; (ch2) solder joint of the BGA component; (ch3) bottom side of the PCB.

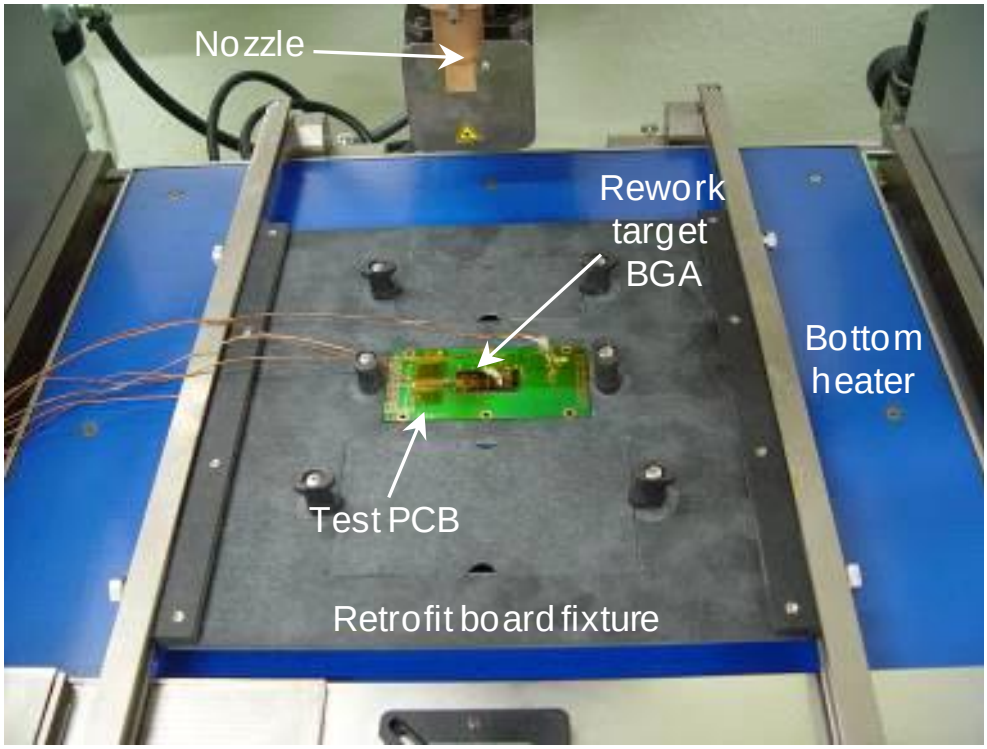
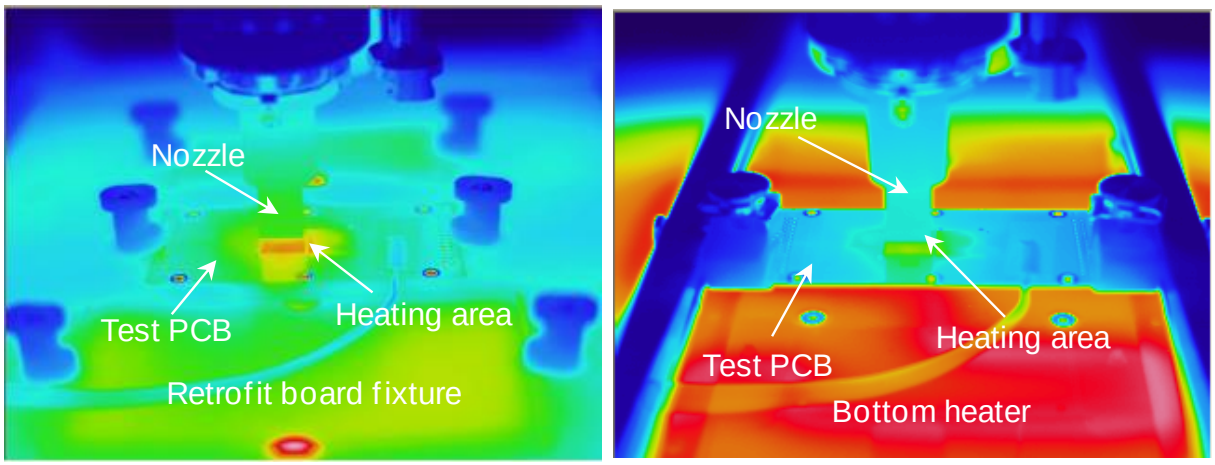


FIGURE 9.13 Photograph of retrofit board fixture applied.



(a) (b)

FIGURE 9.14 Result of IR imaging analysis.

Notes: (a) With retrofit board fixture; (b) without retrofit board fixture.

9.3.3 DIC measurement

Digital image correlation (DIC) measurement was performed to measure the amount of deformation induced by the high temperature reached during the rework process. Both the board itself and a set of components were measured, and observations have been made before and after rework. As a result, the maximum warpage for the reworked BGA component was found to be 0.030 mm, while the maximum warpage for the as-reflowed BGA component was 0.010 mm. There was a permanent deformation seen which was still within specifications after being submitted to a rework thermal cycle as shown in Figure 9.15. The maximum permissible component warpage for a 0.8 mm pitch BGA is 0.170 mm in specification by JEITA ED-7306 [138].

For the board warpage, a similar trend was observed. The maximum warpage was 0.210 mm for the as-reworked BGA board and only 0.170 mm for the as-reflowed BGA board. There was a slight change in the board warpage after the rework process as shown in Figure 9.16.

9.3.4 Reliability study

The thermal shock cycling test was terminated at 2,000 cycles. No failures were observed until after 1,000 thermal shock cycles in both as-reworked and as-reflowed samples. All samples exceed the typical 1,000 cycles required for most portable hand-held electronics applications [139]. With the exception of several instances of time-zero electrical failures, failures occurred at 82 and 222 cycles of rework samples. These were somewhat unexpected rework process defects such as component misalignment and cold joint. First failures during thermal cycling were observed in an as-reflowed sample at 1,500 cycles, and the first failure occurred in an as-reworked sample at 1,187 cycles. The effect of rework process on drop shock reliability was studied for BGA lead-free assemblies. Mechanical reliability is a statistical concept best represented by Weibull distribution. The mean life function, such as the mean time to failure (MTTF), is widely used as the measurement of a product's reliability and performance. This study observed a reliability difference between the reworked BGA and the as-reflowed BGA samples in the drop impact testing (Figure 9.17). The as-reworked BGA sample failed after 31 drops at the target rework BGA component (BGA-A1) and 56 drops at the as-reflowed BGA

sample. Weibull distributions of the data showed a MTTF of 231 cycles for the as-reworked BGA samples, while the mean time to failure for the as-reflowed BGA samples was 362 cycles.

Table 9.2 summarizes the drop testing results for both as-reworked BGA and as-reflowed BGA samples. By comparison, the as-reworked BGA components show an approximate 36 percent reduction in life expectancy over the as-reflowed BGA components.

The flux-only application method in the rework process is beneficial in that it is easy and fast; however it was found that the average life of the BGA components dropped significantly using this method when compared to that of the as-reflowed BGA components. The size of the BGA solder joints was considerably smaller than the size of the as-reflowed BGA components. This is because, solder paste was applied to the as-reflowed BGA components, using the metal stencil printing process in the early SMT process. No solder paste was applied to the BGA components during the rework process with flux-only application method. This difference in the solder volume affects the mechanical reliability; the smaller the solder volume, the less reliable. After the reflow, the solder height was measured, from the top of the solder to the top of the PCB pad. In the experiment using the flux-only method, the as-reworked sample turned out to be four times shorter than the normal components in their early stages (Figures 9.10 and 9.11).

Furthermore, the flux-only application method in the BGA rework process leads to a significant reduction in the mechanical life of the joint because the method cannot offset the difference in the levels between the components and the PCB pads. There is always a possibility for open solder joints in the assembly process, especially if the PCB pads are not level due to heat distortion from during the rework process. However such defects would be prevented if the solder volume was high enough.

X-ray inspection, cross-sectioning, and SEM analysis were performed on selected failed units from both sample groups. Typical X-ray images of the void distribution, in the Sn-Ag-Cu reworked solder joints between the BGA component and ENIG pads, are shown in Figure 9.18. Only minimal voids were observed and all solder joints were observed to be intact, with no evidence of a missing joint, smears, bridging, or other obvious defects.

TABLE 9.2 Drop shock test results summary

	Drops to 1st Failure		Mean Time to Failure (MTTF)	
Components	**As-reworked**	**As-reflowed**	**As-reworked**	**As-reflowed**
BGA-A1 (Top)	31	56	231	362

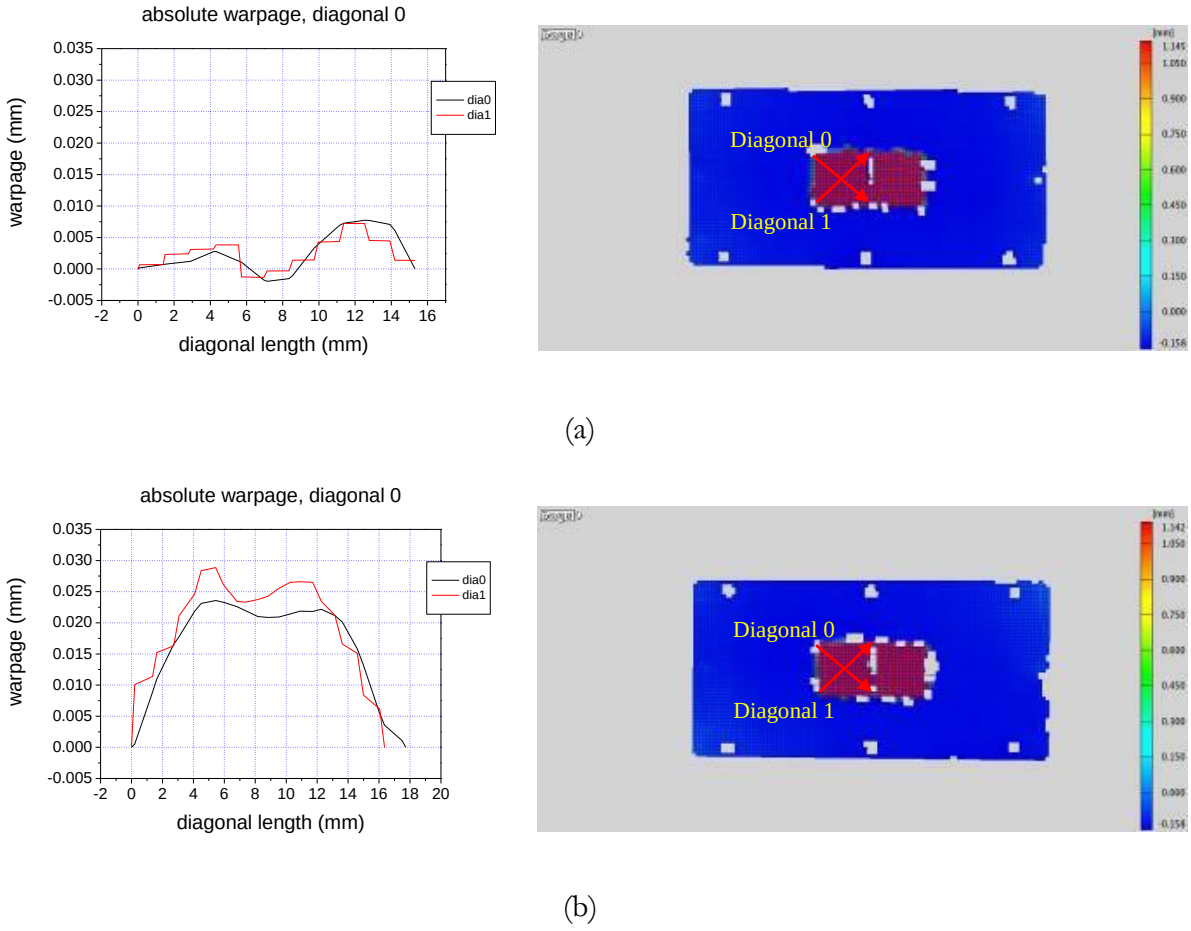
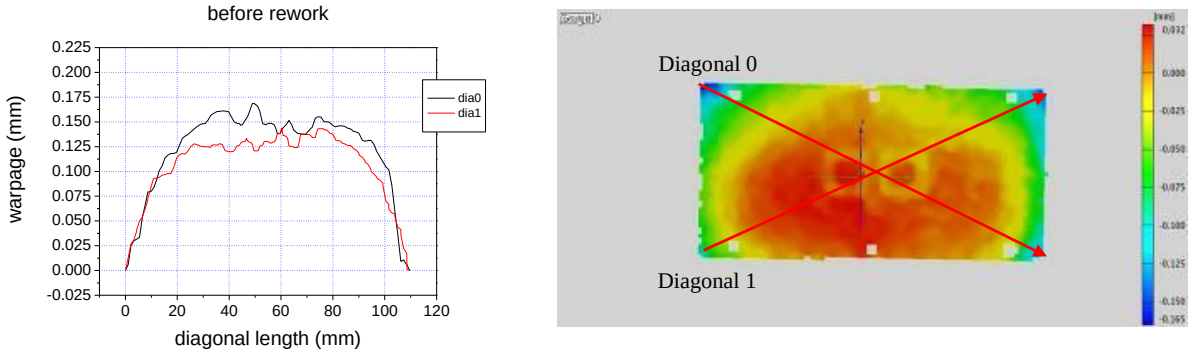
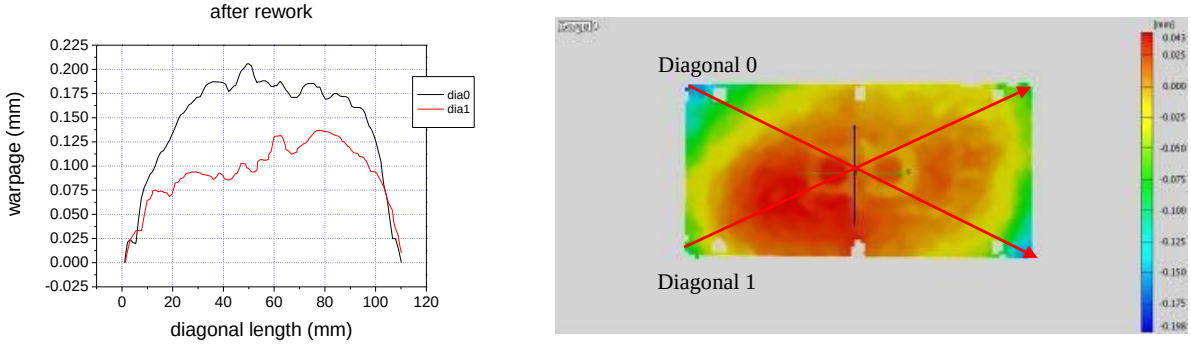


FIGURE 9.15 Result of warpage measurement for component side.

Notes: (a) As-reflowed BGA component; (b) as-reworked BGA component.



(a)



(b)

FIGURE 9.16 Result of warpage measurement for PBA side.

Notes: (a) As-reflowed PBA; (b) as-reworked PBA.

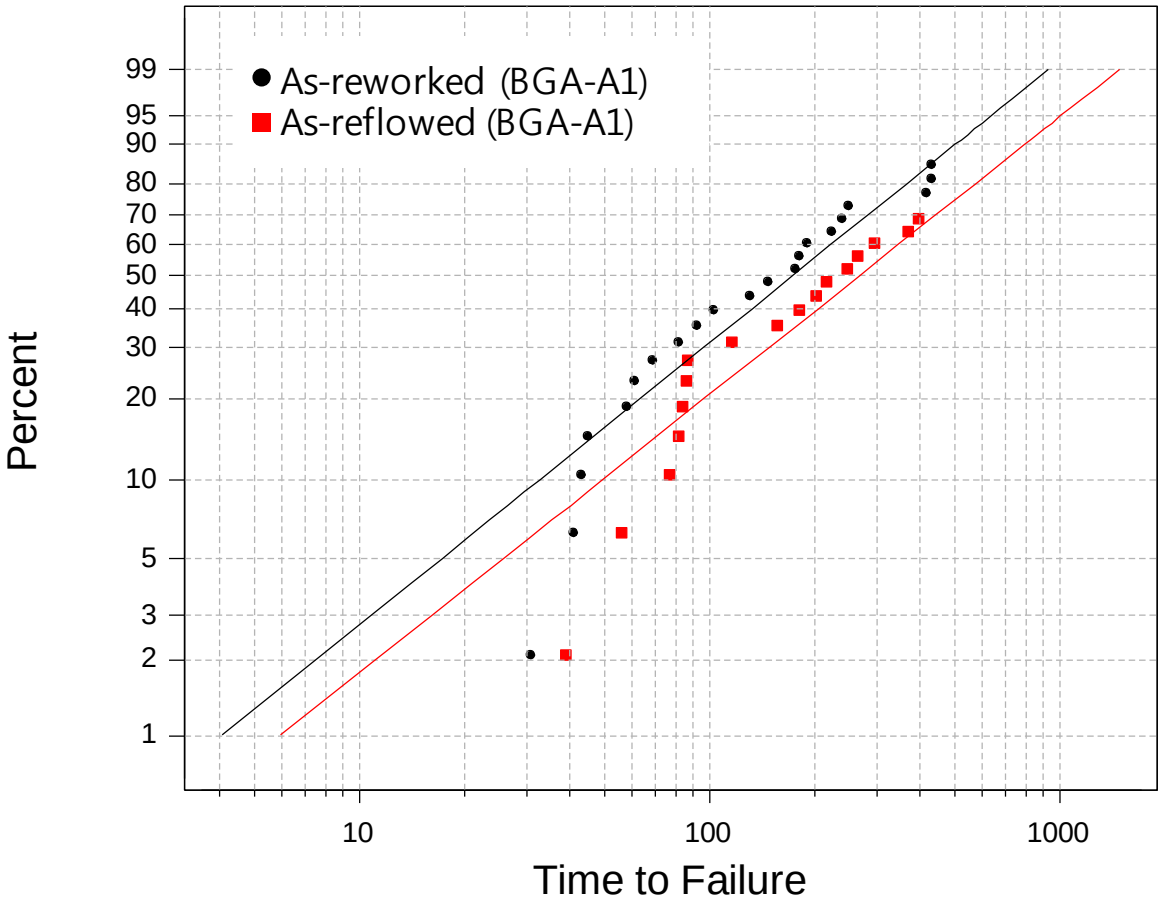


FIGURE 9.17 Weibull distributions for as-reworked samples and as-reflowed samples.

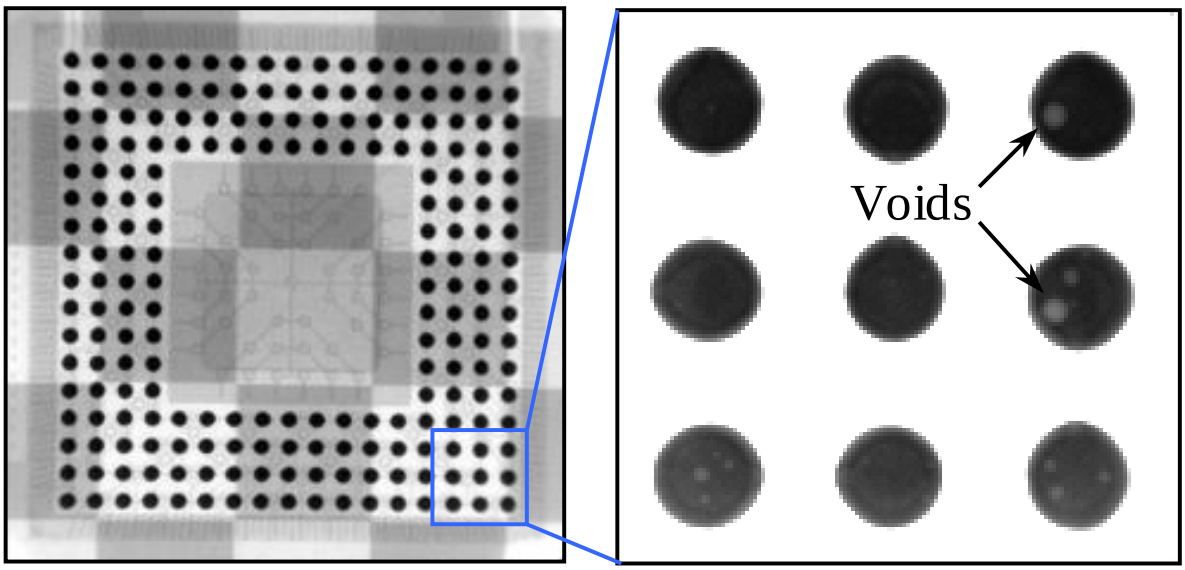


FIGURE 9.18 X-ray image of as-reworked BGA component.

9.3.5 Microstructure analysis

Figure 9.19 shows a cross-sectional SEM image of the interfaces between the Sn-Ag-Cu solder and the ENIG finish on the Cu pad of the substrate after the rework process. For SAC/ENIG solder joints, the consumption of Ni for the formation of Ni-Cu-Sn intermetallics induced vertical voids in the Ni (P) layer [140], and the IMC was formed along the interface, as shown in Figure 9.19(a). EDX analysis indicated that the IMC layer was mainly in the $(Cu, Ni)_6Sn_5$ phase. This is in agreement with general observations of the SAC/ENIG pad finish-solder reaction [141–144]. As shown in Figure 9.19(b), a needle-shaped IMC with irregular morphology was also observed in the bulk solder and at the solder-to-copper interface after rework process. EDX analysis indicated that the needle-shaped IMC was approximately in the Ag_3Sn phase. A similar observation was reported for SAC305/SAC405 by other researchers [142,145]. Studies have reported that this IMC phase are mostly brittle and reduce the mechanical properties of a solder interconnection [146,147].

The average intermetallic compounds (IMCs) thickness was determined by dividing the cross-sectional area of interface intermetallic layer by its base length. For comparison, the interface IMC thickness of the solder bumps, for both the as-reworked BGA and the as-reflowed BGA sample groups, are shown in Figure 9.20. These results show demonstrate that the interface IMC layer thickness of the reworked Sn-Ag-Cu (SAC) bumps is different from those of the as-reflowed SAC bumps. Furthermore, the interface IMC thickness of the as-soldered SAC solder bumps, for both the top (BGA-A1) and the bottom-side (BGA-B1), increased after the rework processing. Additionally, the results show that the rate of growth of the interface IMC thickness, for the rework process, is almost similar for both the top (BGA-A1) and the bottom-side (BGA-B1).

The drop impact failure interfaces, for the packages with SAC/ENIG solder joints after rework, are shown in Figure 9.21. In this experiment, the dominant crack is found at the IMC/Ni (P) interface. For this study, all samples that failed in a drop testing showed the IMC thickness in solders on the PCB pad side to be approximately 10.8 μm and 9.8 μm, respectively, for as-rework samples and as-reflow samples.

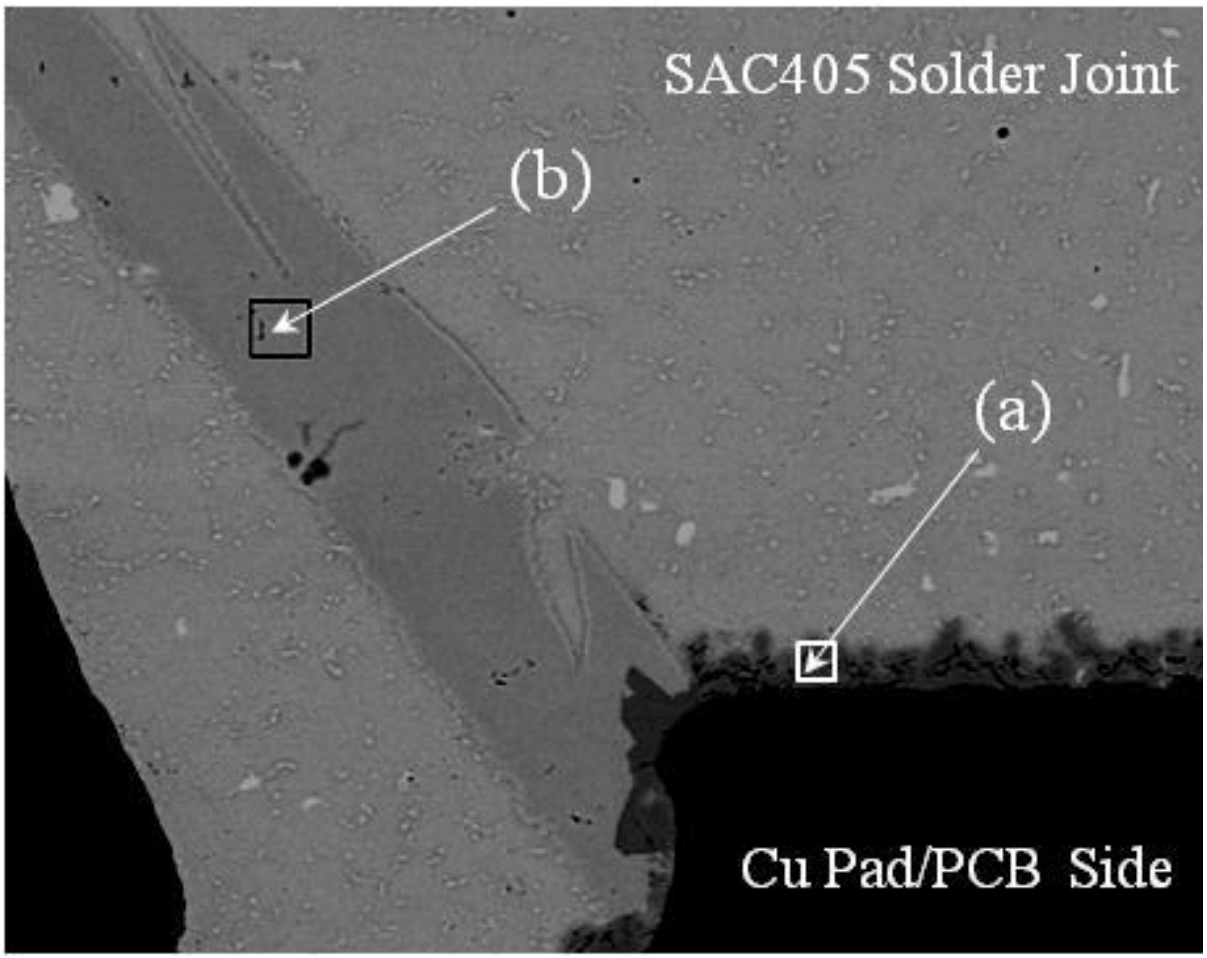
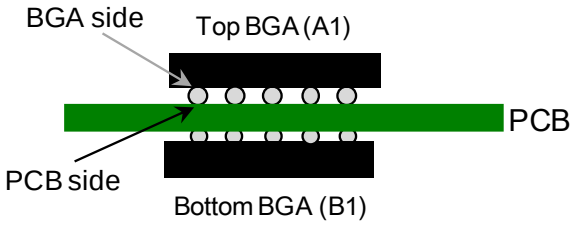
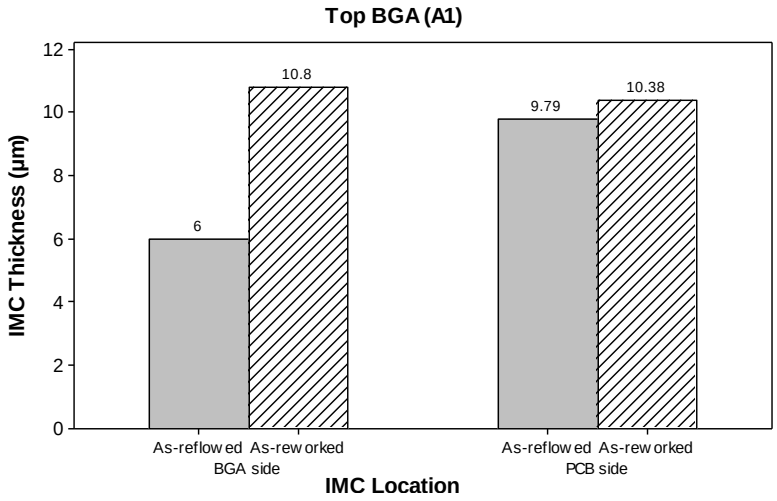
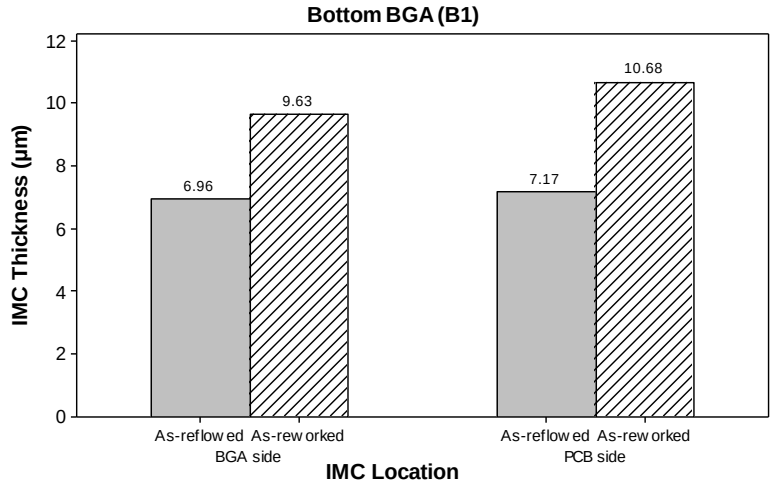


FIGURE 9.19 Interfacial IMCs at the interface between the copper pad with ENIG finish on the board and 95.5wt.%Sn–4.0wt.%Ag–0.5wt.%Cu (SAC405) solder ball attached: (a) A solder joint of a SAC405 BGA on a board pad with ENIG finish showing $(Cu, Ni)_6Sn_5$ IMCs and (b) a solder joint of a SAC405 BGA on a board pad with ENIG finish showing Ag_3Sn IMC layer. Needle-like features in the microstructure of solder joints.





(a)



(b)

FIGURE 9.20 Result of IMC layer thickness measurement.

Notes: (a) Top side; (b) bottom side.

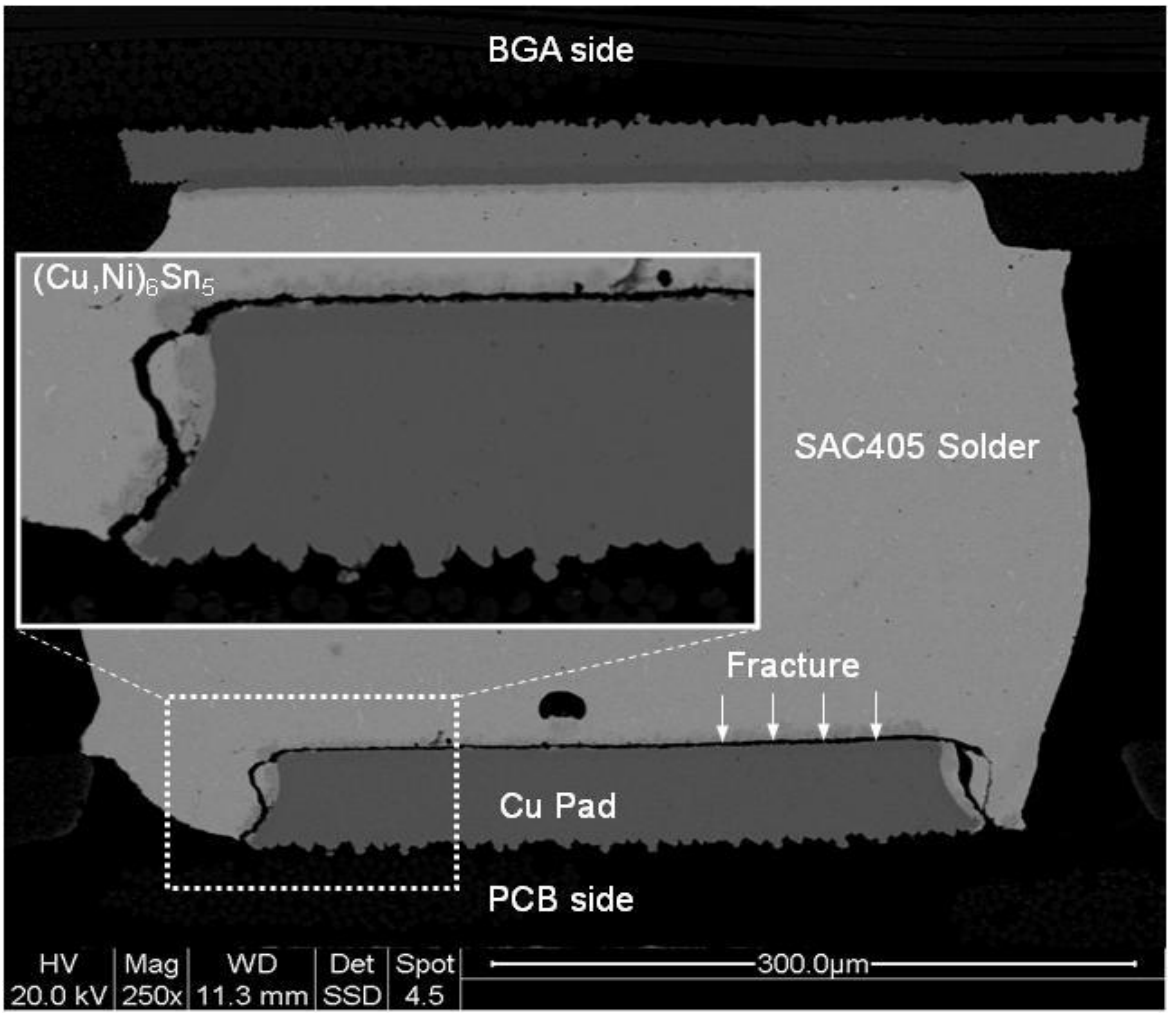


FIGURE 9.21 Crack propagates through the (Cu, $Ni)_6Sn_5$ IMC after the drop test according to the JESD22-B111 standard.

9.3.6 Rework placement gap

The effect of the rework process on board level reliability was studied for adjacent chip components, such as 0201 passive device. The passive components adjacent to the BGA rework area were subjected to a temperature close to 213°C, which raised concerns about partial reflow during the rework process. So, another study investigates the placement gap effects of upon BGA-to-0201 chip components. The test board was assembled using two different placement gap designs.

Shear testing of the passive components was performed for different placement gaps and the as-reflowed component was used as a control sample. Figure 9.22 is a box plot comparing the component shear strength for each placement gap. From the box plot, it can be seen that the shear strength in the as-reflowed sample was approximately 24 percent higher than that of the as-reworked sample. However, the mean shear strength for the adjacent 0201 chip components was 3.8 N and 3.5 N after rework. The placement gaps for the adjacent 0201 chip components are 0.5 mm and 1.0 mm, respectively.

In both cases the placement gaps appeared to be degraded after the rework operation, as a result of the shear force. However, for the adjacent 0201 chip components, no statistically significant difference existed between the 0.5 mm and 1.0 mm gaps (p-value > 0.05). This was done using the two sample t-test and the results are shown in Table 9.3.

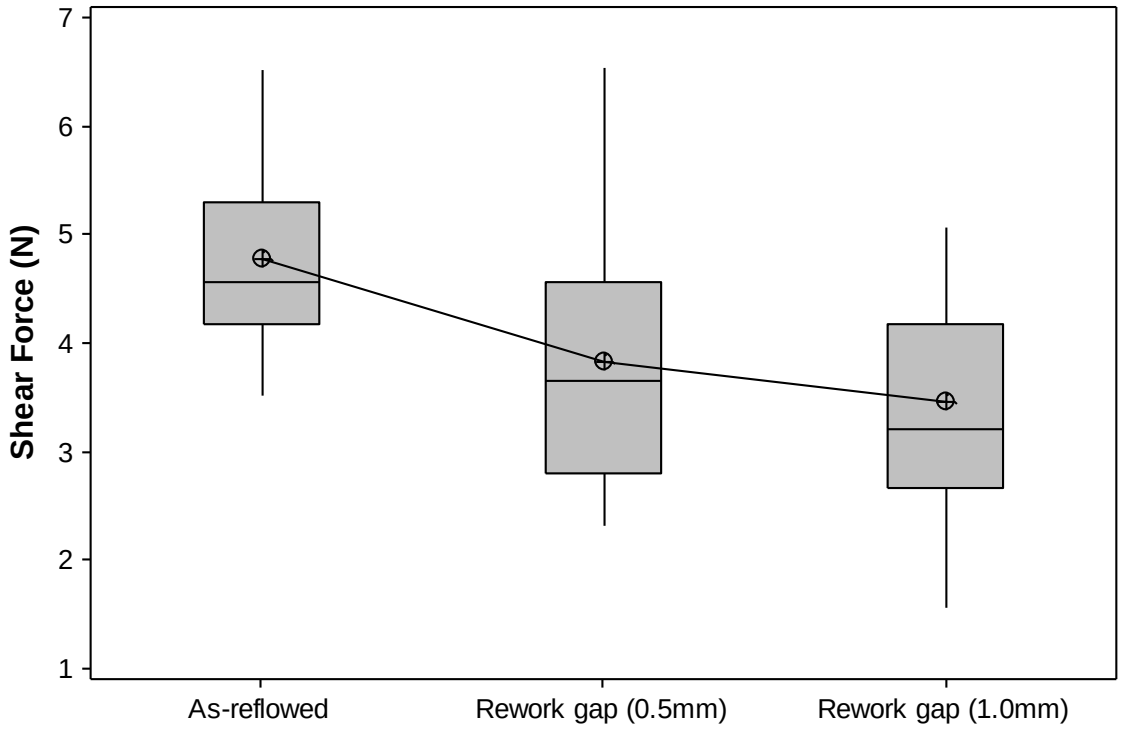


FIGURE 9.22 Average shear forces at the different BGA-to-passive components placement gaps for as-reflowed and as-reworked samples.

TABLE 9.3 Two-sample *t*-test results for component placement gap

Placement gap	*n*	**Mean**	**SD**	**SE mean**	***p*-value**
0.5 mm	20	3.82	1.13	0.25	0.320 ($p > 0.05$)
1.0 mm	20	3.47	1.09	0.24	

Notes: SD - standard deviation; SE mean - standard error mean

9.4 Summary

In this chapter, the following conclusions are drawn from our analysis.

1. Soldering iron and solder wick technique showed significantly better than semi-automatic system with vacuum desoldering machine. Also, off-contact method by soldering iron technique has been shown to be suitable for high-quality site preparation where the application of flux and special care must be taken to avoid damaging the solder mask and prepared pads.

2. The use of retrofit board fixture has proven to be the most efficient method of controlling the temperature of board and bottom side of rework equipment and thermal uniformity during rework process.

3. The reworked BGA components show an approximate 36 percent reduction in the drop reliability and life expectancy over the non-reworked BGA components.

4. The shear force of the adjacent 0201 passive components decreased 24 percent in the reworked sample, due to the heat generated during the rework process, when compared to the initial states of the components.

5. The conditions of the rework process should be optimized for high reliability. If the flux-only method is applied to the rework of BGA components, the under-fill application is crucial in order to ensure heightened reliability.

PART VI: CONCLUSIONS

Chapter 10

Conclusions and outlook

This chapter concludes this dissertation work. First, the research purposes, approach and results of each research area are summarized. Next, recommendations for future work are provided.

10.1 Summary and concluding remarks

As described in Chapter 1, the overall purpose of this research was to develop a robust assembly processes for SiP devices. SiP technology involves packages such as 01005 chip components, so, the passive assembly was optimizing as part of the goal of achieving a robust SiP processing. Several concluding remarks are summarized below.

The first purpose of this research was to optimize assembly processes in order to minimize defects in the assembly of 01005 chip components. For the stencil fabricating techniques, both electroformed and electropolished laser-cut stencils have a comparable print quality that is solder volume delivered to the pads, but the shear strength in the electroformed stencil is somewhat higher than it is in the electropolished laser-cut stencil. If an electroformed stencil is used, the type 4 solder paste, with a smaller sphere size, will give a better overall yield and better paste depositions on the pads. Tombstoning and misalignment defects are minimized using this type of solder paste. A 0.08 mm-thick electroformed stencil with a 90 percent aperture opening was observed to produce good results. Based on the findings and on the observation of zero defects after assembly, this stencil design provided the best self-alignment ability. Characterizing the performance of the vision camera and the vacuum pickup nozzles, for the 01005 chip components Pick-and-Place process, both the DCA camera and the 926 nozzle were observed to produce good results in terms of having fewer missing components and a better overall yield. For the reliability studies, temperature cycle testing of the solder joints showed no failure after 1,500 cycles. However, the shear strength significantly decreased 32 percent after 1,000 cycles.

The second purpose of this research was to study the effect of the stencil manufacturing parameters on the performance of solder paste stencil printing for the assembly of 01005 chip components and 150 μm ultra-fine pitch devices. Stencil aperture wall quality has a direct influence on solder paste release and, as a result, a post-finishing process, such as EP for laser-cut stencil manufacturing, is necessary in order to achieve a smoother surface. In this experiment, the surface roughness of the stencil aperture wall generally showed improvement as the EP time was increased. However, the longest EP time also resulted in a decrease in the stencil thickness and an increase in the aperture size, which may affect solder bridging problems,

such as the spacing between the pads. Thus, it is desirable to select appropriate EP times in order to take the efficiency of the processing into consideration. Furthermore, the phosphoric acid solution concentration is important condition in the EP process used for the surface finishing of laser-cut stencil apertures. In this study, the optimum concentration of phosphoric acid solution for EP process was determined. The smoothness of the stencil aperture and solder paste printing performance are best when the electrolyte solution concentrations are 95 wt.% phosphoric acid and 5 wt.% sulfuric acid. These bath conditions also yielded better performance when compared to the 85 wt.% phosphoric acid solution. During the study, stencil material-related variable, such as grain microstructure, and stencil printing process-related variables, such as solder paste type, print speed, and print force were evaluated with the goal of achieving a high-yield assembly solution for fine-pitch structures. For the stencil metallic materials, the fine-grained SUS301 stainless steel exhibited superior performance, indicating that the grain size of steels has a significant effect on stencil aperture dimensional tolerance. Results of the stencil technology showed that the fine-grained SUS301 metallic stencil indicated a substantially less contaminated assessment in comparison to the alternative stencils. Finer stencil structures over a higher number of print cycles are reproducible and remain printable without cleaning the stencil, which results in a high throughput of PCBs in the printing process. In this study, the fine-grained SUS301 metallic stencil had an acceptable paste volume at a surface area ratio of 0.45. In contrast, the surface area ratio limits are 0.5 and 0.66 for electroformed stencils and laser-cut stencils, respectively. Type 7 solder paste with a smaller sphere size was observed to produce good results in terms of a better solder paste deposition on the pads. Solder paste deposit volumes can also be controlled by optimizing appropriate printer parameters, such as stencil speed and print force. This study demonstrated that fine-grained metallic stencil printing is a strong alternative to electroformed stencil technology for ultra-fine pitch packaging applications.

The third purpose of this research was to propose a solution procedure to minimize /eliminate tombstoning, voiding, and spattering defects in the assembly of 0201 chip components with micro via-in-pads and 95 wt.%Sn–5wt.%Sb solder alloy. The design of micro via-in-pads greatly affects on the occurrence of tombstoning in the assembly of small chip components. In a word, the smaller the via-hole size, the greater the occurrence of tombstoning. The highest tombstoning rate occurred during use of the ultra-small via-in-pad design (10 μm). A

capped via-in pad was effective in reducing the occurrence of tombstoning. The larger solder volume performed much better than the small solder volume in reducing the occurrence of tombstoning in the micro via-in-pad conditions. Tombstoning occurred in about 1.1 percent of components with large via-in-pads (60 μm) at an 80 percent stencil opening. Defects ramped up to about 5.8 percent with small via-in-pads (20 μm) and to 13 percent with ultra-small via-in-pads (10 μm) at 80 percent stencil openings, and they dramatically reduced as the stencil opening size increased. The long-preheat conditions of the reflow profile were effective in reducing the occurrence of tombstoning, but it could not completely remove the defects. In the simulation results, temperature differences between the pad with no via side and the pad with a large via side were within 2°C and consequently resulted in unbalanced wetting. Thus, unbalanced wetting was found to result in a greater tombstoning rate. On the other hand, in the small via-in-pad design, the possibility of voiding becomes lower and for the larger the via-hole size, the greater the occurrence of voiding. A capped via-in-pad and no via-in-pad were effective in reducing the occurrence of voiding. In the via-in-pad design, it was shown that the smaller the via-in-pad designs, the greater the possibility of spattering becomes. The highest spattering rate occurred during use of ultra-small via-in-pad design (d: 10 μm). A capped via-in-pad and no via-in-pad were effective in reducing the occurrence of spattering. The long-preheat conditions of the reflow profile were also effective in reducing the occurrence of spattering, but it could not completely remove the defects in the use of ultra-small via-in-pads and 95 wt.%Sn–5wt.%Sb solder alloy. Therefore, from the above, capped via-in-pads, larger stencil opening size, and the use of a reflow profile with long-preheat conditions are highly desirable, if the micro via-in-pad design and lead-free soldering is considered in the SiP module assembly process.

The fourth and final purpose of this research was to evaluate rework assembly processes in order to minimize defects and the present work is to study the effect of the reworked board assemblies with lead-free BGA packages. For the pad clean-up techniques, soldering iron and solder wick technique showed significantly better than semi-automatic system with vacuum desoldering machine. Also, off-contact method by soldering iron technique has been shown to be suitable for high-quality site preparation where the application of flux and special care must be taken to avoid damaging the solder mask and prepared pads. The use of retrofit board fixture has proven to be the most efficient method of controlling the temperature of board and bottom

side of rework equipment and thermal uniformity during rework process. For the reliability studies, the reworked BGA components show an approximate 36 percent reduction in the drop reliability and life expectancy over the non-reworked BGA components. Furthermore, the shear force of the adjacent 0201 passive components decreased 24 percent in the reworked sample, due to the heat generated during the rework process, when compared to the initial states of the components. Therefore, the conditions of the rework process should be optimized for high reliability. If the flux-only method is applied to the rework of BGA components, the under-fill application is crucial in order to ensure heightened reliability.

In conclusion, the fundamental study represents a significant achievement in miniature components and ultra-fine pitch devices assembly processes. The study may apply to the industrial production of high I/O, fine-pitch devices using lead-free solder alloys. Besides, the experimental and theoretical studies presented in this dissertation provide both design and process guidelines of commercialization of innovative surface mount assembly processes and material to achieve a high stable yield, and robust assembly process in the near future.

10.2 Outlook and future directions

Although this study presented a detailed formal experimentation procedure for the successful assembly of miniature-sized components, such as 01005, numerous other variables that are involved in assembly process could be evaluated. Some key areas for future work are discussed below.

10.2.1 When will the miniaturization trend end?

Perhaps the miniaturization trend will end when chip components are no longer visible. Until such time, however, the miniaturization trend continues with the release of the 008004-size (0201 metric, 0.25 mm × 0.125 mm), which is the world's smallest monolithic ceramic capacitor. The volume of this new chip component is approximately 25 percent of the 01005 (0402 metric, 0.4 mm × 0.2 mm) chip component, as shown in Figure 10.1. Table 10.1 provides a summary of the dimensions of existing chip components, including a component that cannot be seen with the naked eye. These challenges are significant for both the stencil printing process and pick-and-place equipment. Nevertheless, these challenges must be overcome in order for chip components sized 008004 to gain acceptance as an option in high-speed and high-yield assembly.

Lessons learned from the development, manufacturing, and implementation of 01005 will be applied to the present 008004-size chip development project, including design, materials, and optimization of process parameters. Changes in the manufacturing process will include printing parameters, stencils, and equipment, such as nozzles, feeders, and the reflow profile. These changes will be mainly because of the size of the chip component, which reduces the pad size and ultimately requires smaller solder paste deposits.

(a)

(b)

FIGURE 10.1 008004 (0201 metric) chip components [148].

Notes: (a) Comparison of 008004 chip size with larger size chip components and a 0.5mm tip; (b) 008004 chip components (0.25 mm × 0.125 mm × 0.125 mm).
(SOURCE: Murata Manufacturing Co., Ltd.)

TABLE 10.1 Nominal dimensions for each chip capacitor

English	Metric	Length		Width		Height	
		Eng (in)	Met (mm)	Eng (in)	Met (mm)	Eng (in)	Met (mm)
008004	0201	0.008	0.2	0.004	0.1	0.004	0.1
01005	0402	0.016	0.4	0.008	0.2	0.008	0.2

10.2.2 Stencil with hydrophobic surfaces

Now and in the near future, the stencil printing process is the most important technique in the production of electronics that apply solder paste to a PCB quickly and reliably. In particular, the ever decreasing scale of component miniaturization and the increasing density of the components of PCBs will lead to a steadily tightening of the requirements for the stencil printing process.

Water repellant (hydrophobic), super-hydrophobic, and self-cleaning surfaces are highly desirable in the ultra-fine pitch stencil printing process. Because metallic surfaces are inherently hydrophilic (the contact angle for water is less than 90°), hydrophobic surfaces (the contact angle for water greater than 90°), according to the prior art, are created by coating the surface of metallic articles with a suitable inherently hydrophobic material, such as organic coatings. Organic coatings, however, suffer from chemical degradation, low hardness, creep, poor water and abrasion resistance, and poor adhesion. Therefore, rendering metallic surfaces water repellent without requiring the application of soft polymeric hydrophobic coatings of poor durability is also highly desirable [149]. In this research, I have surprisingly discovered that the microstructure of the metallic stencil material significantly affects its wetting behavior. Suitable surface texturing, in the case of fine-grained metallic material, can result in an increase in contact angle, a property that cannot be readily achieved with conventional coarse-grained metallic materials, such as stainless steels. Hence, further studies should be performed to explore the effect of fine-grained metallic material on the performance of ultra-fine pitch stencil printing for a highly stable yield and a robust SMT assembly process. Further tests of parametric stencil fabrication should be conducted.

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[2] Yong-Won Lee (2013), "Process development of ultra-fine pitch assembly for system-in-package devices", Ph.D. dissertation, Department of Adaptive Machine Systems, Osaka University, Osaka, Japan.

Papers included in this dissertation

International paper

[1] Yong-Won Lee, Keun-Soo Kim, and Katsuaki Suganuma (2011), "Process characterization and reliability for the assembly of 01005 chip components", *Soldering & Surface Mount Technology*, Vol. 23 No. 4, pp. 235–243.

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Other publications and presentations

International paper

[1] Yong-Won Lee, Jong-Hoon Kim, Young-Sik Song, and Chang-Sung Seok (2007), "Mechanical strength and microstructural characterization of SUS304 brazed joints with BNi-2 filler metal : Influence of brazing temperature and time", *Solid State Phenomena*, Vol. 124–126, pp. 1673–1676.

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Honors and scientific awards

[1] **Outstanding Achievement Award** (2005), ASE Korea Inc.

[2] **Best Poster Presentation Award** (2005), '05 Fall Conference of the Materials Research Society of Korea, Seoul, Korea.

[3] **NXP Semiconductors Best Paper Award** (2008), IEEE International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP), Shanghai, China.

[4] **Outstanding Achievement Award** (2010), Samsung Electronics Co., Ltd.

[5] **Outstanding Achievement Award** (2011), Samsung Electronics Co., Ltd.

[6] **Highly Commended Paper Award** (2012), Soldering & Surface Mount Technology, Emerald Literati Network.

[7] **IR52 Jang Young Shil Award** (2012), Korean Ministry of Education, Science and Technology.

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