Research on area-efficient, low power reference circuit

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Abstract

The main part of this research was dedicated to propose a new area-efficient and low power bandgap reference (BGR) circuit. Two new BGR circuit architectures utilizing current switched and current memory techniques are presented. Both circuits are designed using manufacturer-provided device models and operations are verified by using SPICE (Simulation Program with Integrated Circuit Emphasis) simulations. Moreover, to study the design area occupation, layout designing is also carried out.

The final part of the research was carried out to propose a novel ultra-low-power temperature independent current reference, which is designed by using subthreshold CMOS devices. In this work also, SPICE simulations were performed to verify the circuit operations, and the results are presented. Therefore, this dissertation consists of six chapters.

In Chapter 1, a brief introduction of this research is given, including research background, objectives and dissertation structure.

In Chapter 2, the conventional BGRs are reviewed and the major problems of available CMOS BGRs are discussed.

In Chapter 3, an area efficient CMOS bandgap reference with switched-current and current-memory technique is presented.

The proposed circuit uses only one parasitic bipolar transistor to generate reference voltage so that significant area reduction is achieved. The circuit produces an output of about 650 mV, and simulated results show that the temperature coefficient of output is less than 10.7 ppm/°Cin the temperature range from 0 °C to 100 °C. The average current consumption is about 49.5 μA in the above temperature range. Furthermore, output can be set to almost any value. The circuit was designed and simulated in 0.25 μm CMOS technology. The layout occupies less than 0.011 mm^2 (100 μm × 110 μm).

In Chapter 4, an area efficient, low power, fractional CMOS bandgap reference utilizing switched-current and current-memory techniques is presented. The proposed circuit uses only one parasitic bipolar transistor and built-in current source to generate reference voltage. Therefore significant area and power reduction is achieved, and bipolar transistor device mismatch is eliminated. In addition, output reference voltage can be set to almost any value. The proposed circuit is designed and simulated in 0.18 μm CMOS process, and simulation results are presented. With a 1.6 V supply, the reference produces an output of about 628.5 mV, and simulated results show that the temperature coefficient of output is less than 13.5 ppm/°C in the temperature range from 0 °C to 100 °C. The average current consumption is about 8.5 μA in the above temperature range. The core circuit, including current source, operational amplifier, current mirrors and switched capacitor filters, occupies less than 0.0064 mm^2 (80 μm × 80 μm).

In Chapter 5, a novel temperature-compensated, ultra-low-power current reference based on two β-multipliers whose resistors are replaced by nMOS devices operated in the deep triode region is

presented. The circuit, designed by a 0.25 μm CMOS process, produces an output reference current of 13.7 nA at room temperature. Simulated results show that the temperature coefficient of the output is less than 100 ppm/°C in the range from −20 °C to 80 °C and the average power dissipation is 0.9 W.

In Chapter 6, conclusions of this study and recommendations for further research are given.

Acknowledgement

It is a pleasure to thank the many people who made this thesis possible.

I would like to express my deep and sincere gratitude to my supervisor, Professor Emeritus Kenji Taniguchi (currently at Nara national college of technology), for his warm encouragement and thoughtful guidance. His wide knowledge and his great efforts to explain things clearly and simply have been of great value for me.

I also thank the members of my thesis committee: Professor Tetsuya Yagi, Associate Professor Toshimasa Matsuoka, and Associate Professor Masanori Hahsimoto, whose helpful suggestions increased readability and reduced ambiguity.

I would like to thank Professor Toshimichi Ito, Professor Yusuke Mori, Professor Mitsuhiro Katayama, Professor Masanori Ozaki, Professor Toshiaki Suhara, Professor Masahiko Kondow, Professor Yutaka Ohmori, and Professor Seizo Morita for their detailed and constructive comments, and for their important support throughout this work.

Also, special thanks go to Associate Professor Yoshinari Kamakura, for his professional advice and guidance in assisting and supporting this research.

This thesis would not have been possible without the help and support of my second supervisor, Associate Professor Toru Ido (currently at Wolfson Microelectronics Corporation), not to mention his advice and unsurpassed knowledge of analog circuit designing.

I especially want to thank Dr. Shunsuke Okura (currently at Renesas Electronics Corporation), for his guidance during my research and study at Osaka University. His perpetual energy and enthusiasm in research had motivated me. In addition, he was always accessible and willing to help me with any thing I needed.

Special thanks are due to my parents Edmon S. Bogoda and Sheela Bogoda, and all dear friends, who enriched my life with their time, love, and friendship, who helped me to accept the sad things that happen in life, and who never stopped reminding me of the wonderful world outside of my research.

I dedicate this thesis to my father and my late mother, who will always be in my heart.

Contents

Chapter 1

Introduction

1.1 Introduction

Designing high-accuracy analog circuit always has been an important research field, and significant developments are expected in the future. This is because, the analog circuits are the interfaces which connect the real world and digital circuits. They are used to amplify, process and filter the analog signals and convert them to digital signals or vice versa. Decades ago it was more common to compose analog LSI and digital LSI separately. But, for the purposes of the mass production and cost reduction of packaging and testing, analog-digital mixed signal system on chip (SoC) applications have emerged recently and become main stream in LSI industry.

However, CMOS technology keeps developing in purpose for high speed and the high density integration of the digital circuit, and hence, various restrictions have been caused in an analog circuit. Moreover, the transmission of the digital signals that have discrete values inflict noise on analog signals that has continuous values. Therefore, it is important and necessary to invent new analog circuit configurations and architectures to solve these problems.

On the other hand, in the latter half of the 1980's, the digital circuitry extended explosively as the CMOS technology developed. As a result of this, a lot of circuit designers move from analog to digital. Thus, the advancement of the analog circuit designing is slower compared to that of digital circuits. On the other hand, high performance analog circuit is necessary to draw out the performance of the digital circuits, and therefore the analog circuit has become the bottle neck of large scale integrated (LSI) circuits.

Many analog circuits require voltage references, such as analog-to-digital (A/D), digital-to-analog (D/A) converters, and operational amplifiers. Thus, voltage reference is a pivotal building block in mixed-signal and radio-frequency systems. For example, most of the mixed-signal systems, as shown in Fig. 1.1, have more than one voltage reference due to different voltage reference requirements and also to avoid crosstalk through a single reference circuit. Most voltage references are usually designed based on a bandgap reference, which was firstly proposed by Widlar [1], and was further developed by Kuijk [2] and Brokaw [3].

Also current reference is a basic building block in analog circuits as a bias source for oscillators, amplifiers, phase-locked loops and etc. All mentioned applications make extensive use of current references and their accuracy is strongly related to the temperature and process stability of these references. Several current references have been proposed previously [4, 5, 6].

The main purpose of this research is to propose area-efficient, low power consumption, voltage and current reference circuits while solving various problems of the analog circuit designing

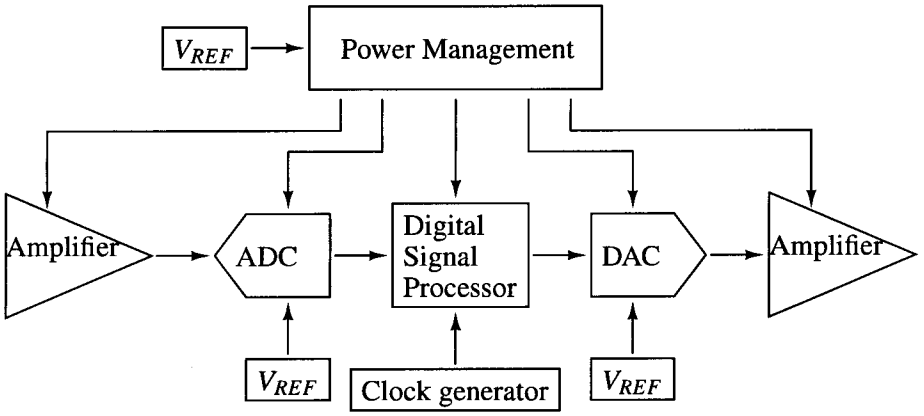

Figure 1.1: Mixed signal system

according to the present demand.

1.2 Research objectives

The main part of this research was dedicated to propose a new area-efficient and low power bandgap reference circuit. Two new circuit architectures utilizing current switched and current memory techniques are presented. Both circuits are designed using manufacturer-provided device models and operations are verified by using SPICE (Simulation Program with Integrated Circuit Emphasis) simulations. Moreover, to study the design area occupation, layout designing are also carried out. Since both the bandgap references were designed to have insensitive outputs for supply voltage and temperature and smaller design areas, the results are compared with conventional bandgap references.

The final part of the research was carried out to propose a novel ultra low-power temperature independent current reference, which is designed by using subthreshold CMOS devices. In this work also, SPICE simulations were performed to verify the circuit operations, and the results are presented.

1.3 Dissertation framework

The core of this dissertation consists of a selection of three publications, two of which are related to the area-efficient CMOS bandgap reference, and one of which describes the ultra low-power current reference based on subthreshold CMOS devices. Therefore, this dissertation consists of six chapters.

Chapter 1 gives a brief introduction of this research, including research background, objectives and dissertation structure.

Chapter 2 reviews the conventional voltage references: Forward-biased diode reference, Zener references, and Subthreshold references. Furthermore discusses the major problems of available CMOS bandgap references.

Chapter 3 describes the area-efficient bandgap reference with new circuit structure and presents

the SPICE simulations and layout results.The circuit produces an output of about 650 mV, and simulated results show that the temperature coefficient of output is less than 10.7 ppm/°C in the temperature range from 0 °C to 100 °C. The average current consumption is about 49.5 μA in the above temperature range. Furthermore, output can be set to almost any value. The layout occupies less than 0.011 mm^2 (100 μm × 110 μm).

Chapter 4 is dedicated to area-efficient and low-power bandgap reference. The major problems of the bandgap reference, which is presented in Chapter 3, are also discussed. With a 1.6 V supply, the reference produces an output of about 628.5 mV, and simulated results show that the temperature coefficient of output is less than 13.5 ppm/°C in the temperature range from 0 °C to 100 °C. The average current consumption is about 8.5 μA in the above temperature range. The core circuit, including current source, opamp, current mirrors and switched capacitor filters, occupies less than 0.0064 mm^2 (80 μm ×80 μm).

Chapter 5 presents the novel temperature-compensated, ultra-low-power current reference based on two β-multipliers whose resistors are replaced by nMOS devices operated in the deep triode region. The circuit produces an output reference current of 13.7 nA at room temperature. Simulated results show that the temperature coefficient of the output is less than 100 ppm/°C in the range from −20 °C to 80 °C and the average power dissipation is 0.9 μW.

Chapter 6 gives conclusions of this study and recommendations for further research.

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Chapter 2

Voltage Reference

2.1 Introduction

One of the most important building blocks in analog circuits is a precise reference, be it voltage or current. This reference should have good stability under various operation conditions such as temperature variations and power supply voltage variations. Some of the examples of applications where reference are required are A/D converters, D/A converters, DC-DC converters, AC-DC converters, operational amplifiers, and linear regulators. Those applications are widely used in almost all modern electronics products such as digital cameras, cellular phones, digital televisions, portable music players, and laptops. Thus the reference generator circuits play an important role in modern analog circuit designing. The requirements for ideal reference are listed as follows.

- Temperature independent output.
- Supply voltage independent output.
- Flexibility in output.

Temperature-drift performance is one of the most important issues to be taken into consideration. Temperature coefficient (TC), which is expressed in parts-per-million per degree (ppm/°C), is the typical metric used for variations across the temperature, and is defined as follows [1].

$$TC = \frac{1}{\text{Reference}} \cdot \frac{\partial(\text{Reference})}{\partial(\text{Temperature})} \tag{2.1}$$

There are a few kinds of process technologies that are used to fabricate the integrated circuits. The standard bipolar process, complementary metal oxide semiconductor (CMOS) process, and BiCMOS technology are the most common. Voltage references can be divided into three main groups.

- Forward-biased diode references
- Zener References
- Subthreshold references

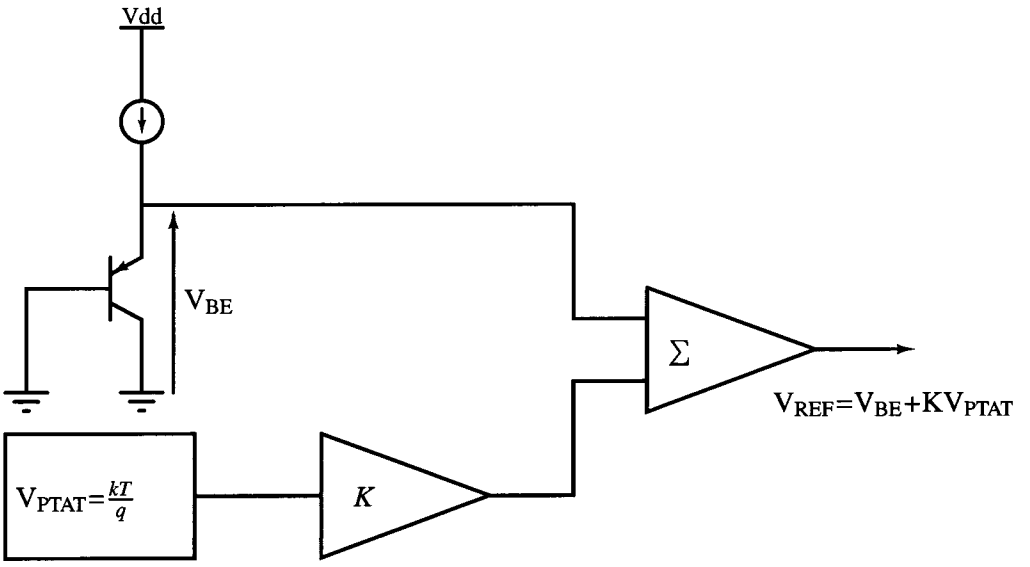

Figure 2.1: Principle of the bandgap reference

2.2 Forward-biased diode reference

The forward-biased diode reference [2, 3], which is also referred to as bandgap reference, is the most common voltage reference. They are capable of generating references having a temperature coefficient (TC) in order of 10 ppm/°C over the temperature range from 0 °C to 100 °C. The principle and the temperature behavior of the bandgap reference are illustrated in Fig. 2.1 and 2.2, respectively. The bandgap reference sums the proportional-to-absolute-temperature (PTAT) voltage and a base-emitter voltage (V_{BE}) of a bipolar transistor or, equivalently, a forward-biased diode with proper weighting to obtain zero TC output. This can be done because V_{BE} shows a negative temperature coefficient (discussed in next section) as shown in Fig. 2.2. Therefore, the output of the conventional bandgap reference can be written as

$$V_{REF} = V_{BE} + KV_{PTAT} \tag{2.2}$$

where, K is a constant. Constant K is chosen to obtain a V_{REF} value that has a minimum variation over the temperature of interest.

2.2.1 Temperature behavior of V_{BE}

Figure 2.3 shows a pnp bipolar transistor biased by a current source I_C. The relationship between bias current I_C and V_{BE} of the bipolar transistor can be expressed as follows.

$$I_C = I_S \exp \frac{V_{BE}}{V_T} \tag{2.3}$$

where,

$$V_T = \frac{kT}{q}$$

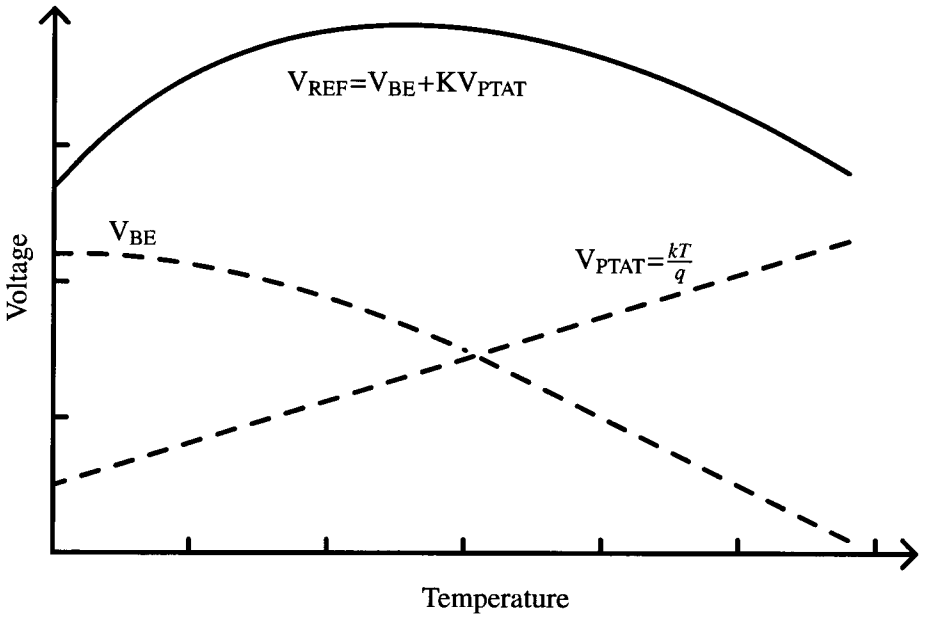

Figure 2.2: Basic temperature behavior of the bandgap reference

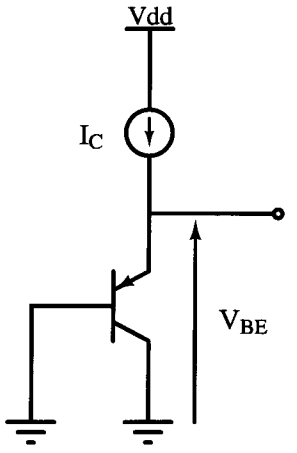

Figure 2.3: V_{BE} of bipolar transistor

where I_S is the saturation current, k is the Boltzmann's constant, T is the absolute temperature, and q is the elementary charge. However, I_S is proportional to μkTn_i^2, where μ represents the mobility of minority carriers and n_i is the intrinsic carrier concentration of silicon. The temperature dependencies of μ and n_i are given by

$$\begin{aligned} \mu &\propto \mu_0 T^m \\ n_i^2 &\propto T^3 \exp\frac{-E_g}{kT} \end{aligned}$$

where constant $m \approx -3/2$, and E_g is the bandgap energy of silicon. Therefore, I_S can be expressed as follows,

$$I_S = bT^{4+m} \exp \frac{-E_g}{kT} \tag{2.4}$$

where b is a proportionality factor. Assuming that I_C is a constant, the temperature dependences of V_{BE} can be written as

$$\frac{\partial V_{BE}}{\partial T} = \ln\left(\frac{I_C}{I_S}\right)\frac{\partial V_T}{\partial T} - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T} \tag{2.5}$$

From eq. (2.4), we can write

$$\frac{\partial I_S}{\partial T} = b(4+m)T^{3+m} \exp \frac{-E_g}{kT} + bT^{4+m}\left(exp\frac{-E_g}{kT}\right)\left(\frac{E_g}{kT^2}\right) \tag{2.6}$$

From eqs. (2.4) and (2.5), we can write

$$\frac{V_T}{I_S}\frac{\partial I_S}{\partial T} = (4+m)\frac{V_T}{T} + \frac{E_g}{kT^2}V_T \tag{2.7}$$

Thus, by using eqs. (2.5) and (2.7), the temperature dependence of V_{BE} can be derived as

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T}\ln\frac{I_C}{I_S} - (4+m)\frac{V_T}{T} - \frac{E_g}{kT^2}V_T \tag{2.8}$$

$$= \frac{V_{BE} - (4+m)V_T - E_g/q}{T} \tag{2.9}$$

By using eq.(2.9), it is possible to calculate the TC of V_{BE} at a given temperature. Assuming that the $V_{BE}\approx$750 mV at room temperature T=300K, and thus, $\partial V_{BE}/\partial T \approx$-1.5 mV/K. Therefore, it is clear that the V_{BE} of bipolar transistors exhibits a negative TC.

2.2.2 PTAT voltage

Assume two bipolar transistors Q_1 and Q_2, biased by identical current sources, as shown in Fig. 2.4. Q_1 is a unit transistor and Q_2 consists of n unit transistors. Thus the V_{BE}s of Q_1 and Q_2, V_{BE1} and V_{BE2}, can be expressed as

$$V_{BE1} = V_T \ln\frac{I_0}{I_s} \tag{2.10}$$

$$V_{BE2} = V_T \ln\frac{I_0}{nI_s} \tag{2.11}$$

respectively. As shown in previous section, both V_{BE1} and V_{BE2} are complementary to absolute temperature (CTAT). On the other hand, the difference between V_{BE1} and V_{BE2}, which is given by

$$\Delta V_{BE} = V_{BE1} - V_{BE2}$$

$$= \frac{kT}{q}\left(\ln\frac{I_0}{I_S} - \ln\frac{I_0}{nI_S}\right) = \frac{kT}{q}\ln n \tag{2.12}$$

is proportional to absolute temperature (PTAT).

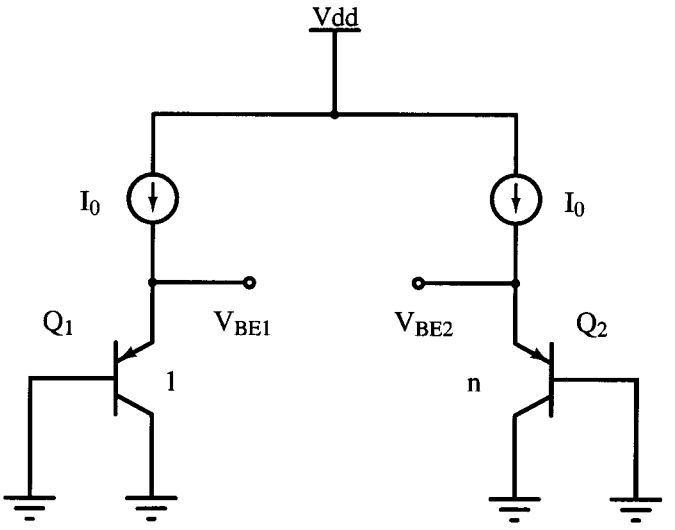

Figure 2.4: Base-emitter voltages at different current densities

2.2.3 Bandgap reference

Conventional bandgap references use above-described CTAT and PTAT voltages to generate temperature independent reference. In 1971, Robert Widlar introduced the first bandgap reference [4]. The simplified schematic of Widlar bandgap reference is shown in Fig. 2.5.

In Fig. 2.5 the bipolar transistor Q_1 is operated at higher current density compared to Q_2. Because Q_1 and Q_2 shares the same base voltage, we can write

$$V_{BE1} = V_{BE2} + I_2 R_3 \tag{2.13}$$

besides,

$$V_{BE1} - V_{BE2} = \Delta V_{BE} = V_T \ln \frac{I_1}{I_2} \tag{2.14}$$

thus, from (2.13) and (2.14)

$$I_2 = \frac{\Delta V_{BE}}{R_3} = \frac{V_T}{R_3} \ln \frac{I_1}{I_2} \tag{2.15}$$

The output of the Wildar bandgap, therefore, can be expressed as

$$\begin{aligned} V_{OUT} &= V_{BE3} + I_2 R_2 \\ &= V_{BE3} + \frac{R_2}{R_3} \cdot V_T \cdot \ln \frac{I_1}{I_2} \end{aligned} \tag{2.16}$$

Even though the Widlar bandgap reference offered the first absolute voltage source with zero (very small) temperature drift, it still has a few drawbacks. First the output voltage is fixed to silicon bandgap voltage and can not be changed. Next, the performance of the circuit depends heavily on the current density in Q_3 which will change if the circuit is loaded.

To overcome those problems, another version of bandgap references [5, 6] have been presented. A simplified version of a common bandgap reference is shown in Fig. 2.6. First, for simplicity, assume that V_{OS}= 0 V. Operational amplifier senses the V_{BE} of Q_1, V_{BE1}, and the voltage across

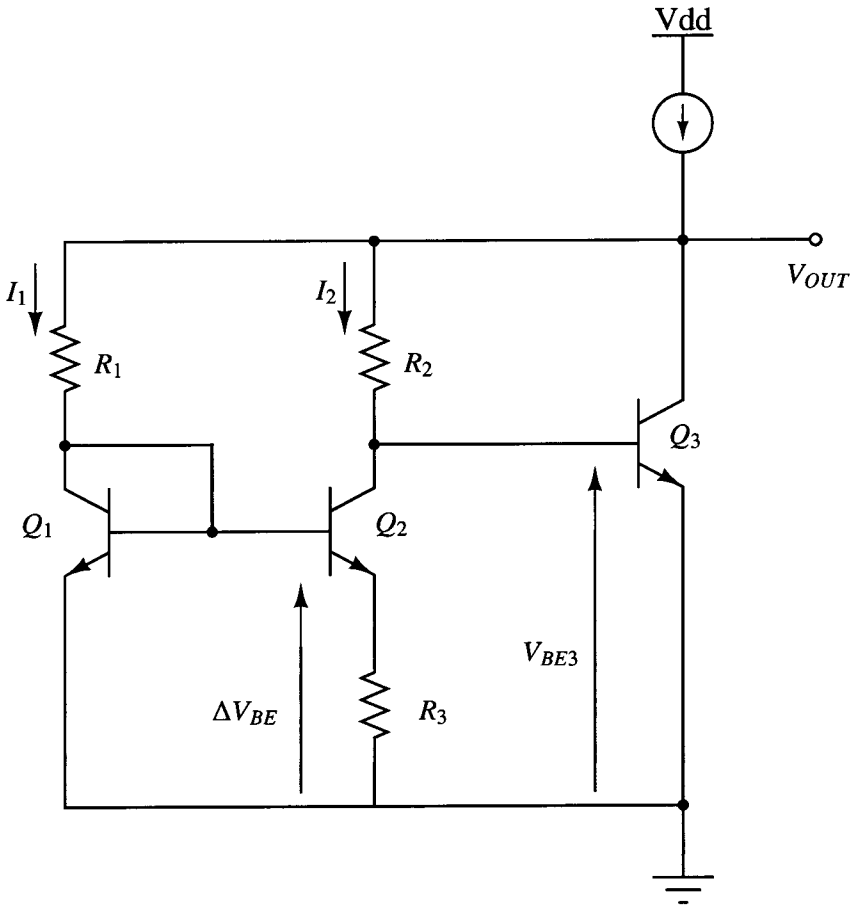

Figure 2.5: A simplified version of Widlar bandgap reference

the Q_2 and R_1, then regulates them to be equal. Assuming that the current through each terminal is I_0, the relationship between the voltages in nodes a and b can be written as follows

$$V_{BE1} = V_{BE2} + I_0 R_1 \tag{2.17}$$

Therefore, by using above relation , the expression for output voltage V_{REF} can be derived as

$$V_{REF} = V_{BE2} + \frac{R_2}{R_1}\Delta V_{BE} \tag{2.18}$$

As discussed in previous section, V_{BE1} shows negative temperature dependence while ΔV_{BE} shows positive temperature dependence. Therefore, setting the resistor ratio R_2/R_1 for a proper value, temperature independent V_{REF} can be achieved. Even though the bandgap references are widely used in modern analog applications because of their accuracy, they are having many problems that required further research.

- Flexibility in output
  Another problem of the traditional bandgap references is no flexibility in the output voltage. This is because, as the name suggests, the output of the bandgap reference is equal to the

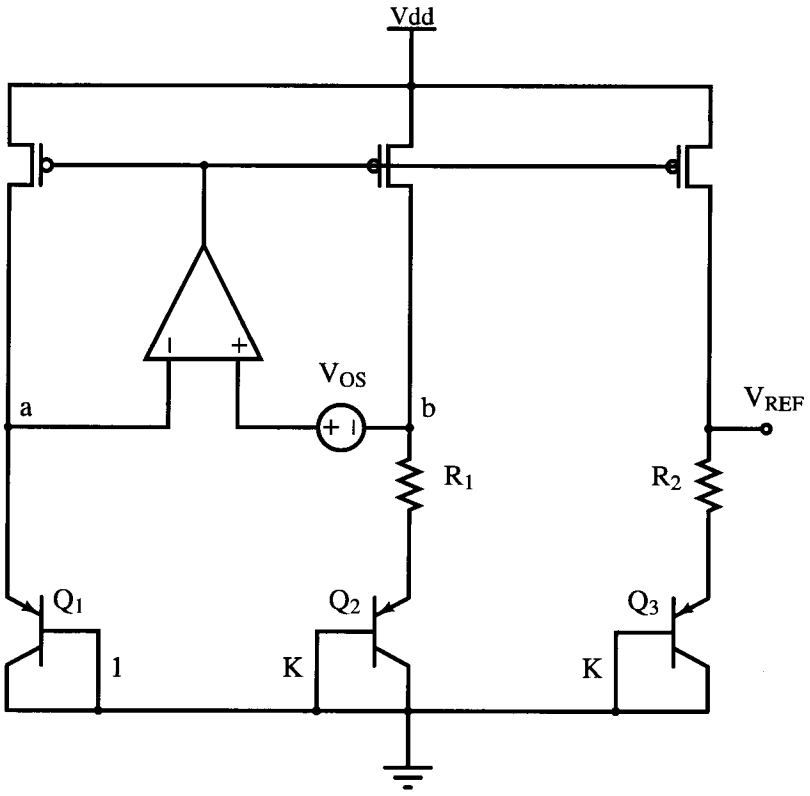

Figure 2.6: A simplified version of common bandgap reference

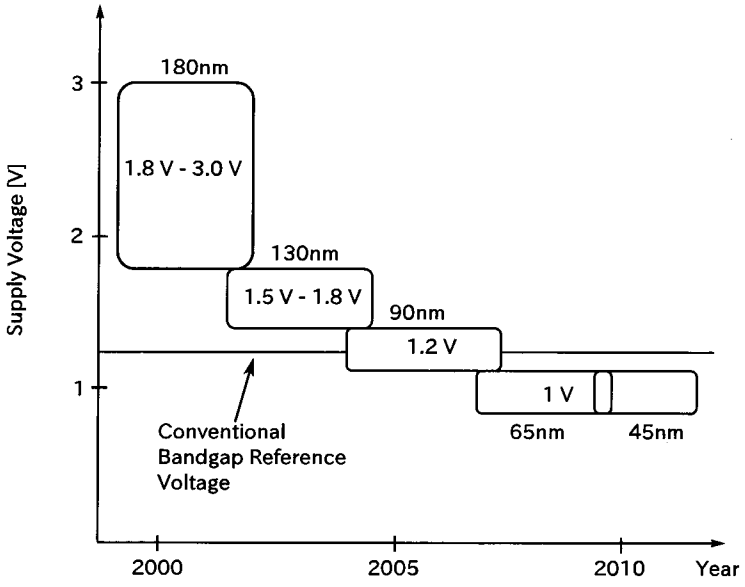

Figure 2.7: Relation between process and power supply

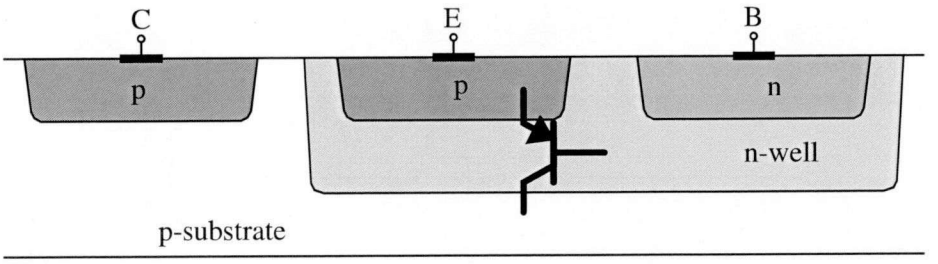

Figure 2.8: Parasitic bipolar transistors in CMOS process

bandgap voltage of silicon, which is approximately 1.2 V at room temperature. Since, as shown in Fig. 2.7, the supply voltage of the modern analog designs falls to near, or rather below the bandgap voltage, the traditional bandgap references are unable to function. To overcome this problem, several techniques have been demonstrated [7, 8, 9]. However, such bandgap references require BiCMOS technologies, CMOS technologies with low-threshold devices, and resistor network with large values that result in extra cost and larger design area.

- Opamp offset effects
  Every operation amplifier comes with an input offset voltage (see appendix A). This offset error introduces a significant error in output of conventional bandgap references. The output voltage of Fig. 2.6, which is influenced with offset of the operational amplifier, can be given by

$$V_{REF} = V_{BE2} + \frac{R_2}{R_1}\Delta V_{BE} - \frac{R_2}{R_1}V_{OS} \tag{2.19}$$

  Therefore, the offset is multiplied by the factor $R2/R1$, which is always grater than 1, and it appears in the output. In typical bandgap references, operational amplifier offset voltage is multiplied by a factor larger than 10 and appears in the reference voltage [10]. Additionally, offset voltage itself has a temperature dependence, rising the temperature coefficient of the reference voltage. For this reason, low-offset operational amplifiers or offset cancellation techniques should be used to achieve a precision reference voltage in conventional bandgap references. But those techniques come with complex circuitry [11], and therefore difficult to design.

- Design area problems
  Since the SoC applications become increasingly popular, CMOS process has shown several advantages compared to BiCMOS process. The main drawbacks of the BiCMOS process are the expensiveness, long period of process development, and the low-performance of BiCMOS digital circuits compared to that of CMOS digital circuits. Thus, the several techniques have been demonstrated on implementation of parasitic bipolar transistors in CMOS process [12, 13, 14]. In standard n-well CMOS process, a parasitic PNP transistor can be fabricated as shown in Fig. 2.8. However, compared with other devices, parasitic transistors need a larger design area. Although, the MOSFETs are scaled down to the nano-scale regime, parasitic transistors are left unchanged. As CMOS technology continues to shrink down, the design area becomes more and more expensive and, thus, is an important aspect of any design. Therefore, the design of common conventional bandgap reference, which uses the area ratio of the parasitic bipolar transistors to generate the reference voltage, becomes a critical problem.

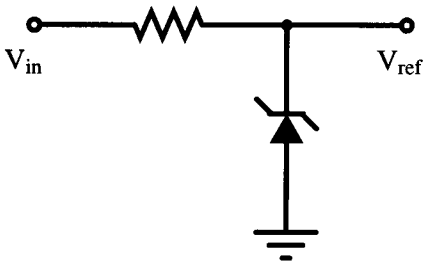

Figure 2.9: Zener voltage reference

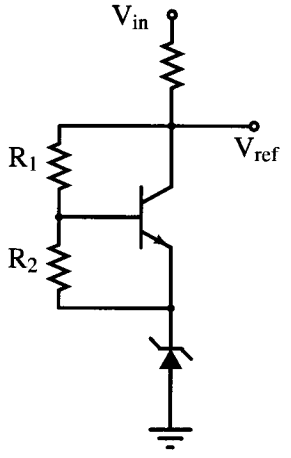

Figure 2.10: Modified zener voltage reference

2.3 Zener references

The zener reference is another widely used voltage reference circuit, which uses zener diode and a resister to generate the reference voltage, as shown in Fig. 2.9. When the zener diode operates in reverse-breakdown region, significant change in bias-current induces nearly negligible change in diode-voltage. Zener reference uses this mechanism to generate reference voltage. The main disadvantage in reference shown in Fig. 2.9 is that the breakdown voltage has a positive temperature drift, approximately between +1.5 and 5 mV/°C. And another problem is, common zener diodes have a high breakdown voltage between 5.5 and 8.5 V, and therefore these voltage references are not suitable to use with low-voltage applications. However, the temperature dependence of zener reference can be effectively reduced by using the structure shown in Fig. 2.10. This technique cascades one or several elements with negative TCs, in Fig. 2.10 forward-biased diode, which shows TC of -2.2 mV/°C per diode. But this method increases the required supply voltage. Thus, the zener reference is only suitable for high-voltage applications with supply voltages greater than 6 to 9 V.

Table 2.1: Summary of comparison of voltage references

Reference	Area	Power Consumption	Low supply Voltage	TC
Bandgap	△	△	△	○
Zener	×	×	×	×
Subthreshold	△	○	○	△

2.4 Subthreshold references

The increasing demand for portable electronic devices, micro-sensors, and bio medical sensors makes the ultra-low power circuits increasingly important. Most references based on bipolar transistors and zener diodes consume relatively large power, and therefore, cannot be used in ultra-low power applications. Even though the reference [7], which is based on vertical substrate bipolar transistors, consumes a few micro watts, it needs a resistors with high resistance of several hundred mega-ohms. Such a high value resistors required large design area to be implemented, causing cost problems. Therefore, to solve those problems, references based on subthreshold CMOS devices [15, 16] have been demonstrated and attracting more attention recently. They consists of the MOS devices that operate in the subthreshold (weak inversion) region, and only consume a few hundred nano-watts to several micro-watts. Additionally, some subthreshold voltage references use only the MOS devices [16], and therefore they are ideal to use with ultra-low power CMOS-only designs.

However, there are a few drawbacks in subthreshold voltage references. First, the leakage current increases as the temperature, and overwhelms the drain current at moderately high temperature. As a result of this, the operating temperature range for subthreshold reference generators are often limited. Second, the output reference voltage is highly dependent on the threshold voltage of pMOS/nMOS devices [16], which vary from MOS-to-MOS, chip-to-chip and wafer-to-wafer. Thus, the output is highly sensitive to process variations.

2.5 Comparison

Our study in this chapter has introduced three voltage reference topologies : forward-biased reference, zener reference, and subthreshold reference. It is instructive to compare the performance aspects of these topologies to gain a better view of their applicability. Table 2.1 compares the important attributes of each reference topology.

2.6 Summary

This chapter gave some fundamental knowledge of reference voltage generators, and described the basic requirements of voltage references. Then, some of most widely used reference voltage generators are presented, and their operating principles, including the process requirements, advantages and the disadvantages are briefly discussed. Finally, the comparison is made between the described reference generators.

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Chapter 3

Area-efficient bandgap reference

3.1 Introduction

Precise voltage references with good stability against temperature and supply voltage are always in great demand in many applications such as analog-to-digital (A/D) converters and voltage regulators. Most voltage references are usually designed based on a bandgap reference [1, 2, 3, 4], which add the forward bias voltage across a p-n diode with a voltage that is proportional to absolute temperature (PTAT). In the conventional CMOS process, nearly ideal diode characteristics can be obtained from a base-emitter voltage (V_{BE}) of parasitic substrate transistors [5]. As CMOS technologies continue to shrink, the design area becomes more expensive. On the other hand, demand for the portable electronic devices and micro sensors makes the low power circuits more and more important. As a result, there is an increasing demand to design area-efficient and low power analog circuits. However, compared to other devices, parasitic transistors need larger design area. Additionally, despite the MOSFETs are scaled down to the nanoscale regime, parasitic bipolar transistors are left unchanged. Therefore the design area of the common conventional bandgap reference, which uses area ratio of the parasitic bipolar transistors to generate reference voltage, becomes a critical problem. Another problem of the traditional bandgap reference is no flexibility in output voltage. Because, as it name suggests, the output voltage is close to the bandgap of silicon, which is approximately 1.2 V at room temperature. To overcome those problems, several techniques have been demonstrated. Switched-capacitor bandgap references proposed in [6, 7, 8], use one parasitic bipolar transistor and a switched capacitor network to generate reference voltage. Thus, this structure can significantly reduce the chip area and eliminate the bipolar transistor device mismatch, and therefore widely used in area-efficient and high-accuracy applications [9, 10, 11]. However, main disadvantage of switched-capacitor references is that the output is not valid in one phase. Another problem is relatively large capacitors should be used in output stage occupying more chip area. Another design challenge in switched-capacitor references is how to generate the current sources, that use to bias the p-n junction. The circuits proposed in [5, 12] are capable of providing a fraction of the bandgap voltage. However, such references require resistor networks with large values occupying large design area.

This chapter presents an improved bandgap reference which is capable of generating reference voltage by using only one parasitic bipolar transistor, thus the area size becomes significantly smaller and bipolar transistors device mismatch is eliminated. Moreover the proposed circuit outputs a fraction of the silicon bandgap voltage, and the reference voltage V_{REF} can be set to almost any value.

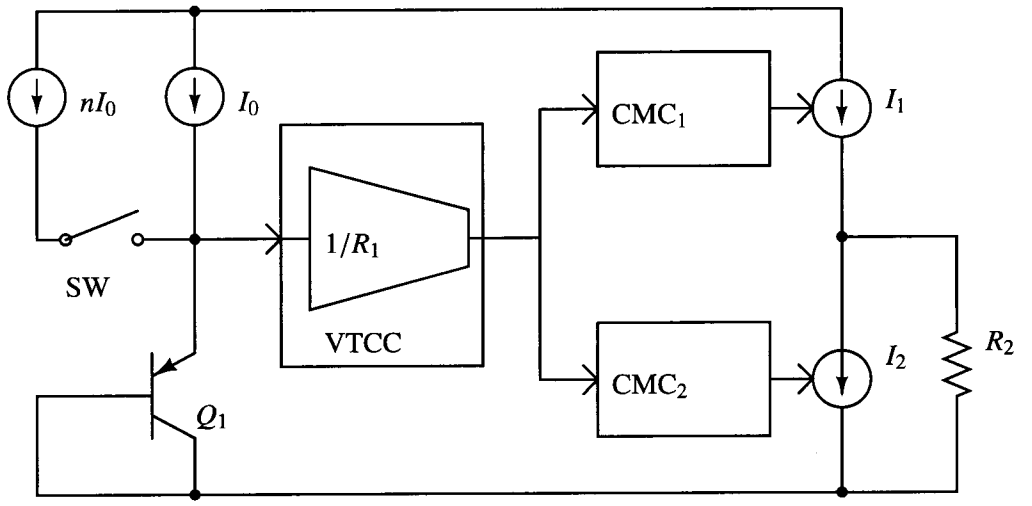


Figure 3.1: Conceptual diagram of the proposed bandgap reference

3.2 Architecture of the proposed circuit

As mentioned in the previous chapter, it is well known that the base emitter voltage of bipolar transistor, V_{BE}, exhibits a negative temperature coefficient. Additionally, the difference between base-emitter voltages (ΔV_{BE}) of two identical bipolar transistors, which operate at unequal current densities, exhibits a positive temperature coefficient. The conventional bandgap reference uses sum of V_{BE} and ΔV_{BE} with proper weighting to obtain zero TC. Therefore, the output voltage of the conventional bandgap reference can be written as

$$V_{REF} = \alpha V_{BE1} + \beta \Delta V_{BE} \tag{3.1}$$

Constants α and β are chosen to obtain a V_{REF} that has a minimum variation over the temperature range of interest. Assuming $\alpha,\beta > 0$, eq. (3.1) can be rewritten as follows.

$$V_{REF} = (\alpha + \beta)V_{BE1} - \beta V_{BE2} \tag{3.2}$$

It is important to notice that, temperature-independent voltage can be generated by using two voltages that have only negative TCs. Two different negative TC voltages can be produced by using only one bipolar transistor and switched current technique. Therefore, this method lets us eliminate the need of parasitic bipolar array, which occupies large design area , from conventional bandgap references. The proposed bandgap reference uses the method shown in eq. (3.2) to generate the reference voltage.

Figure 3.1 illustrates the conception of the proposed bandgap reference. The circuit consists of two supply independent current sources, a parasitic bipolar transistor, a voltage-to-current converter (VTCC), two current memory cells (CMC) and a resistor. Switch SW controls the current feeds into Q_1 and generates two different base-emitter voltages. When SW is ON, current $(n+1)I_0$ is fed into Q_1 and base-emitter voltage becomes V_{BE1}. Next SW turns off, current feeds into Q_1 changes to I_0 and base-emitter voltage becomes V_{BE2}. VTCC network converts those V_{BE1} and V_{BE2} to currents given by V_{BE1}/R_1 and V_{BE2}/R_1. Where $1/R_1$ is transconductance of the VTCC. In the proposed circuit we use CMC_1 and CMC_2, which are designed to behave as high accuracy current cells and

current mirrors, to generate continuous current sources $I_1 = (\alpha + \beta)V_{BE1}/R_1$ and $I_2 = \beta V_{BE2}/R_1$ from discontinuous currents V_{BE1}/R_1 and V_{BE2}/R_1, respectively. As shown in eq. (3.2), it is possible to generate a temperature independent voltage by injecting the subtracted current $(\alpha + \beta)V_{BE1}/R_1 - \beta V_{BE2}/R_1$ into the resistor R_2. Supply independent current sources, VTCC and current memory technique are described in next section.

3.3 Proposed bandgap reference

3.3.1 Circuit operation

The schematic of the proposed area-efficient CMOS bandgap reference circuit is shown in Fig. 3.2, and Fig. 3.3 represents the timing diagram. The proposed circuit has four main parts:

- Supply independent current source
- Current switch
- Output stage
- Startup circuit
- Bias generator

Supply independent current source

The current source has two modes, which depend on the status of switch SW_1. Figure 3.4(a) represents the mode when SW_1 is ON.

Assume that M_1 drain current is mI_0 during this phase and current mirror ratio of $M_1 : M_2$ is $m : n + 1$. The current given by I_0 flows through R_1, generating the voltage of

$$V_{R1,1} = mR_1I_0 \tag{3.3}$$

across the resistor.

On the other hand, M_2 drain current (I_{M2}), given by $(n + 1)I_0$, is injected into Q_1. Therefore, base-emitter voltage of Q_1 can be written as

$$V_{BE1} = \frac{kT}{q} ln \frac{(n + 1)I_0}{I_S} \tag{3.4}$$

However, the differential amplifier compares V_{BE1} and $V_{R1,1}$, then regulates them to be equal. Thus, the gate voltage of M_1 and M_2 is forced to flow supply independent currents through M_1 and M_2. Using eqs. (3.3) and (3.4), we can write the expression for I_0 as

$$mR_1I_0 = \frac{kT}{q} ln \frac{(n + 1)I_0}{I_S} \tag{3.5}$$

Figure 3.5 represents the plot of eqs. (3.4) and (3.4) for R_1 = 48 kΩ, T=300 K, $I_S = 5.839 \times 10^{-12}$ μA, m=27, and $(n + 1)$=32 . It is clear that eq. (3.5) has two roots, corresponding to the currents $I = I_{zero}$ and $I = I_{stable}$. Therefore, to ensure that $I = I_{stable}$ is achieved, a start-up circuit should be used with the supply independent current source. The start-up circuit is discussed in latter section.

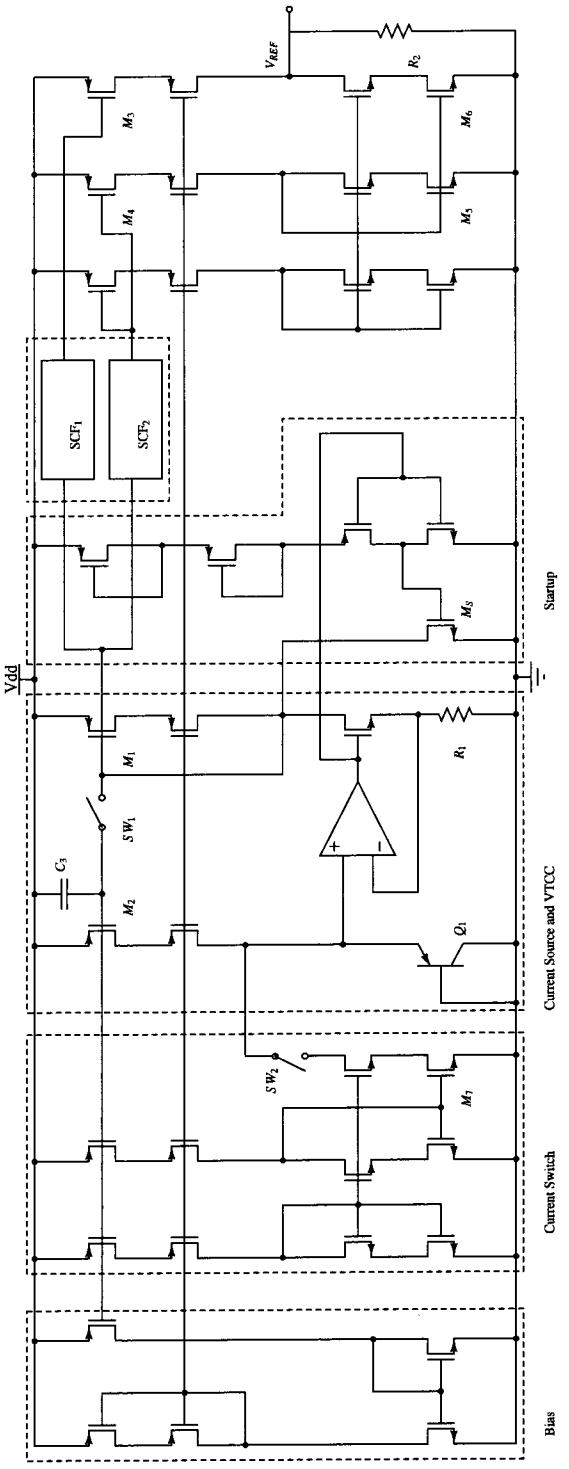


Figure 3.2: Schematic of the proposed area-efficient CMOS bandgap reference.

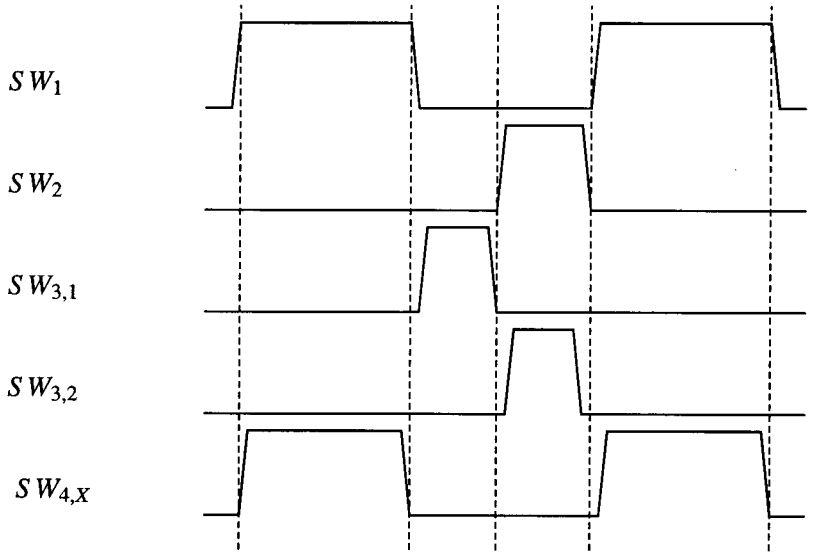


Figure 3.3: Timing diagram

The mode of the supply independent current source changes when SW_1 turns OFF. Figure 3.4(b) represents the schematic of this mode. The charge stored in gate of M_2 and C_3 keeps the same drain current through M_2 as that of when SW_1 is ON. However, in this mode, operational amplifier places the base-emitter voltage of Q_1 across R_1. Thus the current flows through M_1 is determined by the base-emitter voltage of Q_1. Hence we can say that the circuit is functioning as a voltage-to-current converter. In this phase, the current switching circuit starts functioning.

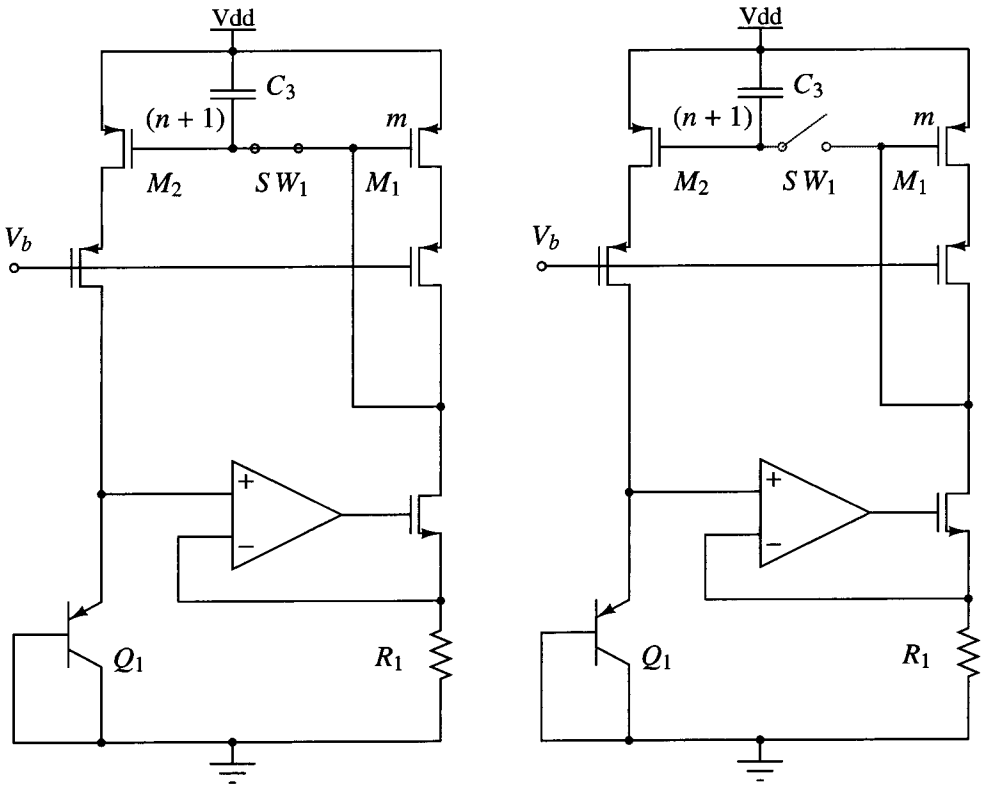
Current switching circuit

In Fig.3.2, when both SW_1 and SW_2 are OFF, the charge stored in gate of M_2 and C_3 keeps the same drain current through M_2 as that of when SW_1 is ON, and all the current is injected into Q_1. Thus base-emitter voltage of Q_1 is also the same as SW_1 was ON, which is given by V_{BE1}. Thus the current flows through R_1 can be written in another way as follows.

$$I_1 = mI_0 = \frac{V_{BE1}}{R_1} \tag{3.6}$$

As shown in Fig. 3.3, SW_2 only turns ON, when SW_1 is OFF. Thus switch SW_2 does not affect the current generated in supply independent current source. However, it changes the current injected into Q_1, when SW_1 is OFF. In the phase when SW_1 is OFF and SW_2 is ON, the charge stored in gate of M_2 and C_3 keeps the same drain current through M_2 as that of when SW_1 is ON, which is given by $(n+1)I_0$. In Fig.3.2, the current switch circuit is designed to sink the current, which is equal to $n/(n+1) \times I_{M2}$, when SW_2 is ON. Thus the current given by nI_0 is sunk by the current switch. The resultant current given by I_0 is injected to Q_1. Therefore, the base-emitter voltage of Q_1 in this phase is expressed by

$$V_{BE2} = \frac{kT}{q} ln \frac{I_0}{I_S} \tag{3.7}$$



(a) Supply independent Current Source

(b) Voltage-to-current converter

Figure 3.4: The two modes of current source

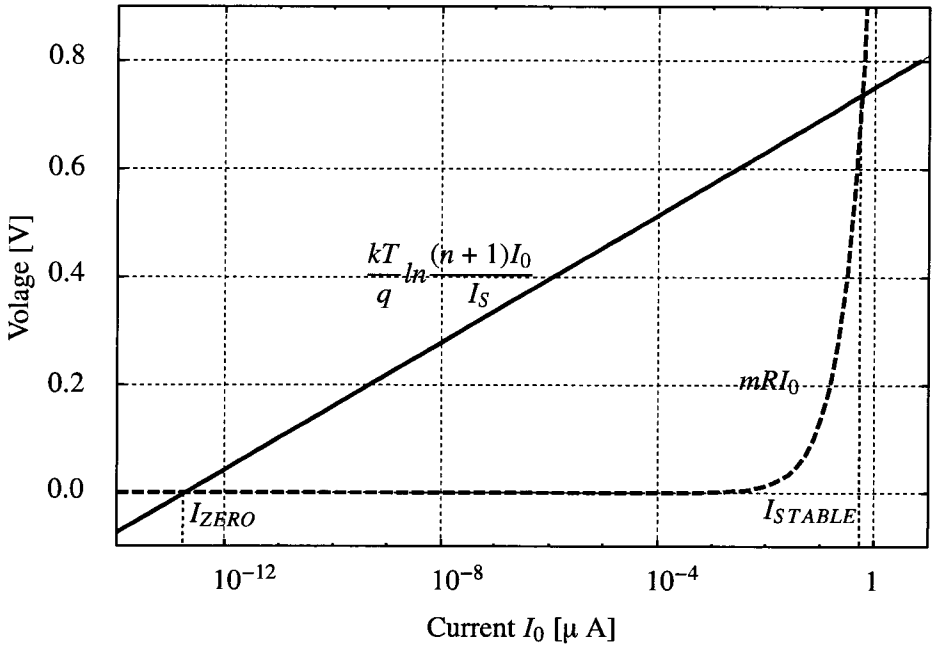


Figure 3.5: Calculated output current of supply independent current source

The operational amplifier places this voltage across R_1, forcing the gate voltage of M_1 to flow the current given by

$$I_2 = \frac{V_{BE2}}{R_1} \tag{3.8}$$

through M_1. Thus, during this phase the current through R_1 is also given by eq. (3.8). The output stage, which is described in next section, mirrors the currents given in eqs. (3.6) and (3.8) with proper weighting, and uses them to generate the reference voltage.

Output stage

In the proposed circuit, current memory technique (discuss later), is used in order to archive a continuous output reference. First, when both SW_1 and SW_2 are OFF, switched-capacitor filter SCF_1 senses the gate voltage of M_1, and memorizes in gate nodes of M_3. Next, when SW_1 is off and SW_2 is ON, SCF_2 senses the gate voltage of M_1, and memorizes in gate nodes of M_4.

Assuming that aspect ratio of $M_1 : M_3 : M_4$ is $m : (\alpha + \beta) : 1$ and that of $M_5 : M_6$ is $1 : \beta$, continuous drain currents of $M_3(I_3)$ and that of $M_6(I_6)$ can be derived as

$$I_3 = \frac{\alpha + \beta}{m} \frac{V_{BE1}}{R_1} \tag{3.9}$$

$$I_6 = \frac{\beta}{m} \frac{V_{BE2}}{R_1} \tag{3.10}$$

Thus the current flows through R_2 becomes

$$I_{OUT} = I_3 - I_6 = \frac{\alpha + \beta}{m} \frac{V_{BE1}}{R_1} - \frac{\beta}{m} \frac{V_{BE2}}{R_1} \tag{3.11}$$

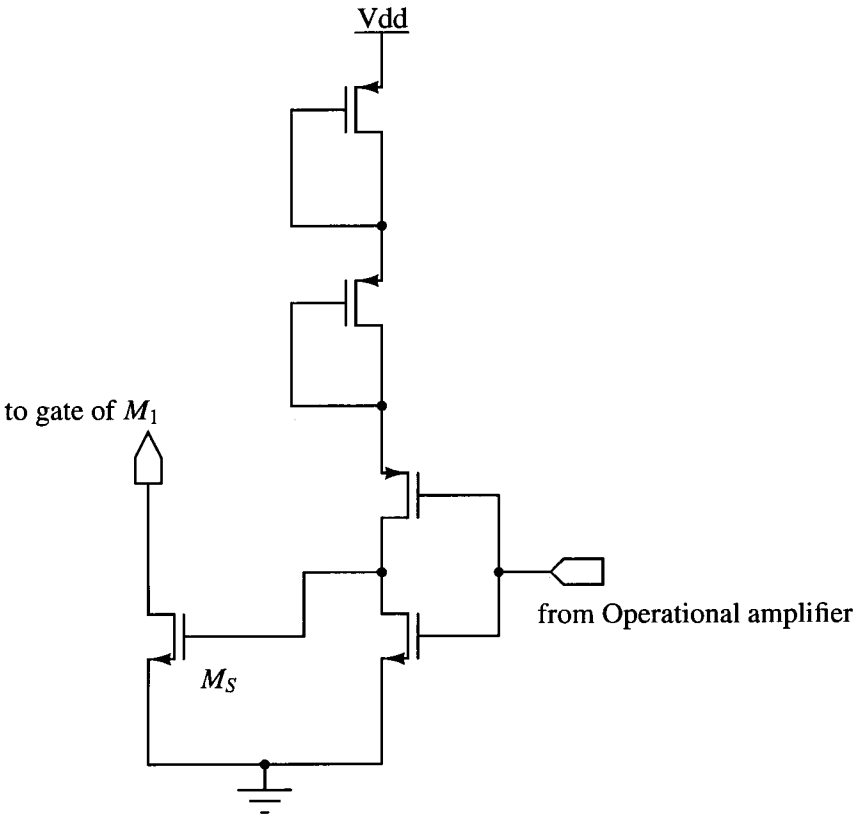


Figure 3.6: Start-up circuit

Therefore, the output voltage of the proposed bandgap reference can be expressed as

$$\begin{aligned} V_{REF} &= R_2 \times I_{OUT} \\ &= \frac{R_2}{mR_1}\frac{kT}{q}\left[(\alpha+\beta)ln\frac{(n+1)I_0}{I_S} - \beta ln\frac{I_0}{I_S}\right] \end{aligned} \tag{3.12}$$

As we discussed in the previous section, by choosing α and β such that

$$(\alpha+\beta)\frac{\partial V_{BE1}}{\partial T} - \beta\frac{\partial V_{BE2}}{\partial T} = 0 \tag{3.13}$$

reference voltage with zero TC can be obtained. Furthermore, by changing R_2 , V_{REF} can be set to any value between $(V_{DD} - 2V_{ODP})$ and $2V_{ODN}$, where V_{ODP} and V_{ODN} are the overdrive voltages of pMOS and nMOS, respectively.

Startup circuit

As discussed in the previous section, the supply independent current source has two stable states, corresponding to the currents given by I_{Zero} and I_{stable}, as shown in Fig. 3.5 . To ensure that the stable state is achieved, a startup circuit shown in Fig. 3.6 is used. The proposed startup circuit consists of an inverter and a pull-down transistor. The input of the inverter is connected to the

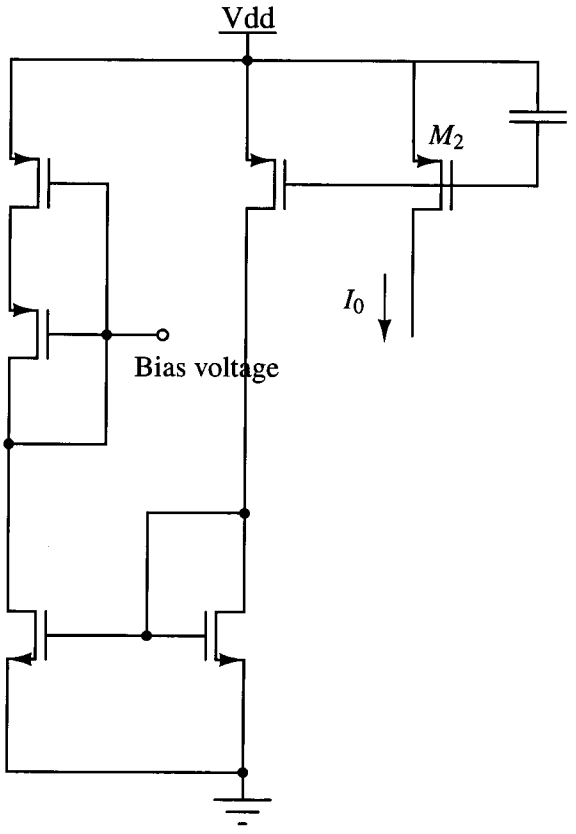


Figure 3.7: Bias generator

output of the operational amplifier, and the output controls the gate of pull-down transistor M_S. If the output voltage of differential amplifier is lower than the inverter threshold voltage, M_S becomes ON and pulls down the voltage on gates of pMOSs, so that M_1 and M_2 avoid the current state of I_{Zero}.

Bias generator

All the current mirrors used in the proposed design is implemented with cascode current mirrors, to achieve the high output impedance and to reduce the current mirror mismatch (discuss later). The bias generator circuit shown in Fig. 3.7 is used to generate the bias voltage of pMOS cascode transistors.

As discussed in the previous section, M_2 drain current is constant regardless of the status of SW_1 and SW_2. The bias generator uses this constant M_2 drain current as the input, and generates the bias voltage of pMOS cascode transistors.

3.3.2 Switched-capacitor filter (SCF)

To achieve continuous current sources from discontinuous currents, the proposed circuit uses current memory technique, which is implemented using the switched-capacitor filter shown in Fig. 3.8, where X represents the SCF number (i.e. SCF_1 consists of C_1 and $C_{2,1}$). Capacitors and

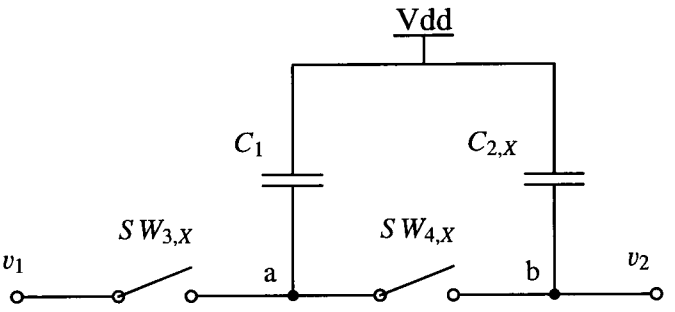


Figure 3.8: Switched-capacitor filter

switches used in SCF were implemented by metal insulator metal capacitors (MIMCAPs) and CMOS switches. $SW_{3,X}$ and $SW_{4,X}$ are controlled by non-overlapping clock signals as shown in Fig. 3.3. When $SW_{3,X}$ is ON, capacitor C_1 is charged to gate voltage of M_1. While $SW_{4,X}$ is ON, if v_1 and v_2 are not equal, then charge is redistributes among C_1 and $C_{2,X}$. The time constant of the switched-capacitor filter is given by

$$\tau = \frac{C_{2,X}}{C_1} \cdot \frac{1}{f_{CLK}} \tag{3.14}$$

where f_{CLK} is the frequency of the switch control signals. Time constant τ, given by the above equation, is an important factor which determines the settling time of the proposed circuit. Another important fact that should be considered is effect of charge injection, which is one of the major problems found in systems using switched capacitors. Voltages in nodes a and b change due to charge injection when $SW_{3,X}$ and $SW_{4,X}$ turn off. However, in node a, the channel charge of $SW_{3,X}$ is absorbed by $SW_{4,X}$, minimizing the voltage difference between two phases. Thus the charge injection is negligible. But the voltage change in node b due to charge injects from $SW_{4,X}$ can not be neglected. This problem will be discussed in a later section.

3.3.3 Differential amplifier

The op-amp used in the proposed bandgap reference circuit is a simple p-channel input two-stage differential amplifier as illustrated in Fig. 3.9. In the proposed design, the operational amplifier common mode voltage equals to the base-emitter voltage of the bipolar transistor, which is approximately 500 mV to 700 mV. This requires an operational amplifier with low input-common mode voltage. The input common mode range of the differential amplifier shown in Fig. 3.9 is from $V_{DD} - V_{THP} - V_{ODP}$ to V_{GND}, so that it enables us to use low input voltages.

V_{PBIAS} shares the same bias voltage with M_2 in Fig. 3.2, providing supply independent bias current. Inputs V_p and V_n are connected to the nodes of Q_1 and R_1, respectively. A compensation capacitor C_C, as shown in Fig. 3.9, is used to ensure the stability of the current source generator.

3.4 Design issues and accuracy analysis

3.4.1 Input offset voltage

As discussed in the previous section, every operational amplifier suffers from input offset voltage, and this input offset voltage of the operational amplifier introduces a significant error in the output

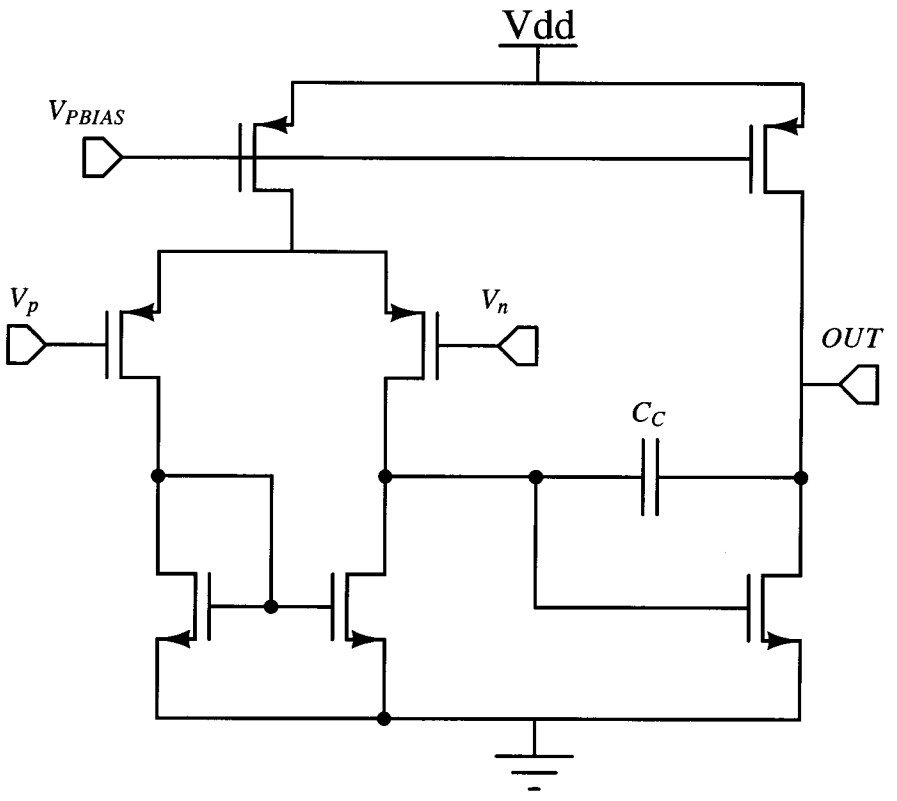


Figure 3.9: Two-stage differential operational amplifier

voltage of bandgap references. In conventional bandgap references, input offset voltage is amplified by a factor larger than 10 and appears in the output [13].

In the proposed design, it is assumed that the operational amplifier input offset varies negligibly between the two phases. Therefore, also taking into account the input offset voltage of operational amplifier, V_{OS}, eq. (3.6) and eq. (3.8) can be rewritten as

$$I_{1,OS} = I_{0,OS} = \frac{V_{BE1} + V_{OS}}{R_1}, \tag{3.15}$$

and

$$I_{2,OS} = \frac{V_{BE2} + V_{OS}}{R_1}, \tag{3.16}$$

respectively.

Hence, the output of the proposed bandgap reference including the effect of input offset voltage is given by

$$V_{REF,OS} = \frac{R_2}{mR_1}\frac{kT}{q}\left[(\alpha+\beta)\ln\frac{(n+1)I_0}{I_S} - \beta\ln\frac{I_0}{I_S}\right] + \frac{R_2}{mR_1}\alpha V_{OS} \tag{3.17}$$

From eq. (3.17), it can be observed that the amplifier input offset voltage is multiplied by the factor of R_2/mR_1. This means in return that the effect of the input offset voltage increases with the increase of R_2/mR_1. For simplicity assume that the current mirror ratios are fixed. Then, as mentioned in the previous section, by only changing the value of R_2, the output reference voltage can

be set to any value between $(V_{DD} - 2V_{ODP})$ and $2V_{ODN}$. Thus the maximum value for R_2/mR_1 can be calculated when the output reference reaches to $(V_{DD} - 2V_{ODP})$. Assuming that V_{ODP}=0.1 V, the maximum output reference voltage for the proposed design can be given by

$$V_{REF,MAX} = 2.8\ \text{V} - 2 \times 0.1\ \text{V} = 2.6\ \text{V} \tag{3.18}$$

To set the output reference to the value given in eq. (3.18), R_2 should be set to 672 kΩ, resulting the maximum theoretical value

$$\frac{R_2}{mR_1}\alpha\Big|_{MAX} = 3 \tag{3.19}$$

Therefore, in the worst case, the input offset voltage of the amplifier will be multiplied by the factor 3 and appears in the output reference.

However, on the other hand, let us assume that the output reference is set to the typical value of the conventional bandgap references, which is approximately 1.2 V at room temperate. By using the same method as above, it can be shown that the input offset voltage of the operational amplifier will be only multiplied by less than 2. Thus, compared to conventional bandgap reference in which the multiplication factor is larger than 10 [13], the proposed circuit attains superior performance.

3.4.2 Current mirror ratios

The performances of most of the current mode circuits rely on matching of the current mirrors.

On the other hand, the matching performance of CMOS current mirror is mainly limited by the matching properties and the operating conditions of MOS transistors in the mirror circuit.

Since the current mirrors are used in the current source, current switching stage and the output stage of the proposed design, the performances of the output voltage is directly related to the matching performances of the current mirrors. By using eq. (3.12), the dependence of output reference on mismatch of current mirror ratios m, $(\alpha + \beta)$, and β can be calculated. Assume that the worst case of current mirror mismatch is ε%. Therefore, the worst case output reference due to ε% mismatch of m, $(\alpha + \beta)$,and β can be written as

$$V_{REF,\varepsilon} = \frac{R_2}{m\left(1 - \frac{\varepsilon}{100}\right)R_1}\left[(\alpha+\beta)\left(1 + \frac{\varepsilon}{100}\right)V_{BE1} - \beta\left(1 - \frac{\varepsilon}{100}\right)V_{BE2}\right] \tag{3.20}$$

From eq. (3.12) and eq. (3.20), the error of the output reference can be expressed as follows.

$$V_{REF,error} = \frac{V_{REF,\varepsilon} - V_{REF}}{V_{REF}} \times 100\% \tag{3.21}$$

Figure 3.10 represents the graph of eq. (3.21). In mass production, the deviation of the bandgap reference voltage is approximately ± 5% [14]. From Fig. 3.10 it is clear that ε should be kept to less than ±0.7%, to guarantee the worst case mismatch of ± 5% in the output of the proposed design. One main source of mismatch is differences in the drain-source voltages of the input transistors and output transistors. However, by using proper circuit techniques such as cascode current mirrors, the nearly ideal operating conditions can be achieved. Thus the influence of differences in the drain-current voltages on matching performance can be eliminated [15]. In the proposed design, all the current mirrors were implemented by using casdode current mirrors, therefore, the current mirror mismatch due to difference in the drain-source voltage of the transistors is negligible. Consider the simple current mirror shown in Fig.3.11. Assume that the threshold voltage mismatch of the nMOS

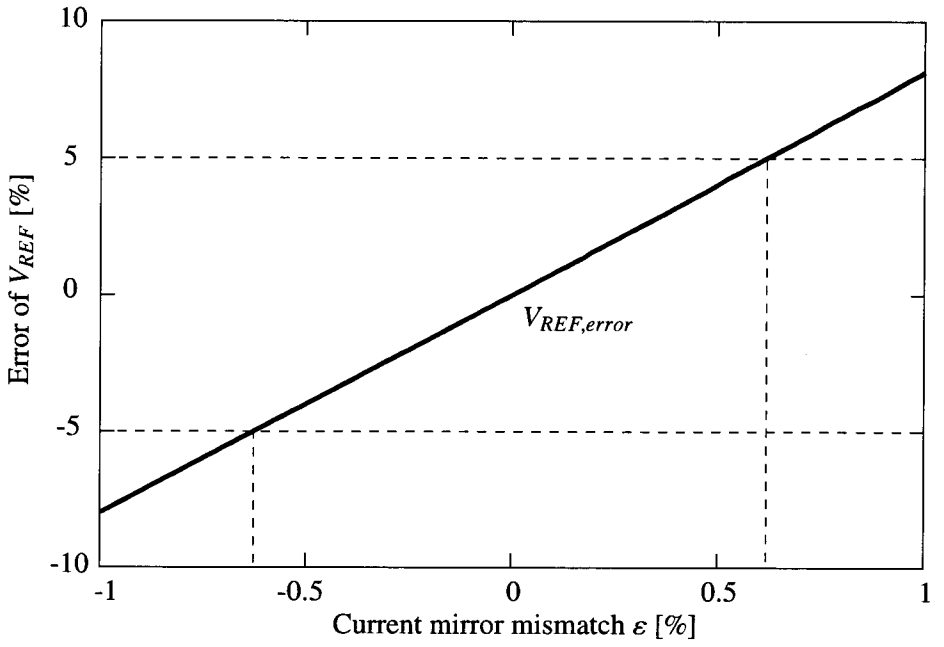


Figure 3.10: V_{REF} variation due to current mirror mismatch

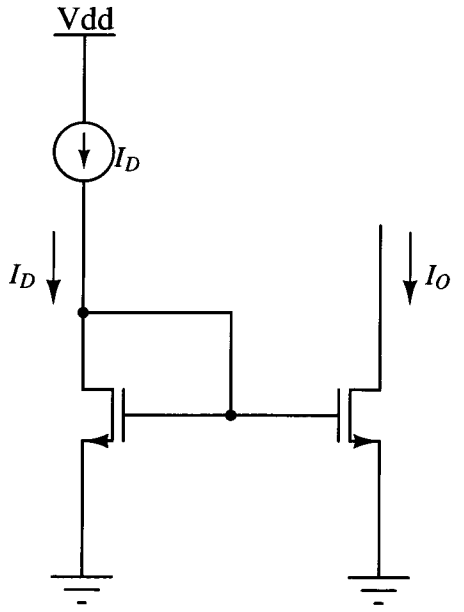


Figure 3.11: Mismatch of simple current mirror

transistors is $V_{TH,1} - V_{TH,2} = \Delta V_{TH}$. Thus the current ratio is described by

$$\begin{aligned} \frac{I_0}{I_D} &= \frac{\beta(V_{GS} - V_{TH} - \Delta V_{TH})^2}{\beta(V_{GS} - V_{TH})^2} \\ &\approx 1 - \frac{2\Delta V_{TH}}{V_{GS} - V_{TH}} \end{aligned} \tag{3.22}$$

The latter part of eq. (3.22) represents the mismatch of the current mirror. From above results, it is clear that to minimize the current mirror mismatch, the overdrive voltage $V_{GS} - V_{TH}$ must be maximized. On the other hand, the threshold mismatch ΔV_{TH} can be expressed by [16, 17]

$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}} \tag{3.23}$$

where A_{VTH} is the proportionality factor and scales down with the gate oxide thickness t_{ox}. When t_{ox} is given in angstroms and W and L in microns, eq. (3.23) can be written as [4]

$$\Delta V_{TH} = \frac{0.1 t_{ox}}{\sqrt{WL}} \text{ mV} \tag{3.24}$$

Therefore, the current mismatch of the current mirror shown in Fig. 3.11 can be approximated by

$$\frac{\Delta I}{I_D} = \frac{0.1 t_{ox}}{\sqrt{WL}} \times \frac{2}{V_{GS} - V_{TH}} \tag{3.25}$$

For simplicity. assume that the current mirror is implemented by square transistors, and the overdrive voltage is approximately 100 mV. The oxide thickness t_{ox} is approximately 40 Å in 0.25 µm CMOS technology, which is used to design the proposed bandgap reference. Thus the minimum values for L and W can be calculated as

$$L_{MIN}, W_{MIN} = 0.1 \times 40 \times \frac{2}{100} \times \frac{100}{0.7} \approx 11.4 \text{ µm} \tag{3.26}$$

However, the good layout techniques such as common centroid and use of dummy devices, can be effectively used to increase the matching performances, on the other words, to reduce the minimum values of L and W.

The circuit techniques presented and demonstrated in [18] and [19] have successfully achieved maximum ε of about 0.1 and 0.01, respectively. Thus, using those current mirror techniques, it is possible to achieve the accuracy of up to 0.1% in the proposed bandgap reference. However, those techniques use more complex circuitry and larger transistors, therefore, occupies more design area.

3.4.3 Switched feedthrough

Since the proposed circuit uses the switched-capacitor technique, the limitations due to the switches is one of the main design challenges. The two of the most non-ideal and serious effects that limit the advantages of MOS switches are :

- Clock feedthrough (also known as charge feedthrough [20] or capacitive through)
- Charge injection

The clock feedthrough occurred due to the overlapping (coupling) capacitance from the gate to source/drain. This gate-drain and gate-source overlapping capacitance allows charge to be transferred from clock signal, which is applied in the gate to switch on and switch off the transistor, to the drain and source. This charge produces an error voltage on load capacitor.

On the other hand, the charge injection depends on many factors such as dimensions and threshold levels of the MOS transistors, voltage and impedance of input and output nodes, waveform and magnitudes of the clock signal. Thus, compared to clock feedthrough, charge injection is more complex and difficult to model and compensate. However, both phenomenas are unavoidable when dealing with analog circuits that use switched control signals.

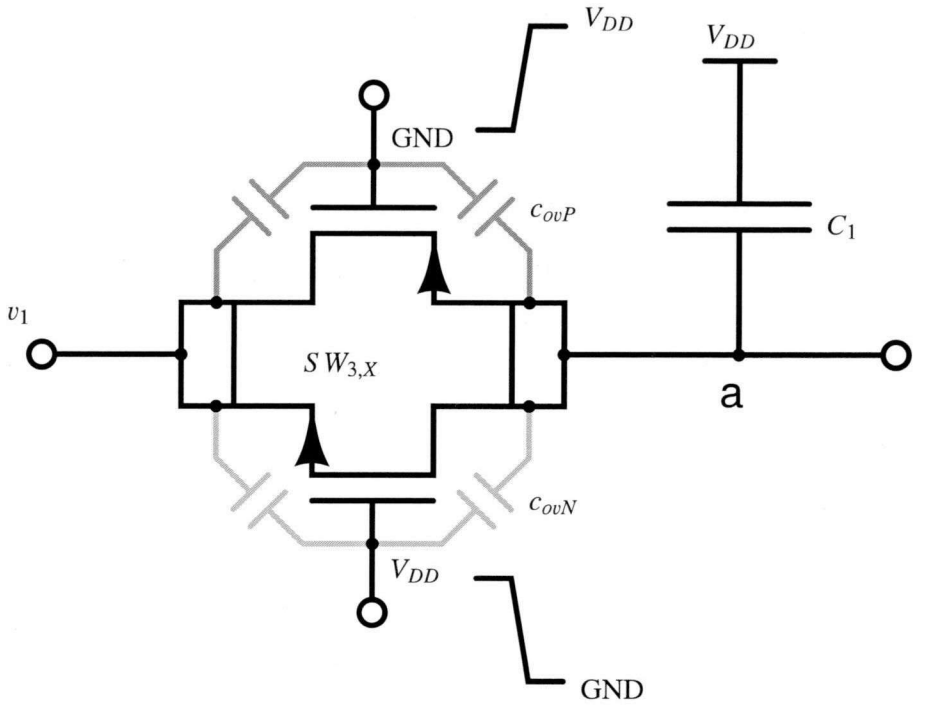


Figure 3.12: Effect of clock feedthrough

Clock feedthrough

The input stage of the switched capacitor filter presented in Fig. 3.8 is shown in Fig. 3.12 in details. The capacitance C_{ovP} and C_{ovN} are the overlap capacitors of pMOS and nMOS transistors that are given by

$$c_{ovP} = C_{OX} \cdot W_P \cdot LD_P, \tag{3.27}$$

and

$$c_{ovN} = C_{OX} \cdot W_N \cdot LD_N, \tag{3.28}$$

here, LD_P and LD_N are the lengths of the gate that overlaps the drain/source.

When the switch turns ON, the input signal v_{in} is connected to C_1 through the pMOS and nMOS transistors. Thus C_1 is charged to input signal. The final voltage of the node a does not have any effects from clock feedthrough. Next, consider the case when switch turns off. In this time, as shown in Fig. 3.12, the gate voltage of pMOS transistor changes from GND to V_{DD}, and the gate voltage of nMOS transistor changes from V_{DD} to GND. This voltage changes in the clock signals effect the final voltage of node a. When the switch turns off, the pMOS transistor causes a voltage change of

$$\delta v_{cf,P} = \frac{c_{ovP}}{C_1 + c_{ovP}} \cdot (-V_{DD}), \tag{3.29}$$

and the nMOS transistor causes a voltage change of

$$\delta v_{cf,N} = \frac{c_{ovN}}{C_1 + c_{ovN}} \cdot (V_{DD}) \tag{3.30}$$

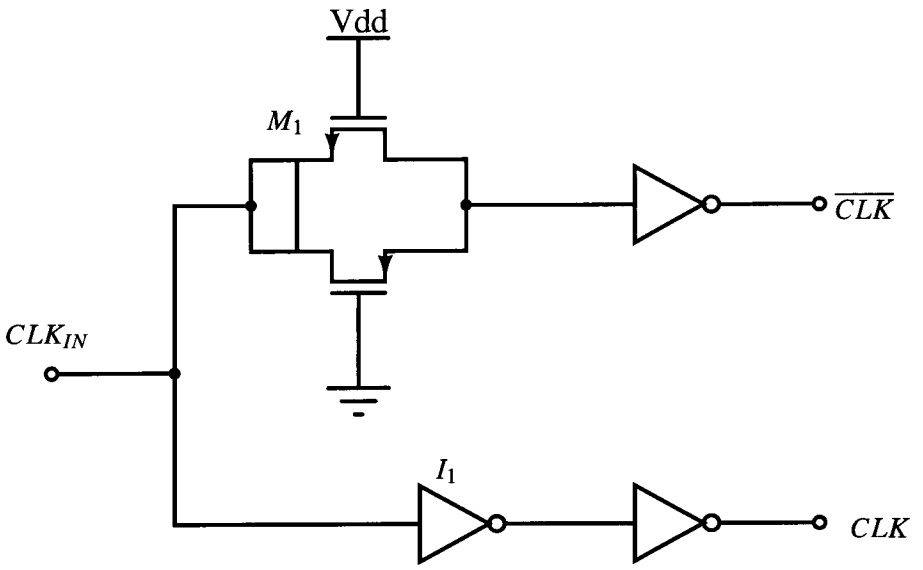


Figure 3.13: Circuit generating complementary clocks

in node a. Thus the resultant voltage change in node a due to the change in clock signals can be expressed by,

$$\begin{aligned}\delta v_{cf,1} &= \delta v_{cf,N} + \delta v_{cf,P} \\ &= V_{DD} \cdot \left\{ \frac{c_{ovN}}{C_1 + c_{ovN}} - \frac{c_{ovP}}{C_1 + c_{ovP}} \right\}\end{aligned} \tag{3.31}$$

Note that $\delta v_{cf,1}$ is independent of the input signal v_1. This means, the clock feedthrough introduces a nearly constant offset voltage in the output. Furthermore, from eq. (3.31) it can be seen that the CMOS switch fairly cancels the effects of clock feedthrough, because the complementary signals act to cancel each other. However, the above expression for δv_{cf} is only valid if precisely controlled complementary signals are used to turn off the pMOS and nMOS transistors. To overcome this problem, the circuit shown in Fig. 3.13 is used in the proposed design to generate complementary clock signals. In Fig. 3.13, the delay of inverter I_1 is duplicated through the gate of M_1, providing complementary clocks.

Charge injection

To study the effects of charge injection, consider Fig. 3.14, which represents the detailed version of the input stage of switched capacitor filter shown in Fig. 3.8 .

When the switch is ON, inverted channels exist at the oxide-silicon interfaces in both nMOS and pMOS transistors. The total charge in the inverted channels pMOS and nMOS transistor can be given by

$$Q_{ch,P} = W_P L_P C_{OX} \left(v_{in} - |V_{TH,P}| \right), \tag{3.32}$$

and

$$Q_{ch,N} = W_N L_N C_{OX} \left(V_{DD} - v_{in} - V_{TH,N} \right), \tag{3.33}$$

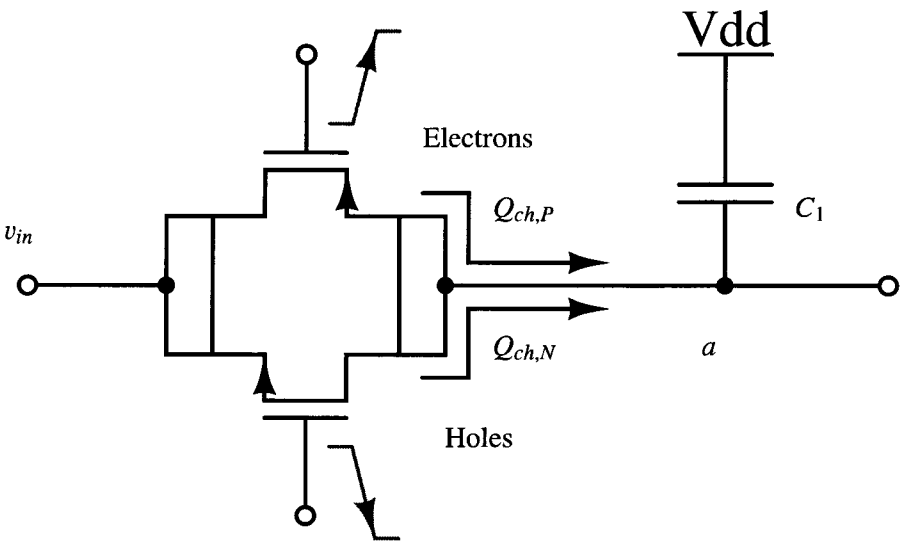


Figure 3.14: Effect of charge injection in node a

respectively. When the switch turns off, this charge in inverted channels is injected to into v_{in} and onto the load capacitor C_1, through source and drain terminals of nMOS and pMOS transistors. This phenomena is called charge injection.

However, the charge injected into v_{in} is absorbed by the input source, which is assumed to be a low-impedance, resulting no error. On the other hand, the charge injected onto the load capacitor introduces an error in the final voltage on the capacitor. For simplicity, assume that the half of the channel charge in pMOS and nMOS transistors is injected onto load capacitor. Therefore, the voltage change in C_1 due to charge injection can be expressed by

$$\begin{aligned}\delta v_{ci,1} &= \frac{Q_{ch,N}}{2C_1} - \frac{Q_{ch,P}}{2C_1} \\ &= \frac{C_{OX}}{2C_1}\Big\{W_N L_N \left(V_{DD} - v_{in} - V_{TH,N}\right) - W_P L_P \left(v_{in} - |V_{TH,P}|\right)\Big\}\end{aligned} \tag{3.34}$$

Note that as shown in Fig. 3.14, pMOS and nMOS transistors injects electrons and holes into load capacitor, respectively. This opposite charges cancel each other reducing the effect of charge injection. However to achieve $\delta v_{ci,1} = 0$, we should select the device sizes of MOS transistors, such that $Q_{ch,P} = Q_{ch,N}$ for selected v_{in}. On other words, the complete cancellation of charge injection occurs only once for varies input levels of v_{in}. Even though the complete cancellation does not occurs for other input levels, the cancellation of opposite charges reduce the effect of charge injection. Thus all the switches in the proposed design implemented by CMOS switches to reduce the effect of charge injection.

Charge cancellation in node a

Figure 3.15 illustrates the instants of SW_1 turning off and SW_2 turning ON, in switched capacitor filter. In the beginning, SW_1 is ON. Then, after the clock changes, it turns off. Then after δT time SW_2 turns ON. In Fig. 3.15, $\delta q_{p,1}$ and $\delta q_{n,1}$ represent the total charge dispatch onto C_1 from pMOS

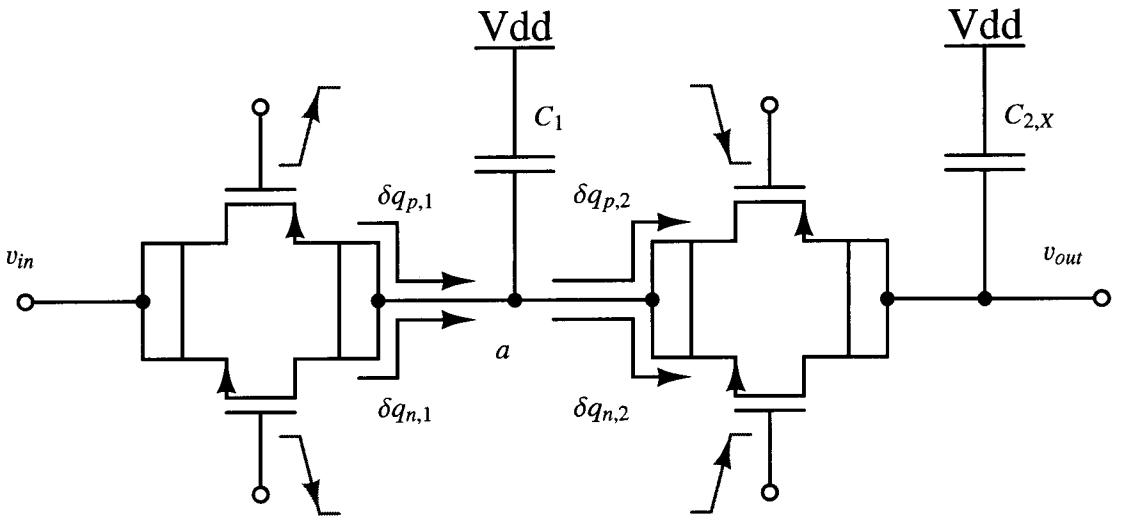


Figure 3.15: Charge injection and clock feedthrough cancellation in node a

and nMOS, due to both charge injection and clock feedthrough, respectively. Then, $\delta q_{p,2}$ and $\delta q_{n,2}$ represent the total charge absorbed from C_1 into pMOS and nMOS when they turn ON, respectively.

Thus the resultant voltage change in node a after SW_2 turns off can be expressed by

$$\delta v_{C1} = \frac{1}{C_1}\Big\{\big(\delta q_{p,1} + \delta q_{n,1}\big) - \big(\delta q_{p,2} + \delta q_{n,2}\big)\Big\} \tag{3.35}$$

From eqs. (3.31), (3.34) and (3.35)

$$\begin{aligned}\delta v_{C1} &= \big(\delta v_{cf,1} + \delta v_{ci,1}\big) - \big(\delta v_{cf,2} + \delta v_{ci,2}\big) \\ &= \big(\delta v_{cf,1} - \delta v_{cf,2}\big) - \big(\delta v_{ci,2} - \delta v_{ci,1}\big)\end{aligned} \tag{3.36}$$

As discussed previously, $\delta v_{cf,1}$ and $\delta v_{cf,2}$ are independent from input levels. Furthermore, pMOS and nMOS transistors used in SW_1 and SW_2 share the same device dimensions. Therefore, neglecting the dimension mismatch of pMOS and nMOS transistors, it can be said that $\big(\delta v_{cf,1} - \delta v_{cf,2}\big) \approx 0$ for all input levels.

On the other hand, as it clear from eq. (3.34), $\delta v_{ci,1}$ and $\delta v_{ci,2}$ depend on not only the input levels, but also the threshold voltage of pMOS and nMOS devices. However, for small values of change in v_{in} and threshold mismatches, it can also be said that $(\delta v_{ci,1} - \delta v_{ci,2}) \approx 0$. Thus, the voltage changes in node a due to charge injection and clock feedthrough can be neglected.

Effect on output reference

In Fig. 3.15, even though the voltage change in node a due to charge injection and clock feed through is negligible, that of node b should be taken into the account. This is because, when SW_2 turns off charges due to charge injection and clock feedthrough are deposited onto node b, and this charges remain unchanged until SW_2 turns ON, resulting a noise current through M_3. This noise current generated in M_3 can be expressed as follows.

$$i_{n,M3} = g_{m,3}\big(\delta v_{cf,21} + \delta v_{ci,21}\big) \tag{3.37}$$

where, $g_{m,3}$ is the transconductance of M_3, $\delta v_{cf,21}$ and $\delta v_{ci,21}$ are the voltage changes in node b due to clock feedthrough and change injection when SW_2 turns off, respectively. The values for $\delta v_{cf,21}$ and $\delta v_{ci,21}$ can be expressed in the same manner as eqs. (3.31) and (3.34).

$$\delta v_{cf,21} = V_{DD} \cdot \left\{ \frac{c_{ovN}}{C_{2,1} + c_{ovN}} - \frac{c_{ovP}}{C_{2,1} + c_{ovP}} \right\} \tag{3.38}$$

$$\delta v_{ci,21} = \frac{C_{OX}}{2C_{2,1}} \left\{ W_N L_N \left(V_{DD} - v_{in,1} - V_{TH,N} \right) - W_P L_P \left(v_{in,1} - |V_{TH,P}| \right) \right\} \tag{3.39}$$

On the other hand, SCF_2 also suffers from the switch injection and clock feedthrough, resulting in a noise current through M_4. Then this noise current is mirrored into M_6. The resultant noise current flows through M_6 can be calculated in the same way as above,

$$i_{n,M6} = g_{m,6} \left(\delta v_{cf,22} + \delta v_{ci,22} \right) \tag{3.40}$$

where,

$$\delta v_{cf,22} = V_{DD} \cdot \left\{ \frac{c_{ovN}}{C_{2,2} + c_{ovN}} - \frac{c_{ovP}}{C_{2,2} + c_{ovP}} \right\} \tag{3.41}$$

$$\delta v_{ci,22} = \frac{C_{OX}}{2C_{2,2}} \left\{ W_N L_N \left(V_{DD} - v_{in,2} - V_{TH,N} \right) - W_P L_P \left(v_{in,2} - |V_{TH,P}| \right) \right\} \tag{3.42}$$

where gm_6 is the transconductances of M_6. Both the filters share the same clock in output stage ($SW_{4,1}$ and $SW_{4,2}$), and therefore the variation of M_3 and M_4 gate voltages due to charge injection are simultaneous. In other words, the resultant noise currents in M_3 and M_6 are also simultaneous, and thus work to cancel each other's effect. Thus, the change in voltage across R_2 due to charge injection and clock feedthrough of SCF_1 and SCF_2can be written as

$$\delta V_{REF,1} = R_2 \left(i_{n,M3} - i_{n,M6} \right) \tag{3.43}$$

In practice, it is difficult to choose the values for $C_{2,1}$ and $C_{2,2}$, such that $\delta V_{REF,1}$ becomes zero in all range of temperature, because $v_{in,1}$ and $v_{in,2}$ are non-linear values. However, smaller $\delta V_{REF,1}$ can be achieved by choosing a higher value for $C_{2,1}$,$C_{2,2}$. But this lends to larger time constant, given by eq. (3.14), and occupies more design area.

Furthermore, as it is clear from Fig. 3.2, the voltage on capacitor C_3 is also sensitive to clock feedthrough and charge injection, and thus should be considered. The voltage changes on C_3 (changes on M_3 gate voltage) causes changes in I_0. Assume that the current change in I_0 due to clock feedthrough and charge injection is ΔI_0. Thus, by using eqs. (3.6) and (3.8), we can rewrite the currents flow through R_1 when SW_1 is OFF as follows

$$I_{1,error} = \frac{V_{BE1}}{R_1} = V_T \left\{ \ln \frac{(n+1)(I_0 + \Delta I_0)}{I_s} \right\} \frac{1}{R_1}, \tag{3.44}$$

and

$$I_{2,error} = \frac{V_{BE2}}{R_1} = V_T \left\{ \ln \frac{(I_0 + \Delta I_0)}{I_S} \right\} \frac{1}{R_1} \tag{3.45}$$

Since both the switched capacitor filters SCF_1 and SCF_2 sense the gate voltage of M_1 when SW_1 is OFF, the currents given in eqs. (3.44) and (3.45) are copied and mirrored into the output stage.

Hence, the output reference voltage that suffers from the clock feedthrough and charge injection on C_3 can be given by

$$V_{REF} = \frac{R_2}{mR_1} V_T \left\{ (\alpha + \beta) \ln \frac{(n+1)(I_0 + \Delta I_0)}{I_S} - \beta \ln \frac{(I_0 + \Delta I_0)}{I_S} \right\} \tag{3.46}$$

From eq. (3.46), it can be calculated that 5% change in I_0 results in only 0.10% change in output reference. Therefore, sensitivity of M_2 gate voltage to clock feedthrough charge injection can be neglected.

In the proposed design, values of $C_{2,1}$= 575 fF and $C_{2,2}$= 500 fF are chosen such that the worst case variation of V_{REF} between two phases become approximately 300 μV. Value of C_1 was set to 425 fF. In the case of applications such as pipeline AD converters, which use sampled reference, a continuous reference is not required; thus, smaller $C_{2,1}$,$C_{2,2}$ can be used, resulting to more design area reduction.

3.5 Simulation results

The proposed area-efficient bandgap reference was designed in a $0.25\mu m$ CMOS process, and following simulations were done to verify the performances.

- Temperature sweep.
  - Operational amplifier
  - The supply independent current source.
  - Switched capacitor filter.
  - The full bandgap reference.
- Stability analysis.
- Power supply sweep.
- Transient sweep.

3.5.1 Temperature sweep

Operational amplifier

The operational amplifier is simulated using the circuitry shown in Fig. 3.16. In this simulation test bench, the operational amplifier is biased by using the supply independent current source, in which SW_1 is set to ON. This method allows us to investigate the various operating possibilities of amplifier in different temperature conditions and various supply voltages. This is because, in the actual design the operational amplifier is biased by the supply independent current source, and the output current of the supply independent current source is temperature dependent. Furthermore, the the base-emitter voltage of Q_1, which correspond to common mode input voltage of the operational amplifier, is also temperature dependent.

Figure 3.17 represents the simulation results of the open-loop transfer function in different temperatures, and various supply voltages. In the proposed design, the inputs of the operational amplifier are forced to virtual ground. This requires a high open loop differential gain. As can be

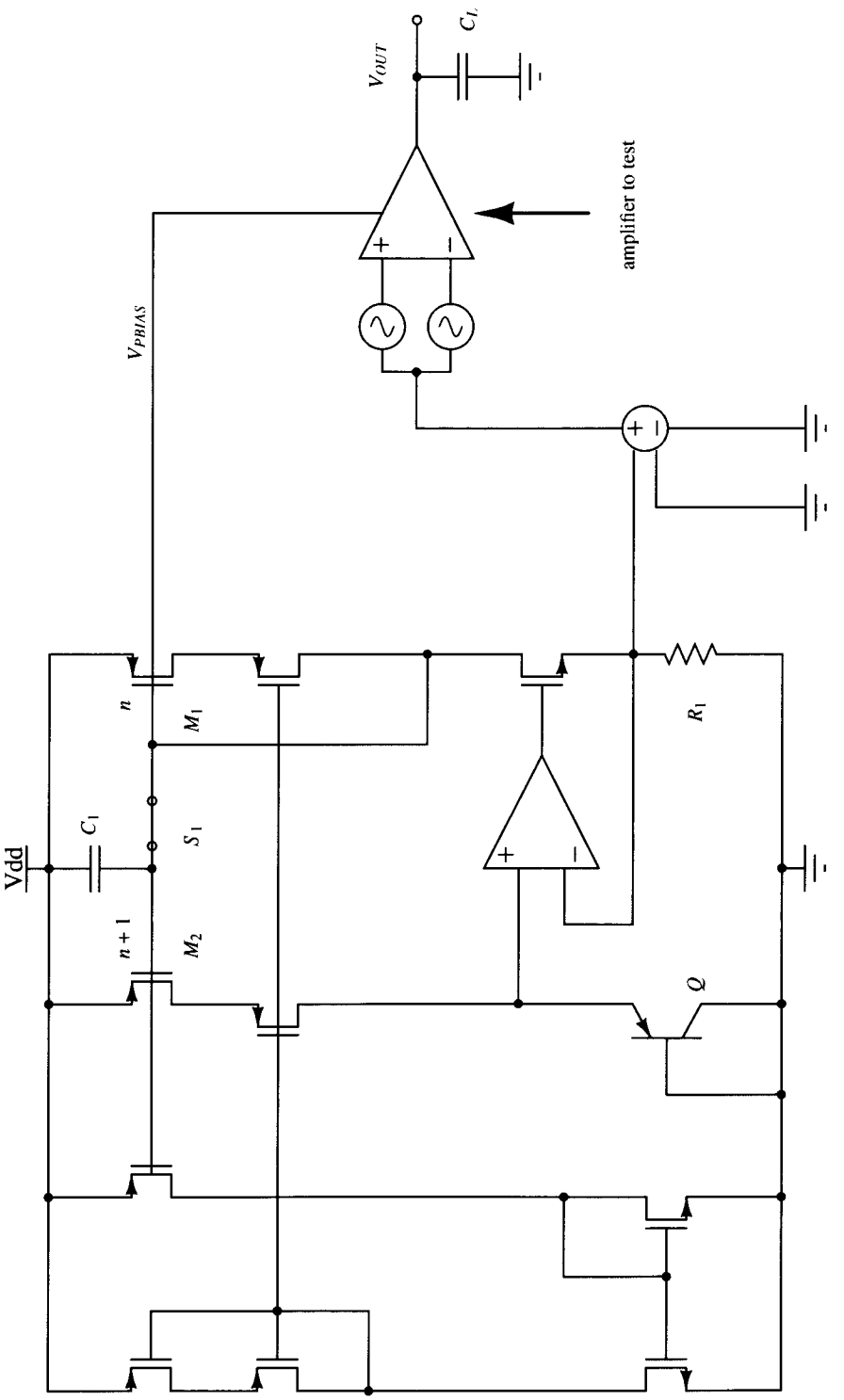


Figure 3.16: Simulation test bench of the open-loop transfer function

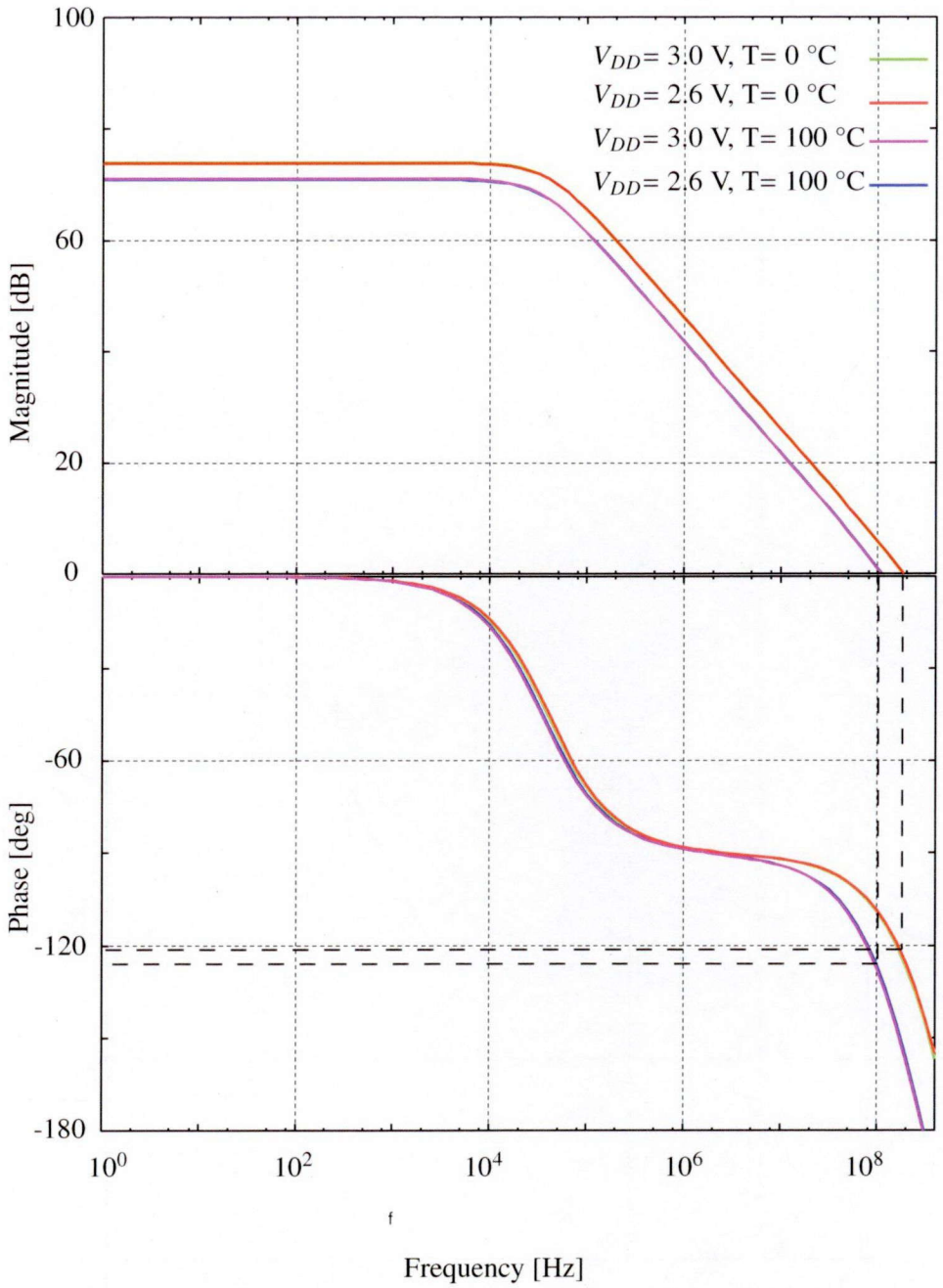


Figure 3.17: Magnitude and phase of the open-loop transfer function

seen in Fig. 3.17, the open loop differential gain is over 70 dB, and remains stable for all operating conditions. Because of the operational amplifier is biased by using supply independent current source, the open loop differential gain and the bandwidth remain constant for supply voltage variations. However, the differential gain drops by approximately 3 dB, and the bandwidth is reduced approximately by 100 MHz, when temperature change from 0 °C to 100 °C.

From Fig. 3.17, the worst case phase margin can be calculated as

$$PM = 180° - 120° = 60° \tag{3.47}$$

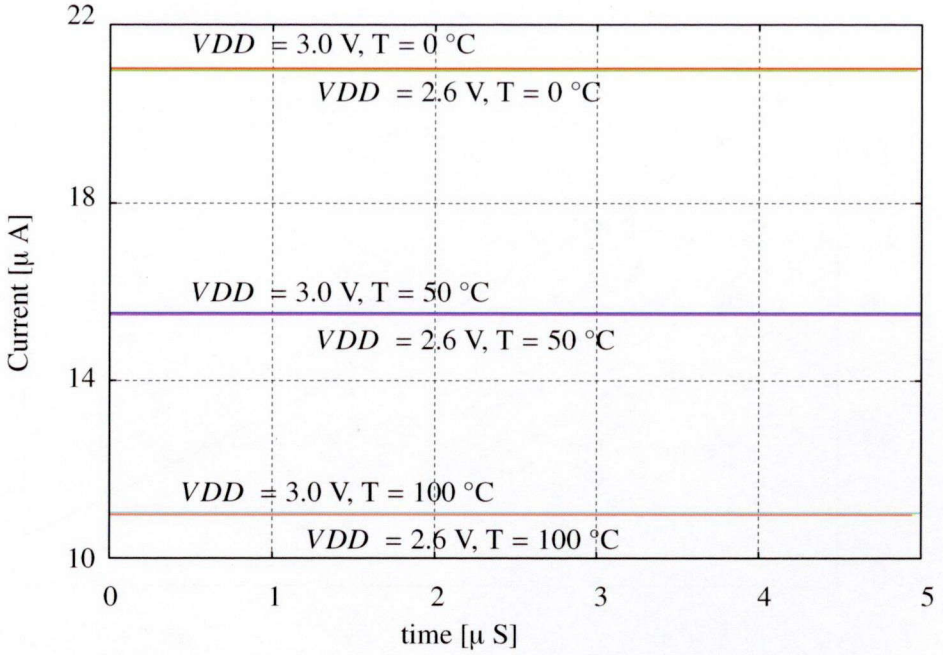


Figure 3.18: Output current of supply independent current source in different temperature

when temperature is 100°C. Thus, it can be said that the system is stable in all the operation conditions. Except this small-signal AC simulations, the stability of the proposed design is examined by using large signal time-domain simulation (applying a step function to V_{DD}), and will be discussed in latter section.

Supply independent current source

The simulated output current of the supply independent current source in different temperatures and the temperature dependence are shown in Fig. 3.18 and 3.19, respectively. From above results. it can be said that the supply independent current source is stable in temperature range from 0°C to 100°C, and the temperature coefficient of the output current is approximately -0.1 μA/°C.

Figure 3.20 represents the simulated results of the base emitter voltages of Q_1, V_{BE1} and V_{BE2}. Proving the discussion in previous section, the temperature coefficients of both V_{BE1} and V_{BE2} are negative, and can be calculated as

$$\frac{\partial V_{BE1}}{\partial T} = \frac{598.3\text{ mV} - 784.6\text{ mV}}{100°\text{C}} = -1.86\text{ mV/°C}, \tag{3.48}$$

and

$$\frac{\partial V_{BE2}}{\partial T} = \frac{490.9\text{ mV} - 702.1\text{ mV}}{100°\text{C}} = -2.11\text{ mV/°C}, \tag{3.49}$$

respectively. Note that, for simplicity, we ignore the second order effects. Thus, selecting the constants α and β in eq. (3.13), such that $(\alpha+\beta) : \alpha = 2.11 : 1.86$, the following condition can be satisfied.

$$(\alpha+\beta)\frac{\partial V_{BE1}}{\partial T} - \beta\frac{\partial V_{BE2}}{\partial T} = 0 \tag{3.50}$$

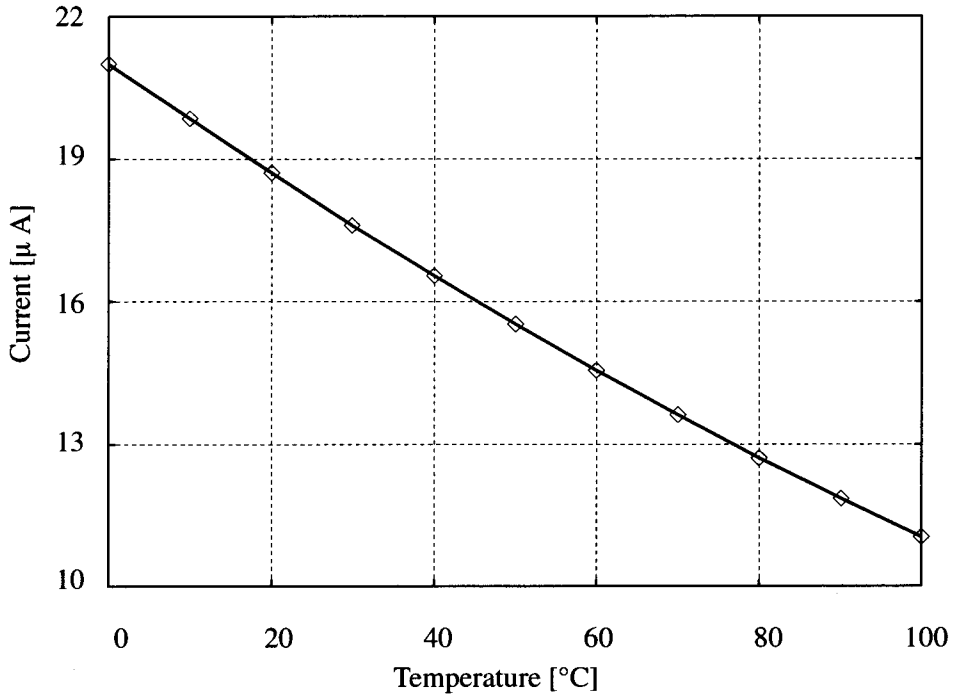


Figure 3.19: Temperature dependence of current source

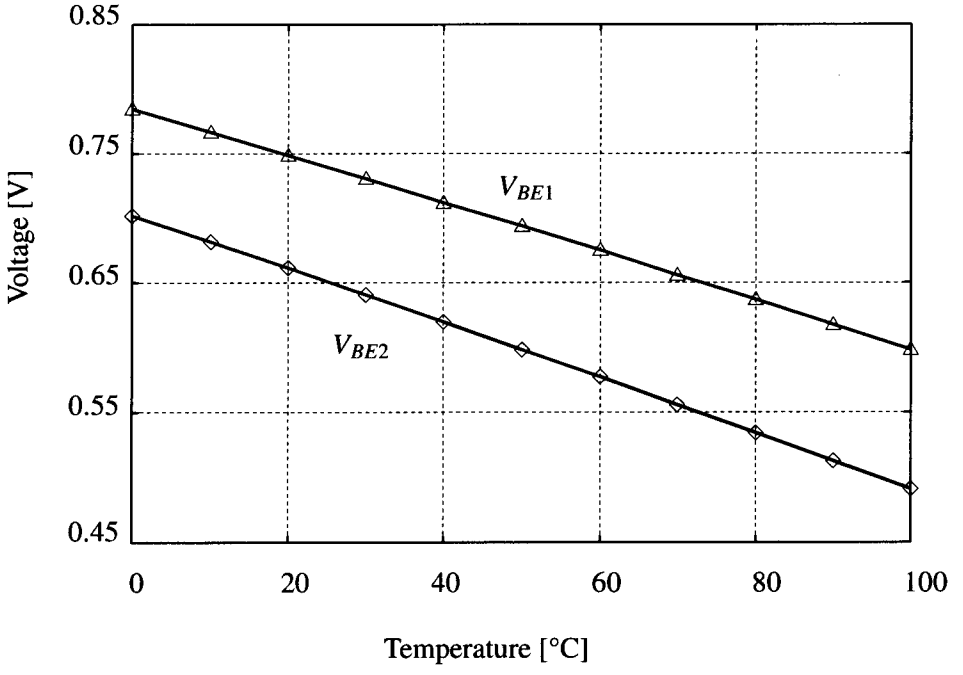


Figure 3.20: Temperature dependence of of V_{BE1} and V_{BE2}

Figure 3.21 shows the numerical calculation results of $(2.11/1.86)V_{BE1} - V_{BE2}$. The results prove that the temperature dependence of the resultant voltage is negligibly small. Thus, in the

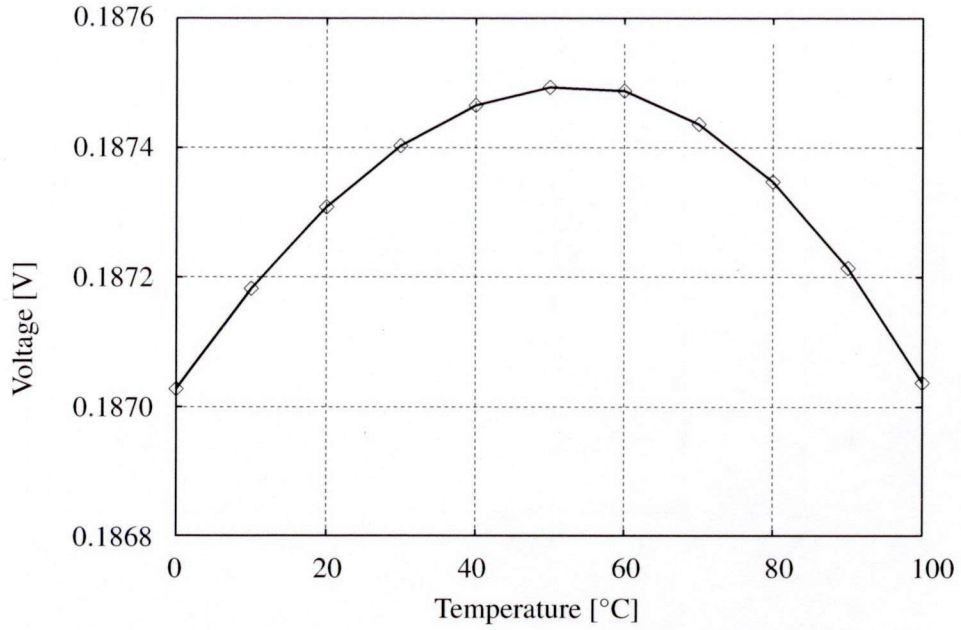


Figure 3.21: Numerical calculation results of $(2.11/1.86)V_{BE1} - V_{BE2}$

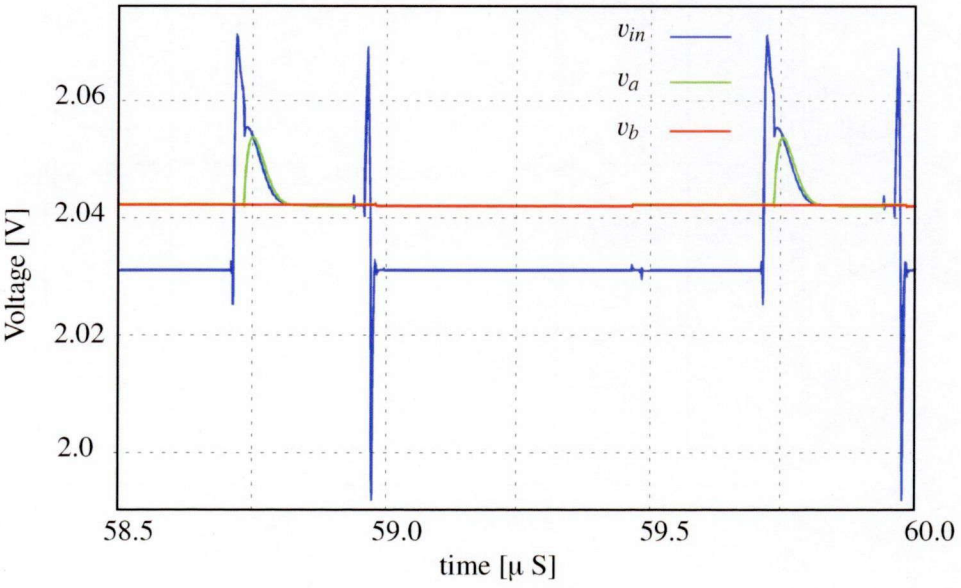


Figure 3.22: Node voltages of SCF_1

proposed design, the aspect ratio of $M_3 : M_6$, which is correspond to current mirror ratio $(\alpha+\beta) : \alpha$, is selected to approximately 33 : 29.

Switched capacitor filters

The switched capacitor filters are simulated in different temperatures and supply voltages, to verify the operations and to study the effects of charge injection and clock feed through. The maximum

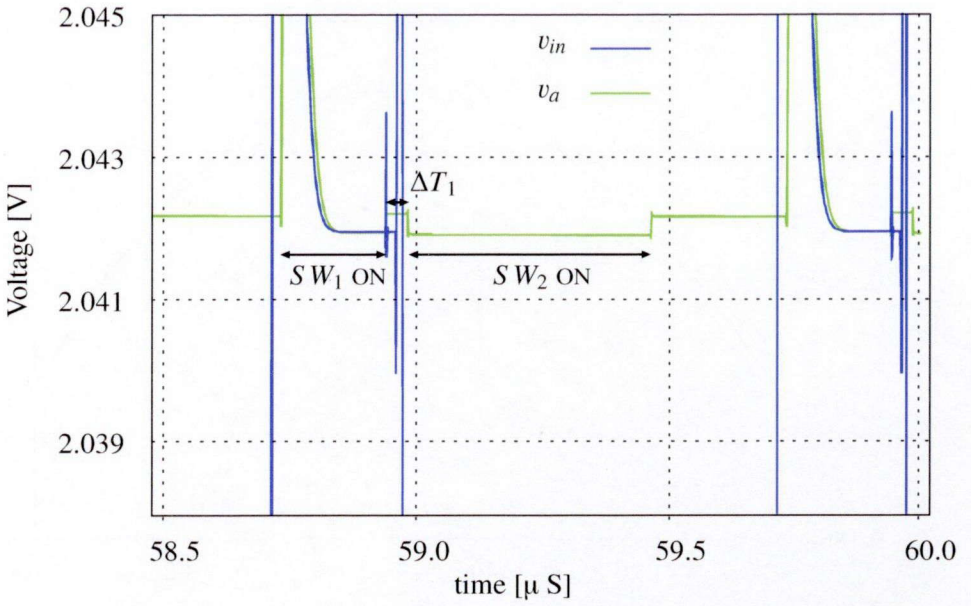


Figure 3.23: Voltage change in node a due to switch feedthrough

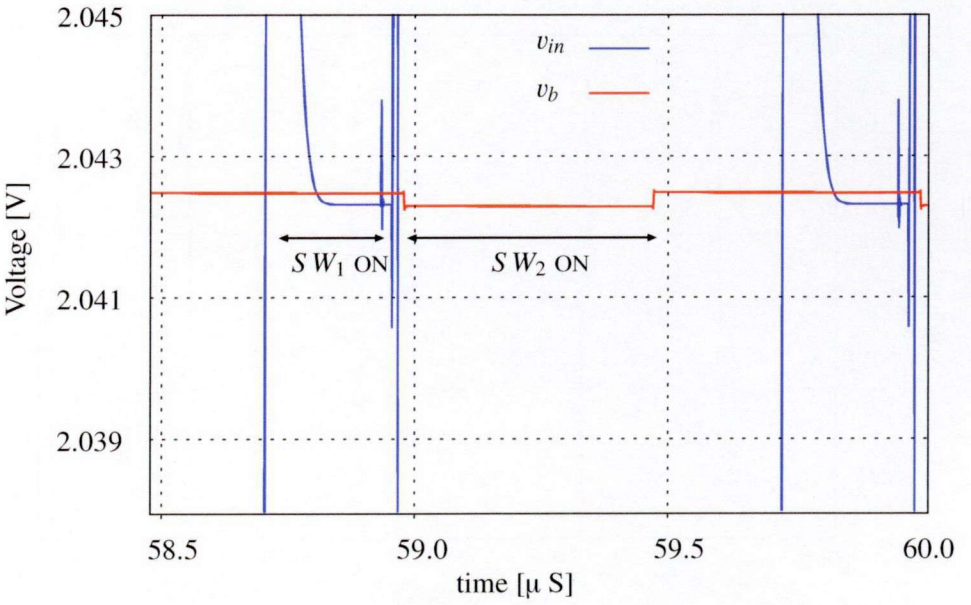


Figure 3.24: Voltage change in node b due to switch feedthrough

variation in V_{REF} due to clock feedthrough and charge injection is observed when V_{DD} = 3.0 V and T = 0 °C. Figure 3.22 shows the simulated node voltages of switched capacitor filter SCF_1, in V_{DD}= 3.0 V and T= 0 °C. The enlarged views of voltage waveforms of node a and node b are represented in Figs. 3.23 and 3.24, respectively. From Fig. 3.23, when SW_1 is ON, the capacitor C_1 is charged to v_{in}, thus the voltage of node a becomes equal to v_{in}. However, after SW_1 turns OFF, a change can be seen in the voltage of node a (during ΔT_1). Then, after SW_2 turns ON, the voltage becomes almost the same as the previous v_{in}, proving the analysis conducted in the previous section.

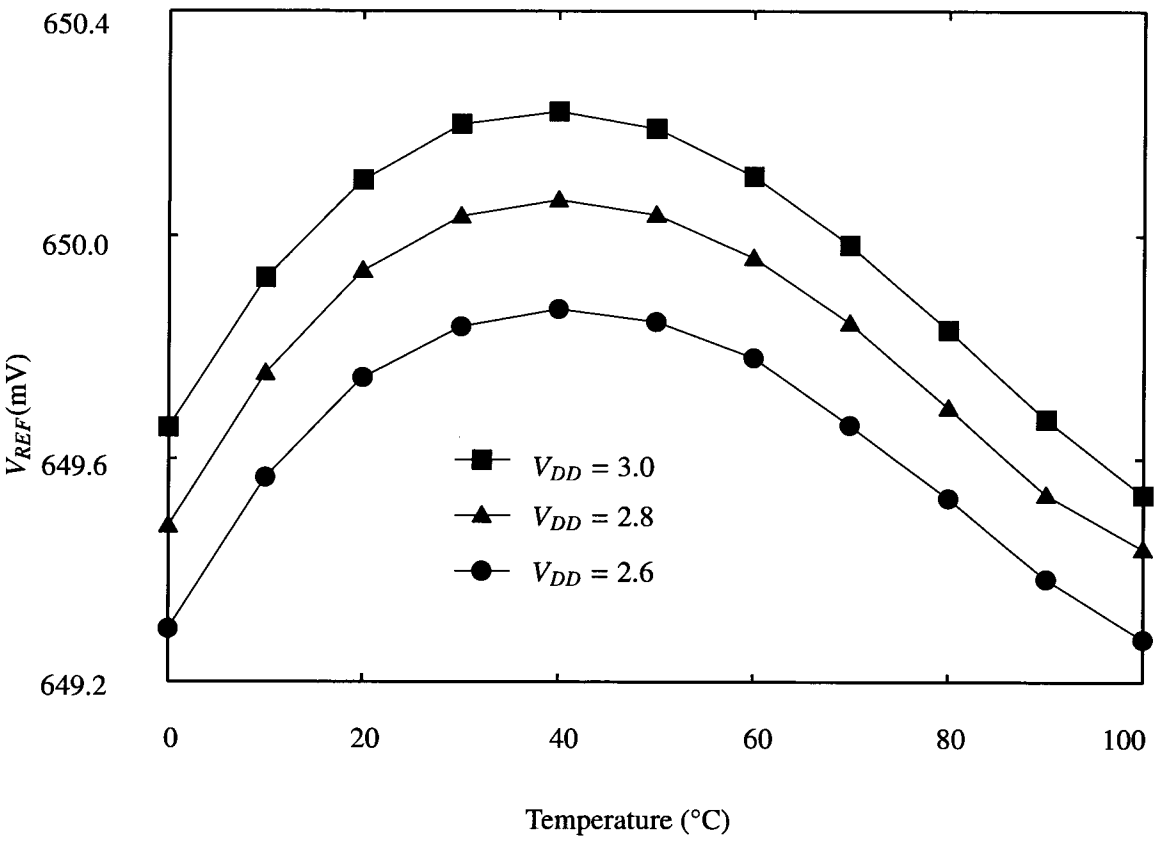


Figure 3.25: Temperature and power supply dependence of reference voltage

Thus, during this phase, as it can be seen in Fig. 3.24, capacitor C_2 is charged into v_{in}. But, after SW_2 turns OFF, the voltage of the node b is changed by $(\delta v_{cf,21} + \delta v_{ci,21})$, which is approximately 217μV. This voltage change causes error current of $g_{m,3}(\delta v_{cf,21} + \delta v_{ci,21})$ to flows through R_2.

Full reference

Considering the matching properties, R_1 and R_2 are implemented by 12 kΩ unit resistors. The resisters values of R_1, R_2 was set to 48 kΩ and 168 kΩ, respectively, such that the output reference voltage becomes 650 mV at room temperature. Figure 3.25 shows simulation results of the output reference voltage (V_{REF}) as a function of temperature for different supply voltages. With a 2.8 V supply voltage, the proposed circuit produces a output voltage of 650 mV at room temperature. With the 2.8V supply voltage (standard supply voltage for the proposed design), the maximum variation of the output voltage over the temperature range of 0 °C to 100 °C is 0.6 mV (650.0 mV at 50 °C-649.4 mV at 100 °C). Thus the temperature coefficient of the output voltage with 2.8 V constant power supply is

$$TC_{VDC=2.8V} = \frac{1}{650\text{ mV}} \cdot \frac{650.0\text{ mV} - 649.4\text{ mV}}{100°\text{C}} \times 10^6 = 9.23\text{ ppm/°C} \quad (3.51)$$

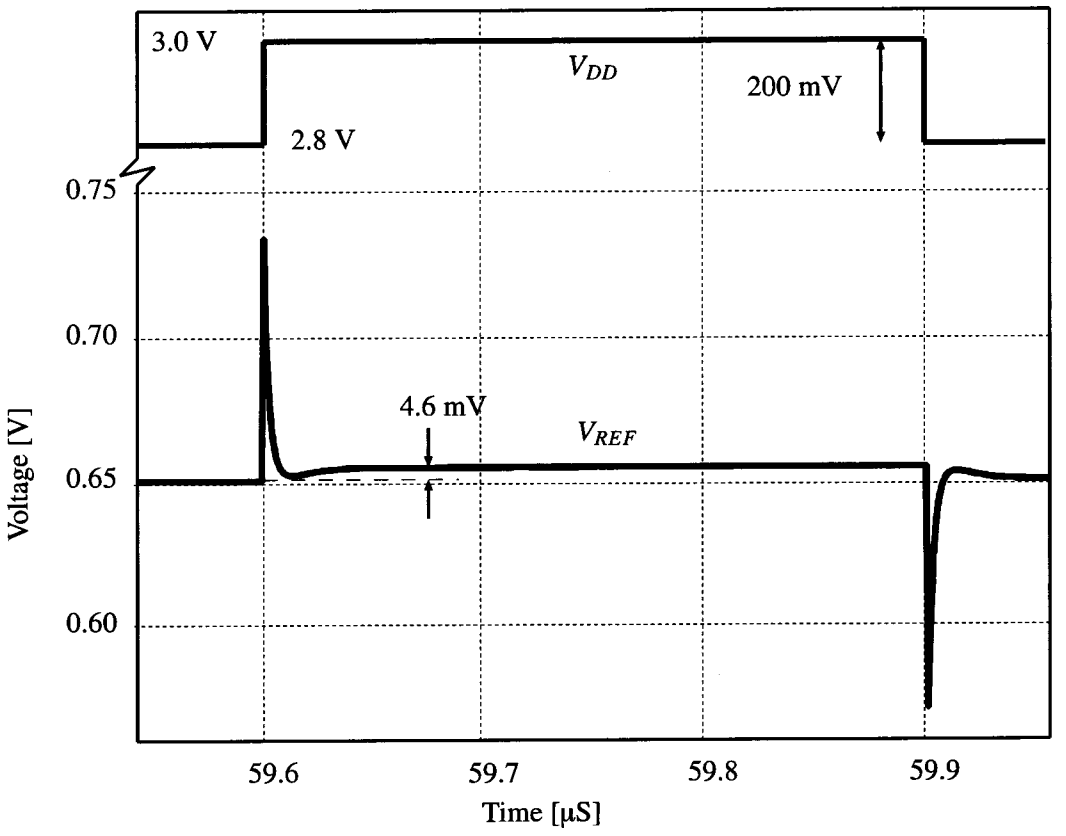


Figure 3.26: Transient response of output voltage when step is applied to supply voltage

The worst case deviation of the output in above temperate range is approximately 0.7 mV (650.2 mV at 50 °C- 649.5 mV at 100 °C), when 3.0 V supply voltage is applied. Thus the worst case temperature coefficient can be given by

$$TC = \frac{1}{650\text{ mV}} \cdot \frac{650.2\text{ mV} - 649.5\text{ mV}}{100°\text{C}} \times 10^6$$
$$= 10.7\text{ ppm/°C} \tag{3.52}$$

3.5.2 Stability verification

To check the stability of the proposed bandgap reference, a small step voltage is applied to the supply voltage and the change in output voltage is examined. Figure 3.26 shows the simulated transient response of the output when 200 mV pulse voltage is applied to supply voltage.

In simulation results, an overshoot and undershoot can be observed in output voltage, when the supply voltage change from 2.8 V to 3.0 V and from 3.0 V to 2.8 V, respectively. However, the output has stabilized with a first order behavior. This observed difference is less than 5 mV, which is approximately ±0.77% of the final output. This can be explained by the fact that the sudden change in power supply voltage, first arrive to output M_4, directly. Then, arrive via $M_4 - > M_5 - > M_6$, with some delay. Thus, an overshoot or an undershoot can be seen in the beginning, but stabilized quickly.

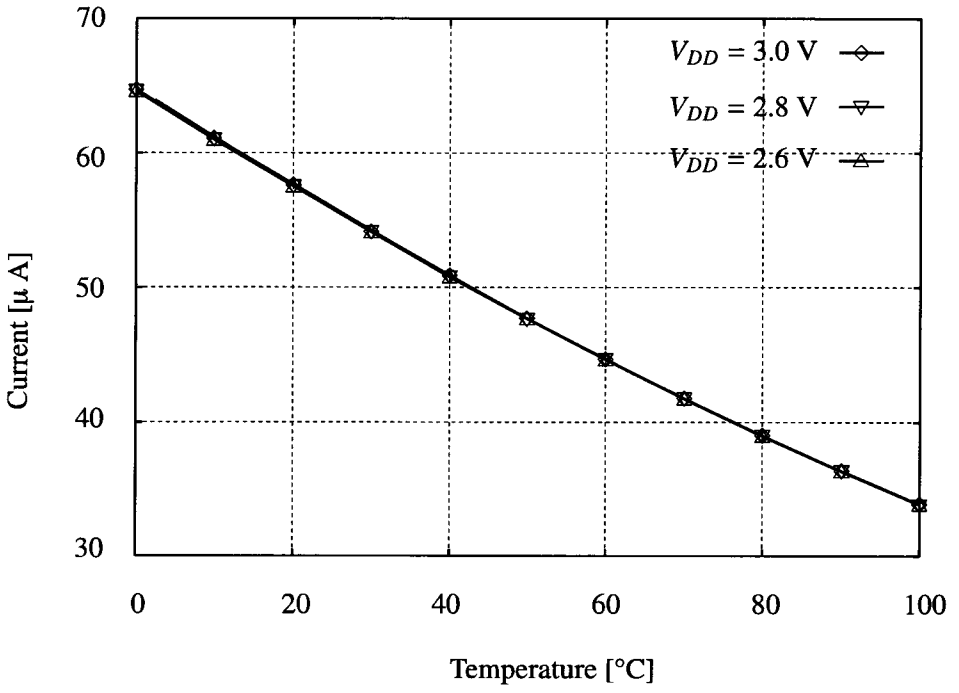


Figure 3.27: Power consumption

3.5.3 Power Supply variation and transient response

From Fig. 3.25, the worst-case deviation in V_{REF} due to power supply variation can be seen at T = 50 °C. Thus the worst-case DC power supply rejection ratio can be calculated as

$$PSRR_{worst} = 20\log\left(\frac{V_{REF,VDD=2.8} - V_{REF,VDD=2.6}}{200\text{ mV}}\right)$$
$$= 20\log\left(\frac{650.0\text{ mV} - 649.8\text{ mV}}{200\text{ mV}}\right) \approx \text{-60 dB} \quad (3.53)$$

Figure 3.27 compiles the simulated results of supply current as a function of temperature for different supply voltages. The current consumption is constant for different supply voltages, and decreases with increase in the temperature. One of the reasons for this is that the power supply independent current source has negative temperature coefficient, resulting in the decrease in bias currents of bias generator and operational amplifier, with increasing the temperature. Another reason is, as discussed previously, the base emitter voltage of parasitic bipolar transistor,V_{BE}, and the resistor R_1 exhibits negative and positive temperature coefficients, respectively. Thus, the current flows through R_1, which is given by V_{BE}/R_1, is reduced in proportion to temperature, and therefore, the drain currents of M_3 and M_4 (in Fig. 3.2) are also reduced in proportion to temperature.

From the results in Fig. 3.27, it can be shown that the reference circuit consumed an average of 49.5 μA in the temperature range from 0 °C to 100 °C, while consuming the maximum of 65.5 μA at 0 °C.

Transient response of the proposed circuit is shown in Fig. 3.28. The settling time is approximately 20 μs. Temperature and supply dependence of settling time can be neglected. Enlarged view of selected area in Fig. 3.28 is seen in Fig. 3.29. The worst case of V_{REF} difference between two phases is 320 μV at 0 °C and V_{DD} =3.0 V.

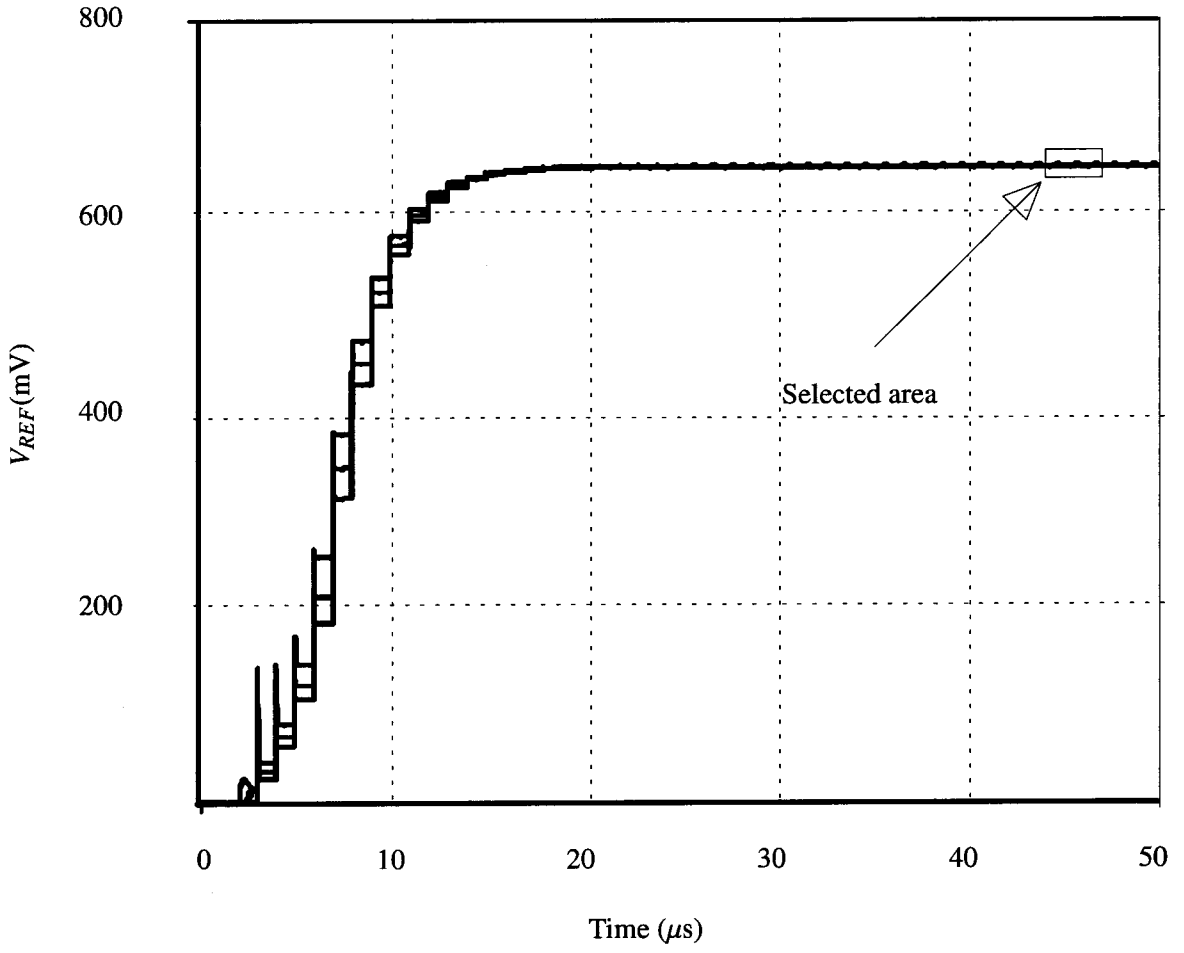


Figure 3.28: Transient response of the proposed circuit

3.6 Layout

The performances of analog circuits are highly sensitive to the matching of devices, such as resistors, capacitors and specially the MOS devices used in current mirrors. By using a advance layout techniques (such as common centroid), the effects of process variation and linear gradients can be effectively minimized, and therefore, the circuit performance can be improved.

As discussed in Sec.3.4, the accuracy of current mirror ratio and matching of resistor ratio play an important role in the proposed circuit. Thus, special attention need to be paid to the following points:

- The current mirrors used in current source and current switch circuits, and in the output stage are placed close together, respectively. Additionally, common centroid layout and dummy elements are used.

- To reduce the error on resistor ratio R_2/R_1 by corners and differing perimeters, both resistors R_1 and R_2 are implemented by 12 kΩ unit resistors. Next, common centroid layout is used to improve the matching between R_1 and R_2. Furthermore, dummy elements are placed in

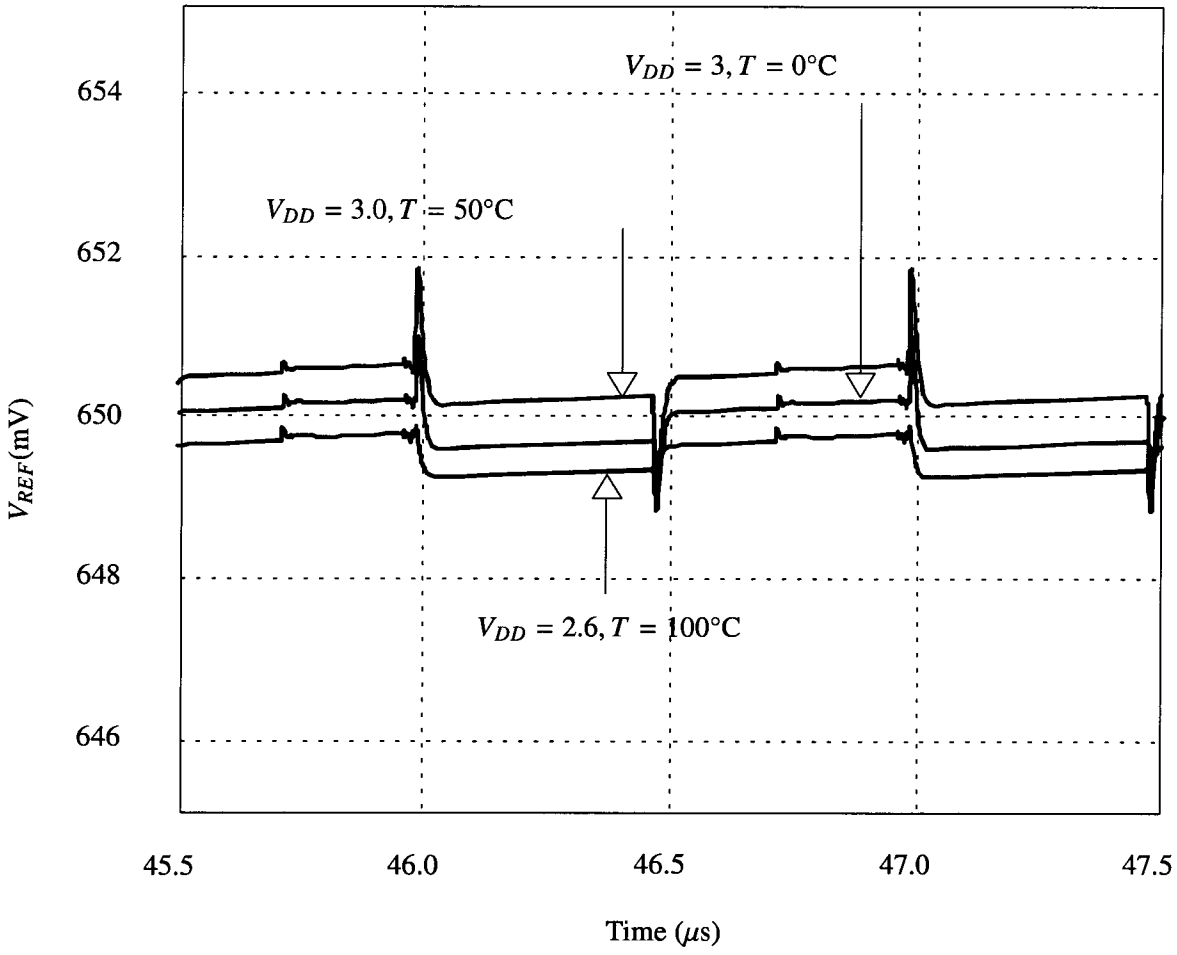


Figure 3.29: Enlarged view of selected area in Fig. 3.28

both sides of the common centroid resistor array to reduce the effects of differing dopant concentrations at differing points on the surface.

- In the operational amplifier layout, matching-sensitive pMOS differential pair are laid out with common centroid technique, and dummy elements are also used.
- The capacitor ratios $C_{2,X}/C_1$ determine the settling time of the proposed bandgap reference. Furthermore, the difference of V_{REF} between two phases mostly depends on matching of $C_{2,1}$ $C_{2,2}$. Thus, the matching of $C_{2,X}$ and C_1 should be considered. To improve the matching, $C_{2,X}$ and C_1 are implemented by 25 fF unit capacitors. Next, common centroid technique and dummy cells are used.

Figure 3.30 displays the layout of the proposed design and the layout size is 0.011 mm^2 (110 μ m $\times$ 100 μ m).

3.7 Comparison

Table 3.1 summarizes the performance of the proposed bandgap reference.

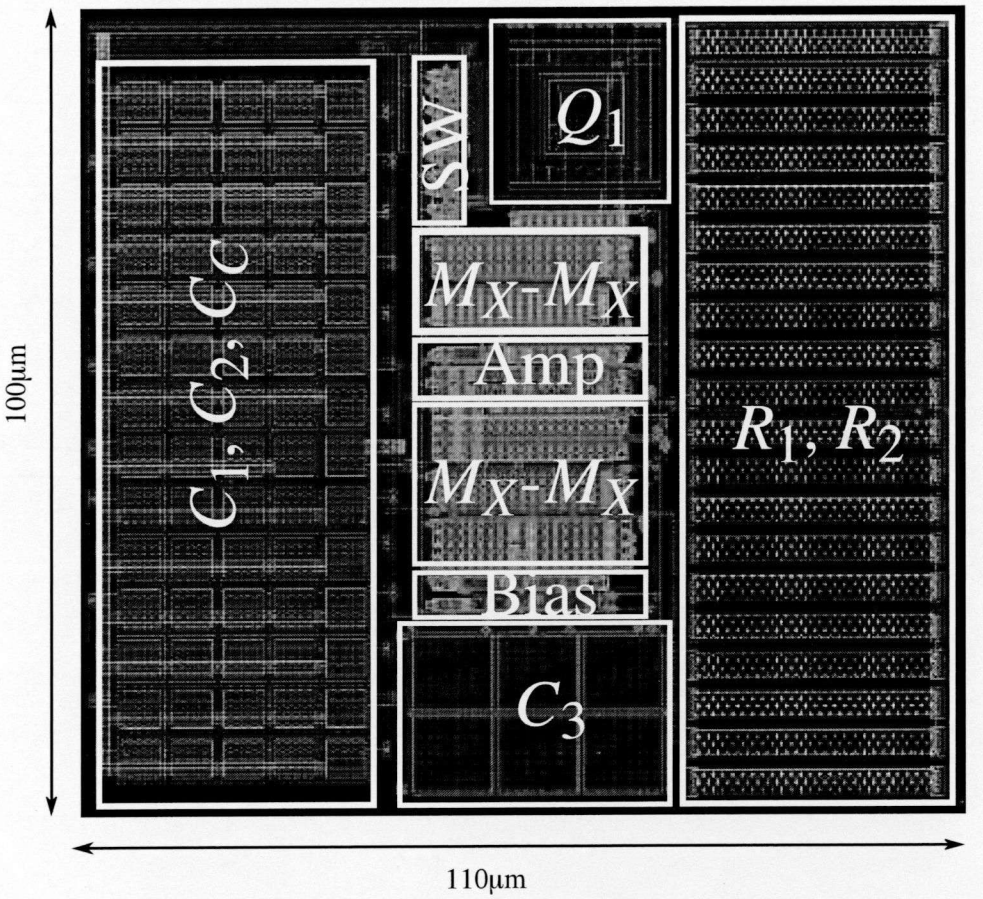


Figure 3.30: Layout of the proposed bandgap reference

Table 3.2 compares the performance of the bandgap reference described in this chapter to that of previously published CMOS bandgap references. The bandgap reference proposed in this thesis shows best performance in terms of chip area and temperature coefficient. Therefore it is ideal for low-cost application. Moreover, the proposed circuit shows very good performance in PSRR. Although [12] demonstrates better PSRR, the design proposed in this chapter occupies significantly smaller chip area. The power consumption of the proposed design is comparably high compared to [5, 21, 22].

3.8 Summary

In this chapter, we presented the design issues and accuracy analysis of novel area-efficient bandgap reference which is utilized by switched-current and current-memory techniques. Conventional bandgap reference circuits are utilized by array of bipolar transistors, thus the layout becomes a critical problem. However, the proposed circuit uses only one bipolar transistor so that the significant area reduction can be achieved. The proposed circuit is designed and simulated and layout design is carried out in 0.25 μm CMOS process. The simulation results show that the output reference voltage V_{REF} is 650 mV, and the temperature coefficient of V_{REF} is smaller than 10.7 ppm/°C for the temperature form 0 °C to 100 °C. The design area is less than 110 μm × 100 μm and consumes

Table 3.1: Performance summary

Technology	0.25μm CMOS
Area	0.011mm^2 (110μm x 100μm)
Supply Voltage	2.8 V
V_{REF}	650 mV
TC of V_{REF}	<10.7 ppm/°C (0 °C to 100 °C)
Average current consume	49.5 μA
SW_1 Switching Frequency	1 MHz
PSRR	-61dB (DC)
	-53dB @ 100Hz
	-51dB @ 1kHz
	-39.4dB @ 10kHz

average supply current of 49.5 μA.

Table 3.2: Comparison to previously published CMOS bandgap references

	V_{REF} (V)	TC (ppm/°C)	Design Area(mm^2)	PSRR (dB)@ (kHz)	Power(μW)	Process μm-CMOS
This	0.650	10.7	0.011	-51 @1	138.6	0.25
[5]	0.518	200	0.1	-20 @1	5	0.4 Flash
[12]	0.858	12.4	1.2	-68 @0.1	162	0.35
[21]	1.2	38.3	0.043	-58 @0.1	24.5	0.35
[23]	1.12	127	0.4	-45 @0.01	1400	0.5 digital
[22]	0.640	580	0.21	N.A.	74	0.35

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Chapter 4

Low-power bandgap reference

4.1 Introduction

The bandgap reference presented in previous chapter uses one bipolar transistor, switched current and current memory technique to produce reference voltage and have archived significant area reduction. It generates two current sources that have different temperature coefficients and subtracts one from other. Then feeds the subtracted current into a resistor to generate the reference voltage. Therefore, it is necessary to use continuous drain currents through the both output stage pMOS and nMOS transistors to generate the resistor output current. Only the difference of those drain currents is used to generate the reference voltage. Thus, in other point of view, the drain current of output stage nMOS transistor flows from VDD to GND uselessly. Practically, however, this drain current is much larger than the current flowing through the output resistor. Approximately, one fourth of the total supply current flows through the output stage nMOS transistor. Furthermore, additional power should be used to generate the bias voltages of output stage nMOS devices. Thus, significant power reduction can be achieved by removing the output stage nMOS devices. Moreover, in this current subtraction method, relatively larger pMOS and nMOS devices should be used at the output stage even to generate a small resistor current, resulting additional design area. Thus, replacing the resistor current generation method from current subtraction to current addition, let us implement smaller devices in the output stage, resulting a reduction of design area.

In this chapter we propose a new circuit technique that allows generating the reference voltage by using only one parasitic bipolar transistor, thus the area size becomes significantly smaller and bipolar device mismatch is eliminated. Also the proposed circuit outputs a fraction of the silicon bandgap voltage, which can be set to almost any value. The output is fairly insensitive to temperature and supply voltage variations and valid in both clock phases. Moreover, the proposed circuit is designed with built-in current sources, thus saving unnecessary power consumption. Section 4.2 describes the concept, operating principle, and the circuits. The design issues and accuracy analysis are discussed in Sect. 4.3, and the simulation results are presented in Sect. 4.4. Section 4.5 presents the layout issues, while Sec. 4.6 compares the performances of the voltage reference presented in this research with that of previously published voltage references. Finally Sect. 4.7 summarizes the research.

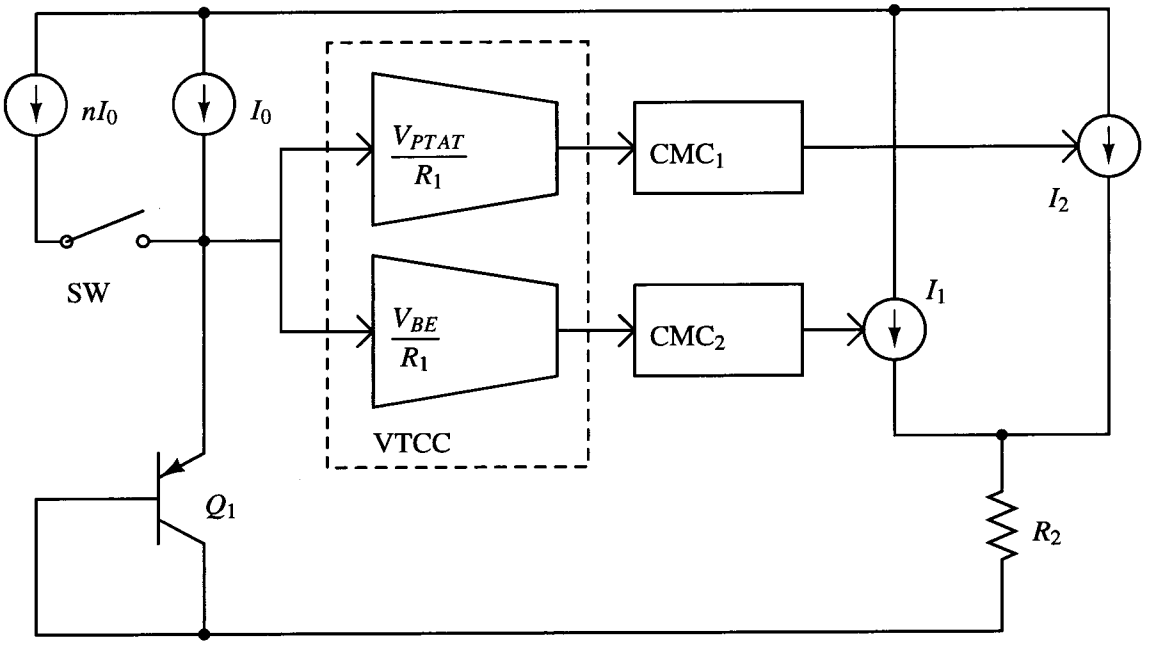

Figure 4.1: Conceptual diagram of the proposed low-power bandgap reference

4.2 Proposed low-power bandgap reference

4.2.1 Conception

The proposed bandgap reference is shown as a conceptual diagram in Fig.4.1. The proposed circuit consists of :

- Two supply independent current sources
- A parasitic bipolar transistor
- A Voltage-to-current converter (VTCC)
- Output stage resister

Switch *SW* controls the current injection into parasitic bipolar transistor (Q_1) and generates two different base-emitter voltages. When *SW* is OFF, current I_0 injects into Q_1 and base-emitter voltage becomes V_{BE1}. Next *SW* turns ON, current fed into Q_1 changes to $(n+1)I_0$ and base-emitter voltage becomes V_{BE2}. VTCC network and current memory cells (CMCs) used in the proposed circuit convert those V_{BE1} and V_{BE2} to currents given by V_{BE1}/R_1 and V_{BE2}/R_1, then also generate the current given by $(V_{BE2} - V_{BE1})/R_1$. ,where $1/R_1$ is the transconductance of the VTCC. The currents memorized at two CMCs, V_{BE1}/R_1 and $\Delta V_{BE}/R_1$, are mirrored with designed ratio α and β, respectively, summed, and fed into R_2. By selecting proper values for α and β, it is possible to generate temperature independent voltage. Note that this new architecture uses current addition method to generate resistor output current. Thus, compared to bandgap reference presented in previous chapter that uses current subtraction, significant power reduction can be achieved. Supply independent current sources, VTCC and CMC are described in next section.

4.2.2 Circuit operation

The schematic of the proposed low-power CMOS bandgap reference circuit is shown in Fig. 4.2, and Fig. 4.3 represents the timing diagram. The proposed circuit is composed of following main circuits:

- Supply independent current source
- Voltage to current converter (VTCC)
- Resistor output stage
- Startup circuit
- Bias generator
- Two switched capacitor filters (SCFs)

Supply independent current source

The supply independent current source used in the proposed design is shown in Fig. 4.4.

The circuit structure and the operating principle is same as the current source described in previous section. However, the location and the usage of the switch SW_1 is different, compared to the current source shown in Fig. 3.4(a). When SW_1 is ON, differential amplifier compares V_{BE} of Q_1 with the voltage across R_1 and regulates them to be equal. Therefore, the gate voltage of M_1 and M_2 is forced to flow supply independent currents through M_1 and M_2. Assuming that the aspect ratios of $M_1 : M_2$ is $m : 1$, and M_2 drain current (I_{M2}) is I_0, the base emitter voltage of Q_1 and the voltage across R_1 can be expressed as

$$V_{BE1} = \frac{kT}{q} \ln \frac{I_0}{I_S}, \tag{4.1}$$

and

$$V_{R1} = mI_0R_1, \tag{4.2}$$

respectively. Hence, $V_{BE1} = V_{R1}$, we can write the expression for I_0 as follows.

$$mI_0R_1 = \frac{kT}{q} \ln \frac{I_0}{I_S} \tag{4.3}$$

Figure 4.5 represents the plots of eqs. (4.1) and (4.2) for R_1 = 140 kΩ, T=300 K, I_S = 1.77 × 10^{-11} μA, and m = 15. As it is clear from Fig. 4.5, eq. (4.3) also has two roots, corresponding to the currents $I = I_{zero}$ and $I = I_{stable}$. Therefore, the proposed design also required a startup circuit so that to ensure $I = I_{stable}$ is achieved. The startup circuit will be discussed in latter section.

Thus, during this phase, M_1 drain current (I_{M1}) and therefore the current through R_1 (I_{R1}) can be expressed as follows,

$$I_{R1} = I_{M1} = \frac{V_{BE1}}{R_1} \tag{4.4}$$

The CMCs, which made up of SCFs (discussed later) and pMOS transistors, are used in the proposed circuit in order to archive continuous output. While SW_1 is ON, SCF_2 senses the gate voltage of M_1 and memorizes it in the gate node of M_5.

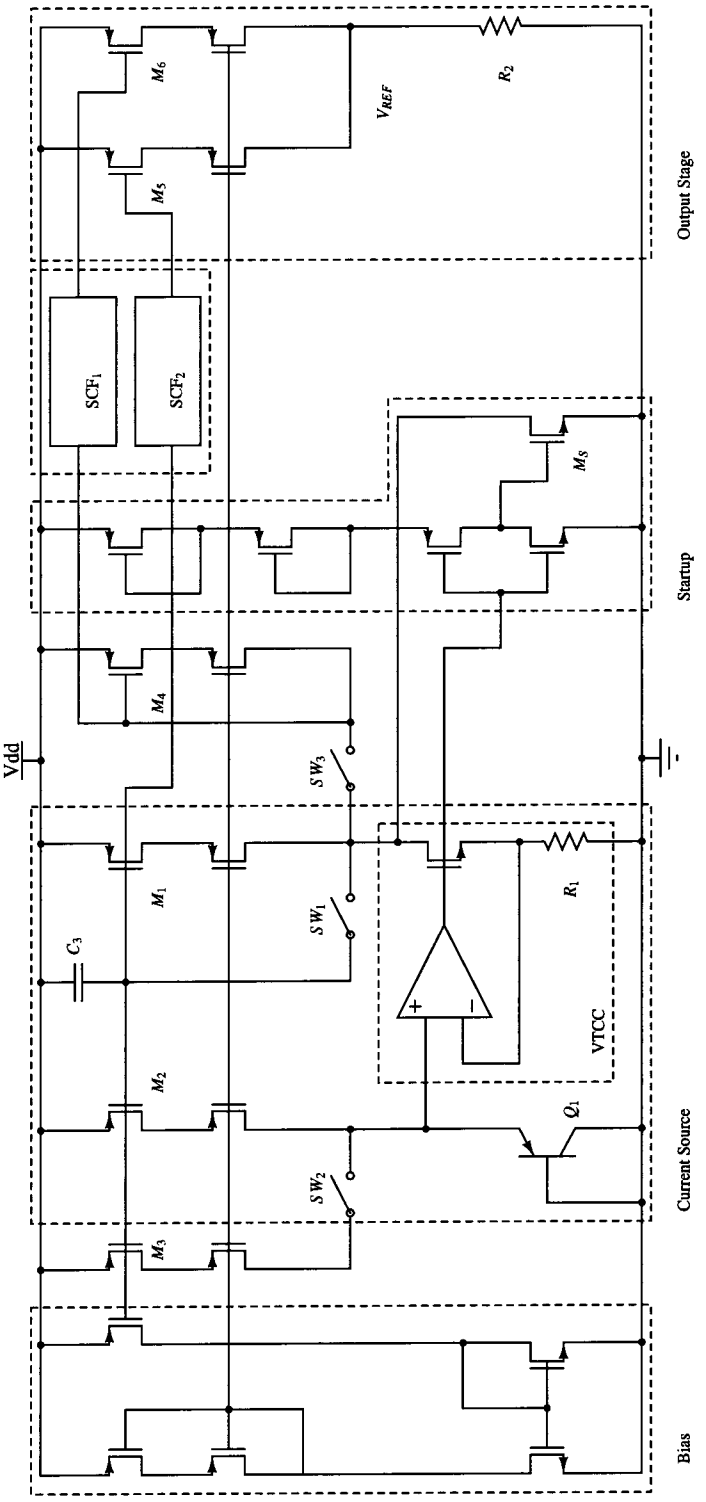

Figure 4.2: Proposed low-power CMOS bandgap reference

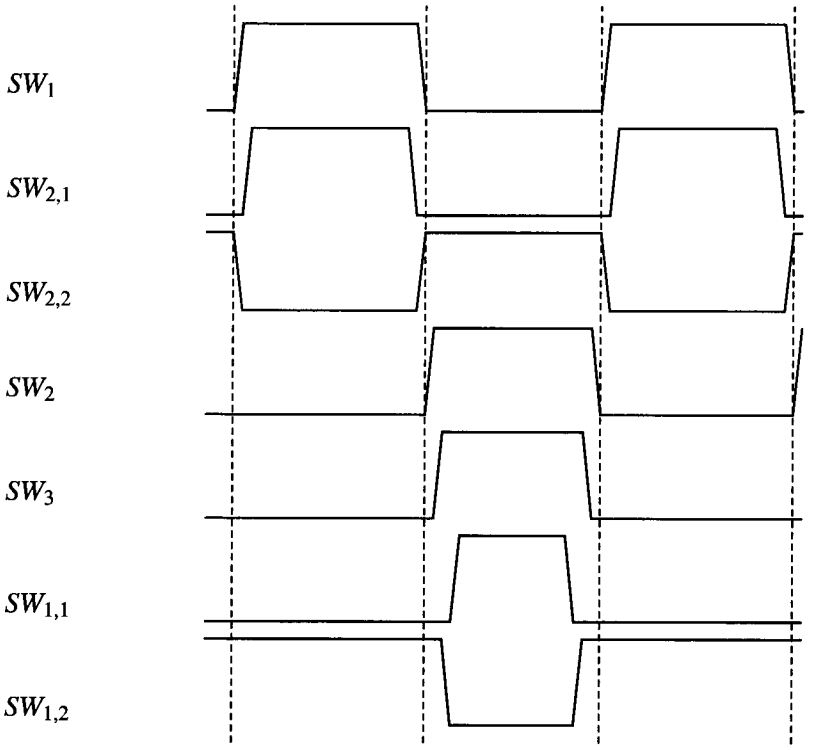

Figure 4.3: Timing diagram

Voltage to current converter

Next, in Fig. 4.2, SW_1 turns OFF and SW_2 turns ON. The capacitor, C_3, holds the gate voltage of M_1,M_2 and M_3 from the previous phase and keeps the same drain current through M_1 and M_2. During this phase, I_{M2} and M_3 drain current, I_{M3}, are summed and fed into Q_1. Assume that aspect ratio of M_2 : M_3 is 1 : n. Therefore, V_{BE} of Q_1 in present phase becomes

$$V_{BE2} = \frac{kT}{q} \ln \frac{(n+1)I_0}{I_S} \tag{4.5}$$

During this phase, SW_3 turns ON. The circuit status on this phase is shown in Fig. 4.6. Through negative feedback, operational amplifier places V_{BE2} across R_1. Therefore the current flows through R_1 can be written as

$$I_2 = \frac{V_{BE2}}{R_1} \tag{4.6}$$

This current is equals to the sum of I_{M1} and drain current of M_4, I_{M4}. Therefore I_{M4} can be given by

$$I_{M4} = I_2 - I_{M1} = \frac{V_{BE2}}{R_1} - \frac{V_{BE1}}{R_1} = \frac{\Delta V_{BE}}{R_1} \tag{4.7}$$

Next, when SW_3 is ON, SCF_1 senses the gate voltage of M_4 and memorizes in gate node of M_6.

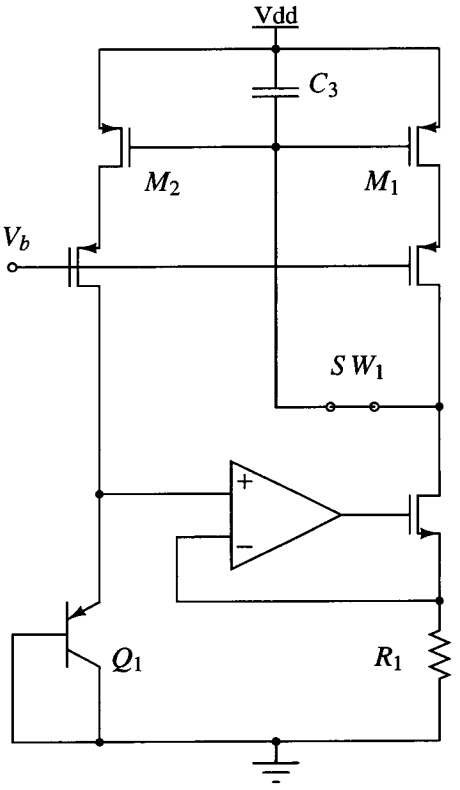

Figure 4.4: Supply independent current source

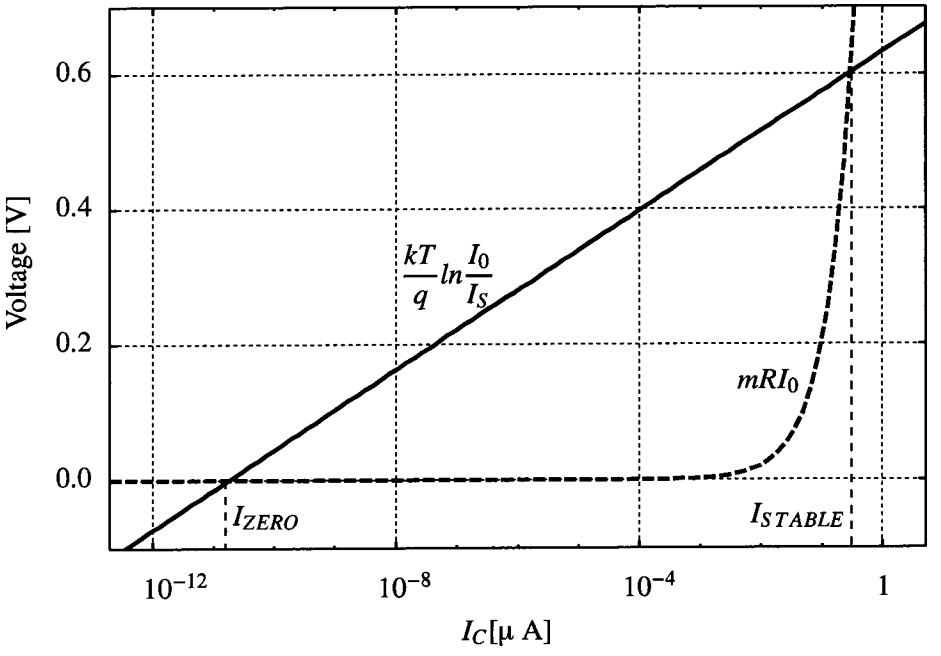

Figure 4.5: Output current of supply independent current source

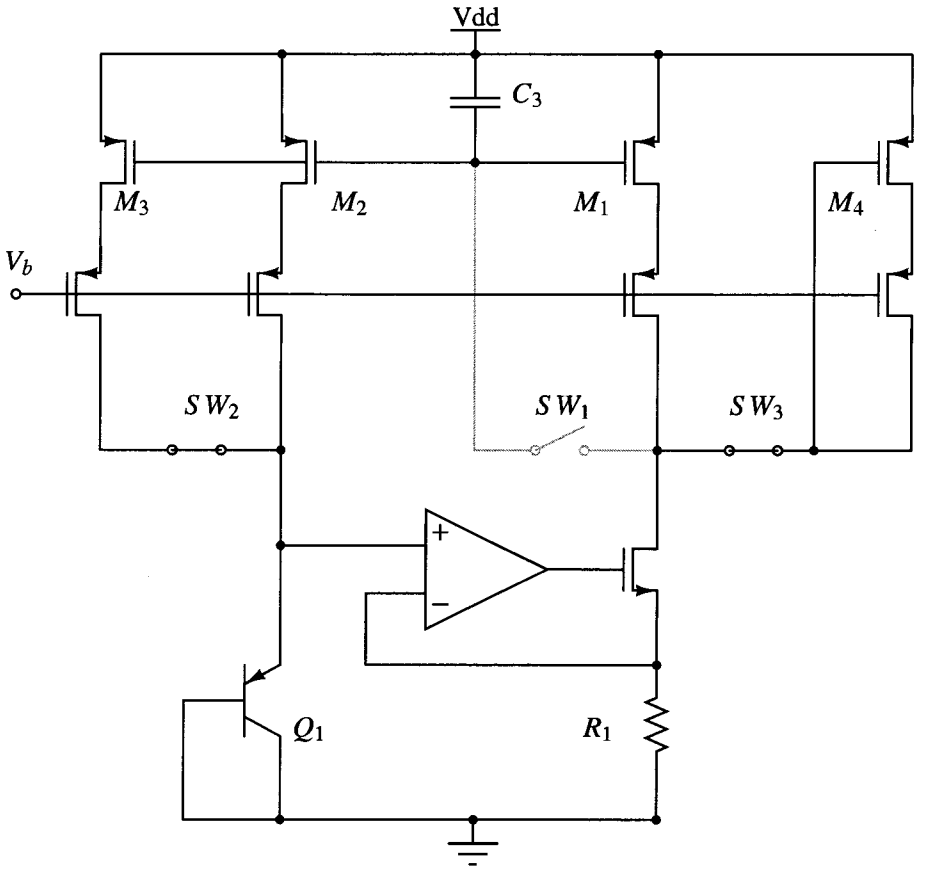

Figure 4.6: Voltage to current converter

Resistor output stage

Assuming that aspect ratio of $M_1 : M_5$ is $1 : \alpha$ and that of $M_4 : M_6$ is $1 : \beta$, continue drain currents of $M_5(I_5)$ and $M_6(I_6)$ can be expressed as

$$I_5 = \alpha \frac{V_{BE1}}{R_1}, \tag{4.8}$$

and

$$I_6 = \beta \frac{\Delta V_{BE}}{R_1}, \tag{4.9}$$

respectively. Thus the total current given by

$$\begin{aligned} I_{REF} &= I_5 + I_6 \\ &= \alpha \frac{V_{BE1}}{R_1} + \beta \frac{\Delta V_{BE}}{R_1} \end{aligned} \tag{4.10}$$

is injected into R_2. Therefore, the output voltage of the proposed bandgap reference can be expressed as

$$\begin{aligned} V_{REF} &= R_2 \times I_{REF} \\ &= \frac{R_2}{R_1}\{\alpha V_{BE1} + \beta V_T \ln(n+1)\} \end{aligned} \tag{4.11}$$

By selecting proper values for α, β and n such that

$$\alpha \frac{\partial V_{BE1}}{\partial T} + \beta \ln(n+1) \frac{\partial V_T}{\partial T} = 0, \tag{4.12}$$

reference voltage with zero TC can be obtain. Further more, by changing the value of R_2, V_{REF} can be set to any value between $(V_{DD} - 2V_{ODP})$ and GND, where V_{ODP} is the overdrive voltage of pMOS.

Startup circuit

As discussed previously, the supply independent current source has two stable states, corresponding to the currents given by I_{Zero} and I_{stable}. To ensure that the stable state is achieved, a startup circuit shown in Fig. 4.2 is used. The structure and the operating principle of the startup circuit used in this design is the same as the startup circuit used in the design, which is explained in previous chapter.

Bias generator

The all current mirrors used in the proposed design is implemented by cascode current mirrors, to achieve the high output impedance and to reduce the current mirror mismatch, as discussed in previous section. The bias generator circuit shown in Fig. 4.7 is used to generate the bias voltage of pMOS cascode transistors.

M_2 drain current is constant regardless of the status of switches. The bias generator uses this constant M_2 drain current as the input, and generate the bias voltage of pMOS cascode transistors based on it.

4.2.3 Switched capacitor filter (SCF)

The proposed circuit uses CMC, which is implemented by using SCF and pMOS transistors, in order to archive continuous output. As shown in Fig. 4.8 the SCF is made up of two capacitors and two switches, where X represents the SCF number. Switches $SW_{X,1}$ and $SW_{X,2}$ are controlled by non over-lapping clock signals as shown in Fig. 4.3. Capacitors and switches used in SCF were implemented by metal insulator metal capacitors (MIMCAPs) and CMOS switches. When $SW_{X,1}$ is ON, capacitor C_1 is charged to input voltage v_{in}. Next, $SW_{X,1}$ turns off and $SW_{X,2}$ turns on. If v_{in} and v_{out} are not equal, then charge redistributed among C_1 and C_2. This repeats until $v_{in} = v_{out}$. The time constant of the switched capacitor filter is given by (see appendix B)

$$\tau = \frac{C_2}{C_1} \cdot \frac{1}{f_{CLK}} \tag{4.13}$$

where f_{CLK} is the frequency of the switch control signals. The time constant τ determines the settling time of the proposed circuit, and therefore it is an important factor.

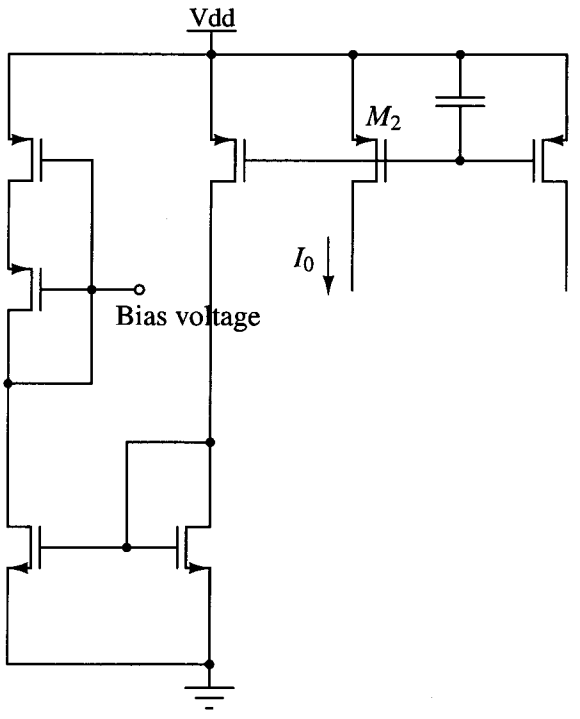

Figure 4.7: Bias generator

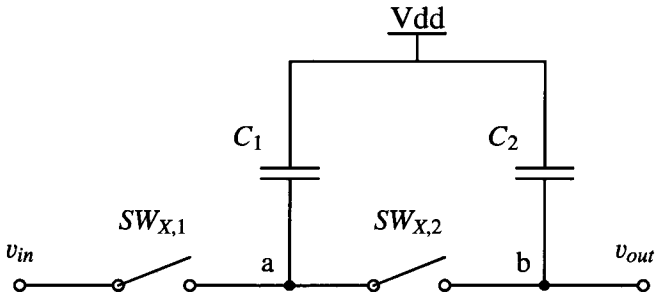

Figure 4.8: Switched-capacitor filter

4.2.4 Differential amplifier

The op-amp used in the proposed bandgap reference circuit is a simple P-channel input two-stage differential amplifier as illustrated in Fig. 4.9. Also in this design, the operational amplifier common mode voltage equals to the base-emitter voltage of the bipolar transistor, which is approximately from 500 mV to 700 mV, requiring a operational amplifier with low input-common mode voltage. The input common mode range of the differential amplifier shown in Fig. 4.9 is from $V_{DD} - V_{THP} - V_{ODP}$ to V_{GND}.

V_{PBIAS} shares the same bias voltage with M_2, providing supply independent bias current. Inputs V_p and V_n are connected to the nodes of Q_1 and R_1, respectively. A compensation capacitor C_C, as shown in Fig. 4.9, is used to ensure the stability of the current source generator.

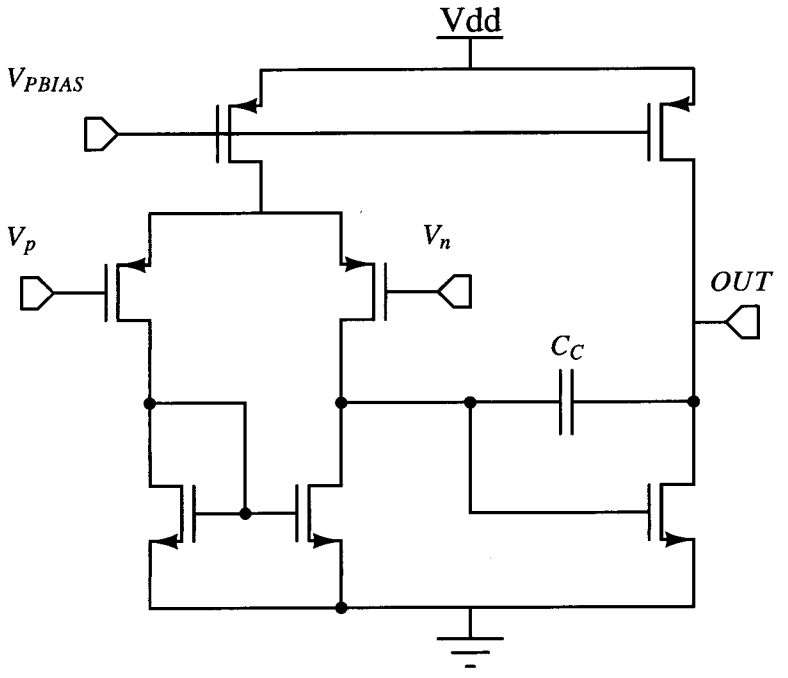

Figure 4.9: Two-stage differential operational amplifier

4.3 Design issues and accuracy analysis

4.3.1 Input offset voltage

The input offset error of the differential op-amp introduces a significant error in output voltage of conventional bandgap references. In typical bandgap references, operational amplifier offset voltage is multiplied by a factor larger than 10 and appears as an error in the reference voltage [2]. Therefore low-offset op-amps or offset cancellation techniques should be used to achieve a precision reference voltage in conventional bandgap references. Considering the offset error of the op-amp, V_{OS}, eqs. (4.4) and (4.6) can be rewritten as

$$I_{R1,OS} = I_{M1\_OS} = \frac{V_{BE1} + V_{OS}}{R_1} \tag{4.14}$$

$$I_{2,OS} = \frac{V_{BE2} + V_{OS}}{R_1} \tag{4.15}$$

Hence the output of the proposed bandgap reference, which includes the offset error of the operational amplifier, can be expressed as

$$V_{REF\_OS} = \frac{R_2}{R_1}\frac{kT}{q}\left\{\alpha \ln \frac{I_0}{I_S} + \beta \ln (n+1)\right\} + \frac{R_2}{R_1}\alpha V_{OS} \tag{4.16}$$

The offset of the operational amplifier is therefore multiplied by the factor $\alpha R_2/R_1$ and appears in the reference voltage. This means in return that the effect of the input offset voltage increases with the increase of R_2/R_1. For simplicity assume that the current mirror ratios are fixed. Then, as mentioned in previous section, by only changing the value of R_2, the output reference voltage can

be set to any value between ($V_{DD} - 2V_{ODP}$) and GND. Thus the maximum value for R_2/R_1 can be calculated when the output reference reaches to ($V_{DD} - 2V_{ODP}$). Assuming that V_{ODP}=0.1 V, the maximum output reference voltage for the proposed design can be given by

$$V_{REF,MAX} = 1.8\text{ V} - 2 \times 0.1\text{V} = 1.6\text{ V} \tag{4.17}$$

To set the output reference to the value given in eq. (4.17), R_2 should be set to approximately 623 kΩ, resulting the maximum theoretical value

$$\frac{R_2}{R_1}\alpha\Big|_{MAX} = 1.2 \tag{4.18}$$

Therefore, in the worst case, the input offset voltage of the amplifier will be multiplied by the factor 1.2 and appeared in the output reference.

However, on the other hand, assume that the output reference set to the typical value of the conventional bandgap references, which is approximately 1.2 V at room temperature. By using the same method as above, it can be shown that the input offset voltage of the operational amplifier will only be multiplied by approximately 0.9. Thus, compared to conventional bandgap reference in which the multiplication factor is larger than 10 [2], the proposed circuit shows superior performance.

4.3.2 Switched feedthrough

Since the proposed circuit also uses the switched-capacitor technique, charge injection and clock feedthrough become important design challenges. When SW_1 turns off, charge injection and clock feedthrough changes the gate voltage of M_2 and M_1. The voltage change due to channel charge injects from SW_1 and the clock feed through can be approximately given by

$$\delta v_{ci} = \frac{C_{OX}}{C_3}\left\{W_N L_N\left(V_{DD} - v_{in} - V_{THN}\right) - W_P L_P\left(v_{in} - |V_{THP}|\right)\right\} \tag{4.19}$$

and

$$\delta v_{cf} = V_{DD}\left(\frac{W_N C_{ovN}}{W_N C_{ovN} + C_3} - \frac{W_P C_{ovP}}{W_P C_{ovP} + C_3}\right) \tag{4.20}$$

respectively, where C_{OX} is the oxide capacitance per unit area, v_{in} is the input voltage of SW_1, V_{THN} and V_{THP} are the threshold voltage of nMOS and pMOS, $W_P L_P$ and $W_N L_N$ are the total gate area of pMOS and nMOS devices, C_{ovP} and C_{ovN} are overlap capacitance per unit width of pMOS and nMOS, respectively. Therefore the total voltage change can be given by $\delta v_1 = \delta v_{ci} + \delta v_{cf}$. As a result of δv_1, the error current of $gm_1\delta v_1$ flow through M_1, where gm_1 is the transconductance of M_1. Furthermore, the error current of $(n + 1)gm_2\delta v_1$ is fed into Q_1, where gm_2 is the transconductance of M_2 and M_3. This error current, which fed into Q_1, results the voltage change of $(n + 1)gm_2\delta v_1/gm_{Q1}$ in V_{BE2}, where gm_{Q1} is the transconductance of Q_1. Therefore the total noise current flow through the output resister R_2 due to δv_1 can be expressed as

$$i_{R2} = \beta\left\{\frac{(n + 1)gm_2}{gm_{Q1}R_1} - gm_1\right\}\delta v_1 \tag{4.21}$$

Since the SCFs are also sensitive to charge injection and clock feedthrough, the effect on the reference voltage should be considered. The voltage of nodes a and b, shown in Fig. 4.8, are

directly affected from $SW_{X,1}$ and $SW_{X,2}$. In node a, most of the channel charge deposited by $SW_{X,1}$ is absorbed by $SW_{X,2}$ minimizing the voltage difference between two phases. However, in practically the charge split between source and drain is not equal. Therefore the voltage difference in node a between two phases is not zero, but compared to that of node b can be negligible. The voltage change in node b due to channel charge injects from $SW_{X,2}$ and clock feedthrough can be calculated by using the same equations of eqs. (4.19) and (4.20). Therefore the noise current flow through R_2 , from M_5, M_6 can be given by

$$\delta i_x = g_M \left(\delta v_{ci,x} + \delta v_{cf,x}\right) \tag{4.22}$$

where x represents the SCF number, and g_M is the transconductance of the corresponding pMOS transistor. From eq. (4.19), it is clear that δv_{ci} can be minimized by selecting proper values for $W_N L_N$ and $W_P L_P$. However, in practice it is impossible to select values for $W_N L_N$ and $W_P L_P$ such that δv_{ci} becomes zero in all range of temperature, because v_{in} is a non-linear value. On the other hand, from eq. (4.20), it can be seen that δv_{cf} is independent of the input level of SCF, and therefore only introduces an offset to output. Both δv_{ci} and δv_{cf} are inversely proportional to C_3, and therefore smaller i_{R2} and δi_x can be archived by selecting larger C_3 and C_2, respectively. But this drives to larger time constant, given by eq. (4.13), and to occupy more design area. However, in case of applications such as pipeline AD converters and DC-DC converters [3, 4] which uses sampled reference therefore continues reference is not required, smaller C_2 can be used. Resulting more design area reduction.

In the proposed design, values of C_1, C_2 and C_3 were set to approximately 3 pF, 80 fF and 180 fF, such that the worst case variation of V_{REF} between two phases to become less than 200 μV.

4.3.3 Current mirror ratios

From eq. (4.11), it is clear that the accuracy of current mirror ratios n, α and β are directly effects the output. Assume that the maximum value of current mismatch is ε%. Thus the worst case of V_{REF} deviation due to mismatch of α, β and n is given by

$$\begin{aligned} V_{REF_\varepsilon} = \frac{R_2}{R_1}\frac{kT}{q}\Bigg[&\left(1+\frac{\varepsilon}{100}\right)\alpha \ln\frac{I_0}{I_S} \\ &+\left(1+\frac{\varepsilon}{100}\right)\beta \ln\left\{n\left(1+\frac{\varepsilon}{100}\right)+1\right\}\Bigg] \end{aligned} \tag{4.23}$$

In mass production, the worst-case deviation of the bandgap voltage is approximately ±5%. From section 4.3.3 it can be seen that to guarantee a worst-case deviation of ±5% in V_{REF} due to current mismatch, ε should be kept less than ±3.75%. For simplicity, considering only the effects of threshold mismatch of pair transistors, current mirror mismatch can be approximated by [5, 6]

$$\frac{\Delta I_D}{I_D} = \frac{0.1 t_{ox}}{\sqrt{WL}} \frac{2}{V_{GS} - V_{TH}} \tag{4.24}$$

where t_{ox} is expressed in angstroms and W and L in microns. Assume that the MOS devices are implemented by square transistors, and the overdrive voltage is 100 mV. Thus, in a 0.18 μm technology with $t_{ox} \approx 40$ Å, the minimum value of L and W should be 2.13 μm to achieve ±5% worst-case deviation in V_{REF}. However, good layout techniques, such as common centroid and use of dummy devices, can be effectively used to minimize the mismatch errors, so that to reduce the minimum values of L and W.

4.4 Simulation results

The proposed area-efficient, Low-power bandgap reference was designed in 0.18 μm CMOS process, and simulations were carried out to verify the performance. The following simulations were done:

- Temperature sweep.
  - The supply independent current source.
  - Operational amplifier
  - Switched capacitor filter.
  - The full bandgap reference.
- Stability analysis.
- Monte Carlo simulations.
  - Operational amplifier input offset and its effect on reference voltage.
  - Device mismatches.
- Power supply sweep.
- Transient Sweep.

4.4.1 Temperature sweep

Operational amplifier

The operational amplifier is simulated using the same circuitry shown in Fig. 3.16. Figure 4.10 represents the simulation results of open-loop transfer function in different temperatures, and various supply voltages. The aim of the operational amplifier used in the proposed bandgap reference is sensing the voltages across the resistor R_1 and bipolar transistor Q_1, and regulate them to be equal. This requires a high differential gain. As can be seen in Fig. 4.10, the open loop differential gain is approximately 80 dB, and remain stable for all operating conditions.

From the Fig. 4.10, the worst case phase margin can be calculated as

$$PM = 180° - 114° = 66° \tag{4.25}$$

when temperature is 100°C. Thus, it can be said that the system is stable in all the operation conditions. However, other than this small-signal ac simulations, the stability of the proposed design is examined by using large signal time-domain simulation (applying a step function to V_{DD}), and will be discussed in latter section.

Supply independent current source

The simulated output current of the supply independent current source in different temperatures and the temperature dependence are shown in Fig. 4.11 and 4.12, respectively. From above results. it can be said that the supply independent current source is stable in temperature range from 0 °C to 100 °C, and the temperature coefficient of the output current is approximately -0.86 nA/°C.

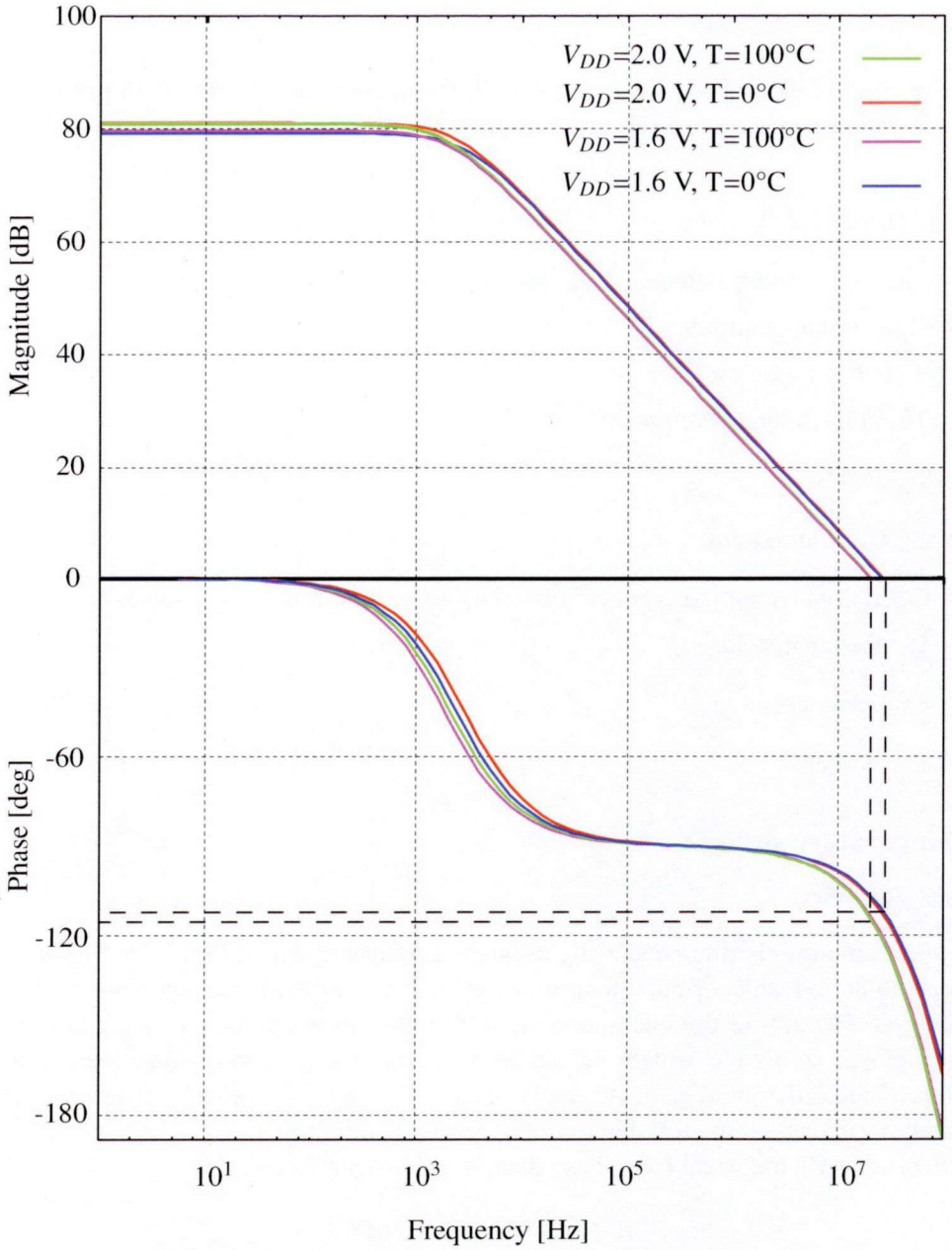

Figure 4.10: Magnitude and phase of the open-loop transfer function

Figure 4.13 represents the simulated results of the base emitter voltages of Q_1, V_{BE1}, and V_{BE2}, corresponding to the phase of SW_2 is OFF and ON, respectively, and calculation results of ΔV_{BE}. As discussion in previous section, the temperature coefficients of both V_{BE1} and V_{BE2} are negative, and the temperature coefficient of ΔV_{BE} is positive. The temperature coefficients of V_{BE1} and ΔV_{BE} can be calculated as follows.

$$\frac{\partial V_{BE1}}{\partial T} = \frac{430.1\ \text{mV} - 663.0\ \text{mV}}{100\ ^\circ\text{C}} = -2.33\ \text{mV}/^\circ\text{C} \tag{4.26}$$

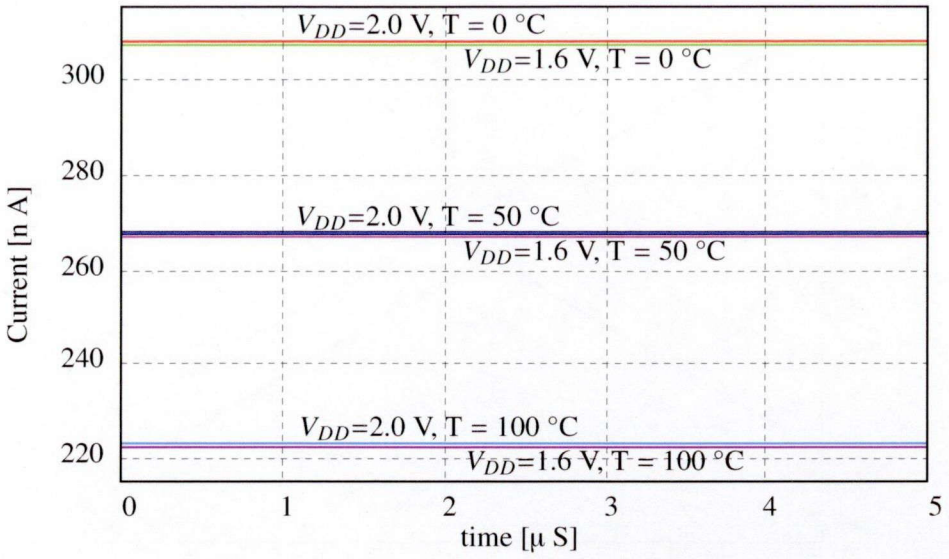

Figure 4.11: Output current of supply independent current source in different temperature

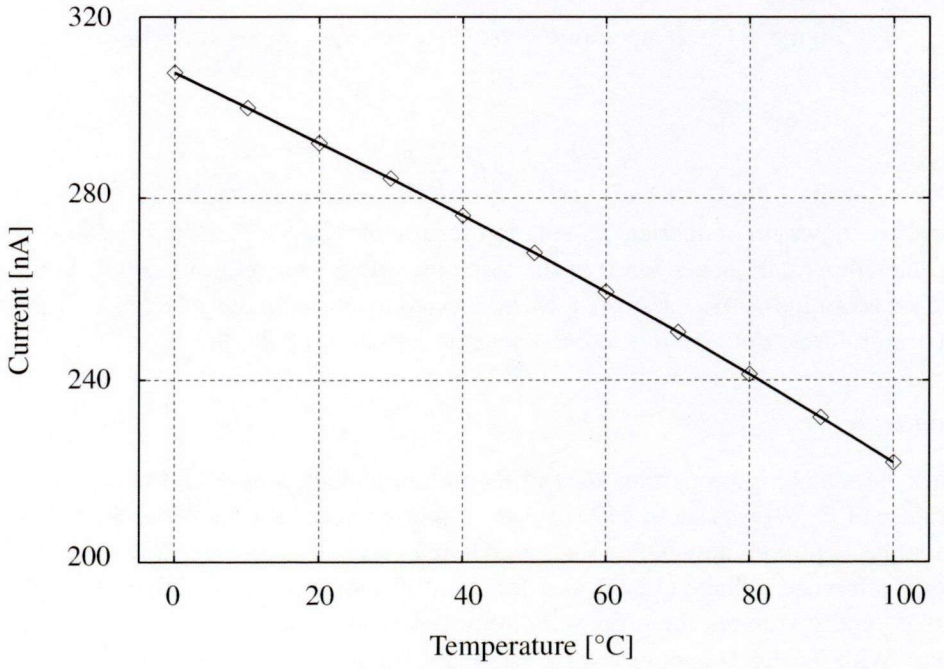

Figure 4.12: Temperature dependence of current source

and,

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{35.4\text{ mV} - 26.2\text{ mV}}{100\text{ °C}} = 0.092\text{ mV/°C} \tag{4.27}$$

Note that, for simplicity, we ignore the second order effects. Thus, selecting the constants α and β in eq. (4.12), such that $\alpha : \beta = 0.092 : 2.33$, the following condition can be satisfied.

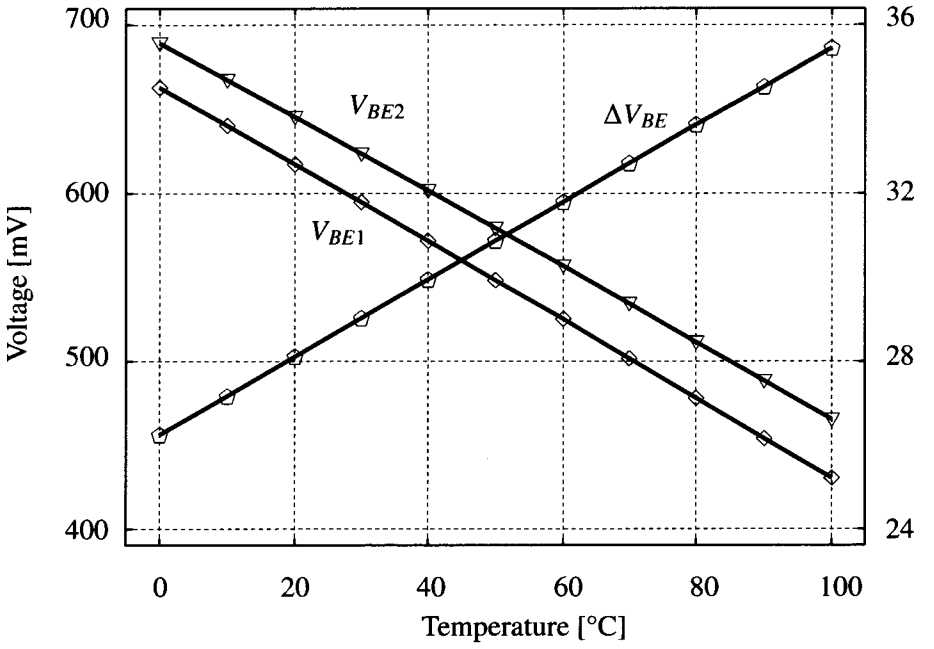

Figure 4.13: Temperature dependence of V_{BE1}, V_{BE2} and ΔV_{BE}

$$\alpha \frac{\partial V_{BE1}}{\partial T} + \beta \frac{\partial \Delta V_{BE}}{\partial T} = 0 \tag{4.28}$$

Figure 4.14 shows the numerical calculation results of V_{BE1} + (2.33/0.092)V_{BE2}. The results prove that the temperature dependence of the resultant voltage is negligibly small. In the proposed design, the aspect ratios of $M_1 : M_5$, $M_4 : M_6$ is selected to approximately 18 : 5, 1 : 7, respectively. Thus the current mirror ratio $\alpha : \beta$ is to become approximately 1 : 25.2.

Full reference

Considering the matching properties, R_1 and R_2 are implemented by 17.5 kΩ unit resistors. The resisters values of R_1, R_2 was set to 140 kΩ and 245 kΩ, respectively, such that the output reference voltage becomes approximately 630 mV at room temperature. Figure 4.15 shows simulation results of the output reference voltage (V_{REF}) as a function of temperature for different supply voltages. With a 1.8 V supply voltage, the proposed circuit produces a output voltage of 629 mV, at room temperature. With the 1.6 V supply voltage (standard supply voltage for for the proposed design), the maximum variation of the output voltage over the temperature range of 0 °C to 100 °C is 0.8 mV (629.3 mV at 50 °C- 628.5 mV at 0 °C). Thus the temperature coefficient of the output voltage with 1.6 V constant power supply is

$$\begin{aligned} TC_{VDC=1.6V} &= \frac{1}{629\ \text{mV}} \cdot \frac{629.3\ \text{mV} - 628.5\ \text{mV}}{100\ °\text{C}} \times 10^6 \\ &= 12.6\ \text{ppm/°C} \end{aligned} \tag{4.29}$$

The worst case deviation of the output in above temperate range is 0.85 mV (628.85 mV at

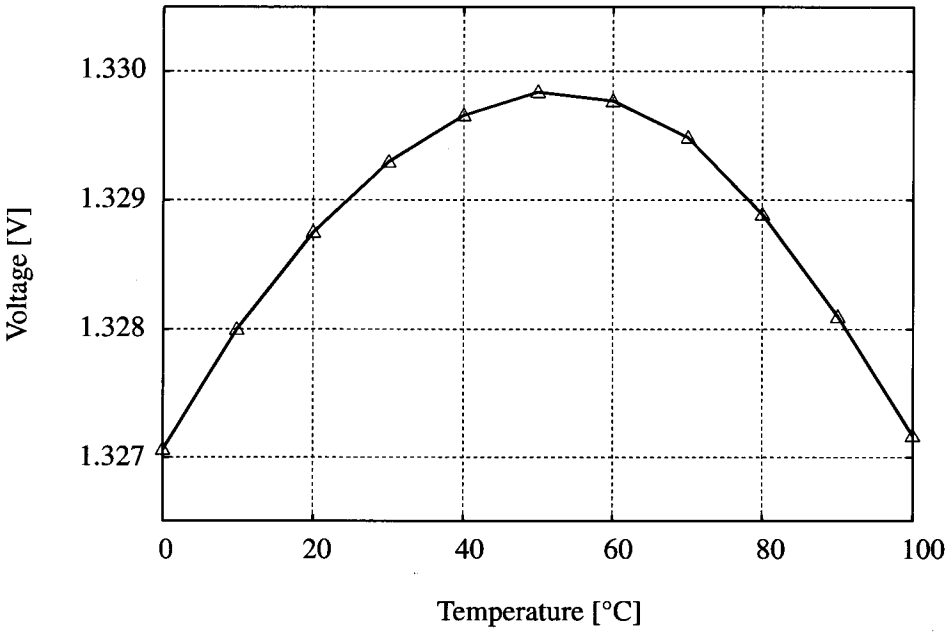

Figure 4.14: Numerical calculation results of $V_{BE1} + (2.33/0.092)V_{BE2}$

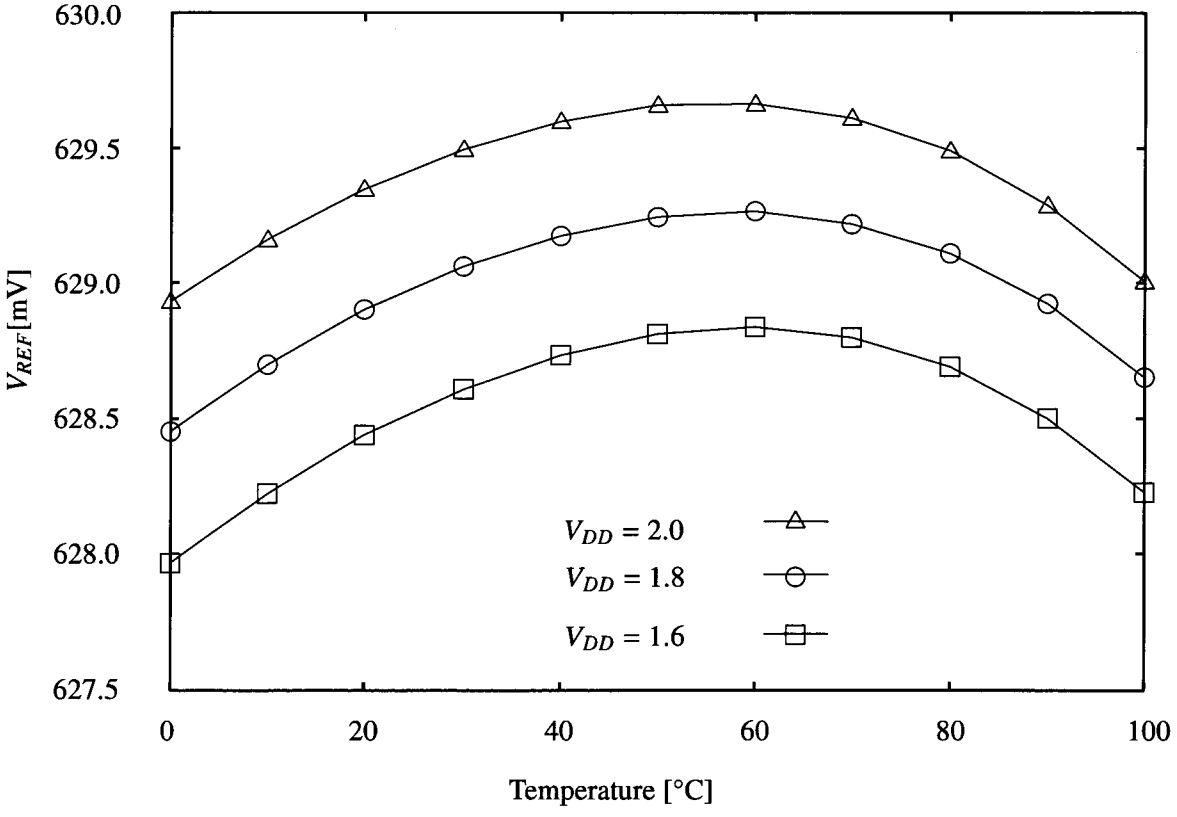

Figure 4.15: Temperature and power supply dependence of reference voltage

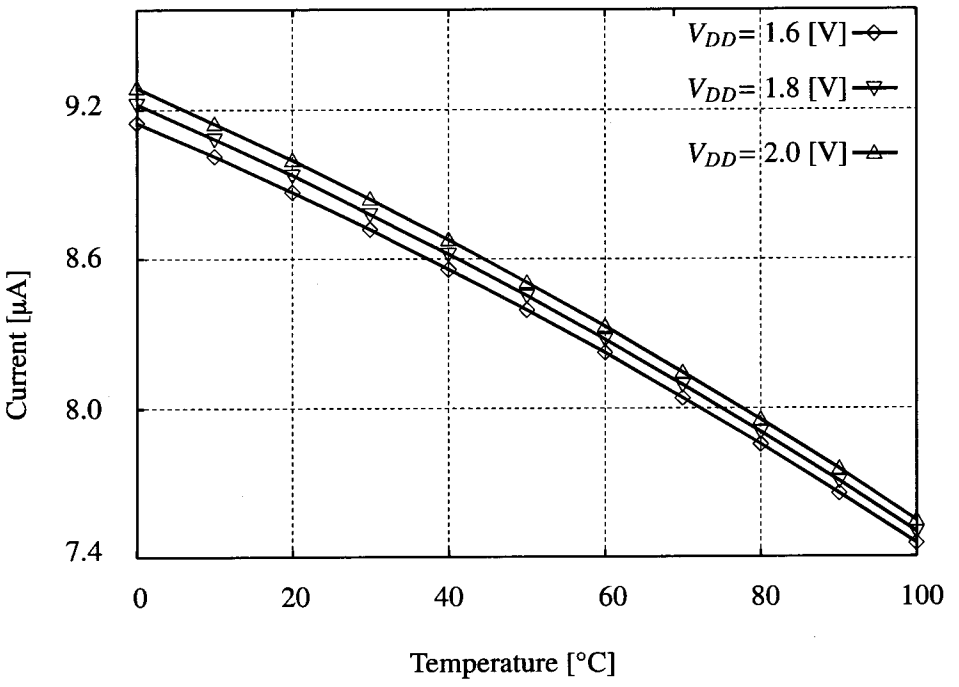

Figure 4.16: Power consumption

50 °C- 628.0 mV at 0 °C), when 1.6 V supply voltage is applied. Thus the worst case temperature coefficient can be given by

$$TC = \frac{1}{629\text{ mV}} \cdot \frac{628.85\text{ mV} - 628.0\text{ mV}}{100°\text{C}} \times 10^6 = 13.5\text{ ppm/°C} \tag{4.30}$$

Figure 4.16 compiles the simulated results of supply current as a function of temperature for different supply voltages. From the results in Fig. 4.16, it can be shown that the reference circuit consumed an average of 8.5μ A in the temperature range from 0 °C to 100 °C, while consuming the maximum of 9.2 μA at 0 °C.

4.4.2 Monte Carlo verification

Monte Carlo (MC) simulation is used in order to estimate the operational amplifier offset and its effect on the reference voltage. We executed 1000 simulation runs under 1.6 V supply voltage in room temperature and the obtained mean value and standard deviation of the operational amplifier offset was 0.45 mV and 9.7 mV. The deviation of the V_{REF} due to operational amplifier offset is shown in Fig. 4.17. The mean value and the standard deviation was 628.67 mV and 4.8 mV, respectively, which means in return that the operational amplifier offset error is reduced and appear in output, as we discussed in previous section. Additionally, the mean value and the standard deviation of the temperature coefficient distribution due to operational amplifier offset was 14.66 mV, and 3.43 mV, respectively, over the temperature range from 0 °C to 100 °C.

Finally, another set of MC simulations were carried out to investigate the effect of device mismatch on the proposed circuit. We performed 1000 MC simulation runs under 1.6 V supply voltage

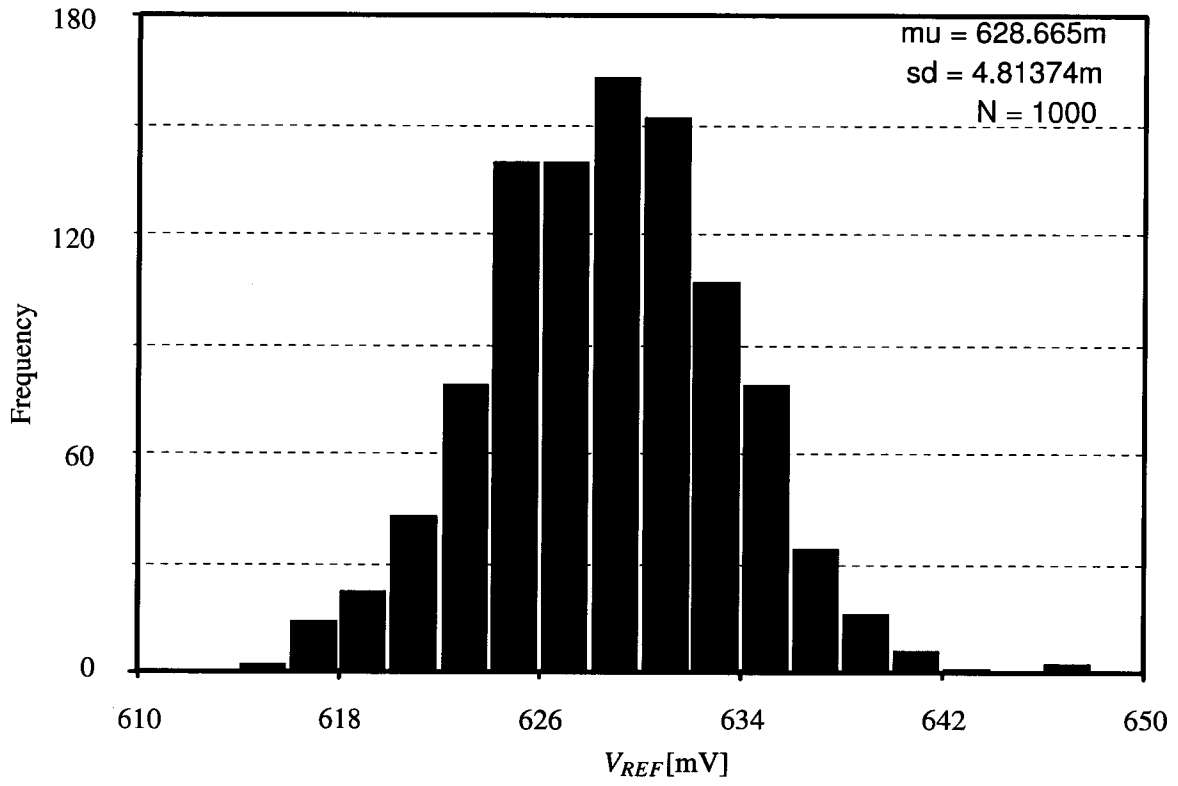

Figure 4.17: V_{REF} variations due to operational amplifier offset (Monte Carlo Simulations: 1000 runs)

at room temperature, and results are presented in Fig. 4.18. The mean value of V_{REF} is 632.82 mV, and the standard deviation is 56.8 mV (9%). The value of standard deviation is slightly larger than that of [5] in which trimming method is used. By implementing a trimming network or other mismatch cancellation methods (such as chopping techniques), V_{REF} deviation due to mismatch can be further minimized.

4.4.3 Power supply variation and transient response

From Fig. 4.15, the worst-case deviation in V_{REF} due to power supply variation can be seen at T=0 °C. Thus the worst-case DC power supply rejection ratio can be calculated as

$$PSRR_{worst} = 20\log\left(\frac{V_{REF,VDD=1.8} - V_{REF,VDD=1.6}}{200\text{ mV}}\right)$$
$$= 20\log\left(\frac{628.48\text{ mV} - 628.00\text{ mV}}{200\text{ mV}}\right) \approx -52.3\text{ dB} \quad (4.31)$$

Figure 4.20 shows the transient response of the proposed circuit, and Fig. 4.21 represents the enlarged view. The settling time is approximately 20 μs. Temperature dependent of the settling time can be neglected. Some spikes can be seen in the output when the clock changes. Therefore in the applications that requires smooth reference voltage, the proposed circuit should be used with a low pass filter. So that the spikes can be eliminated. But in the applications like pipeline A/D converters, which use sampled reference, those spikes will not become a problem.

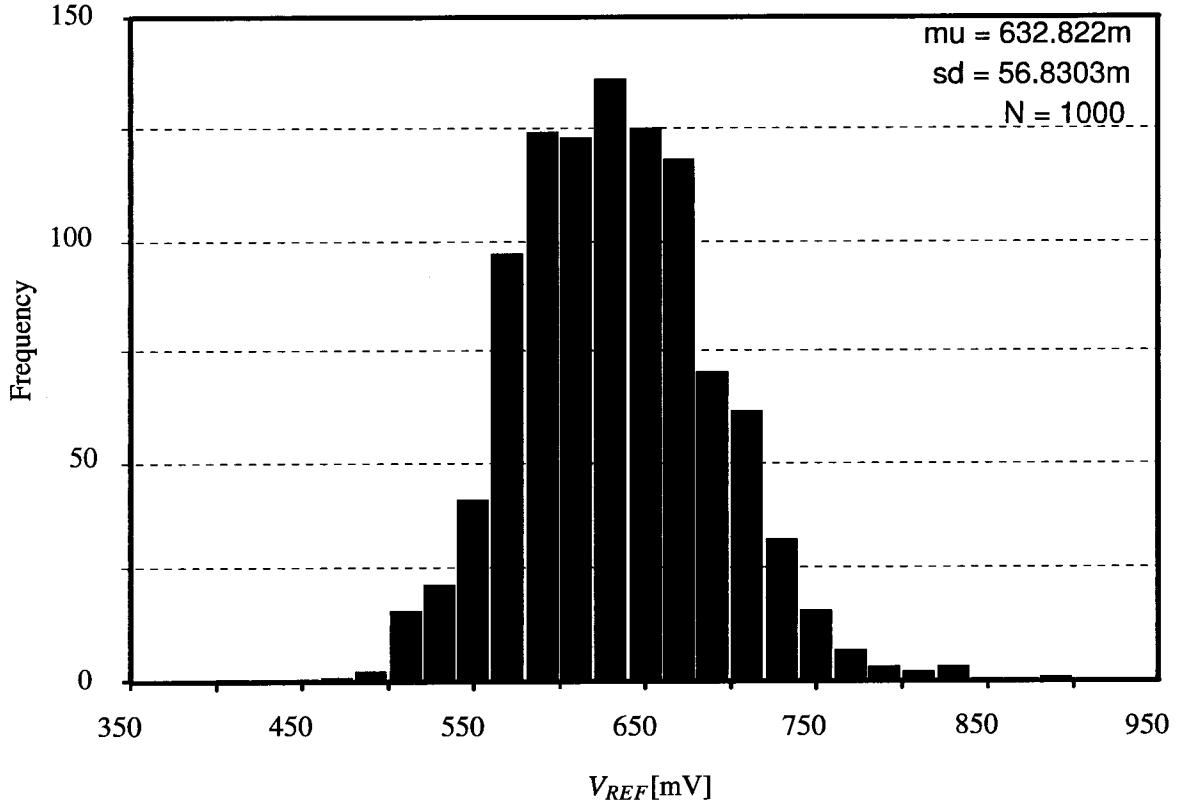

Figure 4.18: V_{REF} variation due to device mismatch (Monte Carlo simulations: 1000 runs)

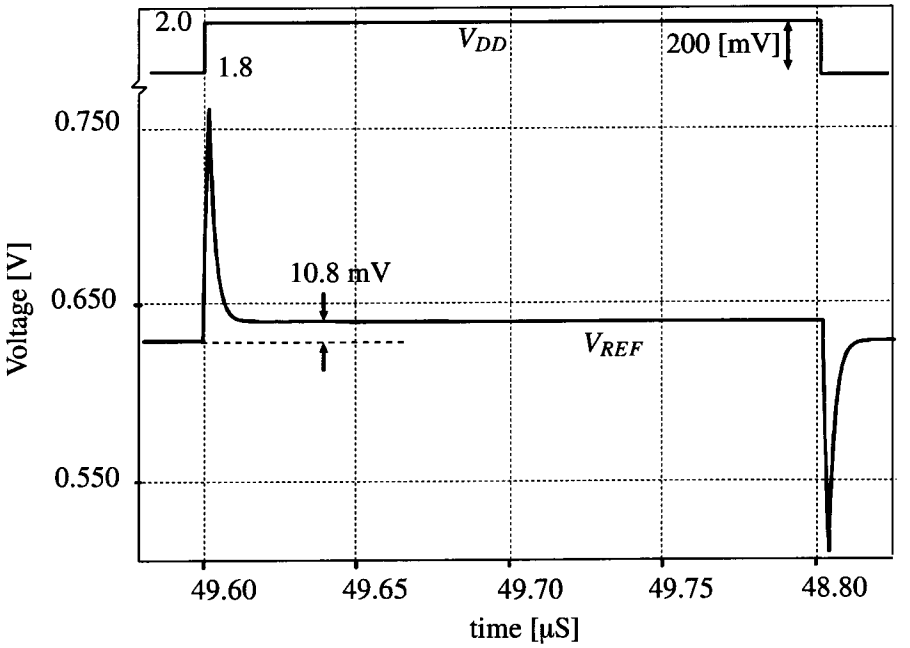

Figure 4.19: Transient response of output voltage when step is applied to supply voltage

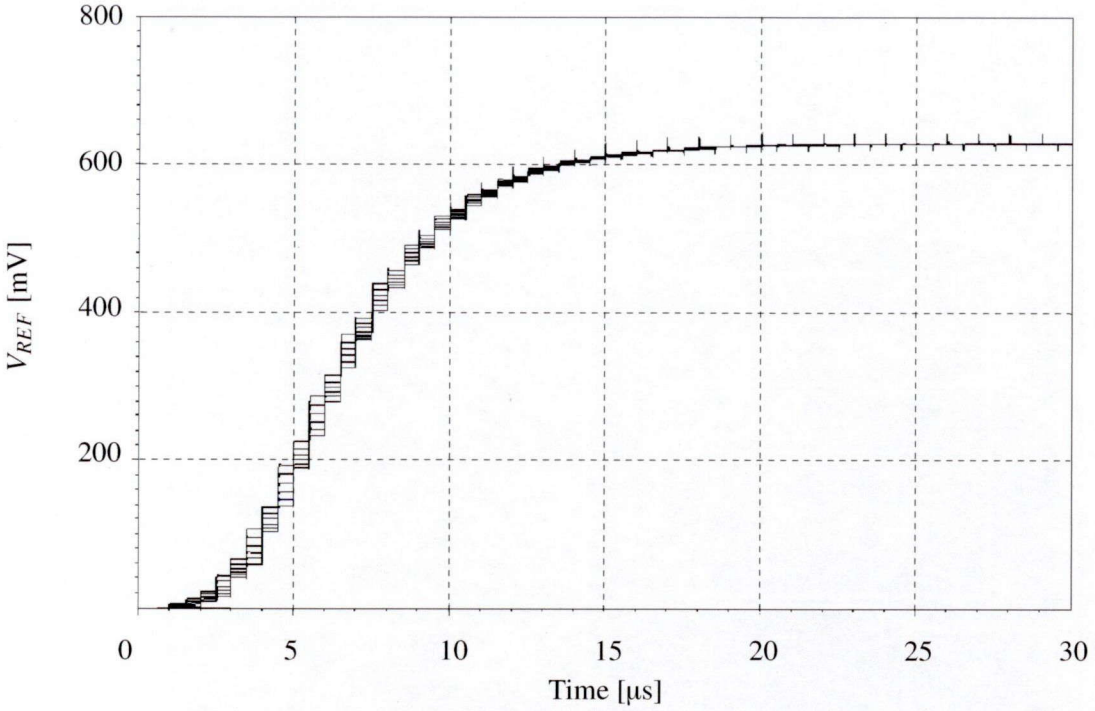

Figure 4.20: Transient response of the proposed circuit

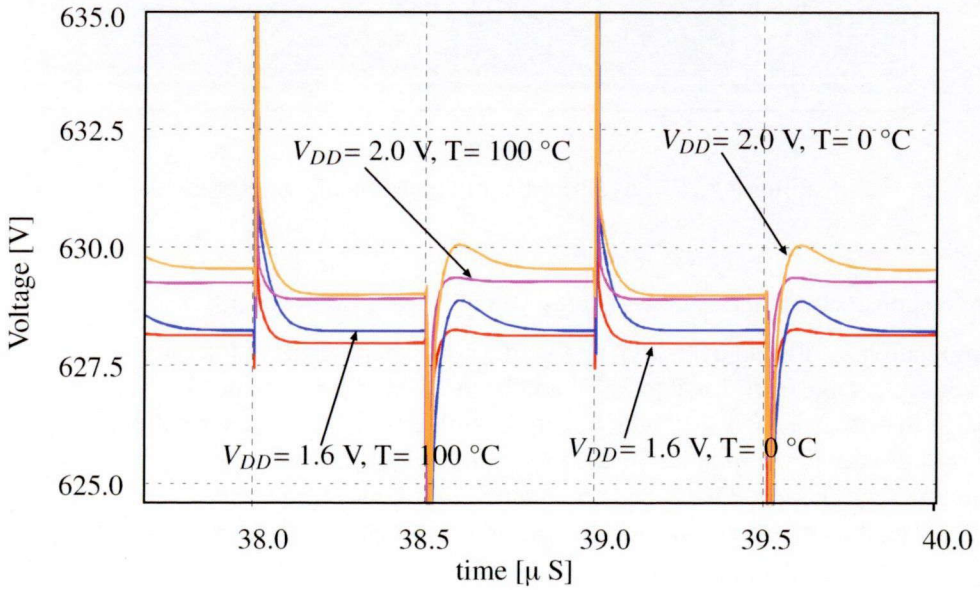

Figure 4.21: Enlarged view of V_{REF} shown in Fig. 4.19

4.4.4 Stability verification

To check the stability of the proposed bandgap reference, a small step voltage is applied to the supply voltage and the change in output voltage is examined. Figure 4.19 shows the simulated

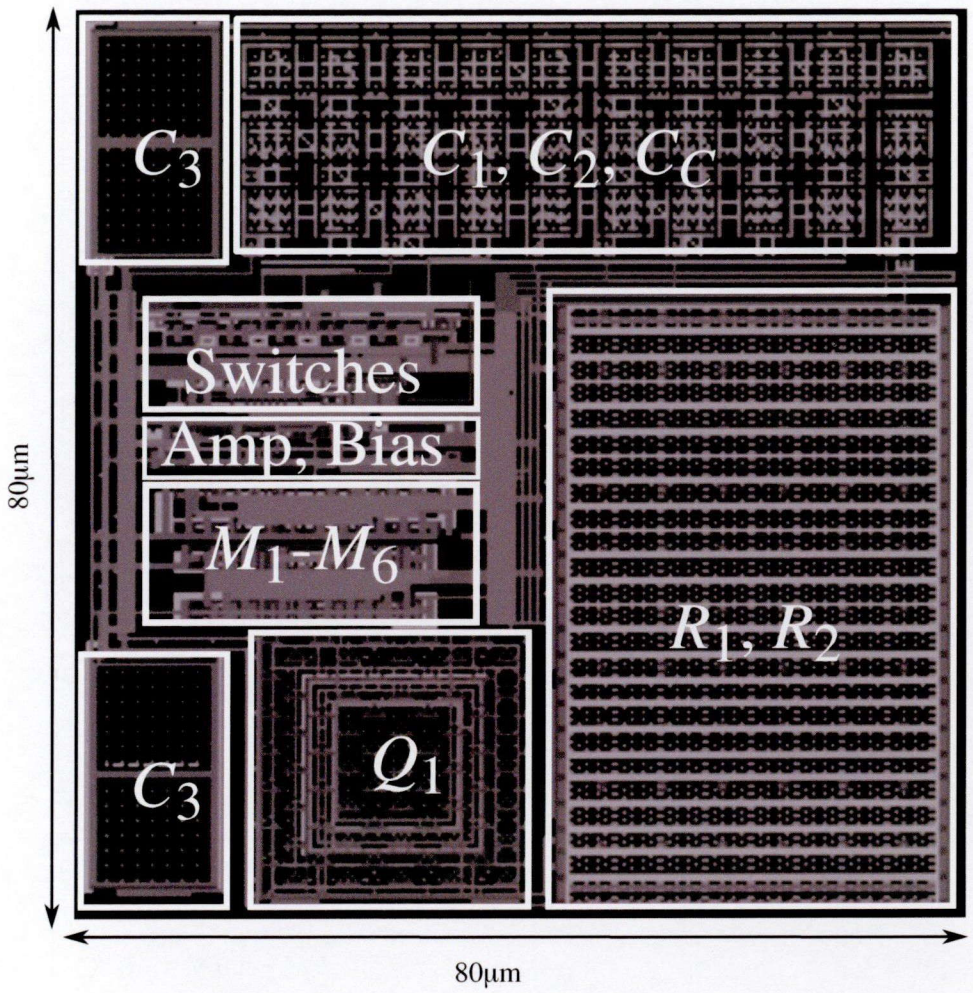

Figure 4.22: Layout of the proposed bandgap reference

transient response of the output when supply voltage change between 1.8 V and 2.0 V.

In simulation results, an overshoot and undershoot can be observed in output voltage, when the supply voltage change from 1.8 V to 2.0 V and from 2.0 V to 1.8 V, respectively. The observed voltage change in output is 10.8 mV, which is approximately ±1.7% of the final output. This voltage change is approximately twice larger than the value which is observed in bandgap reference presented in previous chapter. This is because the previous bandgap reference uses current subtraction in output stage, thus the noise currents due to supply voltage changes act to cancel each other.

4.5 Layout

Fig. 4.22 shows the layout of the proposed circuit. The occupied layout area is less than 0.0064 mm^2 (80 $\mu m \times 80\ \mu m$).

4.6 Comparison

Table 4.1 compares the performance of the bandgap reference described in this research to that of previously published bandgap references. The bandgap reference presented in this research shows good performance in temperature dependence and shows best performance in design area. Therefore it is ideal for low-cost, high accuracy and high performance application. Although [7] demonstrated a low power consumption, our design is superior in all other performances. Moreover, the proposed circuit shows very good performance in PSRR. Compared to this work, [8] and [9] have demonstrated better PSRR, but our design occupies significantly smaller design area and consumes less power.

4.7 Summary

A novel area-efficient, low power, fractional bandgap reference utilizing switched-current and current-memory techniques is presented. The operating principles, design issues, accuracy analysis, and verifications using SPICE simulations are discussed. Table 4.2 summarizes the performance of the proposed bandgap reference. This design also uses only one bipolar transistor to generate the reference voltage so that the significant area reduction is chived. The proposed circuit is designed and simulated in 0.18 μm CMOS process. The simulation results show that the output reference voltage V_{REF} is approximately 628.5 mV, and the temperature coefficient of V_{REF} is smaller than 13.5 ppm/°C for the temperature range from 0 °C to 100 °C. The layout occupies only 0.0064 mm^2 (80 μm ×80 μm) and average power consumption is 13.6 μW.

Table 4.1: Comparison to previously published CMOS bandgap references

	This Work	[7]	[1]	[8]	[9]	[10]	[11]
Process	0.18-μm	0.4-μm Flash	0.25-μm	0.35-μm	0.35-μm	0.5-μm digital	0.35-μm
V_{REF} (V)	0.6285	0.518	0.650	0.858	1.2	1.12	0.640
TC ppm/°C	13.5	118	10.4	12.4	38.3	127	580
Design Area (mm^2)	0.0064	0.1	0.011	1.2	0.043	0.4	0.21
PSRR (dB)@ kHz	-50@0.1	-20@1	-53@0.1	-68@0.1	-58@0.1	-45@0.01	N.A.
Power (μW)	13.6	5	138.6	162	24.5	1400	74

Table 4.2: Performance summary

Technology	0.18 μm CMOS
Area	0.0064 mm^2 (80 μm × 80 μm)
Minimum Supply Voltage	1.6 V
V_{REF}	628.5 mV
TC of V_{REF}	13.5 ppm/°C (0 °C to 100 °C)
Average current consume	8.5 μA
SW_1 Switching Frequency	1 MHz
PSRR	-52 dB (DC)
	-50 dB @ 100Hz
	-49.5 dB @ 1kHz

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Chapter 5

Ultra-low power current reference

5.1 Introduction

The increasing demand for portable electronic devices, micro-sensors, and bio medical sensors makes the power-efficient circuits increasingly important. As a result, subthreshold circuits are attracting attention because of their ultra-low-power consumption. One of the main drawbacks of the circuits, however, is the exponential temperature dependence of drain current, which makes the design of subthreshold circuits quite difficult. The implementation of a proper temperature-independent current source into a chip could significantly suppress the temperature dependence of the subthreshold circuit performance. Most current references based on PTAT use bipolar transistors [1, 2], while those using parasitic bipolar transistors available in the standard CMOS process show poor performances, require a large design area, and consume relatively large power. Therefore, the current references [1, 2] based on CMOS-only designs cannot be used in ultra-low-power applications. Another approach to current reference [3] based on β-multiplier, which requires resistors and consumes several dozen microwatts is still not suitable for CMOS-only and ultra-low-power designs. To overcome these problems, CMOS-only current references using subthreshold circuits have been demonstrated [4, 5]. The CMOS-only current reference proposed by Oguey and Aibischer [4] consumes very little power, and the circuit structure is very simple. However, the output reference current of the circuit is proportional to $T^{0.4}$, where T represents the absolute temperature and is not suitable to be used as a temperature-independent current source. The current reference in the literature [5] has shown reasonable temperature immunity and low-power consumption, although the circuit techniques are quite complex and the temperature coefficient is not small enough for high accuracy applications.

In this chapter, we proposed a new and simple current reference circuit composed of two current subcircuits that have positive but different temperature coefficients. The operation principle and computer-based simulation results are presented. The output reference current is fairly insensitive to temperature and supply voltage variations. The power consumption of the proposed circuit is less than 1 μW. Therefore, the proposed circuit is ideal to be used as a temperature-independent current source, which will help circuit designers overcome the exponential temperature dependence of subthreshold circuit performance.

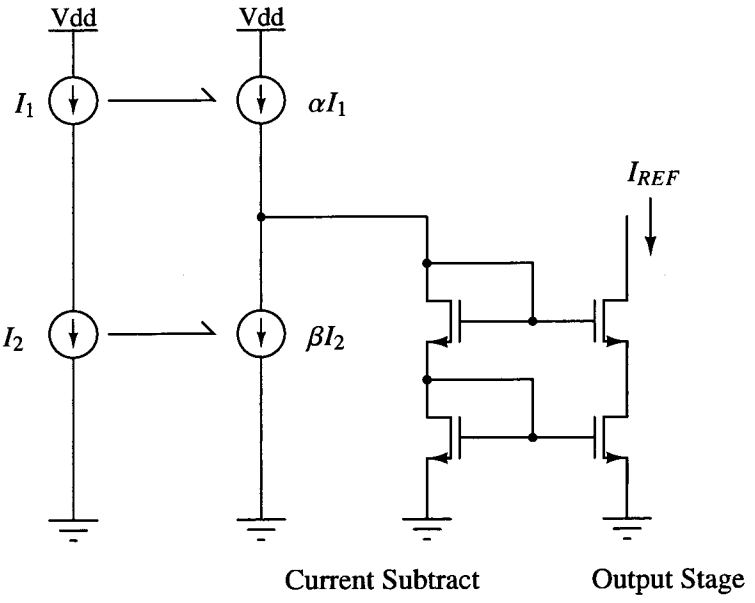

Figure 5.1: Concept of proposed current reference

5.2 Structure of the proposed current reference

5.2.1 Operation principle

Figure 5.1 illustrates the conception of the proposed current reference. The circuit consists of two current sources, I_1 and I_2, that have different TCs, a current subtraction stage, and a output stage. Current sources I_1 and I_2 generate different currents with a different temperature coefficients. In the current subtraction stage, the currents generated by the current sources I_1 and I_2 are multiplied by proper coefficients and subtracted so that the resultant current has the minimum temperature dependence. The output stage mirrors the resultant current to the preferable output reference current. The current source subcircuits that are used to generate current sources with different TCs, current subtraction stage and output stage are described in next section.

5.2.2 Current source subcircuits

The current sources I_1 and I_2 in Fig. 5.1 are implemented using the current source subcircuit shown in Fig. 5.2, which is based on β-multiplier circuit. However, the resistor of the β-multiplier is replaced by a nMOS device M_5, which is operated in the deep triode region. The bias voltages for M_5 is generated by diode-connected nMOS devices, M_6 , operated in the saturation region. All other transistors used in the current source subcircuit are operated in the subthreshold region.

In subthreshold region, the channel of MOSFETs is not inverted and current flows by diffusion. Thus the drain current of the MOSFETs operated in the subthreshold region is mainly composed of the subthreshold leakage current (see appendix C) and can be expressed as follows [6]

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right)\left\{1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right\} \tag{5.1}$$

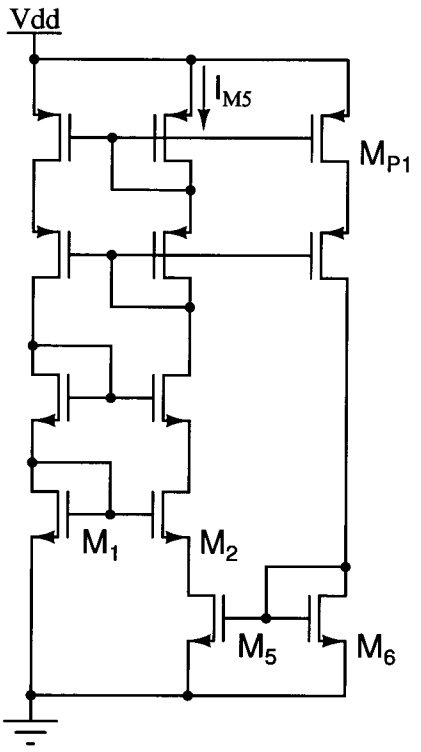

Figure 5.2: Current source subcircuit

where I_0 is the drain current when $V_{GS} = V_{TH}$ given in eq. (5.2).

$$I_0 = \mu C_{OX} (\eta - 1) V_T^2 \tag{5.2}$$

K is the aspect ratio ($= W/L$), η is the subthreshold slope factor, $V_T = (kT/q)$ is the thermal voltage, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance per unit area, k is the Boltzmann constant, and q is the elementary charge. For values of $V_{DS} > 4V_T$ (approximately 100 mV at room temperature), I_D becomes almost independent of V_{DS}. Therefore, eq. (5.1) can be modified as follows.

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \tag{5.3}$$

In the current source subcircuit shown in Fig. 5.2, nMOS transistors M_1 and M_2 shares the same gate voltage. Thus the relationship between the gate-source voltages of M_1 and M_2 ($V_{GS,1}$, $V_{GS,2}$) and drain-source voltage of M_5 ($V_{DS,5}$) can be expressed as

$$V_{GS,1} = V_{DS,5} + V_{GS,2} \tag{5.4}$$

On the other hand, all pMOS devices in the current source subcircuit shares the same aspect ratios, resulting same drain current through M_1, M_2 and M_6. Therefore, from eqs. (5.3) and (5.4), we have

$$\begin{aligned} V_{DS,5} &= V_{GS,1} - V_{GS,2} \\ &= \eta V_T \ln\left(\frac{K_2}{K_1}\right) - \Delta V_{TH} \end{aligned} \tag{5.5}$$

thus,

$$\frac{1}{V_{DS,5}}\frac{\partial V_{DS,5}}{\partial T} = \frac{1}{\eta V_T \ln\left(\frac{K_2}{K_1}\right) - \Delta V_{TH}}\left\{\frac{\eta V_T}{T}\ln\left(\frac{K_2}{K_1}\right) - \frac{\Delta V_{TH}}{\partial T}\right\} \tag{5.6}$$

where $\Delta V_{TH}(= V_{TH,2} - V_{TH,1})$ is the difference between the threshold voltages of M_1 and M_2. The threshold voltage of nMOS devices can be approximated by

$$V_{TH0} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{OX}} \tag{5.7}$$

where Φ_{MS} is the difference between the work functions of the polysilicon gate and the silicon substrate, Φ_F is the Fermi potential given by

$$\Phi_F = \frac{kT}{q}\ln\frac{N_{sub}}{n_i} \tag{5.8}$$

where, N_{sub} is the doping concentration of the substrate, Q_{dep} is the charge in the depletion region,n_i is the intrinsic concentration of silicon, However, in eq. (5.7), the body effect has not been taken into the account. Thus, considering the body effect, the threshold voltage of the nMOS transistor can be re-written as [7]

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right) \tag{5.9}$$

where V_{SB} is the source-bulk potential difference, and γ is the body effect coefficient given by

$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_{SUB}}}{C_{OX}}. \tag{5.10}$$

Therefore, the value of ΔV_{TH} in eq. (5.4) can be approximated by

$$\Delta V_{TH} = \gamma\left(\sqrt{2\Phi_F + V_{DS,5}} - \sqrt{2\Phi_F}\right) \tag{5.11}$$

By using eqs. (5.6) and (5.11), the temperature coefficient of $V_{DS,5}$ can be approximated by

$$\frac{1}{V_{DS,5}}\frac{\partial V_{DS,5}}{\partial T} = \frac{1}{T}\left\{1 + \frac{\eta V_T \ln\left(\frac{K_2}{K_1}\right)}{\eta V_T \ln\left(\frac{K_2}{K_1}\right) - \Delta V_{TH}}\right\} \tag{5.12}$$

The drain current of M_5 operated in the deep triode region can be given by

$$I_{M5} = \mu C_{OX}\left(\frac{W}{L}\right)_5 (V_{GS,5} - V_{TH,5})\, V_{DS,5} \tag{5.13}$$

Moreover, the temperature coefficient ($\frac{1}{I}\frac{\partial I}{\partial T}$) of the current given in eq. (5.13) can be shown by

$$\frac{1}{I_{M5}}\frac{\partial I_{M5}}{\partial T} = \frac{1}{\mu}\frac{\partial \mu}{\partial T} + \frac{1}{V_{GS,5} - V_{TH,5}}\frac{\partial (V_{GS,5} - V_{TH,5})}{\partial T} + \frac{1}{V_{DS,5}}\frac{\partial V_{DS,5}}{\partial T} \tag{5.14}$$

The carrier mobility, μ, decrease with the temperature [8]. This temperature dependence of mobility μ is given by

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m} \tag{5.15}$$

where $\mu(T_0)$ is the carrier mobility at room temperature and m is a constant. As mentioned above, nMOS transistor M_6 is operated in the saturation region, thus, the drain current I_{M6} is given by

$$I_{M6} = \mu C_{OX}\left(\frac{W}{L}\right)_6 (V_{GS,6} - V_{TH,6})^2 \tag{5.16}$$

additionally, the temperature coefficient is given by

$$\frac{1}{I_{M6}}\frac{\partial I_{M6}}{\partial T} = \frac{1}{\mu}\frac{\partial \mu}{\partial T} + \frac{2}{(V_{GS,6} - V_{TH,6})}\frac{\partial (V_{GS,6} - V_{TH,6})}{\partial T} \tag{5.17}$$

However, as shown in Fig. 5.2, nMOS transistors M_5 and M_6 shares the same gate voltage, thus the temperature coefficient of $V_{GS,6}$ is equal to that of $V_{GS,5}$. Since $I_{M5} = I_{M6}$, drain currents I_{M5} and I_{M6} shares the same temperature coefficient. Thus, the temperature coefficient of I_{M5} can be calculated by using eq. (5.17) as follows.

$$\frac{1}{I_{M5}}\frac{\partial I_{M5}}{\partial T} = \frac{1}{\mu}\frac{\partial \mu}{\partial T} + \frac{2}{(V_{GS,5} - V_{TH,5})}\frac{\partial (V_{GS,5} - V_{TH,5})}{\partial T} \tag{5.18}$$

Note that, for simplicity, we assumed $V_{TH,5} = V_{TH,6}$.

Therefore, from eqs. (5.12), (5.14), (5.15) and (5.18), the temperature coefficient of the output current, I_{M5}, of current source subcircuit in Fig. 5.2, can be written as

$$\frac{1}{I_{M5}}\frac{\partial I_{M5}}{\partial T} = \frac{1-m}{T} + \frac{1}{T}\left\{\frac{\eta V_T \ln\left(\frac{K_2}{K_1}\right)}{\eta V_T \ln\left(\frac{K_2}{K_1}\right) - \Delta V_{TH}}\right\} \tag{5.19}$$

The value of m is approximately 1.5 for ordinary nMOS devices. Consequently, the temperature coefficient given in eq. (5.19) is positive. However, from a simple calculation, it can be seen that for a given temperature, the temperature coefficient given in eq. (5.19) decreases with an increase in (K_2/K_1) ratio.

5.2.3 Temperature independent current source

The schematic of the proposed subthreshold current reference is shown in Fig. 5.3. It consists of two current sources (Subcircuit (A) and Subcircuit (B)), a current subtract stage, and a output stage. The current sources are implemented by using the above described current sources that are designed to have current outputs with different temperature coefficients. Thus, the temperature coefficients of the output currents can be calculated in the same manner described in previous section. In the proposed design, we selected the aspect ratios of K_1–K_4 , such that

$$\frac{K_2}{K_1} > \frac{K_4}{K_3} \tag{5.20}$$

As a result, the current source subcircuit (A) has a smaller temperature coefficient compared with that of subcircuit (B). Thus we can write

$$\frac{1}{I_{M7}}\frac{\partial I_{M7}}{\partial T} > \frac{1}{I_{M5}}\frac{\partial I_{M5}}{\partial T} \tag{5.21}$$

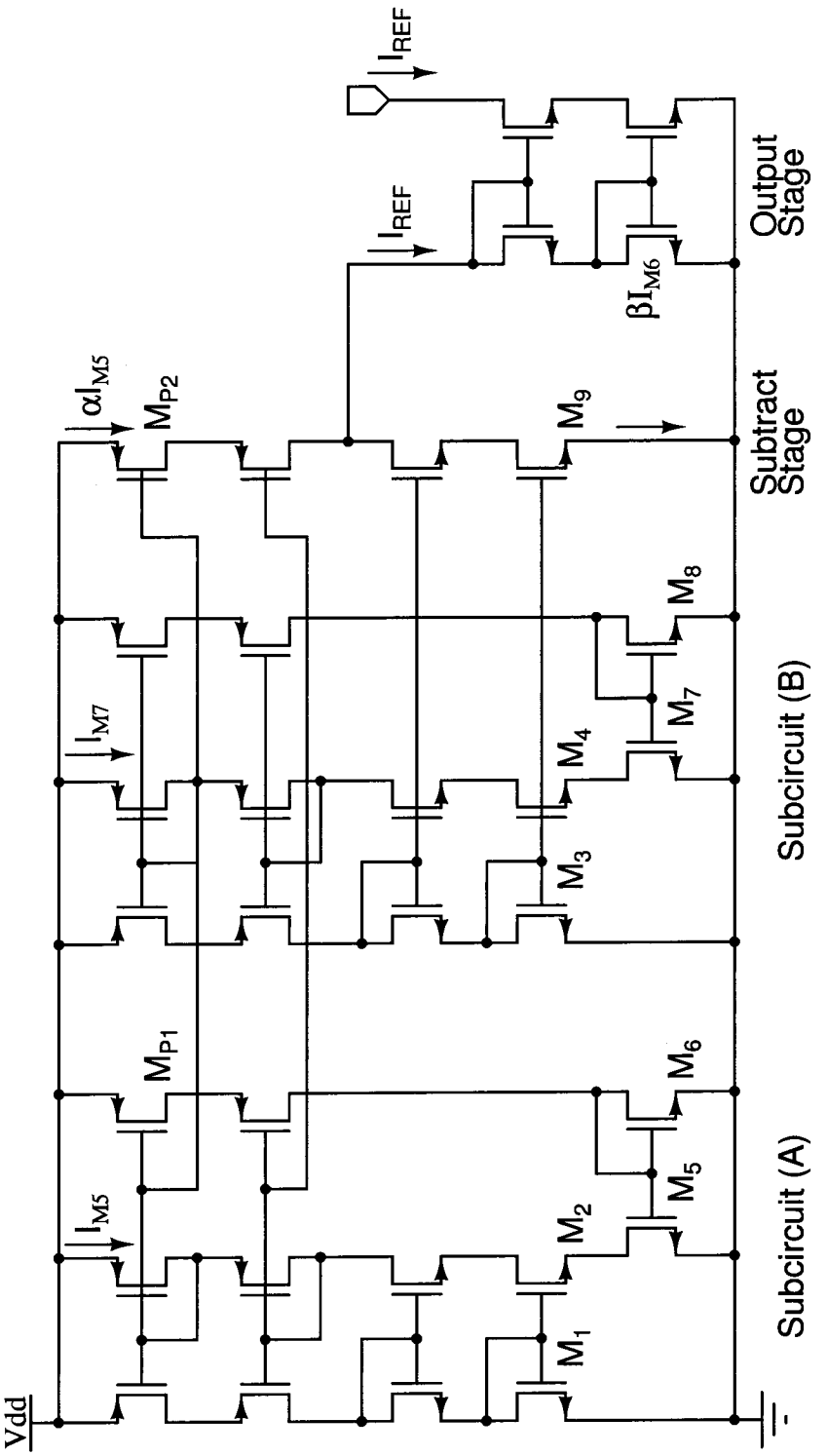

Figure 5.3: Schematic of proposed current reference

On the other hand, all other devices in Subcircuit (A) and Subcircuit (B) were selected so that $I_{M5} > I_{M7}$. Assume that area ratios of $M_{P1} : M_{P2}$ and $M_3 : M_9$ are $1 : \alpha$ and $1 : \beta$, respectively. Therefore, the drain currents of M_{P2} and M_9 become αI_{M5} and βI_{M7}, respectively. Thus, βI_{M7} is subtracted from αI_{M5}, and the resultant current I_{REF} given by

$$I_{REF} = \alpha I_{M5} - \beta I_{M7} \tag{5.22}$$

is mirrored to the output stage.Thus, by choosing proper values for α and β, the temperature dependence of I_{REF} can be eliminated.

5.3 Simulation results

The proposed current reference was designed and simulated in the 0.25 µm CMOS process. Following simulations are done to verify the performance of ultra-low power current reference.

- Temperature sweep.
  - The β-multiplier current subcircuits.
  - The full current reference.
- Corner simulation
- Power supply dependence

5.3.1 Temperature sweep

The β-multiplier current subcircuits

Figure 5.4 shows the simulated output current of the two current sources. The temperature coefficient of I_{M5} and I_{M6} at room temperature can be calculated as,

$$TC_A = \frac{1}{81.28\text{ nA}} \frac{87.2\text{ nA} - 76.4\text{ nA}}{10°\text{C}} \approx 1328\text{ ppm/°C} \tag{5.23}$$

and

$$TC_B = \frac{1}{49.18\text{ nA}} \frac{53.7\text{ nA} - 45.3\text{ nA}}{100°\text{C}} \approx 1708\text{ ppm/°C}, \tag{5.24}$$

respectively.

As discussed previously, both currents have a positive temperature coefficient, and the temperature coefficient decreases with an increase in the current. Thus, selecting the constants α and β in eq. (5.22) such that $\alpha : \beta = 1328 : 1708$, temperature dependence of I_{REF} can be compensated. Figure 5.5 shows the numerical calculation results of $(1328/1708)I_{M5} - I_{M6}$. The results prove that the temperature dependence of the resultant current is negligibly small. Thus, in the proposed design, the current mirror ratios M_{P1}:M_{P2} and M_4:M_9 were 31:24 and 1:1, respectively.

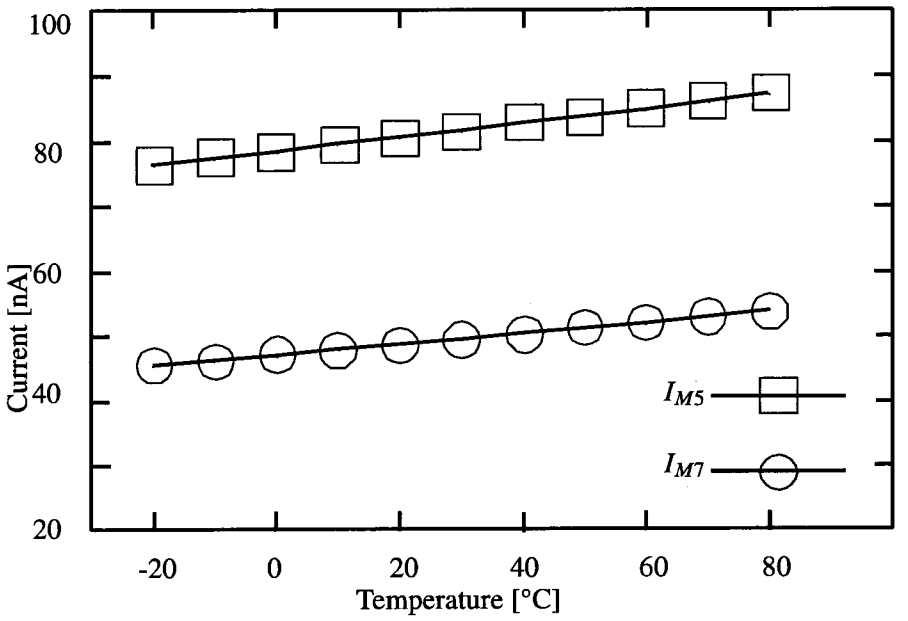

Figure 5.4: Simulated output currents of current source subcircuits

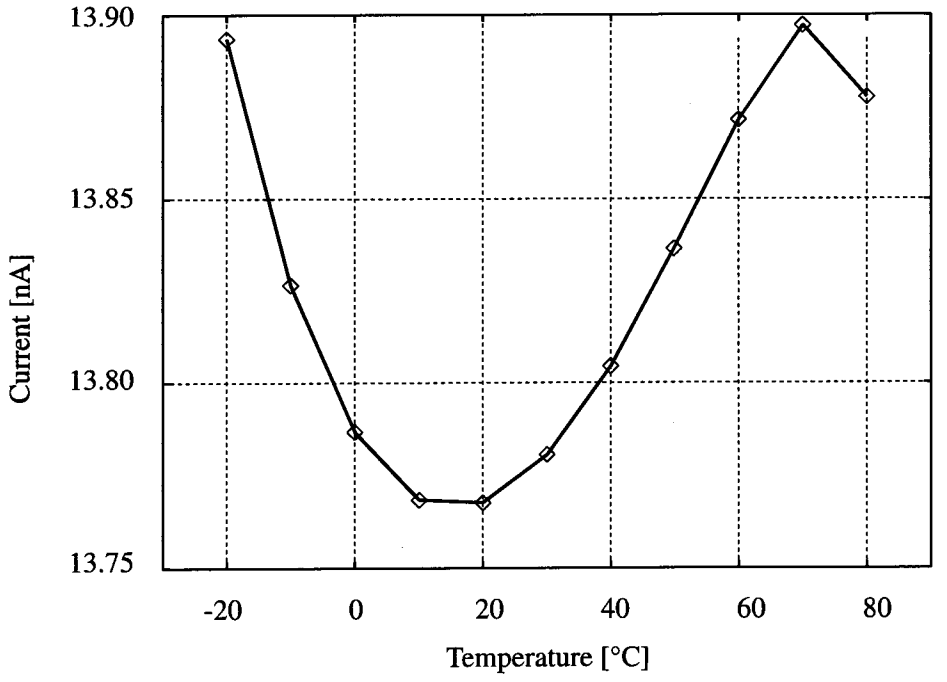

Figure 5.5: Numerical calculation results of $(1328/1708)I_{M5} - I_{M6}$

The full current reference

The temperature dependence of the output reference current I_{REF} is shown in Fig. 5.6. The worst case deviation of the output current in above temperature range is 0.13 nA (13.83 nA at -20 °C-

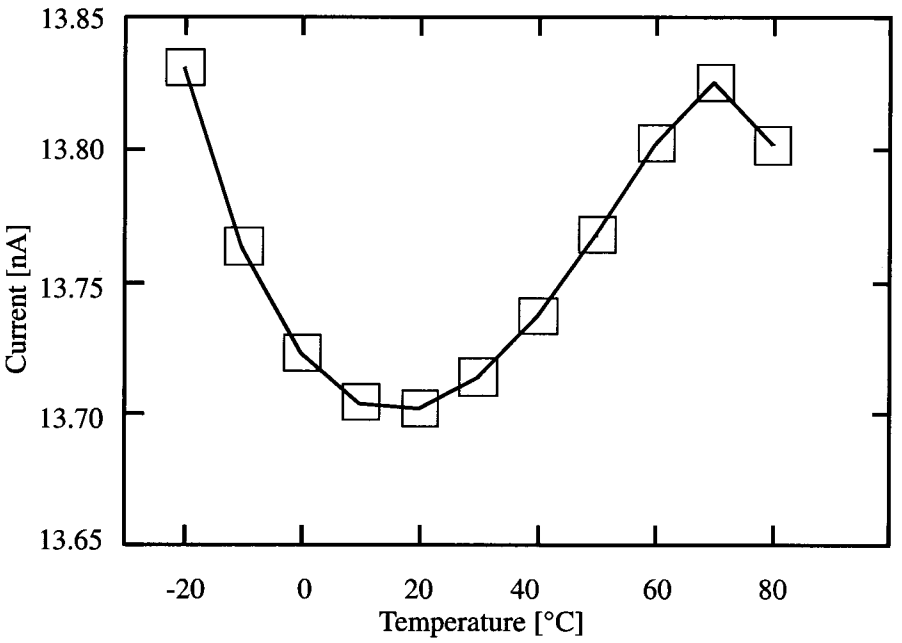

Figure 5.6: Simulated temperature dependence of the reference current

13.7 nA at 50 °C). Thus, the temperature coefficient of the reference current in the temperature range from −20 °C to 80 °C can be calculated as

$$TC = \frac{1}{13.71\ \text{nA}} \cdot \frac{13.83\ \text{nA} - 13.7\ \text{nA}}{100\ °\text{C}} \times 10^6 = 94.8\ \text{ppm/°C} \tag{5.25}$$

Figure 5.7 compiles the simulated results of supply current as a function of temperature. Due to the output currents of both current source subcircuits have positive temperature coefficients, the current consumption increase with the temperature. The average supply current is approximately 455 nA in the temperature range of −20 °C to 80 °C.

5.3.2 Corner simulation

We simulated the proposed circuit using different process corners to investigate the effect of process variation on the reference current. The results are shown in Fig. 5.8. The difference in I_{REF} at the process corners of TT, SF, and FS is negligible. In addition, I_{REF} at each process corner shows almost the same temperature dependence, because as seen from eq. (5.19), the temperature coefficient of I_{M5} and I_{M7} has little process dependence and could be seen as negligible. Therefore, the temperature coefficient of the reference current also has little process dependence and could be seen as negligible.

5.3.3 Power supply dependence

Figure 5.9 shows the power supply dependence of the reference current. As is clear from Fig. 5.9, the proposed current reference operates even at 2 V and this voltage could be reduced further by

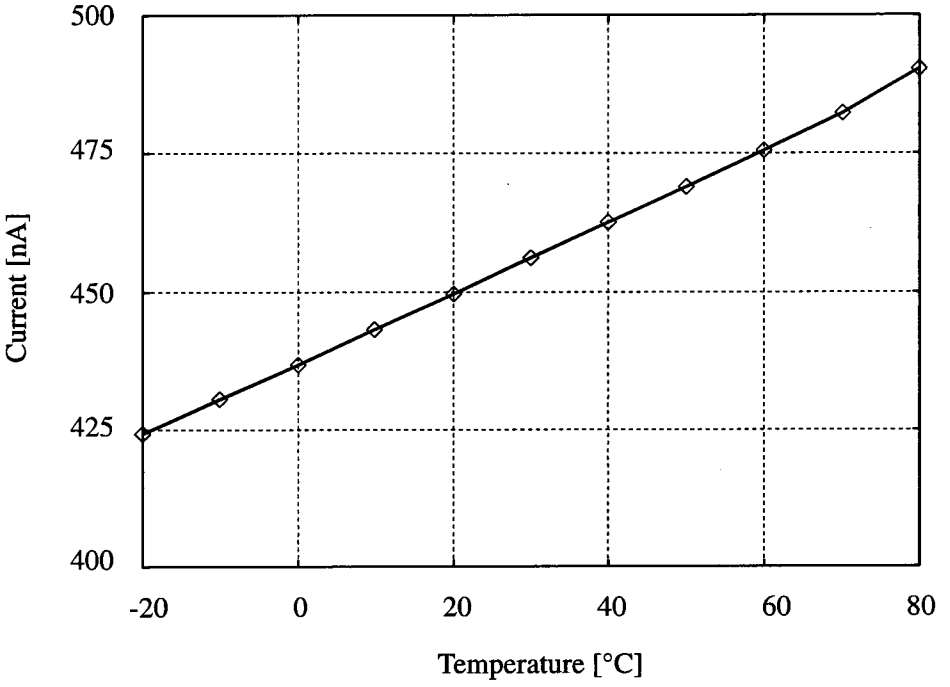

Figure 5.7: Power consumption

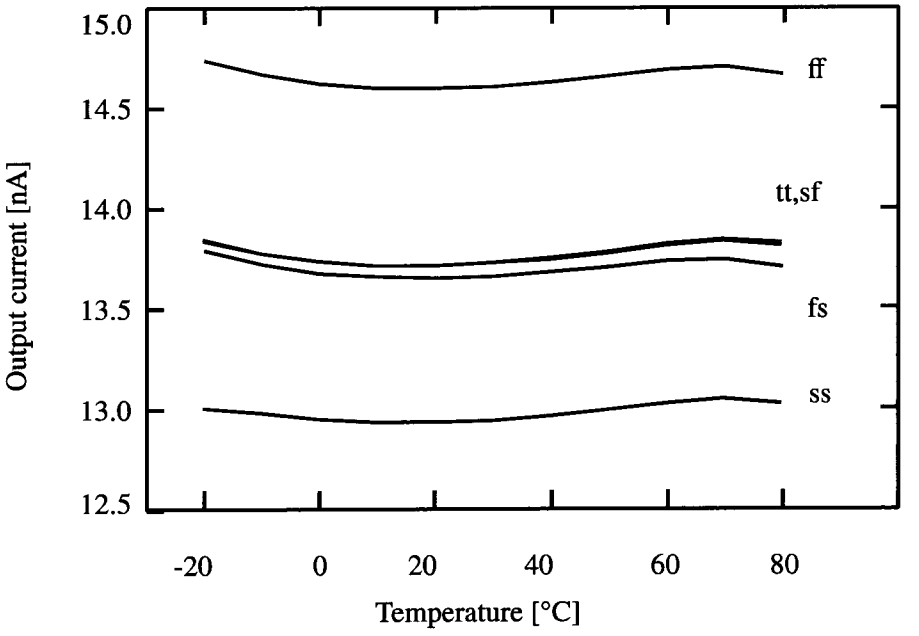

Figure 5.8: Simulated reference current in different process corners

using operation amplifiers instead of cascode current mirrors at the expense of power consumption.

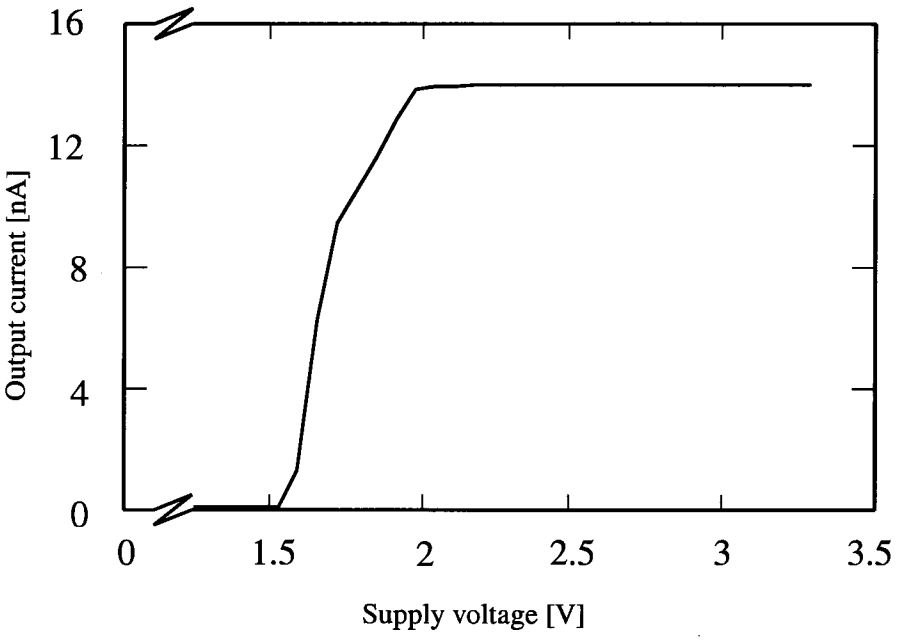

Figure 5.9: Power supply dependence of reference current

Table 5.1: Performance summary

	This Work	[4]	[5]
Process	0.25 μm	2 μm	0.35 μm
Temperature Range	−20 - 80 °C	−40 - 80 °C	0 - 80 °C
Temperate Coefficient	95 ppm/°C	1100 ppm/°C	520 ppm/°C
Power Consumption	0.9 μW	0.07 μW	1 μW
I_{REF}	13.7 nA	1 - 100 nA	96 nA

5.4 Comparison

Table 5.1 compares the performance of the current reference described in this research with that of previously published current references. The current reference proposed in this research shows the best performance in temperature dependence. Although the current reference circuit [4] has demonstrated low power consumption, our design is 10 times superior in temperature dependence.

5.5 Summary

In this chapter, we presented a novel ultra-low-power current reference using subthreshold circuits. The proposed circuit uses only CMOS devices; therefore, it can be implemented in the standard CMOS process without using parasitic bipolar transistors or resistors. The proposed circuit is designed and simulated in the 0.25 μm CMOS process. The operation principle and the simulation results are presented. The simulation results show that the output reference current I_{REF} is approximately 13.7 nA at room temperature, and that the temperature coefficient of I_{REF} is smaller than

100 ppm/°C for the temperature range from −20 °C to 80 °C. The average power consumption is 0.9 μW. Furthermore, the proposed current reference shows temperature independent characteristics in all process corners. This implies that the proposed circuit is ideal to be used as a current reference to compensate for temperate dependence in ultra-low-power, subthreshold designs.

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Chapter 6

Conclusion

6.1 Summary

In Chapter 3, we presented an area efficient CMOS bandgap reference with switched-current and current-memory technique. The proposed circuit uses only one parasitic bipolar transistor to generate reference voltage so that significant area reduction is achieved. The circuit produces an output of about 650 mV, and simulated results show that the temperature coefficient of output is less than 10.7 ppm/°C in the temperature range from 0 °C to 100 °C. The average current consumption is about 49.5 μA in the above temperature range. Furthermore, output can be set to almost any value. The circuit was designed and simulated in 0.25μm CMOS technology. The layout occupies less than 0.011 mm^2 (100 μm × 110 μm).

In chapter 4, we proposed an area efficient, low power, fractional CMOS bandgap reference utilizing switched-current and current-memory techniques. The proposed circuit uses only one parasitic bipolar transistor and built-in current source to generate reference voltage. Therefore significant area and power reduction is achieved, and bipolar transistor device mismatch is eliminated. In addition, output reference voltage can be set to almost any value. The proposed circuit is designed and simulated in 0.18 μm CMOS process, and simulation results are presented. With a 1.6 V supply, the reference produces an output of about 628.5 mV, and simulated results show that the temperature coefficient of output is less than 13.5 ppm/°C in the temperature range from 0 °C to 100 °C. The average current consumption is about 8.5 μA in the above temperature range. The core circuit, including current source, opamp, current mirrors and switched capacitor filters, occupies less than 0.0064 mm^2 (80 μm ×80 μm).

In chapter 5, we proposed a novel temperature-compensated, ultra-low-power current reference based on two β-multipliers whose resistors are replaced by nMOS devices operated in the deep triode region. The circuit, designed by a 0.25 μm CMOS process, produces an output reference current of 13.7 nA at room temperature. Simulated results show that the temperature coefficient of the output is less than 100 ppm/°C in the range from −20 °C to 80 °C and the average power dissipation is 0.9 μW.

6.2 Further research and recommendations

There are many avenues for further research arising from this work. The following are among the most salient:

- The output voltages of the bandgap references presented in chapter 3 and chapter 4 are highly suffered from switched noise. Some spikes of few millivolts can be seen in the output when clock changes, and a drift in the output can be observed between different clock spaces, thus it may limit the applicability of the proposed design. Therefore, further research should be carried out to eliminate the effects of charge injection and clock feedthrough, so that a smooth and constant output reference can be achieved.

- The minimum required supply voltage for the presented voltage references can be calculated as $V_{BE} + 2V_{OD,P}$, thus the proposed designs can be modified to operate in supply voltages less than 1 V. In that case, the main challenge is to design a differential amplifier, which can be operate in less than 1 V supply voltage.

- Since the voltage references presented in this work uses switched control techniques, the operational amplifier offset cancellation methods can be included, so that to eliminate the effects of offset voltage.

- The mismatch of the transistors operating in subthreshold region is comparably higher than the transistors operating in strong inversion region. Thus, for the current reference presented in Chapter 5, the dependence of the output on process and device mismatch should be further investigated. For an example, this can be done by using Monte-Carlo simulation and mismatch models. However, the mismatch model was not included in spice parameters used in this work. Thus, Monte-Carlo simulation was not carried out.

Appendix A

Opamp Offset due to devices mismatch

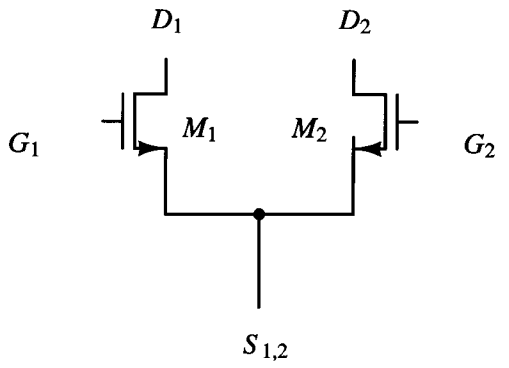

Figure A.1: Source coupled differential pair

Mismatch is the differential performance of two or more devices on a single integrated circuit (IC), and device mismatches plays an important role in the design of accurate analog circuits. In CMOS process, nominally-identical devices suffer from a finite mismatches due to uncertainties in each step of the manufacturing process. Consider the source coupled differential nMOS pair shown in Fig.A.1. As shown in Fig. A.2, the gate dimensions of nMOS transistors suffer from random, microscopic variations and hence mismatches between the equivalent lengths and widths of two transistors. On the other hand, MOS devices suffer from threshold voltage mismatch due to doping levels, which vary randomly from device to device, in the channel and the gate.

One of the most important aspect of differential amplifiers is the input offset voltage, resulting from mismatches in threshold voltage, geometry and load resistance. For an ideal differential amplifier, when the input terminals are connected together, the output voltage is at a desired quiescent point. However, in practically, for a differential amplifier, the output voltage is difference from the ideal output voltage when the input terminals are connected together. By dividing this voltage different by the differential voltage gain of the differential amplifier, the input offset voltage can be calculated.

The input offset voltage of a simple differential amplifier can be calculated by using Fig.A.3. Assume that both the input nMOS transistors and load resistors suffer from mismatch, thus for $V_{out} = 0$, condition $I_{D1}R_1 = I_{D2}R_2$ should be satisfied. Thus assuming $I_{D1} = I_D$ and $I_{D2} = I_D + \Delta I_D$,

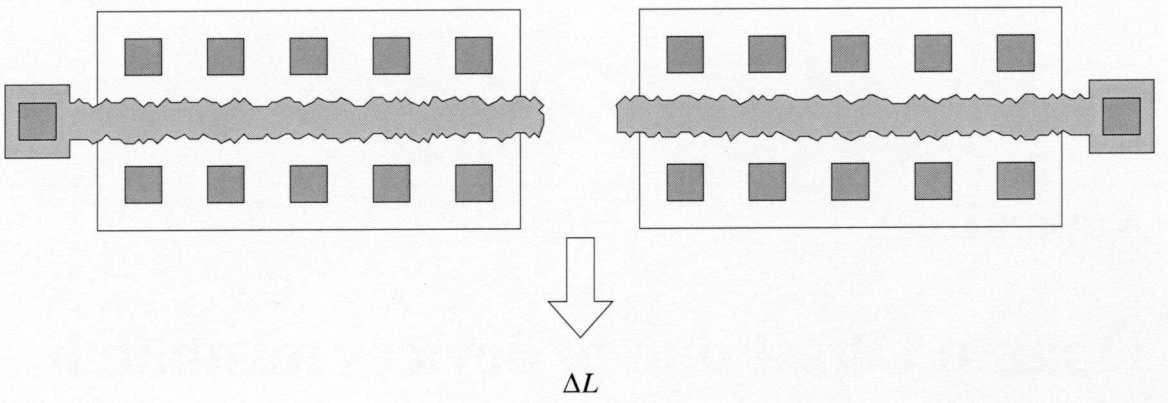

Figure A.2: Random mismatches due to microscopic variation in device dimensions.

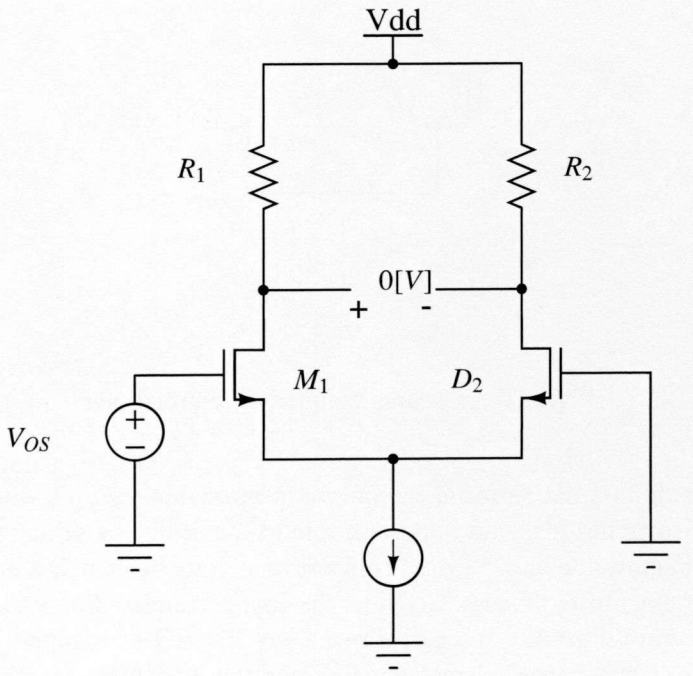

Figure A.3: Determination of differential amplifier input offset voltage

the input offset voltage can be given by,

$$
\begin{aligned}
V_{OS,in} &= V_{GS1} - V_{GS2} \\
&= V_{THN1} + \sqrt{\frac{2I_{D1}}{\beta_1}} - V_{THN2} - \sqrt{\frac{2I_{D2}}{\beta_2}} && \text{(A.1)} \\
&= \sqrt{2}\left\{\sqrt{\frac{I_D}{\beta}} - \sqrt{\frac{I_D + \Delta I_D}{\beta + \Delta\beta}}\right\} - \Delta V_{TH} && \text{(A.2)} \\
&= \sqrt{2}\sqrt{\frac{I_D}{\beta}}\left\{1 - \sqrt{\frac{1 + \frac{\Delta I_D}{I_D}}{1 + \frac{\Delta\beta}{\beta}}}\right\} && \text{(A.3)}
\end{aligned}
$$

where the device mismatches are defined as, $V_{TH1} = V_{TH}$, $V_{TH2} = V_{TH} + \Delta V_{TH}$; $\beta_1 = \beta = \mu_n C_{OX}(W/L)$, $\beta_2 = \beta + \Delta\beta$, and for simplicity, $\lambda = \gamma = 0$. Assuming $\Delta I_D/I_D$, $\Delta\beta/\beta \ll 1$, (A.3) can be reduced to

$$\begin{aligned} V_{OS,in} &= \sqrt{\frac{2I_D}{\beta}}\left\{1-\left(1+\frac{\Delta I_D}{2I_D}\right)\left[1-\frac{\Delta\beta}{2\beta}\right]\right\} - \Delta V_{TH} \\ &= \sqrt{\frac{2I_D}{\beta}}\left[\frac{-\Delta I_D}{2I_D}+\frac{\Delta\beta}{2\beta}\right] - \Delta V_{TH} \end{aligned} \tag{A.4}$$

Hence, $I_D R_D = (I_D+\Delta I_D)(R_D+\Delta R_D) \approx I_D R_D + R_D\Delta I_D + I_D\Delta R_D$, consequently $\Delta I_D/I_D \approx -\Delta R_D/R_D$, and

$$V_{OS,in} = \frac{1}{2}\sqrt{\frac{2I_D}{\beta}}\left[\frac{\Delta R_D}{R_D}+\frac{\Delta\beta}{\beta}\right] - \Delta V_{TH} \tag{A.5}$$

notice that the square-root quantity in (A.5) is approximately equal to the equilibrium overdrive voltage of each transistor, $V_{GS} - V_{TH}$. Thus (A.5) can be rewritten as

$$V_{OS,in} = \frac{V_{GS}-V_{TH}}{2}\left[\frac{\Delta R_D}{R_D}+\frac{\Delta\beta}{\beta}\right] - \Delta V_{TH} \tag{A.6}$$

Since the mismatches are independent statistical variables, (A.5) should be expressed as square quantities as follows.

$$V_{OS,in}^2 = \left(\frac{V_{GS}-V_{TH}}{2}\right)^2\left\{\left(\frac{\Delta R_D}{R_D}\right)^2+\left[\frac{\Delta\beta}{\beta}\right]^2\right\} + \Delta V_{TH}^2 \tag{A.7}$$

From (A.7), it is clear that operational amplifier input offset voltage resulting from load resistor mismatch and transistor dimension mismatch can be reduced by designing with a small overdrive. Furthermore, the threshold voltage mismatch is directly appeared in the input offset voltage. Thus, the threshold voltage mismatch must be reduced using layout techniques such as common centroid, and it is desirable to increase the transistor width, such that minimize to threshold mismatch.

Appendix B

Switched capacitor filters

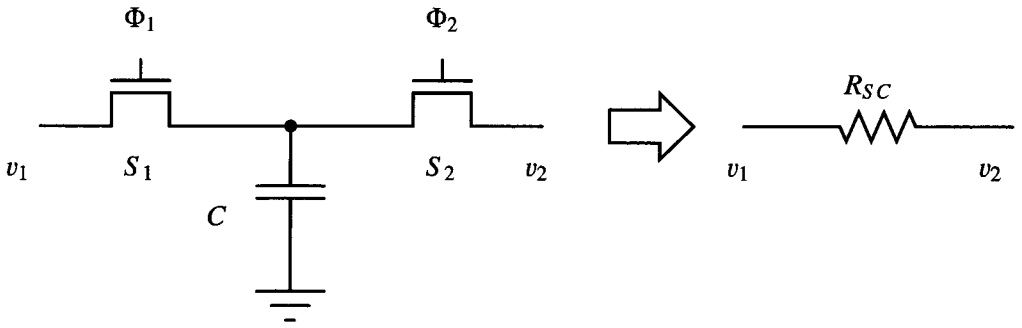

Figure B.1: Switched capacitor resistor.

The switched capacitor resistor circuit is shown in Fig. B.1 [1]. The clock signals Φ_1 and Φ_2 are non-overlapping clock signals with frequency f_{clk} and period T. When Φ_1 is high, switch S_1 becomes closed, the capacitor C is charged to v_1. Assume that the charge q_1 stored on the capacitor during this period. Thus q_1 can be written as

$$q_1 = Cv_1, \tag{B.1}$$

while if S_1 is opened and S_2 is closed, the charge stored on the C is

$$q_2 = Cv_2 \tag{B.2}$$

If v_1 and v_2 are not equal, then charge given by $q_1 - q_2$, which can be given by

$$q_1 - q_2 = C(v_1 - v_2) \tag{B.3}$$

is transfered from v_1 to v_2 during each interval T. Assume that the v_1 and v_2 change slowly compared to f_{clk}, then the average current flowed in an interval T is given by

$$\begin{aligned} I_{avg} &= \frac{C(v_1 - v_2)}{T} \\ &= \frac{v_1 - v_2}{R_{sc}} \end{aligned} \tag{B.4}$$

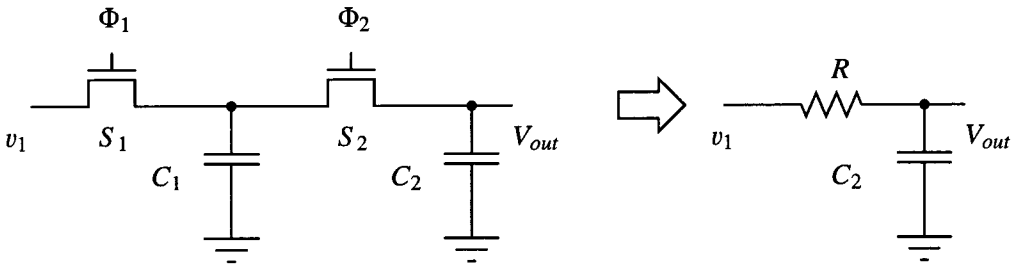

Figure B.2: Switched capacitor filter.

where the effective resistance of the switched-capacitor circuit is given by

$$R_{sc} = \frac{T}{C} = \frac{1}{Cf_{clk}} \tag{B.5}$$

Figure B.2 shown the switched capacitor filter which is implemented by switched capacitor resister shown in Fig. B.1. The time constant, RC, of switched capacitor filter shown in B.2 therefore can be written as

$$RC = \frac{C_2}{C_1}\frac{1}{f_{clk}}. \tag{B.6}$$

Appendix C

CMOS operation regions

The drain current of the nMOS transistor is given by the difference between the forward current ,I_F, and reverse current,I_R , as follows.

$$I_D = I_F - I_R \tag{C.1}$$

Values of I_F and I_R are given by [2]

$$I_F = I_S \ln^2\left[1 + \exp\left\{\frac{\frac{(V_G - V_{T0})}{\eta} - V_S}{2V_T}\right\}\right] \tag{C.2}$$

$$I_R = I_S \ln^2\left[1 + \exp\left\{\frac{\frac{(V_G - V_{T0})}{\eta} - V_D}{2V_T}\right\}\right] \tag{C.3}$$

where $V_T = \frac{kT}{q}$ is the thermal voltage, η is the subthreshold slope factor given by

$$\eta = 1 + \frac{C_{dep}}{C_{OX}} \tag{C.4}$$

and

$$I_S = \frac{W}{L} \cdot 2\mu\eta C_{OX} V_T^2 \tag{C.5}$$

This model covers all regions of normal MOS transistor operation. Note that I_F depends only on V_G and V_S , and on the other hand, I_R depends only on V_G and V_D.

The expressions for I_F and I_R can be simplified to an exponential form in weak inversion and a quadratic form in strong inversion as follows.

$$I_{F(R)} \begin{cases} I_S \exp\left[\dfrac{\frac{(V_G - V_{T0})}{\eta} - V_{S(D)}}{V_T}\right] & \text{for } V_G < V_{T0} + \eta V_{S(D)} \\ \dfrac{W}{L} \cdot \dfrac{\mu\eta C_{OX}}{2}\left\{\dfrac{(V_G - V_{T0})}{\eta} - V_{S(D)}\right\}^2 & \text{for } V_G > V_{T0} + \eta V_{S(D)} \end{cases} \tag{C.6}$$

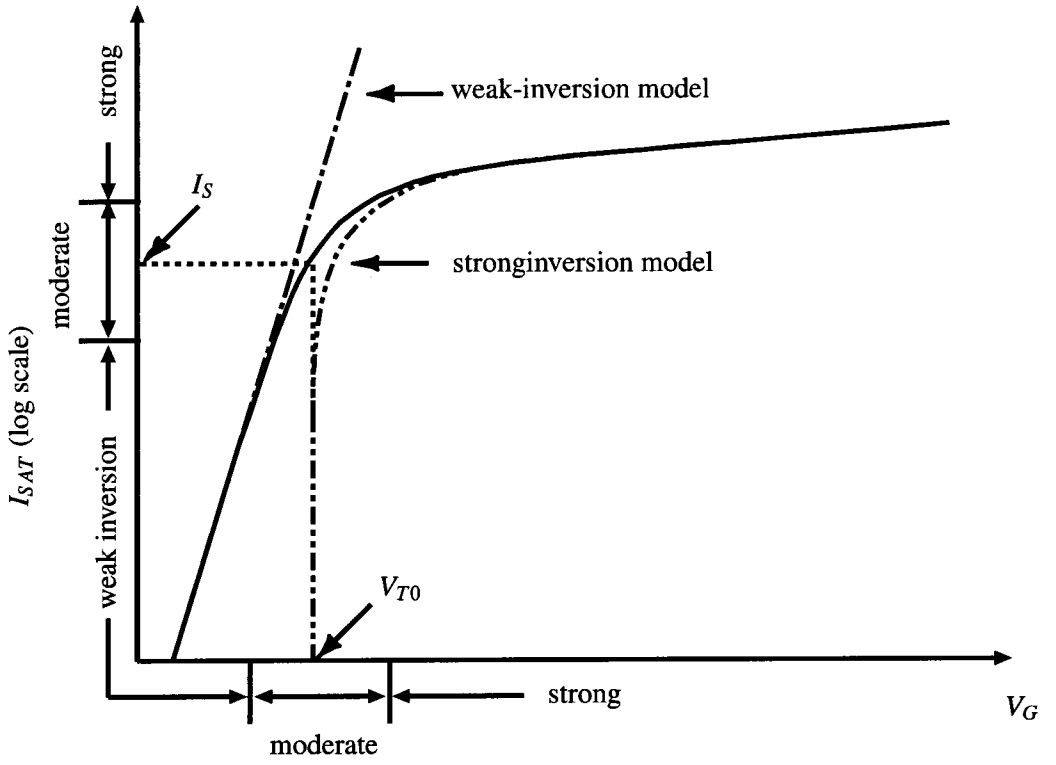

Figure C.1: V_G vs I_D

Equations C.1 and C.6 can be plotted as shown in Fig. C.1. The operation regions of the transistor, which are determined by the magnitudes of I_F and I_R, can be explained by using the plane shown in Fig. C.2.

For simplicity, assume that the $I_{F,R} = I_S$ represent the limit between weak and strong inversion. If $I_F/I_S > 1$ and $I_R/I_S > 1$, then both components are in strong inversion and the whole channel is strongly inverted. Therefore, the transistor is operated in linear region.

If $I_F/I_S > 1$ but $I_R/I_S < 1$, the reverse component is negligible and the current does not increase with the drain voltage. In this condition, the transistor is said to be in forward saturation.

If $I_F/I_S < 1$ but $I_R/I_S > 1$, the the forward component is negligible and the current does not increase with the source voltage. The transistor is still in strong inversion, but in reverse saturation.

If $I_F/I_S < 1$ and $I_R/I_S < 1$, the whole channel is only weakly inverted. Thus the transistor is said to operate in weak inversion region.

Therefore, the level of inversion of the transistor can be characterized by using the inversion coefficient, defined as

$$IC = max\left(\frac{I_F}{I_S}, \frac{I_R}{I_S}\right) \tag{C.7}$$

The transistor operates in weak inversion region for $IC \ll 1$, in strong inversion for $IC \gg 1$, and in moderate inversion region for $IC \approx 1$.

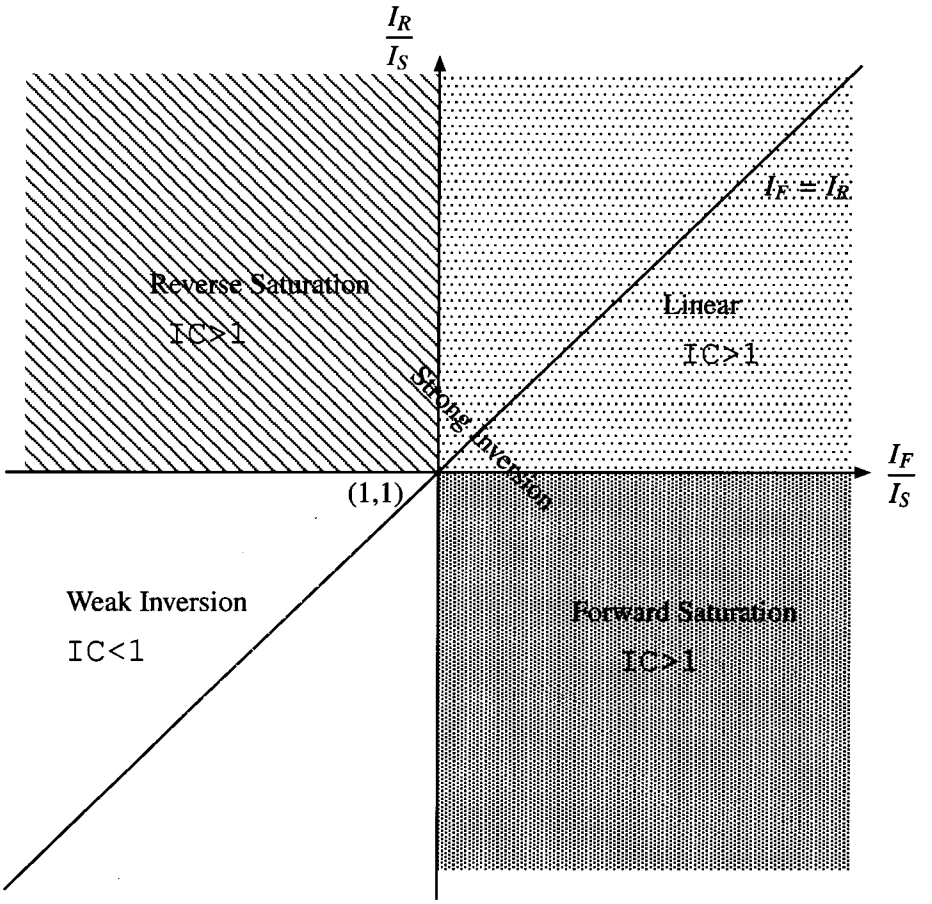

Figure C.2: Operation regions of a MOS transistor

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Research achievement

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