CMOS Voltage Reference Based on Gate Work Function Differences in Poly-Si Controlled by Conductivity Type and Impurity Concentration

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***Abstract*—A new CMOS voltage reference circuit consisting of two pairs of transistors is presented. One pair exhibits a threshold voltage difference with a negative temperature coefficient (−0.49 mV/°C), while the other exhibits a positive temperature coefficient (+0.17 mV/°C). The circuit was robust to process variations and exhibited excellent temperature independence and stable output voltage. Aside from conductivity type and impurity concentrations of gate electrodes, transistors in the pairs were identical, meaning that the system was robust with respect to process fluctuations. Measurements of the voltage reference circuit without trimming adjustments revealed that it had excellent output voltage reproducibility of within ±2%, low temperature coefficient of less than 80 ppm/°C, and low current consumption of 0.6 μA.**

***Index Terms*—Low voltage, poly Si, voltage reference, work function differences.**

I. Introduction

TRADITIONAL voltage reference circuits can be classified into five different categories: bandgap reference circuits, which are based on bipolar integrated circuits and can be applied to CMOS circuits [1]–[4]; circuits based on threshold voltage ($V_{\rm th}$) differences in MOS transistors [5]–[10]; MOS transistor circuits in which threshold voltage and mobility temperature dependencies are compensated for [11], [12]; current mode [13]; and beta multiplier (MOS based) [14]–[16]. Recent state of the art system LSIs, however, demand the use of voltage references which operate at low voltages, are robust to process fluctuations, exhibit low electrical current consumption, can be integrated with standard CMOS technologies, and allow flexible voltage adjustment [17]–[21]. Although bandgap reference circuits are extremely accurate, electrical current consumption is generally larger than MOS-based voltage references. MOS-transistor-based voltage references, however, are susceptible to process fluctuations. Recently, low-power bandgap references have been studied [19].

A voltage reference is proposed that uses pairs of MOS transistors with positive and negative temperature coefficients. The circuit is robust to process fluctuations because the reference voltage is derived from the difference in the work functions of the transistors, which are functions of gate electrode conductivity type and impurity concentration. Combination of positive and negative temperature coefficient components is a method for controlling temperature characteristics. Previous MOS transistor voltage references based on threshold voltage differences also utilized differences in the gate work functions of transistor pairs [7], [8], but without complementary temperature coefficients, accurate voltage references are not easily constructed [8]. Other attempts have used metal gates, which are not suitable to conventional CMOS processes [7]. A new CMOS voltage reference consisting of two pairs of transistors is presented. Theory, circuit implementations, and experimental results are also presented.

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II. Theory of Work Function Difference

Threshold voltage $V_{\rm th}$ of MOS transistors (MOSFETs) is described as

$$V_{\rm th} = V_{\rm fb} + \frac{qN_aW_m}{C_{\rm ox}} + \phi_s \tag{1}$$

where

$$V_{\rm fb} = \phi_{ms} - \frac{Q}{C_{\rm ox}} = (\psi_m - \psi_s) - \frac{Q}{C_{\rm ox}}, \quad W_m = \sqrt{\frac{2\varepsilon_{\rm si}\cdot\phi_s}{qN_a}}.$$

$V_{\rm fb}$ is flat-band voltage, N_a is bulk dopant density, W_m is depletion layer thickness, $C_{\rm ox}$ is gate-oxide capacitance per unit area, ψ_m is the metal work function, ψ_s is surface potential, Q is the gate-oxide charge per unit area, q is the magnitude of electronic charge, and ε_{Si} is the dielectric constant of Si and $\phi s = 2\phi_b$ under conditions of strong inversion. Then $V_{\rm th}$ can be expressed as

$$V_{\rm th} = \psi_m - \psi_s - \frac{Q}{C_{\rm ox}} + \frac{2\sqrt{\varepsilon_{\rm si}\cdot q\cdot N_a\cdot\phi_b}}{C_{\rm ox}} + 2\phi_b \tag{2}$$

where

$$\psi_m = \frac{1}{q}\left(\chi_{\rm polySi} + \frac{Eg_{\rm polySi}}{2}\right) + \phi_{\rm gate}$$

$$\psi_s = \frac{1}{q}\left(\chi_{\rm Si} + \frac{Eg_{\rm Si}}{2}\right) + \phi_b.$$

$\chi_{\rm poly\text{-}Si}$ and $\chi_{\rm Si}$ are electron affinities of poly-Si and Si, $Eg_{\rm poly\text{-}Si}$ and $Eg_{\rm Si}$ are bandgaps of poly-Si and Si, respectively. $\phi_{\rm gate}$ is the potential difference between the Fermi

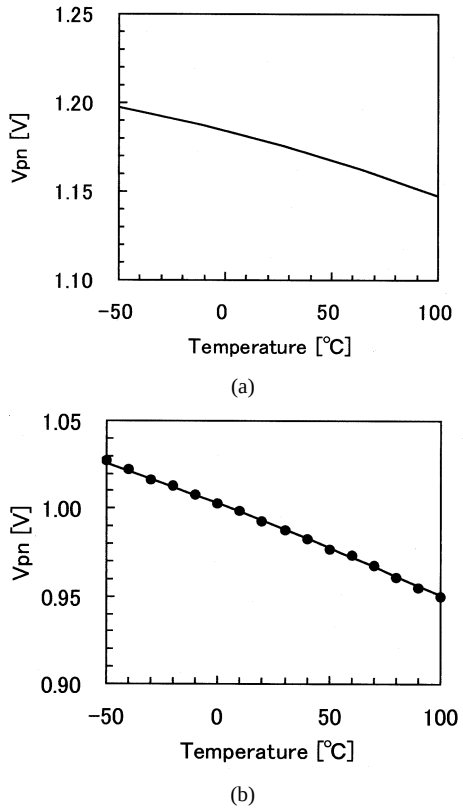

Fig. 1. $V_{\rm pn}$ as a function of temperature. (a) Simulation results based on Seto's model. (b) Experimental results.

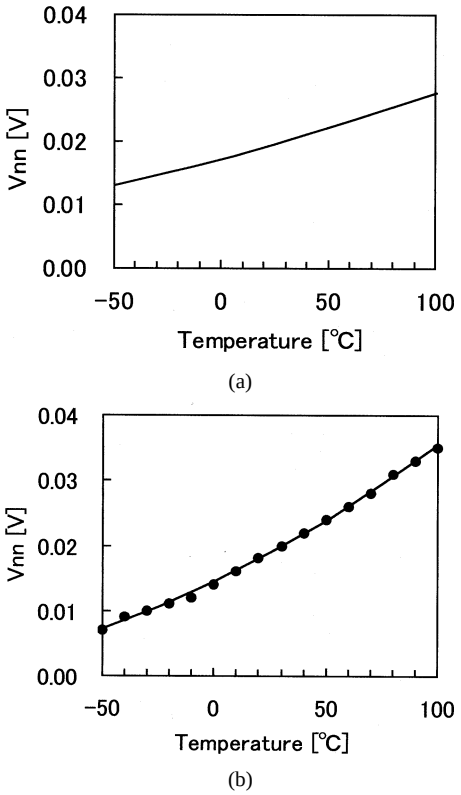

Fig. 2. $V_{\rm nn}$ as a function of temperature. (a) Simulation results based on Seto's model. (b) Experimental results.

level E_f of poly-Si gates and intrinsic Fermi level E_i, and ϕ_b is the potential difference between the Fermi level E_f of Si and intrinsic Fermi level E_i. In this paper, the poly-Si gate work function ψ_m is regarded as a function of gate potential difference $\phi_{\rm gate}$.

For a pair of MOS transistors with gates of different conductivity types or different impurity concentrations, all of the terms on the right-hand side (RHS) of (2) are equal except for ψ_m terms, because substrate conditions are the same for both transistors. Thus, the difference in $V_{\rm th}(\Delta V_{\rm th})$ between two transistors M1 and M2 is given by the difference in gate work function, as shown in (3). This contrasts with previously constructed MOS-based voltage references [5], [6], [8]–[10]

$$\begin{aligned}\Delta V_{\rm th} &= V_{\rm th_{M1}} - V_{\rm th_{M2}} = \psi_{m\rm M1} - \psi_{m\rm M2} \\ &= \left[\frac{1}{q}\left(\chi_{\rm polySi} + \frac{Eg_{\rm polySi}}{2}\right) + \phi{\rm gate}_{\rm M1}\right] \\ &\quad - \left[\frac{1}{q}\left(\chi_{\rm polySi} + \frac{Eg_{\rm polySi}}{2}\right) + \phi{\rm gate}_{\rm M2}\right] \\ &= \phi_{\rm gateM1} - \phi_{\rm gateM2} \end{aligned} \tag{3}$$

where

$$\phi{\rm gate}_n = -\frac{(E_{fn} - E_i)}{q} = -\frac{kT}{q}\cdot\ln\frac{N_n}{N_i} \tag{4}$$

for n-type gates and

$$\phi{\rm gate}_p = -\frac{(E_i - E_{fp})}{q} = \frac{kT}{q}\cdot\ln\frac{N_p}{N_i} \tag{5}$$

for p-type gates. $N_{\rm n}$ and $N_{\rm p}$ are free carrier concentrations of n-type and p-type doped gates, respectively.

In the derivations of (4) and (5), gates with impurity concentrations less than degenerations levels were assumed crystalline silicon so that the Fermi–Dirac distribution could be applied.

For a pair of transistors with gates of opposite conductivity types, having impurity concentrations of p^+ (B^+: 4×10^{19} cm^{-3}) and n^+ (P^+: 5×10^{20} cm^{-3}), the $V_{\rm th}$ difference $V_{\rm pn}$ between the p^+ and n^+ gate transistors is given by

$$\begin{aligned} V_{\rm pn} &= \phi{\rm gate}_{\rm p^+} - \phi{\rm gate}_{N^+} \\ &= \frac{kT}{q}\cdot\ln\frac{N_{\rm p+}}{N_i} - \left(-\frac{kT}{q}\cdot\ln\frac{N_{\rm n+}}{N_i}\right) \\ &= \frac{kT}{q}\cdot\ln\frac{N_{\rm p+}\cdot N_{\rm n+}}{N_i^2}. \end{aligned} \tag{6}$$

Simulation results using free carrier concentrations $N_{\rm p+}$ and $N_{\rm n+}$ derived from Seto's model [22] are shown in Fig. 1(a). Thus, $V_{\rm pn}$ exhibits a negative primary temperature coefficient together with a small negative secondary temperature coefficient due to the strong temperature dependence of N_i. Fig. 1(b) shows experimental measurements of $V_{\rm pn}$ as a function of temperature, which is well fitted by a quadratic regression equation given by

$$V_{\rm pn} = -4.6\times10^{-7}\times T^2 - 4.9\times10^{-4}\times T + 1.0. \tag{7}$$

Differences in $V_{\rm pn}$ between simulation and experiment may originate from both inaccurate estimations of active impurity concentrations and simplicity of the model used.

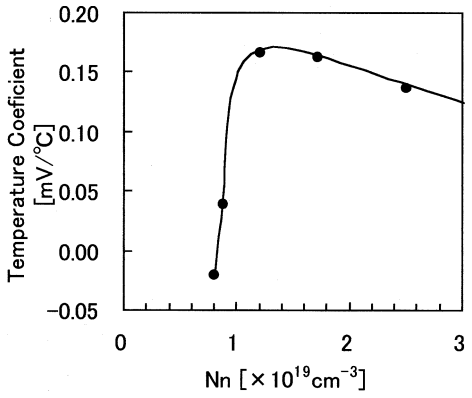

Fig. 3. $V_{\rm nn}$ primary temperature coefficient as a function of impurity concentration $N_{\rm n}$.

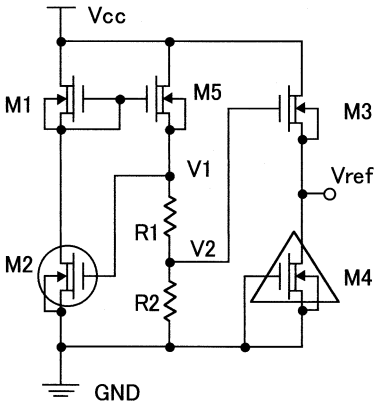

Fig. 4. Basic N-channel MOSFETs voltage reference. Circles indicate p^+ gates, triangles indicate n^- gates, all others are n^+ gate.

For a pair of transistors with gates of the same conductivity type, having gate impurity concentrations of n^- (P^+: 1.7×10^{19} cm^{-3}) and n^+ (P^+: 5×10^{20} cm^{-3}), the $V_{\rm th}$ difference $V_{\rm nn}$ between the n^- and n^+ gate transistors is given by

$$\begin{aligned} V_{\rm nn} &= \phi{\rm gate}_{N^-} - \phi{\rm gate}_{N^+} \\ &= -\frac{kT}{q} \cdot \ln \frac{N_{\rm n-}}{N_i} - \left(-\frac{kT}{q} \cdot \ln \frac{N_{\rm n+}}{N_i} \right) \\ &= \frac{kT}{q} \cdot \ln \frac{N_{\rm n+}}{N_{\rm n-}}. \end{aligned} \tag{8}$$

Both simulation and experimental determinations of the temperature dependence of $V_{\rm nn}$ show positive primary temperature coefficients and small positive secondary temperature coefficients, as shown in Fig. 2. The data is well fitted by a quadratic regression equation

$$V_{\rm nn} = 4.4 \times 10^{-7} \times T^2 + 1.7 \times 10^{-4} \times T + 1.4 \times 10^{-2}. \tag{9}$$

Primary temperature characteristics of $V_{\rm nn}$ depend on the impurity concentration of the n^- gate. Fig. 3 shows measurements of temperature coefficient versus impurity concentration of the gate electrode. Note that temperature coefficient levels off around 1.4×10^{19} cm^{-3}, which is used to make the voltage reference robust with respect to process fluctuations.

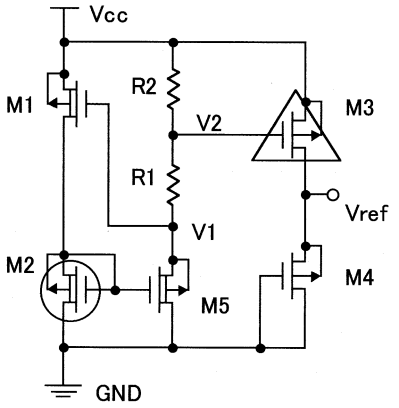

Fig. 5. P-channel MOSFETs voltage reference on a P-type substrate.

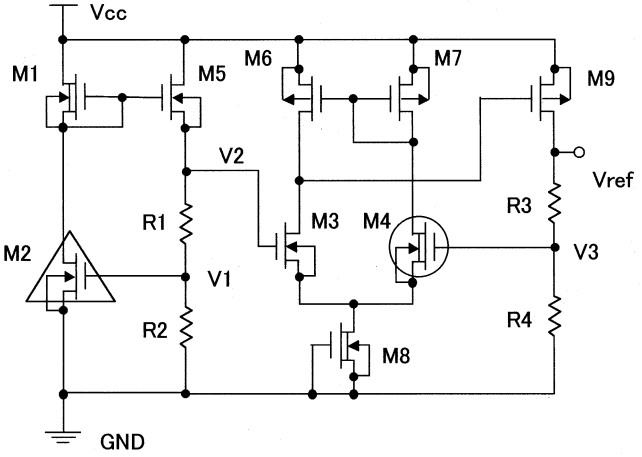

Fig. 6. Voltage reference with opamp.

III. Voltage Reference

From the primary temperature coefficients of $V_{\rm pn} = -0.49$ mV/°C and $V_{\rm nn} = 0.17$ mV/°C given in (7) and (9), it is evident that $V_{\rm pn}$ and $V_{\rm nn}$ could be combined in such a way that the primary temperature coefficient of a voltage reference ($V_{\rm ref}$) cancels out, giving

$$V_{\rm ref} = \frac{0.17}{0.49} \times V_{\rm pn} + V_{\rm nn} = 2.8 \times 10^{-7} \times T^2 + 0.36. \tag{10}$$

The remaining secondary coefficient of 2.8×10^{-7} is equivalent to 18 μV/°C over the temperature range of −50 °C–100 °C.

In this section, a circuit that utilizes the difference between work functions, that is, differences in $V_{\rm th}$, is described. For pairs of transistors, M1 and M2, driven by the same current and operating at saturation, the following equation holds:

$$\begin{aligned} I_{\rm dsat_{M1}} - I_{\rm dsat_{M2}} &= \tfrac{1}{2} C_{\rm ox_{M1}} \cdot \mu_{\rm M1} \cdot \frac{W_{\rm M1}}{L_{\rm M1}} (V_{\rm gs_{M1}} - V_{\rm th_{M1}})^2 \\ &\quad - \frac{1}{2} C_{\rm ox_{M2}} \cdot \mu_{\rm M2} \cdot \frac{W_{\rm M2}}{L_{\rm M2}} (V_{\rm gs_{M2}} - V_{\rm th_{M2}})^2 = 0. \end{aligned} \tag{11}$$

Matching the geometries of the transistors M1 and M2 gives

$$C_{\rm ox_1} = C_{\rm ox_2}, \quad \mu_1 = \mu_2, \quad \text{and} \quad \frac{W_1}{L_1} = \frac{W_2}{L_2}$$

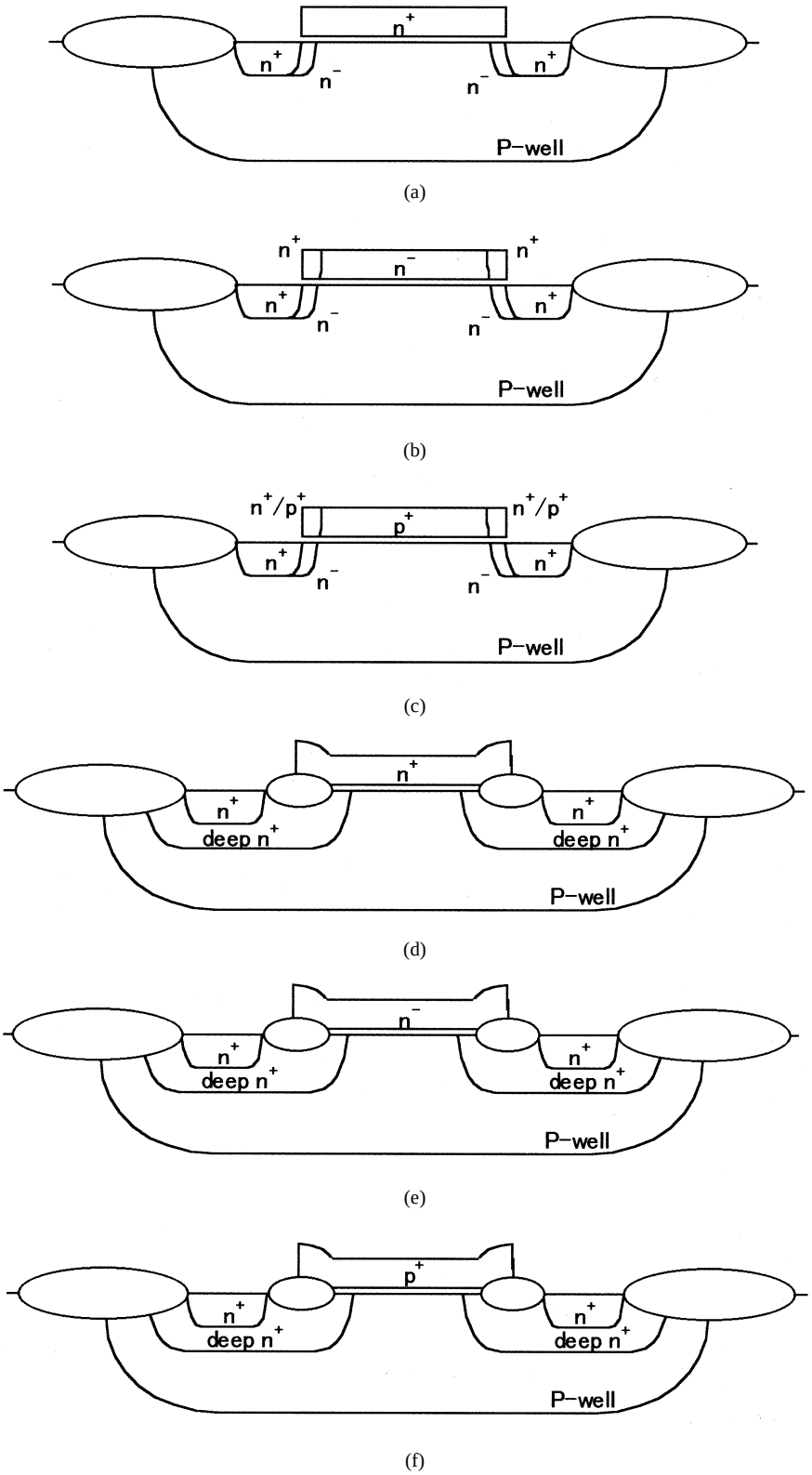

Fig. 7. Conventional and LOCOS offset N-channel MOSFETs. (a) Conventional n^+ gate. (b) Conventional n^- gate. (c) Conventional p^+ gate. (d) LOCOS offset n^+ gate. (e) LOCOS offset n^- gate. (f) LOCOS offset p^+ gate.

and so

$$V_{\mathrm{th}_{M1}} - V_{\mathrm{th}_{M2}} = V_{\mathrm{gs}_{M1}} - V_{\mathrm{gs}_{M2}}. \tag{12}$$

The difference in V_{th} between the two transistors can then be calculated from the difference in V_{gs}.

To implement the theory in a circuit, two points need to be taken into consideration. First, (12) is valid only when the transistor pairs are placed in separate wells but have the same structure. Second, voltage reference has to be provided with respect to ground. Thus, a voltage reference circuit comprised of N-channel MOSFETs, as shown in Fig. 4, has advantages

over circuits comprised of P-channel MOSFETs, as shown in Fig. 5, because N-channel MOSFETs in separate P-wells can directly produce $V_{\rm gs}$ relative to ground. This is not the case for P-channel MOSFETs without using triple wells, because P-channel MOSFETs can only generate the voltage reference with respect to V_{cc}, meaning that the output is offset from ground.

All transistors in the basic voltage reference circuit shown in Fig. 4 are N-channel MOSFETs in separate P-wells to which source electrodes are connected. The pair of transistors consisting of n^+ gate transistor M1 and p^+ gate transistor M2 are connected in series between the power supply and ground so that the difference between $V_{\rm th_{M1}}$ and $V_{\rm th_{M2}}$ is produced as $V_{\rm gs}$ of M2 $(= V_1 = V_{\rm pn})$. Transistor M1 is then a depletion mode transistor acting as a current source, while $V_{\rm th_{M1}}$ and $V_{\rm th_{M2}}$ are about -0.30 and 0.88 V, respectively.

The other pair of transistors consists of n^+ gate transistor M3 and n^- gate transistor M4. Note that $V_{\rm gs}$ of M3 $(= V_2 - V_{\rm ref})$ is equal to the difference between $V_{\rm th_{M3}}$ and $V_{\rm th_{M4}} (= -V_{\rm nn})$ because the gate electrode of M4 is connected to ground. Transistor M4 is then a depletion mode transistor acting as current source, and $V_{\rm th_{M3}}$ and $V_{\rm th_{M4}}$ are about -0.30 and -0.35 V, respectively.

Transistor M5, with $V_{\rm th_{M5}}$ of about -0.30 V, sits between the two pairs of transistors, and in combination with the resistors forms a source-follower circuit that works as a level shifter to define the drain voltage of M2. In addition, the voltage $V_{\rm pn}$ is divided using R1 and R2 and then input to the gate of M3. The final output voltage $V_{\rm ref}$ is then given by

$$V_{\rm ref} = \frac{R2}{R1 + R2} \times V_{\rm pn} + V_{\rm nn}. \tag{13}$$

The ratio of R1 to R2 can then be adjusted to make the primary temperature coefficient zero. The sum of the resistances of R1 and R2 can be chosen depending on the current consumption target. Resistances of R1 and R2 were chosen to be 2976 and 2024 Ω/sq., respectively, for all following experiments.

For the voltage reference circuit composed of P-channel transistors placed in separate N-wells, as shown in Fig. 5, the pair of transistors M1 and M2 generate $V_{\rm pn}$, which is equal to $V_{cc} - V_1$. The voltage V_2 generated by dividing $V_{\rm pn}$ using R1 and R2 is then input to the gate of n^- gate transistor M3, similar to the circuit shown in Fig. 4. Note that $V_{\rm gs}$ of n^+ gate transistor M4 produces $V_{\rm ref}$ relative to ground that is shifted $(R2/(R1+R2) \times V_{\rm pn})$ relative to $V_{\rm nn}$.

Output reference voltage $V_{\rm ref}$ is then given uniquely by $V_{\rm pn}$ and $V_{\rm nn}$ as shown in (13).

To generate an arbitrary reference voltage $V_{\rm ref}$, an additional amplifier is required. Fig. 6 shows a circuit that utilizes the differential input from n^+ gate transistor M3 and p^+ gate transistor M4, which are simultaneously part of an operational amplifier (opamp) circuit. In the circuit, $V_{\rm pn}$ is derived from

$$V_{\rm pn} = V_3 - V_2 \tag{14}$$

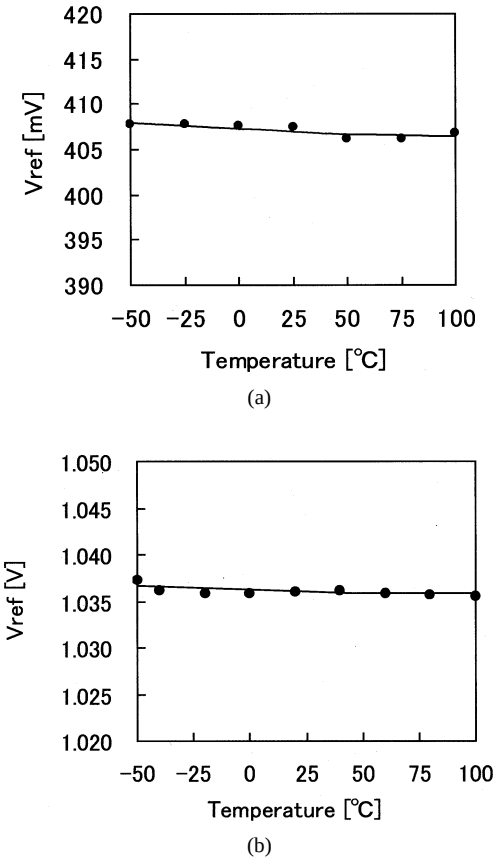

Fig. 8. $V_{\rm ref}$ as a function of temperature. (a) Circuit shown in Fig. 4. (b) Circuit shown in Fig. 6.

where

$$V2 = \frac{R1 + R2}{R2} \times V_{\rm nn}.$$

Then

$$V_3 = \frac{R1 + R2}{R2} \times V_{\rm nn} + V_{\rm pn}.$$

Arbitrary reference voltage $V_{\rm ref}$ is then given by

$$V_{\rm ref} = \left(1 + \frac{R3}{R4}\right) \times V_3. \tag{15}$$

Furthermore, temperature characteristics of the circuit block driven by $V_{\rm ref}$ can be also be compensated for by simply adjusting the ratios of R1 to R2 and R3 to R4.

IV. Experiments and Results

A. Device Structure

Voltage reference circuits were fabricated with conventional CMOS technology using a high-resistivity resistor process, producing separate P-wells and N-wells in the N-substrate. MOSFET gate-oxide thickness is 30 nm and poly-Si gate thickness is 500 nm. Gate electrodes of all of the transistors and resistors were composed of the same poly-Si, but were doped using different processes. Phosphorous doping was performed using PSG deposition to form n^+ (heavily doped) gates. P^+

TABLE I
Vref CHARACTERISTICS VERSUS PROCESS VARIATION

Process Parameter Variation	Deviation(3σ) of Vref at 25°C	Temperature Coefficient
Tox ±7%	1.7%	56ppm/°C
Vth ±23%	1.6%	59 ppm/°C
Poly Si Resistance ±20%	1.7%	80 ppm/°C

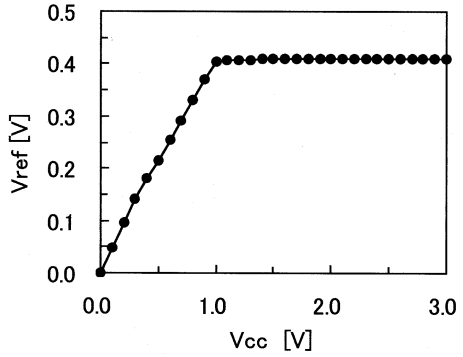

Fig. 9. $V_{\rm ref}$ as a function of supply voltage.

(heavily doped) gates, n^- (lightly doped) gates, and resistances regions were covered by SiO_2 film during the n^+ (heavily doped) gate-doping process. P^+ gates, n^- gates, and resistors were doped by ion implantation with impurity concentrations of B^+: 4×10^{19} cm^{-3}, P^+: 1.7×10^{19} cm^{-3}, and P^+: 8.0×10^{18} cm^{-3}, respectively. The boron ion implantation process was used to simultaneously dope P^+ gates and P-channel MOSFET source and drain. The phosphorous concentration of resistors differed from that of n^- gates. If the phosphorous concentration of the resistors had been chosen to be the same as that of the n^- gates, one step in the fabrication process could have been eliminated.

Both conventional and LOCOS offset transistors with separate source and drain from the active region were manufactured. In the case of conventional transistors, as shown in Fig. 7(a), phosphorous implantation for source/drain was carried out using the self-alignment method, leading to an increase in phosphorus concentration near the edge of the n^-/p^+ gate. In order to avoid this, LOCOS offset structure transistors were fabricated, as shown in Fig. 7(b), in which ion implantation beneath the LOCOS was carried out to reduce parasitic resistance. This ion implantation represents an additional process that is not needed in fabrication of conventional transistors.

Differences in characteristics of the two structures were evaluated from the dispersion of $V_{\rm ref}$. There was no appreciable difference between the two structures for transistors with channel lengths of over 100 μm, but deviations in $V_{\rm th}$ for conventional transistors became larger than for LOCOS offset transistors for channel lengths of less than 50 μm. Deviation of conventional transistors was $3\sigma = 0.9\%$ and that of LOCOS offset ones $3\sigma = 1\%$ for transistors with $L = 100$ μm. This is due to the gate length being too large to have any influence on edge

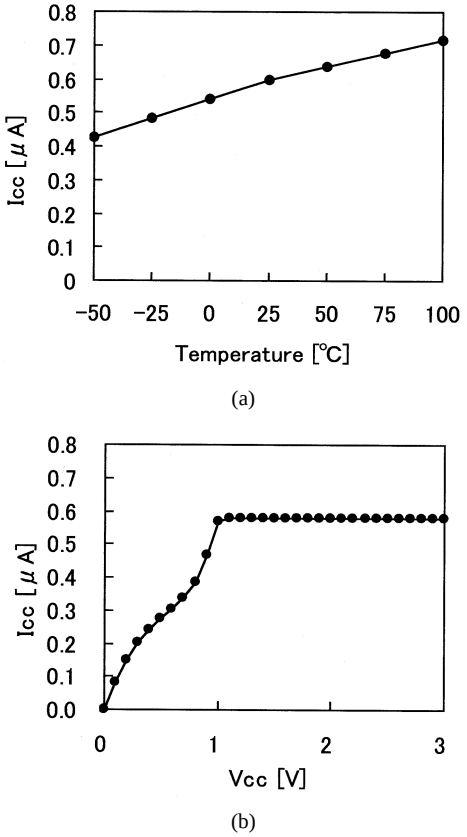

Fig. 10. I_{cc} as a function of (a) temperature and (b) V_{cc}.

phenomena. Conventional transistors with dimensions $W/L = 10$ μm/100 μm were chosen for the rest of this work.

B. Temperature Characteristics

Fig. 8 shows the measured $V_{\rm ref}$ of the voltage reference circuit as a function of temperature without trimming. A ratio of 0.405 for the series resistors R2/(R1 + R2) was used. A small negative temperature dependence that is not well expressed by quadratic regression equations remained, due to the small temperature dependence of R1/R2 ratio for temperatures below 25 °C. Temperature coefficient of the reference voltage measured using the box method was 50 ppm/°C. The ratio R2/(R1 + R2) may also be adjusted by trimming to achieve even more accurate voltage reference circuits.

C. Robustness

In principle, since the proposed voltage reference is based on $V_{\rm pn}$ and $V_{\rm nn}$, which are derived from differences in gate work function as given by (3), output voltage of the system should not fluctuate under process variations as long as both pairs of transistors are subject to the same process variations. Diffusion of impurities to the poly-Si gate electrodes is the only independently controlled process during fabrication. Because poly-Si impurity concentration $N_{\rm n}$ can be chosen so that temperature coefficient of $V_{\rm nn}$ is very stable with respect to changes in impurity concentrations, as shown in Fig. 3, the proposed voltage reference circuit is expected to be robust to process variations. Experimental results, as summarized in Table I, show that 3σ

TABLE II
VOLTAGE REFERENCE PERFORMANCE BENCHMARK INDICATORS

Type	V_{ref}	3σ	I_{cc}	V_{cc}	Temperature Coefficient
Circuit in Fig. 4	0.41V	1.7%	0.6μA	>1	<80ppm/°C
[8]*	1.2 V	5% (max/min)	<1μA	>2	±30 ppm/°C
[10]*	0.30 V	4% (max/min)	9.7μA	>1.4	<62 ppm/°C
[18]**	0.51 V	3%	2μA	2.1	–
[19]**	0.65 V	6%	<1.2μA	>0.85	57ppm/°C

* : MOS V_{th} difference based, ** : Band-gap circuit

deviations of $V_{\rm ref}$ for circuits fabricated under a wide range of process variations were kept within ±2%, while temperature coefficients of less than 80 ppm/°C were obtained without trimming the resistors.

D. Operation Voltage and Electrical Current Consumption

Fig. 9 shows $V_{\rm ref}$ characteristics as a function of supply voltage, indicating that the minimum operating voltage is about 1 V. Minimum supply voltage of the circuit in Fig. 4 is given theoretically by

$$V_{\min} = V_{\rm pn} + V_{{\rm th}_{\rm M5}} - V_{{\rm th}_{\rm M1}}. \tag{16}$$

Electrical current consumption I_{cc} is 0.6 μA at 25 °C, with no exponential increase, even up to temperatures of 100 °C, as shown in Fig. 10(a). Even if thermal junction leakage current increases, $V_{\rm ref}$ remains relatively constant because it originates from work function differences, which are relatively independent of leakage currents. I_{cc} is also largely independent of V_{cc}, as shown in Fig. 10(b).

Table II shows a list of measured voltage reference performance benchmarks. Properties of the circuit presented in Fig. 4 are shown in the first row, with values from other works shown for comparison.

V. CONCLUSION

A CMOS voltage reference based on two pairs of transistors was presented. One pair of transistors consisted of n^+ and p^+ gate transistors, and had a negative temperature coefficient of threshold voltage difference (−0.49 mV/°C). The other pair consisted of n^+ and n^- gate transistors, and had a positive temperature coefficient (+0.17 mV/°C). Measurements were conducted without trimming adjustments, and confirmed that the voltage reference had: 1) excellent output voltage reproducibility within ±2%; 2) low temperature coefficient of less than 80 ppm/°C; and 3) a low current consumption of 0.6 μA.

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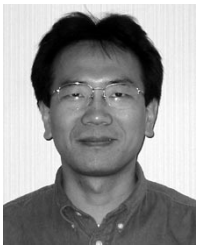

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