An Inference Engine for Gene Network Determination by Means of Optical Array Logic

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1 Introduction

Recent progress in DNA micro-array techniques enables us to obtain a massive amount of gene expression profiles simultaneously. Using the expression profiles we infer a gene network hiding the obtained data. Although several inference methods have been presented, most of them are insufficient in terms of reliability and processing time [1]. To overcome the problem, we develop an inference engine with SIMD (Single-Instruction Multi-Data stream) parallel operations based on optical array logic (OAL). Then we describe the algorithm with HDL (Hardware Description Language) and construct a prototype of the inference engine on an FPGA (Field Programmable Gate Array) device.

2 Method

OAL is originally developed as a paradigm for digital optical computing, which is also useful as a description language for parallel processing due to excellent discriptability for parallel operations [3]. Parallel processing provided by OAL is a SIMD-type of logical operations for a set of neighboring pixels in two 2-D binary images.
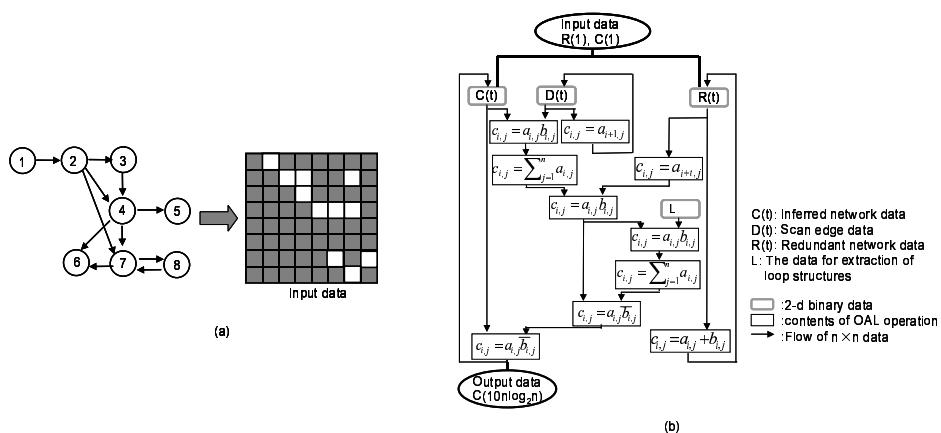
Figure 1: Schematic diagram of the presented method: (a) conversion of the target network and (b) block diagram of the OAL operations for elimination redundancy.

We have developed an inference method for gene network with OAL [2]. The method eliminates redundancy from an initial network obtained by biological experiments. The method provides a highly accurate result by realistic computational costs. Redundancy elimination of a gene network is useful to identify direct interactions among a set of genes [2]. Figure 1 shows a schematic diagram of the presented method. In Fig. 1 (a), a redundant network as the initial data is converted into a two-dimensional image. The several kinds of OAL operations shown in Fig. 1 (b) detect redundant links in the network and delete them. A parsimonious network is constructed from the output image of the operations.

In the simulation using artificial network data, the presented method shows more than 90% of sensitivity [3]. Also, the presented method completes the whole processing in $10n\log_2 n$ steps of the OAL operations for n nodes, whereas the DBRF method requires $O[n^3]$ of computational time costs for redundancy elimination [1]. These advantages of the method come from effective use of parallel processing capability of OAL.

3   Hardware Design and Implementation

A hardware specialized for OAL operations is required to apply the presented method to a large scale of gene set. We describe the processing procedure in HDL format. HDL description is the first process to design LSI (Large Scale Integrated-circuit) and the obtained code can be used for LSI fabrication. We implement a prototype of the inference engine on an FPGA device using the HDL code. The image size for OAL operations is 8×8 (n=8). For the FPGA device, XCV300E-6fg236 (Xilinx) was used. The FPGA provides the correct as shown in Fig. 2.
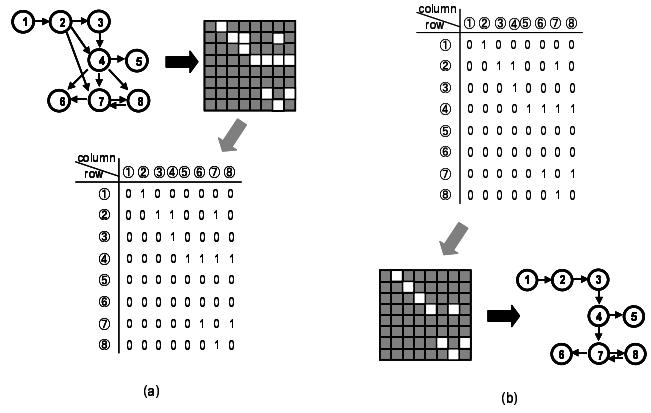

Figure 2: Simulation results obtained by HDL simulator: (a) input signal and (b) output signal.

4   Conclusion

An inference method for gene network using OAL has been developed and a hardware for the method was constructed with an FPGA device. A notable feature of the presented method is the target network is converted into an image format and processed by SIMD logical operations in OAL effectively. We found that OAL is useful for not only algorithm design but also hardware embodiment via HDL description.

References

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