A New Soft Breakdown Model for Thin Thermal SiO_2 Films Under Constant Current Stress

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***Abstract*— Soft breakdown properties of thin gate oxide films are investigated using a constant current stress measurement. The soft breakdown can be classified into two different modes from the current conduction characteristics of post breakdown oxides: one of the modes shows a telegraph switching pattern and the other random noise. The generation probabilities of two soft breakdown modes and hard breakdown strongly depend on the stress current. Time-to-breakdown is well characterized by a universal function of stress conditions regardless of the breakdown modes. These experimental findings imply that all types of breakdown originate from the same precursor and the magnitude of the following local heating due to the transient current in a conductive micro spot determines the charge conduction properties after a breakdown event.**

***Index Terms*— Dielectric breakdown, gate oxide, MOSFET, reliability, silicon.**

I. Introduction

THE reliability of thin silicon dioxide films stressed in high electric fields is one of the most important issues for future ULSI's. For example, stress induced leakage current (SILC) caused by electron injection into gate oxides through the Fowler–Nordheim (FN) tunneling is considered to be a cause of degradation of data retention time in flash E^2PROM cells [1]. Recently, it was found that large leakage currents occur abruptly during electric stressing of ultra thin gate oxide films after a gradual increase of SILC. This new failure mode called as B-mode SILC [2], quasi-breakdown [3], [4], soft breakdown [5]–[7], and partial breakdown [8], has been reported by many groups. The mode appears along with a low frequency conductance fluctuation during the electric stress, and in some cases random telegraph switching noise (RTSN) is observed [5]. The electrical conduction originates from a precursor of the oxide dielectric breakdown, and there is a consensus for the following three stage breakdown model [5], [9]. First, microscopic defects are generated in the Si/SiO_2 system during the electric field stress. A conductive path is created in the gate oxide layer after reaching a critical defect density [10]. Then, the Joule heating in the local conductive path leads to lateral propagation of the leakage spots and the oxide is finally broken down. Nafría *et al*. [9] pointed out that thermal damage can be avoided under limited Joule heating, and Depas *et al*. [5] used a constant current source to stress MOS capacitors to realize this condition.

In this work, we use constant current stress measurements with various bias conditions to investigate soft breakdown properties in thin thermal oxides. A detailed study of oxide breakdown makes it possible to classify the soft breakdown into two modes.

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II. Experimental

The devices used in this study are MOS capacitors with n^+-polycrystalline silicon gate fabricated on (100) oriented p-type substrate. The gate oxides with thicknesses of 4.8–5.8 nm were thermally grown in dry oxygen. The gate electrode with an area of 10×10 μm^2 was connected to a constant current source to degrade the oxide, while the substrate was grounded. The high electric field applied to the gate oxide induces electron injection into the oxide layer by FN tunneling. The time evolution of the applied gate voltage was monitored at intervals of 1 s during the constant current stress. The stress current was interrupted periodically to measure the current–voltage (I–V) characteristics of the leakage current through the degraded gate oxide. Measurements were carried out using an hp-4155A parameter analyzer.

III. Results and Discussion

A. Breakdown Characteristics

Fig. 1(a)–(c) shows typical examples of the gate voltage versus stress time observed during a constant 50 mA/cm^2 current stress. The nearly constant gate voltage up to 200 s indicates a small density of trapped charges in the oxide layer. Although the number of electron traps increases with stress time, the fraction of occupied traps in thin oxide films is very small due to electron detrapping by tunneling. After stressing for over 200 s, the applied voltage abruptly drops in each sample. The oxide breakdown properties are classified into three modes in accordance with their voltage-time characteristics after breakdown. Fig. 1(a) shows a typical voltage change of a sample leading to the normal hard breakdown observed in stress experiments for thicker oxides. The relatively small voltage drop in Fig. 1(b), due to soft breakdown, gives rise to an important reliability issue for future MOS devices with ultrathin gate oxides [7], [8]. After the soft breakdown, small voltage fluctuation was observed. Once the soft breakdown

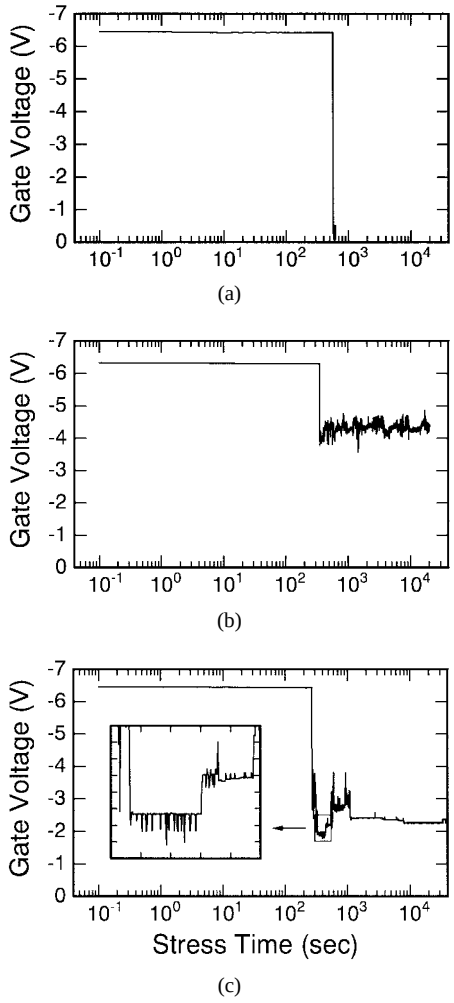


Fig. 1. Typical examples for the evolution of the gate voltage during constant current stress of 50 mA/cm^2. The oxide thickness is 5.8 nm. Breakdown properties can be classified into three modes: (a) hard breakdown, (b) analog-mode soft breakdown, and (c) digital-mode soft breakdown. The inset in (c) shows RTSN.

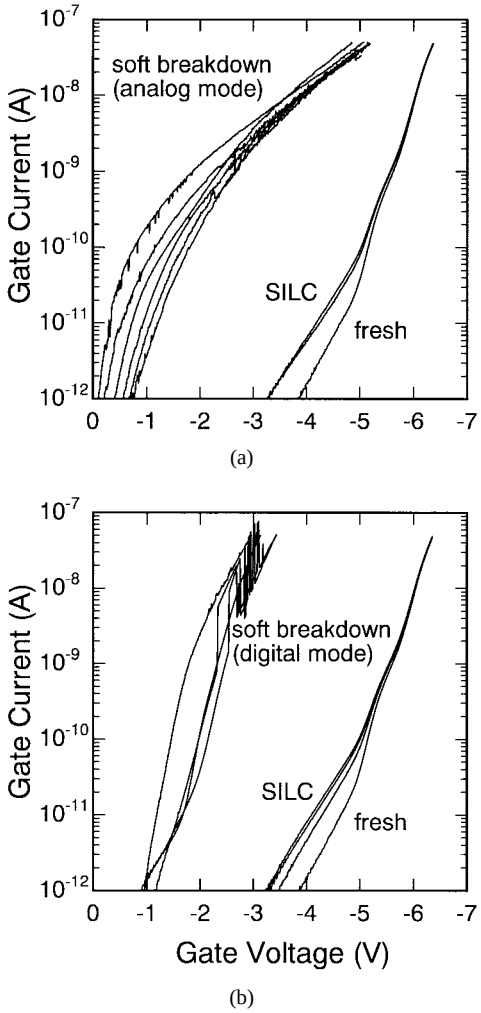


Fig. 2. The evolution of I–V characteristics of MOS capacitors with 5.8 nm oxide layer during 50 mA/cm^2 constant current stress. Measurements after analog and digital-mode soft breakdowns are shown in (a) and (b), respectively.

has occurred, extremely long stress times are necessary to induce hard breakdown. Fig. 1(c) shows another type of soft breakdown, featuring the existence of RTSN after the abrupt voltage drop. Moreover, the range of voltage fluctuation is larger than that observed in Fig. 1(b), impling different current conduction mechanisms for the two cases. In this paper, we define the soft breakdown shown in Fig. 1(b) as analog mode and that in Fig. 1(c) as ditital mode.

The clear difference between analog and digital modes is also seen in the I–V characteristics of the post breakdown oxide films. Fig. 2 shows the gate current versus gate voltage characteristics of MOS capacitors as a function of stress time under a stress current density of 50 mA/cm^2. In the initial stage, SILC increases gradually with stress time. After soft breakdown, the I–V characteristics change dramatically. The characteristics of analog mode are similar to previously reported results in [11]. On the other hand, in the case of digital mode, the I–V curves are quite unstable and fluctuate between several current levels during the measurement. The conductance of digital mode at high gate voltage is normally larger than that of analog mode.

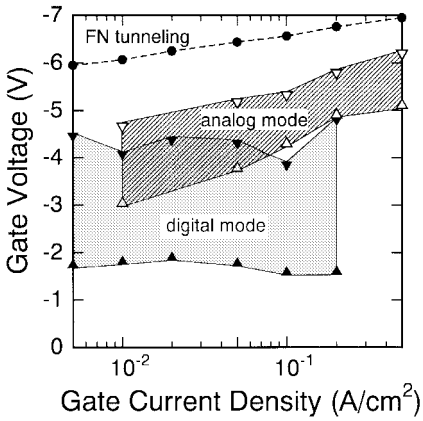


Fig. 3. The range of voltage fluctuation observed from immediately after the soft breakdown to the end of measurements as a function of stress current density. The oxide thickness is 5.8 nm. The cases of analog and digital modes are compared, and FN tunneling current for the fresh sample is also shown for comparison.

B. Stress Current Dependence of Breakdown Properties

Fig. 3 shows the range of voltage fluctuations in post-soft-breakdown oxides as a function of stress current density. The

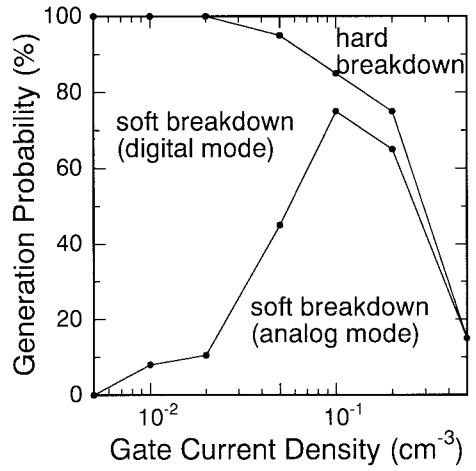


Fig. 4. Generation probability of three breakdown modes as a function of stress current density. At each stress condition 20 samples with 5.8 nm oxide layer are broken.

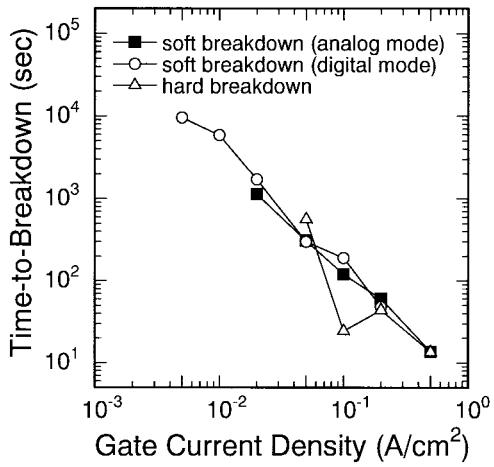


Fig. 5. The stress current dependence of time-to-breakdown for three modes. Time-to-breakdown is defined as the time when a discontinuous voltage drop was observed. Averaged value are obtained using 20 samples with 5.8 nm oxide layer for each stress condition.

minimum and maximum gate voltages observed after soft breakdown are represented by triangles. The I–V characteristics of fresh oxides are also plotted for comparison. Digital mode shows larger voltage fluctuation and current conductance than analog mode. In the case of analog mode, the average gate voltage after soft breakdown is a function of the stress current density, while that for digital mode is independent of current density. This is attributed to the sharp increase in I–V characteristics after digital-mode soft breakdown as shown in Fig. 2(b).

Fig. 4 shows the generation probability of each mode which is a function of stress current density. We carried out the breakdown experiments using 20 samples for each stress condition. Digital mode mainly occurs under small current density. The generation probability of analog mode increases with the stress current, and eventually, hard breakdown becomes dominant at high stress current.

Fig. 5 shows the stress current density versus time-to-breakdown or time-to-soft-breakdown, $t_{\rm BD}$, which is a strong function of the stress current, or the applied electric field.

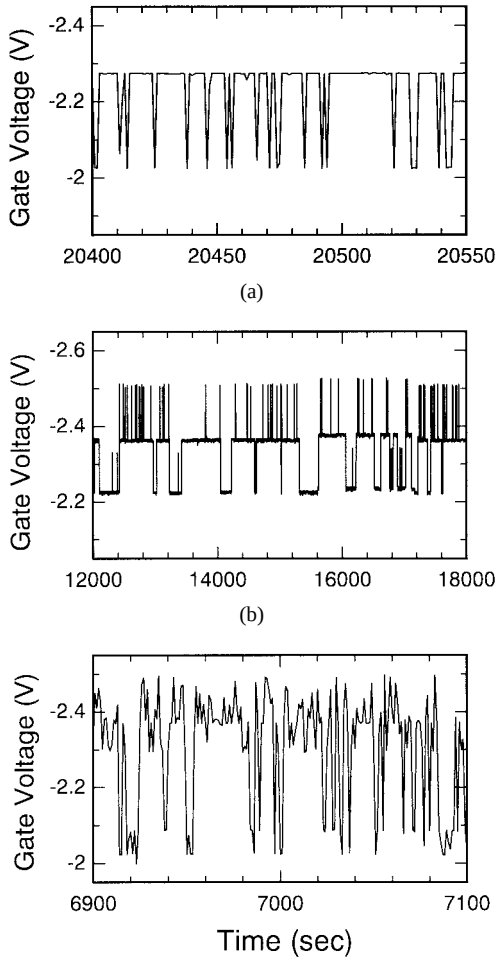


Fig. 6. Time dependence of gate voltage observed in a MOS capacitor with 5.8 nm oxide layer after digital-mode soft breakdown. Typical examples for RTSN, (a) two-level fluctuation, (b) three-level fluctuation, and (c) multilevel fluctuation, are shown.

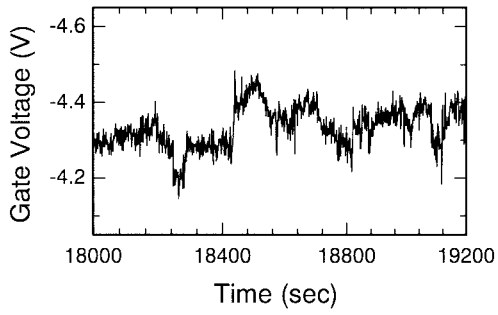


Fig. 7. Typical time dependence of gate voltage observed in a MOS capacitor with 5.8 nm oxide layer after analog-mode soft breakdown. No RTSN was observed.

The data plotted were the values averaged over 20 samples. It should be noted that all the data lie on a universal line, indicating that $t_{\rm BD}$ is a unique function of stress current density regardless of the breakdown mode.

C. Current Conduction After Soft Breakdown

Figs. 6 and 7 are the typical examples of the gate voltage fluctuations after digital and analog-mode soft breakdowns.

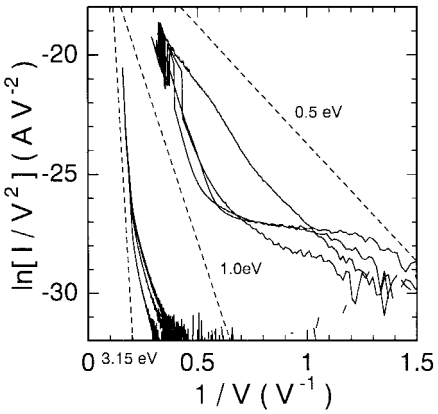


Fig. 8. FN plots of I–V curves shown in Fig. 2(b) before and after the digital-mode soft breakdown. Dashed lines show the characteristics calculated by the FN formula with three different barrier height energies.

In the case of digital mode, telegraph signal patterns are observed, e.g., Fig. 6(a) shows simple fluctuation between two well-defined levels. On the other hand, analog mode normally shows no discrete levels during stress as shown in Fig. 7.

The current conduction of post soft breakdown oxides has been extensively studied by many groups. We found several common features between our two breakdown modes and the data reported previously. I–V characteristic after digital-mode soft breakdown shown in Fig. 2(b) can be fitted by the FN tunneling equation $I = AV^2 \exp(-B/V)$. If we assume the electron effective mass $m^* = 0.5m_0$, the barrier height as determined from FN plots of Fig. 8 ranges from 0.5 to 1 eV. The similar FN-like property has been reported previously by Farmer *et al*. [12] in the excess currents of stressed thin oxide tunnel diodes. They concluded that the tunneling current is enhanced locally as schematically shown in Fig. 9(a). The energy barrier for electron injection from the electrode effectively lowered due to the creation of electron traps accompanied with lattice reconstruction to reduce the local strain. The discrete level fluctuations are attributed to the slow trapping and emission of electrons at the traps which locate near the conductive path. Although they do not contribute the current conduction by themselves, they modulate the current conductance in the adjacent narrow leakage channel via Coulomb potential of trapped electrons. Correlated, multielectron capture and emissions in a strongly interacting cluster of localized trap states could result in the large amplitude of fluctuation [13]. Various V-t patterns during constant current stress can exist according to the number and location of electron traps. Three-level fluctuations in Fig. 6(b) and more complicated multilevel fluctuations in Fig. 6(c) are due to the superposition of several independent telegraph signal patterns.

The I–V characteristic of the oxide after analog-mode soft breakdown is well expressed by the power low: $I \propto V^d$, where d ranges typically from 2 to 5. This characteristic is quite similar to that of B-SILC reported by Okada *et al*. [11]. They attributed this conduction to a variable range hopping process because they found "3D Mott's low [14]," i.e., $\ln I \propto T^{-1/4}$, in the temperature dependence of current conductivity. This mechanism indicates that there exists various leakage paths in the oxide with high density of localized states, the energies of

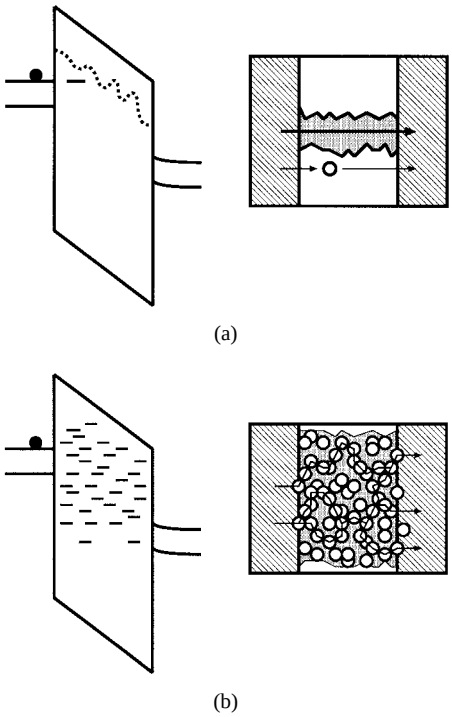


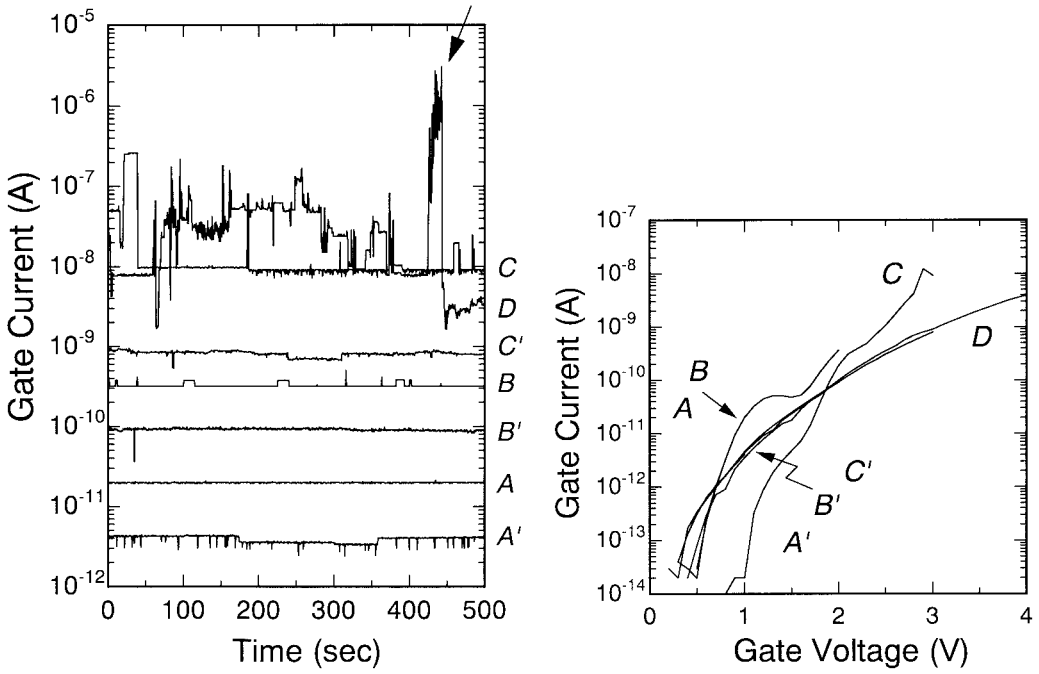
Fig. 9. Schematic view of current conduction mechanisms after (a) digital and (b) analog-mode soft breakdowns.

which are distributed over a wide band as shown in Fig. 9(b). The bottleneck of these conductive paths originate from local electronic trapping processes affects the bulk conductance of the film [15]. Nonswitching $1/f$ noise arises from the superposition of many discrete fluctuations [16].

In order to investigate the bias dependence of the fluctuation properties, we measured the current-time characteristics of the sample after digital-mode soft breakdown at biases different from the stress voltage as shown in Fig. 10(a). The sample has been broken down by the constant 20 mA/cm^2 current stress. Then, I-t characteristics were measured for 500 s using various biases in the order of $A \rightarrow B \rightarrow C \rightarrow D \rightarrow C' \rightarrow B' \rightarrow A'$. From A to C, random telegraph noise was observed, however, very complex switching pattern arose during the measurement D, and then the current dropped abruptly at the time indicated by the arrow in the figure. When I-t characteristics at lower biases were measured again (C', B', A'), the current and its fluctuation patterns extremely changed, which indicates that the analog-mode soft breakdown occurred due to the additional damage in the conductive spot. To confirm this, we monitored the I–V curves after every I–t measurements as shown in Fig. 10(b). It is clearly seen that I–V characteristics changed after measurement D: curves A, B, and C are similar to those of digital mode, while D, C', B', and A' are those of analog mode. Note that under low applied voltage RTSN-like patterns are observed in I–t characteristics of the sample after analog-mode soft breakdown [see A' in Fig. 10(a)]. However, its current levels between the switching events are not clearly defined compared with those of digital mode.

D. Breakdown Model

The soft breakdown features of analog and digital modes are summarized as follows.



(a) (b)

Fig. 10. (a) The current–time I–t characteristics after digital-mode soft breakdown monitored under various biases in the order of $A \rightarrow B \rightarrow C \rightarrow D \rightarrow C' \rightarrow B' \rightarrow A'$. Applied voltages are 1 V for A and A', 2 V for B and B', 3 V for C and C', and 4 V for D, respectively. Breakdown mode was changed from digital to analog at the time indicated by an arrow. I–V curves measured after every I–t measurements are shown in (b). The oxide thickness is 4.8 nm.

1) Clear RTSN patterns are observed frequently after digital-mode soft breakdown.
2) I–V characteristics in the two modes are different.
3) Digital mode is observed under low stress current conditions. With moderate stress current, analog-mode soft breakdown is generated, and hard breakdown dominates the other failure modes in the high current stress limit.

Based on these experimental observations, a soft breakdown model for thin gate oxides is proposed. In the early stage of electrical stress, the electron trap density in the oxide layer increases due to the reaction between injected carriers and the SiO_2 lattice [17], [18]. As the local density of traps reaches a critical threshold value, the tunneling current is enhanced at a local spot in the gate area [6].

Under constant current stress, voltage dropping and partial discharging of the capacitor occurs after a discrete conductance change in the oxide. Consequently, transient excess current flows within the RC time constant through the highly conductive leakage spot. Breakdown modes are determined by the transient current density on the occurrence of soft breakdown. Even if the equal stress current density is applied, spatial locations of generated electron traps just before the breakdown are different among the samples, thus various conductance of the leakage path is possible. This is the cause of accidental appearance of breakdown modes as seen in Fig. 4.

If the energy dissipation in the oxide layer is relatively small, digital-mode soft breakdown would be observed. On the other hand, when the transient current on the occurrence of soft breakdown is large enough to damage the SiO_2 lattice, current conduction significantly changes after the breakdown event. Due to the poor thermal conductance of SiO_2, the local lattice temperature could be heated up to the melting point. Then the local melting of the SiO_2 at the conductive spot and the Si interface layer would give rise to a chemical reaction and its atomic arrangement along the leakage path would be changed. The current conduction properties after analog and digital breakdowns are clearly different as described in Section III–C, thus it is necessary to assume some critical condition, e.g., melting of SiO_2, to separate the generation of two soft breakdown modes. One possible model for analog-mode soft breakdown is the formation of conductive filaments such as Si rich region [19] which contain high-density electron traps.

In the large excess current limit, catastrophic destruction occurs and the oxide film is finally broken down completely. The clear difference between the soft and hard breakdowns with no intermediate process between them, strongly supports the idea that a second physical phenomenon other than melting point of SiO_2 is involved in the oxide breakdown. This could be an explosive evaporation of SiO_2.

IV. Conclusion

We have observed three types of oxide breakdown in thin gate oxide films under various stress current conditions. Soft breakdown was classified into two modes, analog and digital modes, from the current conduction characteristics of the post breakdown oxide. The highly conductive leakage current after a digital-mode soft breakdown generated under small stress current conditions is caused by enhancement of electron tunneling due to trap creation in the oxide layer. The conductivity fluctuation accompanying RTSN originates from trapping and detrapping of single electrons in the traps near the conductive path. In analog mode, a local current

leakage spot is damaged by Joule heating due to the transient current at the breakdown event, and the different feature of charge transport in the conductive filament is attributed to the existence of high-density traps as a result of local SiO_2 melting. We proposed a new model, which explains the generation of three clearly classifiable breakdown modes by assuming threshold temperatures, i.e., melting and boiling points, at a local conductive spot. This is triggered by a dissipation of the capacitance charging energy after dielectric breakdown.

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REFERENCES

[1] J. De Blauwe, J. Van Houdt, D. Wellekens, R. Degraeve, Ph. Roussel, L. Haspeslagh, L. Deferm, G. Groeseneken, and H. E. Maes, "A new quantitative model to predict SILC-related disturb characteristics in Flash E^2PROM devices," in *IEDM Tech. Dig.*, 1996, pp. 343–346.

[2] K. Okada, S. Kawasaki, and Y. Hirofuji, "New experimental findings on stress induced leakage current of ultra thin silicon dioxides," in *Ext. Abstr. 1994 Int. Conf. Solid State Devices Materials*, 1994, pp. 565–567.

[3] S.-H. Lee, B.-J. Cho, J.-C. Kim, and S.-H. Choi, "Quasi-breakdown of ultrathin gate oxide under high field stress," in *IEDM Tech. Dig.*, 1994, pp. 605–608.

[4] T. Yoshida, S. Miyazaki, and M. Hirose, "Analytical modeling of quasi-breakdown of ultrathin gate oxides under constant current stressing," *Ext. Abstr. 1996 Int. Conf. Solid State Devices Materials*, 1996, pp. 539–541.

[5] M. Depas, T. Nigam, and M. M. Heyns, "Soft breakdown of ultra-thin gate oxide layers," *IEEE Trans. Electron Devices*, vol. 43, pp. 1499–1503, Sept. 1996.

[6] K. P. Cheung, J. I. Colonell, C. P. Chang, W. Y. C. Lai, C. T. Liu, and C. S. Pai, "Energy funnels—A new oxide breakdown model," *1997 Symp. VLSI Technology Dig. Tech. Papers*, pp. 145–146.

[7] B. E. Weir, P. J. Silverman, D. Monroe, K. S. Krisch, M. A. Alam, G. B. Alers, T. W. Sorsch, G. L. Timp, F. Baumann, C. T. Liu, Y. Ma, and D. Hwang, "Ultra-thin gate dielectrics: They break down, but do they fail?," in *IEDM Tech. Dig.*, 1994, pp. 73–76.

[8] K.-Y. Fu, "Partial breakdown of the tunnel oxide in floating gate devices," *Solid-State Electron.*, vol. 41, no. 5, pp. 774–777, 1997.

[9] M. Nafría, J. Suñé, and X. Aymerich, "Exploratory observations of post-breakdown conduction in polycrystalline-silicon and metal-gated thin-oxide metal-oxide-semiconductor capacitors," *J. Appl. Phys.*, vol. 73, no. 1, pp. 205–215, 1993.

[10] R. Degraeve, G. Groeseneken, R. Bellens, M. Depas, and H. E. Maes, "A consistent model for the thickness dependence of intrinsic breakdown in ultra-thin oxides," in *IEDM Tech. Dig.*, 1995, pp. 863–866.

[11] K. Okada and K. Taniguchi, "Electrical stress-induced variable range hopping conduction in ultrathin silicon dioxides," *Appl. Phys. Lett.*, vol. 70, no. 20, pp. 351–353, 1997.

[12] K. R. Farmer, R. Saletti, and R. A. Buhrman, "Current fluctuations and silicon oxide wear-out in metal-oxide-semiconductor tunnel diodes," *Appl. Phys. Lett.*, vol. 52, no. 20, pp. 1749–1751, 1988.

[13] K. R. Farmer, C. T. Rogers, and R. A. Buhrman, "Localized-state interactions in metal-oxide-semiconductor tunnel diodes," *Phys. Rev. Lett.*, vol. 58, no. 21, pp. 2255–2258, 1987.

[14] N. F. Mott and E. Davis, *Electronic Processes in Non-Crystalline Materials*. Oxford, U.K.: Clarendon, 1979.

[15] L. M. Lust and J. Kakalios, "Dynamical percolation model of conductance fluctuations in hydrogenated amorphous silicon," *Phys. Rev. Lett.*, vol. 75, no. 11, pp. 2192–2195, 1995.

[16] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency $(1/f)$ noise," *Adv. Phys.*, vol. 38, no. 4, pp. 367–468, 1989.

[17] D. J. Dimaria, "Defect production, degradation, and breakdown of silicon dioxide films," *Solid-State Electron.*, vol. 41, no. 7, pp. 957–965, 1997.

[18] A. Yokozawa, A. Oshiyama, Y. Miyamoto, and S. Kumashiro, "Oxygen vacancy with large lattice distortion as an origin of leakage currents in SiO_2," in *IEDM Tech. Dig.*, 1997, pp. 703–706.

[19] S. Ikeda, M. Okihara, H. Uchida, and N. Hirashita, "Cross-sectional transmission electron microscope studies on intrinsic breakdown spots of thin gate oxides," *Jpn. J. Appl. Phys.*, vol. 36, no. 5A, pp. 2561–2564, 1997.

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