OUKA
Osaka University Knowledge Archive

Title	Characterization of 0.1 μm MOSFETs by Cross-Sectional Scanning Tunneling Microscopy
Author(s)	奥井, 登志子
Citation	大阪大学, 2002, 博士論文
Version Type	VoR
URL	https://hdl.handle.net/11094/323
rights	
Note	

Osaka University Knowledge Archive : OUKA

https://ir.library.osaka-u.ac.jp/

Osaka University

Characterization of 0.1 μm MOSFETs by Cross-Sectional Scanning Tunneling Microscopy

Toshiko OKUI

OSAKA UNIVERSITY
GRADUATE SCHOOL OF ENGINEERING SCIENCE
DEPARTMENT OF PHYSICAL SCIENCE
DIVISION OF MATERIALS PHYSICS

2002

Abstract

Semiconductor devices have been miniaturized to improve their performance. The accelerated reduction of feature size in Si devices requires new techniques for characterizing their structures on a nanometer scale. As a new approach to nano-scale characterization, cross-sectional scanning tunneling microscopy/scanning tunneling spectroscopy (STM/STS) is used to characterize a 0.1 *m*m-scale MOSFET structure on a nanometer scale. The two-dimensional potential profile of the MOSFET is demonstrated by cross-sectional STM/STS.

First, several surface treatments are examined to realize suitable surface for STM/STS measurements. It is required that surfaces are hydrogen-terminated since surface states in the band gap prevent us from obtaining bulk electrical properties through the surfaces. Tunneling current versus bias voltage (I_t-V_s) characteristics show whether a surface is hydrogen-terminated or not. Some suitable surface preparations are established by analyzing the I_t-V_s characteristics.

Secondly, *pn* junction structures are investigated. Focused on investigating the dopant distributions after the annealing, the change in the carrier concentration during the annealing is examined by STM/STS. Comparing the concentration on the samples with different annealing times, the change in the concentrations is discussed in terms of the diffusions of implanted dopants. Cross-sectional STM/STS is applied to obtain the depth profile of I_t-V_s characteristics. It is found by referring the SIMS dopant profiles that the I_t-V_s characteristics sensitively reflect the potential variation of the *pn* junction.

Thirdly, the device structure of 0.1mm MOSFET is examined by cross-sectional STM. Topographic STM images display the source/drain, gate, channel, gate oxide and spacer of the MOSFETs in terms of height, where these regions appear as though they are a different height from each other. The bias voltage dependence of the STM images shows that the contrast observed by STM reflects the differences in electrical properties between the regions in addition to that in the corrugations. The dimensions of these regions as obtained from the images are close to the specifications of devices in feature size that we fabricated.

Finally, I_t-V_s characteristics from STS measurements are analyzed in order to reveal two-dimensional potential profile of the MOSFET. Local electrical properties of the MOSFET can be

obtained from the I_t-V_s curves taken by current imaging tunneling spectroscopy (CITS) measurements. The I_t-V_s mapping of the MOSFET is converted into the potential profile by analyzing the I_t-V_s characteristics obtained on the *pn* junction and the MOSFET. The two-dimensional potential profile clearly shows the source/drain and channel regions.

It is concluded that the two dimensional potential profiling on a 0.1 *m*m-scale MOSFET is realized by STM/STS with a spatial resolution of 5×5 nm^2. The obtained potential profile can reveal the real device structures and play an important part to improve the devices.

Contents

1. Introduction 1

1.1 Background 1

1.2 Purpose of this study 3

1.3 Scanning tunneling microscopy 3

1.3.1 Scanning tunneling microscopy in constant current mode 3

1.3.2 Scanning tunneling spectroscopy 5

1.3.3 Current imaging tunneling spectroscopy 5

References 7

2. Realizing hydrogen-terminated surfaces 9

2.1 Hydrogen-termination 9

2.2 Experimental 10

2.3 STS (I_t-V_s) results 11

2.4 Summary 16

References 17

3. Electrical characterization on *pn* junctions 19

3.1 Dopant diffusions during annealing on planar pn^+ junctions 19

3.1.1 Visualization of the planar pn^+ junctions 20

3.1.2 Dopant diffusions 22

3.2 Characterization of a cross-sectioned pn^+ junction 29

3.2.1 Visualization of the pn^+ junction 29

3.2.2 Secondary ion mass spectrometry spectrum 33

3.2.3 Distribution of I_t-V_s characteristics 33

3.3 Summary 39

References 40

4. Visualization of the MOSFET 41

4.1 STM images of the MOSFET structure 41

4.2 Summary 48

References 49

5. Two-dimensional potential profiling of a MOSFET 51

5.1 How to map the potential profiles 51

5.2 I_t-V_s characteristics mapping of the MOSFET 51

5.3 Potential distribution on the pn^+ junction 56

5.4 Potential profiling of the MOSFET 59

5.5 Summary 61

References 62

6. Conclusions 63

Acknowledgements 65

Publication list 66

International conference list 67

1. Introduction

1.1 Background

Since the invention of the integrated circuit in 1959, the semiconductor industry has improved the productivity of integrated circuits by 25-30 % annually. Much of this improvement results from following Moore's law,[1] which predicts that the number of components per chip doubles every 12 months for silicon-based integrated circuits. Throughout the 1970s and 80s, the actual doubling time was closer to 18 months, but for the past few years, the doubling time has been about 12 months.

The 2001 update of the Semiconductor Industry Association (SIA) International Technology Roadmap for Semiconductors (ITRS)[2] outlines the advances in technology that will be required for the semiconductor industry to continue its rate of improvement in productivity. Comparison of past and projected technology nodes shows that for both dynamic random-access memory (DRAM)

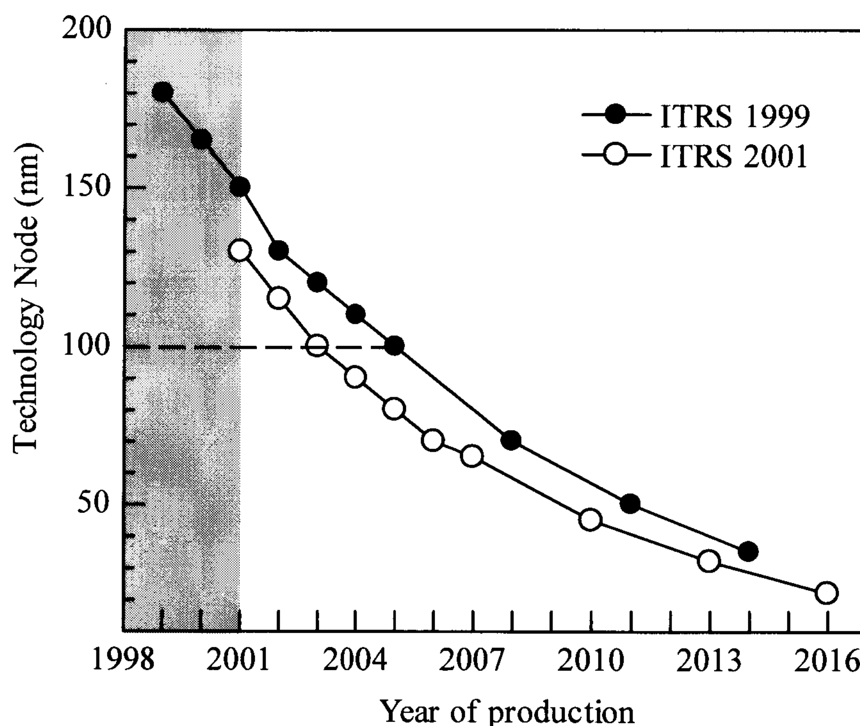


Fig. 1.1. Comparison of the timing of the technology nodes in the 2001 ITRS with that in the 1999 roadmap.

half-pitch and gate length the semiconductor industry has scaled the feature size faster than projected in the 1999. The technology nodes less than 100 nm will be realized by 2005 in the 1999 ITRS, while by 2003 in the 2001 update, as shown in Fig. 1.1. By 2016, the end of the 15-year period addressed in the 2001 ITRS, complementary metal-oxide semiconductor (CMOS) field-effect transistors with gate lengths of 9 nm are projected, as are integrated circuit interconnects with line widths of about 22 nm.

In the case of metal-oxide-semiconductor field-effect transistor (MOSFET) structures as is schematically illustrated in Fig. 1.2, the channel length has shrunk and the junction depth has become shallower. The resultant dimensions thus become comparable to the source/drain depletion width. This causes several issues that need to be resolved, such as the short channel effect and so on.[3] Thus, the accelerated reduction of feature size in Si devices requires new techniques for characterizing their structures on a nanometer scale.

As a new approach to nano-scale characterization, scanning tunneling microscopy/scanning tunneling spectroscopy (STM/STS) has been used to characterize the electrical properties of Si nano-scale *pn* junctions. It has been reported that the *n*-type, *p*-type and depleted regions can be

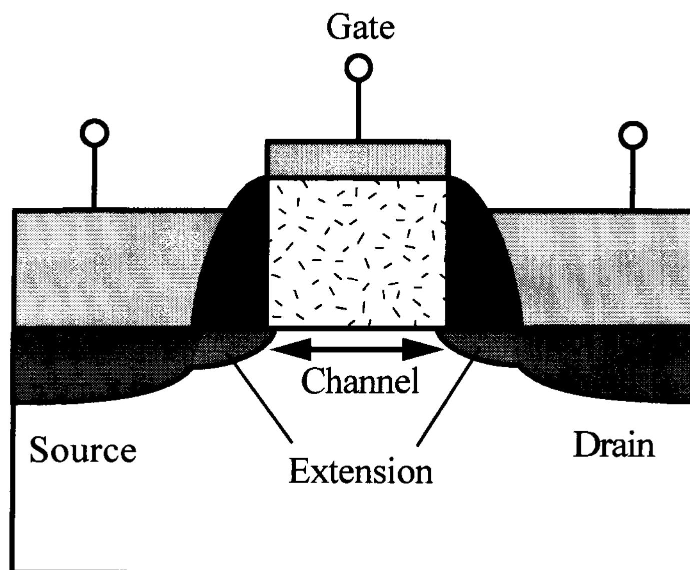


Fig. 1.2. Schematic metal-oxide semiconductor (MOS) field-effect transistor structure, showing the source, gate and drain.

visualized through hydrogen-terminated surfaces.[4] This reveals that STM is a useful technique to evaluate nano-scaled devices.

1.2 Purpose of this study

The purpose of this study is to characterize a 0.1 μm-scale MOSFET structure on a nanometer scale and to realize the two-dimensional potential profile of the MOSFET by STM/STS. There are strong needs for nanometer-scale measurement of carrier concentration profiles for the next decade. STM/STS will satisfy the needs by revealing the potential profiles, which directly leads to the carrier concentration profiles. The purpose falls into four aims. First, chapter 2 attempts to realize suitable surface for STM/STS measurements. It is required that surfaces are hydrogen-terminated since surface states in the band gap prevent us from obtaining bulk electrical properties through the surfaces. Secondly, the aim of chapter 3 is to evaluate the local electrical properties and dopant diffusions during annealing on *pn* junction structures. This chapter also aims to obtain depth profiling of tunneling current versus bias voltage (I_t-V_s) characteristics on a cross-sectioned *pn* junction. The I_t-V_s characteristics provide useful information for realizing the potential profiles on MOSFETs since MOSFETs partly consists of *pn* junctions. Thirdly, chapter 4 aims at the visualization of a 0.1 μm MOSFET structures. It is expected that STM images show the precise information of the structures such as the gate length, source/drain shape, and channel length. Finally, chapter 5 intends to achieve the two-dimensional potential profile of the MOSFET.

1.3 Scanning tunneling microscopy

In this study, measurements are mainly performed with the use of scanning tunneling microscopy (STM).[5] The STM system is JEOL ultra high vacuum JSPM4610.

1.3.1 Scanning tunneling microscopy in constant current mode

The basic idea behind STM is quite simple, as illustrated in Fig. 1.3. A sharp metal tip is brought close enough to the sample surface so that electrons can tunnel quantum mechanically

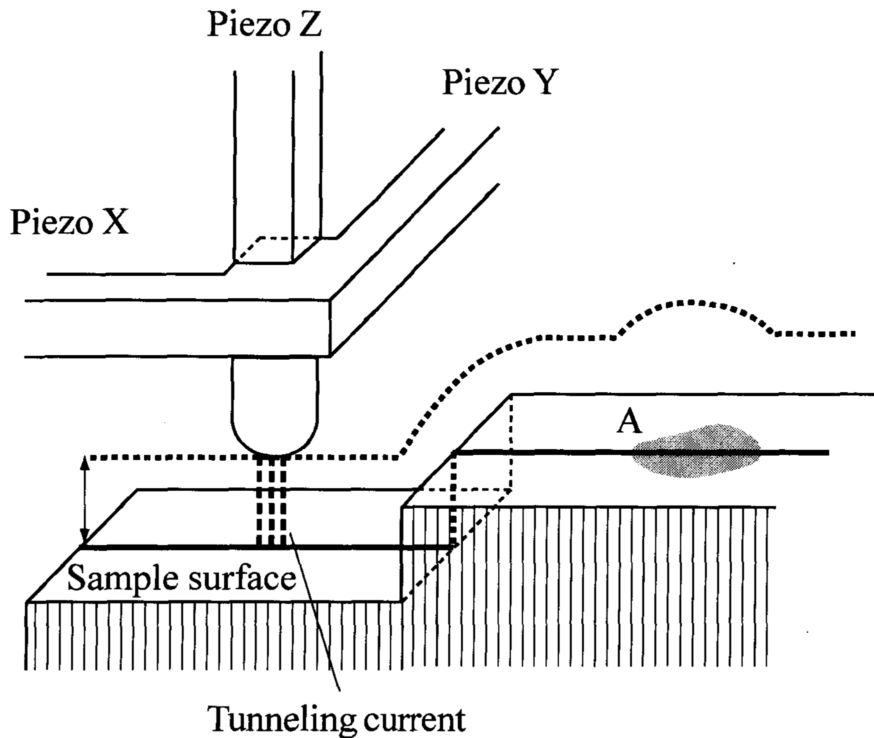


Fig. 1.3. Principle of operation of the scanning tunneling microscopy.

through the vacuum barrier separating tip and sample. This tunneling current is extremely sensitive to the height of the tip above the surface.

The position of the tip in three dimensions is accurately controlled by piezoelectric drivers. The tip is scanned in the two lateral dimensions by piezo X and Y, while a feedback circuit constantly adjusts the tip height in order to keep the tunneling current constant by piezo Z. For homogeneous surface in electronic properties, a constant current yields roughly a constant tip height, so the shape of the surface is reproduced by the path of the tip, which can be inferred directly from the voltage supplied to the piezoelectric drivers. In the case of inhomogeneous surface with regions different barrier heights due to electronic and/or electrical properties (region A in Fig. 1.3), the tip height depends on the difference in property in addition to the surface corrugation.

1.3.2 Scanning tunneling spectroscopy

Tunneling spectroscopy of semiconductor surfaces can reveal the semiconductor properties such as surface band gaps, surface band bending, and dopant carrier concentration. Tunneling current-voltage (I_t-V_s) measurement is performed in the following sequence. A tip is positioned at a measurement point and a sample separation is adjusted at a sample voltage V_s and tunneling current I_t by the feedback loop. After the feedback loop is interrupted, the sample bias voltage ramping is applied and simultaneous tunneling current is measured.

Tunneling current-voltage spectroscopy allows the *n*-type, *p*-type and depleted regions to be identified. The STM current dependence on dopant type and concentration within semiconductors is due to tip-induced band bending at the surface.[5]

1.3.3 Current imaging tunneling spectroscopy

Combining the scanning ability of the STM with the spectroscopic capabilities allows for high spatial resolution spectroscopy measurements.[6, 7] Figure 1.4 shows how the CITS measurement is performed. The I_t-V_s characteristics are measured at each pixel that the topographic STM image is taken. At a pixel, the tip-sample separation is adjusted at a condition of I_t and V_s with the feedback

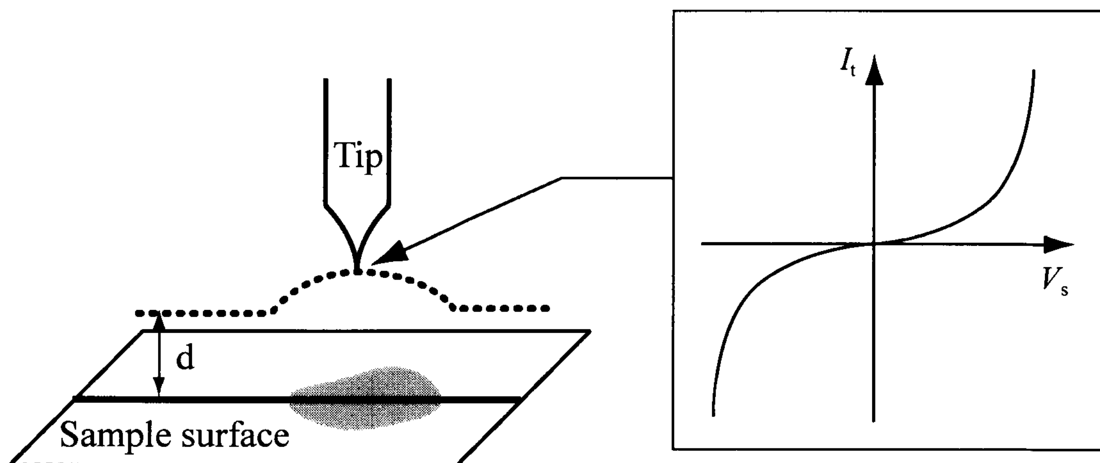


Fig. 1.4. Illustration of CITS measurements. The dots above the surface indicate the pixels that the topographic STM image is taken.

loop on to take a topographic image. Then, the feedback loop is interrupted while the applied tunneling voltage is ramping and the tunneling currents are recorded. After the feedback loop is active, the tip moves to the next pixel to take a topographic image. This sequence is repeated over the scanned area. The I_t-V_s characteristics are obtained at all points in an image.

Variations in electronic and electrical structure across the sample surface produce corresponding variations in the I_t-V_s curves. These spatial variations can be revealed by plotting in the I_t-V_s curves.

References

[1] Moore, G. E., Electronics **38,** 114 (1965).

[2] *International Technology Roadmap for Semiconductors* 2001 ed. (2001).

[3] S. M. Sze, *Physics of Semiconductor Devices* 2nd ed. (John Wiley & Sons, Inc., New York, 1981), Chap. 8.

[4] H. Fukutome, S. Hasegawa, K. Takano, H. Nakashima, T. Aoyama, and H. Arimoto, Appl. Surf. Sci., **144-145**, 554 (1999).

[5] R. M. Feenstra and J. A. Stroscio, J. Vac. Sci. Technol. **B5**, 923 (1987).

[6] J. Tersoff and N. D. Lang, *Methods of Experimental Physics Vol. 27 Scanning Tunneling Microscopy*, Edited by Joseph A. Stroscio and William J. Kaiser (Academic Press, Inc., San Diego, 1993), Chap. 1.

[7] Joseph A. Stroscio and R. M. Feenstra, *Methods of Experimental Physics Vol. 27 Scanning Tunneling Microscopy*, Edited by Joseph A. Stroscio and William J. Kaiser (Academic Press, Inc., San Diego, 1993), Chap. 4.

2. Realizing hydrogen-terminated surfaces

In this chapter, various ways of surface preparation are examined for evaluating device structures. It is essential to realize appropriate surfaces for STM measurement since STM images are extremely surface sensitive. In order to eliminate the surface states, it has already confirmed that the thermally oxidized (001) wafers are well hydrogen-terminated by dipped into a solution (the ratio of HF : HCl is 1 : 19).[1,2] Whereas, in characterizing the device structures, the thermal process for the oxidation affects the dopant distributions. The dopant redistribution makes it difficult to know the as fabricated device structures. The oxidation processes without thermal process are needed.

2.1 Hydrogen-termination

At a surface, the fundamental periodicity of the reconstructed structure taken by the surface atoms is different from that of the underlying bulk material.[3] A simple bulk termination at the surface leaves a large number of unsatisfied (dangling) bonds that result in a large free energy. In order to mitigate the energy associated with these dangling bonds, the surface atoms rearrange themselves to diminish these dangling bonds. Surface states are derived from the reconstructed surface structure, dangling bonds, adsorbates, and defects. In the case of Si, some surface states appear within the band gap leading to the Fermi level pinning at the surface. The resultant band bending near the surface prevents us to obtain the bulk electrical properties (such as carrier types and concentrations) through the surface. In order to eliminate the surface states, hydrogen-termination of the surfaces by chemical etching are examined for the variously prepared surfaces.

2.2 Experimental

The surfaces examined are classified into the four groups by their preparations before the chemical etching and listed below.

1. with thermal oxide (4 types)

A *p*-type (001) wafer (ρ= 0.2 Ω·cm) was thermally oxidized at 800 °C for 30 minutes in dry O_2. A *p*-type (110) wafer (ρ= 3-5 Ω·cm) was thermally oxidized in the same condition. Two more samples were diced from the (001) wafer (ρ= 0.2 Ω·cm). (100) and (110) cross-sections were polished and thermally oxidized in the same condition.

2. with native oxide (3 types)

(100) and (110) cross-sections were cut from a *p*-type wafer (ρ= 0.2 Ω·cm) and chemically/ mechanically polished to realize the smooth surfaces. The other was thinned to be 150 μm thick and cleaved in air. It was confirmed by an optical microscopy that partially flat surface appeared, which is probably (110) surface.

3. with chemical oxide (1 type)

A *p*-type (001) wafer (ρ= 0.1-0.5 Ω·cm) was dipped into a HF solution, and then chemically oxidized in a boiled HNO_3 solution for 10 minutes. In the solution, the oxide grows up to about 1.3 nm thick.[4] This procedure was repeated three times to smooth the surface.

4. with chemical oxide after stripping the thermal oxide 5 nm thick (3 types)

A *p*-type (001) wafer (ρ= 0.2 Ω·cm) was thermally oxidized at 800°C for 30 minutes in dry O_2 in order to form the smooth SiO_2/Si interface. Then, the oxide layer was chemically etched by a HF solution, followed by chemical oxidization in a HNO_3 solution at room temperature for 1, 5, and 29 hours, respectively.

All samples used in this study were dipped into a solution (the ratio of HF : HCl is 1 : 19) for two minutes to remove the oxide layer and to leave hydrogen-terminated surfaces. Then, they were immediately placed in an UHV-STM chamber. STM/STS measurements were performed with tungsten tips.

2.3 STS (I_t-V_s) results

Figure 2.1 shows the curves taken on the hydrogen-terminated surfaces after stripping the thermal oxide. The I_t-V_s curve (a) is taken on the (001) wafer, which shows that the tunneling current obviously increases with the positive sample voltages higher than 1 V, while the negative tunneling current hardly increases with negative sample voltages. The I_t-V_s characteristics strongly depend on Fermi-level positions in the semiconductor and tip-induced band bending.[5,6] Figure 2.2 illustrates the band diagram of tip-vacuum-sample for STM measurement on a hydrogen-terminated *p*-type Si surface. At a sample bias voltage of 0 V (Fig. 2.2(a)), the band bends toward depletion because of the difference in Fermi-level between the tip (W) and Si. For *p*-type Si, the band bends upward resulting in an accumulation for holes at positive sample voltages as is illustrated in Fig. 2.2(b). The holes easily tunnel into the tip, which results in increasing tunneling current. At negative

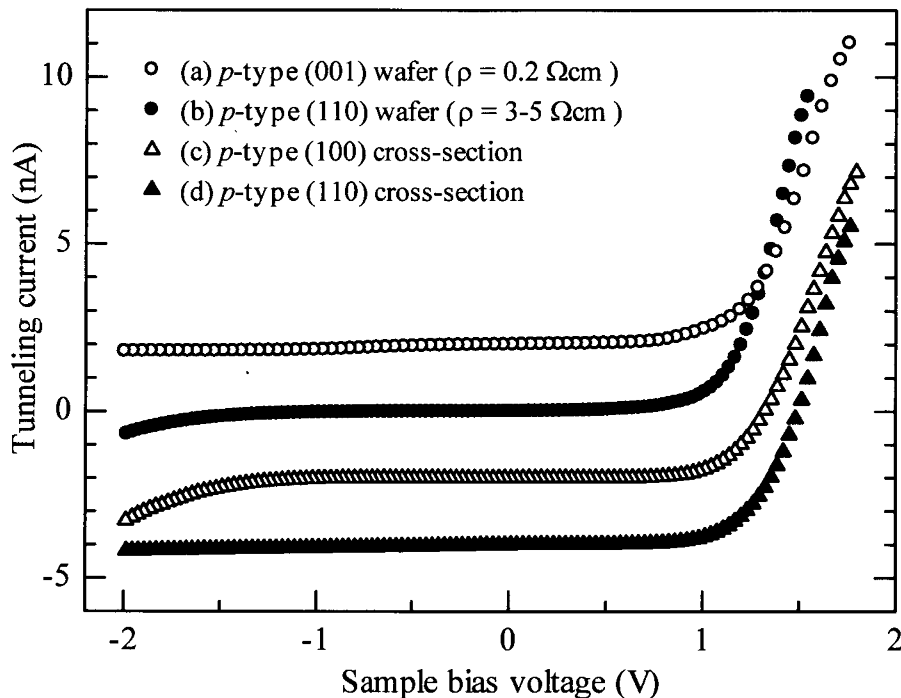


Fig. 2.1. The I_t-V_s curves taken on the surfaces with thermal oxide followed by the chemical treatment for hydrogen-termination. The curves (a) and (b) are taken on the (001) and (110) wafer, (c) and (d) are on the (100) and (110) cross-sections.

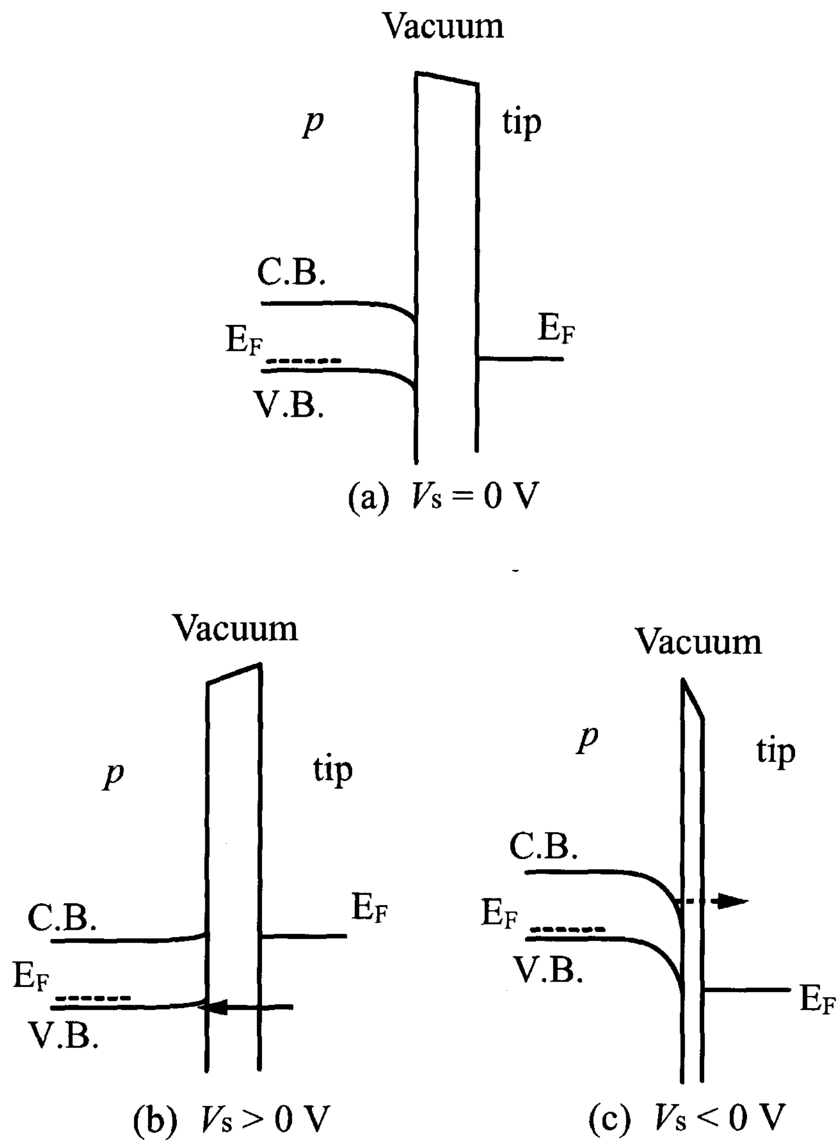


Fig. 2.2. Energy band diagrams representing the components of tunneling current. The main component in each condition is denoted by an arrow. The broken lines in the diagrams indicate the Fermi-level positions.

sample voltages, since the band bends downward to make a depleted region around the surface, the tunneling current hardly increases with the negative sample voltage (Fig. 2.2(c)). The curve (b) is obtained from the (110) wafer, while (c) and (d) are from the (100) and (110) cross-sections. All curves show almost the same characteristics as the curve (a), indicating that the surface treatments realize successfully hydrogen-terminated surfaces.

The thermal oxidation causes the annealing at the same time, leading to the dopant diffusions. In the case of characterizing device structures, the additional dopant diffusions make it difficult to know the initial dopant distributions. Therefore, other oxidation procedures without thermal oxidation are needed to realize well hydrogen-terminated surfaces.

First, surfaces with native oxide layer are examined after chemically treated for the hydrogen-termination. The I_t-V_s curves (a), (b), and (c) shown in Fig. 2.3 are taken on polished (100) and

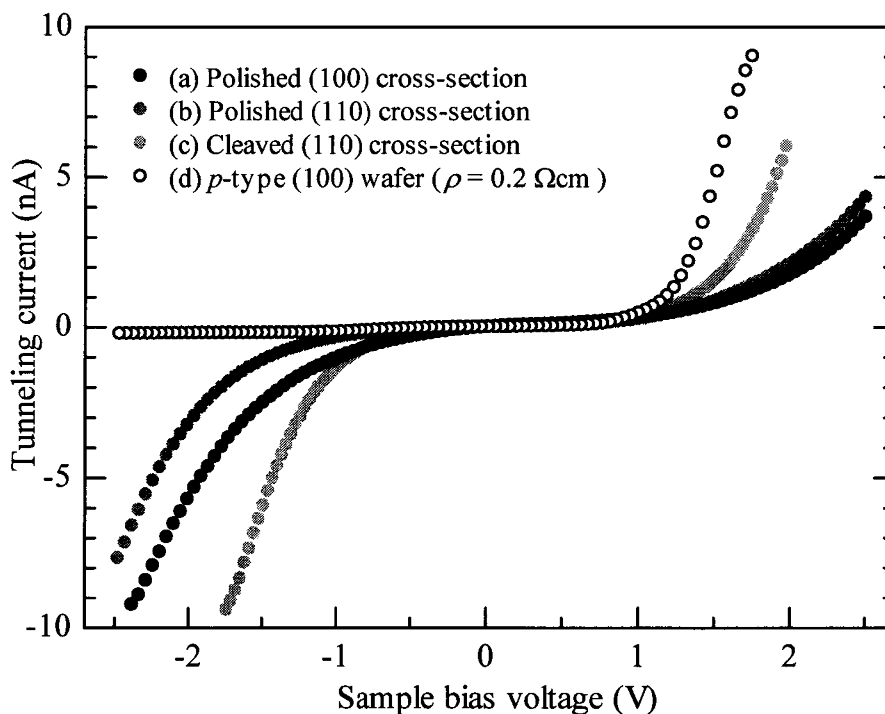


Fig. 2.3. The I_t-V_s curves taken on the surfaces with naive oxide followed by the chemical treatment for hydrogen-termination. The curves (a), (b), and (c) are taken on the polished (100) and (110) wafer and cleaved (110) cross-sections. (d) is taken on a thermally oxidized and hydrogen-terminated p-type (001) wafer.

(110) cross-sections and on a cleaved cross-section, respectively, and the curve (d) is taken on a thermally oxidized and hydrogen-terminated *p*-type (001) wafer (the identical curve shown in Fig 2.1(a)) as a reference. Though these four samples all have the same resistivity of $\rho = 0.2\ \Omega\cdot\mathrm{cm}$ in the bulk, they are not consistent with each other. The I_t-V_s curves (a)-(c) are quite different from the curve (d), which means the HF + HCl treatment for the hydrogen-termination dose not work well for the surfaces with native oxide layer.

Next, chemical oxidation of the surfaces is examined followed by the HF + HCl treatment. The I_t-V_s curves both (a) and (b) are obtained from the surface chemically oxidized by a boiled HNO_3 solution and are shown in Fig. 2.4. The curves indicate the roughly same characteristic as that from the surfaces with thermal oxide (curve (c)). Though these curves differ from each other in some

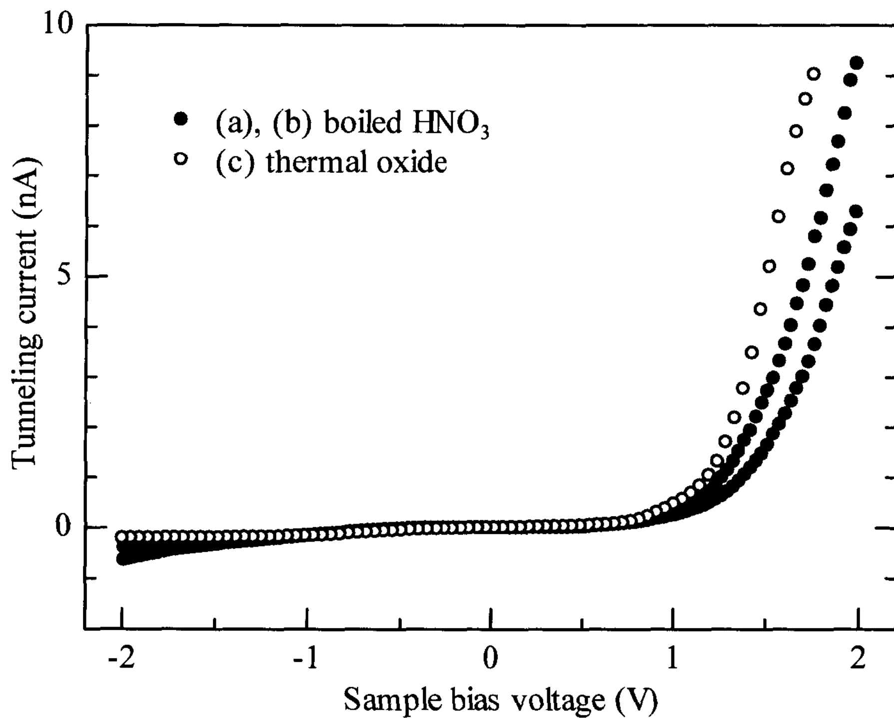


Fig. 2.4. The I_t-V_s curve taken on the surfaces chemically oxidized in a boiled HNO_3 solution. The curves (a) and (b) are taken on the (110) wafer chemically treated for hydrogen-termination. (c) is taken on a thermally oxidized and hydrogen-terminated *p*-type (001) wafer.

range, the difference is much less than that observed on the surfaces with native oxide. It is considered that this surface is, on the whole, hydrogen-terminated, but some regions still have surface states in the band gap.

For the surfaces thermally and chemically oxidized, the termination works well. Figure 2.5 shows the I_t-V_s curves taken on the surfaces chemically oxidized for 1, 5, and 29 hours after stripping the thermal oxide. All surfaces have the *p*-type characteristic indicating the successful hydrogen-termination. It is considered from the results that the chemical oxidation by a HNO_3 solution does not make the thermally oxidized surfaces worth and works effectively for the surfaces with native oxide.

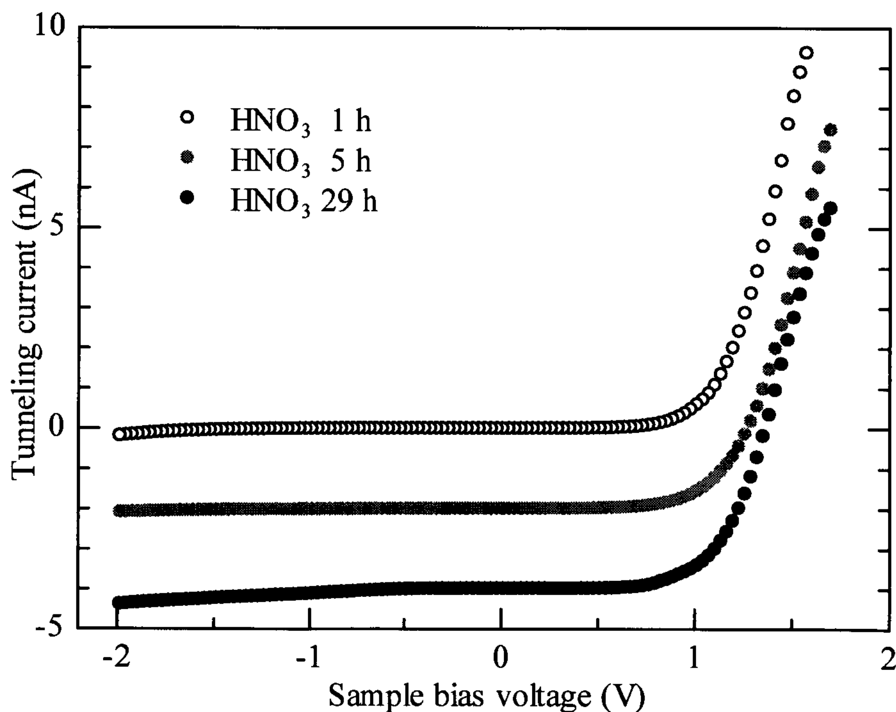


Fig. 2.5. The I_t-V_s curves taken for the surfaces chemically oxidized in a HNO_3 solution for 1, 5, 29 hours followed by the HF + HCl treatment.

2.4 Summary

Various ways of surface preparation are examined to realize the appropriate surfaces for STM measurement. The thermal oxidation is one of the best ways for hydrogen-termination by the chemical etching though it causes the dopant diffusions. The chemical oxidation by a HNO_3 almost works well and does not affect the dopant distributions. It is concluded that the chemical oxidation becomes appropriate way to characterize dopant profiles on device structures when it is more examined for reliability.

References

[1] Y. Morita and H. Tokumoto, Appl. Phys. Lett., **67**, 2654 (1995).

[2] H. Fukutome, K. Takano, H. Yasuda, K. Maehashi, S. Hasegawa, and H. Nakashima, Appl. Surf. Sci., **130-132**, 346 (1998).

[3] R. Becker and R. Wolkow, *Methods of Experimental Physics Vol. 27 Scanning Tunneling Microscopy*, Edited by Joseph A. Stroscio and William J. Kaiser (Academic Press, Inc., San Diego, 1993), Chap. 5.

[4] M. Takahashi and H. Kobayashi et.al, in press (2002).

[5] R. M. Feenstra and J. A. Stroscio, J. Vac. Sci. Technol. **B6**, 1472 (1988).

[6] R. M. Feenstra, E. T. Yu, J. M. Woodall, P. D. Kirchner, C. L. Lin and G. D. Pettit, Appl. Phys. Lett. **61**, 795 (1992).

3. Electrical characterization on *pn* junctions

Device structures and the local electrical properties strongly depend on the fabrication procedure. For example, annealing after ion implantation of dopants is performed both to activate dopants and to re-grow regions damaged by the implantation. The annealing also makes dopants diffuse and be redistributed, which affects the dopant profiles. Especially, on nanometer scale MOSFETs, the channel length becomes comparable to the depletion-layer widths around the source and drain. Since the depletion width strongly depends on the dopant concentration, it becomes much more important to investigate the dopant distribution as the channel length becomes shorter. The diffusions during the annealing have been studied to know the dopant profiles.

It has been reported that damage caused by the implantation greatly enhances the dopant diffusivity, which is known as the implant-induced transient enhanced diffusion (TED).[1,2] The diffusion makes it difficult to fabricate shallow abrupt junctions. In addition, the dopant loss due to the screen oxide remarkably increases with the reduction of the ion implantation energy for shallow junction formations. For As atoms, it is reported that the dopant loss is induced by As pile-up in the vicinity of the SiO_2/Si interface during the furnace annealing.[3,4] Because of the TED and the dopant loss, it is difficult to know the real dopant profiles. The direct investigation of the dopant redistribution gives us great help to understand the precise devise structure and electrical characteristics. As a new approach to nano-scale characterization, scanning tunneling microscopy/scanning tunneling spectroscopy (STM/STS) is used to characterize the electrical properties of Si nano-scale *pn* junctions as a basic structure.

3.1 Dopant diffusions during annealing on planar pn^+ junctions

In this section, nano *pn* junctions formed on Si(001) surfaces are characterized by STM/STS. Focused on investigating the dopant redistributions during the annealing, the change in the carrier concentration during the annealing is examined by STM/STS. Comparing the concentration on the samples with different annealing times, the change in the concentrations is discussed in terms of the diffusions of implanted dopants.

3.1.1 Visualization of the planar pn^+ junctions

Sample structures shown in Fig. 3.1 were fabricated as follows. A p^--type Si wafer (B doped, 9-11 Ω·cm) was covered with a silicon oxide layer of 5 nm, which was formed in a dry O_2 ambient at 800 °C. B ion implantation was carried out at 40 keV with a dose of 1×10^{13} cm^{-2} in order to increase the p-type dopant concentration near the surface to about 1×10^{17} cm^{-3}. After a mask pattern consisting of alternating a line and a space 150 nm wide each was formed along to <110> crystallographic axis by electron beam lithography, As ions were implanted at 10 keV with a dose of 4×10^{14} cm^{-2}. In order both to activate implanted dopants and to eliminate damage caused by As ion implantation, the samples were annealed at 800 °C for 0.5 hour in N_2 gas ambience. After the annealing, it is expected that the dopant concentrations in the p-type and the n^+-type regions are about 1×10^{17} cm^{-3} and 1×10^{20} cm^{-3}. The samples were annealed for additional 9, and 25 hours to examine the annealing time dependence of the dopant distribution. Before STM measurements, all the samples were dipped into a HF and HCl solution for two minutes to remove the oxide layer and to leave hydrogen-terminated surfaces.[6] STM measurements were performed in a constant current mode with tungsten tips in an UHV-STM chamber. A common electrode for the STM measurements was connected to the p-substrate and the n-type region.

Figures 3.2(a), (b), and (c) show STM topographic images of the samples with different annealing times of 0.5, 9, and 25 hours, respectively. All the topographic STM images shown here

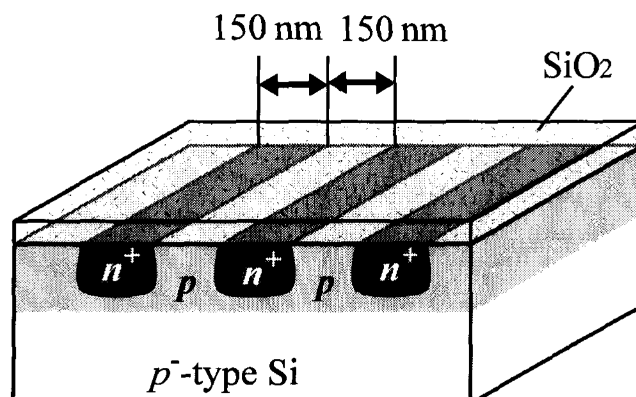


Fig. 3.1. Schematic illustration of the planar pn^+ junctions.

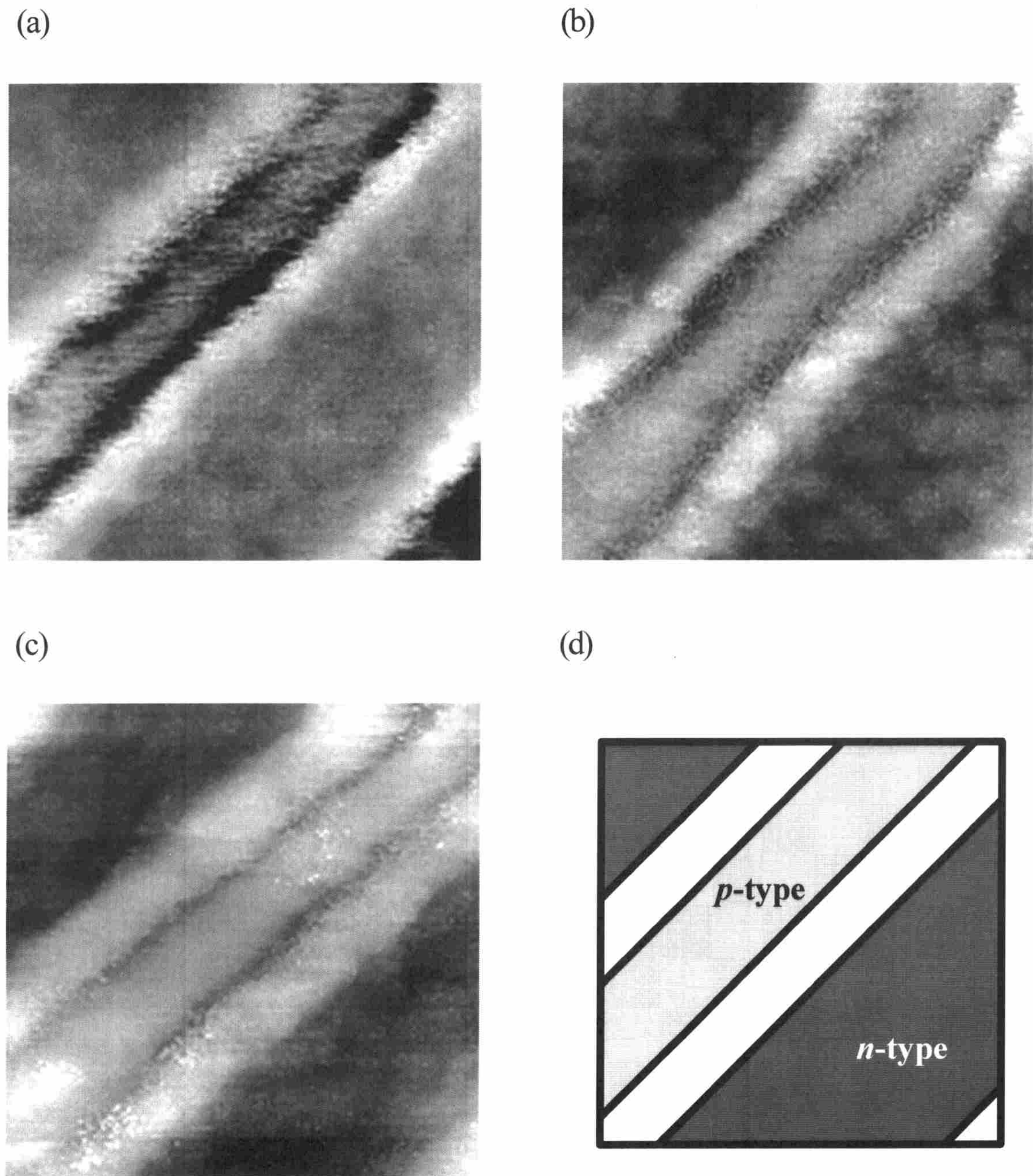


Fig. 3.2. STM images of the pn^+ junctions taken at $V_s = 1.0$ V and $I_t = 0.2$ nA. Scan range is 270 nm × 270 nm. Samples were annealed for (a) 0.5 h, (b) 9 h, and (c) 25 h after B and As ion implantation. (d) Schematic illustration corresponding to the STM images.

are taken at a sample bias voltage of 1.0 V and a tunnel current of 0.2 nA. In these figures (a)-(c), the n^+-type, p-type, and depleted regions are observed as stripes with different contrasts. The dark band shows the n^+-type region, the relatively bright band does the p-type region, and the region between the two indicates the depleted one, as is illustrated in Fig. 3.2 (d). These contrasts are explained by applying a metal-insulator-semiconductor (MIS) model to STM consisting of tip, vacuum gap, and silicon.[5] Focused on the depleted region, the mean width of the regions is about 45 nm in the sample annealed for 0.5 hour. The widths are 50 nm and 54 nm in the samples additionally annealed for 9 and 25 hours.[7] It is found that the width increases with the increase of the annealing time. The expansion of the depleted region means that the ionized acceptor concentration in p-type region decreases, since the dopant concentration in p-type region is much lower than that in n^+-type region.[8] The question is what makes the changes of the ionized acceptor concentration. In the next subsection, the causes of the concentration change are discussed in terms of the dopant diffusions.

3.1.2 Dopant diffusions

The concentration change strongly depends on the diffusions of the dopants. There are mainly five pathways (D1-D5) of the diffusion of B and As dopant atoms in the present structure during the annealing, as is schematically illustrated in Fig. 3.3. First, B atoms in the p-type region move toward n^+-type region damaged by the As implantation (D1). The As implantation creates excess point defects which affect B segregation.[2] Second, B atoms near the SiO_2/Si interface tend to diffuse into the oxide area (D2) because of the difference in solubility between Si and SiO_2.[9] Since the equilibrium concentration of B in SiO_2 is much higher than that in Si, B atoms are more likely to move into the oxide layer. D3 is the spreading of the implanted B atoms in the bulk. Since the projected range of B at 40 keV is about 100 nm,[8] B atoms diffuse from the area 100 nm deep not only into the bulk but also toward the surface.

The others are of As diffusions. The As atoms diffuse through the SiO_2/Si interface (D4). It is reported that a half of implanted As atoms pile up during the furnace annealing at 950 °C for an hour.[3] The pile-up As atoms at the SiO_2/Si interface of the n^+-type region can diffuse into p-type regions through the SiO_2/Si interface. It is expected that the pile-up As atoms diffuse through the interface and reach the p-type region, then spread into the p-type bulk regions. The other is diffusion

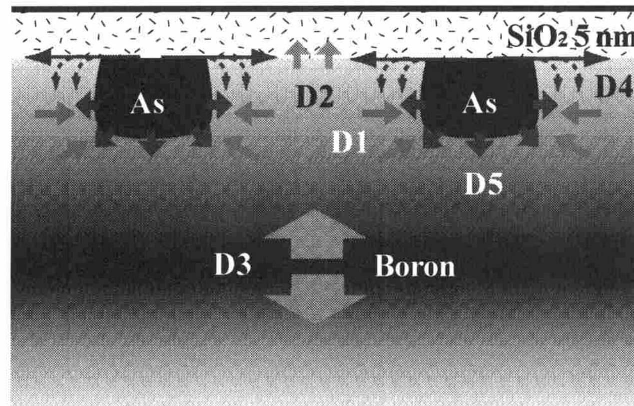


Fig. 3.3. Schematic illustration indicating the pathways (D1-D5) of the diffusion of B and As dopant atoms around the nano pn^+ junctions.

of As spreading into the p-type regions surrounding the n^+-type regions (D5). It should be noted that in the STM images in Fig. 3.2, the width of the n^+-type region slightly shrinks as the annealing time increases. The shrinkage in width measured from the STM images is about 20 nm for the annealing time of 25 hours,[7] which is the same order as is estimated from the As diffusivity at 800 °C in Si.[9] The As diffusion induces graded As distribution around the edge of the n^+-type regions. Such a short diffusion length compared to the width of the p-type region affects the dopant concentration just around the junction rather than in the whole p-type region.

Three of them have possibility to decrease the ionized acceptor concentration of the p-type region. One is the decrease of the dopants due to the transient enhanced diffusion (TED) of B into the As implanted region (D1). Another is the decrease of B dopants due to the B diffusion into the oxide layer (D2). The other is the diffusion of pile-up As atoms into p-type region through SiO_2/Si interface (D4), which leads to the decrease of the p-type carrier concentration because of the compensation by As.

In order to clarify the main cause of the change in the ionized acceptor concentration, pre-annealing at 800 °C was performed after the B implantation prior to the patterning and the As ion implantation. The pre-annealing long enough establishes the equilibrium distribution of the implanted

B atoms in Si and SiO_2. It is expected that the resultant equilibrium distribution of B dopants significantly reduce redistribution of B concentration through the pass way D2 during the post-annealing after As implantation. If the B diffusion into the oxide layer is the main cause, no expansion of the depleted region should be observed with the increase of post-annealing time.

A series of samples with the pre-annealing was fabricated by the following procedure. The samples were annealed for 24 hours after the B ion implantation so that the distribution of B atoms in Si and SiO2 comes to be equilibrium in advance of the As ion implantation. In the sample annealed for more than 25 hours after B and As implantation, it is observed that the depletion width is narrower than that in the sample annealed for 25 hours.[7] This means that the ionized acceptor concentration in the *p*-type region is higher than in the sample annealed for 25 hours. This means that few B atoms diffuse into SiO2 after post-annealing for 25 hours. It is considered from the STM results that the pre-annealing for 24 hours is long enough for B atoms to diffuse and to be in an equilibrium distribution. After the pre-annealing for 24 hours, the resist mask consisting of 160 nm lines and 140 nm spaces was patterned. Arsenic ion implantation was performed in the same condition as mentioned above, followed by the annealing for 0.5, 9, and 25 hours.

Figures 3.4(a), (b), and (c) show the STM topographic images of the samples with the post-annealing for 0.5, 9, and 25 hours after the pre-annealing. In the images, the n^+-type, *p*-type, and depleted regions can be seen as stripes with different contrasts and the width of depleted regions monotonously increases with the post-annealing time. This means that the ionized acceptor concentration in the *p*-type region decreases as the post-annealing time increases despite the pre-annealing. It is considered that B diffusion into SiO2 is not the main cause for the decrease of the ionized acceptor concentration.

In order to confirm the TED of B into the damaged regions by the As implantation, B and As depth profiles in the implanted samples were measured by secondary ion mass spectrometry (SIMS). Each sample for the SIMS measurement has just a planar pn^+ junction without alternate *p*- and n^+-stripes, and the sample was fabricated by the As implantation in the same condition as the pn^+ samples for the STM analysis. In the depth profiles shown in Fig. 3.5, the B and As concentrations are plotted by open (annealed for 0.5 hour) and closed (annealed for 25 hours) circles. It is observed that the As distribution spreads with the annealing time increasing as is expected. Concerning B distribution, the striking segregation after the annealing for 0.5 hour into the region damaged by the

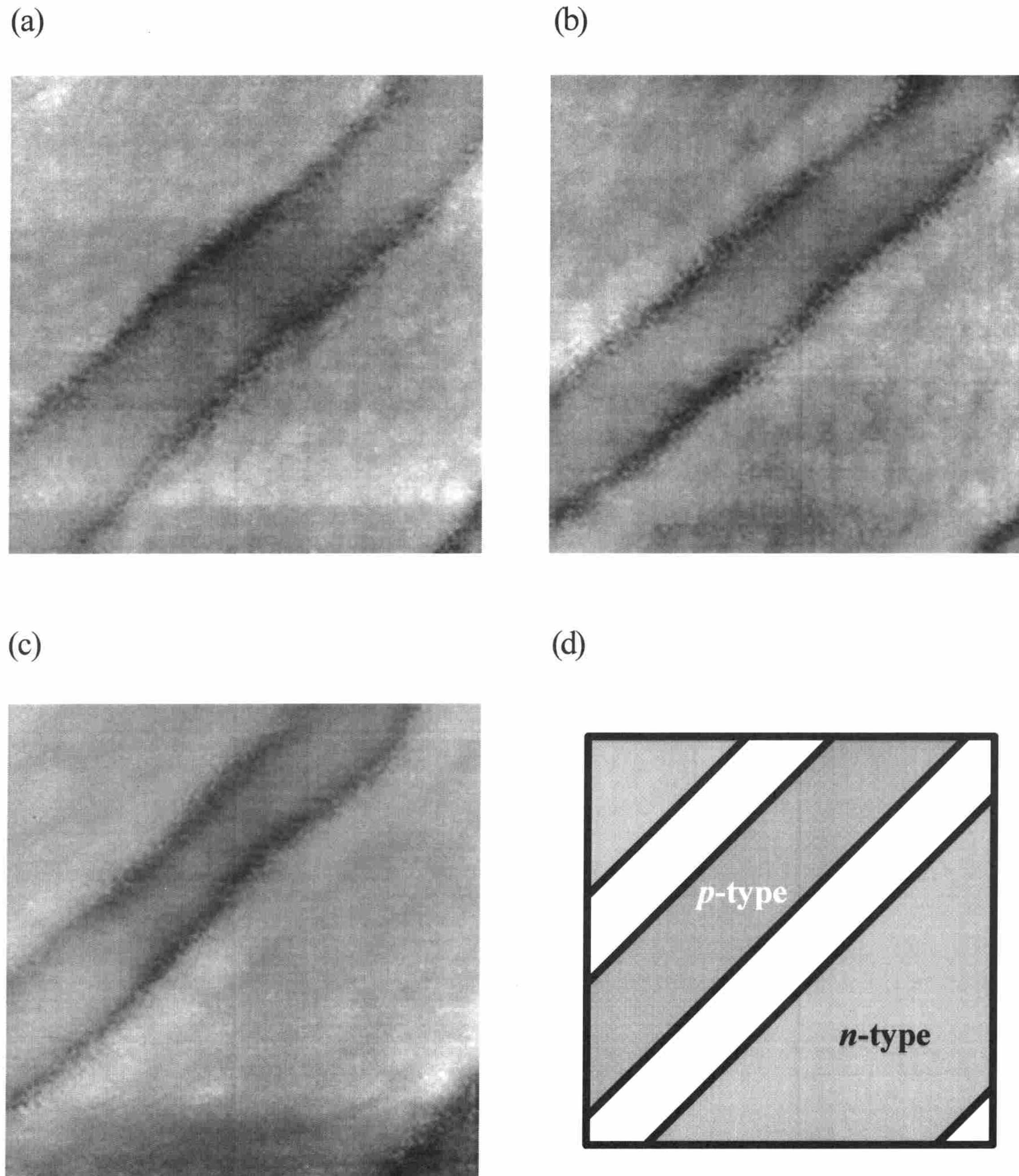


Fig. 3.4. STM images of the pn^{+} junctions taken at $V_s = 1.0$ V and $I_t = 0.2$ nA. Scan range is 270 nm × 270 nm. Samples were pre-annealed for 24 h after B ion implantation, and then annealed for (a) 0.5 h, (b) 9 h, and (c) 25 h after As ion implantation. (d) Schematic illustration corresponding to the STM images.

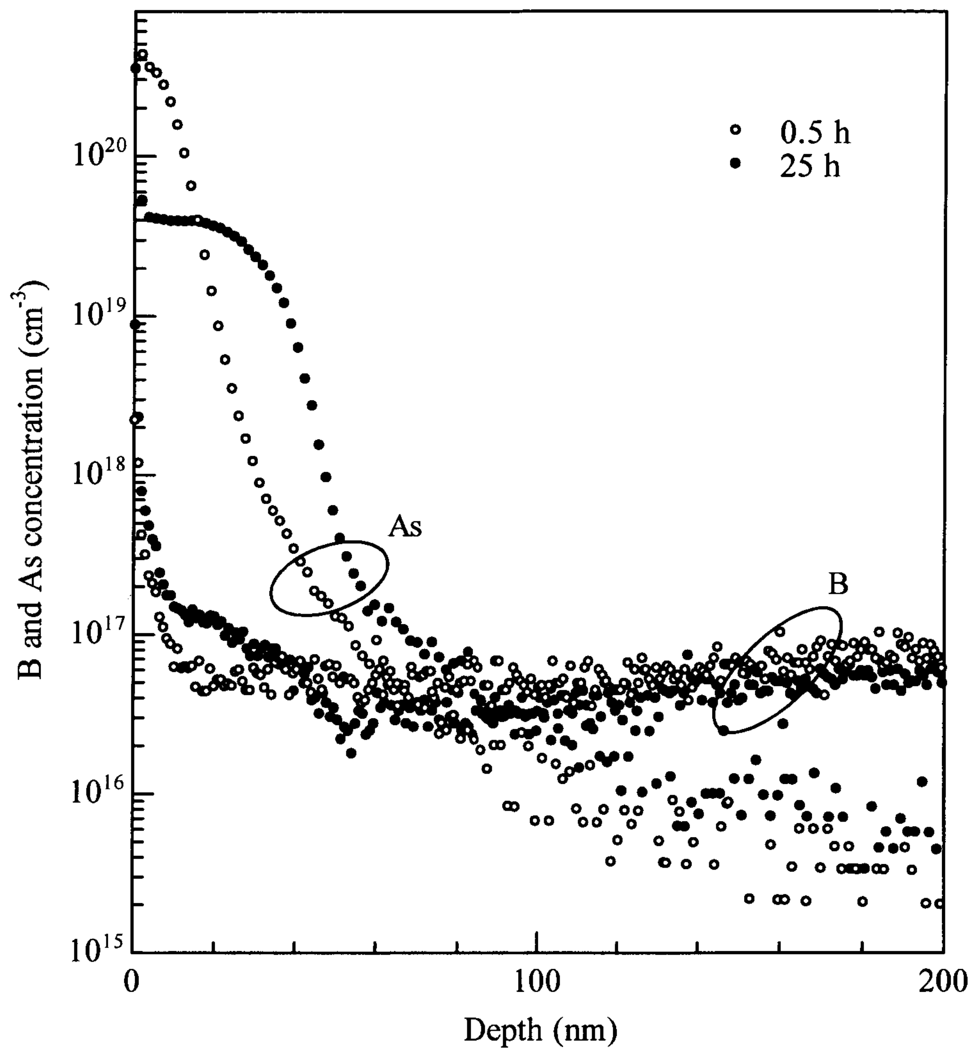


Fig. 3.5. SIMS depth profiles for B and As of the samples annealed for 0.5 and 25 hours after As ion implantation.

As implantation. The B segregation leads to a dip in B concentration beneath the region implanted with As. The regions of the B segregation spreads just the same range as As distribution during the annealing, as is observed in the profiles after the annealing for 25 hours. It is confirmed that the transient enhanced diffusion of B into the As implanted region (D1).

Next, the ionized acceptor concentrations in the *p*-type regions are compared among the samples with and without pre-annealing. The concentration can be qualitatively estimated from the current-voltage (I_t-V_s) characteristics.[10] Figure 3.6 shows the I_t-V_s characteristics acquired in the *p*-type regions of the four samples with the different sequences of the implantation and the annealing. The I_t-V_s curves (a) and (b) are taken on the samples annealed for 0.5 and 25 hours after the B and

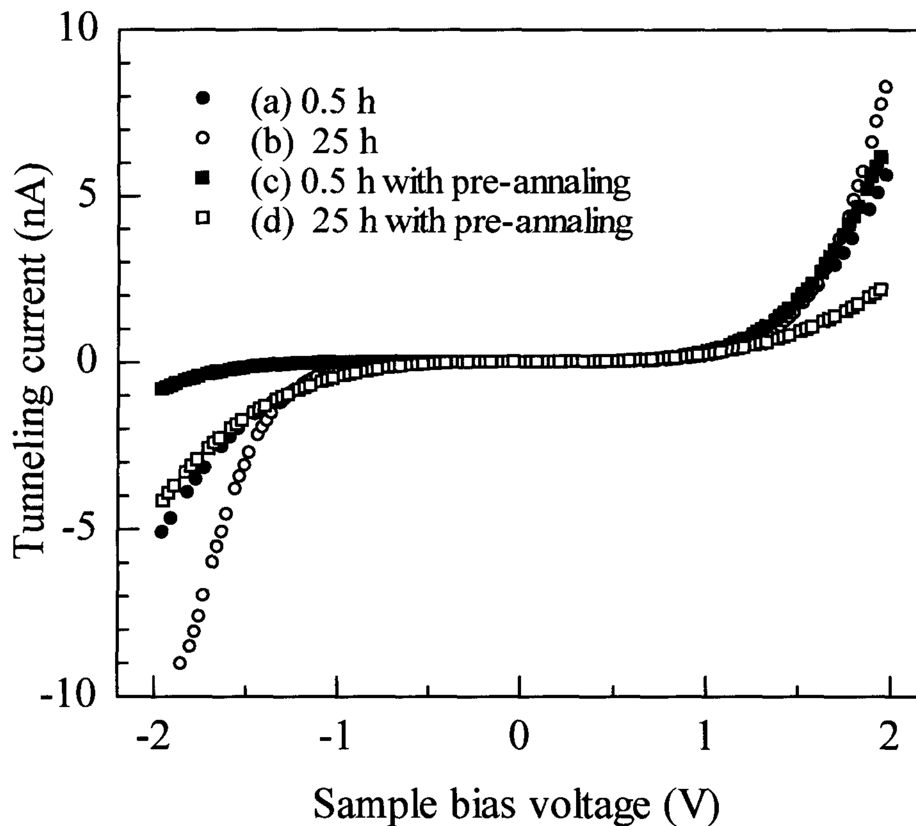


Fig. 3.6. Current–voltage (I_t-V_s) curves taken in the *p*-type regions. The I_t-V_s curves (a) and (b) are taken on the samples annealed for 0.5 h and 25 h without pre-annealing, (c) and (d) are on the sample annealed for 0.5 h and 25 h with pre-annealing.

As implantation. The curve (c) and (d) is for the samples annealed for 0.5 and 25 hours after the As implantation with the previous B implantation and the pre-annealing for 24 hours. The spacing between the tip and the sample was adjusted at a sample bias voltage of 1.0 V and a tunneling current of 0.2 nA. The I_t-V_s curves (a) and (b) are completely different from that obtained from a hydrogen-terminated *p*-type wafer. The negative tunneling current obtained at negative sample bias is more than that from a *p*-type wafer with the dopant concentration of 1×10^{17} cm^{-3}, which shows much lower *p*-type carrier concentration. It is considered that the lack of the ionized acceptor results from the absent of B due to TED.

In contrast, the I_t-V_s curve (c), which is obtained from the *p*-type region of the sample with pre-annealing for 24 hours and post-annealing for 0.5 hour, shows the characteristic like that for a *p*-type wafer. The *p*-type characteristic derives from the pre-annealing before As implantation. During the pre-annealing, since there is no sink of damaged region, enough amount of B atoms have already reached the surface in the *p*-type regions. After the post-annealing for 25 hours, the I_t-V_s curve (d) does not show *p*-type characteristic, indicating the ionized acceptor concentration in the *p*-type regions decreases. It is considered that the decrease is due to the B diffusion from the *p*-type regions to the damaged n^+-type regions. In the samples annealed for 25 hours without pre-annealing (curve (b)), in spite of the same annealing time for B atoms, since the B atoms tend to diffuse into the regions damaged by the As implantation, enough B atoms can not reach the surface in the *p*-type regions during the annealing after As implantation. Compared with the sample with pre-annealing (curve (c)), the sample annealed for 0.5 hour without pre-annealing (curve (a)) has lower *p*-type concentration though both were annealed for 0.5 hour after As ion implantation. This difference shows that the As diffusion through the SiO_2/Si interface D4 does not occur so much as the D1. Thus, the B diffusion into As-implanted damaged region is the main cause of the *p*-type concentration decrease.

3.2 Characterization of a cross-sectioned pn^+ junction

In this section, a pn^+ junction is investigated on a nanometer scale by cross-sectional STM/STS. It is necessary to observe the cross-sectioned device structures in order to obtain the two-dimensional carrier profile (including depth profiles) of the devices. One of the useful techniques for evaluating the depth profile, SIMS has been widely used.[11] SIMS can reveal one-dimensional dopant depth profiles with the high sensitivity and the accuracy in the density, whereas it is difficult to satisfy the demands for two-dimensional spatial resolution. Combining the SIMS depth profiles with the cross-sectional STM/STS results, the I_t-V_s characteristics are correlated with the potential profile of the pn^+ junction.

3.2.1 Visualization of the pn^+ junction

A pn^+ junction was fabricated on a *p*-type Si (001) wafer (ρ= 0.2 Ω·cm) by As ion implantation through the thermal oxide 5 nm thick. The sample structure is schematically illustrated in Fig. 3.7. Ion implantation of As was performed at 10keV with a dose of 4×10^{14} cm^{-2}. Activation of the implanted dopants was achieved by rapid thermal annealing at 1000 °C for 10 seconds. Then, a *poly*-Si layer 2.5 μm thick was deposited as a protective cap layer for the cross-sectional STM

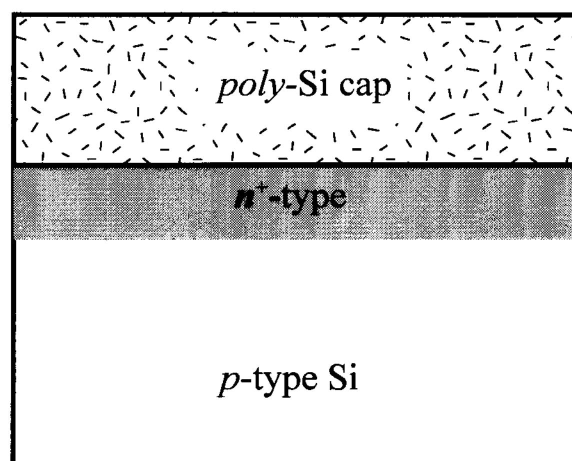


Fig. 3.7. Schematic illustration of the cross-sectioned pn^+ junction.

measurements. The (100) cross-section of the structure was chemically and mechanically polished to realize smooth surfaces, and then the cross-section was thermally oxidized at 800 °C for 30 minutes in dry O_2, followed by hydrogen-termination. The STM measurements were performed in constant current mode with tungsten tips in a UHV-STM chamber. A common electrode for the STM measurements was connected to the *p*-substrate, the n^+-type region, and the *poly*-Si cap layer.

Figure 3.8 shows the sample bias voltage dependence of topographic STM images observed through the hydrogen-terminated cross-section of the pn^+ junctions. The interface between the SiO_2/Si is indicated by an arrow. The image shown in Fig. 3.8(a) is taken at a sample bias voltage V_s of 5 V and a tunneling current I_t of 0.2 nA. In the left side of the image, part of the *poly*-Si cap layer can be observed as bright corrugations. The noticeably depressed region next to the *poly*-Si derives from the thermal oxide between the *poly*-Si layer and the substrate since the HF and HCl solution etched the oxide. Next to the depressed line, the pn^+ junction is observed as an almost flat region. By contrast, the STM image taken at V_s of 1 V visualizes the pn^+ junction as shown in Fig. 3.8(b). The observed protrusive band indicates the n^+-type region, while the flat region in the right area indicates the *p*-substrate region. This bias voltage dependence can be explained by considering the band diagrams for the tip-vacuum-sample conditions. Figure 3.9 shows schematic band diagrams of the *p*-type and the n^+-type regions toward the direction perpendicular to the surface when the tip is close to each region. At V_s of 5 V, electrons can tunnel from the tip into the conduction band for both *p*- and n^+-type regions (Figs. 3.9(a) and (b)). In the condition, the *p*- and n^+-type regions do not show any difference in the STM image. At V_s of 1 V, for the *p*-type region (Fig. 3.9(c)), electrons can tunnel from the tip into the valence band, where the band bends upward resulting in the accumulation of holes. For the n^+-type region, electrons can tunnel from the tip into the conduction band, as is shown in Fig. 3.9(d). In both cases, it is easy for tunneling current to flow. A possible explanation for the different contrasts is the barrier height difference. The barrier height for the tunneling, which is defined to be the energy difference between the tunneling level and the vacuum level, is higher for *p*-type region than for the n^+-type region. Therefore, in the n^+-type region, since it is easier for electrons to tunnel into the n^+-type region than into the *p*-type region, the STM tip rises away from the surface in order to keep the tunneling current constant. This bias voltage dependence provides the evidence that the topographic STM images reflect not only the actual

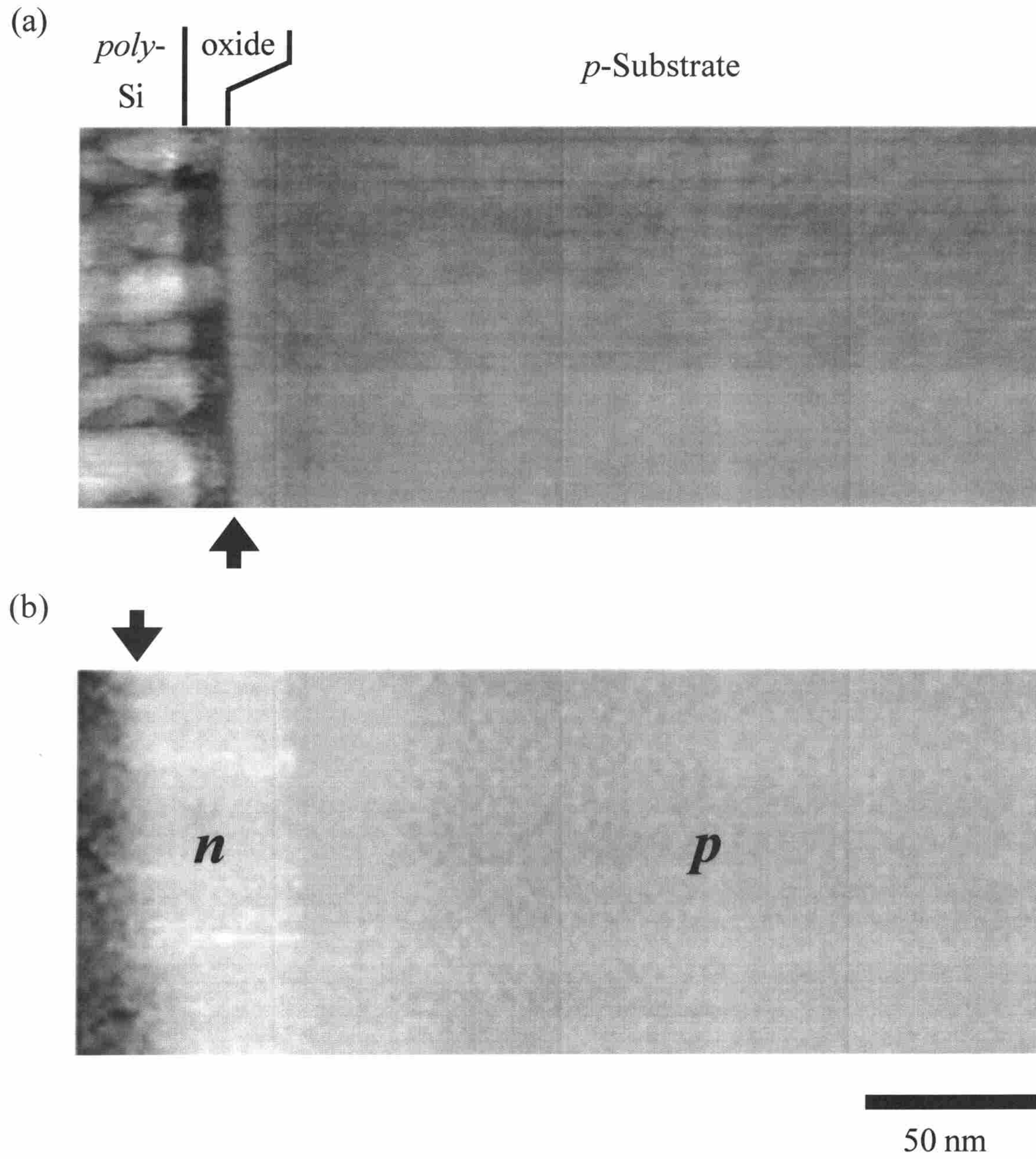


Fig. 3.8. Topographic cross-sectional STM image of the pn^+ junction taken at tunneling current $I_t = 0.2$ nA and sample bias voltage (a) $V_s = 5$ V, (b) $V_s = 1$ V.

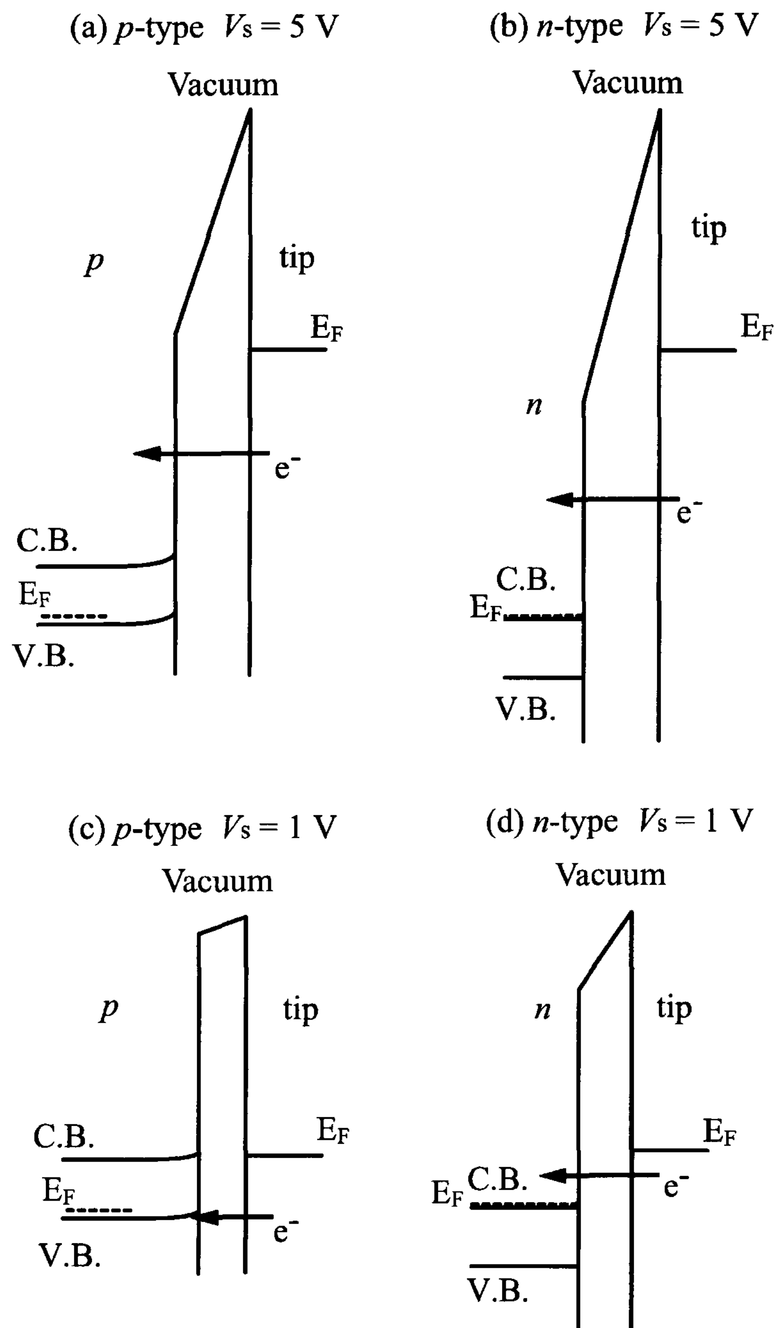


Fig. 3.9. Schematic band diagrams of the p-type and the n^{+}-type regions toward the direction perpendicular to the surface when the tip is close to each region. Here, E_F is the Fermi level, V.B. is the valence band of the sample, and C.B. is the conduction band.

surface roughness but also the electrical properties of each region.

3.2.2 Secondary ion mass spectrometry spectrum

In order to evaluate the relation between dopant concentrations and the corrugations observed in the STM image taken at 1 V, the dopant depth distributions of the pn^+ junction are examined by SIMS. An O_2^+ and a Cs^+ primary beam at 3 keV were used for B and As, respectively. The SIMS measurements were performed from the substrate side to the SiO2/Si interface on a thinned sample to eliminate the knock-on effects of the primary ions.[12] Figure 3.10 shows B and As depth profiles in the pn^+ junction taken by SIMS together with the corresponding STM image taken at 1 V. An arrow in Fig. 3.10 indicates the SiO2/Si interface, where it is defined the depth is 0 nm. The As concentration is over 5×10^{19} cm^{-3} at the region shallower than 20 nm and rapidly decreases to 5×10^{17} cm^{-3} at the depth of 40 nm, and then gradually decreases to less than 1×10^{16} cm^{-3}. The concentration of B slightly changes in the range of 3×10^{16} cm^{-3} and 1×10^{17} cm^{-3} at the depths of shallower than 150 nm and remains almost constant at the deeper regions. From the profiles, it is found that the pn^+ junction exists at the region 80 nm deep assuming that the As and B concentration are the same at the junction.

3.2.3 Distribution of I_t-V_s characteristics

The electrical property of the pn^+ junction is characterized by the measurement of the tunneling current versus sample bias voltage (I_t-V_s) characteristics.[10] Figure 3.11 shows I_t-V_s curves taken at the four areas labeled (I)-(IV) in the STM image in Fig. 3.10. The tip-sample separation is adjusted at each point of the measurements in the condition V_s of 1 V and I_t of 0.2 nA. The dopant concentration at each region estimated from the SIMS measurement is also shown in Fig. 3.11. The I_t-V_s curve taken at the area (I) 216 nm deep shows that the tunneling current obviously increases with the positive sample voltages higher than 1 V, while the negative tunneling current hardly increases with negative sample voltages. The I_t-V_s characteristics strongly depend on Fermi-level positions in the semiconductor and tip-induced band bending.[13, 14] For p-type Si, the band bends upward resulting in an accumulation of holes at positive sample voltages as is illustrated in Fig. 3.12(a). The holes easily tunnel into the tip, which results in rapid increase of the tunneling current. At negative sample

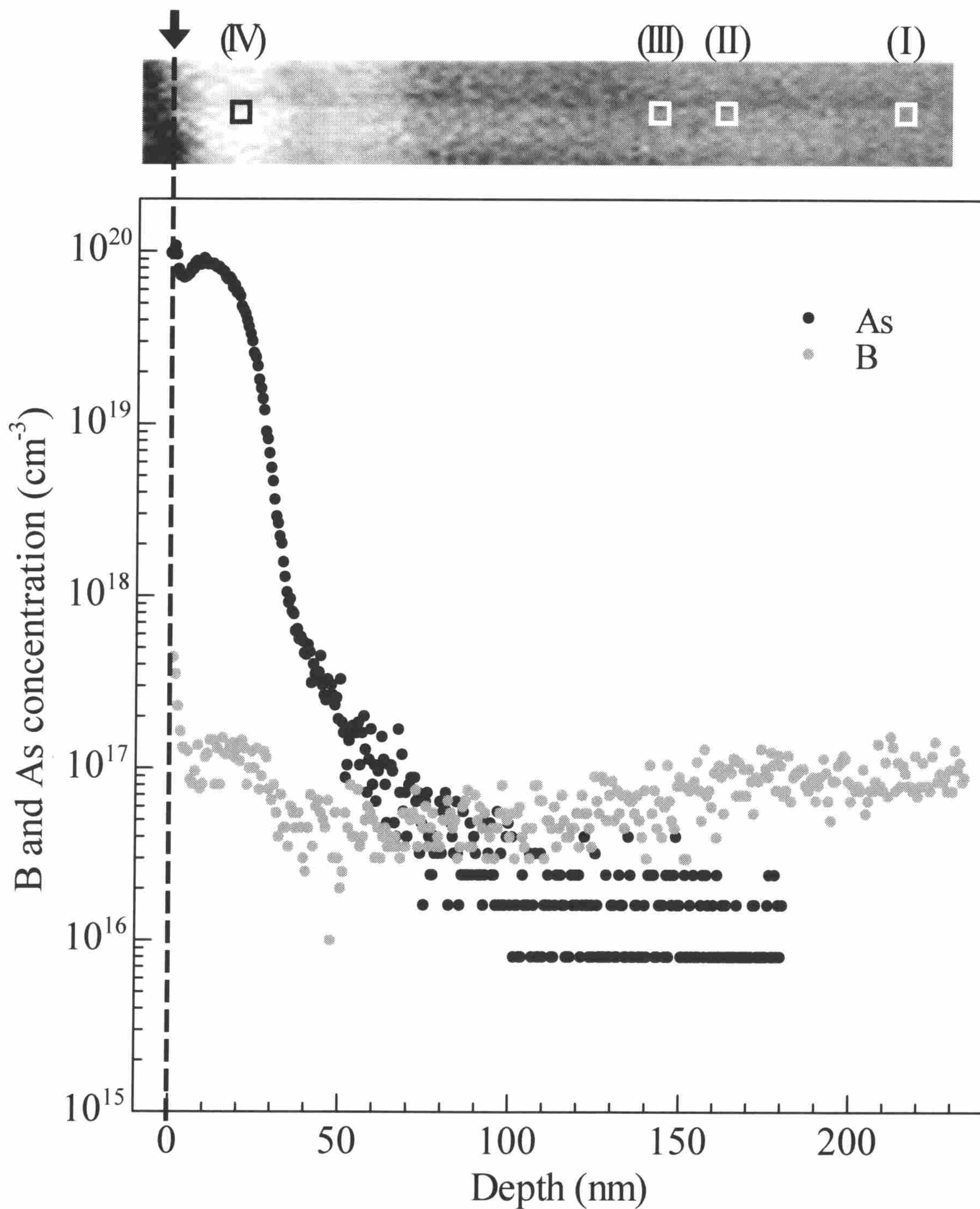


Fig. 3.10. SIMS depth profiles for B and As plotted by black and gray closed circles, respectively. The corresponding STM image taken at 1 V also shown above the profiles.

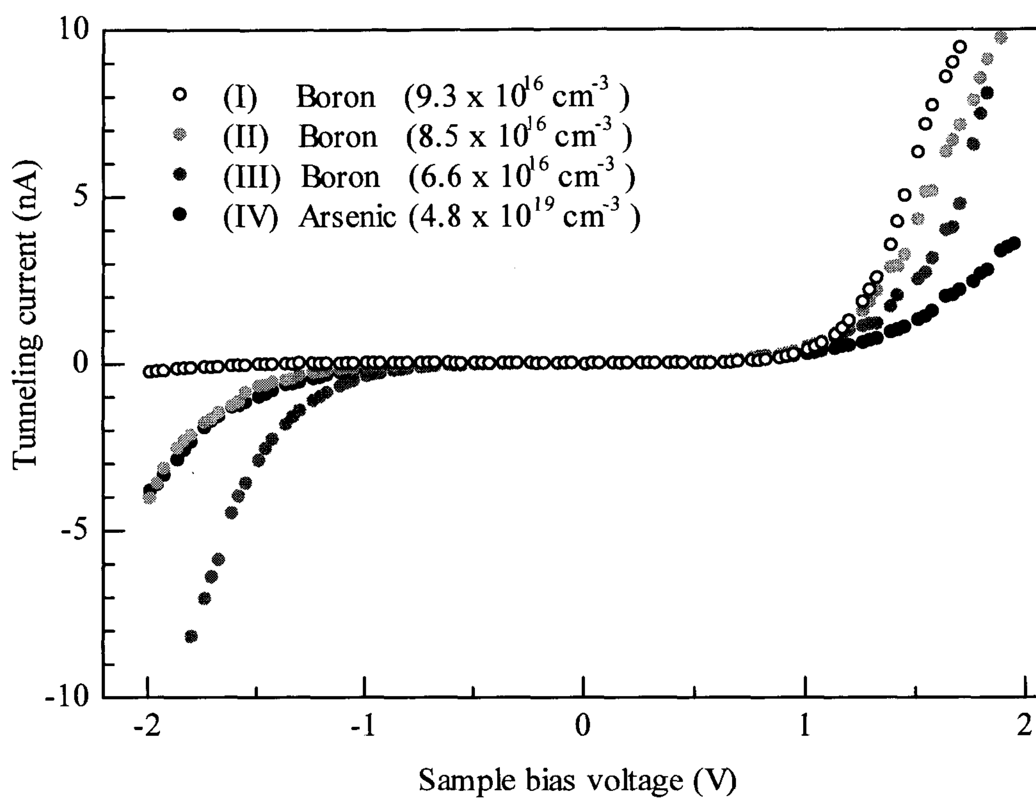


Fig. 3.11. I_t-V_s characteristics taken at the regions labeled (I)–(IV) are plotted. The dopant concentration at each region shown here is estimated from the SIMS profiles.

voltages, the band bends downward toward the surface, which makes a depleted region around the surface (Fig. 3.12(b)). In this condition, the tunneling current hardly increases because of the luck of holes. The I_t-V_s curve taken at (I) shows such characteristic for *p*-type Si and is very similar to that taken on a hydrogen-terminated *p*-type wafer with a carrier concentration of 1×10^{17} cm^{-3}. It is considered that the concentration is consistent with the B concentration of 9×10^{16} cm^{-3} estimated from the SIMS profile at the region 216 nm deep. The curve taken at the area (IV) 20 nm deep indicates the same characteristic as that taken on almost degenerated *n*-type Si wafer with hydrogen-terminated surface, as is expected. For the degenerated *n*-type Si, the electron tunneling from the tip into the conduction band of Si is the main component at positive voltages (Fig. 3.12(c)). At negative sample voltages, the tunneling current has the dopant-induced components originating from electron tunneling out of filled states in the conduction band (Fig. 3.12(d)). It is expected that the much

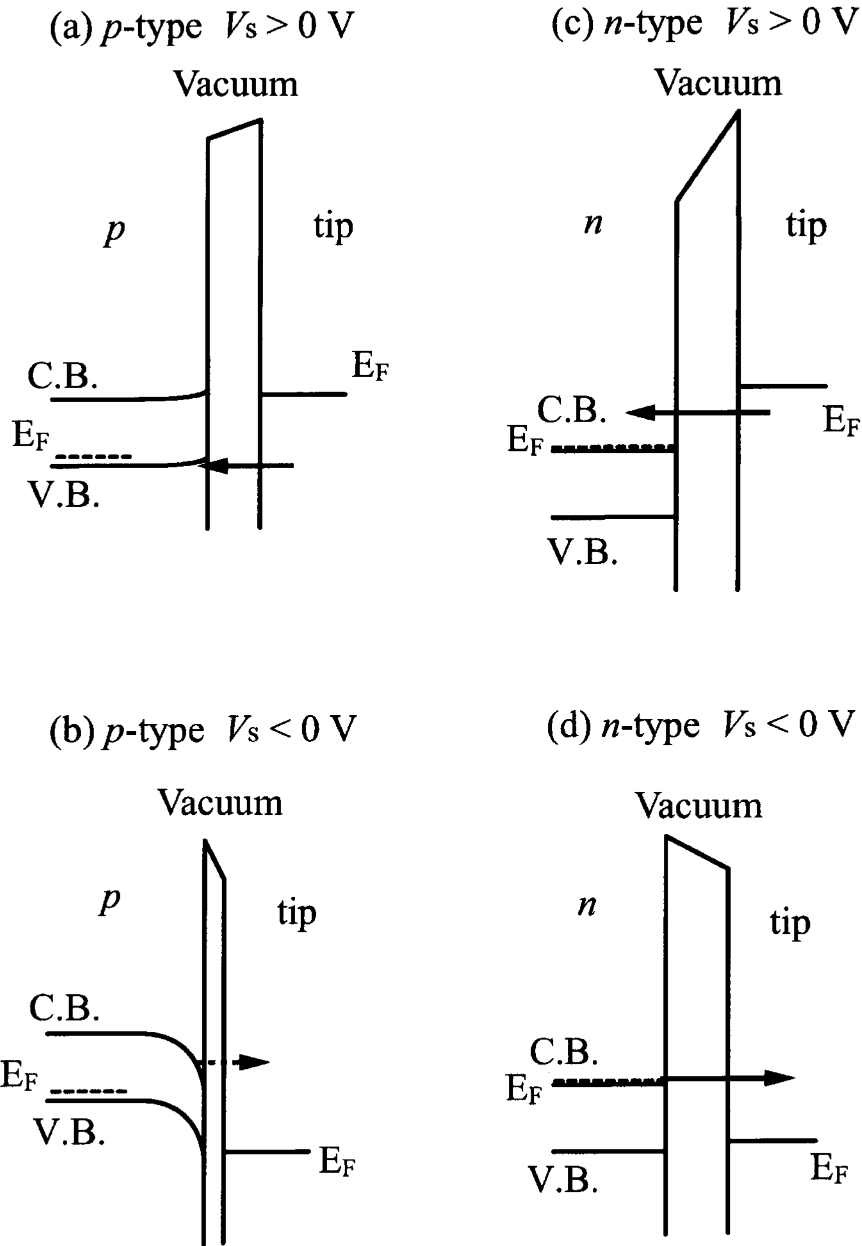
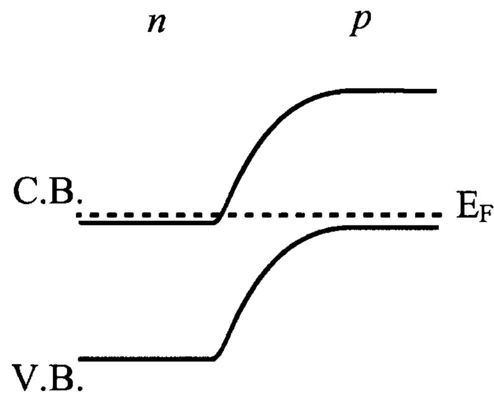
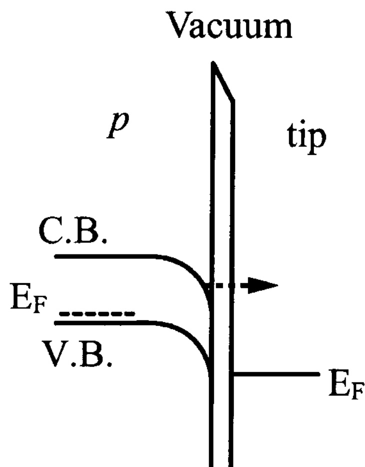


Fig. 3.12. Energy band diagrams representing the components of tunneling current. The main component in each condition is denoted by an arrow. The broken lines in the diagrams indicate the Fermi-level positions. V.B. and C.B. is the valence band and conduction band of the sample.

tunneling current is obtained both at positive and negative sample voltages. However, the I_t-V_s curves acquired at area (IV) shows that the tunneling current does not increase so rapidly as is expected. In the STM image shown in Fig. 3.8(b), this region is observed as a protrusion band. This means that the tip-sample separation for the I_t-V_s measurements is larger at the protrusive region than that at the surroundings since the tip-sample separation is adjusted at each point of the measurements in the condition V_s of 1 V and I_t of 0.2 nA. This results in the rather less current at the degenerated *n*-type region. At a depth of 162 nm (area (II)), the tunneling current shows rapid increase beyond a positive sample bias voltage of 1 V. At negative voltages, the negative tunneling current is rather less than that at positive voltages, which shows depleted characteristic. The B concentration estimated from the SIMS profile is 8.5×10^{16} cm^{-3} at this region. In the case of the I_t-V_s curve taken at a depth of 142 nm (area (III)), the tunneling current steeply increases beyond both at V_s of 1 V and -1 V. The negative tunneling current at negative voltages is obviously more than that obtained at area (II) though the B concentration of 6.6×10^{16} cm^{-3} at this area (III) is slightly different from that at the area (II). It is considered that this feature derives from the depletion layer of the pn^+ junction. In the areas of (II) and (III), the depletion layer of the pn^+ junction exists as is illustrated in Fig. 3.13(a). In the *p*-type regions, the tip-induced band bending toward the surface causes a depletion layer around the surface at negative voltages (Fig. 3.13(b)). The resultant tunneling current hardly increases. In the depleted *p*-type regions, the tip-induced band bending toward the surface causes a depletion layer around the surface at low negative voltages. At rather high negative sample voltages, an inversion layer appears near the surface, which becomes the main component of the tunneling currents as is denoted by an arrow in Fig. 3.13(c). Since the energy difference between the top edge of the valence band and the Fermi-level position is larger at the area (III) than at the area (II), it is easier at the area (II) to form the surface inversion layer. Therefore, the resultant tunneling current increases more steeply at the area (II) than (III). Thus, the observed variation of the I_t-V_s curves reflects not only the dopant concentrations but also the local potential distribution of the pn^+ junction.





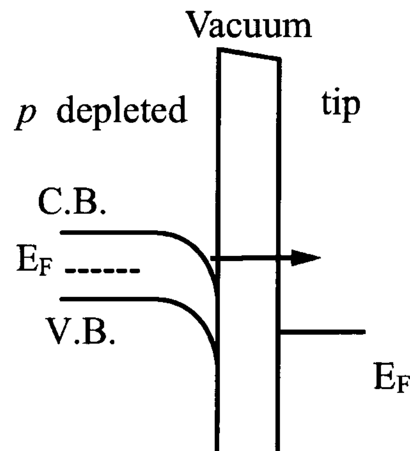


Fig. 3.13. (a) Energy band diagram of the pn^{+} junction. (b), (c) Energy band diagrams for the *p*-type and depleted regions prepresenting the components of tunneling current at a negative voltage. The main component in each condition is denoted by an arrow. The broken lines in the diagrams indicate the Fermi-level positions. V.B. and C.B. is the valence band and conduction band of the sample.

3.3 Summary

The dopant redistribution during the annealing process on the planar nano pn^+ junctions fabricated by the B and As ion implantation are characterized with a use of STM. It is found that the width of the depleted region changes with increasing the annealing time after the implantation. This means that the ionized acceptor concentration in the p-type region changes as the annealing time increases. The changes in ionized acceptor concentration during the annealing are discussed in terms of the diffusions of implanted dopants. It is found that the main cause of the observed changes is the B diffusion into the region damaged by As implantation.

In addition, a pn^+ junction is characterized by cross-sectional STM/STS. The bias voltage dependence of the STM images shows that the corrugation observed by STM reflects the local electrical properties of the p-type and n^+-type regions. The I_t-V_s curves taken at the various areas of the pn^+ junction show obvious differences from each other. Combining with the dopant depth profiles acquired by SIMS measurements, it is found that the I_t-V_s characteristics sensitively reflect the potential distribution of the pn^+ junction.

References

[1] E.G.Roth, O.W.Holland, and D.K.Thomas, Appl. Phys. Lett., **74**, 679 (1999).

[2] R. D. Chang, P. S. Choi, D. L. Kwong, D. Wristers, and P. K. Chu, Appl. Phys. Lett., **72**, 1709 (1998).

[3] N. Aoki, T. Kanemura, and I. Mizushima, Appl. Phys. Lett., **64**, 3133 (1994).

[4] G. A. Sai-Halasz, K. T. Short, and J. S. Williams, IEEE Electron Device Lett., **6**, 285 (1985).

[5] H. Fukutome, S. Hasegawa, K. Takano, H. Nakashima, T. Aoyama, and H. Arimoto, Appl. Surf. Sci., **144-145**, 554 (1999).

[6] H. Fukutome, K. Takano, H. Yasuda, K. Maehashi, S. Hasegawa, and H. Nakashima, Appl. Surf. Sci., **130-132**, 346 (1998).

[7] H. Fukutome, T. Okui, S. Hasegawa, H. Nakashima, T. Aoyama, and H. Arimoto (to be published).

[8] S. M. Sze, *Phyiscs of Semiconductor Devices*, 2nd ed. (John Wiley & Sons, Inc., New York, 1981), Chap. 2.

[9] S. M. Sze, *Semiconductor Devices, Physics and Technology*, 2nd ed. (John Wiley & Sons, Inc., New York, 1985), p. 402.

[10] Joseph A. Stroscio, and William J. Kaiser, *Methods of Experimental Physics Vol. 27 Scanning Tunneling Microscopy*, Edited by Joseph A. Stroscio and William J. Kaiser (Academic Press, Inc., San Diego, 1993), Chap. 4.

[11] V. A. Ukraintsev, P. J. Chen, J. T. Gray, C. F. Machala, L. K. Magel, and M. -C. Chang, J. Vac. Sci. Technol. **B 18**, 580 (2000).

[12] A. Benninghoven, F.G. Rudenauer, H.W. Werner, *Secondary ion mass spectrometry: basic concepts, instrumental aspects, applications, and trends.* (John Wiley & Sons, Inc., New York, 1987).

[13] R. M. Feenstra and J. A. Stroscio, J. Vac. Sci. Technol. **B6**, 1472 (1988).

[14] R. M. Feenstra, E. T. Yu, J. M. Woodall, P. D. Kirchner, C. L. Lin and G. D. Pettit, Appl. Phys. Lett. **61**, 795 (1992).

4. Visualization of the MOSFET

Recently, many semiconductor devices have been miniaturized to improve their performance. In the case of the metal-oxide-semiconductor field-effect transistor (MOSFET) structure, the channel length has shrunk and the junction depth has become shallower. The resultant dimensions thus become comparable to the source/drain depletion width. This causes several issues that need to be resolved, such as the short channel effect and so on.[1] Thus, the accelerated reduction of feature size in Si devices requires new techniques for characterizing their structures on a nanometer scale. In this chapter, a 0.1 μm-scale MOSFET structure is investigated on a nanometer scale by STM.

4.1 STM images of the MOSFET structure

An *n*-channel MOSFET structure was fabricated on a *p*-type Si (001) wafer ($\rho = 0.2\ \Omega\cdot$cm) by an electron beam lithographic technique and As ion implantation (Fig. 4.1). The wafer was thermally oxidized to grow a gate oxide layer 4 nm thick. *Poly*-Si gates 100-120 nm long and 180 nm high were then aligned along the <110> axis with a periodicity of 300 nm. Arsenic ion implantation was performed at 10 keV, with a dose of 4×10^{14} cm^{-2} for the source/drain extensions. After the formation of the spacer oxide, As ions were implanted for the n^+-type doping of the source/drain regions and the *poly*-gates (30 keV, 1×10^{14} cm^{-2}). Activation of the implanted dopants was achieved by rapid thermal annealing at 1000 °C for 10 seconds. Next, a *poly*-Si layer 500 nm thick was deposited as a protective cap layer for the cross-sectional STM measurements. The samples were cross-sectioned using standard techniques. The (110) cross-section of the structure was chemically and mechanically polished, finishing with colloidal silica emulsion to realize smooth surface. In order to evaluate the electrical characteristics through the surface, it is necessary to significantly decrease the surface states in the band gap. It has already described, in chapter 2, that the chemical wet etching of a thermally oxidized (001) surface yields a hydrogen-terminated surface with a low density of surface states. Therefore, to realize cross-sectional surface without surface states, the cross-sectioned sample was thermally oxidized at 800 °C for 30 minutes in dry O_2. Before the STM measurements, the sample surface was hydrogen-terminated. The STM measurements were

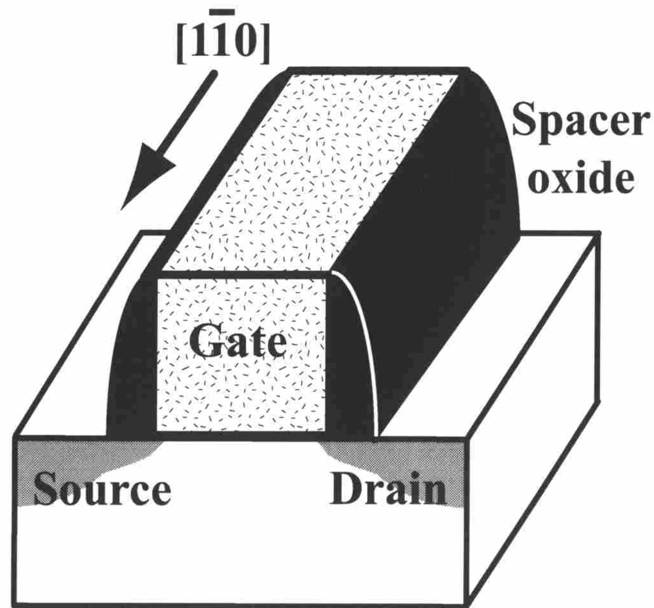


Fig. 4.1. Schematic illustration of the MOSFET.

performed in constant current mode with tungsten tips in a UHV-STM chamber. A common electrode for the STM measurements was connected to the *p*-substrate, the source/drain and the gates.

Figure 4.2(a) shows a topographic STM image of the MOSFET structure observed through the hydrogen-terminated (110) cross-section. The image was taken in constant current mode at a sample bias voltage of 5 V and a tunneling current of 0.2 nA. At the top of the image, part of a *poly*-Si gate can be observed as a bright pentagon. The noticeably depressed regions beside the gate indicate parts of the spacer oxide. Figure 4.2(b) shows a magnified STM image of Fig. 4.2(a) around the thin gate oxide area. The gate oxide is observed as a thin ditch under the gate (indicated by an arrow) since the HF and HCl solution etched the gate oxide. The source/drain regions are slightly depressed compared with the surrounding *p*-substrate region. It is considered that the depression results from the difference in the oxidation rate between n^+-type and *p*-type Si.[2] During the thermal oxidation of the cross-sections, the oxide layer in the n^+-type source/drain region grew thicker than that in the *p*-type substrate, which leads to the depression in the source/drain regions after the chemical etching.

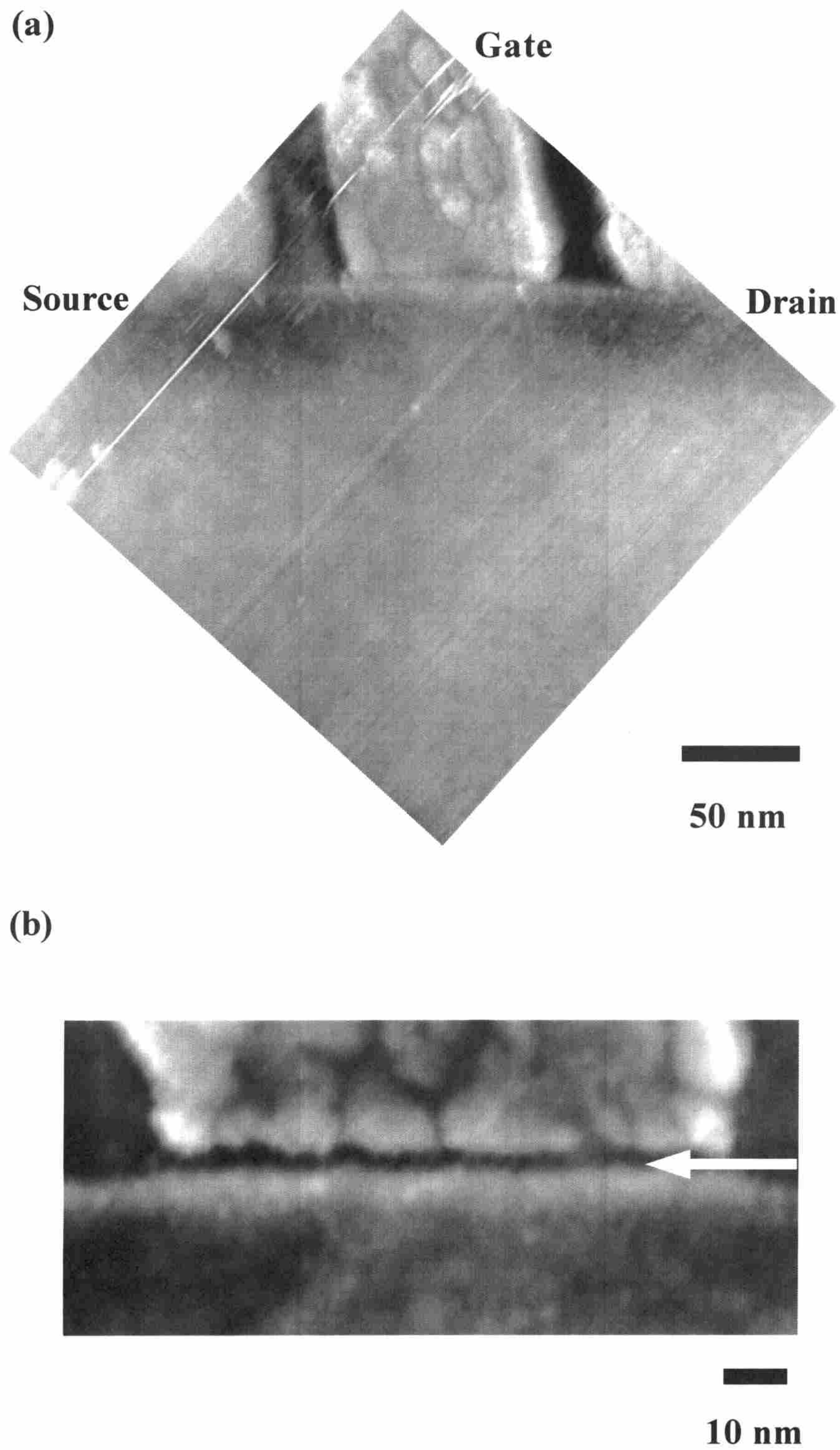


Fig. 4.2. (a) Topographic cross-sectional STM image of the MOSFET taken at a sample bias voltage $V_s = 5$ V and tunneling current $I_t = 0.2$ nA. (b) Magnified STM image of the gate and the gate oxide.

From the STM images, we can evaluate the dimensions of the feature sizes in the MOSFET structure. The gate length of 85 nm is somewhat shorter than the value of 100-120 nm measured by critical dimension scanning electron microscopy (CD-SEM). It is considered that the resultant value is reasonable since the value measured by CD-SEM is possibly more than the real value. The ditch under the gate is 3.5 nm thick, which is slightly thinner than the 4 nm gate oxide layer thickness, because of the convolution effect of the STM tips. It is also estimated from the image that the source/drain regions are approximately 48 nm deep. The measured depth of the source/drain shows good agreement with the value estimated from the initial ion implantation energy and subsequent annealing. The projected range and the straggle for As implanted at 30 keV are 20 nm and 8 nm, respectively.[3] The As distribution subsequently broadens by 20-30 nm during the rapid thermal annealing at 1000 °C for 10 seconds.

An STM image taken at a sample bias voltage of 1 V is shown in Fig. 4.3(a). In the image, an *n*-channel region is clearly observed as a depressed area just under the gate and gate oxide. The bumps to the right and left sides of the channel correspond to the source/drain and the extension regions, which are observed as slight depressions at a sample bias voltage of 5 V in Fig. 4.2(a). Figure 4.3(b) shows the line profile between the source and drain (the broken line in Fig. 4.3(a)) on the STM images. The profile indicates the difference in height between the channel region and the source/drain region. The channel region for the profile taken at 1 V is much deeper than the source/drain region. In the channel region, it is considered that the depletion layer exists, which has the much lower carrier density than the *p*-substrate. Therefore, the STM tip approaches the surface, leading to the depression in the STM image. It is estimated from the profile that the channel length is 52 nm.

Here, let us discuss about the bias voltage dependence of the STM images. In the STM image taken at 5V, the source/drain regions are slightly depressed compared with the channel region. By contrast, the source/drain regions are greatly protrusive in the image taken at 1 V. This bias voltage dependence can be explained by considering the band diagrams for the tip-vacuum-sample.[4] Figure 4.4 shows schematic band diagrams of the *p*-type and the n^+-type regions toward the direction perpendicular to the surface when the tip is close to each region. At a sample bias voltage of 5 V, electrons can tunnel from the tip into the conduction band for both *p*- and n^+-type regions (Figs. 4.4(a) and (b)). In the condition, the *p*- and n^+-type regions do not show any difference in the STM

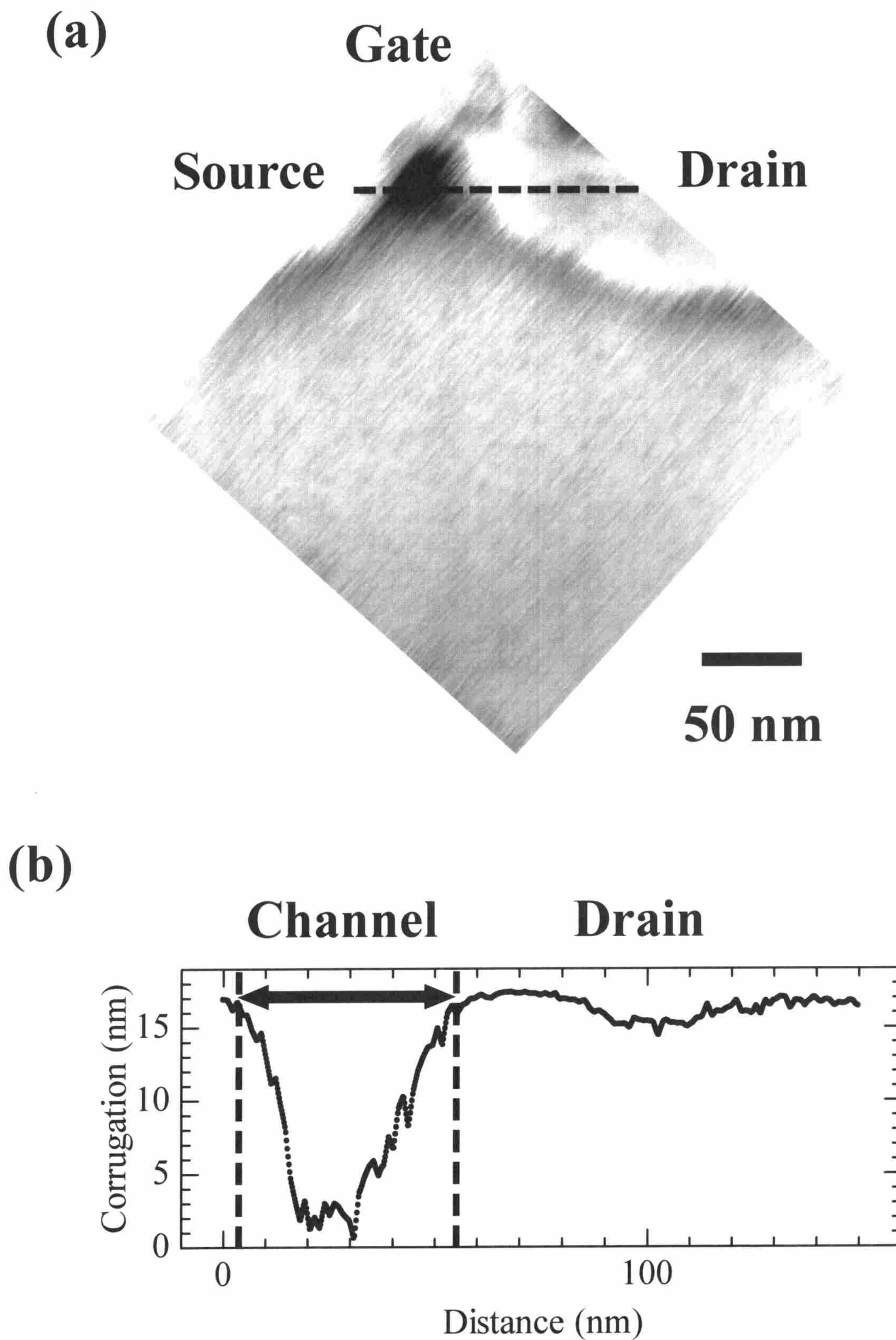


Fig. 4.3. (a) Topographic cross-sectional STM image taken at $V_s = 1$ V and $I_t = 0.2$ nA. (b) Line profile from the source to the drain on the STM image.

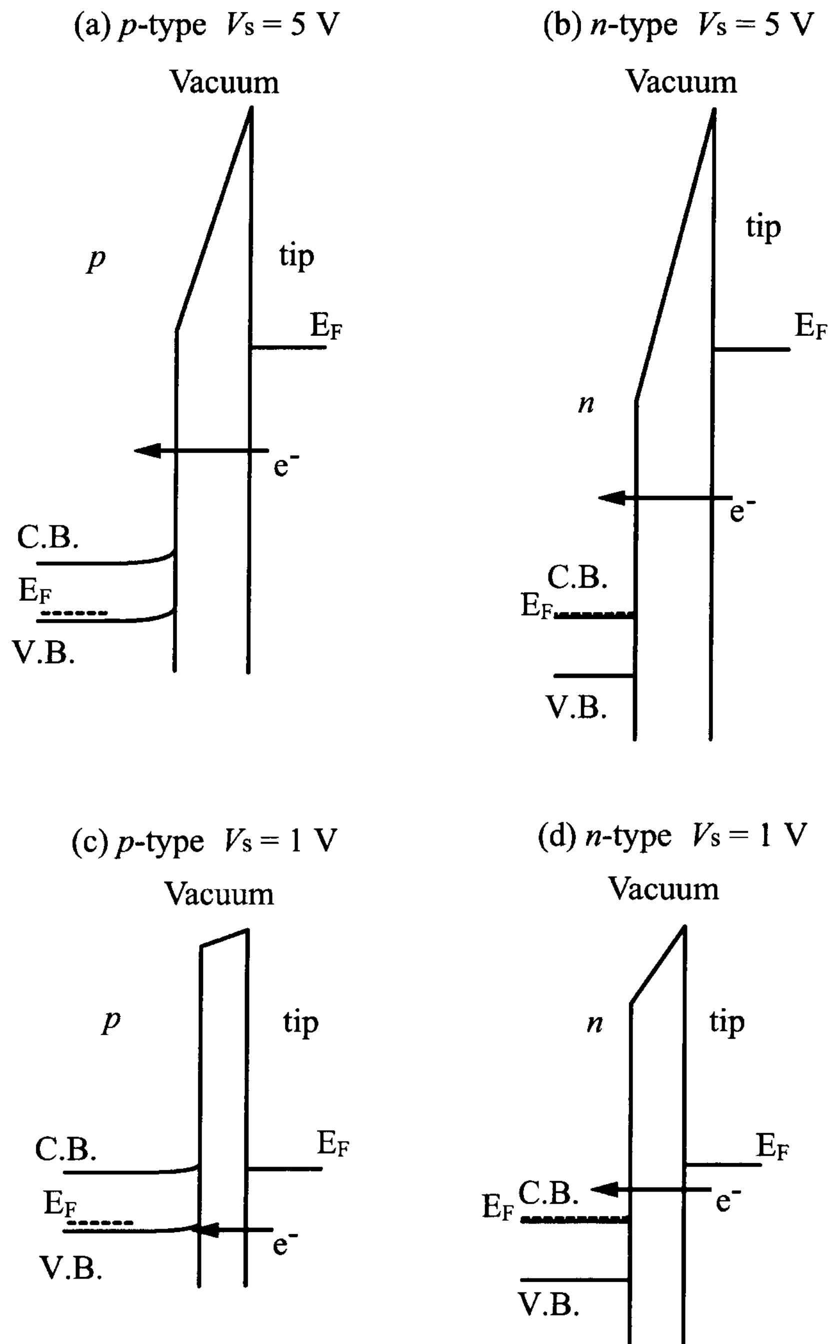


Fig. 4.4. Schematic band diagrams of the p-type and the n^+-type regions toward the direction perpendicular to the surface when the tip is close to each region. Here, E_F is the Fermi level, V.B. is the valence band of the sample, and C.B. is the conduction band.

image. At a sample bias voltage of 1 V, for the p-type region (Fig. 4.4(c)), electrons can tunnel from the tip into the valence band of the sample, where the band bends upward resulting in the accumulation of holes. For the n^+-type region, electrons can tunnel from the tip into the conduction band of the sample, as is shown in Fig. 4.4(d). In both cases, it is easy for tunneling current to flow. A possible explanation for the different contrasts is the barrier height difference. The barrier height for the tunneling, which is defined to be the energy difference between the tunneling level and the vacuum level, is higher for p-type region than for the n^+-type region. In addition, it is considered that the carrier density is much higher in the n^+-type region than that in the channel region. Therefore, in the n^+-type region, since it is easier for electrons to tunnel into the n^+-type region than into the channel region, the STM tip rises away from the surface in order to keep the tunneling current constant (Fig. 4.5). This bias voltage dependence provides the evidence that the topographic STM images reflect not only the actual surface roughness but also the electrical properties of each region.

Apart from the visualization of the device structures, it is also found that networks of depressed lines can be observed, not only in the *poly*-Si gates, but also in the *poly*-Si cap layers in Fig. 4.2(a).

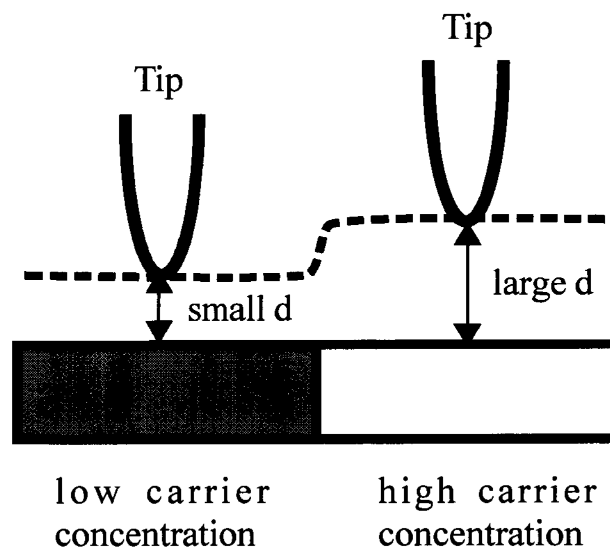


Fig. 4.5. Schematic drawing of STM on the regions with different carrier densities.

These networks are considered to be *poly*-Si grain boundaries. Therefore, cross-sectional STM observation also has the potential to evaluate various process parameters on a nanometer scale.

4.2 Summary

A 0.1μm MOSFET structure has been visualized on a nanometer scale by using STM. Topographic STM images taken at an appropriate bias voltage reveal the source/drain, gate, channel, gate oxide and spacer of the MOSFET. The dimensions of the gate length, channel length and source/drain depth evaluated from the STM images agree with the target values. In addition, the bias voltage dependence of the STM images shows that the depressed channel region observed in the STM image taken at 1V reflects the fact that it has a lower carrier density than its surroundings. This provides the evidence that STM not only has the potential to characterize nano-scaled MOSFET structures, but also to reveal their local electrical properties by observing hydrogen-terminated cross-sections.

References

[1] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (John Wiley & Sons, Inc., New York, 1981), Chap. 8.

[2] L. E. Katz, *VLSI Technology*, 2nd ed., edited by S. M. Sze (McGraw-Hill Book Company, New York, 1988), Chap. 3.

[3] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (John Wiley & Sons, Inc., New York, 1981), Chap. 2.

[4] J. Tersoff and N. D. Lang, *Methods of Experimental Physics Vol. 27 Scanning Tunneling Microscopy*, Edited by Joseph A. Stroscio and William J. Kaiser (Academic Press, Inc., 1993), Chap. 1.

5. Two-dimensional potential profiling of a MOSFET

With the aggressive scaling of MOSFETs approaching gate lengths of shorter than 100 nm, determining the cross-sectional potential profile of miniaturized MOSFETs and specifically the direct measurement of their channel length is necessary for true channel engineering to be possible. STM/STS has the capability to provide the potential distribution with a two-dimensional spatial resolution. In this chapter, potential profiling of a MOSFET is demonstrated by STM/STS.

5.1 How to map the potential profiles

The electrical property of the MOSFET is characterized by current imaging tunneling spectroscopy[1] (CITS). The I_t-V_s characteristic on each point shows the local electrical properties of the MOSFET. The I_t-V_s characteristics are converted into the potential by referring to those taken on the pn^+ junction characterized in Chap. 3. Each I_t-V_s curve of the MOSFET is compared with the I_t-V_s curves of the pn^+ junction. Given that the same I_t-V_s characteristic indicates the regions with a same potential, it is possible to estimate the potential on each region of the MOSFET.

5.2 I_t-V_s characteristics mapping of the MOSFET

The local I_t-V_s characteristics are analyzed around the channel region of the MOSFET structure. Figure 5.1 shows the magnified topographic STM image taken at a sample bias voltage V_s of 1V and a tunneling current I_t of 0.2 nA with the CITS measurement. The area of the STM image is sketched also in Fig. 5.1. Part of the gate is observed as a triangle protrusion at the top, and parts of the source/drain are observed as bumps left and right sides below the gate.[2] The depressed region appears in the p-type substrate surrounding the source/drain, indicating the depleted region of the MOSFET.

The I_t-V_s curves taken at three regions labeled A, B, and C are plotted by gray closed circles, open and closed circles in Fig. 5.2. The tip-sample separation is adjusted at V_s of 1 V and I_t of 0.2 nA. It is found that the I_t-V_s curve taken at region A shows the almost similar characteristic to that of a p-type wafer with resistivity of 0.2 Ω·cm. It is considered that the region A indicates the p-type substrate region. The curve taken at the region B indicates the characteristic of almost degenerated n-type Si, which shows the source/drain region. In the STM image shown in Fig. 5.1, this region is observed as a protrusion. Since the tip-sample separation is adjusted at V_s of 1 V and I_t of 0.2 nA

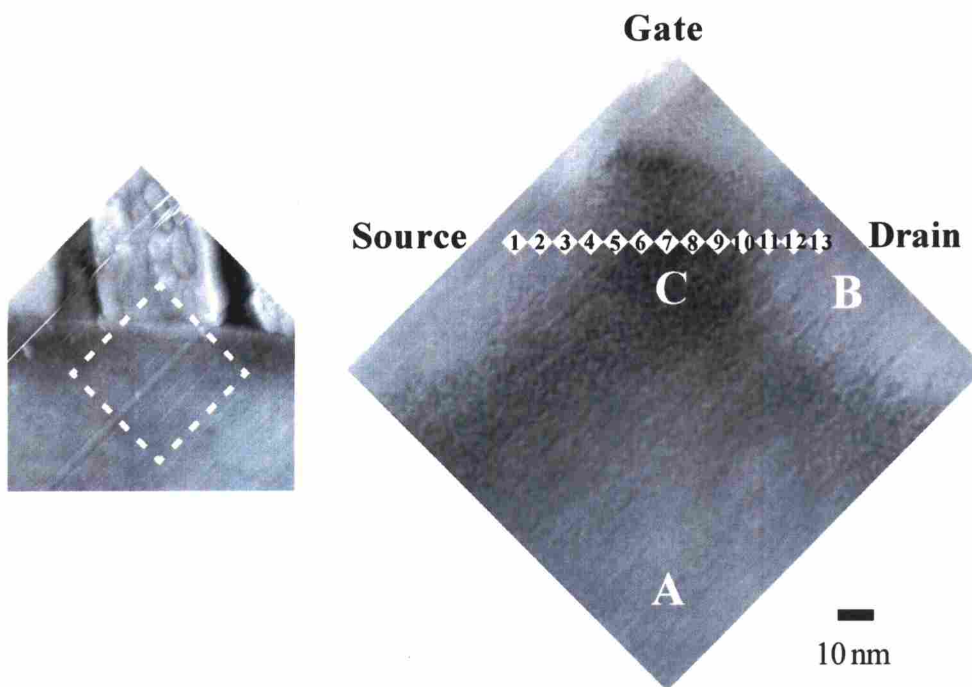


Fig. 5.1. Topographic cross-sectional STM image of the MOSFET. Sample bias voltage V_s = 1.0 V and tunneling current I_t = 0.2 nA.

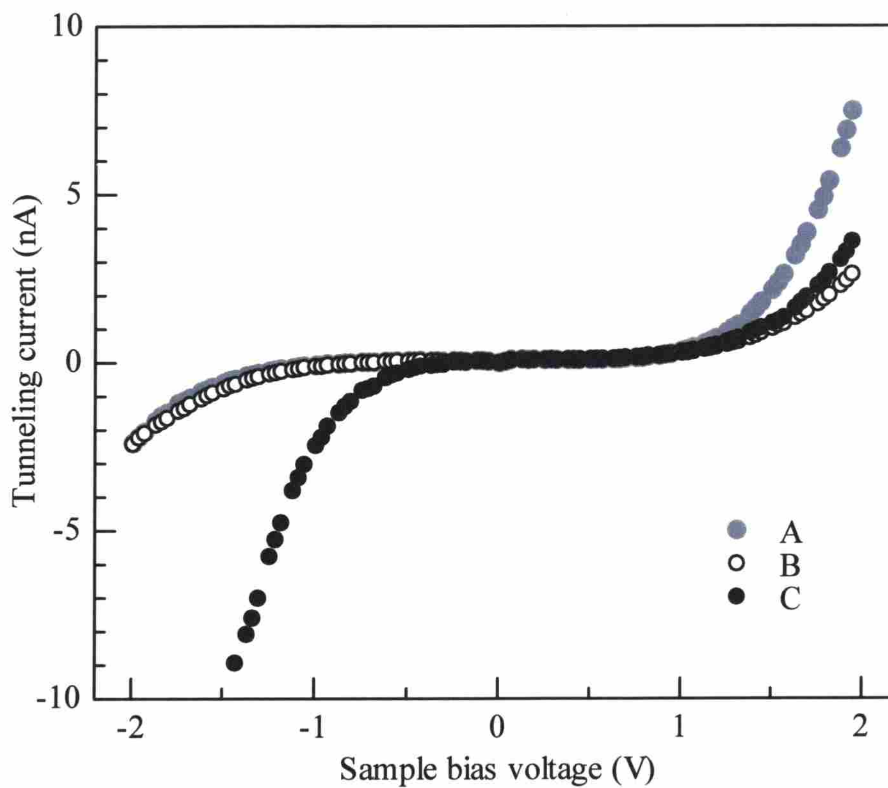
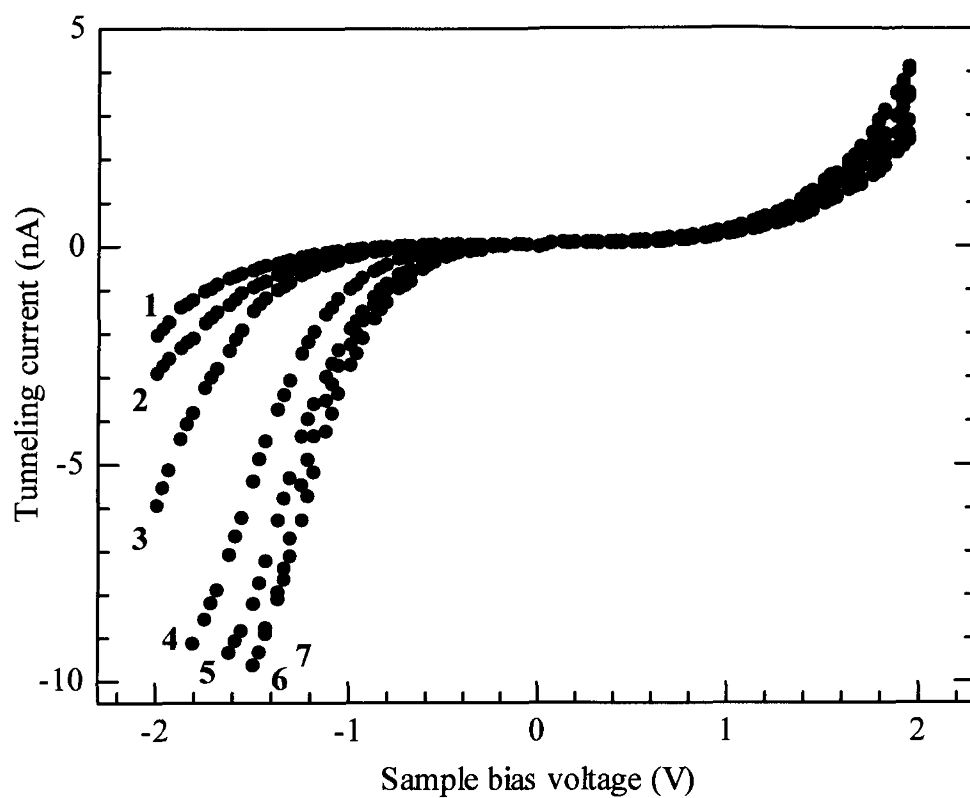


Fig. 5.2. I_t-V_s characteristic on each region of A, B, or C shown in Fig. 5.1.

at each point of the measurements, the adjusted tip-sample separation for the I_t-V_s measurements is large at the region B. This results in the rather slight increase in the tunneling current at the degenerated n-type region. The I_t-V_s curve taken at the channel region (region C) reveals a depleted characteristic. It is considered that the depletion layer of the pn^+ junction between the source/drain and the p-substrate exists in this channel region. Thus, local I_t-V_s characteristics reflect the electrical properties of each region.

Figure 5.3 shows how the I_t-V_s curves change along regions 1-13 of 5×5 nm^2 in Fig. 5.1. Beginning from the region 1, the degenerated n-type characteristic of the I_t-V_s curve steeply changes into lower n-type one of the region 3. From the region 3 to 4, the I_t-V_s curve obviously changes into the depleted one indicating the graded potential variation. The I_t-V_s curve from the regions 4 to 7 shows the depleted characteristics in the channel region. Beyond the region 7, the I_t-V_s curve change back into n-type, and then the degenerated n-type features steeply start to come back at the region 11. This change of the I_t-V_s characteristics along the channel is quite reasonable for the present MOSFET. It is found that the depleted feature shown in the I_t-V_s curve at the region 4-11 reflects the potential difference in the channel region. It is estimated that the channel length is 56 nm assuming that the depleted area of region 4-11 is the channel region.

The I_t-V_s curves are taken at each region of 5×5 nm^2 and classified by analyzing their characteristics. The mapping of the I_t-V_s characteristics on the MOSFET is shown in Fig. 5.4. In the source/drain regions, almost uniform I_t-V_s characteristics indicating degenerated n-type features are obtained. From the source/drain into the channel region, the I_t-V_s characteristics steeply change, and then they remain almost same in the channel region. Around the source/drain, the depletion layer exists, where the characteristics gradually change, as is plotted by the green colors. Uniform p-type substrate regions appear on the bottom. Thus, the I_t-V_s characteristics mapping reveals the two-dimensional distribution of the electrical properties on the MOSFET structure.



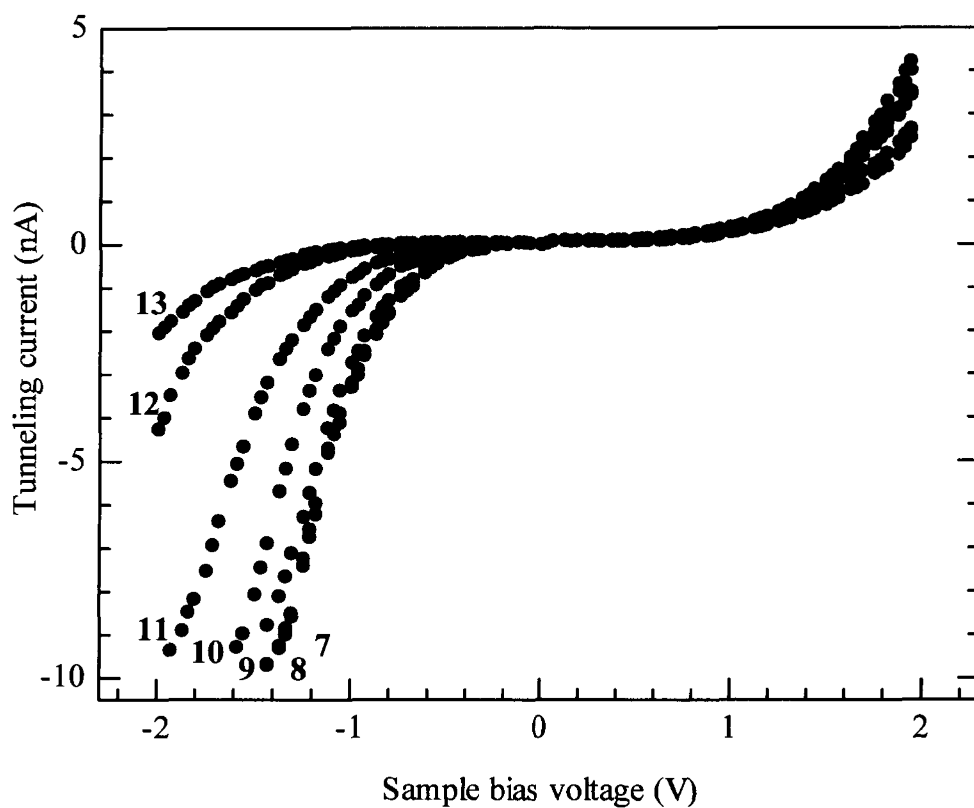


Fig. 5.3. I_t-V_s characteristic on each 5 × 5 nm^2 region labeled 1–13 in Fig. 5.1.

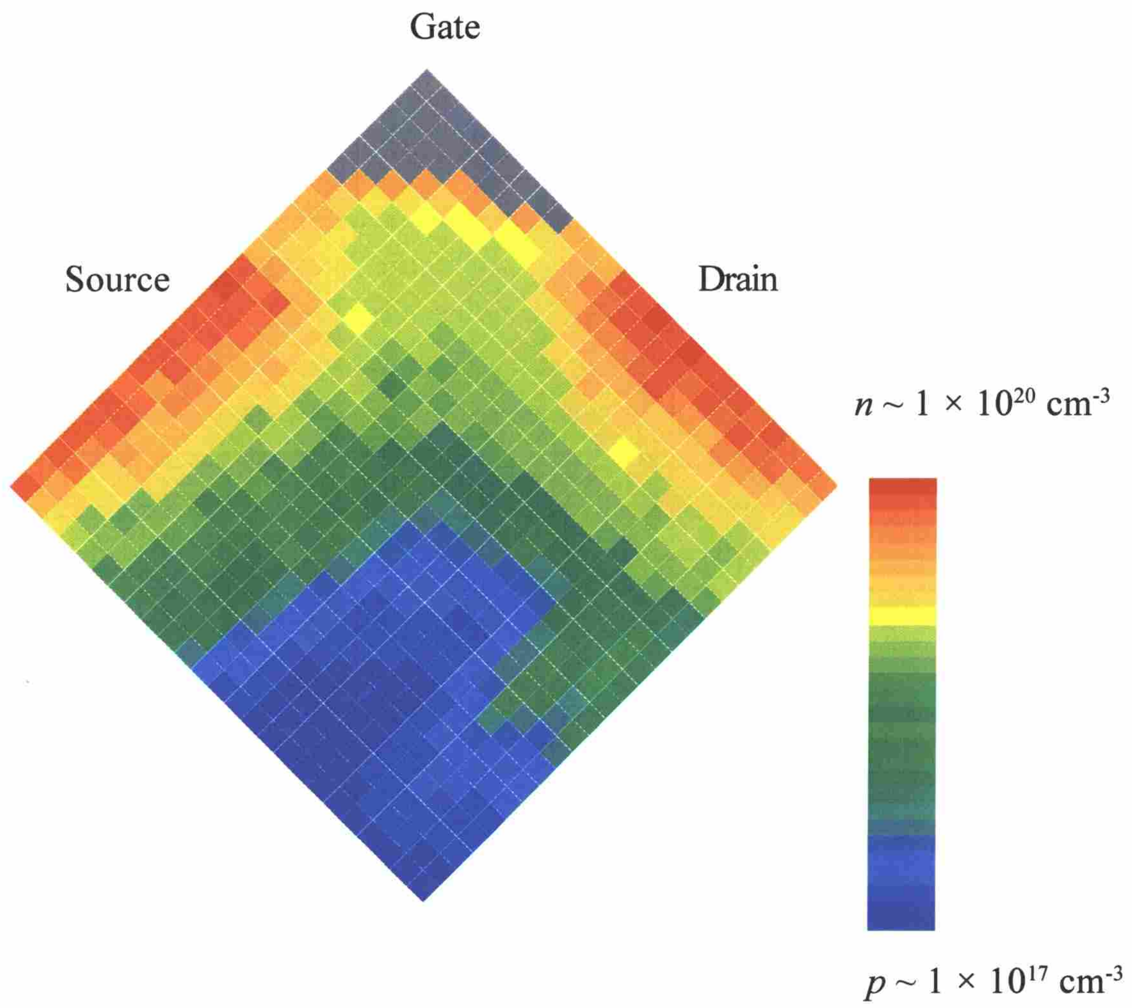


Fig. 5.4. I_t-V_s characteristics mapping of the MOSFET.

5.3 Potential distribution on the pn^+ junction

In order to realize the potential mapping of the MOSFET, the I_t-V_s characteristics of the pn^+ junction, which is characterized in Chap. 3, are converted into the potential by referring the corresponding SIMS dopant profiles. The one-dimensional potential profile of the pn^+ junction is calculated from the carrier concentration profile. The carrier concentration is defined to be the difference between B and As concentrations and is plotted in Fig. 5.5. The depth of the pn^+ junction is estimated to be 80 nm. The n-type carrier concentration steeply increases from the junction toward the surface, while the p-type carrier concentration gradually increases toward the p-substrate. The calculated potential is plotted with respect to the p-type region also in Fig. 5.5. From the potential distribution, it is found that the depletion layer width of the pn junction is 153 nm, consisting of 43 nm in the n-type region and 110 nm in the p-type region. Figure 5.6 shows a various I_t-V_s curves taken at areas of 6.7×6.7 nm^2 from near the surface (area A) to 216 nm deep (area T). The I_t-V_s curves are classified into 20 types labeled A-T, and the curves are converted into the potential by referring the depth dimension. The I_t-V_s characteristic distribution is consistent with the potential distribution in the depletion layer and the potential at each area is summarized in Table 5.1. It is found that the I_t-V_s curve differs from each other corresponding to the potential difference. Thus, the I_t-V_s characteristics sensitively reflect the potential variation of the pn^+ junction.

Table 5.1. The potential at each area labeled A–T.

I-V type	Depth	Potential		*I-V* type	Depth	Potential
A	20 nm	0.877 V		K	128 nm	0.222 V
B	37 nm	0.877 V		L	135 nm	0.179 V
C	54 nm	0.800 V		M	142 nm	0.140 V
D	61 nm	0.748 V		N	149 nm	0.105 V
E	68 nm	0.694 V		O	155 nm	0.0781 V
F	74 nm	0.644 V		P	162 nm	0.0510 V
G	83 nm	0.564 V		Q	169 nm	0.0289 V
H	105 nm	0.393 V		R	179 nm	0.0077 V
I	115 nm	0.310 V		S	183 nm	0.0029 V
J	122 nm	0.262 V		T	216 nm	0 V

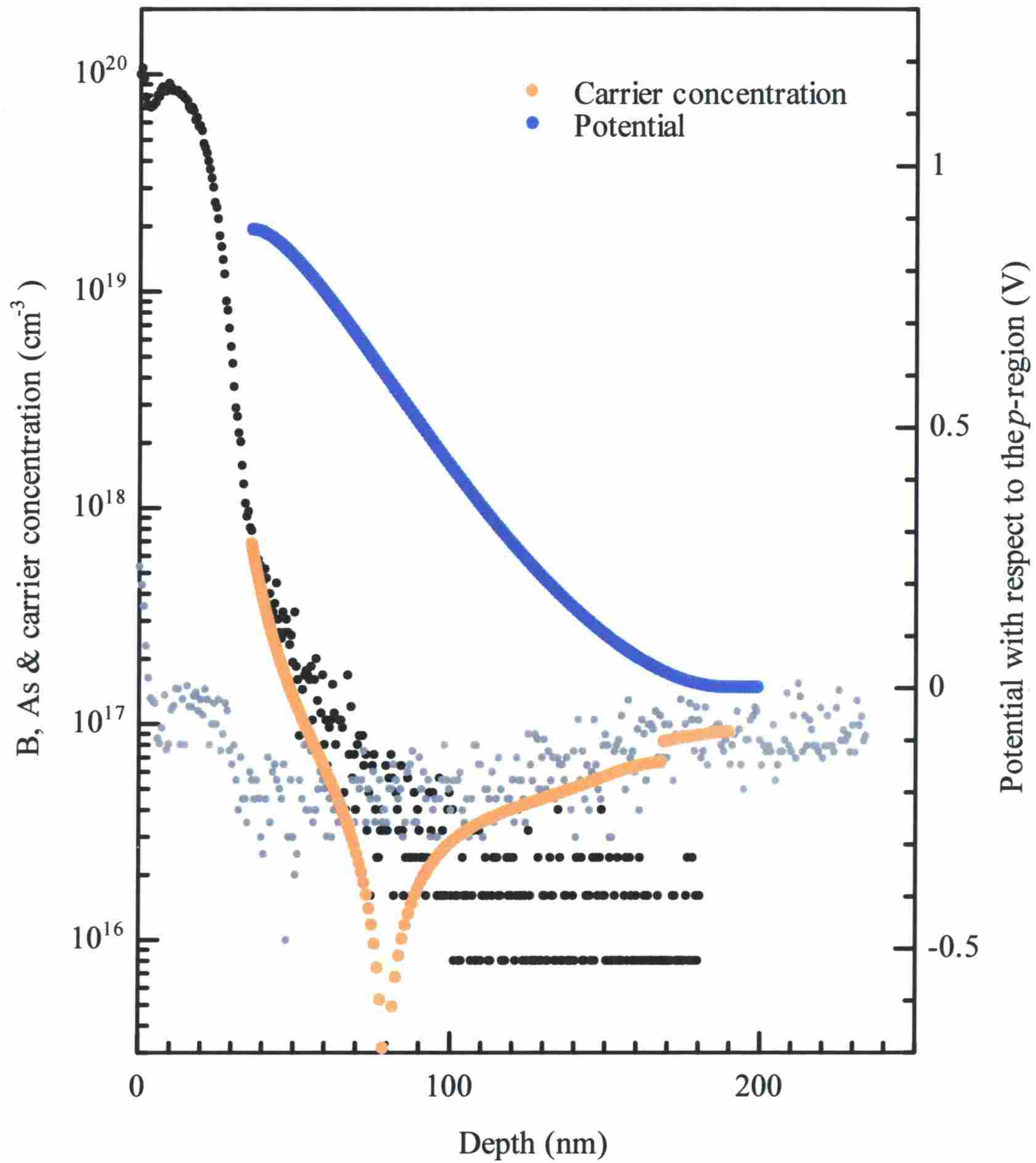


Fig. 5.5. One-dimensional carrier concentration and potential profile of the pn^+ junction plotted by arange and blue dots. B and As concentrations are also shown.

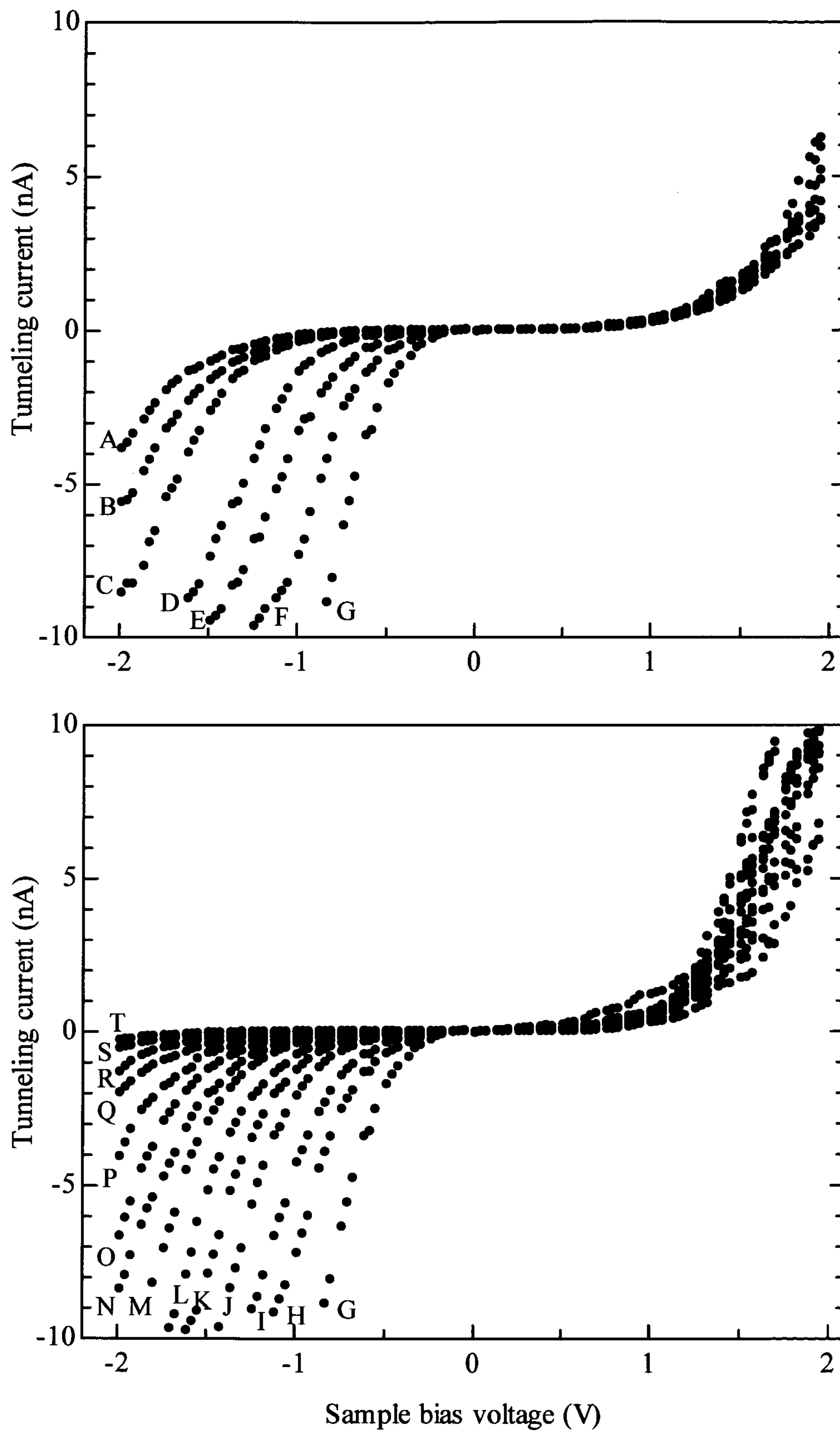


Fig. 5.6. I_t-V_s characteristics taken at the areas near the surface (area A) to 216 nm deep (area T) are plotted.

5.4 Potential profiling of the MOSFET

Based on the consideration, a map showing the distribution of the potential is successfully deduced from analyzing the I_t-V_s curves. An example of the analysis is shown below. An I_t-V_s curve is taken from a region of the MOSFET and plotted by open circles in Fig. 5.7. The I_t-V_s curve is compared with I_t-V_s curves A-T obtained from the pn^+ junction. In the case shown in Fig. 5.7, the I_t-V_s curve of MOSFET is consistent with type E on the pn^+ junction (closed circles). It is estimated that the potential of the region is same as the potential of type E, 0.694 V.

Figure 5.8 shows the potential profile of the MOSFET in the same area as that shown in Fig. 5.4. The areas with a constant potential reveals the n^+-type source/drain, and the channel region appears as a potential valley existing between the source and the drain under the gate. In the region surrounding the source/drain, the depletion layer with gradual potential variation is clearly visualized. The p-type substrate region with a potential of 0 V exists at the bottom of the map. Thus, the CITS measurements realize the spatial profiling of the potential with a high resolution of 5 nm.

The potential in the channel is 0.694 V, which is lower than that at the source/drain of 0.877 V by 0.183 V. The potential drop is much smaller than that expected. It is considered from the value that an inversion layer is formed in the channel region without applying the gate voltage. In contrast to the result, it is estimated from the MOSFET structure that the potential at the channel region is much lower indicating a depleted region. The difference between the estimated and the resultant values possibly derives from the baring the cross-section.

There are some areas without any plots in Fig. 5.8. The I_t-V_s curves at the areas are not consistent with any characteristics of those classified 20 types (A-T) on the pn^+ junction. In addition, the regions with a potential between 0.644 V and 0.262 V do not appear in the profile of MOSFET. A possible cause for these features is some surface related effects such as surface states.

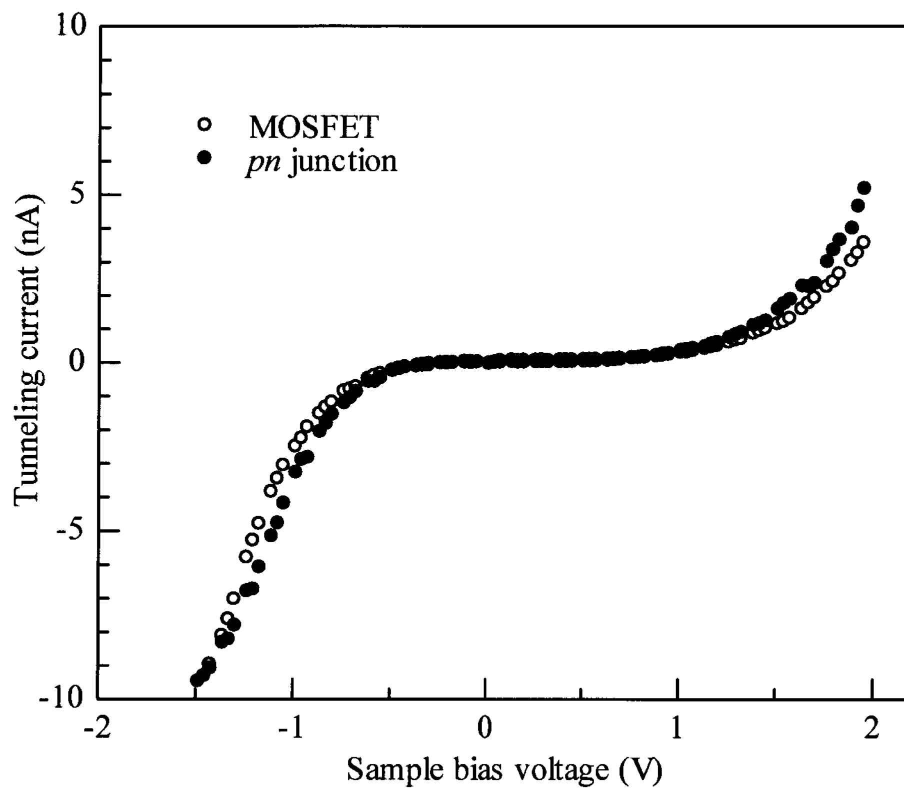


Fig. 5.7. An example of a comparison between two I_t-V_s characteristics obtained from the MOSFET and the pn^+ junction.

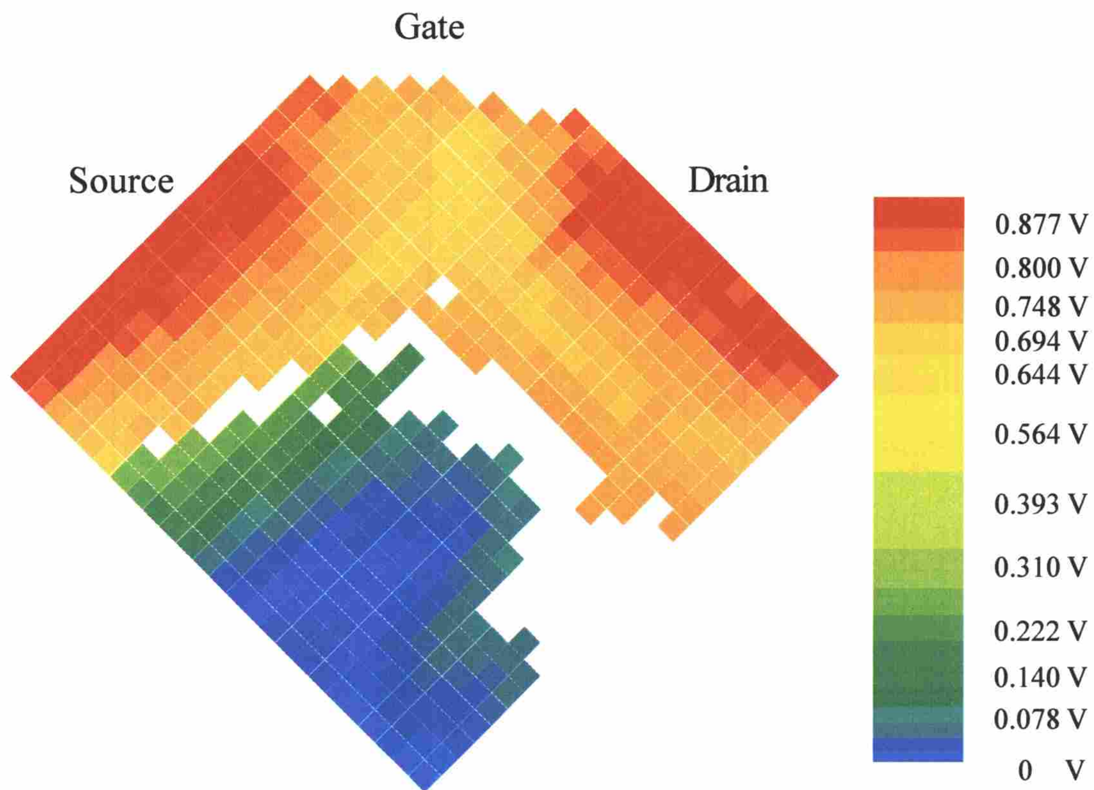


Fig. 5.8. Potential profile of the MOSFET.

5.5 Summary

Local electrical properties of the MOSFET can be obtained from the I_t-V_s curves taken by CITS measurements. A spatial potential distribution converted from the I_t-V_s characteristics reveals the uniform source/drain regions. The channel region is clearly appeared in the I_t-V_s map and potential profile, and it is estimated from the plots that the channel length is 56 nm. It is concluded that the two-dimensional potential profiling is realized with a spatial resolution of 5×5 nm^2 by cross-sectional STM/STS.

References

[1] J. Tersoff and N. D. Lang, *Methods of Experimental Physics Vol. 27 Scanning Tunneling Microscopy*, Edited by Joseph A. Stroscio and William J. Kaiser (Academic Press, Inc., San Diego, 1993), Chap. 4.
[2] T. Okui, S. Hasegawa, H. Nakashima, H. Fukutome, and H. Arimoto, to be submitted to Appl. Phys. Lett.

6. Conclusions

In this study, a 0.1 μm-scale MOSFET structure is characterized on a nanometer scale with the use of cross-sectional scanning tunneling microscopy/scanning tunneling spectroscopy (STM/STS). The main achievements of the study are summarized as follows:

Chapter 2.

Various ways of surface preparation are examined to realize appropriate surfaces for STM measurement. The thermal oxidation is one of the best ways for hydrogen-termination by the chemical etching through it causes the dopant diffusions. The chemical oxidation by a HNO_3 almost works well and does not affect the dopant distributions. It is concluded that the chemical oxidation becomes appropriate way to characterize dopant profiles on device structures when it is more examined for reliability.

Chapter 3.

The dopant redistribution during the annealing process on planar nano pn^+ junctions fabricated by the B and As ion implantation are characterized with STM. It is found that the width of the depleted region changes with increasing the annealing time after the implantation. This means that the ionized acceptor concentration in the p-type region changes as the annealing time increases. It is found that the main cause of the observed changes is the B diffusion into the region damaged by As implantation.

The bias voltage dependence of the cross-sectional STM images of a pn^+ junction show that the corrugation observed by STM reflects the local electrical properties of the p-type and n^+-type regions. The I_t-V_s curves taken at the various areas of the pn^+ junction show obvious differences from each other. Combining with the dopant depth profiles acquired by SIMS measurements, it is found that the I_t-V_s characteristics sensitively reflect the potential distribution of the pn^+ junction.

Chapter 4.

A 0.1*m*m MOSFET structure has been visualized on a nanometer scale by using STM. Topographic STM images taken at an appropriate bias voltage reveal the source/drain, gate, channel, gate oxide and spacer of the MOSFETs. The dimensions of the gate length, channel length and source/drain depth evaluated from the STM images are consistent with the target values. In addition, the bias voltage dependence of the STM images shows that the depressed channel region observed in the STM image taken at 1 V reflects the fact that it has a lower carrier density than its surroundings. This provides the evidence that STM not only has the potential to characterize nano-scaled MOSFET structures, but also to reveal their local electrical properties by observing hydrogen-terminated cross-sections.

Chapter 5.

Local electrical properties of the MOSFET can be obtained from the I_t-V_s curves taken by CITS measurements. A spatial potential distribution converted from the I_t-V_s characteristics reveals the steep junctions at the source/drain edge. The channel region is clearly appeared in the potential map, and it is estimated from the plots that the channel length is 56 nm. It is concluded that the two-dimensional potential profiling is realized with a spatial resolution of 5×5 nm^2.

It is concluded that the two-dimensional potential profiling on a 0.1 μm-scale MOSFET structure is revealed by cross-sectional STM/STS. The resultant potential profile can be directly converted to the carrier concentration profile and become a great help to improving the established devices. The spatial resolution make it possible to realize the potential profiling on nanometer-scale devices, which will be fabricated in the next decade.

Acknowledgements

It is a pleasant task to thank all those who helped in writing this thesis. The author is very grateful to Professor Hisao Nakashima of the Institute of Scientific and Industrial Research, Osaka University, who interests her in the semiconductor physics and gave much encouragement for the exploration of the subject. Sincere thanks are due to Professor S. Hiyamizu and Professor T. Kawai for their valuable comments and reading of the manuscript. The author is especially indebted to Dr. S. Hasegawa for his helpful suggestions, comments and discussions to the manuscript; his valuable comments and discussions in the subject are gratefully acknowledged. The author is grateful to Dr. H. Fukutome for his helpful suggestions and discussions regarding the subject. The author greatly acknowledges Dr. Maehashi for his helpful discussions and valuable comments. Special thanks are due to Dr. H. Yasuda for his theoretical supports on STM measurements. The author is grateful to Dr. H. Arimoto and Dr. T. Aoyama of Fujitsu Laboratories Ltd. for the sample fabrication and their helpful discussions. The author would like to thank all members of Nakashima's group for their experimental assistance and encouragements. Finally, I wish to thank my family and friends for their hearty encouragements.

Publication list

[1] Toshiko Okui , Shigehiko Hasegawa, Hidenobu Fukutome, and Hisao Nakashima
"Shearing orientation dependence of cleavage step structures on GaAs(110)"
Surf. Sci. **448**, 219 (2000).

[2] Toshiko Okui , Shigehiko Hasegawa, Hisao Nakashima, Hidenobu Fukutome, Takayuki Aoyma, and Hiroshi Arimoto
"Characterization of a 0.1 μm MOSFET using cross-sectional scanning tunneling microscopy"
59th Device Research Conference Conference Digest, 59 (2001).

[3] Toshiko Okui, Shigehiko Hasegawa, Hisao Nakashima, Hidenobu Fukutome, and Hiroshi Arimoto
"Visualisation of 0.1 μm Metal-Oxide-Semiconductor Field-Effect Transistors by Cross-Sectional Scanning Tunnelling Microscopy"
to be submitted to Appl. Phys. Lett.

[4] Toshiko Okui, Shigehiko Hasegawa, and Hisao Nakashima
"Characterization of the potential profiles on a planar *pn* junction by cross-sectional scanning tunneling microscopy/scanning tunneling spectroscopy"
to be submitted

[5] Osamu Suekane, Masakazu Tanaka, Toshiko Okui, Katsuhito Arakawa, Shigehiko Hasegawa and Hisao Nakashima
"Annealing effect on InAs dot structures grown on GaAs (001) substrates"
J. Vac. Soc. Jpn. **44**, 394 (2001).

[6] Osamu Suekane, Toshiko Okui , Masahiro Takata, Shigehiko Hasegawa, and Hisao Nakashima
"Growth temperature dependence of InAs islands grown on GaAs(001) substrates"
International Conference on Indium Phosphide and Related Materials Conference Proceedings, 288 (2001).

[7] Osamu Suekane, Shigehiko Hasegawa, Masahiro Takata, Toshiko Okui, and Hisao Nakashima
"SCANNING TUNNELING MICROSCOPY STUDY OF InAs ISLANDS GROWN ON GaAs (001) SUBSTRATES"
Materials Science & Engineering B. **88**, 158 (2002).

[8] Osamu Suekane, Shigehiko Hasegawa, Masahiro Takata, Toshiko Okui, and Hisao Nakashima
"Annealing effect on InAs islands on GaAs(001) substrates studied by Scanning tunneling microscopy"
to be published in Appl. Surf. Sci. (2002).

[9] Osamu Suekane, Shigehiko Hasegawa, Masahiro Takata, Toshiko Okui, and Hisao Nakashima
"Growth temperature dependence of InAs islands grown on GaAs (001) substrates"
to be published in Jpn. J. Appl. Phys. (2002).

International conference list

[1] Toshiko Okui , Shigehiko Hasegawa, Hidenobu Fukutome, and Hisao Nakashima
"Shearing orientation dependence of cleavage step structures on GaAs(110)"
10th International Conference on STM'99 TuP1-9 July 1999, in Seoul, Korea

[2] Hidenobu Fukutome, Shigehiko Hasegawa, Toshiko Okui, Hisao Nakashima,
Takayuki Aoyma, and Hiroshi Arimoto
"Scanning tunneling microscopy study of annealing effects on Si nanoscaled *pn* junctions formed by ion implantation"
International Microprocesses and Nanotechnology Conference 6B-2-5 July, 1999 in Yokohama.

[3] Toshiko Okui , Shigehiko Hasegawa, Hisao Nakashima, Hidenobu Fukutome,
Takayuki Aoyma, and Hiroshi Arimoto
"STM/STS study of the annealing effect on Si nano *pn* junction formed by ion implantation"
2nd COE symposium on atomic scale processing and novel properties in nanoscopic materials
P7 December, 1999 in Osaka.

[4] Toshiko Okui , Shigehiko Hasegawa, Hisao Nakashima, Hidenobu Fukutome,
Takayuki Aoyma, and Hiroshi Arimoto
"STM/STS study of Si nano *pn* junctions under illumination"
The Third SANKEN International Symposium P2-13, March 2000, in Osaka.

[5] Hidenobu Fukutome, Shigehiko Hasegawa, Toshiko Okui, Hisao Nakashima,
Takayuki Aoyma, and Hiroshi Arimoto
"Quantitative evaluation of the carrier concentrations in Si substrates witn the use of scanning tunneling microscopy / spectroscopy "
The Third SANKEN International Symposium P2-14, March 2000, in Osaka.

[6] Toshiko Okui , Shigehiko Hasegawa, Hisao Nakashima, Hidenobu Fukutome,
Takayuki Aoyma, and Hiroshi Arimoto
"STM study of annealing effects on Si nano *pn* junctions fabricated by ion implantation"
2000 MRS Fall Meeting D9.12 November, 2000 in Boston, U.S.A.

[7] Shigehiko Hasegawa, Katsuhito Arakawa, Masakazu Tanaka, Osamu Suekane,
Toshiko Okui , and Hisao Nakashima
"Scanning tunneling microscopy study of InAs islanding and dissolving on GaAs(001) surfaces"
2000 MRS Fall Meeting J8.7 November, 2000 in Boston, U.S.A.

[8] Osamu Suekane, Masakazu Tanaka, Toshiko Okui, Katsuhito Arakawa,
Shigehiko Hasegawa, and Hisao Nakashima
"Annealing effect on InAs quantum dots grown on GaAs(001) substrates"
3rd COE symposium on atomic scale processing and novel properties in nanoscopic materials P8
December 2000, in Osaka.

[9] Osamu Suekane, Toshiko Okui, Masakazu Tanaka, Shigehiko Hasegawa, and Hisao Nakashima
"Growth temperature dependence of InAs islands on GaAs(001) surfaces observed by STM"
4th International symposium on intermaterials P29 February 2001, in Osaka.

[10] Osamu Suekane, Toshiko Okui, Masahiro Takata, Shigehiko Hasegawa, and Hisao Nakashima
"Growth temperature dependence of InAs islands grown on GaAs(001) substrates"
13th International Conference on Indium Phosphide and Related Materials WP-41 May 2001, in Nara.

[11] Osamu Suekane, Toshiko Okui, Masahiro Takata, Shigehiko Hasegawa, and Hisao Nakashima
"Scanning tunneling microscopy study of InAs islands grown on GaAs(001) substrates"
E-MRS 2001 Spring Meeting, I-III.3 June 2001, in Strasbourg, France.

[12] Toshiko Okui, Shigehiko Hasegawa, Hisao Nakashima, Hidenobu Fukutome, Takayuki Aoyma, and Hiroshi Arimoto
"Characterization of a 0.1 μm MOSFET using cross-sectional scanning tunneling microscopy"
Device Research Conference, III.-4 June 2001, in Notre Dame, U.S.A.

[13] Osamu Suekane, Toshiko Okui, Masahiro Takata, Shigehiko Hasegawa, and Hisao Nakashima
"Annealing effect on InAs islands on GaAs(001) substrates studied by Scanning tunneling microscopy"
8th International Conference on the Formation of Semiconductor Interfaces, TuP-16 June 2001, in Sapporo

[14] Toshiko Okui, Hidenobu Fukutome, Shigehiko Hasegawa, Hisao Nakashima, Takayuki Aoyma, and Hiroshi Arimoto
"Visualization of a 0.1 μm MOSFET by cross-sectional scanning tunneling microscopy"
4th International COE Symposium on Atomic Scale Processing and Novel Properties in Nanoscopic Materials, P7 December 2001, in Osaka.

[15] Osamu Suekane, Shigehiko Hasegawa, Msahiro Takata, Toshiko Okui and Hisao Nakashima
"Post-annealing effects on InAs islands studied by scanning tunneling microscopy"
4th International COE Symposium on Atomic Scale Processing and Novel Properties in Nanoscopic Materials, P8 December 2001, in Osaka.