Discrete correlation processor as a building core of a digital optical computing system: architecture and optoelectronic embodiment

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In this paper we present a general-purpose discrete correlation processor (DCP) expected to be the building core block of a digital optical computing system. The DCP-1 is embodied by optoelectronic devices such as a VCSEL and a complementary metal-oxide silicon photodetector. The application targets of the DCP-1 are optical interconnection and various types of digital optical computing. It is expected that digital optical computing techniques coupled with the optoelectronic technology will provide large capability and flexibility in information processing. Introduction of a processing scheme of optical array logic enlarges the applicable field of the DCP-1 as well as its processing capability. With the experimental DCP-1 a bit error rate smaller than 10^{-9} was obtained for $A \cdot \bar{B}$ operation under a 500-kHz clock rate. © 1999 Optical Society of America

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1. Introduction

Digital optical computing is a promising technological field, owing to the excellent features of light for information processing, e.g., large parallelism, high-speed, and large communication capability. Smart-pixel technology,[1] in which integration of semiconductor electronic circuits and optical input–output ports is positively applied, is one of the important technical foundations for digital optical computing. Great progress in smart-pixel research enables us to design various kinds of optoelectronic devices with ultrawide communication bandwidths. To show the smart-pixel applications, various demonstration systems have been presented, for example, sorting systems,[2] optical backplanes,[3] network routers,[4] and so on. Because of the steady increase in integration density and operation frequency of very large scale integration (VLSI) chips, smart-pixel technology seems to be effective for ultra-high-speed optical interconnection systems.

From the viewpoint of optical application, the current optical interconnection demonstrators use optical properties for simple data links only; thus they do not make the best use of the unique features of light. Therefore there is the question of whether such optical data links will retain their advantage over electronic counterparts when wafer-scale integration and the stacked structure of thinned VLSI chips[5] become accessible. To explore the utility of the optical technologies, sophisticated applications should be considered.

Motivated by the above findings, we study an advanced form of optical interconnection based on optoelectronic hybrid technologies. The essential idea of the architecture is effective use of optical computing techniques in the optoelectronic hybrid system. Not only simple data transfer but also parallel operations over the image data are achieved by the architecture. The core part of the architecture is a discrete correlating processor (DCP), which is one of the most fundamental operations in digital optical computing.

To provide an example of the DCP, we constructed an experimental processor, DCP-1, with VCSEL's and complementary metal-oxide silicon photodetectors (CMOS-PD's). To our knowledge, the DCP-1 is the first demonstrator of optical-intensive digital optical computing embodied by optoelectronic devices. As a concrete scheme for logic implementation, optical array logic (OAL) is adopted on the DCP-1. With the help of OAL,[6] the system consisting of the DCP-1 can execute a wide range of applications including

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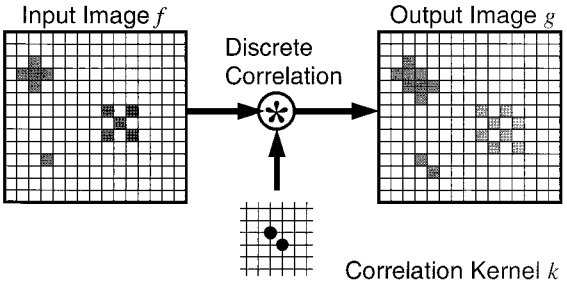

Fig. 1. Fundamental procedure of discrete correlation.

image processing,[7–9] numerical processing,[10] database management,[11] etc.

In this paper, the concept of the DCP is presented and the experimental results obtained by the DCP-1 are described to show the feasibility of the digital optical computing embodied by optoelectronic devices. In Section 2 the architecture of the DCP is explained, and in Section 3 two types of DCP-1 with different configurations are described. In Section 4, experimental results obtained by the experimental DCP-1's are presented and their performance is evaluated.

2. Architecture

The fundamental operation performed by the DCP is discrete correlation. Discrete correlation is defined as follows:

$$g_{i,j} = \sum_m \sum_n k_{m,n} f_{i-m,j-n}, \tag{1}$$

where f and g are the input and the output images and k is a correlation kernel that determines the contents of the operation. Illustrative explanation of discrete correlation is shown in Fig. 1. Discrete correlation is an essential and commonly used operation in various digital optical computing techniques. As presented by many researchers, discrete correlation coupled with a spatial coding technique enables us to achieve flexible operations on two-dimensional images.[12,13] In the spatial coding technique a single image or multiple target images are converted into a spatially coded image f according to a predefined coding rule. A logical or arithmetic operation is configured by the contents of the correlation kernel k and the coding rule.

A noncoded technique for optical computing has been presented.[14] This technique has the potential to achieve optical logic with simple optical components. However, the technique seems difficult to implement practically, owing to a lack of high-speed image display devices and to difficulty in image alignment. On the basis of what we know about current optoelectronic technology, some optoelectronic devices such as VCSEL data should be used for high-speed processing, in which the spatial coding process is not necessarily a troublesome task. In addition, the spatial coding technique can minimize difficulty in alignment, because coded patterns to be overlapped are located neighboring positions. Therefore we adopt the spatial coding scheme in our architecture.

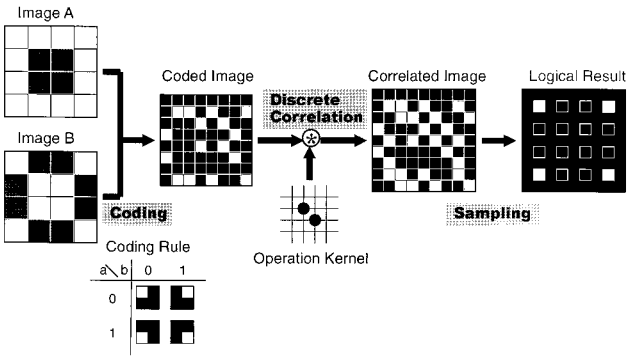

Fig. 2. Procedure of OAL scheme.

As an example of a spatially coded scheme, OAL is explained. Figure 2 shows a schematic diagram of OAL. A pair of binary images are converted into a coded image according to the spatial coding rule. Original images with $N \times N$ pixels are expanded to a coded image with $2N \times 2N$ pixels by the encoding. Then discrete correlation is applied to the coded image with an operation kernel, which is identical to the correlation kernel. The pattern of the operation kernel specifies the logical operation. The correlated image is sampled pixel by pixel, and the signal is inverted to obtain the output image. For arbitrary logical operation, OR operation must be executed for a set of sampled images produced by different operation kernels.

Figure 3 shows a block diagram of the DCP architecture. The system is composed of three blocks: image emitter, optical correlator, and image detector. For the image emitter an array of point sources, e.g., a VCSEL array, is used. The optical correlator performs discrete correlation with various optical setups. As the image detector, a high-speed semiconductor array sensor can be used. Since all the operations in the DCP are executed in parallel, the degree of parallelism directly affects the processing performance. Therefore scalability of the performance in space and time is an important feature of the architecture.

The DCP can be applied to various application fields: simple optical interconnection, parallel processing based on a spatial coding technique, and

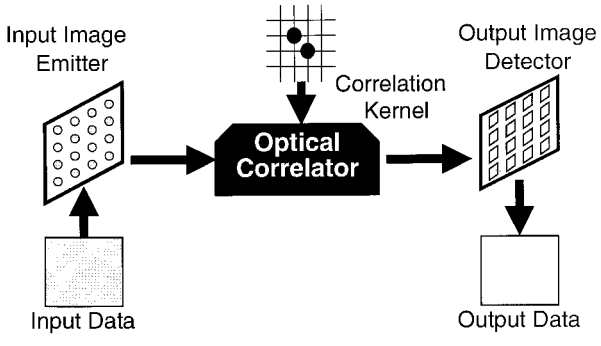

Fig. 3. Architecture of DCP.

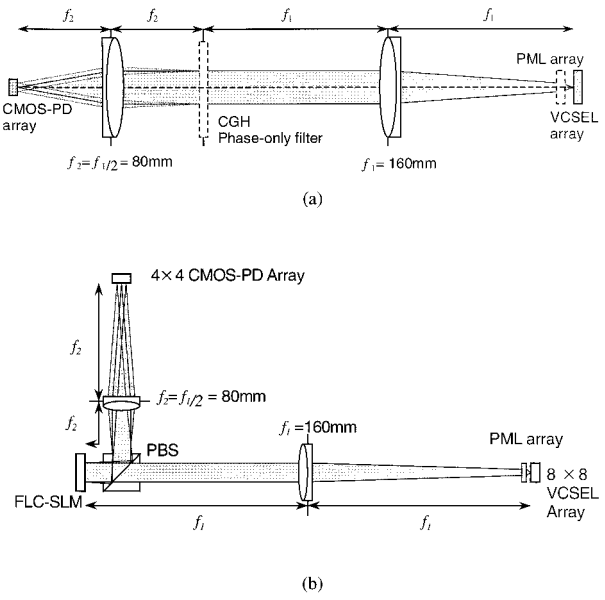

Fig. 4. Optical setups for the DCP-1 of (a) type A and (b) type B.

computing-oriented optical interconnection.[15,16] Centering a core processor based on the DCP, we can construct an optoelectronic hybrid computing system effectively.

3. DCP-1: Optoelectronic Embodiment

As examples of the DCP, two experimental systems were constructed. One is a static kernel system (type A), and the other is a dynamic kernel system (type B). Figure 4 shows their optical setups. As the image emitter, an 8 × 8 VCSEL array (Gigalase, Micro Optical Devices; emitting wavelength, 850 nm; pixel pitch, 250 μm) was used. The VCSEL's were driven by the driver supplied by the United States–Japan Joint Optoelectronics Project (JOP), whose maximum operation speed is estimated by SPICE simulation to be greater than 100 MHz. The swing of the driving current is controlled by bias voltage V_{bias} and modulation voltage V_{ss}. For the optical correlator, a 4-f Fourier transform configuration was adopted with a computer-generated hologram (CGH) filter specifying the correlation kernel. The correlated image was detected by a CMOS-PD array with 4 × 4 pixels (supplied by JOP). The maximum operation speed of the detector is 15 MHz for 100 μW of incident light. The pixel pitch and the photosensitive areas are 250 μm × 250 μm and 110 μm × 110 μm, respectively. The photosignal is amplified and binarized by a series of two comparators in the receiver circuit. The threshold signal level can be controlled by two external voltages, V_{t1} and V_{t2}, which are threshold voltages to the first and the second comparators. Because the pixel pitches of the VCSEL array and the CMOS-PD array are identical, the magnification ratio of the optical system f_2/f_1 must be set as 0.5 to satisfy the sampling condition of the OAL scheme.

The difference between two types of DCP-1 is the method of CGH embodiment. Although the performance of recent spatial light modulators (SLM's) has increased notably, there is no candidate for the CGH filter that can control the wave front of light signals at the high speed rate with high optical efficiency and contrast ratio. As an alternative solution, two kinds of prototype were considered for the different application targets. In general, static filters can be realized by optical passive devices, which provide fast operation speed in exchange for processing flexibility. Dynamic filters are attractive for flexibility and applicability. However, their optical transmission is relatively low, and the setup time for changing the filter patterns is too slow compared with the transmission bit rate of the optical signals. The optical component devices used in both types of DCP-1 are summarized in Table 1. The lenses in the optical systems are common for convenience of changing the configurations.

The CGH filter for the type A system is embodied by a binary phase-only filter etched on a SiO_2 substrate. The filter pattern is exposed by a laser beam writer[17] onto photoresist (Model AZ1500, Hoechst Industry Ltd.) spin-coated on a SiO_2 substrate. After the development the pattern is etched by ionized CF_4 gas. In the type B system the filter pattern is directly displayed on a ferroelectric liquid crystal-(FLC-) SLM (SLM Developer Kit, Displaytech) with binary amplitude modulation. The resolution and

Table 1. Specifications of Optoelectronic Devices Used in the DCP-1

Product	Supplier	Array Size	Pixel Pitch (μm)	Pixel Size (μm)	Operational Speed	Etc.
VCSEL array, Gigalase	Micro Optical Devices	8 × 8	250	ϕ8	—	—
VCSEL driver	JOP	16 I/O[a]	—	—	>100 MHz	—
Ferroelectric spatial light modulator, SLM Developer Kit	Displaytech	256 × 256	15	14	2.5 kHz at 25°C	Reflectivity, <20%; peak operating wavelength, 680 nm
CMOS photodetector	JOP	4 × 4	250	110	15 MHz	—
Planar microlens array[b]	Micro-Opt	0.96 mm × 0.96 mm	250	ϕ250	—	Focal length, 720 μm at 850 nm

[a]I/O, input–output.
[b]Model PML FW0250S0096S-NC.

the pixel pitch of the FLC-SLM are 256×256 and 15 μm, respectively. The contrast ratio of the displayed image is 100:1 (zero order at 633 nm), and the maximum operation speed is 2.5 kHz at 25 °C.

A practical problem of the VCSEL array is its large divergence angle, typically ±15°, which causes optical loss, owing to the small aperture size of the lenses and the SLM. To converge the beam into the aperture of the FLC-SLM, 3.84-mm^2, we use a planar microlens (PML) array (Model PML-FW0250S0096S-NC, Micro-Opt). The pitch of the lenslets is identical to that of the VCSEL array (250 μm), and the focal length is 720 μm at 850 nm.

To design the CGH filters, we used a method based on the Gerchberg–Saxton algorithm.[18,19] The basic procedure of the algorithm is iteration of a sequence of Fourier and inverse-Fourier transformations under constraints to obtain the target intensity profile of the point-spread function. In our design the following parameters were used: the pixel pitch of VCSEL array δ, the number of VCSEL's $N \times N$, the pixel pitch of the filter Δ, the wavelength of the VCSEL's λ, and the focal length of the second lens f_2 shown in Fig. 4. Figure 5 shows the reconstructed image of the CGH filter, which is identical to the pattern of the correlation kernel. When an image is displayed at the VCSEL array, its correlated image is obtained at the position of the −1st diffraction. For full interconnection between all pixels in the input image the size of the correlation kernel is $2N - 1$. The minimum value of f_2 is given by the condition that the 0th diffraction image of the VCSEL array and the correlated image by the −1st diffraction do not overlap. Considering the parameters δ = 250 μm, λ = 850 nm, Δ = 15 μm (SLM), and $N = 8$, we determine that f_2 is 80 mm; so the margin between the two images is 133.3 μm.

4. Experimental Results

To evaluate the performance of the constructed DCP-1's, we observed several characteristics including the optical efficiency of the CGH filter, the maximum frequency of electric and optical signals, and the speed of logical operation.

Figure 6 shows the electric and the optical signals observed in the experimental system. The waveforms of the function generator (Model 33120A, Hewlett Packard), the VCSEL driver, and the optical output detected by the avalanche photodetector module (Model S5331–01; Hamamatu Photonics; bandwidth 100 MHz) are depicted for several operation speeds. For the VCSEL driver, V_{bias} and V_{ss} were set to 4.95 and 6.1 V, respectively. The optical intensity was 22 μW (measured by an optical power meter), and the contrast ratio between the ON and the OFF states of the VCSEL was more than 100:1. As seen from the results, the driver circuit functions at least up to 8 MHz.

Optical efficiency is an important factor for determining the operation frequency of the optoelectronic system. Table 2 shows the measured optical efficiencies to verify the effect of the PML array. With the PML array the divergence angle of the emitting

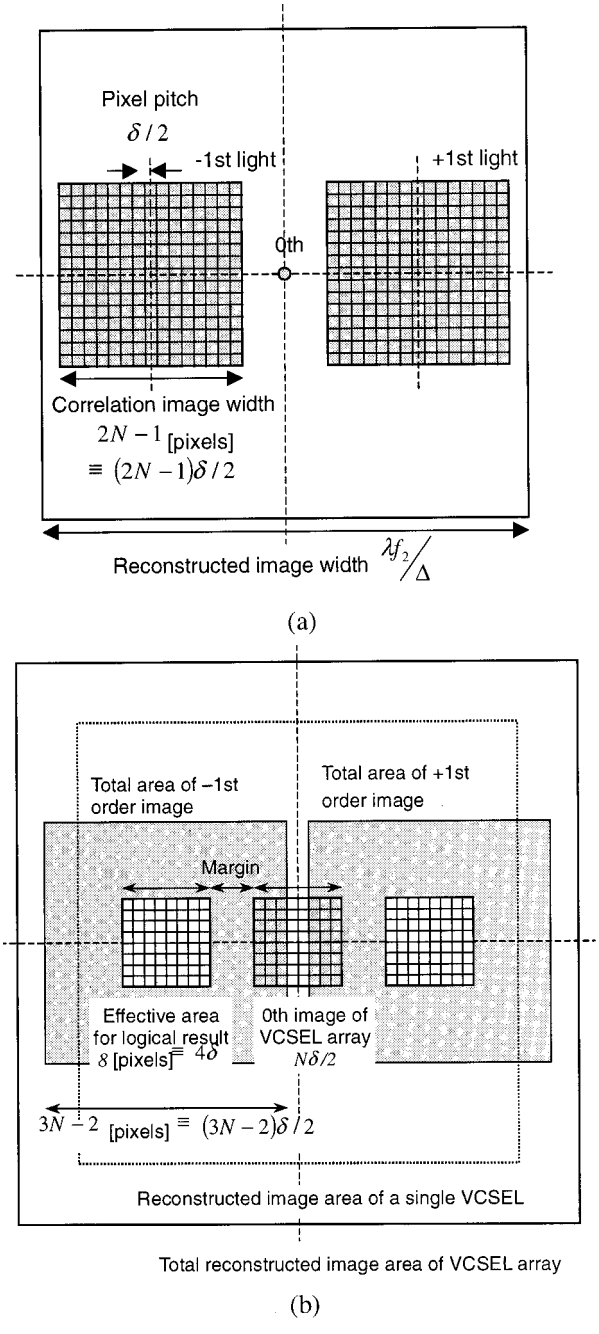

Fig. 5. Reconstructed image plane mapping for (a) a single light source and (b) a VCSEL array.

beam from the VCSEL is reduced to ±0.9° from ±15° so that the optical efficiency is improved to be 13.75% (4.3 times the case without the PML array). The main reason for the remaining optical loss is the mismatch between the divergence angle of the VCSEL and the field angle of the PML.

We reconstructed several CGH filters in the type A and type B systems to observe the diffraction efficiency and the quality of the output images. We designed a CGH filter to execute an operation $\overline{A \oplus B}$, whose fan-out number is 2. The pixel size and the pattern size were the same in both systems, which

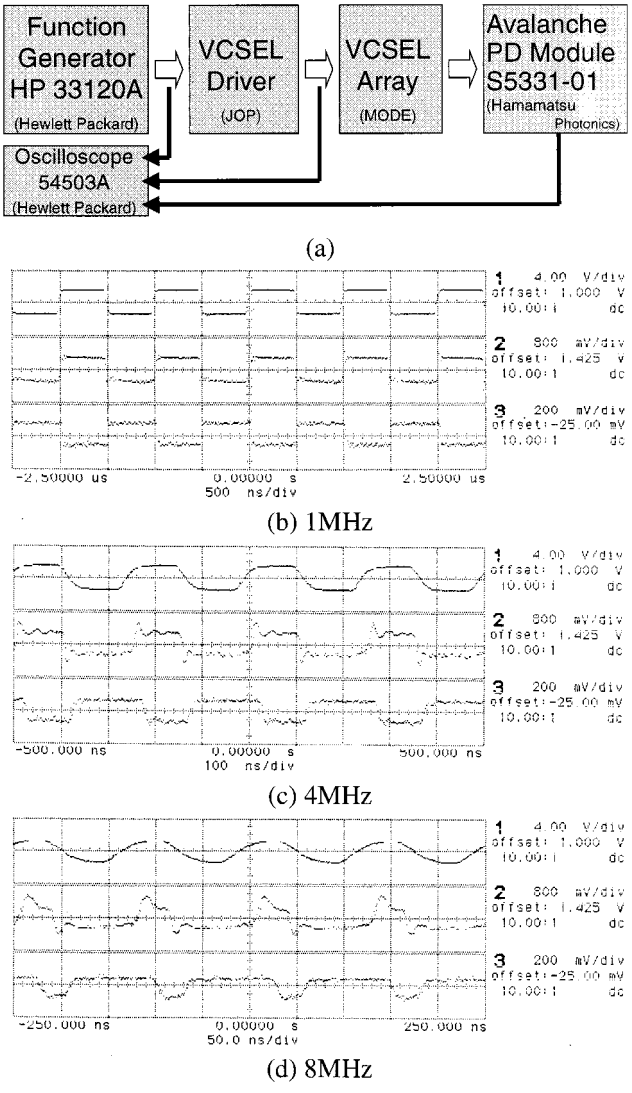

Fig. 6. (a) System block diagram for measurement of signals. (b)–(d) Measured waveforms; CH1 and CH2 are output signals of a function generator (Model 33120A, Hewlett Packard) and a VCSEL driver, respectively; CH3 is amplified photocurrent from an avalanche photodiode module (Model S5331–01, Hamamatu Photonics).

were 15 μm ×15 μm and 256 × 256 pixels, respectively. Observed diffraction efficiencies of the CGH filters were 37.14% (type A) and 5.2% (type B). The reason for low diffraction efficiency of type B is that the SLM is operated by amplitude modulation. Figure 7 shows experimental results of the correlation. The average diameters of the type A and type B reconstructed spots were 60 and 115 μm, which were smaller than the detector area, 120 μm × 120 μm. The differences between the theoretical and the experimental correlation patterns in Fig. 7 were caused by a malfunction of the VCSEL drivers.

On the type A system we measured bit error rate (BER) of operations $A \cdot \bar{B}$ and $\overline{A \oplus B}$ for pseudorandom sequences of input signals. The BER is defined as the ratio of the number of logical errors to the total number of pairs of input bit signals. Since operation $A \cdot \bar{B}$ is achieved by an operation kernel with a single point pattern, we can implement it by a simple imaging system with lateral translation so that no CGH filter is inserted and so that the system shows the maximum performance. In the measurement the 10^9-bit-long pseudorandom sequences were generated by a personal computer (PC), and the optical outputs were stored in the memory of the PC to calculate the BER. On the experimental system no error occurred in the measurement of logical operation $A \cdot \bar{B}$ under 500 kHz, which was restricted by the maximum speed of the PC's input–output. Therefore we concluded the BER was smaller than 10^{-9} under 500 kHz. For the operation $\overline{A \oplus B}$ the BER was 10^{-5} at 25 kHz for the 10^5-bit-long pseudorandom sequence. Degradation of the contrast ratio of the correlation image and the optical efficiency of the system forced us to reduce the operation speed. In the type B system the CMOS-PD could not detect the logical results, because the light intensity was too weak for the CMOS photodetectors (but was sufficient for the CCD camera for observing the correlation images). The reasons for detection failure are assumed to be the mismatch between the designed specification of the peak operating wavelength of the

Table 2. Optical Efficiencies for the Different Setups[a]

System Configuration	Lenses (%)	Filter Transmission (%)	Diffraction Efficiency (%)	Fan-Out	Etc. (%)	Total Efficiency (%)
Type A simple imaging without PML	3.2	—	—	1	—	3.2
		—	—	1	—	13.75
Type A simple imaging with PML	Total: 13.75 PML / BL 13.75 / <100	63.34	31.74	2	—	1.62
Type A with CGH phase-only filter and PML	Total: 13.75 PML / BL 13.75 / <100	—	5.2	2	PBS	0.03
Type B with PML	Total: 13.75 PML / BL 13.75 / <100				and SLM, 8.4	

[a]BL, balk lens; PBS, polarized beam splitter.

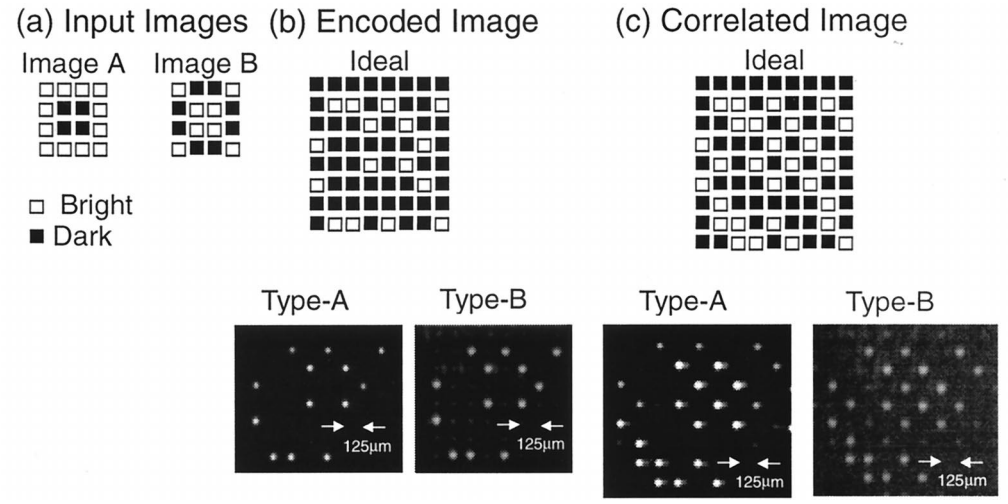

Fig. 7. Encoded and correlated images of types A and B for a pair of input images.

SLM, 680 nm, and the emission wavelength of the VCSEL's, 850 nm, as well as the low diffraction efficiency of the SLM caused by amplitude modulation.

5. Conclusions

In this paper we have presented a discrete correlation processor (DCP) as a building core block of a digital optical computing system. On the basis of state-of-the-art optoelectronic technologies, two types of system (DCP-1) were constructed. We adopted an OAL scheme on the DCP-1 and successfully confirmed the achievement of optical logic operations. For the DCP-1 with a static kernel, the experimental results show that the maximum frequency of the electric circuit is 8 MHz and that the BER is smaller than 10^{-9} for a logical operation at 500 kHz. The maximum speed is restricted by the response time of the photodetector. Because the response time is heavily affected by the incident optical power, improvement of the optical power efficiency is a critical issue for future development.

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