Optical logic array processor using shadowgrams

J. Tanida and Y. Ichioka

Department of Applied Physics, Faculty of Engineering, Osaka University, Suita, Osaka, Japan, 565

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On the basis of a lensless shadow-casting technique, a new, simple method of optically implementing digital logic gates has been developed. These gates are capable of performing a complete set of logical operations on a large array of binary variables in parallel, i.e., the pattern logics. A light-emitting diode (LED) array is used as an incoherent light source in the lensless shadow-casting system. Sixteen possible functions of two binary variables are simply realizable with these gates in parallel by controlling the switching modes of the LED's. Experimental results demonstrate the feasibility of various gate arrays, such as AND, OR, NOR, XOR, and NAND. As an example of application of the proposed method, we construct an optical logic array processor that can implement parallel operations of addition or subtraction for two binary variables without considering the carry mechanism. Use of the light-modulated LED array means that the proposed method can be applied to combinational circuits.

INTRODUCTION

The large-scale electronic computer has developed dramatically with the progress of the development of electronic devices. To solve the problem of high-speed processing of large amounts of data, such as two-dimensional or three-dimensional images, however, the present electronic computer is not necessarily promising because of its fundamental serial nature. At present, to overcome this drawback, a new computing principle is sought, and development of a new computing system on the basis of that principle is needed. It appears that the optical digital computer is one of the promising new generation of computing systems. The capability for parallel, ultrahigh-speed processing in optics is attractive for dealing with large amounts of data. Also, use of optical logic or pattern logic would serve to develop the new philosophical and architectural principles for the computing system.

The electronic digital computer is designed based on Boolean algebra and is constructed by combinations of numerous logic gates as the switching elements and flip-flops as the memory elements. Thus, to construct an optical digital computer based on a new principle, optical logic gates operating in parallel as switches and memory elements recording the optical signal must be developed. Several methods of optically implementing digital logic gates have been investigated.[1–6]

In this paper, we propose a new, simple method of optically implementing logic gates based on the shadow-casting technique. The optical system used is the lensless shadow-casting system, in which a light-emitting diode (LED) array is used as an incoherent light source. The characteristics of the proposed method of implementing optical logic gates are the following:

(1) The processing system used is extremely simple, and thus cost effectiveness is high.

(2) All logic functions are realizable spatially in parallel for two binary variables, i.e., for black-and-white images. Consequently, pattern logic can be easily obtained for two binary images.

(3) The processor has programmability, and hence any combinatorial logical operation can be performed simply.

(4) Parallel operations of all logic functions can be implemented by switching LED's with the proper combination mode. No electronic or mechanical scanning is required.

(5) The gates operate in a single-instruction-stream, multiple-data architecture.

(6) It requires spatial encoding of an input binary image, but decoding is done by means of a simple decoding mask.

By modifying the proposed method, a parallel logic array processor, which can carry out arithmetic operations for gray-level images as well as for binary ones, is formed.

In the following sections, we describe a method that can achieve optical logic gates in parallel. We also show experimental results demonstrating implementation of parallel operations of the 16 logic functions or pattern logic. Then the limitation of the proposed method is discussed by evaluating the effect of diffraction. Finally, the applications of the proposed method to the parallel logic array processor are presented.

OPTICAL LOGIC GATES USING A SHADOWGRAM

The electronic digital computer consists of a number of memory elements and of a combination of logic gates for binary variables. Logic gates are essential elements of the electronic digital computer and operate as the switching elements. As is well known, combinations of the 16 possible functions of two binary variables are the fundamentals of the arithmetic operation of the computer. Although all the 16 logic functions can be constructed by combinations of NOR gates, the use of other logic functions saves interconnection in the system. These logic gates in the electronic digital computer operate at high speed under the control of the time-series signals.

Table 1 shows the 16 possible functions of the two binary variables. The first two rows on the left-hand side represent the combinations of values for the two binary variables A and B. The rows labeled F_0–F_{15} show the 16 possible functions resulting from combining two binary variables. In the table,

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Table 1. Sixteen Possible Functions of Two Binary Variables

Function		Function Name 1 (True Logic)	Function Name 0 (True Logic)
INPUT			
A	0 0 1 1		
B	0 1 0 1		
OUTPUT			
F_0	0 0 0 0	F	T
F_1	0 0 0 1	AND	OR
F_2	0 0 1 0	$A\bar{B}$	$A+\bar{B}$
F_3	0 0 1 1	A	A
F_4	0 1 0 0	$\bar{A}B$	$\bar{A}+B$
F_5	0 1 0 1	B	B
F_6	0 1 1 0	XOR	$\overline{XOR}$
F_7	0 1 1 1	OR	AND
F_8	1 0 0 0	NOR	NAND
F_9	1 0 0 1	$\overline{XOR}$	XOR
F_{10}	1 0 1 0	$\bar{B}$	$\bar{B}$
F_{11}	1 0 1 1	$A+\bar{B}$	$A\bar{B}$
F_{12}	1 1 0 0	$\bar{A}$	$\bar{A}$
F_{13}	1 1 0 1	$\bar{A}+B$	$\bar{A}B$
F_{14}	1 1 1 0	NAND	NOR
F_{15}	1 1 1 1	T	F

the functions named for true logic and false logic are represented in the right-most two columns.

All the 16 functions for the two binary variables can be realized in parallel by means of a lensless shadow-casting system in which the two binary variables are the spatially coded two input binary images (transparencies). The results of the logical operations can be obtained in parallel through the decoding mask. The output can be represented by bright-true-logic, i.e., some with a bright area taken as 1 and a dark area as 0.

Figure 1 is a schematic diagram of the lensless shadow-casting system capable of generating all the 16 functions. The LED's arranged in the source plane are the incoherent light source of the system. Divergent light beams radiating from the LED's illuminate the spatially coded transparency (input data) and project multiple shadowgrams onto the screen, interlacing them with each other. The way of interlacing the multiple shadowgrams depends on the combinations of the spatial positions of the LED's switched to the on state. The projected shadowgrams are decoded through the mask shown in Fig. 1 and photographed or detected by the photodiode array. The input transparency is the superposition of the spatially coded two binary images. The method of coding for two binary images is as follows.

Consider an input binary image consisting of $N \times N$ small square areas. Hereafter each small area is called a cell. The values of all the cells are coded into a pattern composed of black-and-white rectangles, as shown in the top row of Fig. 2(a) (the a_{ij} row). If the value of the cell is black (opaque), it is coded like that on the top left of Fig. 2(a). Otherwise, it is coded like that on the top right of Fig. 2(a). In this manner, the values of all cells in input image A are encoded. Then input image B is also encoded in a similar manner. In this case, the patterns used for encoding are not the same as those in the top row but are those in the bottom row of Fig. 2(a).

The two spatially encoded binary images are superposed so that the coded cells of the corresponding pixels of two images are precisely overlayed. This superposed binary image

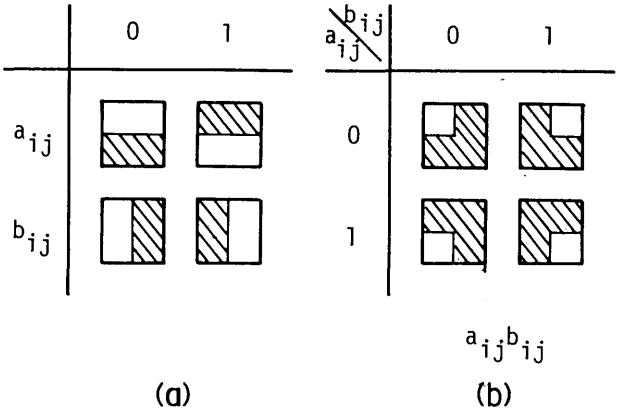


Fig. 2. (a) Coding of the two binary variables and (b) overlay of the two coded patterns.

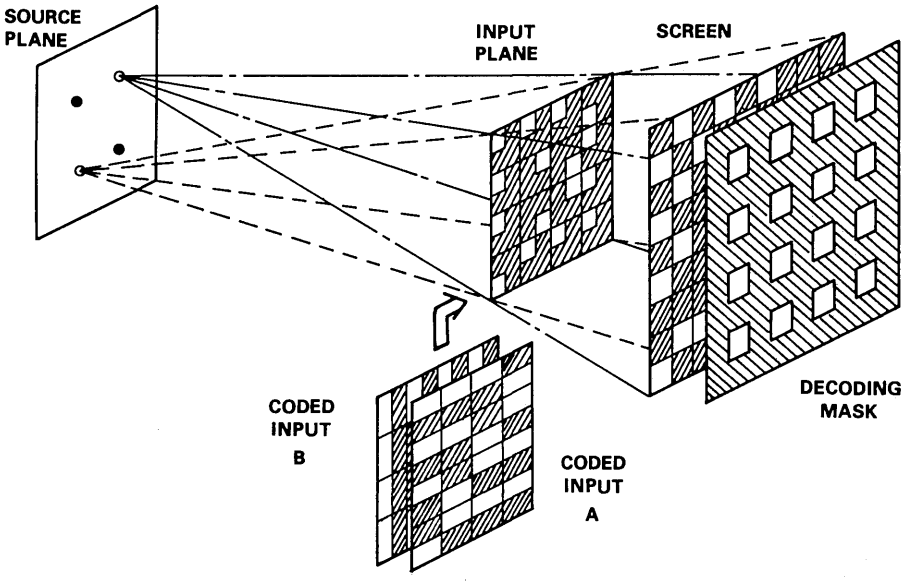


Fig. 1. Schematic diagrams of the lensless shadow-casting system for implementing optical logic gates.

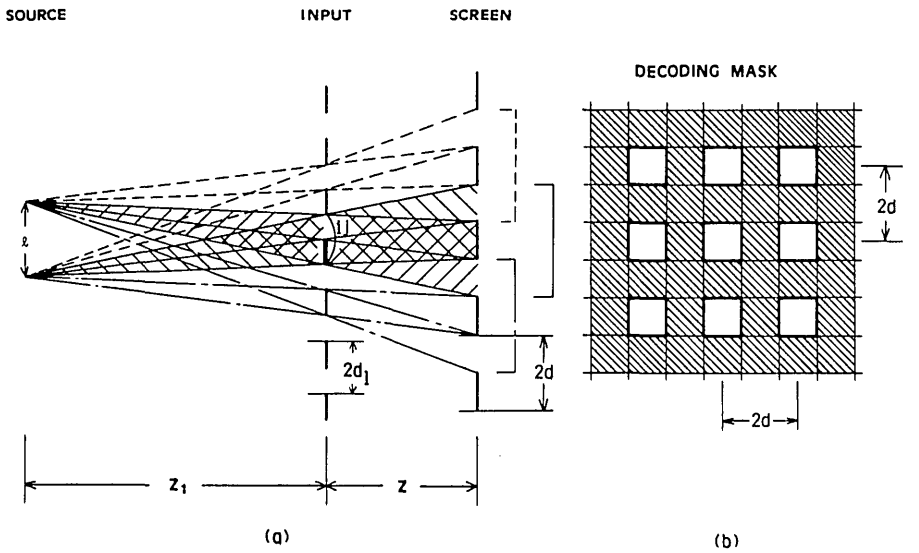


Fig. 3. (a) Geometrical configuration of the shadow-casting system and superposition of shadowgrams and (b) decoding mask.

is set in the input plane of the optical system in Fig. 1. Thus the ij cell in the input is encoded by any one of the four patterns in Fig. 2(b) according to combinations of the values in the ij cell of both images, i.e., $a_{ij}b_{ij} = 11, 10, 01, 00$. In Fig. 2(b), the white area of the ij cell is transparent, and the hatched area is opaque. This coding method of the input image and the manner of overlay of the coded images play an important role in realizing parallel logic operations of two binary variables using the lensless shadow-casting system.

Now we describe the method of implementing the various logical operations in Table 1 in parallel. Figure 3(a) shows the geometrical configuration of the shadow-casting system. In Fig. 3(a), l is the spacing between the LED's in the vertical and horizontal directions, z_1 and z are distances from the source plane to the input plane and from input plane to the screen, respectively, and $2d_1$ and $2d$ are cell sizes in the input and the projected images, respectively. If the conditions

$$d = \frac{ld_1}{l - d_1}, \qquad z + z_1 = \frac{lz_1}{l - d_1}, \qquad d_1 < l \tag{1}$$

are fulfilled in the lensless shadow-casting system, shadowgrams of the ij cell projected by the individual LED's are superposed on the screen, shifting one another by an amount half of the projected cell size along the vertical and horizontal directions. This situation is depicted in Fig. 3(a).

If the four LED's are in the on state, the four projections of the ij cell overlap only in the boxed area in the central part of the projections, as shown in Fig. 4. Note that, under the condition satisfying relations (1), any projection of the neighboring cell $(i, j+1)$, $(i, j-1)$, $(i-1, j)$ or $(i+1, j)$ does not overlap the boxed area defined by the projection of the ij cell. This situation is generalized for every other cell over an entire image. The interval between the neighboring two boxed areas is equal to the projected cell size, $2d$, for vertical and horizontal directions, as shown in Fig. 3(a). The light intensity in the boxed area of the projections of the ij cell is represented by

$$g_{ij} = \alpha(a_{ij}b_{ij}) + \beta(a_{ij}\bar{b}_{ij}) + \gamma(\bar{a}_{ij}b_{ij}) + \delta(\bar{a}_{ij}\bar{b}_{ij}), \tag{2}$$

where α, β, γ, and δ denote the switching state of four LED's arranged in Fig. 4 and + means an OR operation. Any operation on the ij cell of an image is also done on every other cell

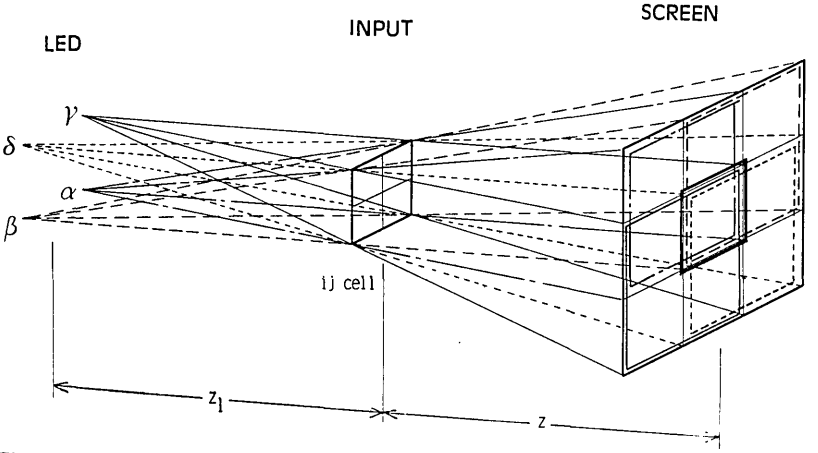


Fig. 4. Overlapping of projections of the ij coded cell illuminated with four LED's and the boxed area in the central part.

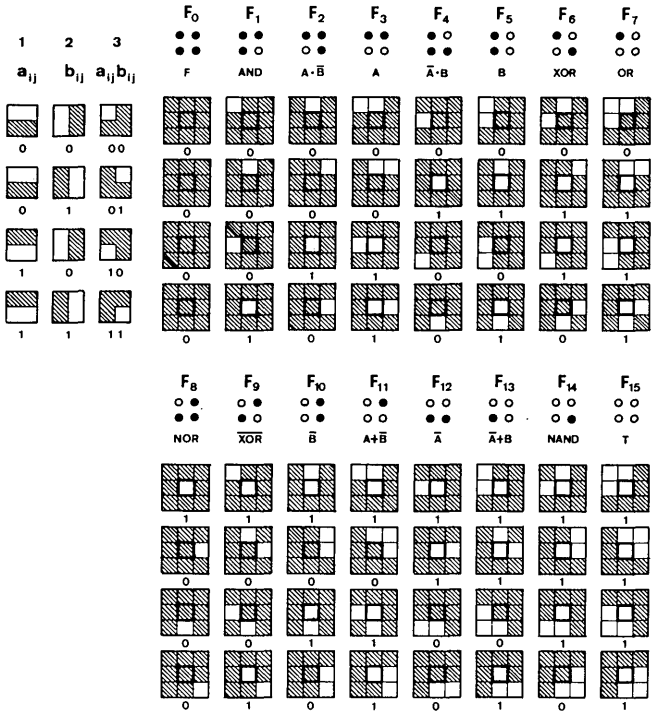


Fig. 5. Spatial representation of the 16 possible logic functions of two binary variables with bright-true-logic. Columns F_0–F_{15} show the projections of the combinatorial variables expressed in column 3 with the LED's with switching states shown at the top. Bright-true-logic is represented by combination of bright (1) and dark (0) in the boxed areas in the central parts of the projections.

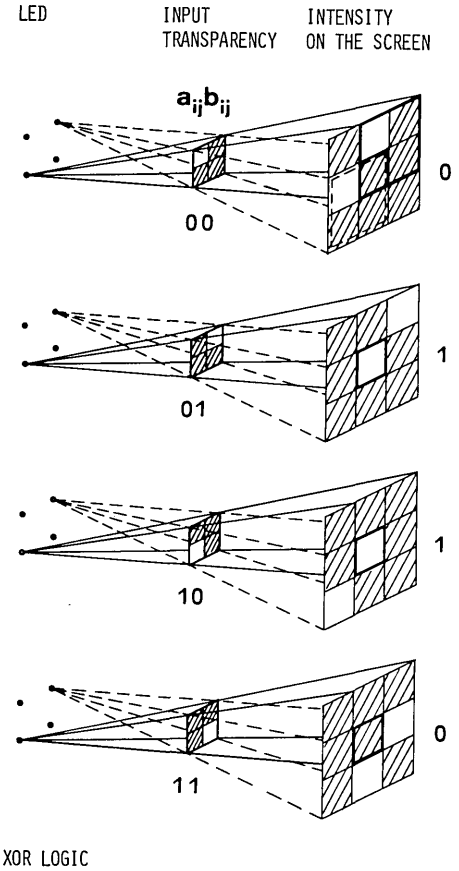


Fig. 6. Realization of XOR gate in the boxed area in the central part.

in parallel. The boxed area becomes bright or dark according to the switching state of the LED's, and all the 16 possible logic functions are realizable in parallel by bright or dark true logic only at the boxed areas over an entire image by controlling the switching states of four LED's.

The results of pattern logic can be observed as the assembly of the boxed areas through the decoding mask shown in Fig. 3(b).

Figure 5 shows spatial representations of the 16 possible functions of two binary variables to be realized by the lensless shadow-casting system for the ij cell. The left-most two columns show the combinations of the coded values of the two binary variables. The third column is an overlay of columns 1 and 2, showing the four states of the input. Columns F_0–F_{15} represent the projections of the ij cell obtained by the switching states of four LED's shown on the top. The operations of the 16 possible functions, such as AND, OR, NOR, XOR, $\overline{\text{XOR}}$, and NAND, whose configurations are shown in Table 1, are realized with bright-true-logic in the boxed area in the central part of the projected images.

We illustrate the operation of the XOR gate, for example, whose configurations are shown in column F_6 of Fig. 5. In this gate, a bright output in the boxed area has to be given only when the value of the ij cell in either of input images A or B is true (1, or transparent). This occurs when a pair of LED's located diagonally is switched to the on state and another diagonal pair of LED's is in the off state. Figure 6 shows a perspective view illustrating the configurations of the output given for the four combinations of $a_{ij}b_{ij}$ = 00, 01, 10, 11. It is apparent from simple geometrical consideration that the boxed area in the central part of the superposition of the projections of the ij cell represents the XOR configuration with bright-true-logic. In this manner, the operation of the XOR gate can be carried out in parallel for all cells in the input images.

Some of pattern logic can be observed from a single projection by shifting the decoding mask by the amount of the half-output cell size, vertically or horizontally. For example, results of AND, NOR, $\overline{A}B$, and $A\overline{B}$ gates can be obtained from the projection given by illumination of a single LED by using the above decoding method. This fact tells us that the projection obtained by illumination of a single LED includes the results of parallel operations of four functions of AND, NOR, $A\overline{B}$, and $\overline{A}B$ at mutually shifted positions. We also obtain the results of parallel operations of functions A and $\overline{A}$ or B and $\overline{B}$ from the projection given by illumination of two LED's lined up horizontally or vertically. It should be noted that the parallel operations of multiple logic functions are executed

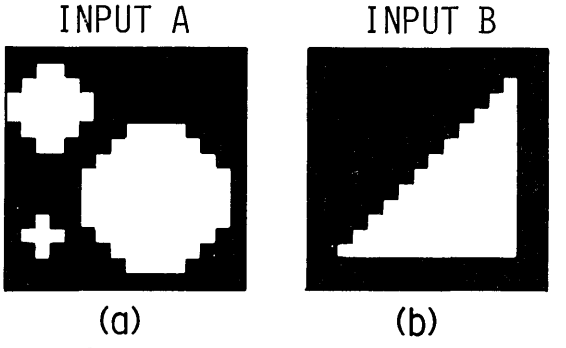


Fig. 7. Two binary images.

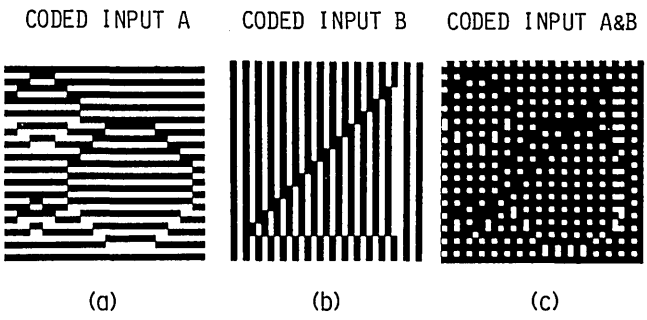


Fig. 8. Two coded images and their overlay.

simultaneously by a simple experiment using the shadow-casting system.

Vertical or horizontal shift of the array of LED's in the source plane results in the shift of the entire projection image on the screen, which is useful for parallel, arithmetic operations of the two binary variables.

EXPERIMENTAL VERIFICATIONS

To confirm the parallel operations of the 16 logic gates by means of the lensless shadow-casting system, the two binary images in Figs. 7(a) and 7(b) are used as the inputs A and B. Both patterns have 16 × 16 pixels. The two images are encoded by the coding method described in the previous section

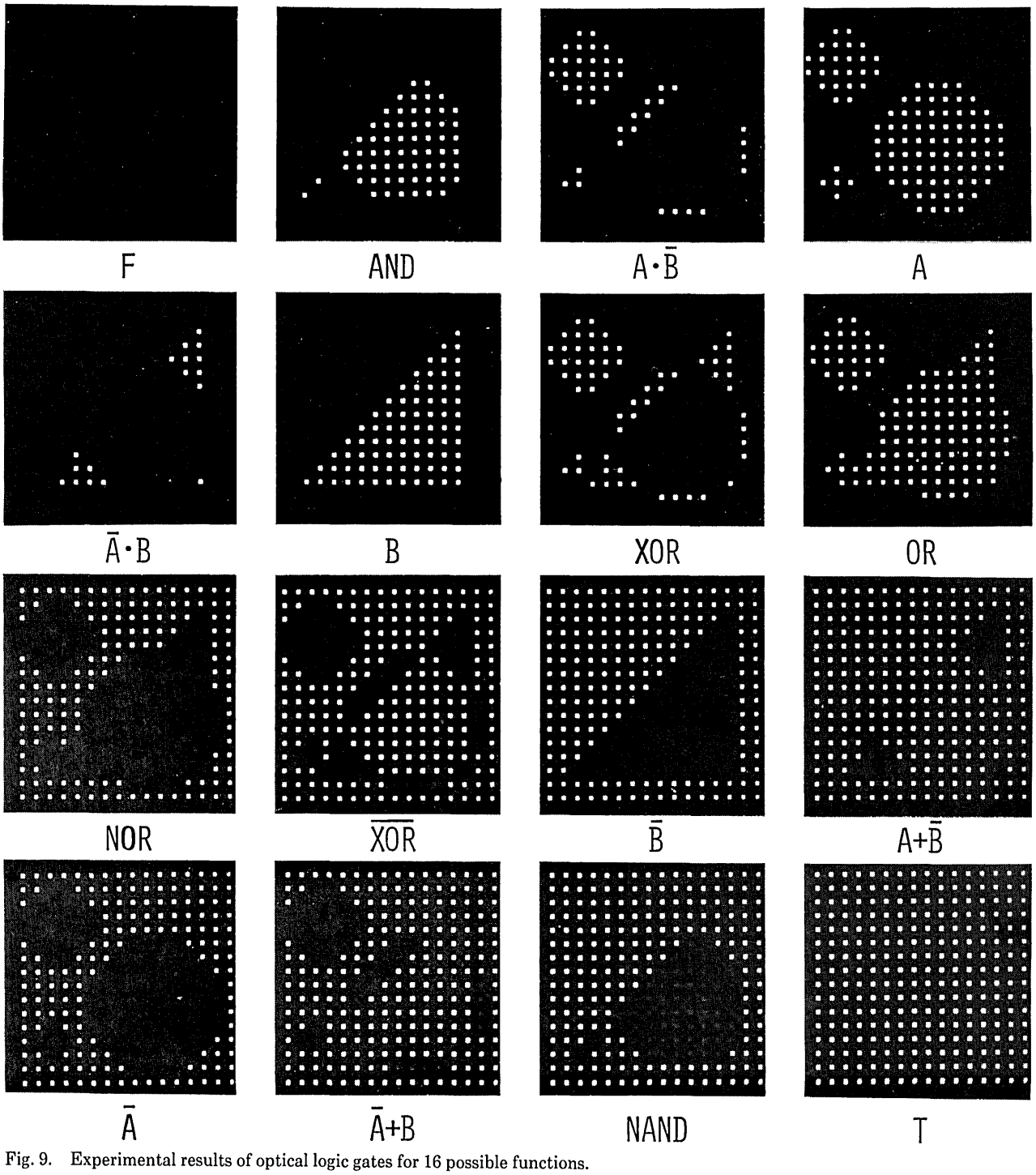


Fig. 9. Experimental results of optical logic gates for 16 possible functions.

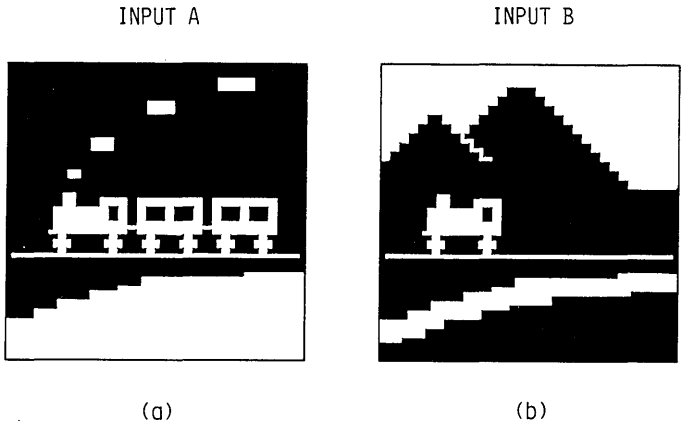


Fig. 10. Two binary images with 64 × 64 pixels.

and are depicted in Figs. 8(a) and 8(b). The two coded images are overlaid in the input plane as shown in Fig. 8(c). In the experiment, the two input images are transparencies with square areas 18 mm on a side. The vertical or horizontal separation of individual LED's on the source plane l is set to be 7.2 mm. Distances from the source plane to the input plane and from the input plane to the screen are adjusted to be 65 and 6 mm, respectively. Various projection patterns obtained by changing the switching modes of the LED's are photographed through the decoding mask.

Figure 9 shows the results of implementation of parallel operations of the 16 possible functions for two binary variables. These results represent 16 kinds of pattern logic. In this experiment, parallel logic operations for 256 channels can be executed.

In order to emphasize the usefulness of the proposed method, we attempt an experiment in pattern logic for two binary objects with high space–bandwidth products. Figure 10 shows the two binary objects with 64 × 64 pixels. Figure 11 shows the results of parallel operations of six gates of AND, NAND, XOR, $\overline{\text{XOR}}$, $\text{A}\overline{\text{B}}$, and NOR. In this case, logical operations for 4096 channels are implemented in parallel by the optical method. In this experiment, the distance between the input plane and the screen has to be 0.5 mm. Therefore these two planes are united with a slide holder. Use of the unit of the input plane and the screen facilitates adjusting the experimental setup.

EFFECT OF DIFFRACTION

The operation of optical logic gates can be achieved by using the lensless shadow-casting system based on the principle of geometrical optics. However, the law of geometrical optics becomes invalid as the spatial detail of the input increases, because of the effect of diffraction. This effect of diffraction must be considered when treating an input image having a high space–bandwidth products by the proposed method.

To examine the effect of diffraction and to determine the region of the geometrical shadow behind the input plane, the Fresnel diffraction pattern of a fine slit of width d is calculated. We consider the case when the slit is illuminated with a divergent spherical wave radiating from a monochromatic point source at $(x_p, 0)$, as shown in Fig. 12.

Let z_1 and z be the distances between the source plane and the input plane and the input plane and the screen, respectively, and let λ be the wavelength of the light. The light distribution on the screen is, by using the parabolic approximation of Huygens–Fresnel–Kirchhoff integral for the one-dimensional case,

$$u(x, z) = \int_{-d/2}^{d/2} \exp\left\{\frac{i\pi}{\lambda}\left[\frac{(x_1 - x_p)^2}{z_1} + \frac{(x_1 - x)^2}{z}\right]\right\} dx_1. \tag{3}$$

Evaluation of Eq. (3) by means of the stationary phase method described in Ref. 7 gives the following relation to determine the region where the law of geometrical optics holds accurately:

$$4\lambda < z \ll \frac{d^2}{\lambda}\left(\frac{z + z_1}{z_1}\right)^3. \tag{4}$$

In a practical optical setup implementing operations of optical logic gates, the distance z must decrease as the spatial detail of the input increases. In such a case, $z_1 \gg z$, so $(z_1 + z)^3/z_1^3 \simeq 1$. Thus relation (4) becomes

$$4\lambda < z \ll \frac{d^2}{\lambda}. \tag{5}$$

Table 2 shows the relation between the spatial detail d in the image and z satisfying condition (5). In Table 2, the resolution points recordable in a square area of 20 mm × 20 mm of the input image under the stated condition are also indicated.

APPLICATIONS

As an application of the optical logic gate proposed here, an optical logic array processor capable of implementing parallel operations of addition or subtraction is formed. Major design improvements to form this parallel logic array processor include (1) development of methods for electro-optical digital-to-analog conversion applying the modulated LED array, (2) use of a number system with redundancy, and (3) development of a method of encoding the input gray-level images.

Parallel Half-Adder

In an electronic digital computer, calculation of addition of two binary variables, A and B, by means of conventional binary arithmetic is performed by binary half-adders composed of OR or XOR gates and AND gates. To execute this calculation, sum-and-carry signals are obtained in the intermediate stage. Table 3 is a truth table for a binary half-adder. Optical implementation of addition according to binary arithmetic is, however, not easy because the parallel carry mechanism becomes extremely complicated.

We find a method of optically implementing addition in which no carry mechanism is required. In the method, use of a carry mechanism can be avoided by allotting three states of numbers for the results of addition of two binary variables and by adopting a modified coding method for the input.

The addition of two binary variables can be designated by three states, 0, 1, and 2, as shown on the right-hand side of Table 3. In optics, these three states of numbers can be realized by the combined operations of two logic operations, such as AND and OR or A and B, sequentially or simultaneously. This situation is illustrated in the right-most two columns in Table 3, where a † is the operation combiner. For

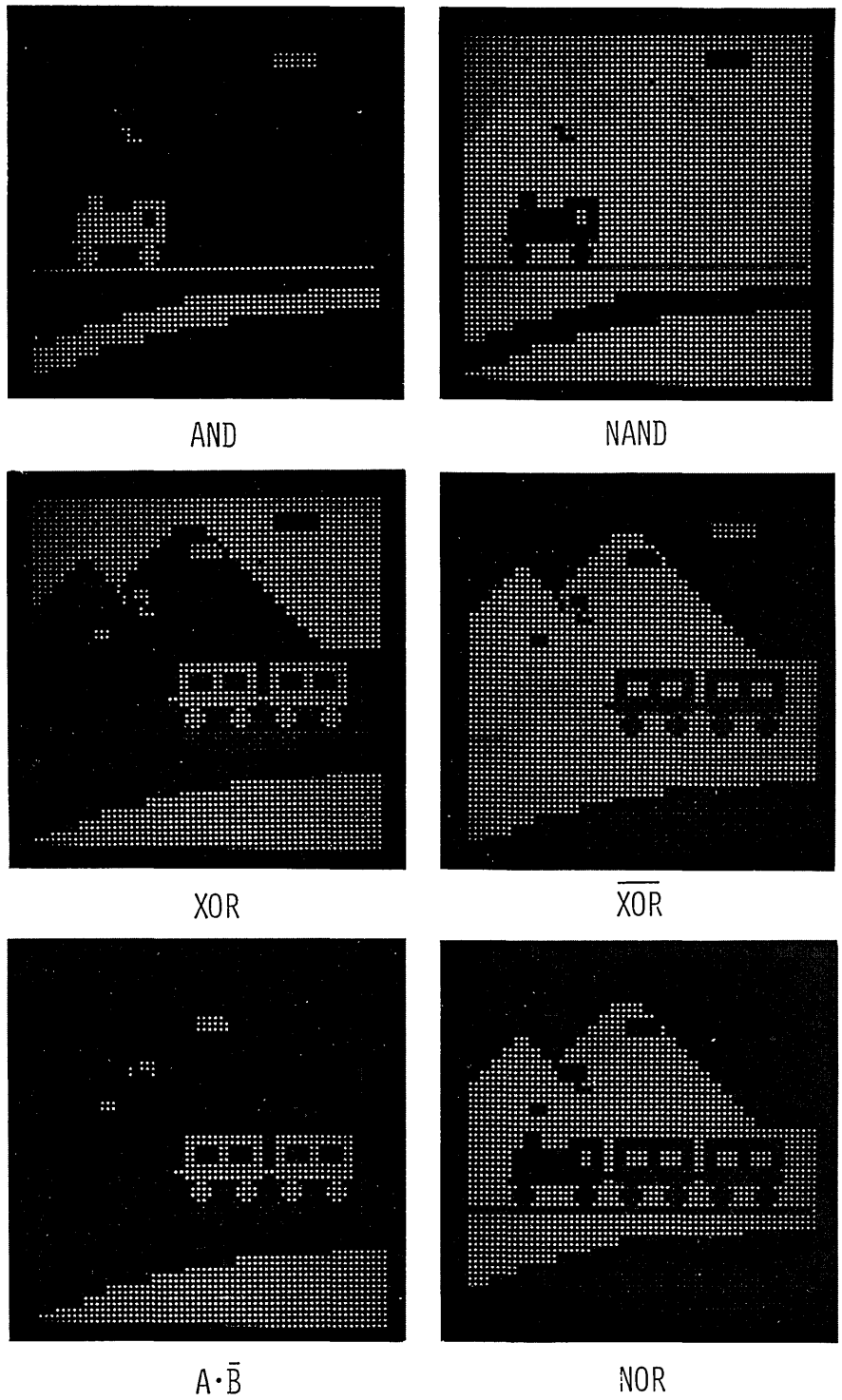


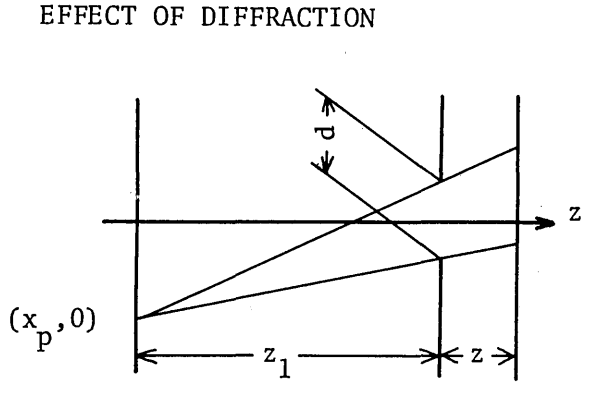
Fig. 11. Experimental results of pattern logic for AND, NAND, XOR, $\overline{\text{XOR}}$, $A\bar{B}$, and NOR gates. Four thousand ninety-six channels of parallel operations are optically implemented.

example, if OR and AND operations are achieved sequentially in the system in Fig. 1 and if the light passing through the decoding mask can be accumulated on the film plane, the integrated light intensity shows the addition of the two binary variables. This leads to the concept that parallel addition of two binary images of a particular digit can be carried out by using LED's with the radiating configuration shown in Fig. 13, in which the number inside the circle means the strength of the radiance of a LED. Referring to Fig. 5, the radiation mode of Fig. 13 is that capable of implementing the combined logic AND † OR or A † B, which is schematically illustrated on the right-hand side of Fig. 13.

Figure 14 represents the experimental result of parallel processing for addition of the two binary variables of a particular digit based on this concept. The LED's with the radiating configuration shown in Fig. 13 are set in the source plane. The shadowgrams of the input of Fig. 8(c) are projected onto the screen and decoded by the decoding mask. Three intensity levels of 0 (black), 1, and 2 are displayed in the processed result.

Parallel Half-Subtractor

Subtraction of two binary variables, A − B, by binary arithmetic can be performed by addition of the binary variable A and the complement of the subtrahend, $\overline{B}$. Table 4 shows results of subtraction by both binary and decimal arithmetic. By using the same consideration as before, the parallel operation of subtraction for two binary variables can be attained optically by using the combined logic $(A + \overline{B}) \dagger (A\overline{B})$ or $A \dagger \overline{B}$. Thus the parallel operation of subtraction can be simply implemented by using the LED array whose radiating configuration is shown in Fig. 15.



$$4\lambda < z << \frac{d^2}{\lambda}\left(\frac{z_1+z}{z_1}\right)^3 \simeq \frac{d^2}{\lambda}$$

Fig. 12. Projection of the slit by a point source.

Operations for a Gray-Level Image

Here we describe a method of encoding the input gray-level image. For illustration, we consider two gray-level images designated by four-bit signals (16 gray levels). The following consideration will be generalized for a gray-level image with n-bit signals.

Table 2. Region of Shadow Z, Allowable for Slit of Width d

d (μm)	d^2/λ (mm)	z (= $d^2/10\lambda$) (mm)	Resolution Points in 20-mm × 20-mm Area
5	0.05	>0.005	2000 × 2000
10	0.2	>0.02	1000 × 1000
25	1.25	>0.125	400 × 400
50	5	>0.5	200 × 200
100	20	>2	100 × 100
250	125	>12.5	40 × 40

[a] d, Slit width; λ, wavelength of light.

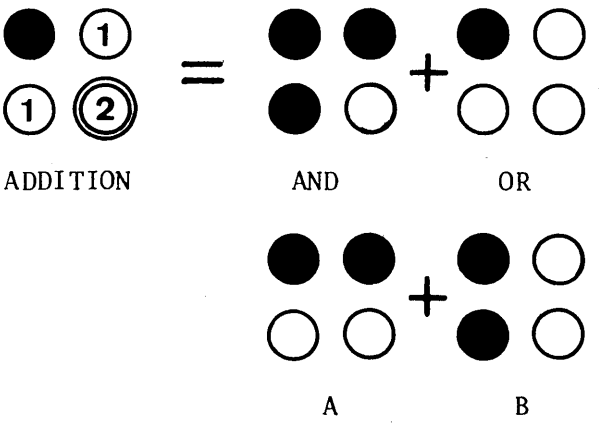


Fig. 13. Radiating configuration of LED's for addition of two binary images.

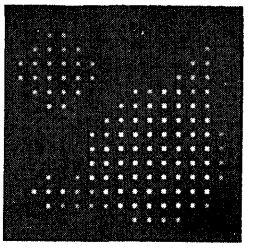


Fig. 14. Experimental result of parallel processing for addition of two binary images.

First, two gray-level images A and B are analog-to-digital converted. Then the digitized four-bit signal of the ij pixel of input A is encoded into the pattern with black-and-white stripes at four neighboring cells, as shown in Fig. 16(a); that of input B is encoded into the pattern of Fig. 16(b). Black-and-white stripes in four cells represent coded signals of the binary ones of the 2^0, 2^1, 2^2, and 2^3 bits, respectively. Coding is made on every other pixel in the image. Two encoded images overlap each other and are used as the input of the processor. Figure 16(c) shows the superposition of Figs. 16(a) and 16(b), which is the ij cell of the input. The extent of the coded image is twice as large as that of the image coded with single digits for the vertical and horizontal directions.

Now we show the optical logic array processor that can do the arithmetic operation of addition for two gray-level images. The salient feature of this processor is its ability to implement operations of combined logic and digital-to-analog conversion simultaneously. Figure 17 is an illustration of the projection of the ij cell of a coded input image in the processor. In the source plane, 16 LED's are arranged, and they are divided into 4 blocks. The distance between the source plane and the input plane is adjusted so that the images projected by the neighboring two LED's are overlaid, shifting with respect to each other by an amount one half of the projected cell size d.

Table 3. Truth Table for Addition of Two Binary Variables Designated by Binary and Decimal Arithmetic

A	B	Binary Addition	Sum	Carry	Decimal Addition	OR † AND	A † B
0	0	0	0	0	0	0 † 0	0 † 0
0	1	1	1	0	1	1 † 0	0 † 1
1	0	1	1	0	1	1 † 0	1 † 0
1	1	10	0	1	2	1 † 1	1 † 1

Table 4. Truth Table for Subtraction of Two Binary Variables Designated by Binary and Decimal Arithmetic

A	B	Binary Substraction Using Complement	Decimal Subtraction	Decimal Subtraction + 1	$(A + \overline{B}) \dagger (A \times \overline{B})$	$A \dagger \overline{B}$
0	0	1	0	1	1 † 0	0 † 1
0	1	0	−1	0	0 † 0	0 † 0
1	0	10	1	2	1 † 1	1 † 1
1	1	1	0	1	1 † 0	1 † 0

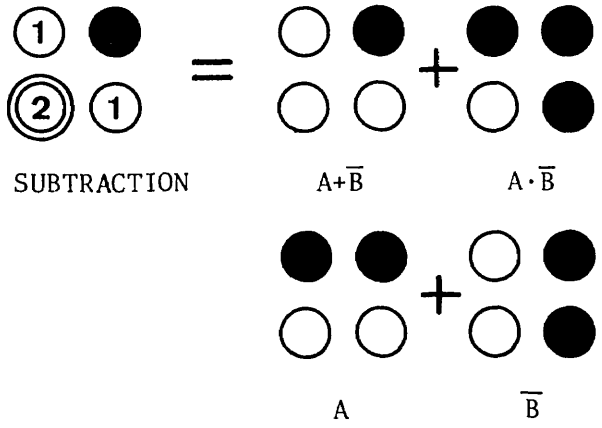


Fig. 15. Same as Fig. 13 but for subtraction.

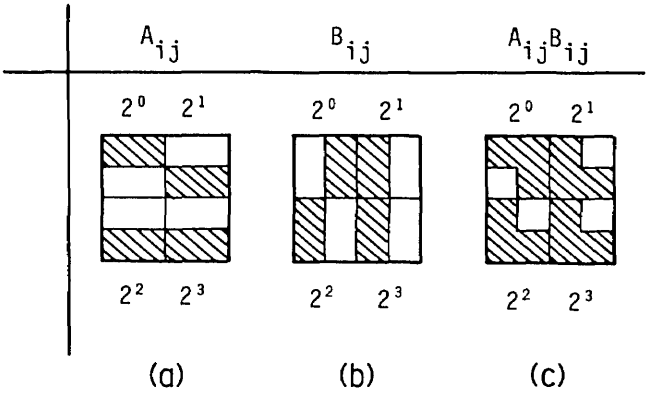


Fig. 16. Coding of the ij cell of a gray-level image designated by four-bit signal. (a) Coding for image A, (b) that for image B, and (c) overlay of the two coded patterns.

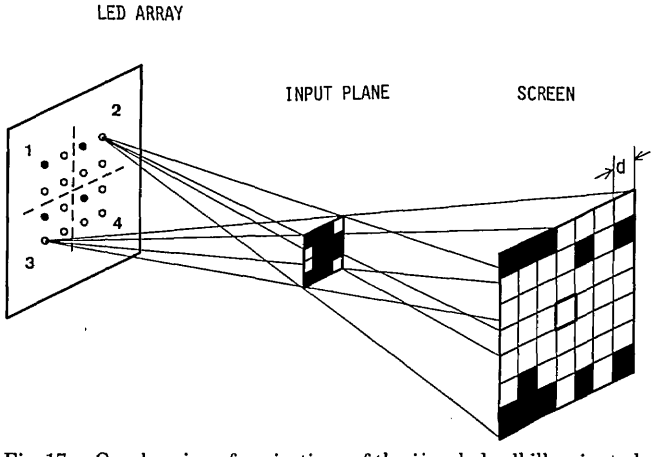


Fig. 17. Overlapping of projections of the ij coded cell illuminated with 4 × 4 LED's.

The geometrical condition for the one-dimensional case is depicted in Fig. 18(a).

LED's in block 1 of Fig. 17 serve to project the relevant shadow of the coded signal of the 2^0 bit in the boxed area, LED's in block 2 that of the 2^1 bit, etc. In this manner, the results of logical operations for four-bit signals are superposed in the boxed area if the LED's in all blocks are switched simultaneously. If the modulated light source of Fig. 19 is in the source plane of the processor, the addition of the two images with 16 gray levels is carried out in parallel by this optical logic array processor. The total light intensity coming to the boxed area of the ij pixel is proportional to $c_0 + 2c_1 + 4c_2 + 8c_3$, where c_0, c_1, c_2, and c_3 represent the bit signals corresponding to 2^0, 2^1, 2^2, and 2^3 bits, respectively, of the binary signal of the ij pixel. This operation is done on every other pixel at the same time.

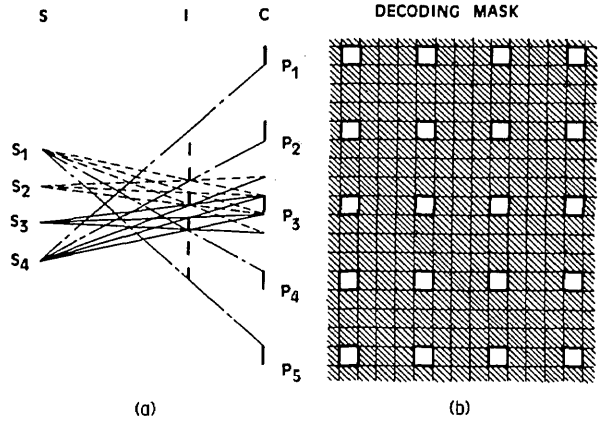


Fig. 18. (a) Geometrical configeration of the optical array processor and superposition of shadowgrams and (b) decoding mask.

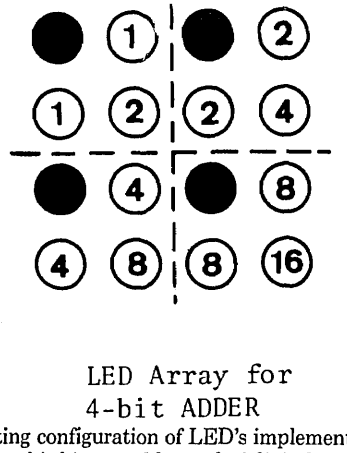


Fig. 19. Radiating configuration of LED's implementable combined operations of four-bit binary adder and of digital-to-analog conversion.

Consequently, this processor can do both operations of combined logic AND † OR (or A † B) and of digital-to-analog conversion in parallel. The result of these operations is observed through the decoding mask shown in Fig. 18(b). Of course, this processor can perform other useful arithmetic operations if the radiation mode of the LED's is changed by programming.

CONCLUDING REMARKS

We have proposed a new, simple method of performing a complete set of logical operations in parallel. The parallel operations of the 16 logic gates can be implemented by switching four LED's in a lensless shadow-casting system with 16 possible combination modes. Since these switching modes can easily be changed by a simple program, various combined logical operations can also be performed simply in parallel. Experimental results have demonstrated the feasibility of the proposed method. The optical system used for experiments is extremely simple and cheap.

Although the limitation of the proposed method depends on the effect of diffraction, evaluation of the diffraction effect has clarified that the method can deal with a fairly large amount of data consisting, for example, of 500 × 500 or 1000 × 1000 pixels. When such data are processed, the distance between the input plane and the screen has to be shortened. This would allow us to use a thin input-screen unit in which the decoding mask is sandwiched between the input plane and the screen.

If a spatial light modulator device, such as a liquid-crystal light valve, can be used for recording the input, and if a highly sensitive photodiode array can be used as the image detecting system on the screen, a compact, parallel logic array unit might be developed. Such a logic unit will probably consist of a LED array, a light valve, and a charge coupled linear imaging array. Building such logic units would serve to develop a kind of parallel optical digital processor based on the new concept.

As an example of applications of the proposed method, a parallel logic array processor implementing the parallel operations of addition or subtraction for gray-level images has been described.

Allowance of the three states of the image intensity extends the applicability of the method. This allowance is not necessarily impractical from the point of view of the dynamic range of the detector. This might be an unconventional method for performing the desired applications by optical computing combined with the concept of logic gates in the digital computer.

Although the spatial coding of the input image seems to be a bottleneck in the proposed method, the method presented here would be one of useful approaches to carry out operations of parallel logic gates.

REFERENCES

1. D. R. Maure, "Optical logic function generator," U.S. Patent 3,680,080 (July 25, 1972).
2. D. H. Schaefer and J. P. Strong III, "Tse computers," Proc. IEEE **65,** 129–138 (1977).
3. R. A. Athale and S. H. Lee, "Development of an optical parallel logic device and a half-adder circuit for digital optical processing," Opt. Eng. **18,** 513–517 (1979).
4. B. H. Soffer, D. Boswell, A. M. Lackner, P. Chavel, A. A. Sawchuk, T. C. Strand, and A. R. Tanguay, Jr., "Optical computing with variable grating mode liquid crystal devices," Proc. Soc. Photo-Opt. Instrum. Eng. **232,** 128–136 (1980).
5. S. H. Lee, "Nonlinear optical processing," in *Optical Information Processing Fundamentals*, S. H. Lee, ed. (Springer-Verlag, Berlin, 1981), pp. 261–303.
6. M. T. Feteri, K. C. Wasmundt, and S. A. Collins, Jr., "Optical logic gates using liquid crystal light valve: implementation and application example," Appl. Opt. **20,** 2250–2256 (1981).
7. A. W. Lohmann, *Optical Information Processing* (Lohmann, Erlangen, Federal Republic of Germany, 1979).