IEICE TRANS. ELECTRON., VOL.E84–C, NO.3 MARCH 2001

PAPER *Special Issue on Optical Interconnects/Optical Signal Processing*

Design and Fabrication of Pipelined Digital Correlator for Opto-Electronic Discrete Correlation Processor

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SUMMARY In this paper, we report on design and fabrication of the pipelined digital correlator (PDC) for the opto-electronic discrete correlation processor (OEDCP). The OEDCP consists of optical fan-in and fan-out interconnection systems and several number of PDC's with optical I/O ports. The OEDCP achieves high processing performance with sophisticated combination of optics and electronics. We design and fabricate a prototype of the PDC which is the processing engine of the OEDCP. For the prototype, the pixel number of the input and the output images is 8×8 and that of the kernel is 3×3. The designed chip is composed of approximately 10,000 transistors. Operation of the fabricated chip was verified using test vectors.

key words: *opto-electronic implementation, discrete digital correlation, smart pixel*

1. Introduction

According to the recent progress in silicon technology, information systems based on electronic computers have been advanced dramatically. Applications of the information system cover various fields such as internet communication, document preparation, games, and science calculation. According to the spread of the application fields, the amount of information is expanding, as seen in image processing and database management. So that the demand for processors capable of handling a large amount of data effectively is rapidly increasing.

Discrete digital correlation (DDC) is a fundamental operation applicable to a wide range of problems. A processor executing DDC is expected to be a key system for a large amount of data. However, this system requires large I/O bandwidth for the input and the output. In addition, dense interconnection appeared in LSI implementation brings serious problems such as signal delay, decrease of noise resistance, and power consumption. It seems difficult to implement DDC by the sole silicon technology.

As a solution for this problem, there is a method utilizing light as information carrier. Light has excellent features for information processing, e.g., spatial parallelism, fast propagation in free space, and large transmission capacity. Smart pixels are proposed and investigated for the devices capable of combining optics and electronics effectively [1]–[5]. Figure 1 shows a typical structure of smart pixels. In the smart pixels, two-dimensional arrays of emitters and detectors are integrated with electronic circuits. This device achieves optical on-chip and off-chip interconnections [1]. Optical interconnection enables us to implement large I/O bandwidth with flexible connecting patterns. A lot of studies have been achieved on evaluations of the LSI's integrated with a VCSEL's (vertical cavity surface-emitting laser) and photo detectors [2], [3] and the optical interconnection systems utilizing smart pixels [4], [5]. In spite of a proposal of optical parallel DDC [6], demonstration with acceptable performance has not been constructed yet. Generally opto-electronic (OE) devices, e.g., emitter, SLM(spatial light modulator) and photo detector, limit system performance.

In this paper, we present an OE implementation of DDC with sophisticated combination of optics and electronics to explore the capabilities of the optical interconnected processing systems. The processore is called opto-electronic discrete correlation processor (OEDCP) which centers a set of core processors called piplined digital correlators (PDC's). With complementary combination of the optoelectronic system and the semiconductor technology, the OEDCP provides higher performance than that implemented by a simple optoelectronic architecture or sole electronics. In Sect. 2, DDC is explained and its applications are shown. In Sect. 3, the characteristics of a simple optoelectronic architecture and a semiconductor integration are compared, and the OEDCP architecture is presented. In Sect. 4, the details of the pipelined digital correlator (PDC) are described, and the fablication result of the PDC chip is presented.

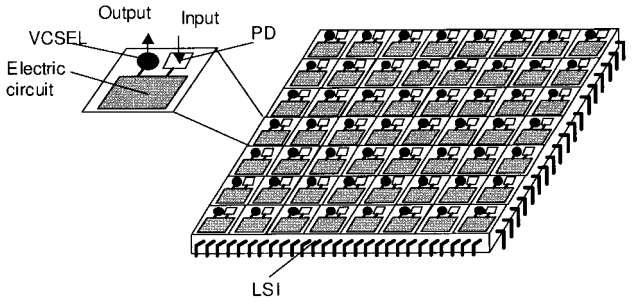

Fig. 1 Structure of smart pixels.

Manuscript received August 21, 2000.
Manuscript revised November 3, 2000.

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2. Discrete Digital Correlation

Discrete digital correlation (DDC) is defined as a cross-correlation between a 2-D discrete image and a correlation kernel. Figure 2 illustrates the process of DDC. DDC is expressed as Eq. (1).

$$c_{i,j} = \sum_{p=-L}^{L} \sum_{q=-L}^{L} k_{p,q} a_{i+p,j+q}, \quad (1)$$

where $a_{i,j}$ and $c_{i,j}$ are the (i, j) pixels of the input A and the output C, and $k_{p,q}$ is the (p, q) element of the correlation kernel K that determines the contents of the operation. $a_{i,j}$, $c_{i,j}$, and $k_{p,q}$ are binary data. L specifies the kernel size. Equation (1) shows that C is equal to the sum of $A's$ duplicated with shifting. The shift amount of each duplication is determined by the elements of K.

DDC can be used for parallel logic operations and image processing. As seen from Eq. (1), DDC is represented as a sum-of-product form, so that it can be directly applied to the above applications. DDC also achieves parallel neighborhood operations with spatial coding of the data. This technique is known as optical array logic (OAL) [7]. Figure 3 shows a processing procedure of the OAL. Two binary images with $n \times n$ pixels are converted into a coded image with $2n \times 2n$ pixels according to the spatial coding rule. Then DDC is executed to the coding image with a correlation kernel. The correlated image is sampled pixel by pixel, then the sampled image provides the operation result. In this scheme the pattern of the correlation kernel specifies the contents of the operation. The kernel pattern in Fig. 3 corresponds to the XOR operation. As examples of the image processing based on the OAL, edge detection [8] and image thinning [9] were presented.

The important feature of DDC is that primitive manipulations for images such as duplication, overlap, and sampling, can be extended to higher level processing like image processing and other operations. An optical system has potential capability to implement DDC for large images in high speed. This comes from the excellent features of light such as spatial parallelism and fast propagation in free space.

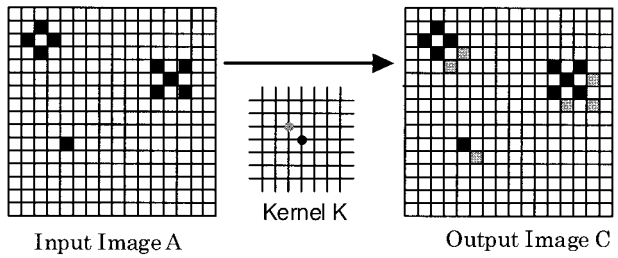


Fig. 2 Process of discrete digital correlation.

3. Opt-Electronic Discrete Correlation Processor

DDC is implemented by arrays of emitters and detectors with simple electronic circuits and a spatial light modulator (SLM) [6]. However, this simple OE architecture does not show distinctive advantages against electronic implementations because of the limitation of current OE devices. As the limitations of the OE devices, power consumption, array size of the integrated emitters and detectors, operational speed, and conversion time between the optical and the electronic signals are pointed out [10].

An advantage of the electronic technology is dense integration of various functions based on semiconductor integration. Typical disadvantages of the electronics are I/O bottleneck, signal delay, and decrease of noise resistance in dense interconnection. Table 1 summarizes the characteristics of the simple OE architecture

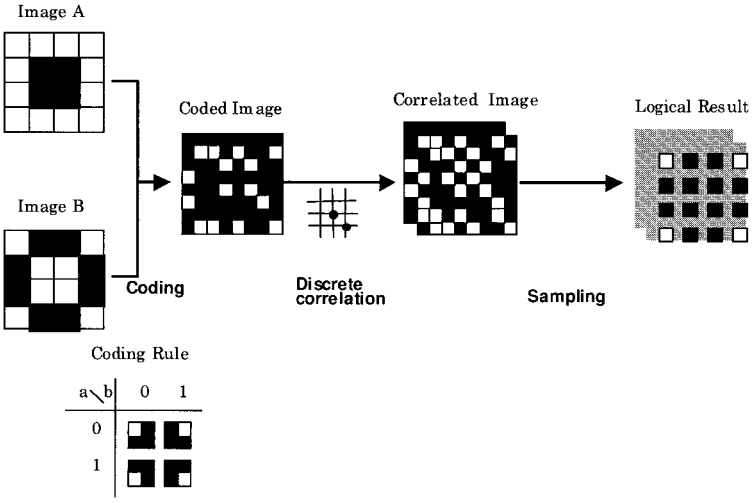


Fig. 3 Processing procedure of optical array logic.

Table 1 Characteristics of simple OE architecture and semiconductor integration.

	Advantage	Disadvantage
Simple OE architecture	Parrarelism High bandwidth	Limitation of OE device
Semiconductor Integration	Large scale integration	I/O bottleneck High density interconnection

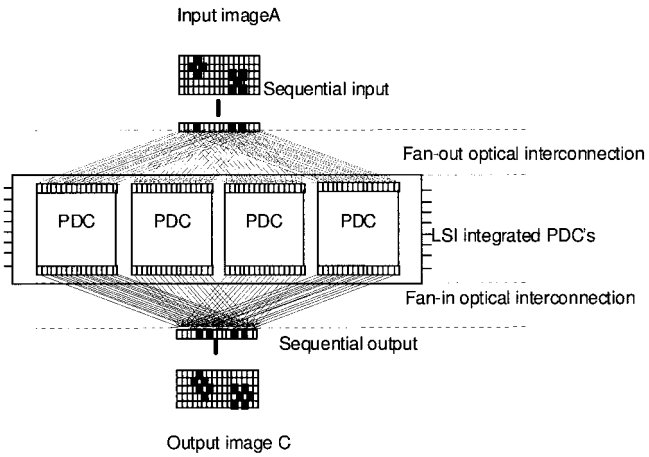


Fig. 4 Schematic diagram of the OEDCP.

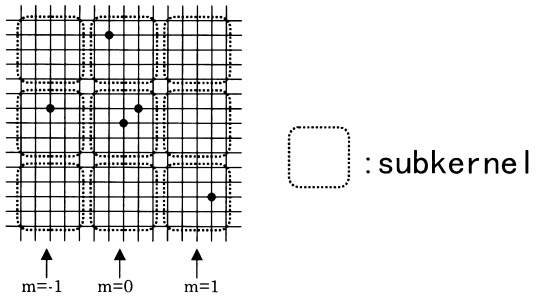
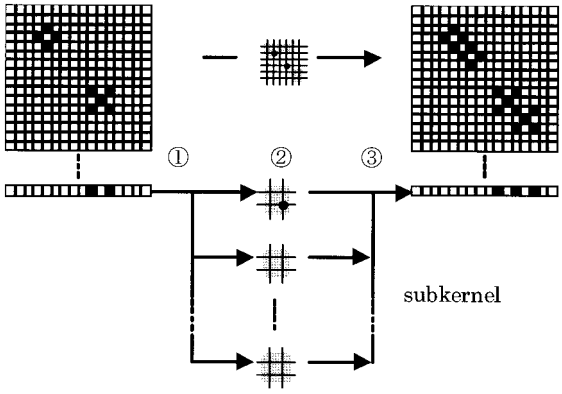


Fig. 5 Division of correlation kernel.



① Fan-out optical interconnection
② pipeline correlator
③ Fan-in optical interconnection

Fig. 6 Processing procedure of the OEDCP.

and the semiconductor integration.

Complementary combination of the OE system and the semiconductor technology is expected to be effective for a high performance processor comparing to the simple OE architecture or the sole electronics. According to this idea, we propose the OEDCP. A notable feature of the OEDCP is sophisticated combination of optics and electronics. In the OEDCP, DDC is divided into subprocesses which are suitable for processing by the semiconductor circuits. By optimizing the division format, we can construct the OEDCP with high processing performance.

Figure 4 shows the schematic diagram of the OEDCP. The OEDCP consists of optical fan-out interconnection, a smart pixel device integrating a set of PDC's with optical I/O ports, and optical fan-in interconnection. The optical fan-out interconnection transmits the row datum of the input image to each PDC. The PDC's execute correlations with different subkernels which is generated by kernel division as shown in Fig. 5. Multiple PDC's are assumed to be integrated on a single smart pixel device. The optical fan-in interconnection collects the output from the PDC's to get a row datum of the output image. Note that the optical fan-in interconnection achieves not only signal transmission but also a logical OR operation for multiple data.

Refering to Figs. 4 and 6, concrete procedure of the OEDCP is explained as follows: First, one row of the input image is selected and displayed on the emitter. The optical fan-out interconnection system transfers the signals to the optical input ports of the PDC's. Each PDC performs correlation between a set of rows and the subkernel. The result of the PDC is displayed on the optical output ports, and the optical fan-in interconnection transfers these signals to the photo detector array. The detected signals provide one row of the output image. The optical fan-out interconnection system duplicates the input image with shifting, and the optical fan-in interconnection system overlaps the correlated results. The OEDCP carries out correlation between the input image and the correlation kernel electronically, and duplication and overlap of images optically.

Although electronic fan-out and fan-in interconnections can be used to construct an equivalent system, such a system encounters problems such as noise, interconnection area, and power consumption. The OEDCP can avoid these problems using optical interconnection. Optical interconnection also achieves high bandwidth I/O communication. Another advantage of the OEDCP is flexibility in system configuration ac-

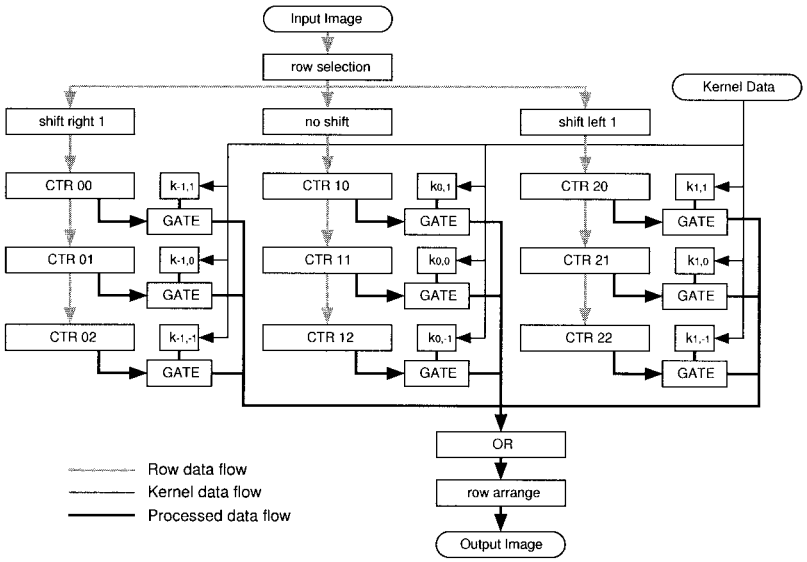


Fig. 7 Block diagram of the PDC.

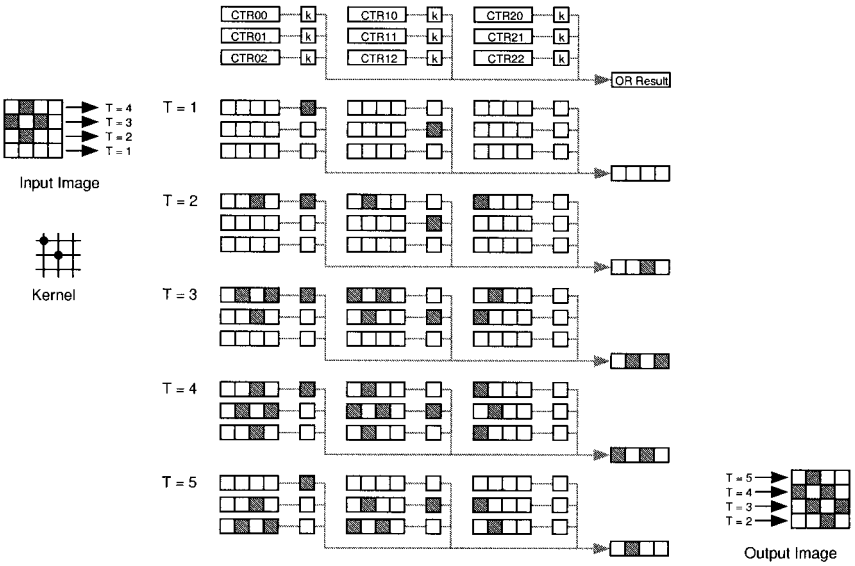


Fig. 8 Time sequence of operation by the PDC.

cording to the performance of the OE devices. For example, effect of the size of the subkernel can be evaluated in terms of processing capability. Such an analysis enables us to optimize the OEDCP architecture.

4. Pipelined Digital Correlator

4.1 PDC Architecture

The PDC is the core processing engine of the OEDCP. Multiple PDC's share the task of DDC as shown in Figs. 4 and 6. The PDC takes a single row and returns the correlated result to the row, and the same processing is repeated row by row. Figure 7 shows the block diagram of the DDC for an example case ($n = 4$ and $L = 1$). For an image with $n \times n$ pixels, the input and the output of the PDC are both n-bit data. The input row datum is duplicated to $2L + 1$ sets of n-bit data for the kernel with $(2L + 1) \times (2L + 1)$ elements. Each datum is laterally shifted bit by bit and stored into the clocked-transfer register (CTR). The contents of the CTR is gated by the contents of the kernel register which stores the element datum of the kernel ($k_{i,j}$). All results of the gated data are logical-summed bit-by-bit for the n-bit data, which is the correlated result for a row of the image. After get the row result, the contents of the CTR's are transfered to the lower CTR's and the same operation is repeated. The final result of the correlation is obtained after several steps of the operation.

Table 2 Operation mode and control pins.

Operation Mode	EK	ED
Correlate Mode	0	1
Renewal (of kernel pattern) Mode	1	0

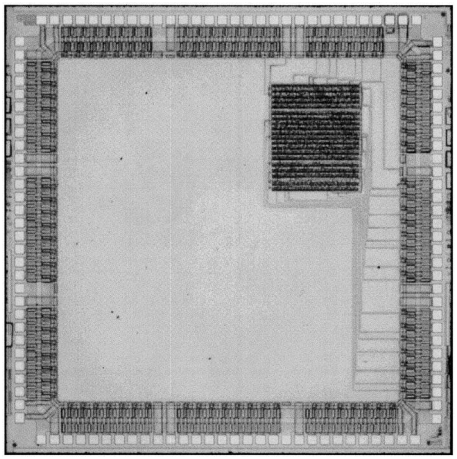


Fig. 9 Photograph of the PDC chip.

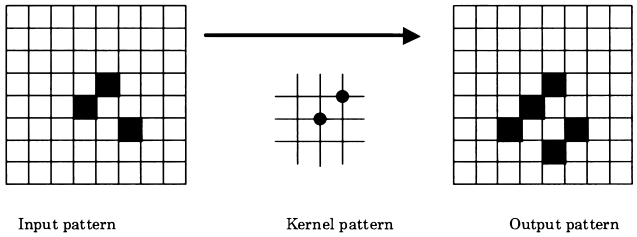


Fig. 10 Test signal for the fabricated chip.

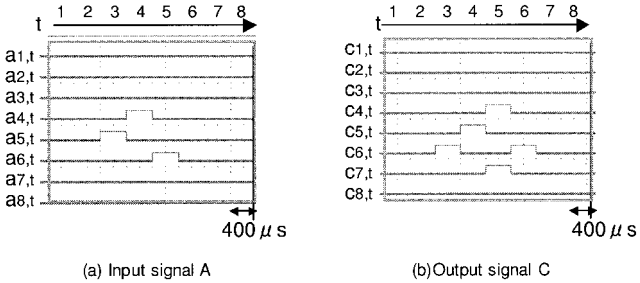


Fig. 11 Measured waveforms: (a) input signals of timing generator, (b) output signals of logic analizer.

Figure 8 shows a time sequence of the operation. The contents of the CTR's, the kernel register and the correleted row are depicted. Assuming that the initial state of the CTR is '0' and that the kernel data are preloaded. Black and white boxes in the figure indicate '1' and '0,' respectively. As shown in the figure, the correct result is obtained after 5 steps. Generally, $n+L$ steps are required for the PDC to complete DDC. The time sequential output can be expressed as follows:

$$o_i(t) = c_{i,n-t+2} \tag{2}$$

where $o_i(t)$ is the ith element of the PDC's output at time t.

4.2 LSI Design of the PDC

According to the PDC architecture in Sect. 4.1, we executed the logical design. The PDC was assumed to be composed of flip-flops, AND gates, and OR gates. For duplication of the input row, we use shift registers composed of the flip-flops. For correlation with each kernel element, shift registers, AND gate and OR gate are prepared. For logical OR, n sets of the OR gates with $2L+1$ inputs and are prepared. The CTR is composed of the shift registers. Two operational modes are selected by the control signals EK (Enter Kernel) and ED (Enter Data). Table 2 shows the signal assignment. For EK=1 kernel pattern is renewal and for ED=1 the PDC execute correration.

4.3 Prototype Chip

The PDC LSI shown in Fig. 8 was designed and fabricated. Figure 9 shows a photograph of the PDC LSI. This process is 0.6 μm CMOS, in which the routing layer are two polycrystalline silicon and three metals and the supply voltage is 5 V. The chip area is 4.5 mm square and the number of external pins are 87 [11].

For the PDC LSI, the pixel number of the input and the output images is 8×8 (n=8), and that of the kernel is 3×3 (L=1). The digital circuits were designed using standard cells. We described the PDC architecture in the register transfer level by verilog-HDL. For the logic synthesis and the layout design, the Design Compiler (SYNOPSYS) and the Cell Ensemble (CADENCE) were used, respectively. Routing between the designed circuits and the I/O pads were achieved manually with the Virtuoso Editor (CADENCE). This is preparation to integrate optical I/O ports to the substrate in future.

The operation of the PDC LSI is verified using test vectors shown in Fig. 10. Figure 11 depicts the measured wave forms; (a) is the input signal and (b) is the output signal. Note that the measured wave form arranged in Fig. 11 directly corresponds to the image data in Fig. 10. The waveform in Fig. 11(b) is equivalent to the output image. Correct operation of the PDC LSI was verified under 25 MHz. 17 steps are required to complete DDC including the preset of the kernel pattern, so that the LSI executes DDC for 8×8 image and 3×3 kernel at 1.5 K frame/sec.

The designed PDC LSI contains 9,820 transistors. With the present silicon technology, several tens million transistors can be integrated on a chip. Therefore, it is possible to integrate several number of PDC's including the optical input and output ports into a chip. Of course, increase of the data size n is another op-

tion. Considering the area for the optical ports and the PDC's, we can optimize system configuration of the OEDCP for high processing performance.

5. Conclusion

In this paper, we presented the OEDCP as an instance of the OE hybrid computing system to explore the capabilities of the optical interconnected processing systems. The OEDCP executed DDC by dividing the task into small sized correlations. Each subcorrelation is executed by the PDC with a pipeline architecture, which was fabricated and the correct operation was verified. For the data broadcast and collection, optical interconnection is effectively utilized. As a result, the OEDCP provides high processing performance based on sophisticated combination of optics and electronics.

As future issues, we should tackle performance evaluation considering the optical I/O band-width and investigation on emitter integration on a silicon substrate. The OEDCP is expected to provide high processing performance using a MCM (Multi Chip Module) packaging.

Acknowledgenment

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

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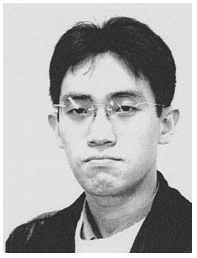

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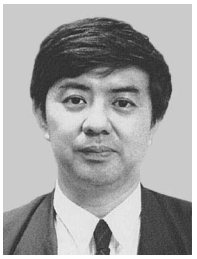

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