Microwave high power field-effect transistors amplifiers with high efficiency and low distortion

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ABSTRACT

In recent years, the large-capacity and high-speed communication technology has accomplished rapid progress focusing on mobile communications. The microwave high-power amplifier is a key component constituting a high-speed communication system, and the performance enhancement of the high-power amplifier is connected directly with the technological advance of the system. In order to perform large-capacity and high-speed communications with a power-saving and a high quality, high efficiency and low distortion characteristics are strongly required for the high power amplifiers. This study-achievement is related to the unique and practical studies of the matching circuit and the power combining circuit which make it possible to maximize the performance of the microwave transistors used in the high power amplifiers. The results have contributed to significant improvements of the communication system.

Chapter 1 describes the history and technology trends of microwave high-power device development as a background of this study. Next, the composition of a microwave high power amplifier and the problems of the device and circuit technique in high power amplifier are described. Then, the purpose and meaning of a main subject are described and the composition of a main subject is shown.

Chapter 2 describes a study on the push-pull power combining circuit and the stability analysis under the large-signal operation for microwave high-power amplifiers.

To realize low-loss power-combining circuits, a novel microstrip balun circuit was proposed and fabricated. Developed balun circuit attained low insertion loss of −0.3 dB at 2.2 GHz and the improvement of design flexibility by adopting a multi-stage configuration different from the conventional balun circuits. By applying this balun circuit, the push-pull amplifier delivered the saturated output-power (P_{sat}) of 140 W with the power-added efficiency (PAE) of 42% at 2.2 GHz using GaAs hetero-structure FET (HFET).

Furthermore, the *S*-probe method which can determine the reflection coefficient in arbitrary point without affecting circuit characteristics was modified so that the loop gain at the large signal operation is obtained. This method reproduced the oscillation phenomenon at the large signal operation in the C-band (5.9 GHz) 60-W power amplifier which combines four chips of AlGaAs/GaAs HFETs in parallel. It clearly showed that the cause of an oscillation is due to the increase of loop gain at the large signal operation. Furthermore, it showed the effect on the design of the balance resistance connected between the chips for the oscillation suppression, and it contributed to the stable operation of the amplifiers.

Chapter 3 describes the study on high efficiency microwave high power amplifiers.

The harmonic termination techniques in the matching circuits were examined to achieve high efficiency characteristics in high power amplifiers. The voltage waveforms were observed using a large signal simulation and Electro Optical Sampling (EOS), and the high efficiency termination condition of load second harmonic was found out to be open condition opposite to conventional Class-F. Moreover, by clarifying the effect of the termination condition of source second harmonic, it was confirmed that the nonlinear gate-to-source capacitance (C_{gs}) affects the overlap of the voltage and the current waveforms. A 2.14-GHz 320-W GaAs FET amplifier with 62% drain-efficiency has been developed by employing the second-harmonic termination technique in both the input and output matching circuits.

Chapter 4 describes the study on low distortion microwave high power amplifiers.

Focusing on transconductance (*gm*)-profile of GaAs hetero-junction (HJFET), it was found that HJFET with shallow threshold voltage (V_{th}) and steep *gm*-profile has small third-order coefficient of *gm* (gm_3) at deep Class-AB, and exhibits low distortion characteristics. Furthermore, the influence of second harmonic and difference frequency impedance on third-order distortion characteristics was investigated using Volterra series analysis. The circuit configuration terminating source- and load-second harmonics with short impedance was newly proposed. An L/S-band 150-W GaAs HJFET employing the second harmonic termination circuits realized low third-order intermodulation distortion (IM3) characteristics less than −40 dB.

In addition, the source- and load-difference frequency termination circuits in package as well as the technique lowering drain bias circuit impedance were proposed. The proposed techniques realized low distortion characteristics without degradation over 100-MHz frequency-spacing (Δf). The result is the widest bandwidth and low distortion characteristics so far, and the deployment to next-generation mobile communications such as a fourth generation (4G) can be expected.

Chapter 5 describes the study on low distortion and high efficiency Doherty amplifiers.

It was clarified that the optimal configuration of Doherty amplifier is present based on the impedance of the device load-pull characteristics. The design approach to perform the distortion compensation in Doherty amplifier was proposed using the distortion cancellation effect of the main and the peak amplifier in power-combining. Proposed distortion-cancelled Doherty amplifier demonstrated high efficiency of 42% and low distortion less than −35dB using 330-W GaAs HJFETs. In addition, the evaluation techniques of each AM-AM and AM-PM characteristics of the main and the peak amplifiers in an operating Doherty amplifier was proposed, and the distortion cancellation of the main and the peak amplifiers in Doherty amplifier linearity was experimentally proved for the first time.

Chapter 6 describes the study on broadband, high efficiency, and low distortion microwave high-power amplifiers using GaN FETs.

High efficiency and high-power GaN FET amplifiers were examined. The device structure was optimized for the efficiency characteristics improvement of the GaN FET on low cost Si substrate, and the Doherty amplifier was developed using the GaN FET. The developed inverted Doherty amplifier delivered the *P*sat of 537 W with the linear gain of 15.5 dB under a pulsed continuous wave signal condition of 2.14 GHz, and demonstrated the digital pre-distortion linearization characteristics with the high efficiency of 48% and the adjacent channel leakage power ratio of −55 dBc at 50 dBm. These results are state-of-the-art performance among the ever reported GaN FET high-power amplifiers.

Furthermore, a broadband and low distortion amplifier module with the GaN FETs capable of high voltage operation was examined to improve output power performance. To realize low distortion characteristics required for modern cable television (CATV) system, low distortion cascode configuration composed of GaAs HJFET for first stage and GaN FET for final stage was investigated. The third-order distortion characteristics were improved by realizing distortion cancellation between GaAs HJFET and GaN FET with optimized *gm*-profile employing Volterra distortion analysis on load-line. The developed CATV power amplifier demonstrated the lowest composite triple beat (CTB) characteristics less than −72 dBc at low drain current condition of 380 mA from 40 MHz to 865 MHz.

Chapter 7 summarizes the conclusions of this dissertation, and describes the challenges and prospects for the future.

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Chapter 1

Introduction

1.1 Research background and issues

In recent years, the large-capacity and high-speed communication technology has accomplished rapid progress focusing on mobile communications. Figure 1.1 shows the annual changes in the traffic volume of information and communications. The volume of information is explosively increasing with the evolution of information and communication systems. In the high-speed communication systems, the microwave high-power amplifier is a key component constituting the digital cellular base station applications, and the performance enhancement of the high-power amplifier is connected directly with the technological advance of the system. So far, in the base station amplifiers, in order to expand the communication area that can be covered by one base station, higher output power has been required. In addition, in the advanced communications system of Wideband Code Division Multiple Access (WCDMA), High Speed Packet Access (HSPA) and Long Term Evolution (LTE), the multi-carrier transmission scheme is adopted for the effective use of radio wave resources. To realize the broadband multi-carrier transmission, higher output power has been required in the amplifier. Furthermore, in order to perform large-capacity and high-speed communications with a power-saving and a high quality, high efficiency and low distortion characteristics are strongly required for the high power amplifiers.

This study is related to the unique and practical developments of the matching circuit and the power combiner circuit which make it possible to maximize the performance of the microwave transistor used in the high power amplifier. This section describes the history and technology trends of microwave high-power device development as a background of this research. Next, the composition of a microwave high power amplifier and the issues of the device and circuit technique in high power amplifier are described.

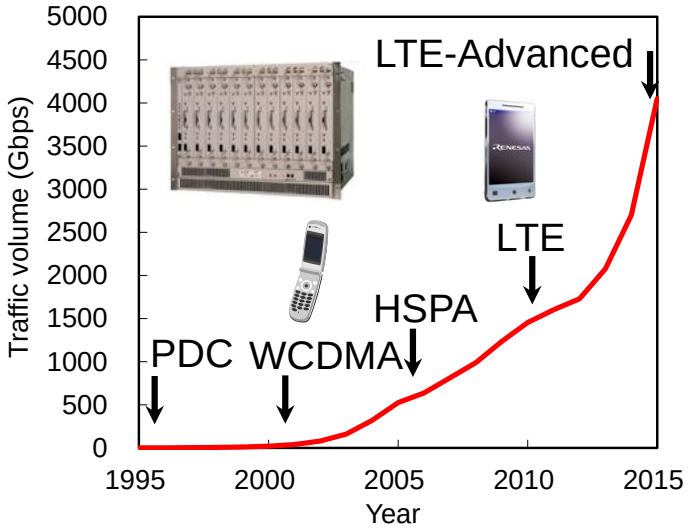


Fig. 1.1 Annual changes in traffic volume of information and communications.

1.1.1 History and technology trends of microwave high power device development

Currently, not only is the microwave constructing the microwave communication network as the social infrastructure around the mobile phone, but also is used to the indeed wide application fields, such as terrestrial TV broadcasting, satellite broadcasting, radar, microwave plasma generator, accelerator, microwave heater, microwave medical treatment, microwave spectroscopy, microwave sensor, millimeter wave sensor, microwave power transmission and energy harvesting, and so on.

It depends on the progress of the microwave semiconductor transistor including GaAs field-effect transistor (FET), that microwaves have become widespread among the familiar apparatus, such as a mobile phone and satellite broadcasting. The traveling-wave tube (TWT) invented by Rudolf Kompfner in 1947 had been a key device of wireless communications for many years because the high output power can be obtained with broadband and high efficiency [1.1]. However, for the downsizing, high reliability, and cost-reduction of the equipment, the replacement with the semiconductor device has become an important technical issue. High-power FET developments started from the invention of multi-channel FET by S. Teszner in 1955 [1.2]. The research of Si metal oxide semiconductor (MOS) FET began in around 1969, and 10-W class output power was realized [1.3]. High-power GaAs metal semiconductor (MES) FET operating in the X-band where the Si transistor was difficult to operate appeared in 1972, and was to be used for various kinds of wireless equipment, such as the transponder for satellite communication and the amplifier for fixed

wireless access (FWA) [1.4], [1.5]. However, in the millimeter wave system and the wireless system needed for high output power more than 1 kW, the transistor is fiercely pursuing the TWT but is still slightly inferior at the point of the high-power and high-efficiency characteristics even today [1.6].

Since high electron mobility transistor (HEMT) using the high mobility two-dimensional electron gas of AlGaAs/GaAs hetero-junction was invented by T. Mimura in 1980 [1.7], high performance microwave transistor development has rapidly progressed. Since HEMT was excellent in low noise characteristics, it was widely used for the satellite broadcasting receiver at first. In addition, the practical use of AlGaAs/InGaAs pseudomorphic HEMT using an InGaAs strained layer with high electron mobility to the channel layer has advanced [1.8]. Against the power amplifier used for the second-generation mobile phone terminals with personal digital cellular (PDC) started in 1993 and code division multiple access (CDMA) operated from 1998, the development of the transistors with high-current and low resistance became active for low voltage operation suitable for long battery life. Double-doped double-hetero AlGaAs/InGaAs/AlGaAs pHEMTs with twice current density were developed [1.9], [1.10]. In addition, the research and the development of hetero bipolar transistors (HBT) have progressed to apply the positive supply, and AlGaAs/GaAs HBT has evolved to InGaP/GaAs HBT [1.11], [1.12].

On the other hand, for mobile phone base stations, the development competition of high-power transistors more than 100 W at 2-GHz-band has begun targeting the third-generation mobile phone services start of wideband code division multiple access (W-CDMA) from 2001. The output-power more than 100 W has difficulty in achievement by improving only the transistor performance. The effort of both the devices and the circuits is required for high output power performance.

In the device, AlGaAs/GaAs hetero structure FET (HFET) of 12-V-operation [1.13], [1.14] and Si lateral diffused MOS (LDMOS) FET of 28-V-operation [1.15] were successfully developed. The optimization of epitaxial structure and electrode structure was performed for high voltage operation. Double-doped double-hetero pHEMT of 12-V-operation was also realized [1.16]. In the circuit, the push-pull amplifier was developed by combining the output power of a pair of single-ended amplifiers using the balun circuit with impedance transformation effect [1.13], [1.17]. A push-pull amplifier has larger impedance transmission ratio than a single-ended amplifier by four times.

The W-CDMA modulating signal (3GPP test model 64 ch down-link) used in the base station has large peak-to-average ratio (PAR) of 8 dB. It is necessary that the amplifier

operates taking the back-off of the PAR from the saturated output power to amplify the signal without deterioration of the signal quality. However, efficiency characteristics decrease in the back-off operation. Therefore, from system side, higher efficiency and lower distortion characteristics as well as high output power were strongly required for the amplifier. In order to meet the demand, the device aimed at high voltage operation, and to apply high efficiency and low distortion circuits was attempted.

In 1998, K. Asano et al. realized GaAs HFET of 35-V-operation for the first time applying the field-plate (FP) electrode that has already been employed in the Si LDMOS FET to the gate-electrode, and achieved high power density of 1.7 W/mm [1.18]. Aiming at the higher voltage operation and the improvement of gain characteristics, dual field plate (gate and source) structure was applied to the AlGaAs/InGaAs pHEMT, and the push-pull amplifier attained the 28-V-operation and the high output power of 300 W in 2005 [1.19]. The saturation efficiency characteristic was improved by applying harmonic terminations in the internal matching circuits.

Attention was focused on the realization in the microwave band of the Doherty amplifier using a Class-AB amplifier and a Class-C amplifier which W.H. Doherty invented with a vacuum tube amplifier as a circuit technique to improve efficiency characteristics at the back-off operation in 1936 [1.20]. The concrete circuit configuration of the microwave Doherty amplifier which combines the Class-AB amplifier and the Class-C amplifier through a quarter-wave transmission line of fundamental frequency was shown by R.J. McMorrow et al. in 1994 [1.21]. Thereafter, the number of the reports of the Doherty amplifier increased at a stretch. As another method to improve the efficiency characteristics at the back-off operation, an envelope-tracking (ET) amplifier of drain voltage modulation method was proposed by P. M. Asbeck et al. in 1998 [1.22].

In base station amplifiers, the research and development of the distortion compensation circuits have made progress to improve the distortion characteristics. Feed-forward (F.F) distortion compensation technology was developed in the second-generation mobile phone base station system [1.23]. In the W-CDMA system of the third-generation, digital pre-distortion (DPD) technology integrated with the baseband signal processing circuits was put to practical use in 2004 [1.24]. Here, the study of so-called "memory effect" to disturb the distortion compensation has become active [1.25], [1.26].

For long term evolution of the fourth generation commercially started in 2010, the broadband performance was also demanded for the high-power amplifiers to cope with the rapid expansion of communication data volume shown in Fig. 1.1. For that, the research and

development of the high voltage, broadband, low distortion, high efficiency and high power amplifiers have become active by applying the heterostructure FET using wide bandgap semiconductor GaN whose development started in 1990s [1.27]. The performance that was not realized by the conventional device has been demonstrated by the combination of DPD, Doherty, ET, and GaN FET [1.28], [1.29].

Since low-power consumption of the base stations can be realized by these technologies, it is thought that a cooling device can be simplified, and the downsizing and weight-saving of a base station proceed further. As shown in Fig. 1.2, the peak-output power and the back-off efficiency of the 2-GHz-band high-power amplifiers have been greatly extended by the progress of the device and circuit techniques. In recent years, the pursuit of the back-off efficiency rather than the peak output power becomes the target. That is to say, in the microwave high power amplifiers, both the high efficiency and low distortion have become important issues. The estimates of KDDI say that the CO_2 of 555-ton a year can be reduced deploying high efficiency base stations [1.30]. These high-performance technologies of high-power amplifier are expected to contribute to the green of information and communication technology (ICT).

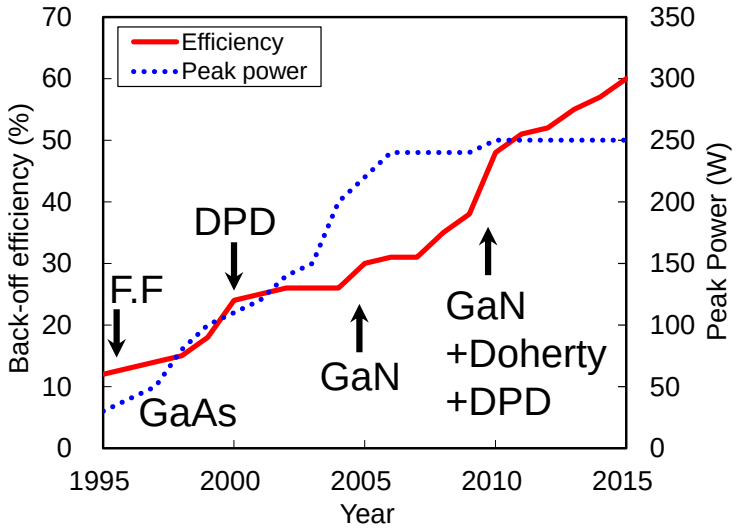


Fig. 1.2 Annual changes in peak-output power and back-off efficiency of 2-GHz-band high-power amplifiers

1.1.2 Configuration of microwave high power amplifiers and issues of device and circuit techniques

The basic configuration of microwave high-power amplifiers is shown in Fig. 1.3. The microwave high-power amplifier is composed of the microwave transistors, the input and

output matching circuits to match the input and output impedance of the transistors to the system impedance of 50 Ω, the gate and drain bias circuits to supply a DC bias for the transistors, and the power-combining circuits to divide and combine the RF signals. In the microwave high-power amplifiers, since the multiple transistors are combined in parallel to achieve higher output-power, the input- and output-impedances of the high-power FETs are greatly reduced. Therefore, the matching circuit and the power-combining circuit are required for efficiently combining the microwaves.

This microwave high-power amplifier is a key component constructing a transmitter system. In order to perform large-capacity and high-speed communications with a power-saving and a high quality, high efficiency and low distortion characteristics are strongly required for the high-power amplifiers. It goes without saying that the performance enhancement of the microwave transistor itself is necessary for the technological advance of the high-power amplifiers, but the development of circuit technology to maximize the performance of the microwave transistors is also required. The technical background and issues of the devices and circuits constituting the high-power amplifiers are outlined as follows.

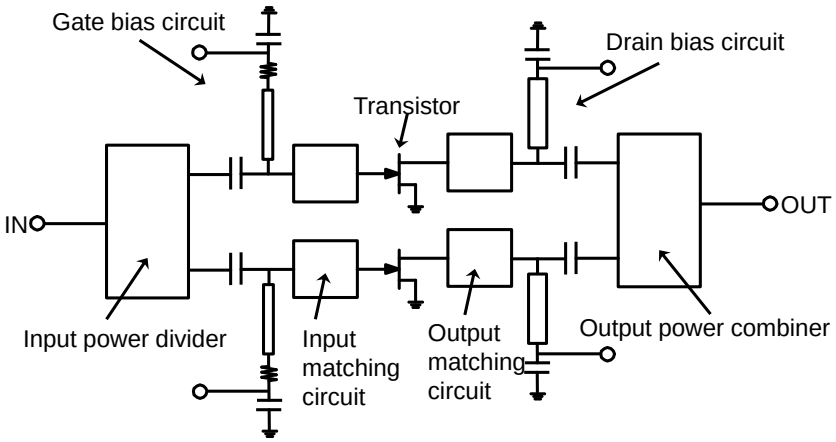
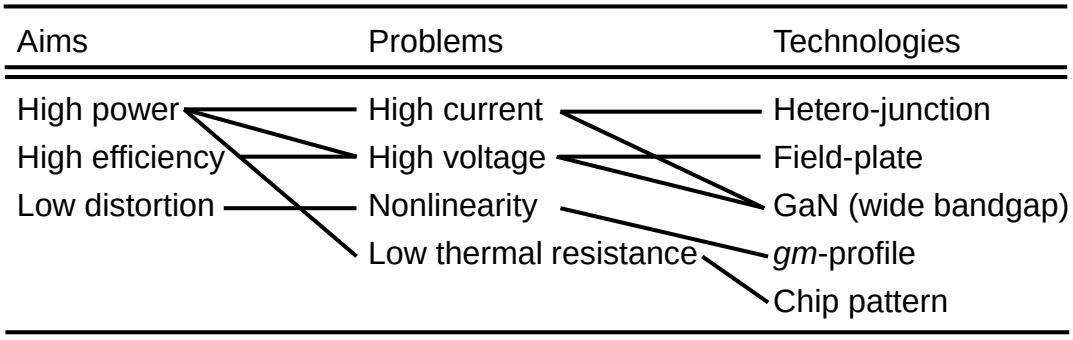


Fig. 1.3 Basic configuration of microwave high-power amplifiers.

1.1.2.1 Microwave high-power FET

Table 1.1 shows the problems and the technologies of microwave high-power FETs against the aims of high power, high efficiency, and low distortion at power amplifier. In general, there are trade-off relations in the problems of high current, high voltage, high linearity, and low thermal resistance. They are overcome by designing the structure and the material in high-power FET.

Table 1.1 Problems and the technologies of microwave high-power FETs against the power amplifier with high power, high efficiency, and low distortion.



In order to make it easy to understand the RF operation of FET, ideal Class-A operation is assumed.

The condition of the load-resistance (R_L) to obtain the maximum output power in ideal Class-A operation as shown in Fig. 1.4 is the following formula (1.1).

$$R_L = \frac{V_{br} - V_{knee}}{I_{\max}} \tag{1.1}$$

where I_{max} is the maximum drain current, V_{br} is the breakdown voltage, and V_{knee} is the knee voltage. The current bias condition of Class-A operation is 1/2 I_{max}.

Then, the maximum output power ($P_{o,\max}$) and the maximum power-added efficiency ($\eta_{add,\max}$) are expressed as the following formulas (1.2) and (1.3), respectively.

$$P_{o,\max} = \frac{I_{\max} \cdot (V_{br} - V_{knee})}{8} \tag{1.2}$$

$$\eta_{add,\max} = \frac{1}{2}\left(1 - \frac{1}{G}\right)\left(\frac{V_{br} - V_{knee}}{V_{br} + V_{knee}}\right) = \frac{1}{2}\left(1 - \frac{1}{G}\right)\frac{1}{\left(1 + \frac{R_{on}}{R_L}\right)} \tag{1.3}$$

where G is the RF gain and $R_{on}=V_{knee}/I_{max}$ shows the on-resistance which is equivalent to the resistance between the drain-electrode and the source-electrode when the FET is in on-state.

Here, it can be seen that high current and high breakdown voltage are required for high-power devices. Moreover, it is found that the devices with high breakdown and low knee voltage are suitable for high efficiency operation. Since the on-resistance is represented by the following expression (1.4), the microfabrication of the device-structure becomes important for high efficiency characteristics.

$$R_{on} = R_{ch} + R_s + R_d \propto L_g + L_s + L_d \tag{1.4}$$

where R_{ch} is channel resistance, R_s is source resistance, R_d is drain resistance, L_g is gate-length, L_s is source-gate distance, and L_d is gate-drain distance.

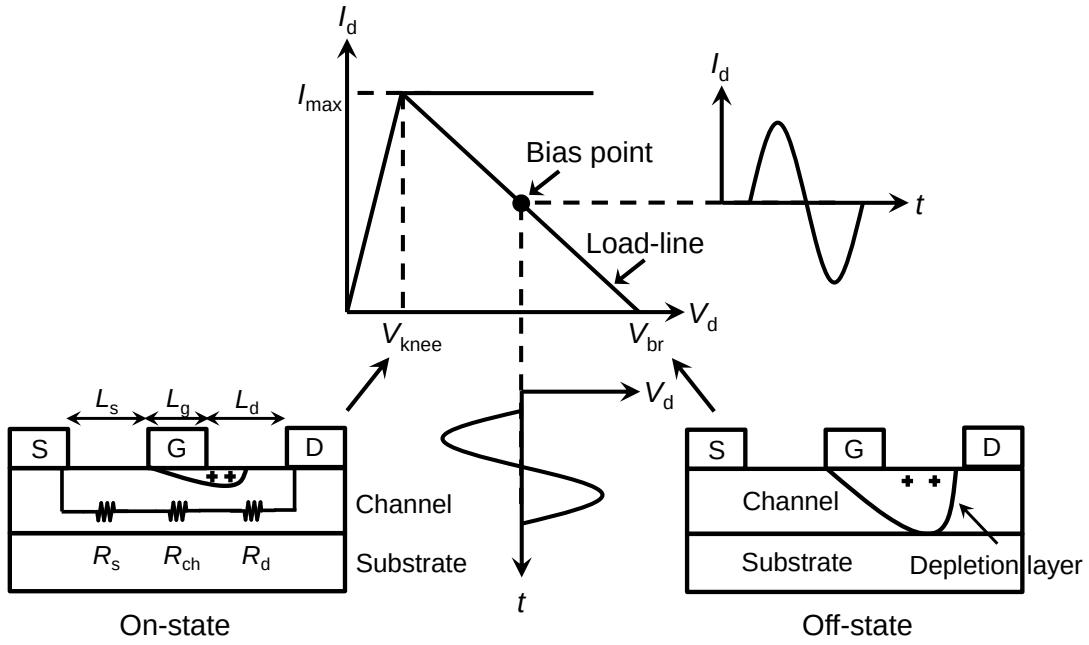


Fig. 1.4 Ideal Class-A operation.

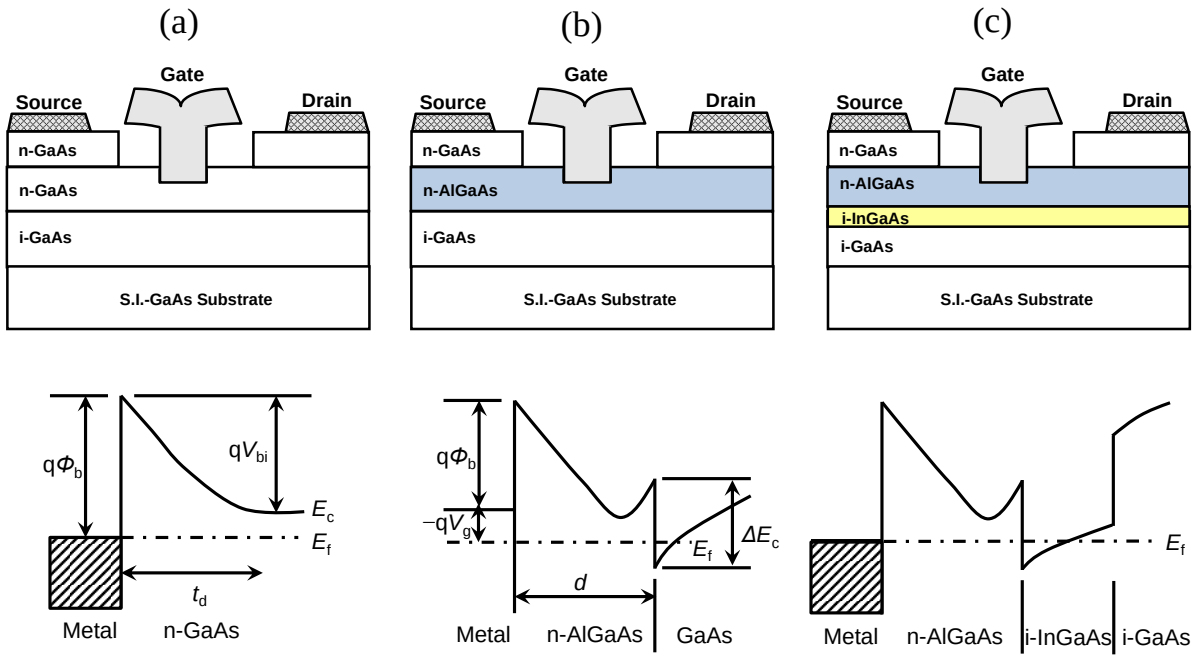


Fig. 1.5 Schematic cross-section and the energy band diagram of the typical microwave GaAs high-power FETs, (a) MESFET, (b) AlGaAs/GaAs HFET, (c) n-AlGaAs/i-InGaAs/i-GaAs pseudomorphic HEMT.

Figure 1.5 shows the schematic cross-section and the energy band diagram of the typical microwave GaAs high-power FETs used for the power amplifiers more than 1 W.

Figure 1.5 (a) shows the MESFET. MESFET uses the Schottky electrode with the rectification due to the contact of metal and semiconductor as the gate electrode. The current is controlled depleting the electron of the n-type channel layer by the gate-bias. The saturation drain current of the MESFET is represented by the following expression (1.5), assuming that all of the channel electrons under the gate transit with the saturation velocity v_s when the gate-length is sufficiently short [1.31].

$$I_{\max} = W_g (a - t_d) q N_d v_s \tag{1.5}$$

where W_g is the gate-width, a is the thickness of n-type semiconductor layer, q is elementary charge, N_d is the impurity concentration, v_s is the saturation velocity of electron, and t_d is the thickness of the depletion layer as follows (1.6).

$$t_d = \sqrt{\frac{2\varepsilon_s (V_{bi} - V_g)}{q N_d}} \tag{1.6}$$

where ε_s is the dielectric constant of the semiconductor and V_{bi} is the built-in potential of Schottky contact.

To increase the drain current density, the increase of impurity concentration, the increase of channel layer thickness, and the improvement of electron saturation velocity can be introduced from the above equations. However, there is a problem that the gate breakdown voltage V_{br} represented by the following formula (1.7) decreases when increasing the N_d and a [1.32].

$$V_{br} = \frac{\varepsilon_s F_a^{\,2} L_{eff}}{2 q N_d a} \tag{1.7}$$

where F_a is the avalanche breakdown voltage and L_{eff} is the equivalent gate-length as fitting parameter.

In the n-type layer in MESFET, the mobility of channel electron decreases due to the scattering caused by the donor impurity. The mobility of 8000 cm^2/Vs in the intrinsic semiconductor drops to about 2000 cm^2/Vs. In contrast, HFET employs GaAs for the channel layer, and AlGaAs of wider bandgap than GaAs for the Schottky layer. This is the same as the so-called HEMT. HFET is an advantageous structure to high output power performance since the gate leakage current at the large signal operation can be reduced by increasing the Schottky barrier height using AlGaAs as a barrier layer. Figure 1.5 (b) shows the schematic

cross-section and the energy band diagram of AlGaAs/GaAs HFET. In HFET, since the thickness of n-AlGaAs electron supply layer is thin enough, it is completely depleted, and free electrons are accumulated in the triangular potential formed in the interface of electron supply layer and i-GaAs channel layer. That forms the channel called two-dimensional electron gas (2DEG). GaAs can be lattice-matched with AlGaAs. Because of using a high-purity GaAs containing no impurities in the channel layer, high mobility can be obtained with almost no effect of the ionized impurity scattering. Thereby, high-speed and high-frequency operation can be realized. The two-dimensional electron gas concentration n_s is expressed as the following formula (1.8) [1.33], [1.34].

$$n_s = \frac{\varepsilon_s}{q(d+\Delta d)}\left[V_g - (\phi_b - \frac{qN_d d^2}{2\varepsilon_s} - \frac{\Delta E_c}{q} + \frac{E_{F0}}{q})\right] = \frac{\varepsilon_s}{q(d+\Delta d)}(V_g - V_{th}) \tag{1.8}$$

where d is the thickness of AlGaAs barrier layer, Δd is the channel thickness of 2DEG (≈8nm), N_d is the donor concentration, ΔE_c is the conduction band energy discontinuity in the heterointerface, E_{F0} is the Fermi energy at n_s=0, and Vth is the threshold voltage. The saturation drain current (I_{dsat}) is expressed as the following formula (1.9), assuming that the electron drift velocity equals to the saturation velocity $v_s=\mu E_s$ (μ is the mobility and E_s is the saturation electric field).

$$I_{dsat} = \frac{\varepsilon_s \mu W_g E_s}{d+\Delta d}\left[\sqrt{(V_g - V_{th})^2 + E_s{}^2 L_g{}^2} - E_s L_q\right] \tag{1.9}$$

where L_g is the gate-length. Assuming $E_sL_g << V_g - V_{th}$ (supposing a short gate-length), the following formula (1.10) can be obtained.

$$I_{dsat} = \frac{\varepsilon_s W_g v_s}{d+\Delta d}(V_g - V_{th}) \tag{1.10}$$

The current characteristics of HFET can be characterized by the value of $d+\Delta d$ and N_d. The cut-off frequency f_T showing a high-frequency performance is the following formula (1.11).

$$f_T = \frac{g_m}{2\pi C_{gs}} = \frac{v_s}{2\pi L_g} \tag{1.11}$$

HFET can be expected to obtain high frequency characteristics improvement due to high v_s.

Figure 1.5 (c) shows the schematic cross-section and the energy band diagram of n-AlGaAs/i-InGaAs/i-GaAs pseudomorphic HEMT using InGaAs for a channel layer as a material with higher electron mobility. High current and high frequency performance can be improved than AlGaAs/GaAs HEMT by carrier confinement effect of the double heterostructure.

However, as mentioned above, there is a tradeoff between the increase of the carrier density and the breakdown voltage. To improve the breakdown voltage is a problem. Figure 1.6 shows the schematic cross-section of high-voltage operation AlGaAs/InGaAs hetero-junction FET (HJFET) employing the dual-field plate electrode structure [1.19]. The electric field concentration to the gate-edge at high voltage operation is relaxed by the dual-field plates of gate-field plate and source-field plate. Not only can the breakdown voltage be improved by the electric field relaxation, but also the electron-capture to the trap in the semiconductor or in the interface of semiconductor and protection film can be suppressed. So-called current collapse can be improved. Thereby, high efficiency characteristics can be achieved improving the output decrease at high voltage operation. The gate-to-drain capacitance (C_{gd}) can be greatly reduced terminating the line of electric force by the source-field-plate (SFP) connected to the ground. Therefore, high-power device with high gain and high efficiency characteristics can be realized.

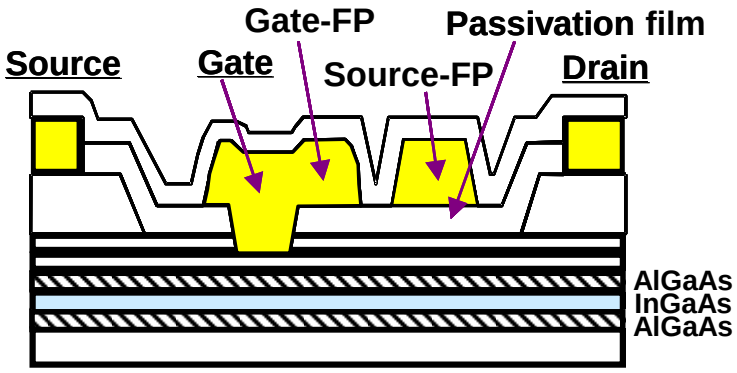


Fig. 1.6 Schematic cross-section of high-voltage operation AlGaAs/InGaAs HJFET.

Furthermore, when paying attention to the material, a wide bandgap semiconductor, GaN has attracted attention. Figure 1.7 shows the schematic diagram and the energy band diagram of AlGaN/ GaN heterojunction. The 2DEG generation mechanism of GaN HEMT is different from GaAs HEMT. GaN has a wurtzite structure, and the spontaneous polarization P_{SP} occurs along the c-axis direction within the crystal. When AlGaN with short a-axis lattice constant is grown on the Ga-face of GaN, the tensile strain occurs in AlGaN, and piezoelectric polarization P_{PE} is added to P_{SP}. The positive fixed charge is generated in the

AlGaN/GaN heterojunction interface by two polarization effect. According to the report of O. Ambacher [1.35], the relation between AlN mole fraction *x* and interfacial polarization charge *P*(x) becomes the following equation (1.12).

$$P(x) = P_{SP} + P_{PE} = (3.25x) + (1.15x^2 + 2x) \qquad (10^{13} cm^{-2}) \qquad (1.12)$$

The polarization charge extends to 1×10^{13}cm^{-2} at AlN mole fraction of 20%. This generates high-concentration 2DEG in the heterojunction interface. The 2DEG concentration is given by the following equation (1.13) in consideration of the influence of the interfacial polarization charge N_{PZ}.

$$n_s = \frac{\varepsilon_s}{q(d+\Delta d)}\left(V_g - V_{th}\right) = \frac{\varepsilon_s}{q(d+\Delta d)}\left(V_g - \Phi_B + \frac{qN_{PZ}d}{\varepsilon_s} + \frac{\Delta E_C}{q} - \frac{E_{F0}}{q}\right) \qquad (1.13)$$

It can be said that GaN is suitable for the channel layer of the high-power FET because the electron saturation velocity is twice as high as GaAs, and breakdown electric field is 10 times as high as GaAs as shown in Table 1.2 [1.36].

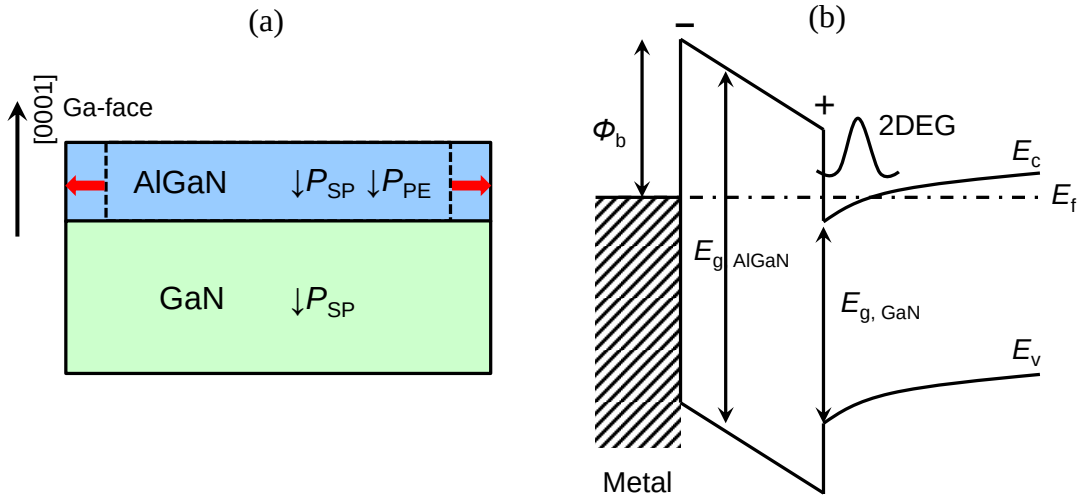


Fig. 1.7 (a) Schematic diagram and (b) energy band diagram of AlGaN/ GaN heterojunction.

Table 1.2 Comparison of material properties of SiC, GaN, GaAs, and Si.

Material		4H-SiC	GaN	GaAs	Si
Bandgap	E_g (eV)	3.26	3.39	1.4	1.1
Dielectric constant	ε	10	9	12.8	11.8
Thermal conductivity	κ (W/cm·K)	4.5	1.3	0.5	1.5
Electron mobility	μ (cm^2/V·s)	700	1600	8500	1350
Saturation velocity	v_s (cm/s)	2.0E7	2.5E7	2.0E7	1.0E7
Breakdown Field	E_b (V/cm)	2.0E6	3.3E6	4.0E5	3.0E5
Johnson's FOM	$(v_s E_b)^2$	180	760	7	1

The distortion in the high-power amplifier is caused by the non-linearity of the transistor. As for the nonlinear factor of transistor, the main elements are the transconductance (g_m), the drain conductance (g_d) of drain current, and the nonlinearity of gate capacitance (C_g). The high frequency drain current (i_d) and gate current (i_g) at large signal operation are indicated by Taylor-series expansion with gate voltage (v_g) (1.14), (1.15) [1.37]. Here, the most important nonlinear element that dominates the third-order intermodulation distortion (IM3) is a third-order transconductance (g_{m3}). The *gm*-profile can be optimized by designing the epitaxial structure of FET. Nonlinearity of the gate capacitance cannot be ignored at high frequency.

$$i_d = \sum_{k=1}^{n} g_{mk} v_g^k \tag{1.14}$$

$$i_g = \frac{d}{dt}\left(\sum_{k=1}^{n} C_{gsk} v_g^k\right) \tag{1.15}$$

As shown in Fig. 1.8 (a), the chip pattern of the comb form electrode structure is adopted to increase the gate width in the high-power FET. In high-power FET with large power consumption (P_{DC}), the thermal design is important. The channel temperature rise ΔT_{ch} is expressed as the following formula (1.16) [1.37].

$$\Delta T_{ch} = R_{th} \cdot P_{dis} = R_{th}(P_{DC} + P_{in} - P_{out}) = R_{th} \cdot P_{DC}(1 - \eta_{add}) \tag{1.16}$$

where R_{th} is the thermal resistance, and P_{dis} is the dissipation power. Although based also on the η_{add} at the actual high-power operation, the problem is to lower the thermal resistance. There are the thinning of the substrate and the expansion of the gate pitch (G_P) as the chip design for low thermal resistance. In addition, as shown in Fig. 1.8 (b), the metal plated heat sink (PHS) is formed on the substrate backside thinned to 20~30 μm. The PHS and source

electrode are connected by providing with a via-hole to the source electrode to minimize ground inductance. These high-power FET chips are mounted on the package with the metal heat sink having the high thermal conductivity and the thermal expansion coefficient close to the semiconductor such as GaAs.

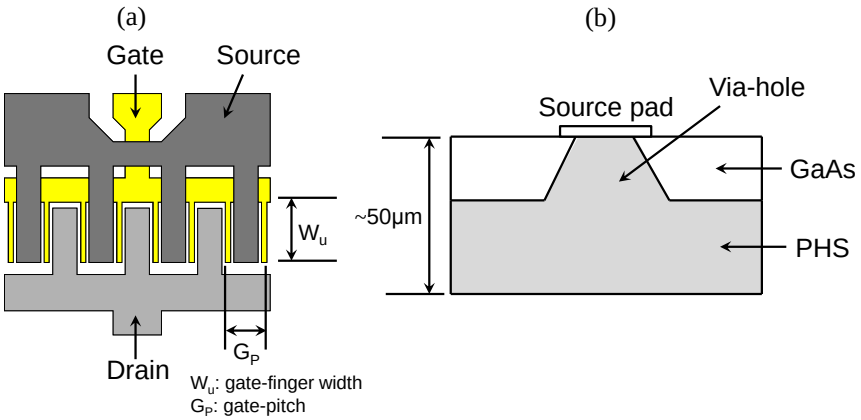


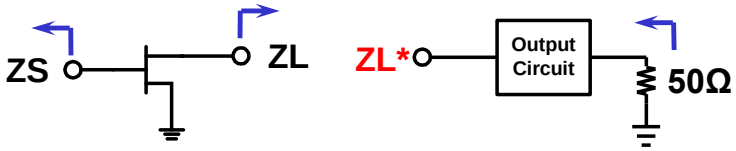
Fig. 1.8 Schematic (a) chip pattern and (b) cross section of source electrode of high-power FET.

As mentioned above, various technologies have been taken against the aims of high-power, high-efficiency, and low distortion in high-power FET.

1.1.2.2 Matching circuits

The circuit techniques of high power amplifiers are outlined from here.

Since the large gate-width is needed to obtain higher output power in high-power FET, the input and output impedance greatly decreases compared to the system impedance of 50 Ω. Therefore, the impedance matching is performed providing the impedance matching circuits directly connected to the chips in a package (PKG). There is a problem that the matching circuits of high-power FET realize the fundamental frequency matching and the harmonic terminations with low loss. As shown in Fig. 1.9, the matching circuit parameters are optimized so as to minimize the circuit return-loss measured from the system port when the port impedance of the transistor side is to be complex conjugate of the optimum load impedance for the transistor. The optimum load impedance is determined using for example, on-wafer source- and load-pull measurement system as shown in Fig. 1.10. Thereby, the transistor can operate on the optimum load condition.



ZL*: Complex conjugate optimum load impedance
Minimize the return loss measured from system port

Fig. 1.9 Optimization of matching circuit parameters.

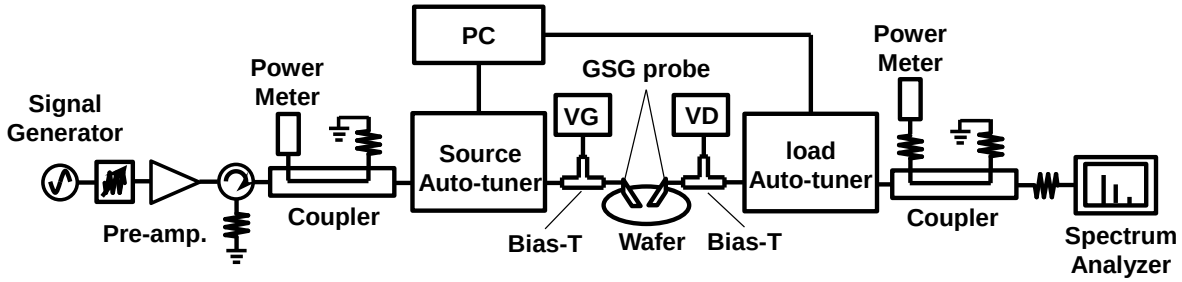


Fig. 1.10 Schematic of on-wafer source- and load-pull measurement system.

Figure 1.11 shows the typical matching circuit configuration of high-power FET. The matching circuit in high-power FET with low impedance generally takes the configuration of low-pass filter network which consists of the inductance of the bonding wires and the capacitance of the chip capacitors. When there is no room to configure the circuits in a small PKG, the high-pass filter type matching circuit composed of shunt inductor can be employed. It is also possible to configure the matching circuit using the distributed constant lines formed on the dielectric substrate. Depending on the desired circuit constant, using the impedance lines is able to set higher allowable current than bonding wires. However, since the circuit element has a loss, there is a problem that the impedance transformation loss increases, and the bandwidth becomes narrow as the impedance transformation ratio r (= $50/|Z_L^*|$ in Fig. 1.9) increases. Although the bandwidth and the circuit loss can be improved by increasing the number of circuit elements, the minimum number within permission should be selected considering the complexity of circuits. The following formula (1.17) indicates the relation between the transformation ratio and the transmission loss in the *LC* low pass filter networks with the loss. Figure 1.12 shows the calculation results.

$$Loss(dB) = -20Log(1+\frac{(r^{\frac{1}{2}}-1)^{\frac{1}{n}}}{2Q_0}) \tag{1.17}$$

where r is the transformation ratio, Q_0 is the Q-factor of circuit element, and n is the stage-number of low pass filter networks.

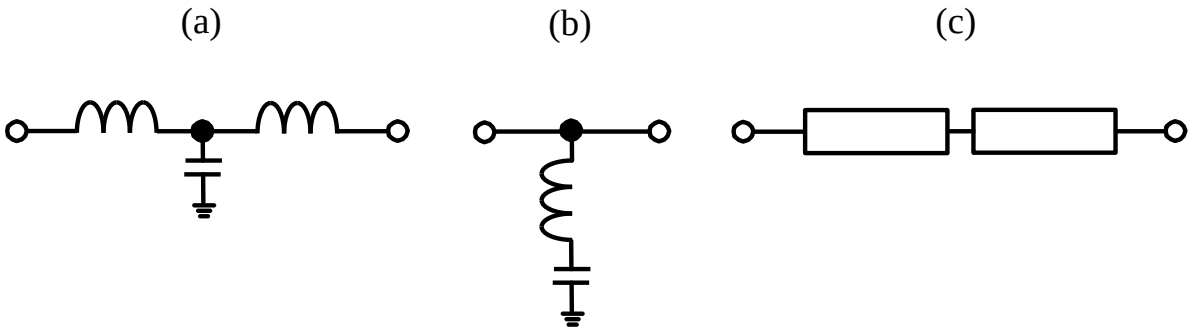


Fig. 1.11 Typical matching circuit configuration of high-power FET. (a) low-pass filter network type, (b) high-pass filter network type, (c) distributed constant line type.

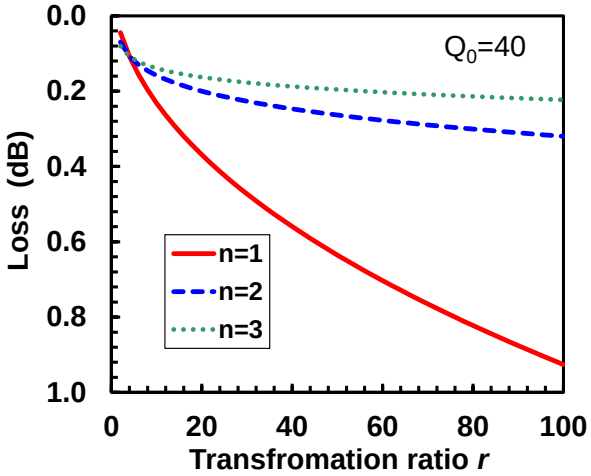


Fig. 1.12 Calculation results of the relation between the transformation ratio and the transmission loss in the *LC* low pass filter networks with the loss.

Moreover, in the high-power FET combining the multi-chips in parallel, a loop oscillation may occur between chips. In order to suppress the oscillation, the balance resistance can be prepared between chips on the matching circuits. Even when the amplifier is stable at the DC bias setting, a loop oscillation may occur from a certain RF input power level. Therefore, the loop oscillation analysis at the large signal operation is needed for the stable operation in the wide range.

1.1.2.3 Power combining circuits

The realization of the high-power amplifiers over 100W at 2-GHz-band has become challenging target for the third generation mobile phone base station. Also, the high-power amplifiers delivering the P_{sat} of from 200 W to 500 W are required for the macro-cell base station in the fourth generation system. These high-power amplifiers combine the output power of partially- or fully-matched several single-ended high-power amplifiers employing power dividing and combining circuits.

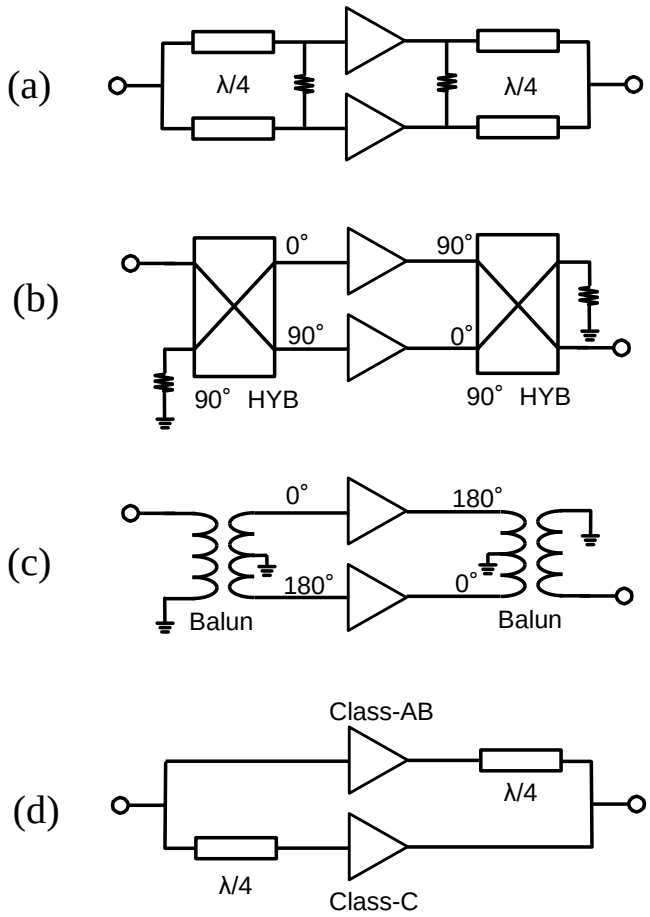


Fig. 1.13 Typical configuration of the high-power amplifiers using the typical two-branch type power-combining circuits. (a) in-phase power dividing/combining amplifier using the Wilkinson divider, (b) balance amplifier using the 3 dB-directional couplers of 0°-90°, (c) push-pull amplifier using the balun, (d) Doherty amplifier

Figure 1.13 shows the configuration of the high-power amplifiers using the typical two-branch type power-combining circuits. Figure 1.13 (a) shows the in-phase power dividing/combining amplifier using the Wilkinson divider composed of the quarter wave transmission lines and the isolation resistor. This type is characterized by high isolation between the branches obtained by the impedance transformation effect of quarter wave ($\lambda_g/4$) line and the isolation resistor. The distributed constant line with the characteristic impedance of Z_0 and the line-length of l can transform the impedance of Z_1 to the impedance of Z_2 as follows (1.18).

$$Z_2 = Z_0 \frac{Z_1 + jZ_0 \tan(\beta l)}{Z_0 + jZ_1 \tan(\beta l)} \tag{1.18}$$

where $\beta = 2\pi/\lambda_g$. Especially, when $l = \lambda_g/4$, (1.18) becomes as follows (1.19).

$$Z_1 \cdot Z_2 = Z_0^{\,2} \tag{1.19}$$

This quarter wave line is employed in various microwave circuits.

The balance amplifier shown in Fig. 1.13 (b) uses the 3 dB-directional couplers of 0°-90° for input/output dividing/combining circuits. Therefore, the two amplifiers composing the balance amplifier operate with a phase difference of 90° each other. The balance type not only can take the isolation between branch ports (balance ports) by a termination resistor, but also is characterized by being able to make the reflection coefficient at an input or an output signal port small even if not taking the matching at a balance port.

The push-pull amplifier shown in Fig. 1.13 (c) uses the 0°-180° couplers or balun (balance-unbalance) circuits for power dividing/combining circuits. The two amplifiers of push-pull configuration operate with the phase difference of 180° each other. Since the two amplifiers operate with the opposite phase, the fundamental frequency is combined in-phase at the output port through the 180° coupler, and the even order harmonics are cancelled at the output port. That is to say, in the push-pull amplifier, even-order harmonics are not generated. Furthermore, in the push-pull amplifier using the balun circuits, since balun itself has the impedance transformation effect, the two amplifiers of push-pull configuration require only to match to 25 Ω, respectively. Since the two amplifiers combined in single-end need to match to 100 Ω, respectively, a push-pull amplifier has four times merits compared with a single-ended amplifier against an impedance transformation ratio. Thus, since the push-pull amplifier is an efficient amplifier in power-combining, the examinations were promptly advanced as the configuration of the wireless base station amplifiers. Broadband and low-loss power-combining circuit becomes essential to achieve the high output power more than 100 W at 2-GHz-band. Conventionally, the balun circuits have been fabricated using coaxial lines. Newly, the balun circuits configured in microstrip coupled lines were developed by utilizing an electromagnetic field analysis [1.16].

Doherty amplifier shown in Fig. 1.13 (d) combines the output power of the main amplifier biased in Class-AB and the peak amplifier biased in Class-C through a quarter wave line [1.21]. A quarter wave line is connected to the main amplifier side. Since a quarter wave line has the phase difference of 90°, the input side is constituted using a 90°-hybrid circuit, or a quarter wave line. Thereby, the output power is combined in-phase. Doherty amplifier is characterized by the efficiency characteristics improvement of 6 dB back-off due to the load impedance shift of the main amplifier caused by the impedance transformation effect of the quarter wave line at signal input. However, Doherty amplifier has a problem that the distortion characteristics deteriorate due to the distortion the peak amplifier generates in

Class-C operation. The problem is to establish the design methods of Doherty amplifier to achieve both high efficiency and low distortion characteristics.

1.1.2.4 Bias circuits

Figure 1.14 shows a typical gate bias circuit and drain bias circuit used for microwave high-power FET amplifier. It is basic to design the bias circuit of microwave amplifier so as not to generate the loss in fundamental frequency band. Therefore, the other end of the quarter wave line at fundamental frequency is short-circuited by a capacitor. This is because, as is introduced by the formula (1.19), the other end of the short-circuited quarter wave line becomes open, and does not affect the RF signal. The gate bias circuit may prepare a resistor in the line end for the stabilization of the amplifier. In the high-power amplifier with low frequency below 1 GHz, a chalk inductor may be used instead of a quarter wave line.

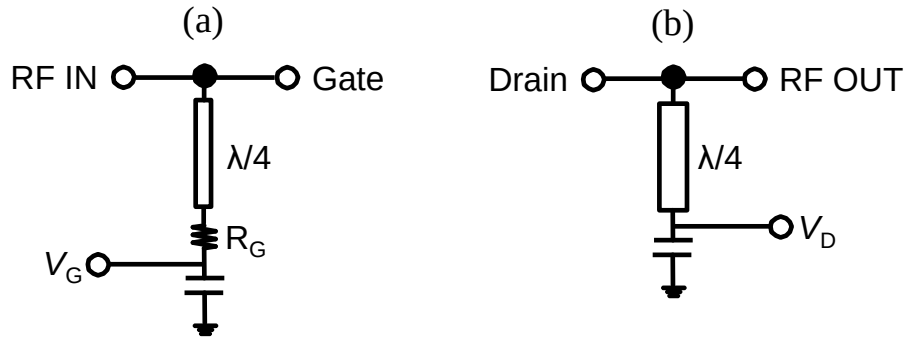


Fig. 1.14 Typical (a) gate bias circuit and (b) drain bias circuit used for microwave high-power FET amplifier.

As shown in Fig. 1.15 (a), the digital modulation signals handled by modern mobile phone communication systems have the bandwidth according to the bit rate. If the signal has a bandwidth, difference frequency corresponding to the band width is caused by the second-order nonlinearity of the transistor. This difference frequency, influenced by the low-frequency impedance of the drain bias circuit, would degrade the distortion characteristics being superimposed on the third-order intermodulation when the mixing of the fundamental frequency and the difference frequency occurs. These phenomena are called the memory effect [1.25]. The main factor of low-frequency impedance increase of the drain bias circuit is the inductance component of the quarter wave line.

For simplicity, the memory effect of the amplifier is found by measuring the frequency spacing (Δf) dependence on two-tone IM3 characteristics as shown in Fig. 1.15 (b). When there is a memory effect, the difference is generated in the magnitude and phase of the upper and lower IM3 components ($2f_1-f_2$, $2f_2-f_1$). The degradation of the distortion

characteristics by such a memory effect can be suppressed by short-circuiting the low-frequency impedance of the drain and gate side. In the fourth generation mobile phone system of the multi-carrier signal that enables high-speed, large-capacity communication, the broadband characteristics of 100 MHz is required for the IM3-Δ*f* characteristics. Technical proposals for that purpose are necessary.

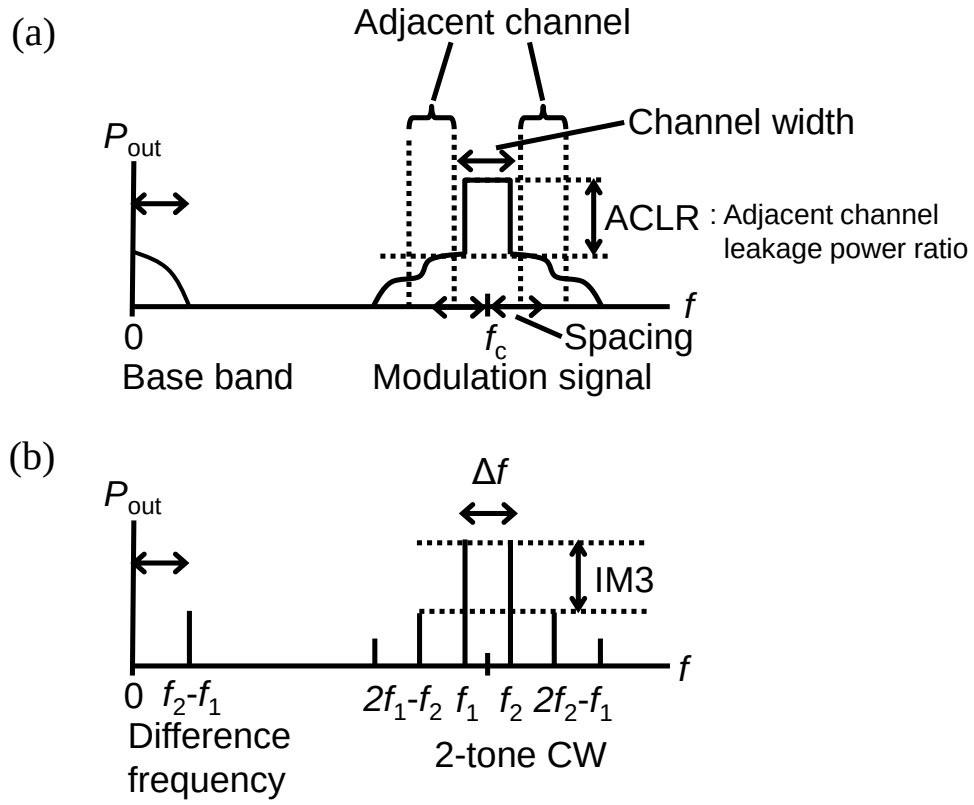


Fig. 1.15 Schematic output signal spectrum in high-power amplifier under (a) the digital modulation signal and (b). the two-tone CW

1.1.2.5 Distortion compensation techniques

There is a problem that the distortion characteristics deteriorate when operating in the nonlinear region where microwave amplifier can obtain high efficiency characteristics. In the high-efficiency microwave amplifier, the distortion characteristics can be improved with distortion compensation techniques. The typical distortion compensation techniques are a feedback method, a feedforward method, and a predistortion method [1.38].

In the feedback method shown in Fig. 1.16, the distortion characteristics are improved by a loop gain at the negative feedback of a part of output power to the input side. The approach to feedback the carrier signal directly is not practical because of the stability and the small gain characteristics of the amplifier in the microwave band.

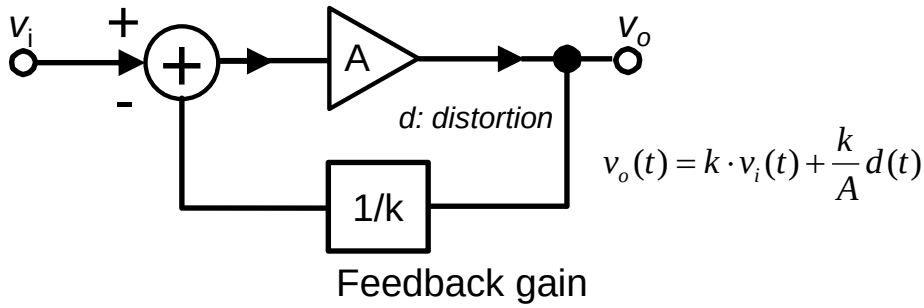


Fig. 1.16 Feedback distortion compensation method.

The feedforward distortion compensation amplifier shown in Fig. 1.17 is composed of a carrier amplifier, a carrier signal canceling loop for extracting the distortion component generated by the carrier amplifier, an error amplifier for amplifying the extracted distortion component, and a distortion canceling loop for canceling the distortion component included in the carrier signal using it. Large distortion compensation amount can be obtained by performing the distortion compensation using the distortion itself generated by the carrier amplifier in the feed-forward amplifier. However, since the delay lines for phase adjustment and an error amplifier are required, the circuit-size becomes large, and the power consumption also increases.

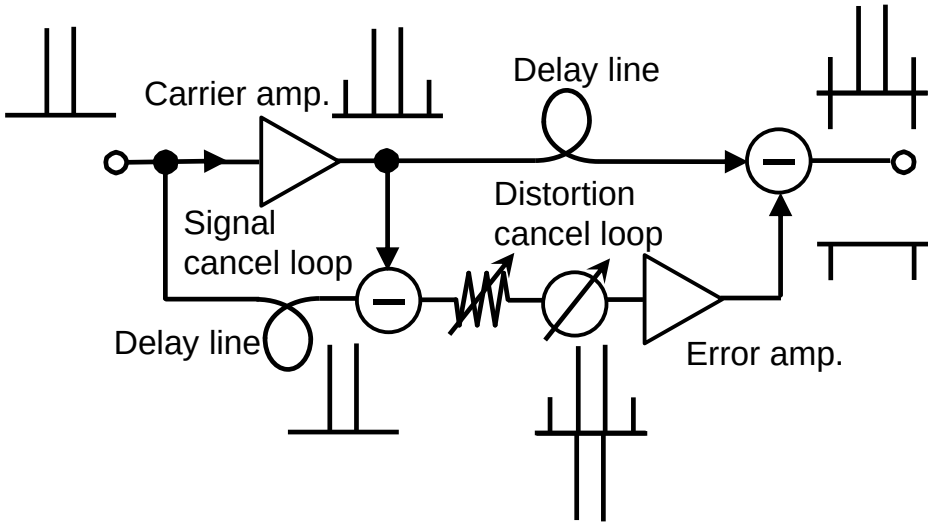


Fig. 1.17 Feedforward distortion compensation amplifier.

In the pre-distortion method shown in Fig. 1.18, the distortion characteristics (amplitude-to-amplitude modulation: AM-AM, and amplitude-to-phase modulation: AM-PM) of the entire amplifier can be cancelled by using the inverse characteristics of the distortion characteristics (AM-AM, AM-PM) generated by the power amplifier (PA) as the input signal. The predistortion method is advantageous in terms of the efficiency and the downsizing of the circuits.

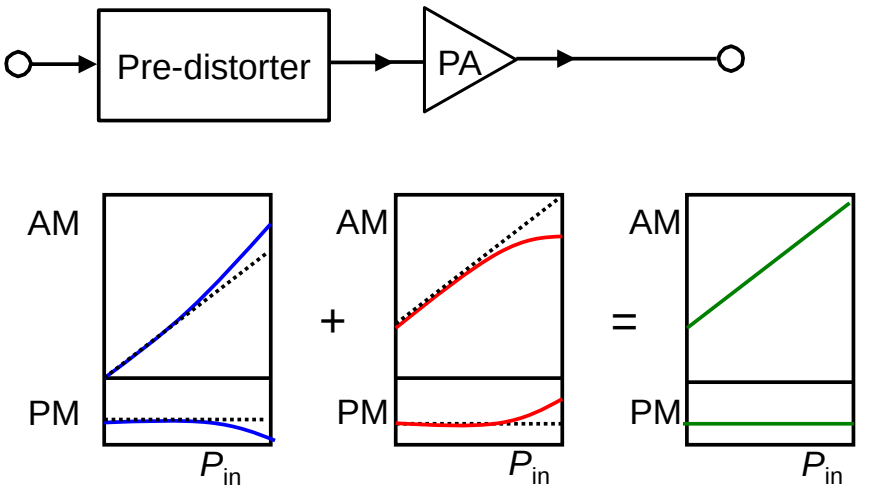


Fig. 1.18 Predistortion method.

Figure 1.19 shows the baseband digital pre-distortion (DPD) amplifier making the baseband signal of the digital modulation signal an inverse characteristic. The speed improvement of the digital signal processing circuits in recent years enabled the DPD method. It is corresponding also to the expansion of the modulation signal bandwidth by the advancement of the communication system. The DPD method is becoming the mainstream of the distortion compensation techniques of the mobile phone communication system. The memory effect that occurs in the amplifier becomes a problem here. Since the DPD method creates the inverse distortion characteristics of the amplifier in advance, it is impossible to compensate the distortion if the distortion characteristics of the amplifier have differed when inputting the inverse characteristic signal. The technical proposals have been made to suppress the memory effect of the amplifier to a broadband. In recent years, low distortion and high efficiency characteristics have been demonstrated by the combination of DPD and Doherty, or ET circuits.

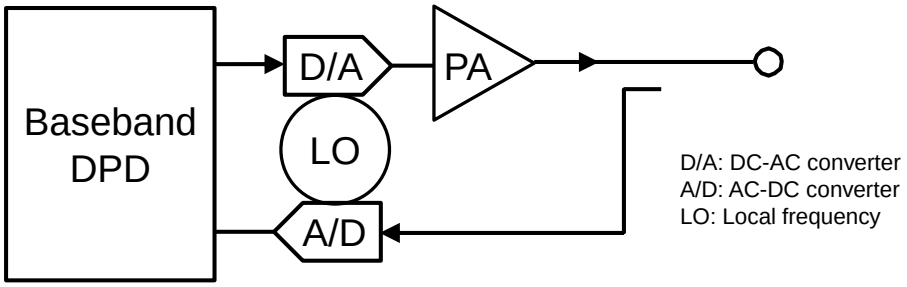


Fig. 1.19 Baseband digital predistortion amplifier.

1.2 Purpose and significance of this dissertation

This study was carried out under the above-mentioned background. The purposes of this study are as follows.

Firstly, a novel low loss broadband microwave power combining circuit is proposed, and the high-efficiency push-pull amplifier more than 100 W at an L/S-band is demonstrated using the proposed circuit. In addition, the instability analysis method at the large signal operation is established and demonstrated. This is a problem in case of the power-combining of the high-power amplifier.

Secondly, the matching circuit configuration with a new harmonic termination conditions is proposed by establishing the matching circuit design method for high-efficiency high-power amplifier. The effectiveness of the design method is verified by observing the actual voltage waveform by the EOS method. The best performance of high efficiency and high output power characteristics is demonstrated.

Thirdly, the design techniques of low distortion devices and circuits for the realization of low-distortion high-power amplifiers are established. The device structure to achieve both low distortion and high efficiency characteristics is proposed. The low distortion second harmonic termination matching circuits are proposed by investigating the effect of the second harmonic and the difference frequency impedance on the third-order distortion characteristics. In addition, to achieve low distortion characteristics without deterioration over the difference frequency spacing of 100MHz which was not be realized until now, the source- and load-difference frequency termination circuits in package as well as the technique lowering drain bias circuit impedance are proposed.

Fourthly, a new Doherty amplifier is proposed to achieve both high efficiency and low distortion characteristics. The design method of optimal Doherty amplifier based on the impedance of the load pull characteristics of the device is proposed. In order to solve the problem of the distortion characteristic degradation which exists in the Doherty amplifier, the design method for performing the distortion compensation by the distortion cancellation of the main and peak amplifiers of the Doherty amplifier is proposed. In addition, the evaluation technique of each amplitude-to-amplitude modulation (AM-AM) and amplitude-to-phase modulation (AM-PM) characteristics of the main and the peak amplifiers in an operating Doherty amplifier is proposed, and the distortion cancellation mechanism of the main and the peak amplifiers in Doherty amplifier linearity is experimentally proved for the first time.

Fifthly, as a further possibility of wide bandgap semiconductor GaN, the deployment of broadband, high efficiency, and low distortion amplifier using GaN FET is demonstrated. The base station high-power amplifiers and the cable television (CATV) power amplifier modules are exemplified to achieve the realization of high performances which cannot be realized in the conventional devices, using the GaN FET of high-voltage operation and high power density. The Doherty amplifier using GaN FET is developed optimizing the device structure to improve the efficiency characteristics of the GaN FET on low cost Si substrate for base station amplifiers. The high-efficiency and low-distortion characteristics of the highest level employing the DPD techniques in the GaN FET Doherty amplifier are demonstrated. Furthermore, the distortion compensation at the device level by the distortion cancellation effect of the high *gm* GaAs HJFET and the GaN FET is demonstrated employing Volterra distortion analysis on load-line based on the pulsed-*IV* characteristics in the CATV power amplifier module. The realization of broadband and low distortion characteristics of the highest level is aimed by the techniques of the gm profile optimization.

1.3 Outline of this dissertation

This dissertation consists of seven chapters. The outline of this dissertation is shown in Fig. 1.20.

Chapter 1 "Introduction" describes the history and technology trends of microwave high-power device development as a background of this study. Next, the composition of a microwave high power amplifier and the problem of the device and circuit technique in high power amplifier are described. Then, the purpose and meaning of a main subject are described and the composition of a main subject is shown.

Chapter 2 "Push-pull high power amplifiers using a microstrip balun" describes the study results on the push-pull power combining circuit and the stability analysis under the large-signal operation for microwave high-power amplifiers.

Chapter 3 "High efficiency high-power amplifiers with second harmonic termination" describes the study results on high efficiency microwave high power amplifiers.

Chapter 4 "Low distortion GaAs HJFET high-power amplifiers using second harmonic and difference frequency termination techniques" describes the study results on low distortion microwave high power amplifiers.

Chapter 5 "Inverted Doherty high-power amplifiers with high efficiency and low distortion" describes the study results on low distortion and high efficiency Doherty amplifiers.

Chapter 6 "Broadband low distortion and high efficiency GaN FET high power amplifiers" describes the study results on broadband, high efficiency, and low distortion microwave high-power amplifiers using GaN FETs.

Chapter 7 "Conclusions" summarizes this dissertation, and describes the challenges and prospects for the future.

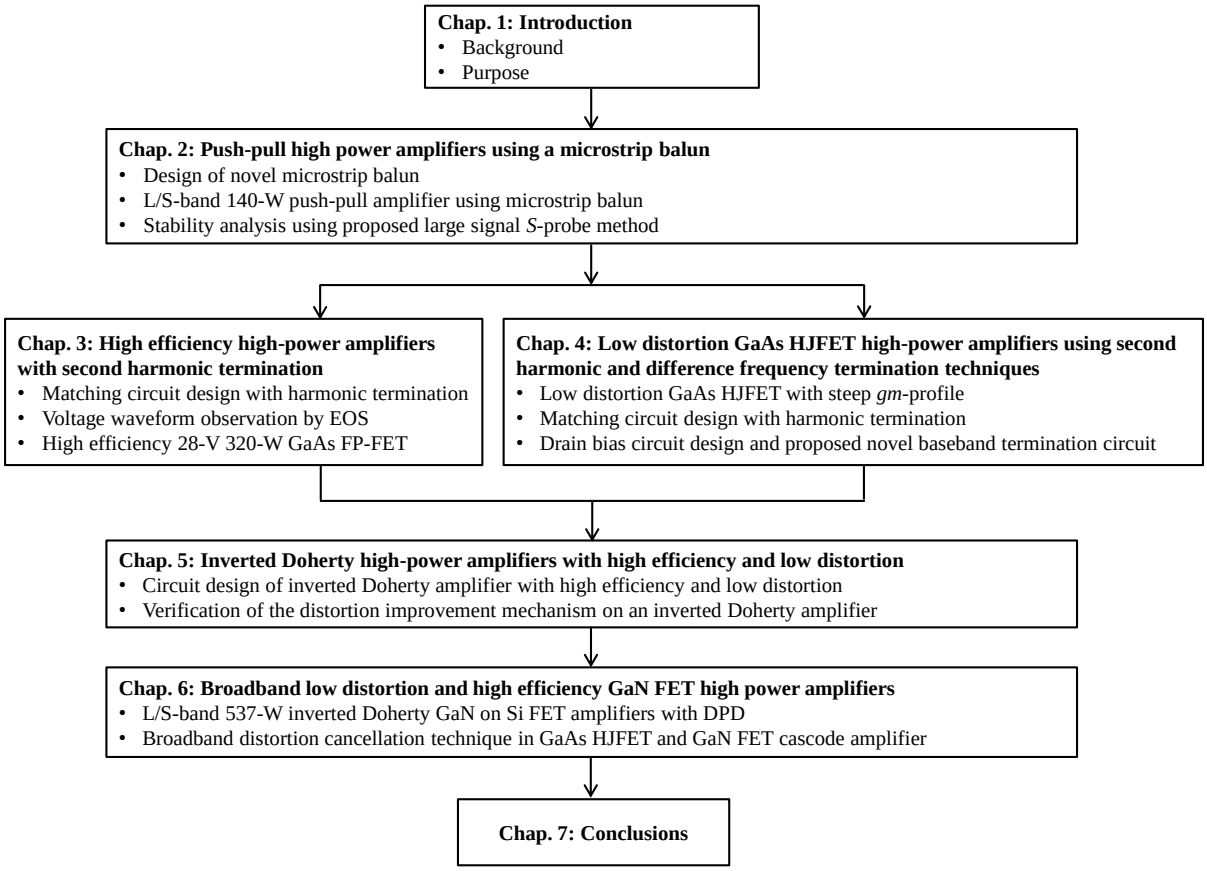


Fig. 1.20 Outline of this dissertation.

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Chapter 2

Push-pull high power amplifiers using a microstrip balun

2.1 Introduction

The emergence of next-generation personal digital communication services such as W-CDMA in the 1.8 to 2.2-GHz frequency range has stimulated a great demand for linear and high power base station transmitting amplifiers. For such applications, high output power level of more than 100 W is one of the most challenging requirements for the final stage devices in the solid-state power amplifiers (SSPAs) because of the size and cost reduction. For the above 100-W class device, it is the key to develop high thermally reliable device structure and low-loss power combining technique. The thermal reliability problems arise from the increased power dissipation. The device thermal destruction is caused by an increase of channel temperature and thermal run-away promoted by gate leakage current. In this study [2.1], [2.2], to avoid these problems, newly designed AlGaAs/GaAs heterostructure FET (HFET) with excellent DC and RF characteristics was employed. This HFET has higher Schottky barrier height than a GaAs MESFET, resulting in a low gate leakage current. In addition, the FET chip pattern was optimized to reduce the thermal resistance. For a power combining technique, a push-pull power combining technique with a balun-transformer was employed. It has the advantage that the impedance transforming loss is suppressed since the balun itself works as the impedance transformer. To realize efficient push-pull approach, a novel low-loss microstrip balun was designed [2.2].

In the high-power FET amplifier operating several FET chips in parallel, the operation stability against the odd-mode loop oscillation, in which FET on the loop is operating with inverse phase each other, becomes important.

Since the loop gain analysis techniques in the amplifier so far were limited to the stability analysis at the DC or small signal operation [2.3], [2.4], they were not effective in the loop oscillation at the large signal operation which is dependent on the input-power and input-frequency. In this study, in order to determine the loop gain occurring in the FETs and the circuits at the large signal operation, a new large-signal loop gain analysis technique was proposed combining the harmonic balance simulation and the *S*-probe circuit which can determine the reflection coefficient in arbitrary point without affecting circuit characteristics. The proposed method reproduced the oscillation phenomenon at the large signal operation in the C-band (5.9 GHz) 60-W power amplifier which combines four chips of AlGaAs/GaAs HFETs in parallel. It clearly showed that the cause of an oscillation is due to loop gain increase. Furthermore, it showed the effect on the design of the balance resistance connected between the chips for the oscillation suppression, and it contributed to the stable operation of the amplifiers.

2.2 Configuration of push-pull amplifier

To obtain more than 100-W-output power level, it is necessary to combine the output power of very large total gate-width devices with very low impedance. A high impedance transformation ratio is needed to match the input and output impedance of the FET to 50 Ω, so that the transforming loss reduction of the matching circuit becomes more crucial. In this case, the push-pull configuration using the balun-transformer for power-divider/combiner offers an efficient solution. This approach has the following advantages:

(1) The impedance transformation ratio of the matching circuit can be reduced because the balun itself can work as an impedance transformer. Therefore, the push-pull configuration allows the designer to realize less matching loss and broader bandwidth than a paralleled amplifier.

(2) A balun without resistive terminations has comparatively low loss and broader bandwidth characteristic [2.5].

(3) Even-order harmonic spurious can be suppressed [2.6].

Since the mutual amplifiers combined in a push-pull configuration operate with the phase difference of 180° as shown in Fig. 2.1, the output voltage of each amplifier has the relation represented as the following formula (2.1), (2.2).

$$V_o(t,\varphi) = A_0 + A_1\cos(\omega_0 t + \varphi_1) + A_2\cos(2\omega_0 t + \varphi_2) + A_3\cos(3\omega_0 t + \varphi_3) + A_4\cos(4\omega_0 t + \varphi_4) + \cdots \quad (2.1)$$

$$\begin{aligned} V_o(t,\varphi+\pi) &= A_0 + A_1\cos(\omega_0 t + \varphi_1 + \pi) + A_2\cos(2\omega_0 t + \varphi_2 + 2\pi) + A_3\cos(3\omega_0 t + \varphi_3 + 3\pi) + A_4\cos(4\omega_0 t + \varphi_4 + 4\pi) + \cdots \\ &= A_0 - A_1\cos(\omega_0 t + \varphi_1) + A_2\cos(2\omega_0 t + \varphi_2) - A_3\cos(3\omega_0 t + \varphi_3) + A_4\cos(4\omega_0 t + \varphi_4) - \cdots \end{aligned} \quad (2.2)$$

When the both signals are combined with a 180° phase shifter, the each other formula has the inverted phase, and the even-order components are cancelled each other, and the output of a fundamental and the odd-order components are doubled.

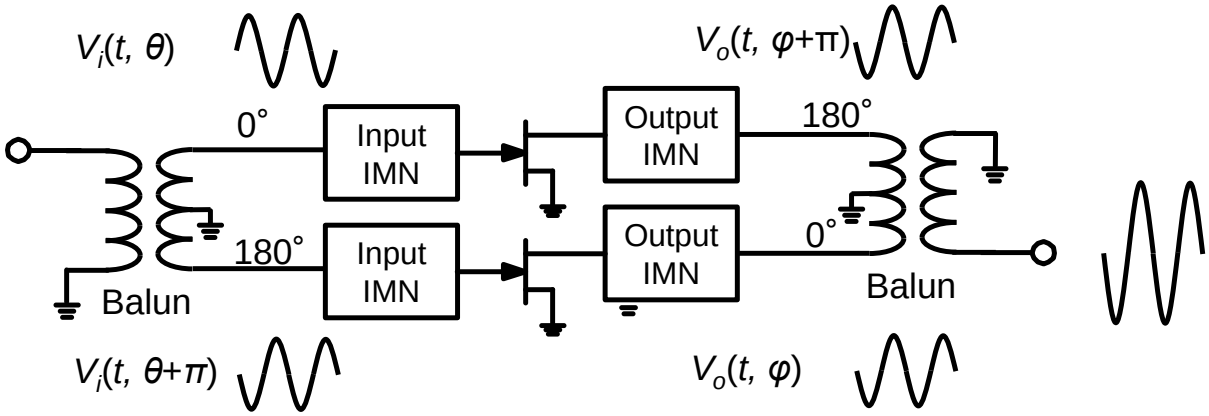
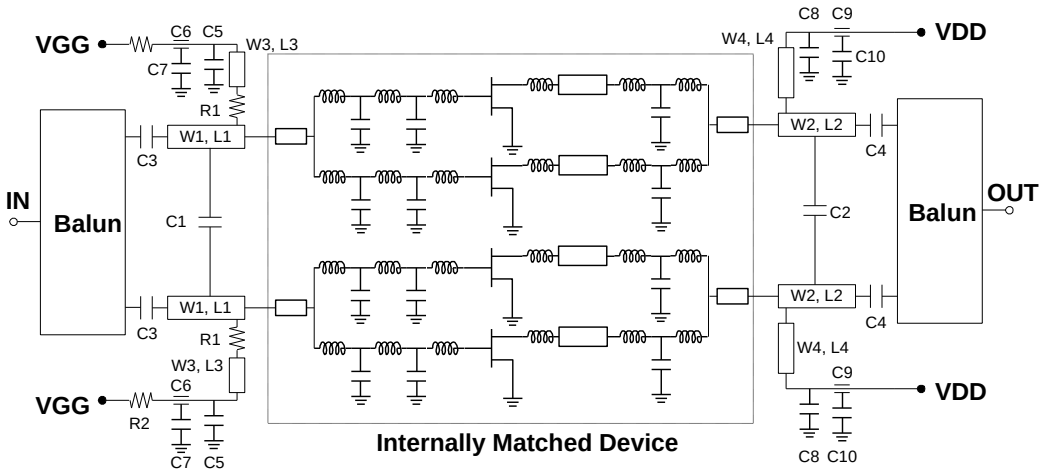


Fig. 2.1 Push-pull configuration.

To make good use of these advantages, a novel low loss and broadband 1:1 balun has been developed. Figure 2.2 shows the developed push-pull amplifier circuit. The amplifier employs two pairs of pre-matched GaAs chips mounted on a single package, and the total output-power was combined in a push-pull configuration with a low-loss microstrip balun circuit. Since the 1:1 balun can work as the impedance transformer from the 50-Ω asymmetric port (system port) to the 25-Ω symmetric ports (device-connected ports), the push-pull configuration of the two pairs allows us to reduce the impedance-transformation ratio of the internal matching circuit to a quarter of a four-chip parallel combining, resulting in reducing the loss of matching circuits.



External Circuit Value

C1 (pF)	C2 (pF)	C3 (pF)	C4 (pF)	C5 (uF)	C6 (pF)	C7 (uF)	C8 (uF)	C9 (pF)	C10 (uF)	R1 (Ω)	R2 (Ω)	W1, L1 (mm)	W2, L2 (mm)	W3, L3 (mm)	W4, L4 (mm)
1	1	39	39	2.2	1000	22	2.2	1000	22	4.7	5.0	5.5, 25	5.5, 25	4.0, 26	4.0, 26

Fig. 2.2 Overall push-pull amplifier circuit.

2.3 Design and fabrication of a novel microstrip balun

Figure 2.3 shows the configuration of the balun using a coaxial cable. It is constructed using the two coaxial lines of which the other end of the outer conductor side is shorted. The line A produces the balance-unbalance termination. The other line B works as the shorted-stub of a quarter wave length to improve the symmetry. The length of the coaxial line is approximately 1/4 wavelength of 35 mm at 2.2 GHz. The characteristic impedance Z_a is 50 Ω. Since $Z_a^2 = 2R \times 50$, the balance-port impedance R is matched to 25 Ω against the system impedance of 50 Ω [2.7].

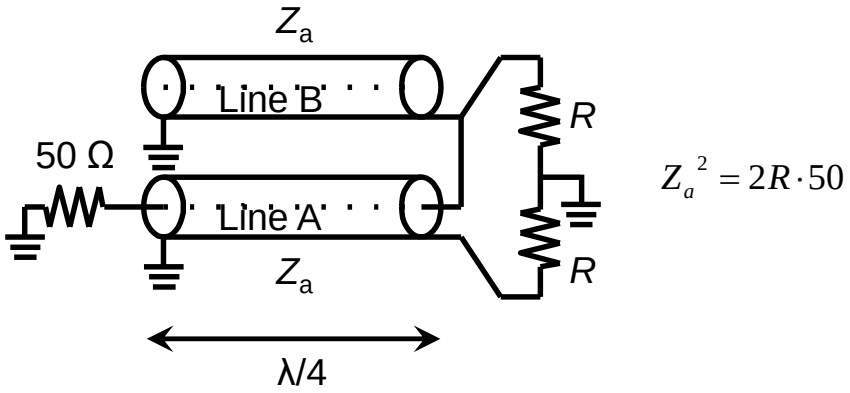


Fig. 2.3 Coaxial balun circuit.

Figure 2.4 shows the circuit configuration of the balun using microstrip coupled-lines. This is a balun type called Marchand balun. Marchand balun is excellent in a high frequency

characteristic, and has a broadband characteristic [2.8]. It is constituted from 1/4 wavelength coupled-lines of operating frequency, and is characterized by having an open-end coupled-lines and two short-end coupled-lines. The characteristic impedance (Z_a, Z_b) of the lines connected to an unbalance-port and a balance-port is set to each load-impedance. In this case, Z_a is 50 Ω and Z_b is 25 Ω. The open-end line connected to the unbalanced signal transmission line works as an open stub for creating a virtual ground. Also, the short-end lines serve as ground lines.

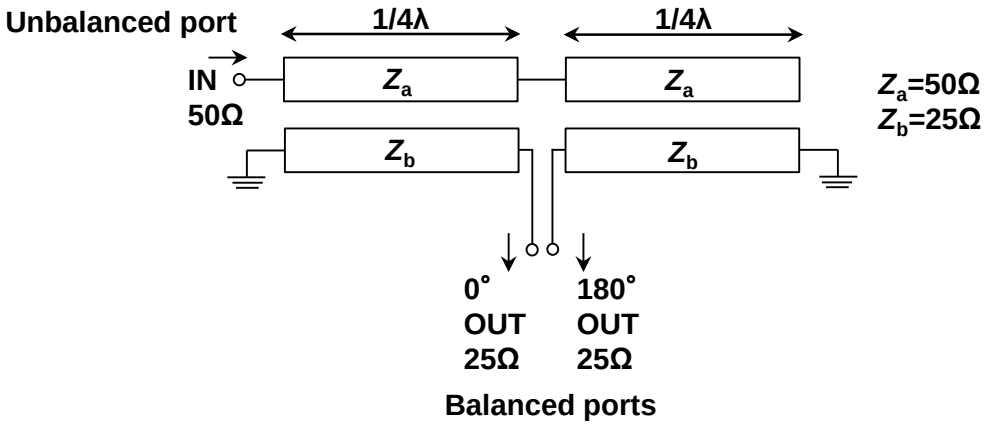


Fig. 2.4 Marchand balun circuit.

A novel microstrip balun was proposed and designed with an electro-magnetic (EM) simulation. Figure 2.5 shows the layout of the developed microstrip balun. The circuit configuration is shown in Fig. 2.6. The substrate of the 0.8mm thickness and the dielectric constant of 2.3 were employed. The uppermost conductor plane contains the input line (balun unbalanced line), the output lines (balun balanced line), and the compensating open stub. Each line-width of these quarter-wave-coupled lines was optimized to match the unbalanced port impedance of 50 Ω to the balance port impedance of 25-Ω each. The middle conductor plane carries the ground plane for the lines in the uppermost plane. The 1.2 mm depth hole for the balun resonant cavity is cut in the circuit fixture, and covered with the middle conductor plane. On this microstrip balun, separate ground planes replace the shields of each upper conductor plane. This new configuration enables us to freely select the direction of input and output balun-ports, and is more suited for combining push-pull devices than the previous layout [2.9], [2.10]. Moreover, increasing the number of stages of the coupled-lines contributes to the low-loss characteristics.

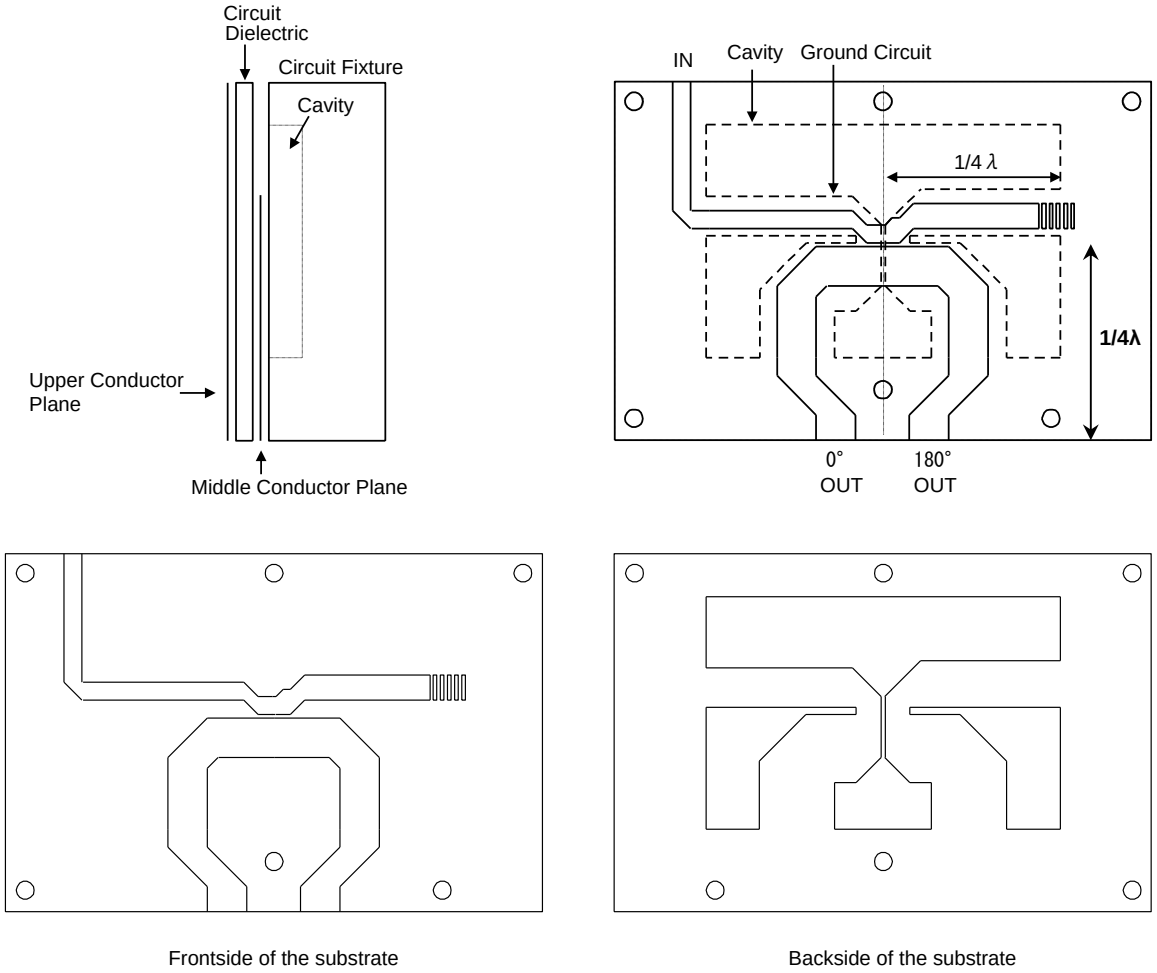


Fig. 2.5 Layout of the developed microstrip balun.

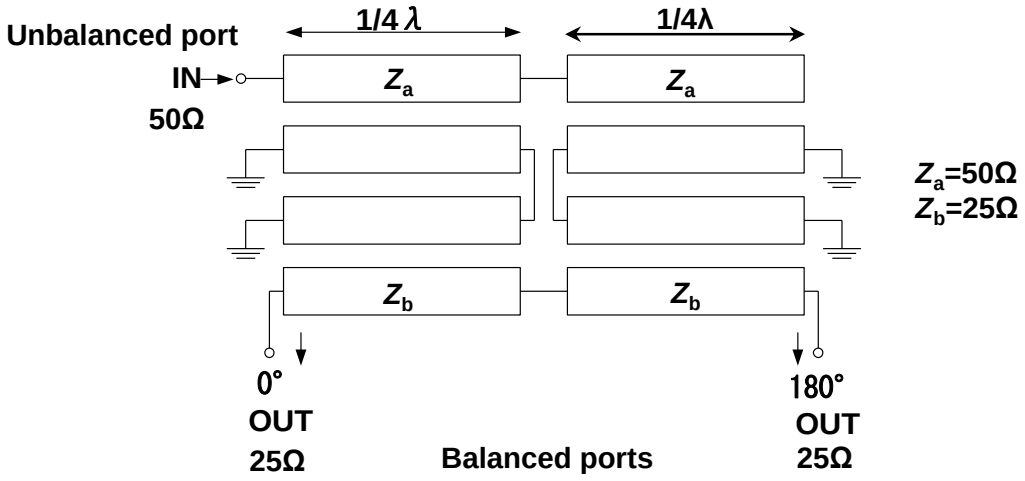


Fig. 2.6 Circuit configuration of the developed microstrip balun.

Figure 2.7 compares the measured performance of the balun with the EM simulation results. The thick line shows the measurement results and the thin line shows the EM simulation results. Measured responses are close to the simulation results. The developed balun showed low loss and broadband characteristic with an insertion loss of 0.3 dB, and

maximum phase and amplitude imbalance of less than 2° and 0.2 dB, respectively, in the 1.8 to 2.3-GHz frequency range.

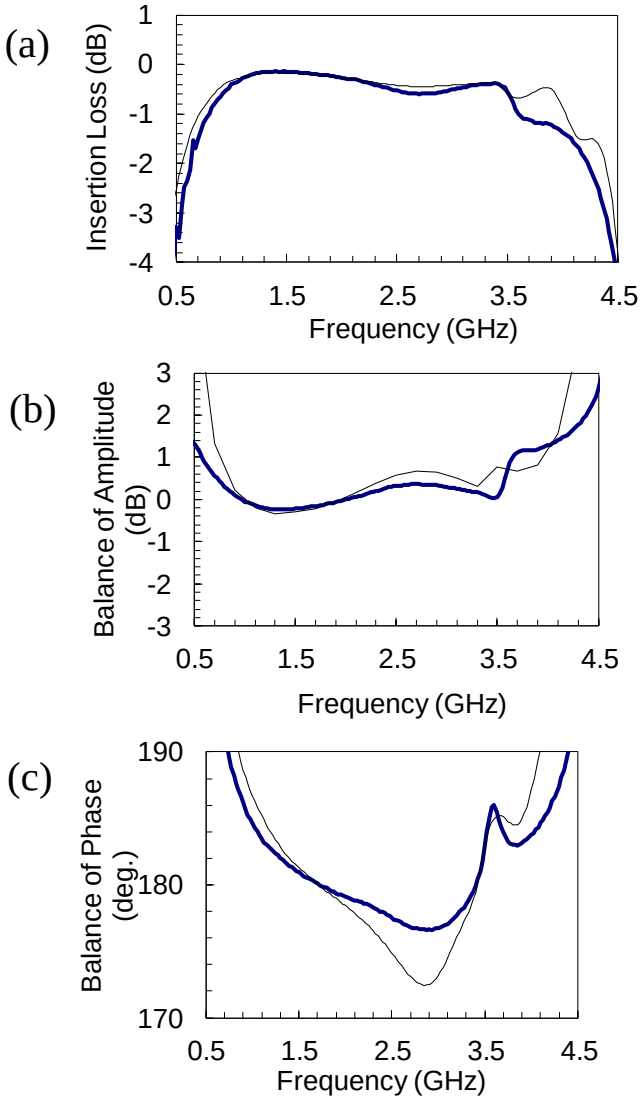


Fig. 2.7 Performance of the developed microstrip balun and comparison with the EM simulation results.

Thick line: measured, thin line: simulated. (a) Insertion loss, (b) balance of magnitude, and (c) balance of phase

Figure 2.8 shows the comparison of the measurement results of the coaxial balun and the microstrip balun against the frequency-dependence of the pass characteristics. The coaxial-line balun shown in Fig. 2.3 was fabricated and evaluated on the Teflon board using the SMA coaxial line (ε_r = 2.3, 50 Ω, l = 35 mm). It is confirmed that the proposed microstrip balun can obtain the broadband low-loss characteristics with the balance compared to the coaxial balun.

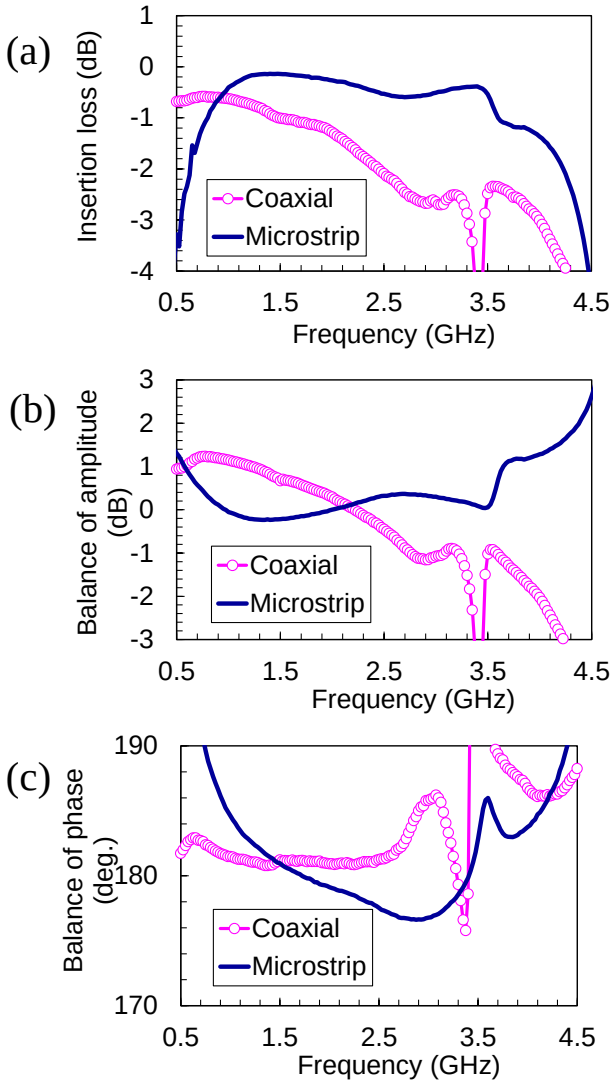


Fig. 2.8 Comparison of the coaxial balun and the microstrip balun against the frequency-dependence of the pass characteristics. (a) Insertion loss, (b) balance of magnitude, and (c) balance of phase

2.4 L/S-band 140-W push-pull amplifier

2.4.1 Device structure

The power AlGaAs/GaAs HFETs with 1.0-μm WSi gate fabricated in a recessed structure was employed for high power amplifiers [2.11]. A schematic cross-section of the fabricated HFET is shown in Fig. 2.9. The thickness and concentration of the Si-doped n-type AlGaAs Schottky layer and the Si-doped n-type GaAs channel layer were designed to achieve an optimal maximum drain current (I_{max}) and gate breakdown voltage (BV_{gd}). Since an HFET has higher Schottky barrier height than a GaAs MESFET, an improved BV_{gd} with

reduced gate leakage current which is of principal importance for high-power applications can be achieved. In such case of high-power FET, power dissipation remarkably increases so that the device thermal destruction occurs by the increase of channel temperature and thermal run-away promoted by gate leakage current [2.12]. Adopting the heatproof WSi gate AlGaAs/GaAs HFET that has higher Schottky barrier can greatly reduce gate leakage current under operation and prevent the thermal runaway. Furthermore, the HFET structure is inherently suitable for precise recess-depth control because of the selective dry-etching capability between AlGaAs and GaAs, resulting in good uniformity and high yield. Typical I_{dss}, I_{max}, transconductance, threshold voltage, and BV_{gd} value are 280 mA/mm, 380 mA/mm, 120 mS/mm, −2.5 V and 30 V, respectively. The breakdown voltage is enough to operate under the drain bias voltage of 12 V. The comparison of AlGaAs/GaAs HFET DC characteristic to GaAs MESFET [2.13] is shown in Table 2.1.

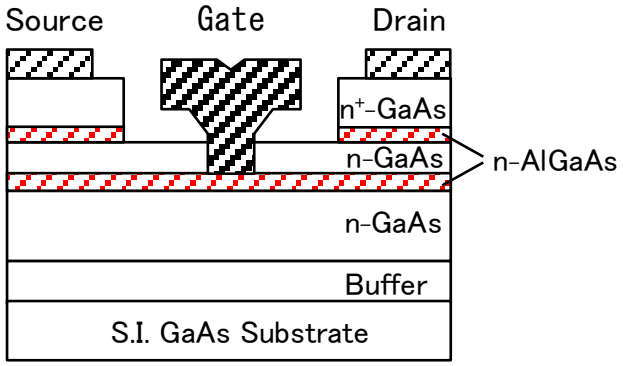


Fig. 2.9 Schematic cross-sectional view of the developed HFET.

Table 2.1 Comparison of AlGaAs/GaAs HFET DC characteristic to GaAs MESFET.

	Idss (mA/mm)	Imax (mA/mm)	gmmax (mS/mm)	Vt (V)	BVgd (V)	ΦB (eV)	Igd (μA/mm)*
HFET	280	380	120	-2.5	30	0.9	0.1
MESFET	200	340	120	-2.0	25	0.6	1

* @12V, 3%Idss

The amplifier composition to combine the output power of four chips with the 82-mm total gate-width of each chip was chosen in order to obtain more than 100-W-output power level. The gate-pitch (Gp) and finger-width (W_u) of FET chip were optimized considering a trade-off between the thermal resistance and the RF linear gain of the device. It is effective to widen the gate-pitch in order to reduce the thermal resistance of FET chip. However, the finger-width must be simultaneously lengthened because of the chip-width limitation. The longer finger-width tends to cause more degradation in the linear gain of the amplifier. The gate-pitch dependence of the thermal resistance for 82 mm total gate-width HFET chip is

shown in Fig. 2.10. From the measurement results, the gate-pitch and the finger-width were determined to be 25 μm and 560 μm, respectively. Moreover, the GaAs substrate was thinned to 40 μm and a gold plated-heat-sink (PHS) with 50 μm was formed on the backside of the substrate. Air-bridges and via-holes were used to reduce the parasitic capacitance and inductance. They are also performed as the thermal path. These four chips were assembled in a hermetic sealed package. For the package base metal, the Cu based mixed materials were adopted in order to obtain both suitable thermal conductance and thermal expansion similar to GaAs. They influence the device long-term reliability. As a result, a low thermal resistance of 1.4 °C/W for an FET chip with a total gate-width of 82 mm was obtained. It is a small value enough to obtain more than 100-W stable operation with four chips. A photograph of the completed HFET chip is shown in Fig. 2.11. The chip size is 1.3×4 mm^2.

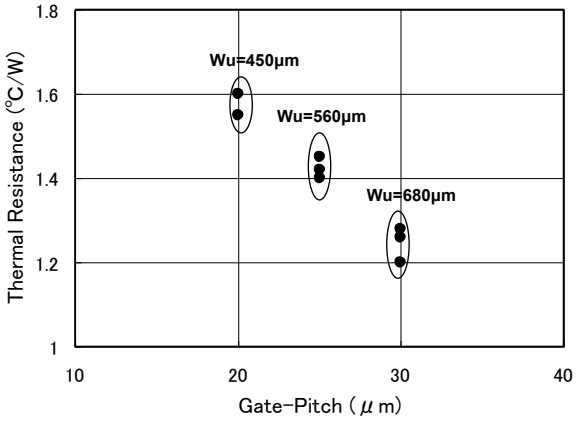


Fig. 2.10 Gate-pitch dependence of the thermal resistance for 82 mm HFET chip.

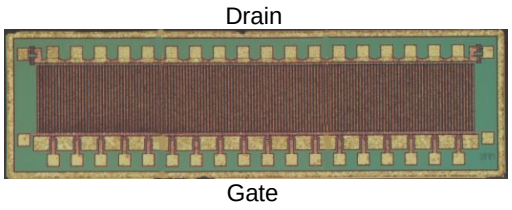


Fig. 2.11 Photograph of HFET chip (total gate width = 82 mm, chip size = 1.3×4mm^2.

2.4.2 Circuit design

A top view of the internally matched device is shown in Fig. 2.12. Two pairs of pre-matched HFET chips (W_g = 4×82 mm) are assembled with partially impedance transforming circuits in a single package. The package size is 17×34mm^2. The typical thermal resistance of the overall device was 0.8 °C/W which was measured by delta-V_{GS} method. It is a small value enough to operate this device in a digital cellular base station application. The internal input

matching circuit consists of a two-stage *LC* low pass filter network, where the bonding wire and chip capacitors act as inductors and capacitors. The internal output matching circuit consists of a transmission line on an alumina substrate (εr = 9.6) and an *LC* low-pass filter network. The input and output circuit elements were designed to transform optimum source impedance (0.2 + j0.3 Ω) and load impedance (0.4 + j0.15 Ω), estimated by a large-signal model simulation, to around 25 Ω of the balun-port impedance as well as to minimize the matching circuits loss at the fundamental frequency (= 2.2 GHz). The HP's nonlinear model (EEFET3) was employed for circuit simulation and optimization.

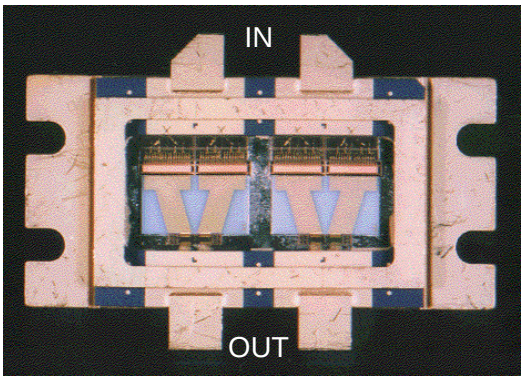


Fig. 2.12 Top view of the internally matched device. (package size = 17×34mm^2).

The developed push-pull amplifier is shown in Fig. 2.13. The amplifier was matched to 50 Ω at the input and output ports with the balun transformer, impedance matching capacitors and transmission lines on a plastic substrate. To avoid unwanted oscillation, the out-of-band damping circuit composed of a resistor and quarter-wavelength short stub circuit was placed close to the input ports of the device. This circuit can also provide gate bias. By connecting a resistor of 4.7 Ω between the principal transmission line and the quarter-wavelength shunted short stub circuit, the K-factor at a low frequency of the amplifier was able to be improved without degrading the in-band RF performance.

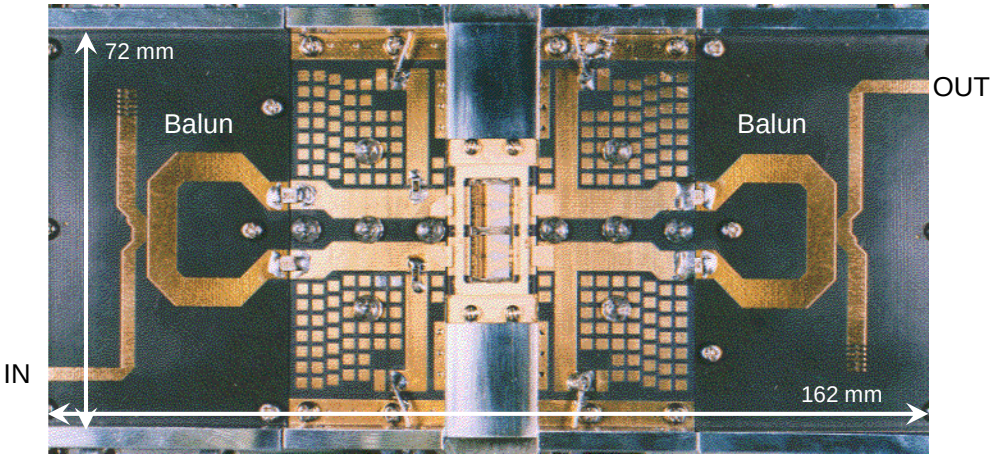


Fig. 2.13 Photograph of the developed push-pull amplifier.

2.4.3 RF performance

Measured output power and power-added efficiency versus input power are shown in Fig. 2.14. The developed L/S-band push-pull GaAs HFET power amplifier exhibited a saturation output power of 50.5 dBm (112 W) with a linear gain of 11.5 dB and a power-added efficiency of 46% at 2.2 GHz (at a drain-source voltage (V_{ds}) of 10 V, a quiescent drain-source current (I_{dq}) of 6 A). At V_{ds} = 12 V, the amplifier demonstrated 51.5-dBm (140-W) output-power with 42% power-added efficiency. To author's knowledge [2.14], [2.15], [2.16], these results were the best output-power performance reported in those days using GaAs FET technology.

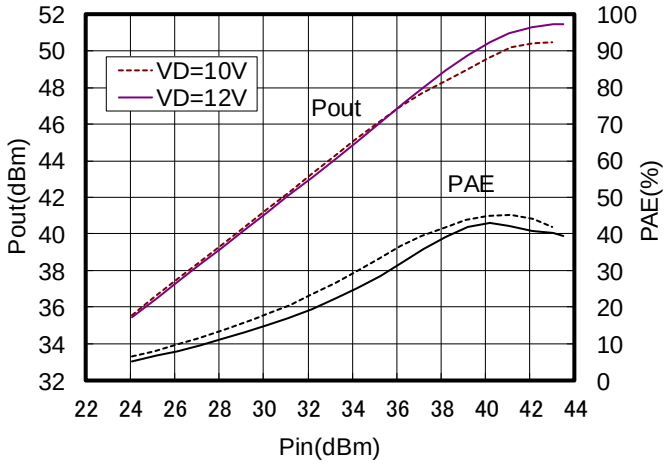


Fig. 2.14 Output power and power-added efficiency versus input power at 2.2GHz, Idq=6A.

The third order intermodulation distortion (IMD3) versus total output power at two tones (2.2 GHz, 2.201 GHz) is shown in Fig. 2.15. By re-tuning the device for optimized linearity with respect to the external circuit, the amplifier exhibited low intermodulation distortion (IMD) characteristics of less than −30 dBc at two-tone total output-power of 45 dBm. At 12 V, the amplifier exhibited low IMD3 of less than −30 dBc at two-tone total output-power of 46 dBm. In addition, the I_{dq} dependence of IMD3 versus two-tone total output power at 12 V is shown in Fig. 2.16. In particular, when the bias condition is below 2 A which corresponds to about 1.5% of I_{dss}, the developed push-pull amplifier showed low IMD3 of less than −32 dBc up to around two-tone total output power of 46 dBm. Figure 2.17 shows the frequency response of output power at a various input power. The amplifier featured the flat bandwidth of more than 60 MHz.

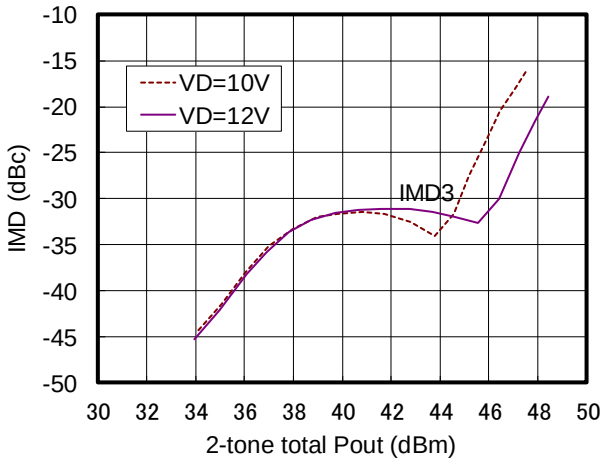


Fig. 2.15 IMD3 versus two-tone total output power at 2.2GHz + 2.201GHz, *I*dq=6A.

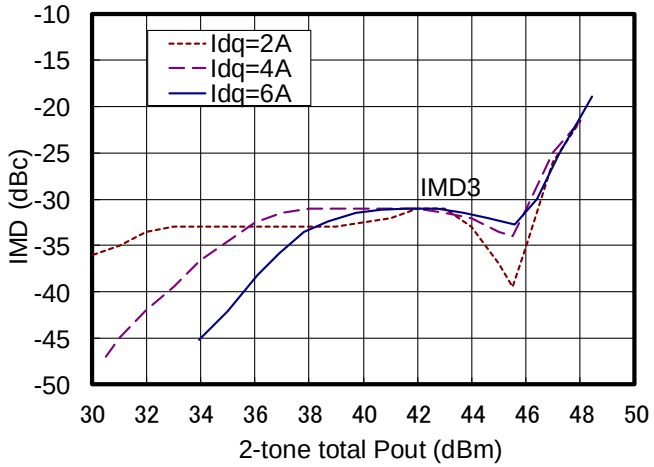


Fig. 2.16 *I*dq dependence of IMD3 versus two-tone total output power at 12V, 2.2 + 2.201GHz.

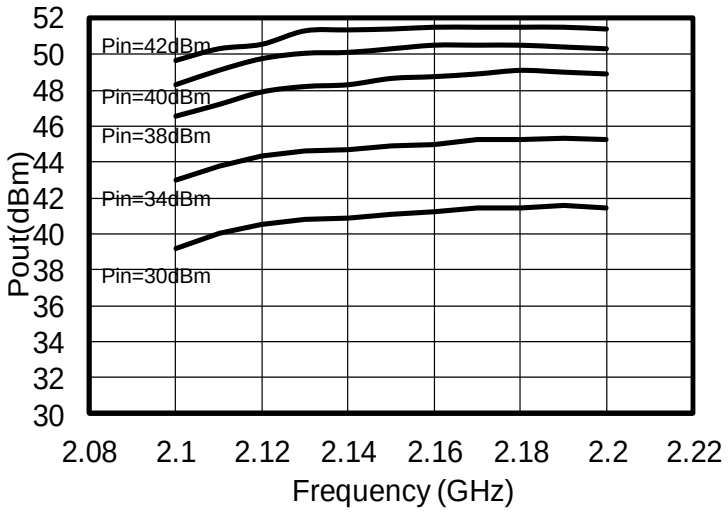


Fig. 2.17 Frequency response of output power at a various input power level, Idq=6A.

2.5 Stability analysis using large signal *S*-probe method

Here is explained about the stability analysis employing the large signal *S*-probe method.

Figure 2.18 shows the *S*-probe circuit [2.17]. The very low resistance (typically, 100 μΩ) is inserted in series to the signal transmission line, and the voltage excitation is performed from the both ends of the resistor through the very high resistance (typically, 10 MΩ). Thus, by using the *S*-probe method, the impedance and the reflection coefficient measured from the circuit side can be determined without affecting the entire circuit by probing the very small potential difference generated at the both ends of the low resistance element by the current flowing into the circuit side (see Appendix A). In order to determine the loop gain which exists in the amplifier at the small signal operation, the *S*-probe is inserted in the input/output terminals of a unit-FET of power FETs operating in parallel as shown in Fig. 2.19, and the reflection coefficient is calculated using the small signal circuit analysis. If the loop gain S_1 of the input side excitation and the loop gain S_2 of the output side excitation are less than one as follows (2.3), it is determined to be stable.

$$\begin{aligned} &\mathrm{Re}\{S_1 = \Gamma_s \Gamma_{in}\} < 1 \\ &\mathrm{Re}\{S_2 = \Gamma_l \Gamma_{out}\} < 1 \end{aligned} \tag{2.3}$$

where Γ_s is the reflection coefficient of the input matching circuit side connected to the unit-FET, Γ_{in} is the input reflection coefficient of the unit FET, Γ_l is the reflection coefficient of the output matching circuit side, and Γ_{out} is the output reflection coefficient of the unit FET.

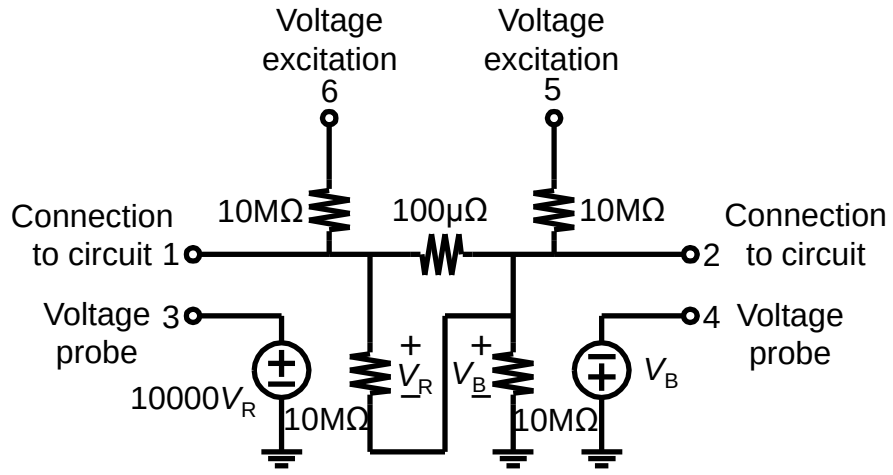


Fig. 2.18 *S*-probe circuit.

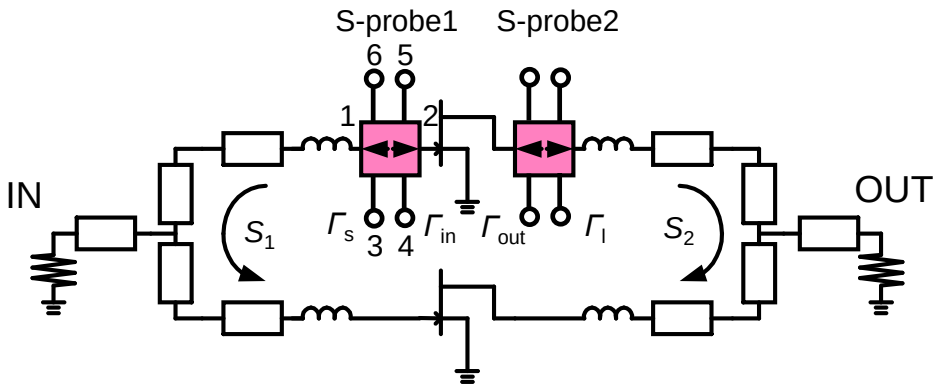


Fig. 2.19 Loop oscillation small signal analysis using *S*-probe.

To distinguish whether the amplifier is stable against the odd-mode operation when inputting the large signal, it is necessary to find the loop gain which exists in the amplifier at the large signal operation. The *S*-probe circuit is inserted in the input/output terminals of the unit-FET of the power FETs operating in parallel as shown in Fig. 2.20, and the reflection coefficient is calculated employing the two-tone harmonic balance simulation. The procedure obtaining the frequency characteristic of the loop gain at the large signal operation by using the two-tone harmonic balance simulation is shown below.

- The amplifier is biased, and is made the operating state to be analyzed inputting the fundamental frequency of f_0 at a certain power-level from the signal source.
- When determining the reflection coefficient Γ_s of the input matching circuit side connected to the unit FET, the small side-band signal of f_1 is inputted sweeping the frequency with the sufficiently lower power-level (for example, less than −40 dB) than the fundamental input signal from the voltage excitation port 5 of the *S*-probe circuit.
- Then, the Γ_s can be found from the f_1 component of the voltage V_3 and V_4 which appears in the voltage probe ports 3 and 4 as follows (2.4).

$$\Gamma_s(f_1) = \frac{\{-\frac{V_4(f_1)}{V_3(f_1)}\} - Z_0}{\{-\frac{V_4(f_1)}{V_3(f_1)}\} + Z_0} \tag{2.4}$$

- Similarly, when determining the input reflection coefficient Γ_{in} of the unit FET, the small side-band signal of f_1 is inputted sweeping the frequency with the sufficiently lower power-level than the fundamental input signal from the voltage excitation port 6 of the *S*-probe circuit.

- Then, the Γ_{in} can be found from the f_1 component of the voltage V_3 and V_4 which appears in the voltage probe ports 3 and 4 as follows (2.5).

$$\Gamma_{in}(f_1) = \frac{\{\frac{V_4(f_1)}{V_3(f_1)}\} - Z_0}{\{\frac{V_4(f_1)}{V_3(f_1)}\} + Z_0} \tag{2.5}$$

- In exactly the same way, the reflection coefficient Γ_{l} of the output matching circuit side and the output reflection coefficient Γ_{out} of the unit FET can be found by determining the fundamental voltage component of the side-band signal at the voltage probe ports of the *S*-probe inserted in the output side of the unit-FET.
- The condition that the loop oscillation at the large signal operation occurs is the following equation (2.6).

$$\begin{aligned} &\text{Re}\{S1 = \Gamma_s \Gamma_{in}\} > 1, \textit{and}\ \text{Im}\{S_1 = \Gamma_s \Gamma_{in}\} = 0 \\ &\text{Re}\{S2 = \Gamma_l \Gamma_{out}\} > 1, \textit{and}\ \text{Im}\{S_2 = \Gamma_l \Gamma_{out}\} = 0 \end{aligned} \tag{2.6}$$

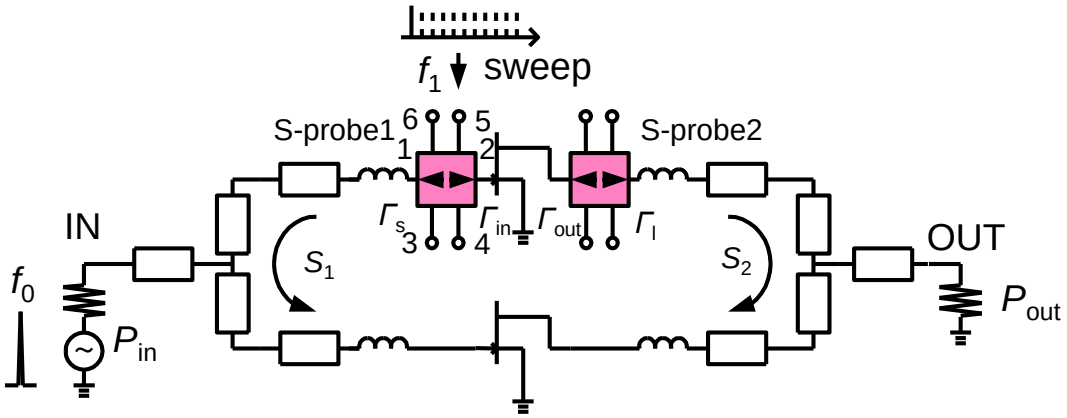


Fig. 2.20 Loop oscillation analysis at large signal operation using *S*-probe.

2.6 Oscillation analysis at large signal operation in C-band 60-W AlGaAs/GaAs HFET

To confirm the effectiveness of the newly proposed large signal *S*-probe method, this technique was applied to the oscillation analysis at the large signal operation in the C-band 60-W AlGaAs/GaAs HFET.

Figure 2.21 and 2.22 show the circuit configuration and the photograph of internally-matched C-band 60-W AlGaAs/GaAs HFET used for the examination of this analysis technique. The amplifier combines the four chips with the total gate-width of 35 × 4mm in the PKG including the input/output matching circuits. The input-and-output matching circuits are formed by patterning the metal film on the high dielectric constant substrates and the alumina substrates. The odd-mode oscillation can be completely suppressed at the DC bias connecting the pattern on the input and output matching circuits by the resistor of 10 Ω.

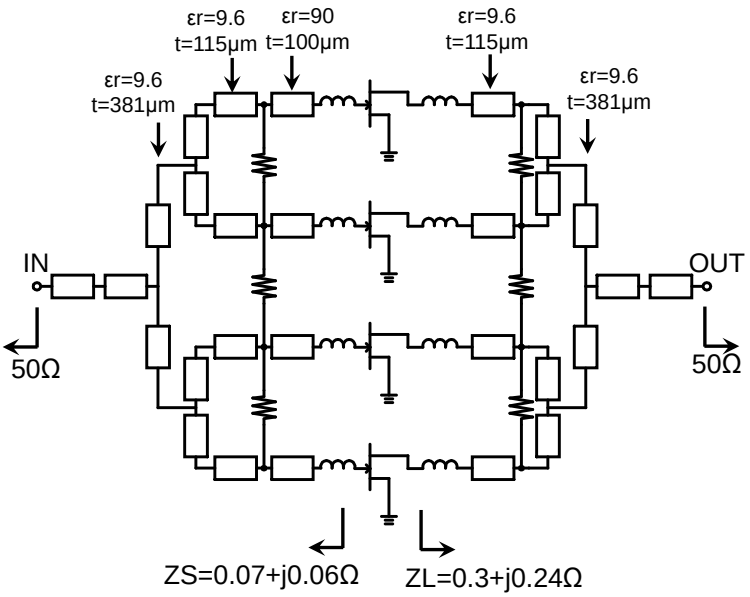


Fig. 2.21 Circuit configuration of internally-matched C-band 60-W AlGaAs/GaAs HFET.

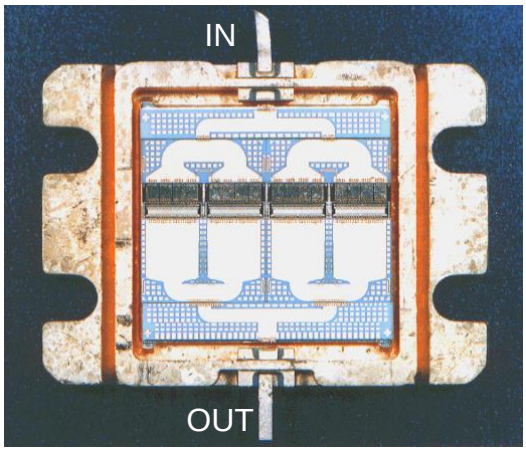


Fig. 2.22 Photograph of internally-matched C-band 60-W AlGaAs/GaAs HFET.

However, when the RF signal of 6.7 GHz was inputted, the gap from a straight-line occurred in a certain input power region (P_{in} = 30~40 dBm, region of B) of input-output characteristics as shown in Fig. 2.23. The output spectrum in the gap region from a straight-line is shown in Fig. 2.24. It is found that unnecessary spurious is generated besides the RF input frequency. It was identified that the observed output spectra are RF input frequency of

6.7 GHz and its harmonics, a fundamental oscillation spectrum of 6.5 GHz and its even harmonics, and their sum and difference frequency.

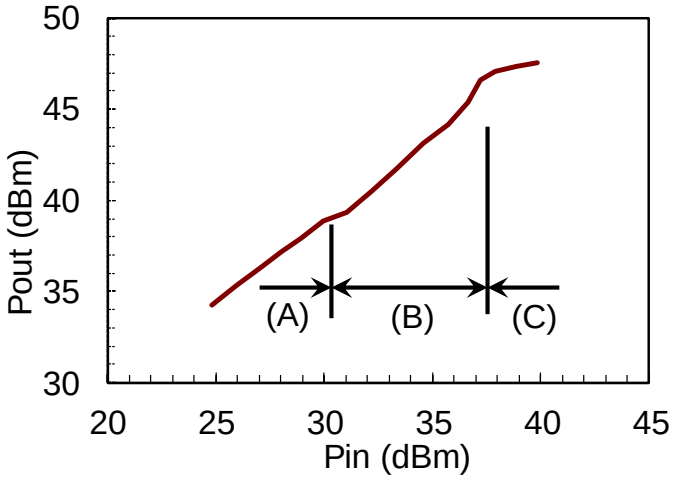


Fig. 2.23 P_{in} vs P_{out} of C-band 60-W AlGaAs/GaAs HFET.

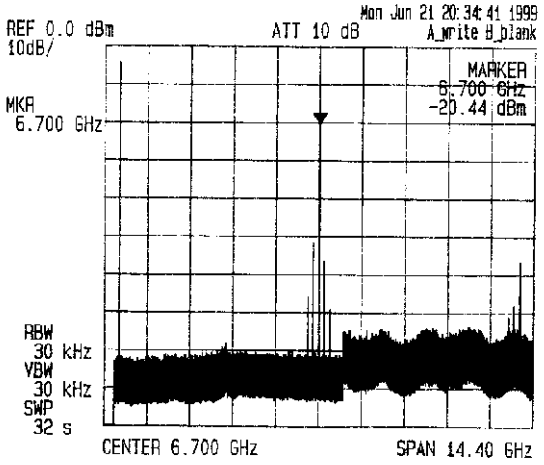


Fig. 2.24 Output spectrum in the discontinuity region.

As shown in Fig. 2.25, the large signal *S*-probe circuit was inserted in the input and output terminals of the one unit-FET in the amplifier combining the four chips in parallel, and the reflection coefficient in the input and output terminals of unit-FET at the large signal operation was calculated employing two-tone harmonic balance simulation. The loop gain at the large signal operation was calculated from these reflection coefficients. The balance resistances are connected to the input and output matching circuits. Since the *S*-probe circuit is non-invasive, all the closed loop gain can be determined at once by inserting in arbitrary circuit courses.

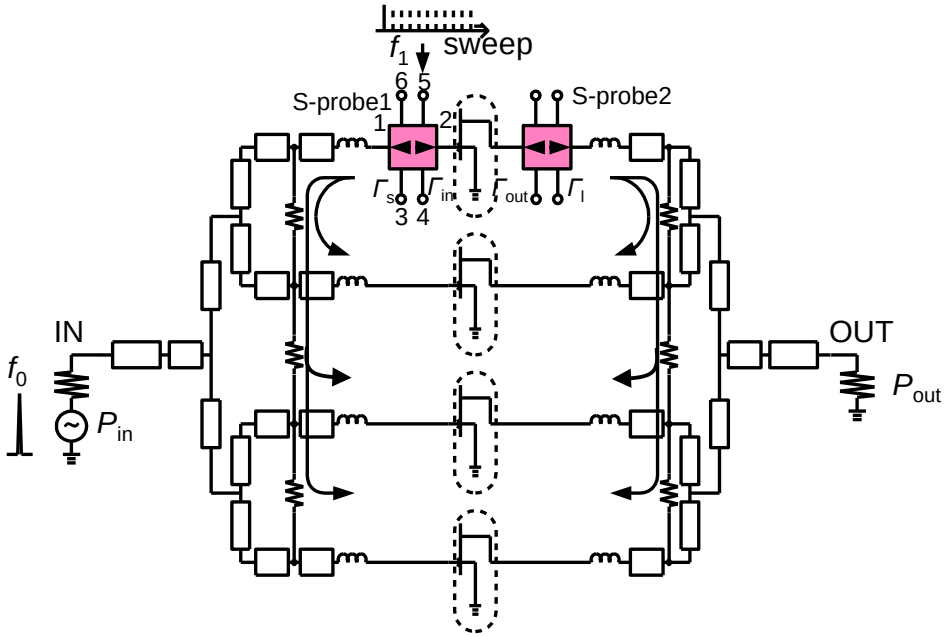


Fig. 2.25 Loop oscillation analysis at large signal operation using *S*-probe in C-band 60 W power FET.

Figure 2.26 shows the simulation results of the frequency characteristic of the loop gain at the large signal operation. The magnitude versus frequency characteristic, the phase versus frequency characteristic, and the Nyquist plot (*I*-*Q* plot) were shown at each input power level. The loop gain of the input side excitation is represented as $S_1 = \Gamma_s\Gamma_{in}$, and the loop gain of the output side excitation is represented as $S_2 = \Gamma_l\Gamma_{out}$.

In the small input power level of 20 dBm, since the balance resistances were connected between circuits, the magnitude of the loop gain of S_1 and S_2 did not become more than 1 in the frequency range from 0 to 11 GHz. Namely, the amplifier was stable against the odd-mode operation. In contrast, at the input power level of 35 dBm, the magnitude of the loop gain of S_1 and S_2 near 7.4 GHz became more than 1, and the phase became 0 degree. In addition, from the Nyquist plot, it was found to satisfy the oscillation condition at the 7.4 GHz. Therefore, when the input power level is 35 dBm, it can be said that the oscillation occurs at 7.4 GHz even in the state where the balance resistance is connected between circuits. Furthermore, when the input power level increased to 45 dBm, the magnitude of the loop gain of S_1 and S_2 became less than 1 from 0 to 11 GHz, and the amplifier became stable again.

A series of behavior obtained by the simulation reproduces comparatively the actual oscillation phenomenon at the large signal operation. Also, the fundamental oscillation frequency of the simulation is relatively close to the actual frequency.

From the above result, it can be said that the large signal loop gain analysis technique by the large signal *S*-Probe which combines the *S*-Probe circuit and the harmonic balance simulation is an effective means to the oscillation analysis at the large signal operation. Also,

the large signal loop oscillation condition became clear by this analysis. Furthermore, it showed the effect on the design of the balance resistance connected between the chips for the oscillation suppression, and it contributed to the stable operation of the amplifiers.

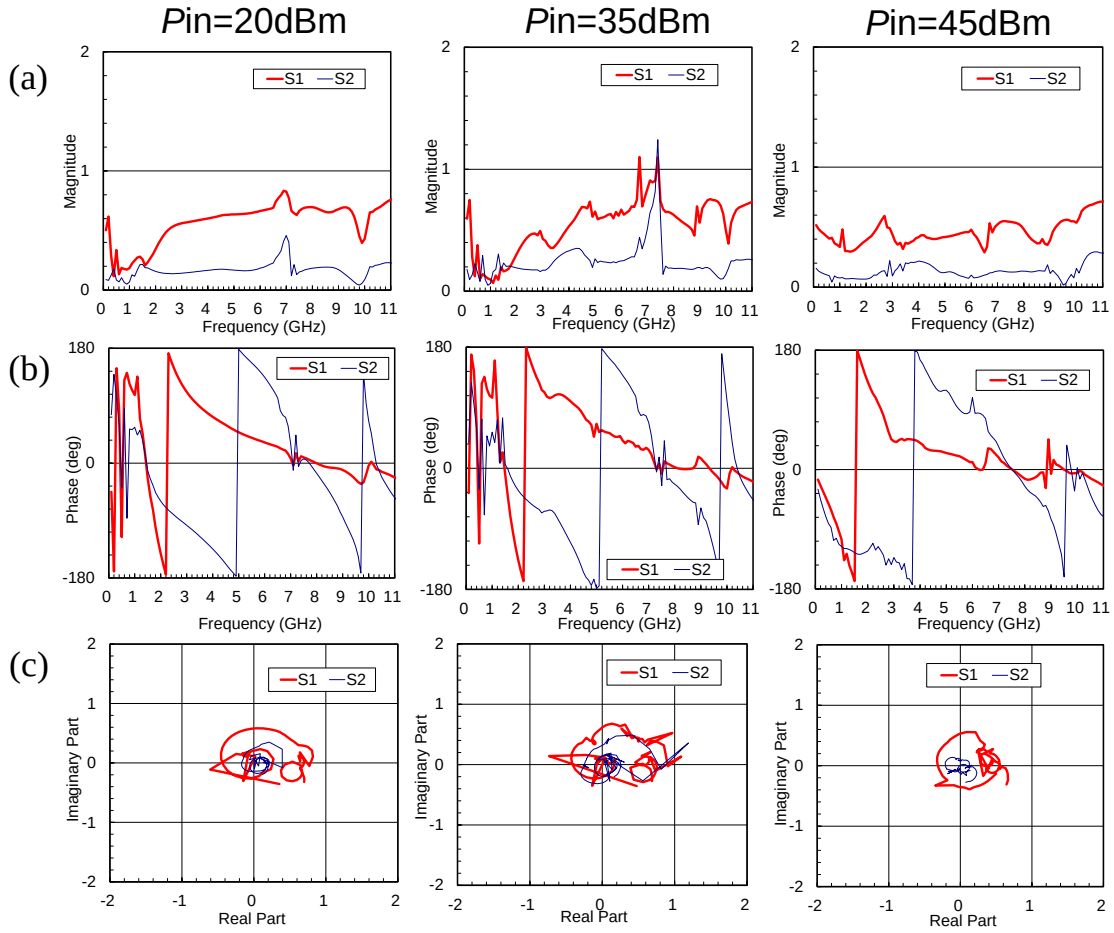


Fig. 2.26 Simulation results of the frequency characteristic of the loop gain at the large signal operation. (a) Magnitude versus frequency characteristic, (b) phase versus frequency characteristic, and (c) Nyquist plot (*I*-*Q* plot) are shown at each input power level.

2.7 Summary

In this chapter, the push-pull power combining circuit technique and the stability analysis technique under the large-signal operation for microwave high-power amplifiers have been developed. What has been demonstrated is as follows.

An L/S-band high-power and low-distortion AlGaAs/GaAs HFET push-pull amplifier has been developed using a low-loss microstrip balun.

At 2.2 GHz, an output power of 140 W has been obtained with 11.5-dB linear gain and 42% power-added efficiency. Under two-tone test conditions (2.2 GHz, 2.201 GHz), the

amplifier exhibited low intermodulation distortion characteristics of less than −30 dBc at two-tone total output-power of 46 dBm.

The developed HFET amplifiers are promising for improving RF power handling capability of digital cellular base station systems.

In order to determine the loop gain occurring in the FET and the circuit at the large signal operation, the large signal loop gain analysis technique that combines the *S*-Probe circuit and the harmonic balance simulation was proposed.

The proposed technique was applied to the oscillation analysis at the large-signal operation in the internally-matched C-band 60-W power-FET. The simulation result well reproduced the actual oscillation phenomenon, and the effectiveness of this analysis was confirmed.

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Chapter 3

High efficiency high-power amplifiers with second harmonic termination

3.1 Introduction

Chapter 3 describes the study on high efficiency microwave high power amplifiers. So far, many reports have been carried out about high efficiency operation classes such as Class-F [3.1], [3.2], [3.3]. However, in a 100-W-class high power amplifier, it often becomes difficult to realize these operations due to a lowering of the device impedance. There are not so many reports about the harmonic termination techniques of high power amplifiers.

In this study [3.4], the harmonic termination techniques in the matching circuits were examined to achieve high efficiency characteristics in high power amplifiers. The voltage waveforms were observed using a large signal simulation and Electro Optical Sampling (EOS), and the high efficiency termination condition of load second harmonic was found out to be open condition opposite to conventional Class-F. Moreover, by clarifying the effect of the termination condition of source second harmonic, it was confirmed that the nonlinear gate-to-source capacitance (C_{gs}) affects the overlap of the voltage and the current waveforms.

High output power transistors of over 200 W are strongly required to realize the size-reduction of a base station amplifier. Especially, the final stage transistors in the solid-state power amplifiers (SSPAs) used for W-CDMA base stations are demanded to provide both high efficiency and low distortion characteristics with high saturation output power. In order to improve the power-added efficiency, Class-B operation is commonly employed, although it sacrifices the distortion characteristics and linear gain. In a power amplifier, the third order intermodulation (IM3) is dominated by the third order transconductance coefficient ($gm_3 = d^3I_d/dV_g^3$) derived from a Volterra series expansion for the drain current. It was found

that FET with a steep *gm*-profile exhibits better symmetry and smaller value for gm_3 at low current bias point [3.5].

Furthermore, high voltage operation is one of the most desirable solutions to achieve high efficiency characteristics, because high load impedance due to high voltage operation can reduce power combining loss.

To realize low distortion and high gain characteristics at low current operation, a double-doped pseudomorphic heterojunction FET (HJFET) which gives both high gm and small gm_3 values was employed [3.6], [3.8]. In addition, for high voltage operation, a dual-field plate structure was adopted to HJFET [3.7]. Moreover, the design technique of the matching circuit with harmonic terminations was established. The second harmonic tuning for the input matching circuit as well as output matching circuit was employed to obtain the high efficiency characteristic [3.6].

3.2 High efficiency performance by harmonic termination

In Fig. 3.1, when the ωt which the drain current I_d becomes zero is set to θ, 2θ is the conduction angle. Then, the drain current of a rectified cosinusoid is given by the following formula (3.1) [3.9].

$$\begin{aligned} I_d &= I_0(\cos\omega t - \cos\theta) \qquad (-\theta < \omega t < \theta) \\ I_d &= 0 \qquad\qquad\qquad\quad (\omega t < -\theta,\ \ \theta < \omega t) \end{aligned} \tag{3.1}$$

The following formula (3.2) is obtained by Fourier series expansion.

$$I_d = \frac{I_0}{\pi}\left\{(\sin\theta - \theta\cos\theta) + (\theta - \sin\theta\cos\theta)\cos\omega t - \frac{1}{2}(\sin\theta - \frac{1}{3}\sin 3\theta)\cos 2\omega t - \cdots\right\} \tag{3.2}$$

From the DC component and the fundamental component, P_{dc}, P_{out}, and η_d can be found as follows (3.3), (3.4), (3.5).

$$P_{DC} = \frac{I_0 V_{ds}}{\pi}(\sin\theta - \theta\cos\theta) \tag{3.3}$$

$$P_{out} = \frac{I_0(V_{ds} - V_{knee})}{2\pi}(\theta - \sin\theta\cos\theta) \tag{3.4}$$

$$\eta_d = \frac{1}{2}\left(1 - \frac{V_{knee}}{V_{ds}}\right)\left(\frac{\theta - \sin\theta\cos\theta}{\sin\theta - \theta\cos\theta}\right) \tag{3.5}$$

By $\theta = \pi$ in Class-A, $\eta_d = 50\%$, by $\theta = \pi/2$ in Class-B, $\eta_d = 78.5\%$, and by $\theta = 0$ in Class-C, $\eta_d = 100\%$, but the output power in Class-C would become zero.

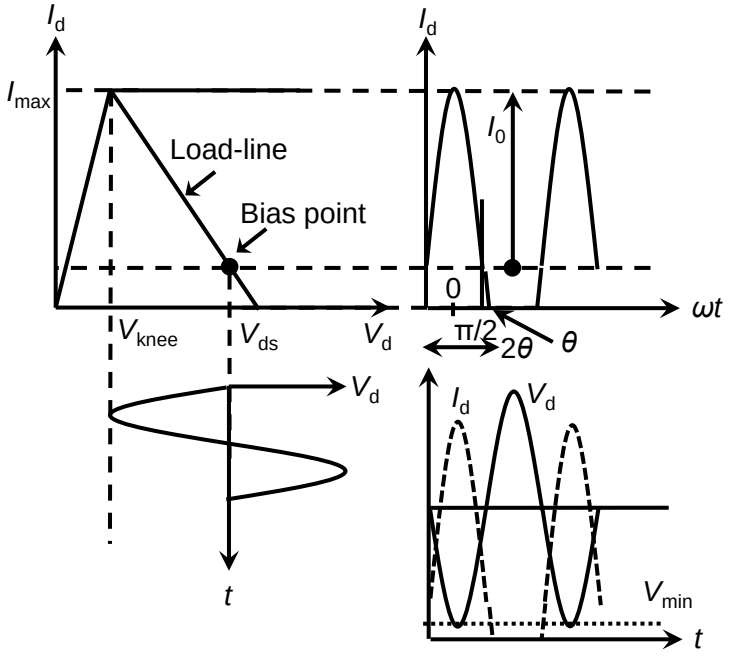


Fig. 3.1 Drain current and voltage waveform in amplifier operation.

The drain current waveform in Class B operation ($\theta = \pi/2$) serves as a half-wave rectification. The Fourier series expansion of the drain current of a half-wave rectified sinusoid is expressed as follows (3.6). It is found that there is only the even-harmonics except a direct-current component and a fundamental component.

$$I_d = \frac{I_{max}}{\pi}\left(1 + \frac{\pi}{2}\sin\omega t - \sum_{n=1}^{\infty}\frac{2}{4n^2 - 1}\cos 2n\omega t\right) \tag{3.6}$$

At this time, in Class-F operation [3.10], the drain voltage waveform is controlled to a square wave by load harmonic termination conditions ($Z_L(nf_0)$) provided at the drain-electrode of the transistors as shown in Fig. 3.2. The square drain voltage waveform is expressed by Fourier series expansion as follows (3.7). It is found that the even-harmonics are not included.

$$V_d = V_{ds} - \frac{4(V_{ds} - V_{knee})}{\pi}\sum_{n=1}^{\infty}\frac{1}{2n-1}\sin(2n-1)\omega t \tag{3.7}$$

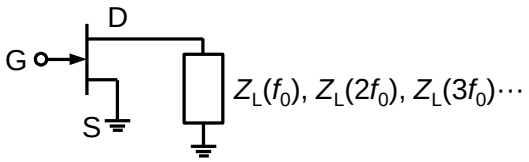


Fig. 3.2 Load harmonic termination conditions provided in transistor.

The harmonic termination conditions to realize Class-F operation become the following expressions (3.8), that is, even-harmonics are terminated at short condition, and odd-harmonics are terminated at open condition.

$$Z_L(nf_0) = \begin{cases} 0 & (n = even) \\ \infty & (n = odd) \end{cases} \tag{3.8}$$

In Class F operation, at the ideal FET ($V_{knee} = 0$), the overlap of the drain current waveform and the drain voltage waveform becomes zero as shown in Fig. 3.3, and the drain efficiency of 100% can be acquired.

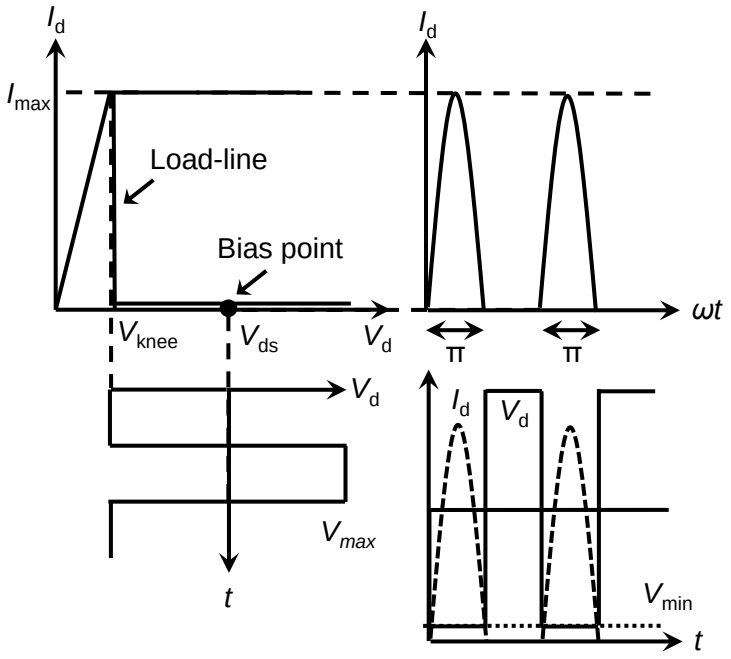


Fig. 3.3 Drain current and voltage waveform in Class-F operation.

The voltage waveform in inverse Class-F operation is replaced with the current waveform in Class-F operation. The Fourier series expansions of the drain current and the drain voltage in inverse Class-F operation are expressed as the following formulas (3.9), (3.10), respectively [3.2], [3.11].

$$I_d = \frac{I_{\max}}{2}\left(1+\frac{4}{\pi}\sum_{n=1}^{\infty}\frac{1}{2n-1}\sin(2n-1)\omega t\right) \tag{3.9}$$

$$V_d = V_{ds} + (V_{\max} - V_{knee})\left(\frac{1}{\pi} - \frac{1}{2}\sin\omega t + \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{1}{4n^2-1}\cos 2n\omega t\right) \tag{3.10}$$

In inverse Class F operation, the drain current waveform turns into a square wave and the drain voltage waveform becomes a half-wave rectification, as shown in Fig. 3.4. The harmonics termination conditions are the following formulas (3.11).

$$Z_L(nf_0) = \begin{cases} \infty & (n = even) \\ 0 & (n = odd) \end{cases} \tag{3.11}$$

In inverse Class-F operation, on ideal conditions of the V_{knee} of 0 V, the overlap of the current and the voltage waveform also disappears and the drain efficiency can be 100%. The characteristics of Class-F and inverse Class F operation are summarized in a Table 3.1. Here, R_{L} is the fundamental load impedance. In inverse Class F operation, it is featured that the maximum drain voltage amplitude becomes π/2 times as large as Class-F operation.

However, an actual FET includes the reactance components and the nonlinear components. Besides, in high-power FETs being low impedance, the terminations up-to second harmonics are realistic. Therefore, the optimization of second harmonic termination conditions was discussed in this study.

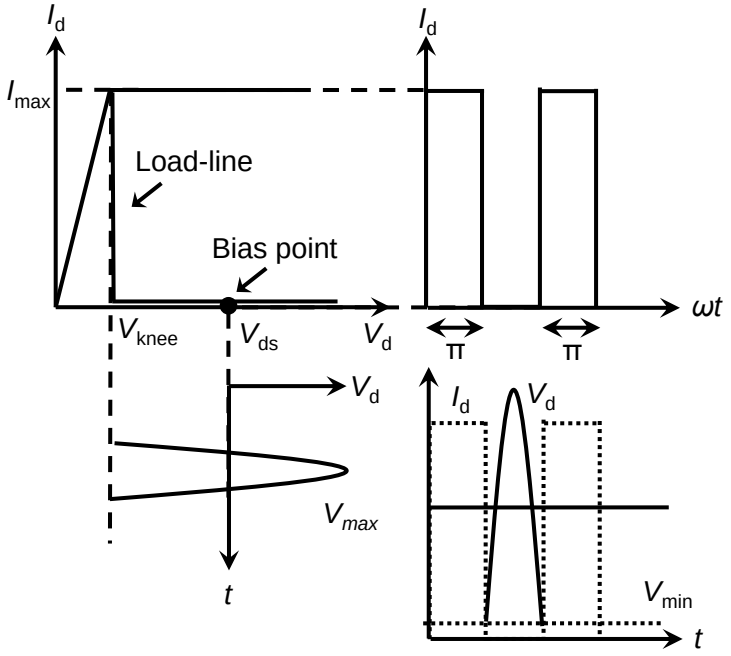


Fig. 3.4 Drain current and voltage waveform in inverse Class-F operation.

Table 3.1 Characteristics of Class-F and inverse Class F operation.

	Class-F	Inverse Class-F
P_{out}	$\frac{(V_{max}-V_{knee})}{2\pi} I_{max}$	$\frac{(V_{max}-V_{knee})}{2\pi} I_{max}$
η_d	$\frac{1}{1+\frac{2V_{knee}}{2V_{ds}-V_{knee}}}$	$\frac{1}{1+\frac{\pi V_{knee}}{\pi V_{ds}-V_{knee}}}$
R_L	$\frac{2V_{ds}}{I_{max}}$	$\frac{\pi V_{ds}}{I_{max}}$
V_{max}	$2V_{ds}$	πV_{ds}
Z_L (even)	0	∞
Z_L (odd)	∞	0

3.3 Design procedure of the matching circuit with harmonic termination in high-power FET

Since the large gate-width is needed to obtain higher output power in high-power FET, the input and output impedance greatly decreases compared to the system impedance of 50 Ω. Therefore, the impedance matching is performed providing the impedance matching circuits directly connected to the chips in a PKG. There is a problem that the matching circuits of high-power FET realize the fundamental frequency matching and the harmonic terminations with low loss. The matching circuit parameters are optimized so as to minimize the circuit return-loss measured from the system port when the port impedance of the transistor side is to be complex conjugate of the optimum load impedance for the transistor. Thereby, the transistor can operate on the optimum load condition.

Figure 3.5 shows the impedance-matching method scaling the optimum load impedance obtained in a unit-cell device to the *n*-cell device with an output of *n* times. What is necessary is to optimize the circuit parameters to minimize the return-loss measured from the system port after setting the complex conjugate of the optimum load impedance of one-cell to 1/*n*.

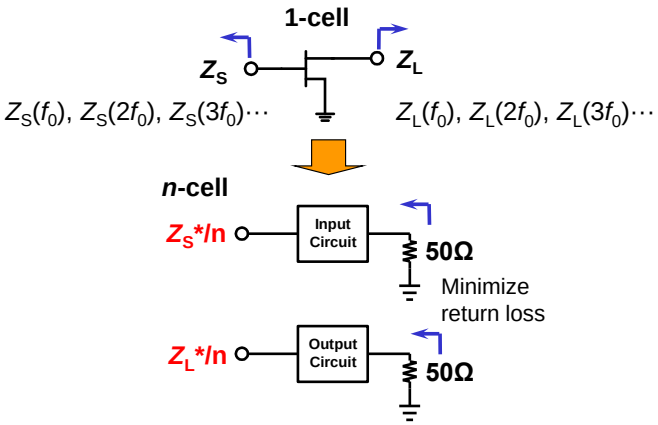


Fig. 3.5 Impedance-matching method scaling the optimum load impedance obtained in a unit-cell device to the *n*-cell device.

Generally, in high-power FET, it also becomes very difficult to perform the second harmonic termination because of the decrease and the phase-imbalance of the input/output impedance due to the large gate-width and the increase of chip-size. In order to realize the impedance-matching of both the fundamental and second harmonic, it is necessary to fix the setting of the second harmonic impedance in the internal matching networks (IMN) of the pre-matched push-pull FET. For example, when performing the second harmonic termination using lumped elements, the IMN must consist of the circuits more than at least two stages (having more than four parameters). In the power FET with the multi-cells, since *Q*-factor of the circuit element is low, it is difficult to acquire a sufficient reflection coefficient and phase condition against second harmonic.

In the IMN with the second harmonic termination applied to the push-pull FET amplifier of Fig. 3.6, the circuit parameters are determined to be matched to the desired impedance against the fundamental frequency and the second harmonic in the state of one side before combining with push-pull configuration. A circuit configuration when the output IMN was determined is shown in Fig. 3.7. The system port is connected to the impedance of 25 Ω at the balance port of the balun circuit, and transistor side port impedance is given the complex conjugate of the fundamental load impedance for maximizing efficiency and the reflection phase condition desired for second harmonic. In this circuit configuration, the circuit parameters of IMN are optimized so as to minimize the return loss measured from the system port at the fundamental and the second harmonic. After determining the circuit parameters of IMN, the external matching circuits and the balun circuit are connected to this, and the whole output-matching circuits are constituted as shown in Fig. 3.8. Finally, the circuit parameters of the external matching circuits are optimized so as to minimize the return loss measured from the system port against the fundamental frequency. In the same way, the

circuit parameters of the input IMN are optimized so as to obtain the desired impedance and the low circuit loss against the fundamental frequency and the second harmonic.

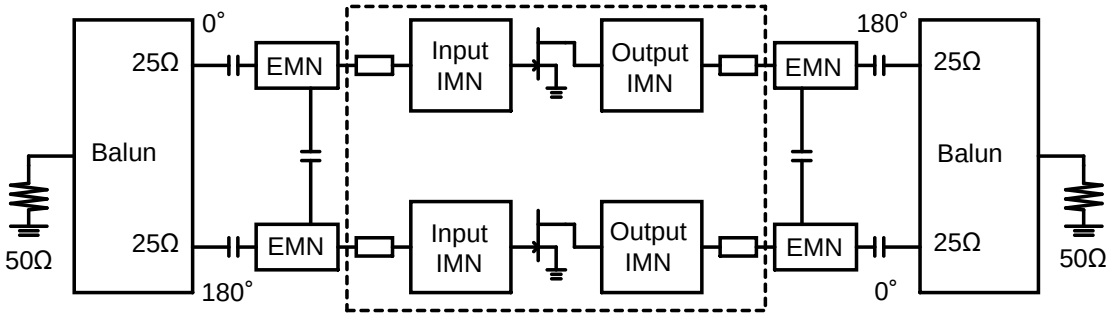


Fig. 3.6 Circuit configuration of push-pull FET amplifier.

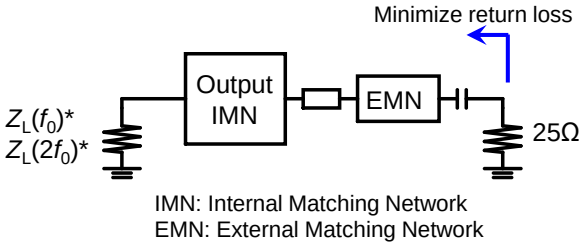


Fig. 3.7 Impedance-matching for the optimum load impedance at fundamental frequency and second harmonic.

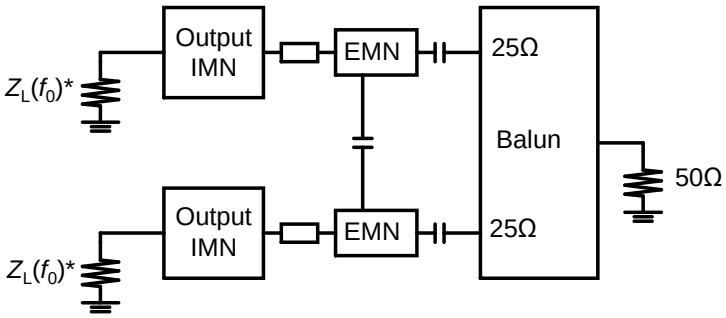


Fig. 3.8 Impedance-matching in a whole output-matching circuit.

3.4 Harmonic load-pull simulation

The influence of the second harmonic source impedance as well as the second harmonic load impedance on the power-added efficiency (PAE) was simulated using a large signal model (Agilent EEHEMT1 model) extracted for a unit cell device. Using a unit cell model with the gate-width of 4.2 mm, the second harmonic ($2f_0$ = 4.2 GHz) source-pull and load-pull simulation were performed while keeping the same fundamental (f_0 = 2.1 GHz) load condition for maximizing efficiency. Figure 3.9 shows the PAE contours at the 2-dB-gain compression operation point on the second harmonic load-pull simulation. The second-harmonic load impedance dependence on PAE indicated that the second harmonic impedance

for high efficiency should be open condition rather than short condition. This result is opposite to the Class-F terminal condition [3.10] on the second-harmonic load impedance. Figure 3.10 shows the PAE contours at 2-dB-gain compression operation point on the second harmonic source-pull simulation. A high efficiency was obtained at around short condition for the source impedance at the second harmonic. In addition to the load second harmonic impedance, the source second harmonic impedance plays an important role for high efficiency operation.

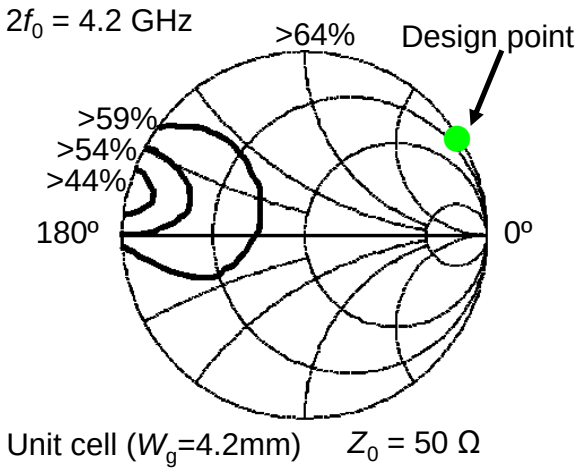


Fig. 3.9 PAE contours at the 2-dB-gain compression operation point on the second harmonic load-pull simulation.

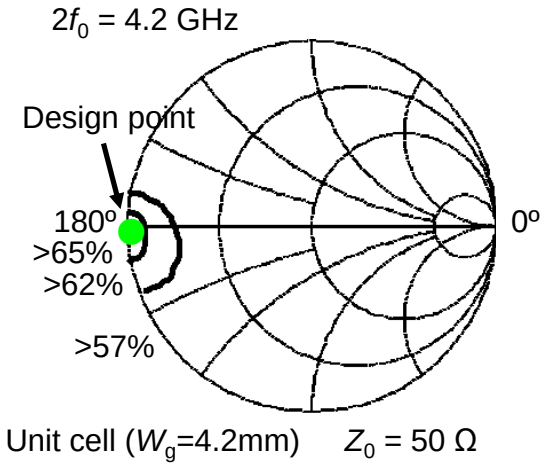


Fig. 3.10 PAE contours at the 2-dB-gain compression operation point on the second harmonic source-pull simulation.

The simplified equivalent circuit of an FET is shown in Fig. 3.11. In the second harmonic load-pull simulation of Fig. 3.9, it was found that the second harmonic load impedance where the efficiency decreases can be expressed by the following equation (3.12).

$$Z_L(2\omega_0) = \left(\frac{1}{j \cdot 2\omega_0 \cdot C_{ds}} \right)^* \tag{3.12}$$

where * denotes the complex conjugate and C_{ds} is the drain-to-source capacitance of the FET.

This is the condition that the second harmonic impedance at the A-plane of Fig. 3.11 diverges to infinity. Thus, the optimum load impedance of the second harmonic at the A'-plane is greatly affected by the C_{ds}. In an actual FET, due to the C_{ds}, the unsuitable load condition for high efficiency operation has approximated to short condition of second harmonic load impedance of Class-F condition.

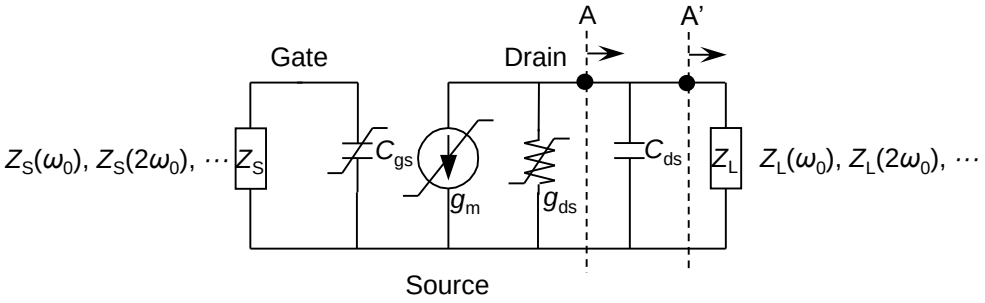


Fig. 3.11 Simplified equivalent circuit of FET.

Figure 3.12 shows the load second-harmonic impedance dependence on drain current and voltage waveforms. The case of open condition on load second harmonic impedance becomes the waveforms with large drain voltage amplitude and small drain current amplitude compared with the short condition on load second harmonic impedance. As the result, the load-line of open condition expands toward the plus V_{ds}. On the other hand, the load-line of short condition expands toward the I_{max}. As shown in the figure, the waveform of open condition is able to reduce the overlap of voltage and current rather than short condition. The difference of load-line results in PAE improvement.

From harmonic load-pull simulation, on the matching circuits, the second harmonic source impedance was designed to the short condition, and the second harmonic load impedance was designed to the open condition.

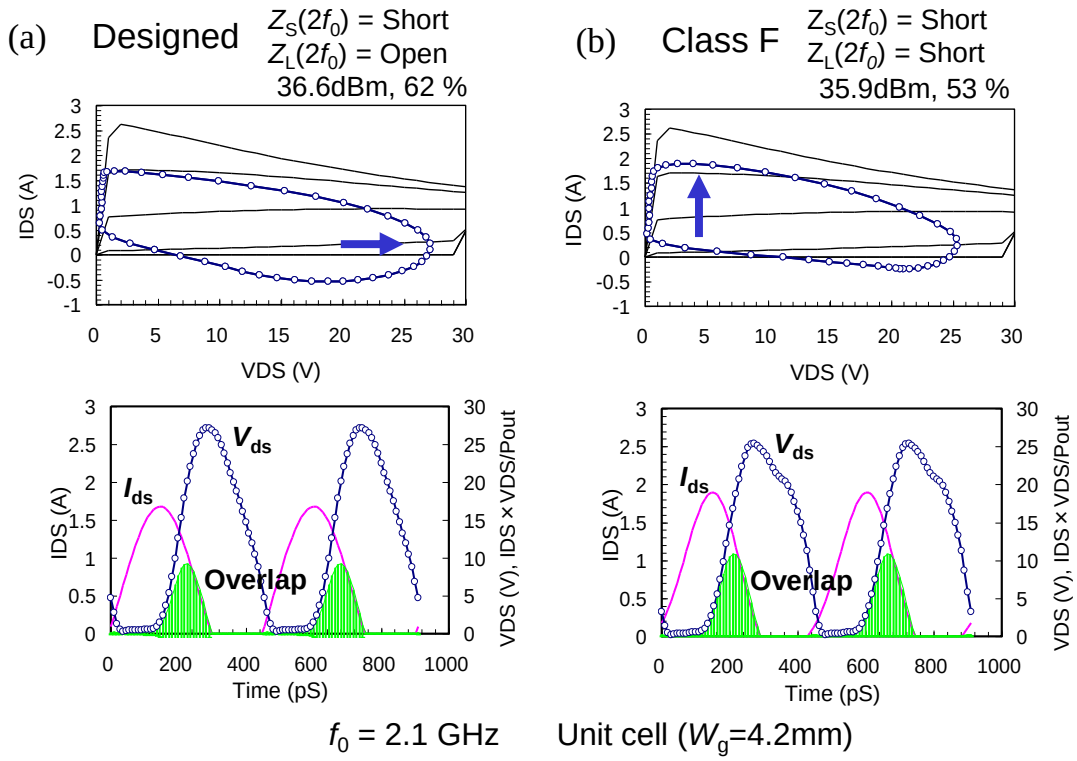


Fig. 3.12 Load second-harmonic impedance dependence on drain current and voltage waveforms. (a) Open condition and (b) short condition on load second harmonic impedance.

3.5 Voltage waveform observation by Electro-Optic Sampling

In order to confirm successful termination of the second-harmonic, the voltage waveforms on gate and drain electrodes by the contact-less EOS method [3.12] were measured. Figure 3.13 shows the principle of the contact-less EOS method. The pulsed laser synthesized to input RF-signal is applied to the nonlinear optical crystal of ZnTe putted near the measurement point of gate and drain pad. The electric-field generated from the electrode of FET changes the refractive index of ZnTe. Therefore, the voltage waveform of the electrode is sampled as the polarized spectrum of the laser applied to ZnTe.

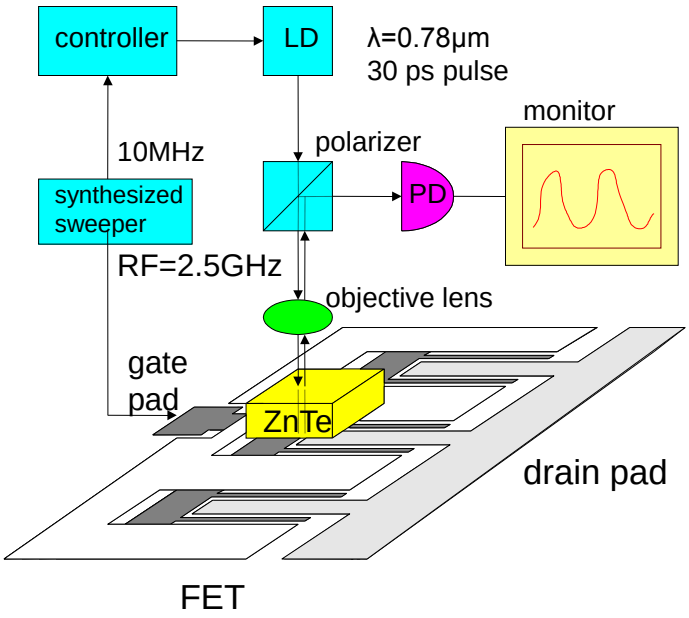


Fig. 3.13 Voltage waveform measurement by contact-less EOS method.

The three amplifiers terminated in different source and load second-harmonic impedances were investigated. Figure 3.14 shows the position of source and load second harmonic impedance for the three amplifiers.

type	$Z_S(2f_0)$ Z_0=50/32Ω	$Z_L(2f_0)$ Z_0=50/32Ω
(A)	0.01-j0.05(0.98∠186°) short	0.02-j0.1(0.96∠192°) short
(B)	0.01-j0.05(0.98∠186°) short	6.9+j22.3(0.97∠5.2°) open
(C)	0.01+j0.58(0.98∠119°) inductive	6.9+j22.3(0.97∠5.2°) open

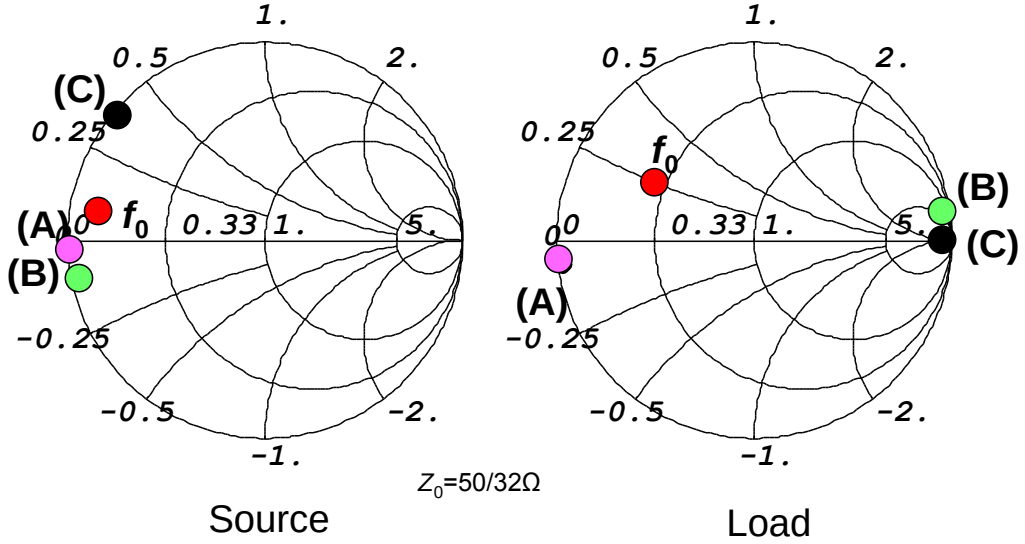


Fig. 3.14 Position of source and load second harmonic impedance for the three amplifiers.

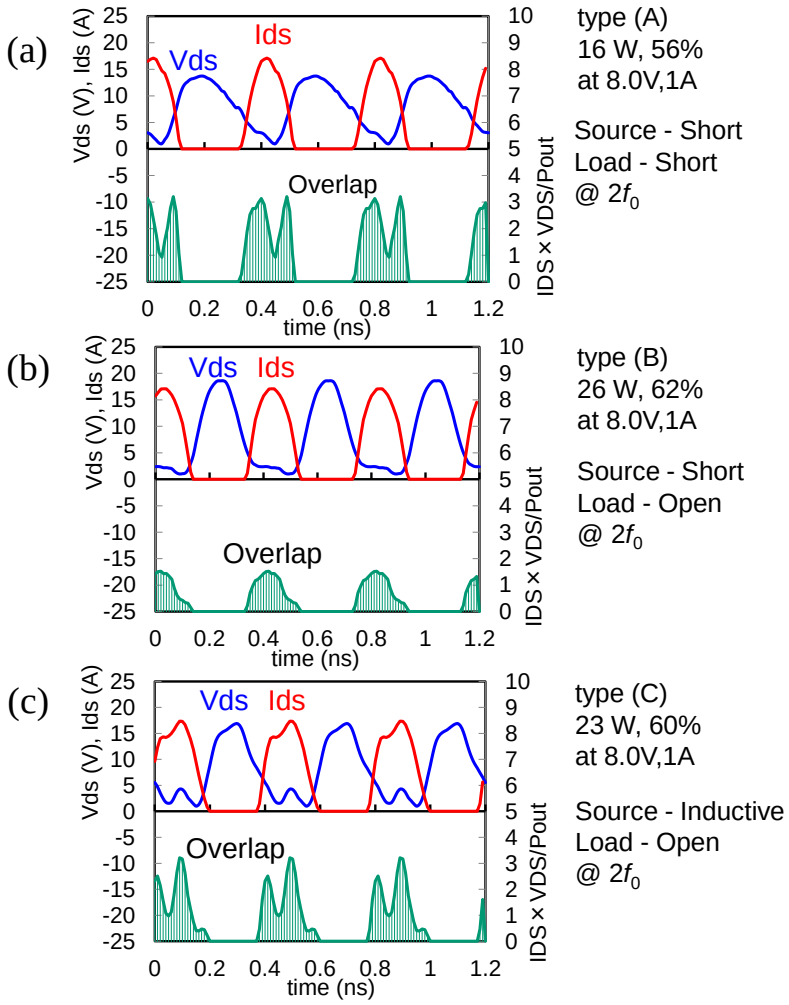


Fig. 3.15 Drain voltage and current waveforms at maximum efficiency operation measured by EOS for the three amplifiers terminated in different source and load second-harmonic impedances. (a) Type (A) with short-short, (b) type (B) with short-open, and (c) type (C) with inductive-open of second harmonic impedance.

Figure 3.15 shows drain voltage and current waveforms at maximum efficiency operation (P_{in} = 33 dBm) measured by EOS for the three amplifiers terminated in different source and load second-harmonic impedances. The amplifier type (A), in which both the source and load second-harmonic impedances are short, delivered P_{out} of 16 W with PAE of 56% at V_d = 8 V. The drain voltage observed by EOS seems to be a sawtooth waveform. In comparison, the drain voltage of the developed amplifier type (B), in which the source and load second-harmonic impedances are short and open respectively, was found to be a quasi-half wave rectification waveform. This quasi-half wave drain voltage with a flat portion at low V_d tends to reduce the overlap of drain-voltage and drain-current in the time domain. This reduction avoids power dissipation and results in PAE improvement. The drain current as shown here, was calculated by large signal model on the basis of the gate and drain voltage measured by EOS. Furthermore, comparing the voltage waveform of the amplifier type (C), in which the source and load second-harmonic impedances are inductive and open

respectively, with that of type (B), it is found that the drain voltage waveform depends significantly on the source second-harmonic phase condition. This indicates the requirement to optimize both the harmonic source and load terminations simultaneously.

Among amplifier types from (A) to (C), both the drain voltage and current waves of type (C) seem to be the closest to square waves. However, the second-harmonic ripple was observed in the waveform of drain voltage. The increase of voltage/current overlap due to the second-harmonic ripple caused power dissipation, and this resulted in type (C) having an efficiency slightly inferior to that of type (B). It was confirmed that the nonlinear gate-to-source capacitance (C_{gs}) affects the overlap of the voltage and the current waveforms. These results indicate that the developed amplifier type (B) was optimally terminated with respect to the second-harmonic frequency in both source and load matching circuits.

3.6 High efficiency 28-V-operation 320-W GaAs FP-FET amplifier

3.6.1 Device structure

A schematic cross-section of the developed 28-V-operation HJFET [3.7] is shown in Fig. 3.16. An AlGaAs/InGaAs/AlGaAs HJFET was fabricated using a selective dry etching process for the high threshold voltage (V_{th}) control and Au/WSi gate metallization technology for high reliability. To achieve high gain and low distortion characteristics, the epitaxial layers of double-doped double heterojunction were designed to have the steeper *gm*-profile and small gm_3 [3.5].

For high voltage operation, the dual field-modulating-plates (Dual-FP) technology in which one of the FP electrodes is connected to the gate (Gate-FP) and the other to the ground (Source-FP) was employed [3.8]. These FP electrodes contribute to obtain high break down voltage relaxing the electric field between gate and drain electrodes. The electric field relaxation due to the FP electrodes also results in decreasing the pulse drain current dispersion. In addition, the Source-FP improves the gain characteristics decreasing the gate-to-drain capacitance. The Source-FP length is 1.0 μm. The recess length between the gate and the recess edge in the drain side is 3.0 μm.

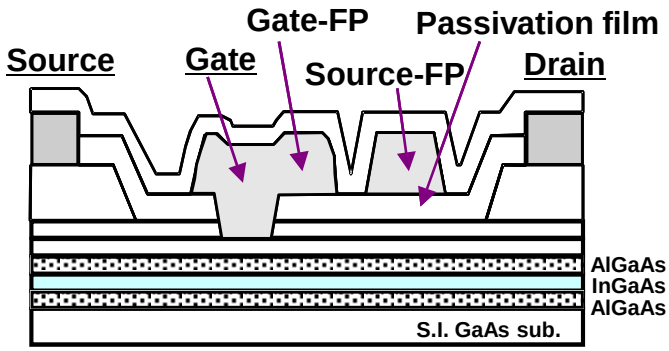


Fig. 3.16 Schematic cross-section of the developed 28-V-operation HJFET.

Figure 3.17 shows the photograph of a Dual-FP HJFET chip. The gate width (W_g) was 98 mm. The unit finger width (W_u) was 1000 μm. The chip size is 1.6 × 4.0 mm^2. The substrate was thinned to 40 μm and a gold plated-heat-sink of 15 μm thickness was formed on the backside of the substrate. Air-bridges and via-holes were used to reduce the parasitic capacitance and inductance. The FET exhibited a maximum drain current (I_{max}) of 260 mA/mm and a threshold voltage of −0.4 V. The transconductance (*gm*) was 180 mS/mm. The developed FET has enough breakdown voltage of 63 V for 28-V-operation.

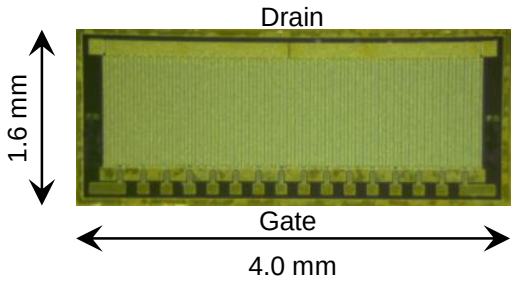


Fig. 3.17 Photograph of a Dual-FP HJFET chip.

3.6.2 Circuit design

Using the developed Dual-FP HJFETs, the L/S-band push-pull amplifier was designed. The overall developed amplifier circuit is shown in Fig. 3.18. Two pairs of GaAs HJFET chips (i.e. total $W_g = 4 \times 98$ mm) were mounted on a single package with pre-matching circuits. The FETs exhibited low thermal resistance of about 0.3 °C/W measured by the delta V_{gs} method. The output-power was combined in push-pull configuration with external balun circuits. The package size is 17 × 34 mm^2.

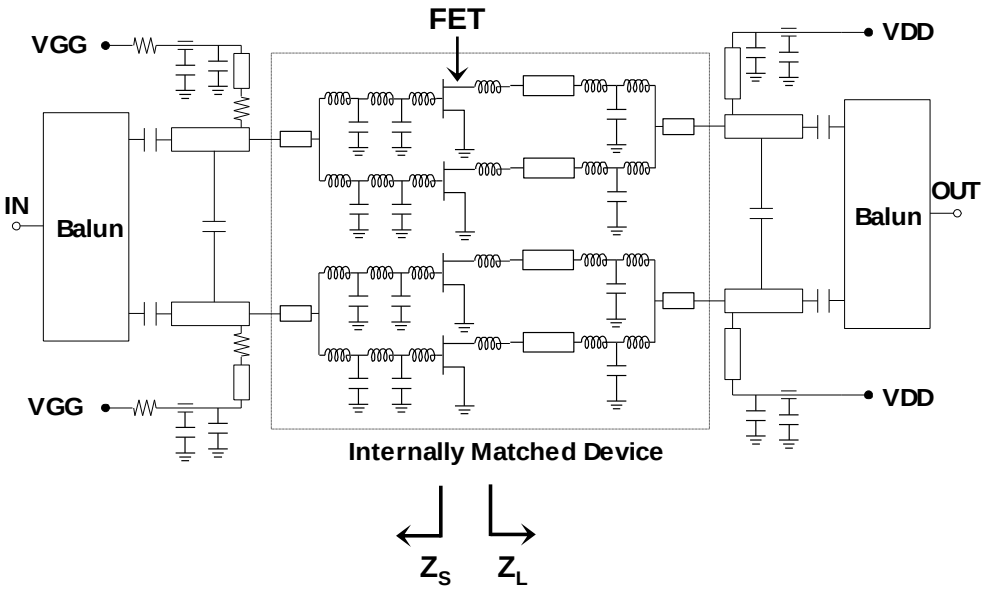


Fig. 3.18 Overall push-pull amplifier circuit.

Figure 3.19 shows the top view of the internally matched device. The internal input matching circuit consists of a two-stage *LC* low pass filter network in order to realize short condition for second harmonic source impedance. The internal output matching circuit consists of transmission lines and one-stage *LC* low pass filter networks in order to realize open condition for the second harmonic load impedance. The simulated input- and output-circuit impedance (Z_S, Z_L) locus in the frequency range from 10 MHz to 10.01 GHz is shown in Fig. 3.20. The normalized impedance is 50/32 Ω. The points and values of the impedance of the fundamental frequency (f_0), the second harmonic frequency ($2f_0$), and the third harmonic frequency ($3f_0$) are also indicated in Fig. 3.20.

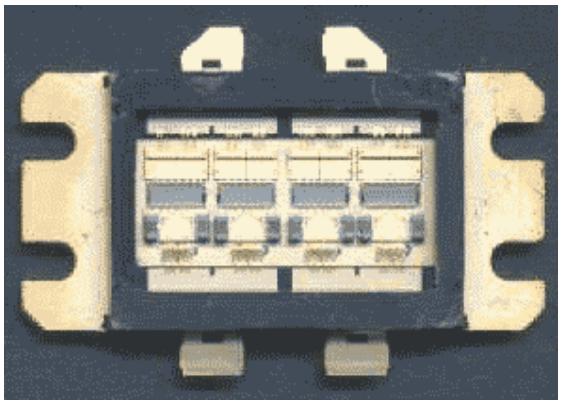
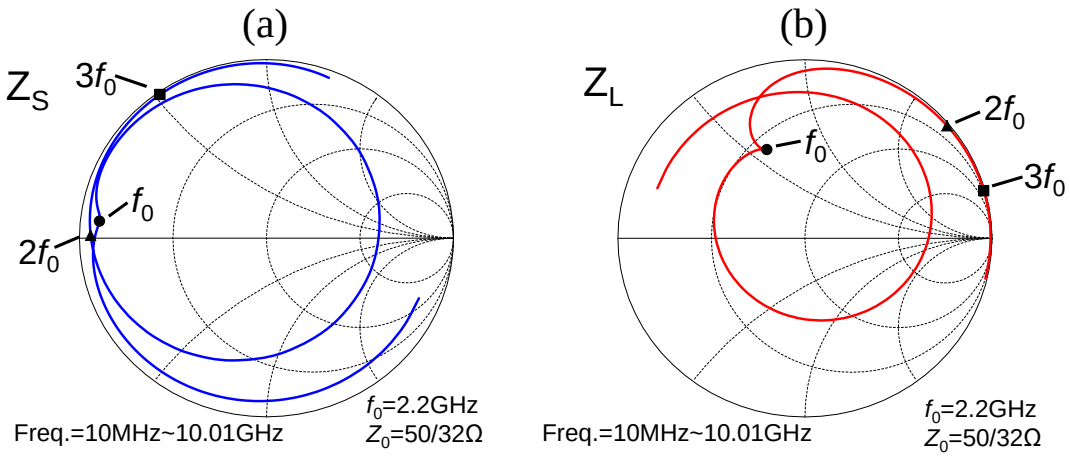


Fig. 3.19 Top view of the internally matched device.



	$Z_S(\Omega)$ Z_0=50/32Ω
f_0	0.05+j 0.05
$2f_0$	0.03+j 0.01
$3f_0$	0.01+j 0.52

	$Z_L(\Omega)$ Z_0=50/32Ω
f_0	0.42+j 0.59
$2f_0$	0.06+j 2.77
$3f_0$	0.20+j 7.34

Fig. 3.20 Simulated (a) input- and (b) output-circuit impedance (Z_S, Z_L) locus in the frequency range from 10 MHz to 10.01 GHz.

3.6.3 RF performance

Measured output power and efficiency versus input power under the CW condition is shown in Fig. 3.21. The developed amplifier exhibited a saturation output power (P_{sat}) of 55.1 dBm (320 W) with a linear gain (GL) of 14 dB and a drain efficiency (η_d) of 62% at 2.14 GHz (at V_{ds} = 28 V, quiescent drain-source current (I_{dsq}) = 1.5 A).

Figure 3.22 demonstrates the modulation signal output performance with two W-CDMA signals of the 15 MHz carrier spacing (2.1325 GHz, 2.1475 GHz). The W-CDMA signal condition is a 3-GPP test model 64ch with a clipping factor of 100%. The amplifier exhibited low IMD3 characteristics of −37 dBc and high η_d of 30% at an average P_{out} of 47.5 dBm (8-dB back-off). These RF results demonstrated the most excellent performance ever reported among GaAs and LDMOS FETs to author's knowledge [3.13], [3.14], [3.15].

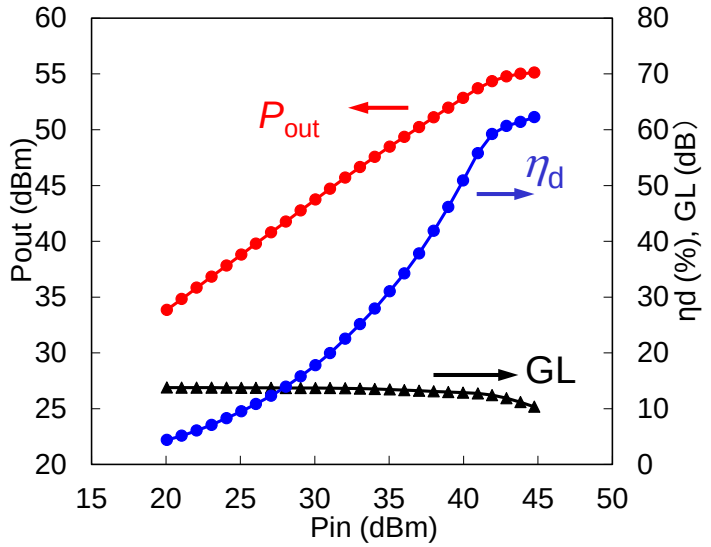


Fig. 3.21 Measured output power and efficiency versus input power under the CW condition.

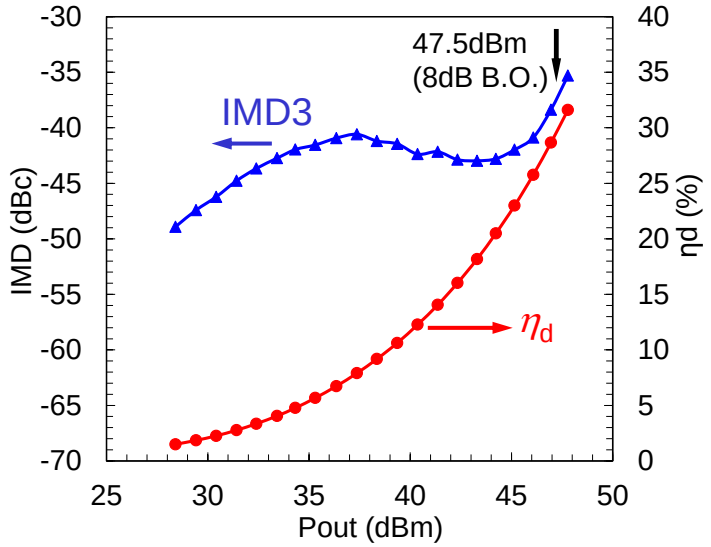


Fig. 3.22 Modulation signal output performance with two W-CDMA signals of the 15-MHz carrier spacing (2.1325 GHz, 2.1475 GHz).

3.7 Summary

In this chapter, the harmonic termination techniques in the matching circuits were examined to achieve high efficiency characteristics in high power amplifiers. What has been demonstrated is as follows.

The voltage waveforms were observed using a large signal simulation and Electro Optical Sampling (EOS).

The high efficiency termination condition of load second harmonic was found out to be open condition opposite to conventional Class-F.

By clarifying the effect of the termination condition of source second harmonic, it was confirmed that the nonlinear gate-to-source capacitance (C_{gs}) affects the overlap of the voltage and the current waveforms.

An L/S-band highly efficient 320-W GaAs FET amplifier has been developed by employing the second-harmonic terminating technique in both the input and output matching circuits.

At 2.12 GHz, an output power of 320 W has been obtained with 62% power added-efficiency and 14-dB linear gain.

Under a two-carrier W-CDMA signal condition, the amplifier exhibited low IMD3 performance of less than −37 dBc with high drain-efficiency of 30% at an output-power of 47.5 dBm.

The developed GaAs HJFETs are promising for the 3rd generation digital cellular base station applications.

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[3.15] W. Burger, H. Brech, D. Burdeaux, C. Dragon, G. Formicone, M. Honan, B. Pryor, X. Ren, “A Device Technology for High Power RF Infrastructure Applications”, 2004 IEEE CSICS Symp. Dig., pp. 189-192.

Chapter 4

Low distortion GaAs HJFET high-power amplifiers using second harmonic and difference frequency termination techniques

4.1 Introduction

Wideband code division multiple access (W-CDMA) systems are the focus of attention as one of the 3rd generation mobile communication standards. The final stage devices in the solid-state power amplifiers (SSPAs) used for W-CDMA base stations are demanded to provide both high efficiency and low distortion characteristics with high saturation output power. In order to improve the power-added efficiency, deep Class-AB operation is commonly employed, although it sacrifices the distortion characteristics. In a power amplifier, the third order intermodulation distortion (IMD3) is dominated by the third order transconductance coefficient ($gm_3 = d^3I_d/dV_g^3$) introduced from a power series expansion for the drain current.

In this time [4.1], the gm_3 characteristic dependence on transconductance (gm) profiles was investigated and it was experimentally found that FET with a steep gm-profile exhibits better symmetry and smaller value for gm_3 at Class-AB bias point. Therefore, to realize low distortion characteristics with high power, a double-doped pseudomorphic heterojunction FET (HJFET) which gives both high gm and steep gm-profile due to the high electron mobility and high aspect ratio has beed developed. Moreover, the second harmonic termination technique for the output matching circuit to obtain the low distortion characteristic was employed.

In addition, here [4.2] was focused on the influence of drain bias circuits to the distortion characteristics. The relationship between the distortion characteristics and the drain bias circuit impedance was systematically studied. A drain bias circuit to minimize intermodulation distortion (IMD) or noise power ratio (NPR) has been newly designed. By lowering the drain bias circuit impedance at the two-tone difference frequency, the push-pull AlGaAs/GaAs HFET amplifier was developed for digital cellular base station system.

High-speed broadband telecommunication technologies largely progress in the next generation mobile communication system. High efficiency and low distortion characteristics with wide frequency range are strongly demanded in power amplifiers which are the key devices of the system. In the present base station amplifiers handling modulated signals with a high peak factor such as W-CDMA signals, the linearization techniques such as a feed-forward and a digital pre-distortion have been adopted [4.3], [4.4]. The deterioration and asymmetries of IMD, which are related to the memory-effect, are obstacles to the distortion compensation. It has been reported that IMD asymmetries are caused by the termination impedance characteristics of the difference frequency and second harmonics [4.5]-[4.9]. Hitherto, difference frequency has been terminated by a bias circuit of an amplifier [4.10]-[4.12]. In these approaches, the baseband impedance was reduced by optimizing the bypass capacitor and the line-width of the drain bias circuits. However, the carrier spacing of 15MHz at the maximum is necessary on W-CDMA system. In a high power amplifier, the bias circuit is not sufficient to terminate the baseband impedance of 15 MHz in short-circuit condition. Thus far, an improvement methodology of IMD asymmetries has not yet been clearly reported for wide carrier-spacing signals in high power amplifier applications.

The improvement technique of IMD asymmetries for wide carrier-spacing signals in *L/S*-band high power amplifiers was described [4.13]. The circuit technique proposes to directly connect *LC* series resonant circuits to the gate and the drain electrodes of the transistor die in a package for baseband termination with wide frequency range. By applying this circuit technique to a 28-V-operation 200-W GaAs heterojunction field-effect transistor (HJFET) amplifier, the effect of IMD3 asymmetries improvement is provided even if the two-tone carrier spacing (Δf) exceeds 100 MHz. There is no report that exhibits flat IMD3 characteristics without deterioration against the Δf over 100 MHz in high power transistors, so far.

4.2 Volterra series analysis

The IMD3 obtained by performing the third-order Volterra series analysis with the equivalent circuit of Fig. 4.1 under the two-tone input signals of ω_1 and ω_2 is expressed as the following formulas (4.1), (4.2), (4.3) [4.14].

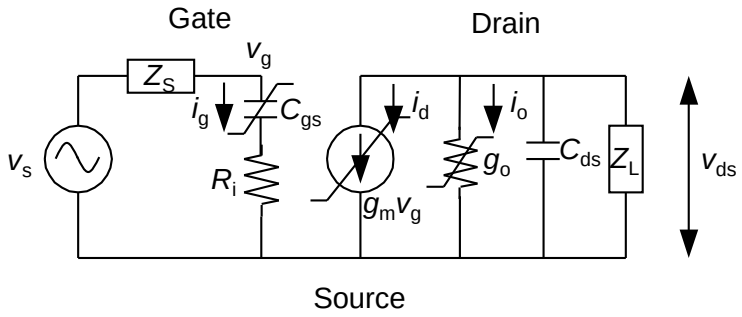


Fig. 4.1 Equivalent circuit for Volterra analysis.

$$\begin{cases} i_g = \dfrac{\partial}{\partial t}(C_{gs1}v_g + C_{gs2}{v_g}^2 + C_{gs3}{v_g}^3) \\ i_d = g_{m1}v_g + g_{m2}{v_g}^2 + g_{m3}{v_g}^3 \\ i_o = g_{o1}v_{ds} + g_{o2}{v_{ds}}^2 + g_{o3}{v_{ds}}^3 \end{cases} \tag{4.1}$$

$$\begin{cases} Y_S = \dfrac{1}{Z_S(\omega) + R_i} \\ Y_i = j\omega C_{gs1} + Y_S \\ Y_o = g_{o1} + j\omega C_{ds} + \dfrac{1}{Z_L(\omega)} \end{cases} \tag{4.2}$$

$$IMD3(dBc) = 20\log\left[\frac{3}{4}{V_S}^2\left|\frac{Y_S(\omega)}{Y_i(\omega)}\right|^2\left|\begin{array}{l} \dfrac{g_{m3}}{g_{m1}} + \dfrac{1}{Y_o(\omega)}\left(\dfrac{\frac{4}{3}g_{o2}g_{m2}}{Y_o(\omega_d)} + \dfrac{{g_{m1}}^2}{|Y_o(\omega)|^2}\left(\dfrac{\frac{4}{3}{g_{o2}}^2}{Y_o(\omega_d)} - g_{o3}\right)\right) \\ + \dfrac{j2\omega C_{gs2}}{3Y_i(2\omega)}\left(\dfrac{j2\omega C_{gs2}}{Y_i(\omega)} - \dfrac{2g_{m2}}{g_{m1}}\right) - \dfrac{j\omega C_{gs3}}{Y_i(\omega)} \\ + \dfrac{\frac{2}{3}g_{o2}}{Y_o(2\omega)Y_o^*}\left(\dfrac{-2g_{m1}j\omega C_{gs2}}{Y_i(2\omega)} + g_{m2} + \dfrac{g_{o2}{g_{m1}}^2}{Y_o(\omega)^2}\right) \end{array}\right|\right] \tag{4.3}$$

where $\omega_1 \sim \omega_2$ is assumed and is replaced with ω, and $\omega_d = \omega_2 - \omega_1$ is defined as the difference frequency.

IMD3 is found to be proportional to g_{m3}/g_{m1} from the first approximation of this analysis formula. Therefore, as a design policy for a low distortion device, from the analysis expression, the device with small g_{m3} and high g_m is advantageous for the low distortion characteristics. Furthermore, as the circuit design policy, the analysis expression is shown that the IMD3 is influenced by the load second harmonic and the load difference frequency impedance, and the source second impedance. It means that the second harmonic and the difference frequency of a two-tone signal occur when a two-tone signal is inputted into FET, and they cause mixing again with an input signal, and are superposed on the original IMD3 as shown in Fig. 4.2. The analysis formula indicates that when the load impedance given to the difference frequency and the second harmonic is short-circuited condition, the distortion characteristics can be improved suppressing the nonlinear terms.

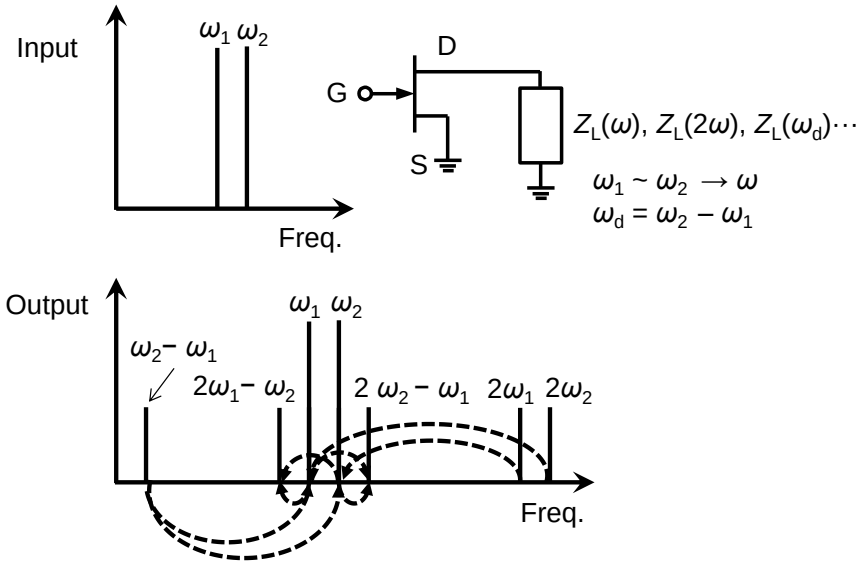


Fig. 4.2 Mixing of second harmonic and difference frequency with two-tone input signals.

4.3 Relation between gm-profile and third-order distortion characteristics in low distortion GaAs HJFET

From Volterra series analysis, it was found that, small gm_3 and high gm are important to improve the IMD3 characteristics. Therefore, the gm characteristics of HJFET were investigated because HJFET inherently gives high gm due to the high electron mobility and high aspect ratio [4.1].

A double-doped GaAs pseudomorphic HJFET was fabricated using a selective dry etching process for the threshold voltage (V_{th}) control and Au/WSi gate metallization

technology. A schematic cross-section of the fabricated HJFET is shown in Fig. 4.3. In order to obtain the steeper gm-profile, V_{th}, epitaxial layer structure and recess structures of the device were experimentally optimized.

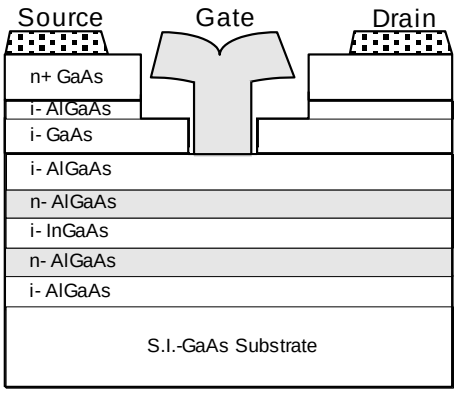


Fig. 4.3 Cross sectional view of the developed pseudomorphic HJFET.

As shown in Fig. 4.4, the fabricated HJFETs showed a small gm_3 of one-fourth compared with that of a flat-*gm* MESFET around Class-AB bias point. Thus, it was experimentally found that HJFET with a steep *gm*-profile exhibits better symmetry and smaller value for gm_3 at Class-AB bias point.

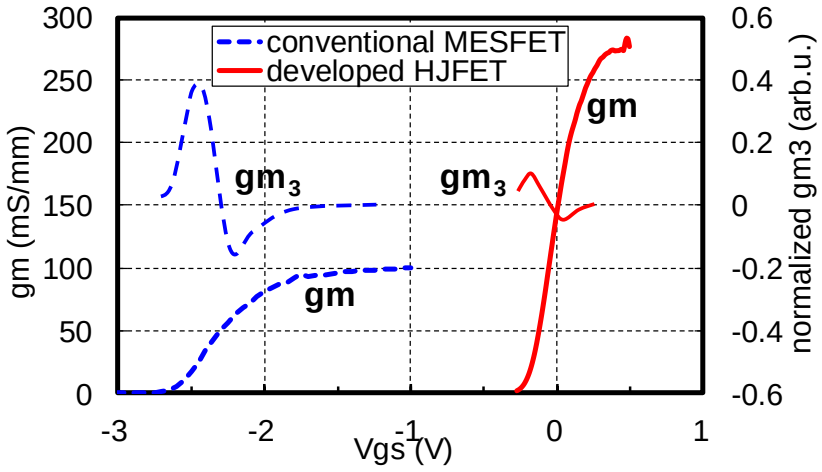


Fig. 4.4 Gm and gm3 profile of developed HJFET and conventional MESFET.

Figure 4.5 shows 3rd-order intermodulation (IM3) versus two-tone total output power of the developed HJFET and the conventional MESFET for a unit cell. The HJFET revealed 5-dB lower IM3 plateau level than that of the MESFET.

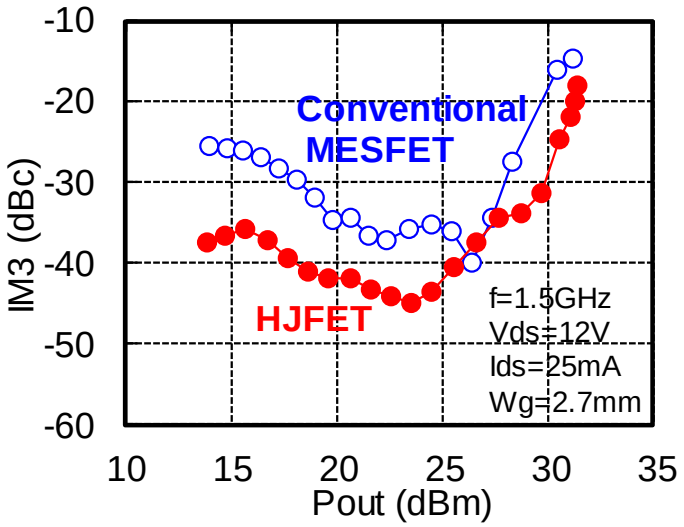


Fig. 4.5 IM3 versus two-tone total output power of developed HJFET and conventional MESFET.

4.4 Low distortion characteristics by harmonic terminations

The influence of the second harmonic load impedance on IM3 has been experimentally investigated [4.14]. Using the unit cell device of 2.7 mm, the second harmonic load impedance was changed while keeping the same fundamental load condition by tuning the trimmer condenser added on the output test-fixture as shown in Fig. 4.6. Figure 4.7 shows the position of second harmonic load impedance on IM3 measurement. Figure 4.8 shows IM3 versus two-tone total output power of the developed HJFET at Class-AB operation while changing the second harmonic load impedance. When the second harmonic impedance was tuned at around short condition, the device showed the lowest IM3 plateau level. Thus, it was found that not only obtaining a steep gm-profile but also employing the second harmonic termination of the output matching circuit was very important to obtain the low distortion characteristics.

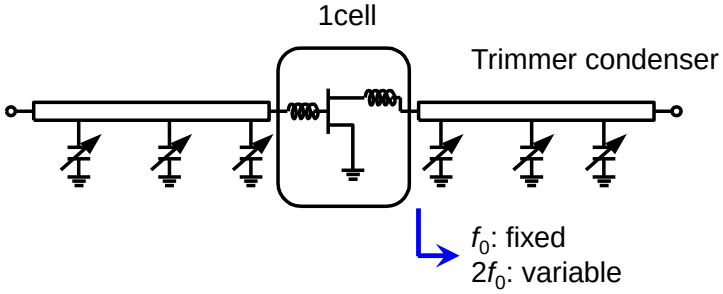


Fig. 4.6 Schematic diagram of test fixture.

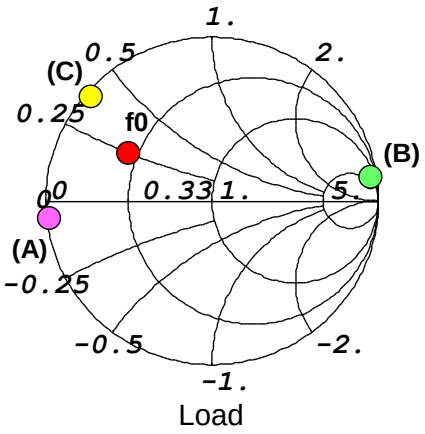


Fig. 4.7 Position of second harmonic load impedance.

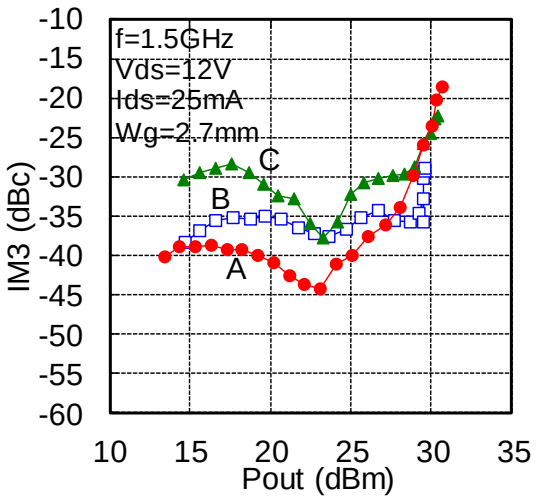


Fig. 4.8 Influence of second harmonic load impedance on IM3.

4.5 Low distortion L/S-band 150-W GaAs HJFET

4.5.1 Device structure

To realize low distortion characteristics, a double-doped AlGaAs/InGaAs pseudomorphic heterojunction FET with 0.9-μm WSi gate fabricated in a recessed structure was employed [4.1]. The thickness and concentration of AlGaAs Schottky layer and double-doped AlGaAs/InGaAs/AlGaAs epitaxial layer were designed to achieve the steeper *gm*-profile, optimal maximum drain current and gate breakdown voltage with reduced gate leakage current.

Figure 4.9 shows the photograph of the FET chip used in a push-pull amplifier. The total gate width is 82 mm and chip size is 1.3×4 mm^2. The gate-pitch (G_P) and the finger-

width (W_u) were determined to be 24 μm and 680 μm, respectively, considering the trade-off between the thermal resistance and the RF linear gain of the device as shown in Fig. 4.10. The GaAs substrate was thinned to 40 μm and a gold plated-heat-sink (PHS) with 15 μm was formed on the backside of the substrate in order to reduce the thermal resistance. The thermal resistance of the FET chip was 1.2 °C/W. Air-bridges and via-holes were used to reduce the parasitic capacitance and inductance. The typical I_{max}, transconductance, threshold voltage, and BV_{gd} are 380 mA/mm, 280 mS/mm, −0.3 V and 29 V, respectively. The breakdown voltage is enough to operate under the drain bias voltage of 12 V.

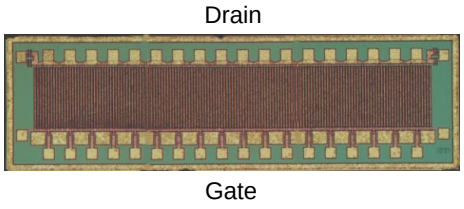


Fig. 4.9 Photograph of HJFET chip.

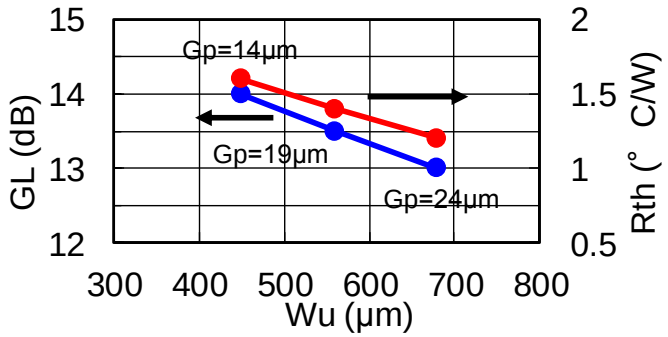


Fig. 4.10 Trade-off between the thermal resistance and the RF linear gain of the device.

4.5.2 Circuit design

Using the newly developed pseudomorphic GaAs HJFETs, the L/S-band push-pull amplifier was designed. The overall developed amplifier circuit is shown in Fig. 4.11. Two pairs of GaAs HJFET chips (i.e. total $W_g = 4 \times 82$ mm) were mounted on a single package with pre-matching circuit. The total output-power was combined in push-pull configuration with external balun circuits. The package size is 17×34 mm^2. Figure 4.12 shows the top view of the internally matched device. The internal input matching circuit consists of a two-stage *LC* low pass filter network. The internal output matching circuit consists of a transmission line and a two-stage *LC* low pass filter network in order to realize short condition for second harmonic load impedance. The simulated input- and output-circuit impedance (Z_S, Z_L) locus in the frequency range from 10 MHz to 10.01 GHz is shown in

Fig. 4.13. The normalized impedance is 50/40 Ω. The points and values of the impedance of the fundamental frequency (f_0), the second harmonic frequency ($2f_0$), and the third harmonic frequency ($3f_0$) are also indicated in Fig. 4.13.

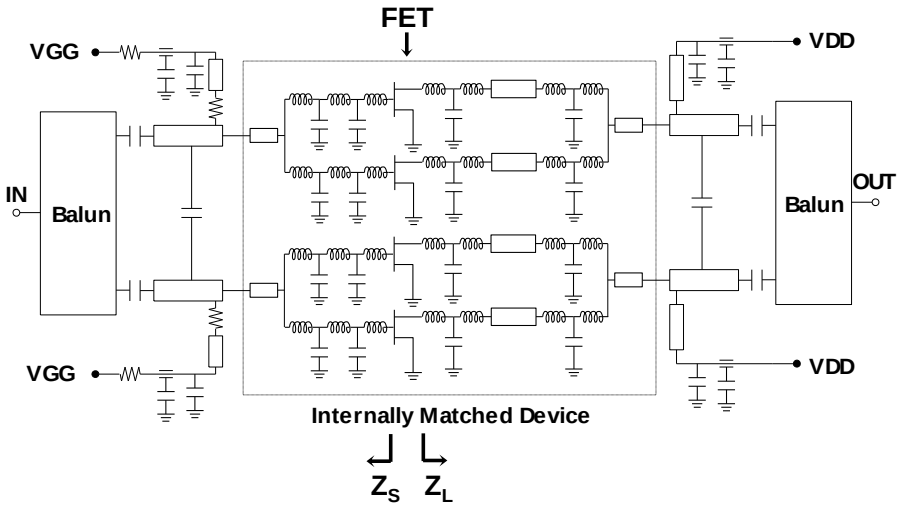


Fig. 4.11 Overall push-pull amplifier circuit.

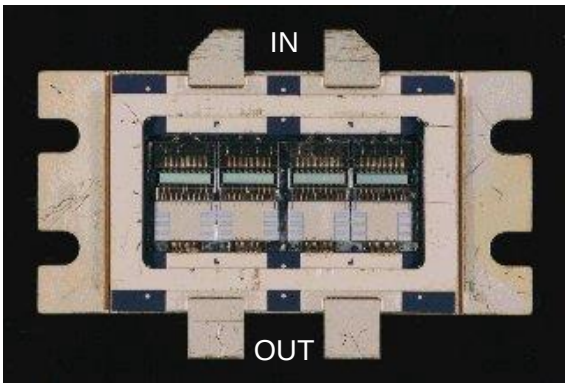
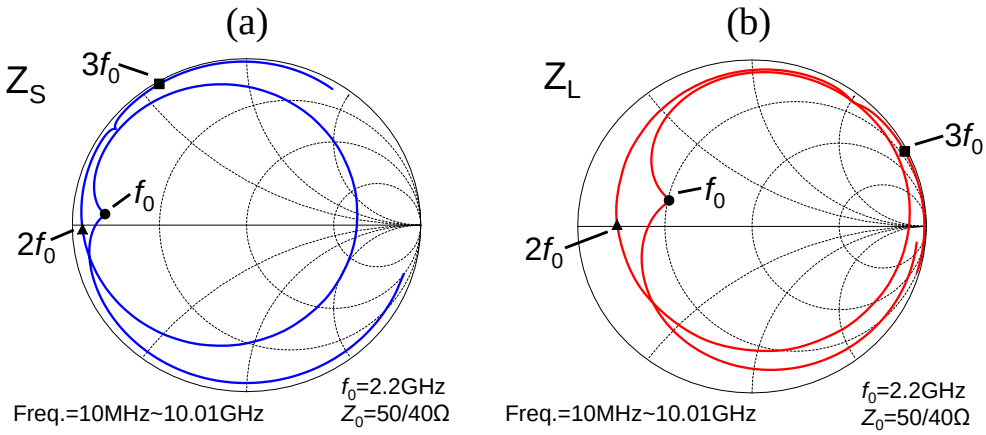


Fig. 4.12 Photograph of developed internally matched device.



	$Z_S(\Omega)$ Z_0=50/40Ω
f_0	0.10+j0.04
$2f_0$	0.03-j0.01
$3f_0$	0.01+j0.57

	$Z_L(\Omega)$ Z_0=50/40Ω
f_0	0.34+j0.14
$2f_0$	0.13+j0.01
$3f_0$	0.13+j4.14

Fig. 4.13 Simulated (a) input- and (b) output-circuit impedance (Z_S, Z_L) locus in the frequency range from 10 MHz to 10.01 GHz.

4.5.3 RF performance

Measured output power and power-added efficiency versus input power are shown in Fig. 4.14. The developed amplifier exhibited a saturation output power of 51.5 dBm (140 W) with a linear gain of 13 dB and a power-added efficiency of 50.5% at 2.2 GHz (at V_{ds} = 12 V, I_{dsq} = 4% I_{max}). IM3 versus total output power at two tones (2.2 GHz, 2.201 GHz) is shown in Fig. 4.15. The amplifier exhibited low IM3 characteristics of less than −40 dBc at the total output-power of 43 dBm, and achieved more than 5 to 10-dB improvement of the IM3 in comparison with the ever-reported GaAs MESFETs [4.15], [4.16]. Using this GaAs HJFET technology, high-gain, high-efficiency, high-power, and low distortion characteristics have been simultaneously achieved.

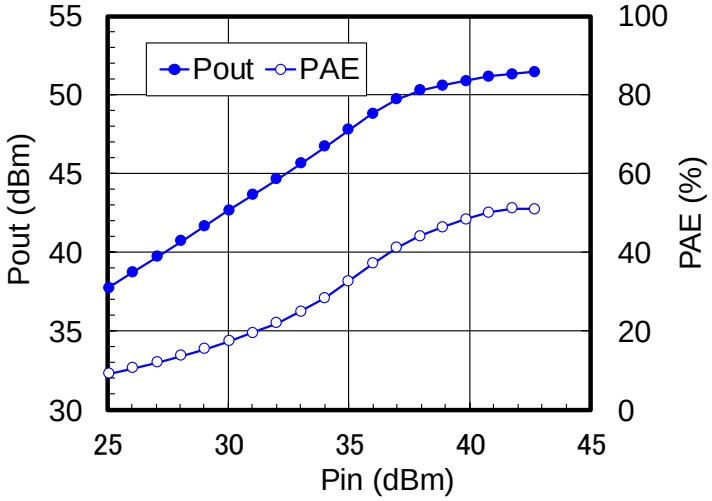


Fig. 4.14 Output power and power-added efficiency versus input power of developed push-pull amplifier at 2.2 GHz, V_{ds} = 12 V, I_{dsq} = 4 A.

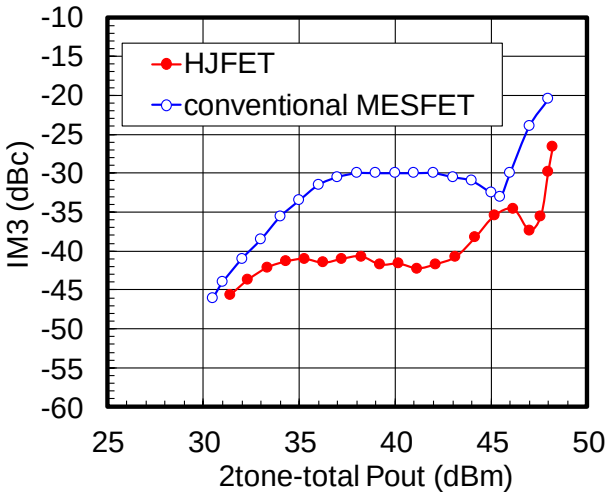


Fig. 4.15 IM3 versus two-tone output power at 2.2 + 2.201 GHz, V_{ds} = 12 V, I_{dsq} = 4 A.

4.6 Improvement of IMD characteristics by lowering drain bias circuit impedance

4.6.1 Experiments of lowering drain bias circuit impedance on L/S-band 17-W GaAs FET

It was reported that when the output bias circuit impedance was high at the 2-tone intermediate frequency ($|f_2 - f_1|$), RF carrier outputs were distorted by the amplitude modulation at the intermediate frequency [4.11]. Figure 4.16 is the drawing which explains the relationship between intermodulation distortion (IMD) and the drain bias circuit impedance. When a 2-tone signal is introduced, odd-order distortion causes intermodulation at frequencies close to the input signals, such as IM3 (3rd-order intermodulation) or IM5 (5th-order intermodulation). On the other hand, even-order distortion causes spurious signals at low frequencies. As found from the IM3 expression (4.3) determined by the Volterra series analysis in Section 4.2, the IM3 is proportional to difference frequency impedance. If the impedance of the drain bias circuit at these frequencies is high, the difference frequency voltage increases. Then, the difference frequency signal is again mixed with the input signals to yield odd-order distortion, which is added to the original odd-order distortion. In this case, IM3 is considered to depend on the spurious signals generated by 2nd-order distortion and 4th-order distortion, which are the spurious at the difference frequency of the input signals and at the 2nd harmonic frequency of the difference frequency.

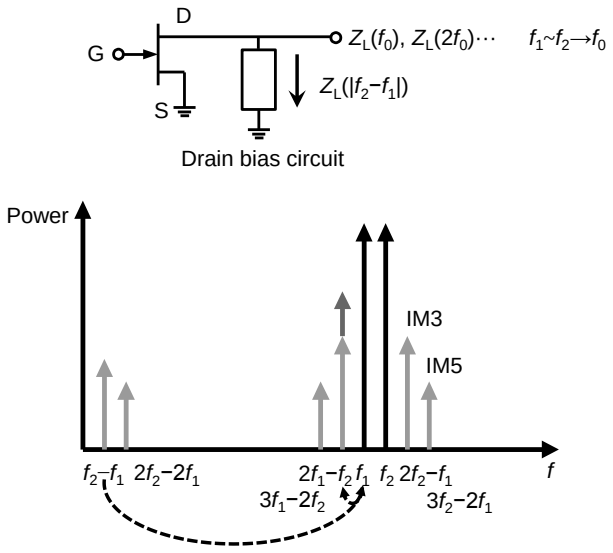


Fig. 4.16 Intermodulation distortion degradation.

Figure 4.17 shows the relationship between noise power ratio (NPR) and the drain bias circuit impedance. It can be seen that the spurious signals are generated at the frequency region from DC to the input noise bandwidth frequency. These spurious signals cause additional signals at the notch area in exactly the same manner as the 2-tone case. Therefore, the NPR is influenced by the spurious signal from the DC region to half of the noise bandwidth.

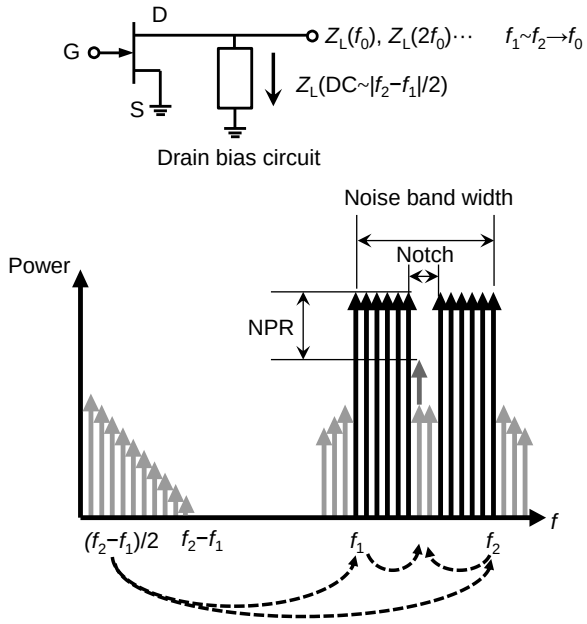
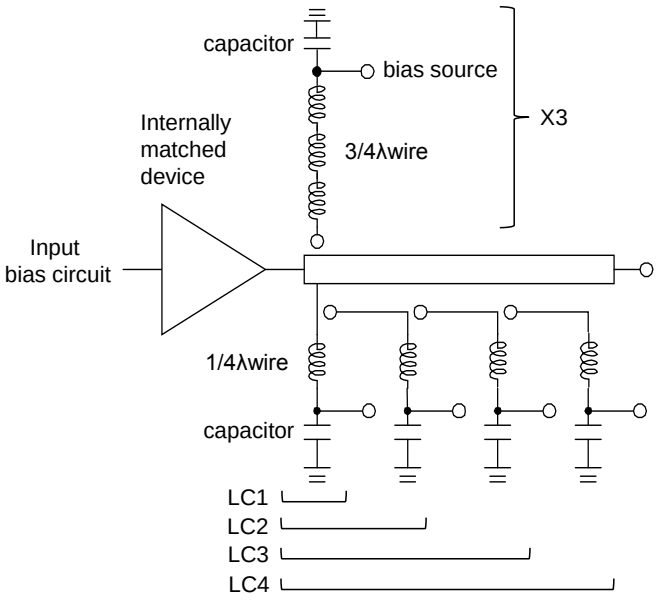


Fig. 4.17 Noise power ratio degradation.

The internally matched amplifier employed in experiments was designed at 1.5 GHz to combine the output power of two FET chips with a total gate-width of 70 (35 × 2) mm. The single-ended amplifier featured a high PAE (Power-Added Efficiency) of 68% with 17-W output power and 16-dB linear gain at 1.5 GHz at V_d = 8 V.

The relationship between the distortion characteristics and the drain bias circuit impedance was investigated by measuring not only IM3 but also NPR at various difference frequencies ($|f_2 - f_1|$) for IM3 (0.05~10 MHz) and various noise-band widths for NPR (0.1~40 MHz). Figure 4.18 shows the drain bias circuit employed in our experiment. The impedance of the output bias circuit was varied by connecting a unit circuit consisting of a 1/4λ Cu-wire at 1.5 GHz and a capacitor in parallel (LC1~LC4) or by using additional circuit consisting of a 3/4λ Cu-wire and a capacitor (X3). The calculated values of inductance and capacitance for each bias circuit are also shown in Fig. 4.18.



	LC1	LC2	LC3	LC4	X3
C[uF]	22	44	66	88	10
L[nH]	32	16	10.7	8	96

Fig. 4.18 Schematic of the output bias circuit used for the experiment.

4.6.2 Results of experiment and simulation

Figure 4.19 shows the measured impedance of the output bias circuit, indicating that the principal part of the bias circuit is dominated by the line inductance at frequencies over 1MHz. Figure 4.20 shows the measured IM3 and NPR as a function of the bias circuit impedance, defined as the impedance calculated at the difference frequency for IM3 and at half of the noise bandwidth for NPR. It was found that IM3 and NPR are drastically degraded when the absolute value of the bias circuit impedance is larger than 1 Ω. These results indicate that choosing a low impedance value less than 1 Ω in the low frequency range while ensuring sufficiently high impedance at the fundamental frequency is essential to suppress degradation in the distortion characteristics.

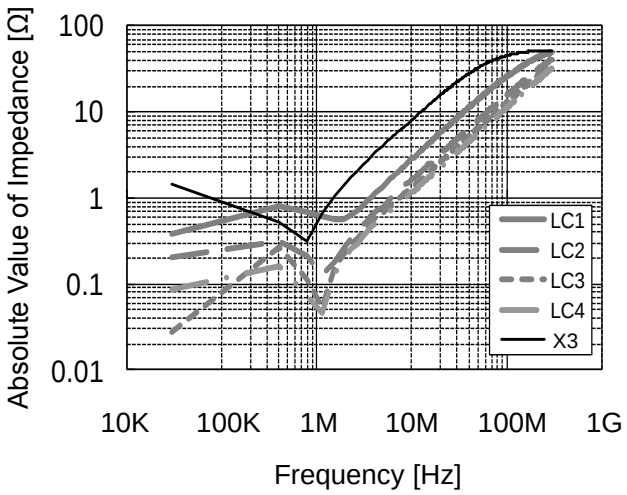


Fig. 4.19 Measured impedance of bias circuits including a terminal output of 50 Ω.

Slight discrepancies of the critical impedance or degradation rate between IM3 and NPR in Fig. 4.20 seem to be caused by the difference of the effective low frequency region between IM3 and NPR. As shown in Fig. 4.16, IM3 is influenced by the impedance at the difference frequency of the input signals and the 2nd harmonic frequency of the difference frequency. On the other hand, NPR is, at most, influenced by the impedance at frequencies from DC to half of the noise bandwidth as shown in Fig. 4.17.

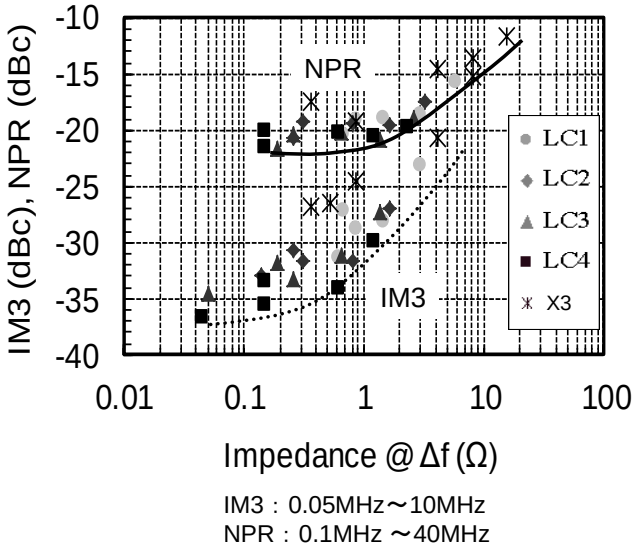


Fig. 4.20 NPR and IM3 at 5 dB output power back-off point as a function of the output bias circuits impedance at the differential frequency for IM3 and at half of the noise bandwidth for NPR.

Figure 4.21 shows the simulated IM3, where measured IM3 and the simulated drain bias voltage modulation at the difference frequency are also plotted. The simulated IM3 agrees well with the measured IM3. The amplitude of the drain bias voltage modulation increases in proportion to the bias circuit impedance at the difference frequency. The

amplitude of drain bias voltage modulation is about 1 V when the bias circuit impedance is chosen to a critical value of 1 Ω. In other words, the critical drain bias voltage modulation to significantly influence the distortion characteristics is about 1 V when the drain voltage is 8 V.

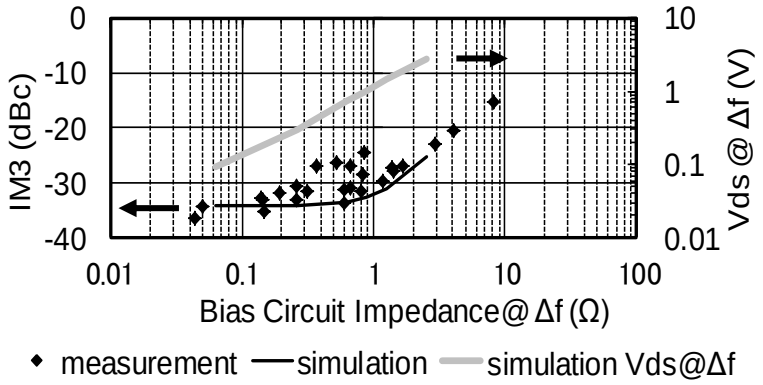


Fig. 4.21 Simulated IM3, measured IM3 and the amplitude of the drain bias voltage modulation at the differential frequency.

Figure 4.22 shows the noise output power and the noise PAE as a function of the drain bias circuit impedance at half of the noise-band width frequency. It is seen that the high drain bias circuit impedance detrimentally influences these characteristics as well as the distortion characteristics. These degradations seem to be caused by the drain bias voltage swing in the low frequency range, which moves the matching point to that far from the optimal matching condition.

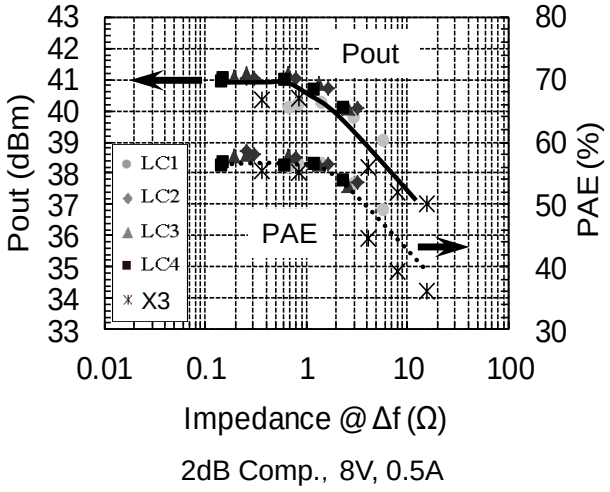


Fig. 4.22 Noise output power and noise power-added efficiency as a function of the output bias circuits impedance at half of the noise bandwidth frequency.

Figure 4.23 shows the 2-tone input load lines simulated at 1.5 GHz with 10-MHz-spacing for the high bias circuit impedance case (a) and for the low bias circuit impedance case (b). Simulation was performed at 2-dB-gain compression operation in Class-AB mode

(8 V, 0.5 A). The time domain simulation of the drain voltage and current waveforms indicates that the load line is modulated by the 10-MHz beat frequency toward a smaller drain voltage nonlinear-region when the bias circuit impedance is high. On the other hand, when the bias circuit impedance is low, the bias point is moved to a larger drain current linear-region as in the case of a single tone input. Therefore, the distortion characteristics at high bias circuit impedance are inferior to those at low bias circuit impedance. Moreover, maximum drain voltage amplitude at high bias circuit impedance is more seriously degraded than that at low bias circuit impedance. Thus, the degradation of 2-tone (or multi-carrier) output power and efficiency is ascribed to the drain voltage modulation associated with the magnitude of drain bias circuit impedance.

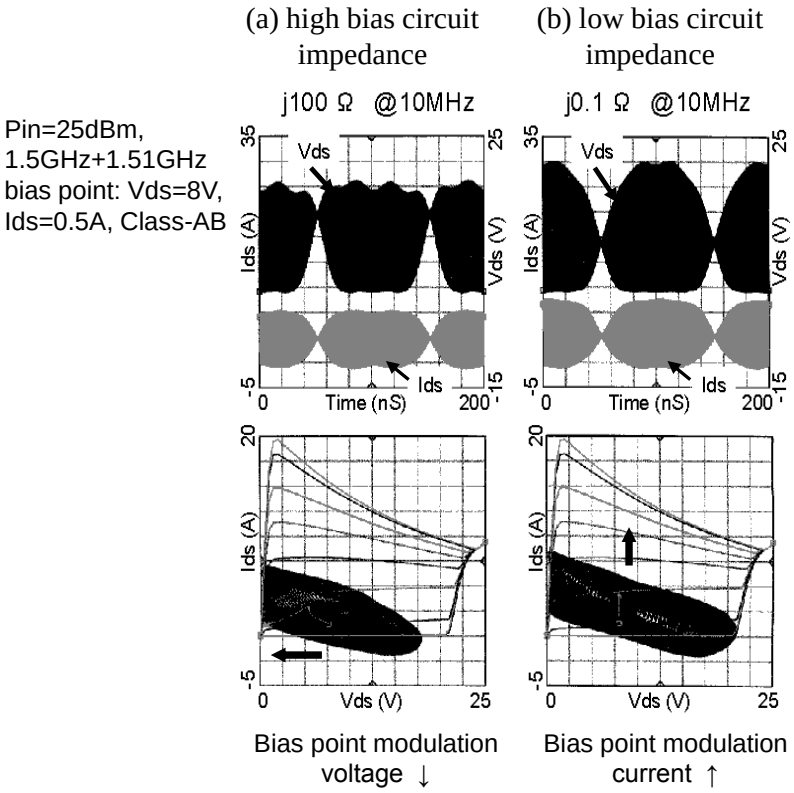


Fig. 4.23 Simulated 2-tone input load lines at 1.5 GHz with 10-MHz-spacing for the high bias circuit impedance case (a) and for the low bias circuit impedance case (b).

4.6.3 Drain bias circuit design

Based on the experimental results obtained for the single-ended amplifier with W_g = 35 × 2 mm and $1/gd$ = 4.5 Ω, a drain bias circuit for the push-pull amplifier has been designed. Sufficiently lowering the drain bias circuit impedance is efficient to suppress drain bias voltage modulation by low frequency even-order distortion. This low frequency even-

order distortion power increases in proportion to the total-W_g. Therefore, the bias circuit critical impedance (=Rc) to begin affecting the distortion characteristics was estimated by scaling the total-W_g or gd as

$$\begin{aligned} Rc &= 70/Wg \qquad (\Omega) \\ Rc &= (1/gd)/4.5 \qquad (\Omega) \end{aligned} \tag{4.4}$$

When the drain bias circuit impedance is larger than Rc, the drain bias voltage modulation becomes more than about 1 V. Each device, combined in push-pull configuration, is provided with a drain bias circuit. The critical impedance for a single-ended FET amplifier (i.e. W_g = 82 × 2 mm) is estimated to be less than 0.4 Ω from eq.(4.4). As the amplifier for base station application is required to provide optimized IMD performance over a 20-MHz bandwidth, the absolute value of the drain bias circuit impedance needs to be less than 0.4 Ω.

A drain bias circuit was designed as shown in Fig. 4.24. The bias circuit impedance was optimized by choosing the micro-strip line width so as to reduce the line inductance. After all, the characteristic impedance of 25 Ω was chosen for the drain bias circuit micro-strip line, considering the influence on the fundamental frequency band-width at the same time.

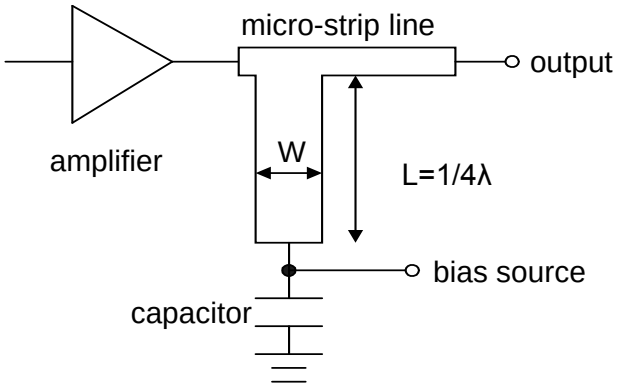


Fig. 4.24 Schematic of the designed output bias circuit for L/S-band amplifier.

Figure 4.25 shows the measured IM3 at a two-tone total output-power of 40 dBm as a function of the 2-tone frequency spacing (Δf). The IMD for the developed push-pull amplifier was found to be flat over a 10-MHz bandwidth. Figure 4.26 shows the IM3 as a function of the bias circuit impedance at the difference frequency. Note that IM3 is degraded with a 3-dB/oct. slope when the absolute value of the bias circuit impedance is higher than about 0.4 Ω.

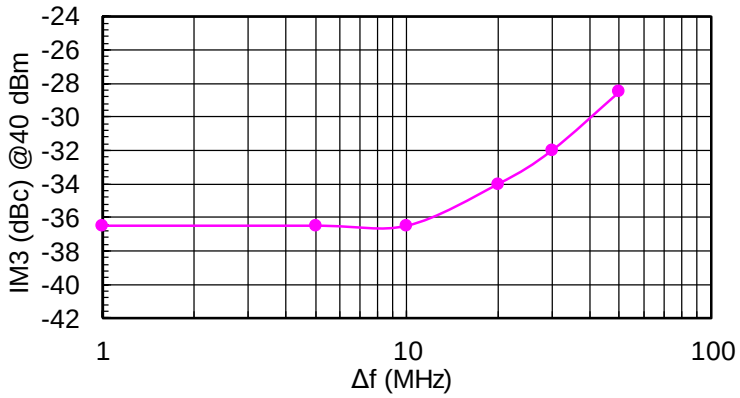


Fig. 4.25 Measured IM3 at two-tone output power of 40dBm as a function of the two-tone spacing. V_d=10V. I_{dsq}=8A.

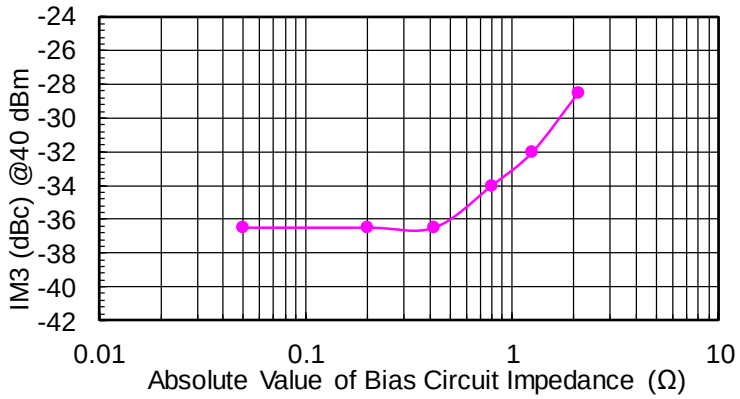


Fig. 4.26 Measured IM3 at two-tone output power of 40dBm as a function of the drain bias circuit impedance at the differential frequency. V_d=10V. I_{dsq}=8A.

However, the carrier spacing of 15 MHz at the maximum is necessary on W-CDMA system. Namely, in a high power amplifier, the bias circuit is not sufficient to terminate the baseband impedance of 15 MHz in short-circuit condition. The improvement methodology of IMD degradation is strongly required for wide carrier-spacing signals in modern high power amplifier applications.

4.7 Improvement technique of IMD Asymmetries caused by second-order Nonlinearity

4.7.1 IMD3 asymmetries caused by second-order nonlinearity

As shown in Fig. 4.27, in addition to IMD3 generated by third-order nonlinear processes, IMD3 also occurs by mixing processes of fundamental frequency components with

difference frequency components and second harmonics, which are the second-order nonlinear components generated by current and charge nonlinearity in a transistor[4.17]-[4.19]. Then, the difference frequency plays major role in IMD3 asymmetries. The second harmonics also contribute to IMD3 asymmetries through the difference frequency. If the source or the load termination impedances of the difference frequency are finite, IMD3 deteriorates and IMD3 asymmetries occur [4.17]. In other words, to eliminate the IMD3 asymmetries, both the source and the load baseband impedance must be terminated in short-circuit condition. In the Appendix B, the IMD3 analysis formula was expressed and discussed by introducing the baseband and the second harmonic impedances of input circuits as well as output circuits by using Taylor-series approximation model with current and charge nonlinearity. The perturbation method is employed for IMD3 analysis instead of Volterra series analysis [4.18].

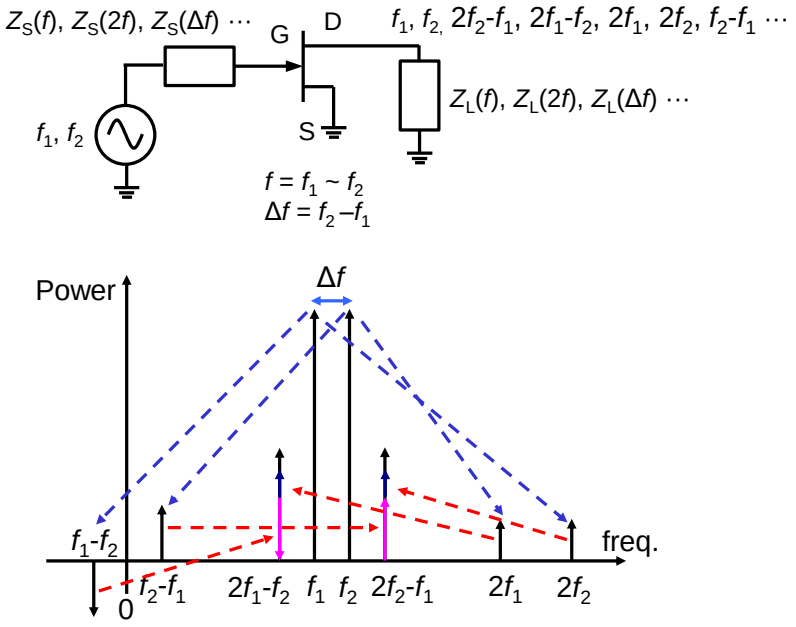


Fig. 4.27 IMD3 asymmetries generation mechanism by second-order nonlinearity.

4.7.2 Design of novel baseband termination circuits

In a high power amplifier, the distortion components of difference frequency increase according to the increase of output power. Therefore, in order to eliminate the influence of difference frequency to the IMD characteristics, the baseband impedance must be sufficiently reduced. Furthermore, for wide carrier-spacing signals, the baseband impedance must be terminated in short-circuit condition for wide frequency range. Newly, the circuit technique to directly connect *LC* series resonant circuits to the gate and the drain electrodes of the

transistor dies in a package (PKG) for baseband terminations with wide frequency range is proposed.

Figure 4.28 shows the equivalent circuit of the proposed amplifier with bias circuits and difference frequency termination circuits. Bias circuits usually consist of a quarter wave length ($\lambda/4$) line of fundamental frequency and RF termination capacitors to avoid the power loss in fundamental frequency band. The difference frequency termination circuits are composed of inductance L of bonding wires and capacitance C of difference frequency short-circuit capacitors. To reduce the baseband impedance in wide frequency range, the L and the C of LC series resonant circuits need to be minimized and maximized, respectively, considering the power loss in fundamental frequency band and the stability. As for the baseband impedance, ωL becomes dominant in that $1/\omega C$ can be ignored using the capacitors with enough large capacitance. The inductance can be smaller by shortening bonding-wires, and, as a result, baseband impedance can be reduced for wide frequency range. On the other hand, the 2-GHz fundamental frequency impedances at the gate and the drain electrodes of the 100-W-class high power FETs show very small absolute values of about 0.05 Ω and 0.2 Ω, respectively. Since the fundamental frequency is more than twenty times as high as difference frequency, there is little influence to fundamental frequency band by connecting difference frequency LC short-circuits to the gate and the drain electrodes.

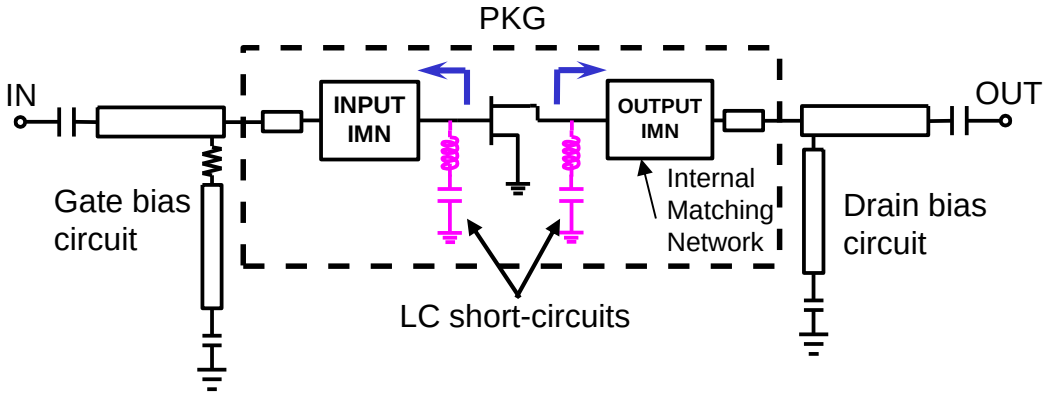


Fig. 4.28 Equivalent circuit of proposed amplifier with bias circuits and difference frequency termination circuits.

Figure 4.29 shows the calculation results of the output circuit impedance adding the difference frequency termination circuits at the drain electrodes of the FETs in comparison with the case of only the external bias circuits. The baseband impedance is significantly reduced in a wide frequency range more than 100 MHz by adding difference frequency termination circuits. Besides, the difference frequency termination circuits are also confirmed to have little influence to fundamental frequency and second harmonics.

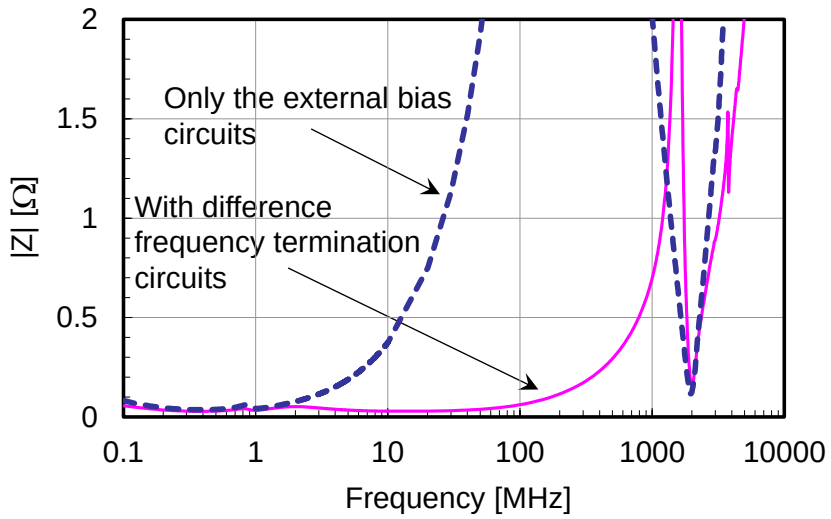


Fig. 4.29 Calculation results of the output circuit impedance.

About the 2.2-GHz 28-V-operation 200-W GaAs HJFET push-pull amplifier described in Chapter 3, the effect of the difference frequency termination circuits on the IMD3 characteristics against the Δf at constant output power (P_{out}) of 40 dBm was simulated utilizing a large signal model (EEHEMT1). The amplifier was biased at the V_{ds} of 28 V and the V_{gs} of −0.35 V with the I_{dsq} of 1.5 A. Figure 4.30 shows the two-tone continuous wave (CW) IMD3 versus Δf characteristics and the frequency dependence of baseband-impedance in the case of equipping the difference frequency short-circuits only at the drain electrodes of the FETs. To realize the circuits in PKG, the L of 0.35 nH and the C of 1 μF are selected. Then, the drain bias circuit comprises a fundamental frequency λ/4 line with RF termination capacitors (20 pF, 10 μF). The gate bias circuit consists of the gate resistance of 1.1 Ω and a fundamental frequency λ/4 line with RF termination capacitors. In spite of the fact that the load baseband impedance is reduced sufficiently in the range of 100 MHz, the IMD3 magnitude characteristics are deteriorated by around 20 dB from 20 MHz to 100 MHz, and the upper and the lower components of IMD3 ($IMD3_U$, $IMD3_L$) show asymmetry characteristics. The reason of the deterioration and the asymmetries on IMD3 is that the difference frequency gate voltage occurs by concerning the even-order nonlinearities in a transistor.

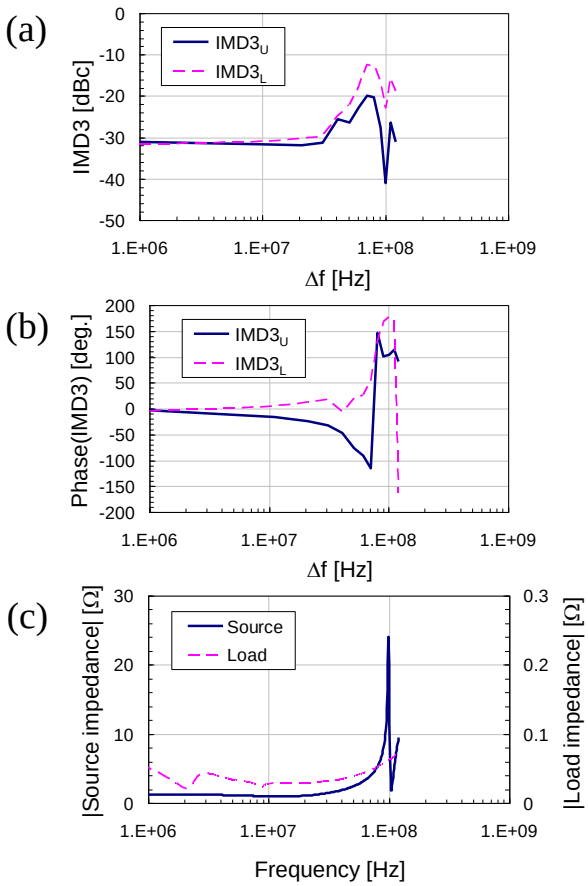


Fig. 4.30 Simulated two-tone CW IMD3 versus Δf characteristics and frequency dependence of baseband-impedance in the case of equipping the difference frequency short-circuits only at the drain electrodes. (a) Magnitude of IMD3 versus Δf characteristics. (b) Phase of IMD3 versus Δf characteristics. (c) Frequency dependence of source and load baseband impedance.

As shown in Fig. 4.31, the difference frequency drain voltage is held down with less than 0.35 V for the drain-source voltage (V_{ds}) of 28 V, but the difference frequency gate voltage of 0.25 V occurs for the gate-source voltage (V_{gs}) of −0.35 V. This is because the source baseband impedance becomes large due to the external gate bias circuit with the gate resistance and the fundamental frequency λ/4 line.

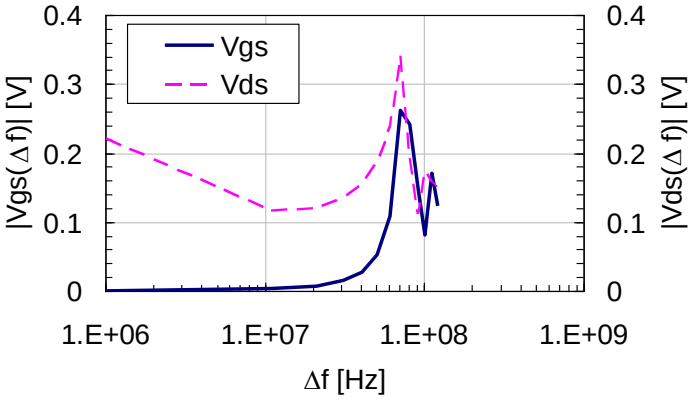


Fig. 4.31 Simulated difference frequency gate and drain voltage in the case of equipping the difference frequency short-circuits only at the drain electrodes.

Figure 4.32 shows the magnitude and the phase of two-tone CW IMD3 versus Δf characteristics and the frequency dependence of baseband impedance in the case of adding the difference frequency short-circuits (L = 0.15 nH, C = 1 μF) to the gate electrodes of the FETs. By adding the difference frequency short-circuits to the gate electrodes, the baseband impedance in the input circuits is reduced sufficiently to the frequency range over 100 MHz. Hereby, the IMD3 characteristics against the Δf become flat without deterioration in the frequency range over 100 MHz.

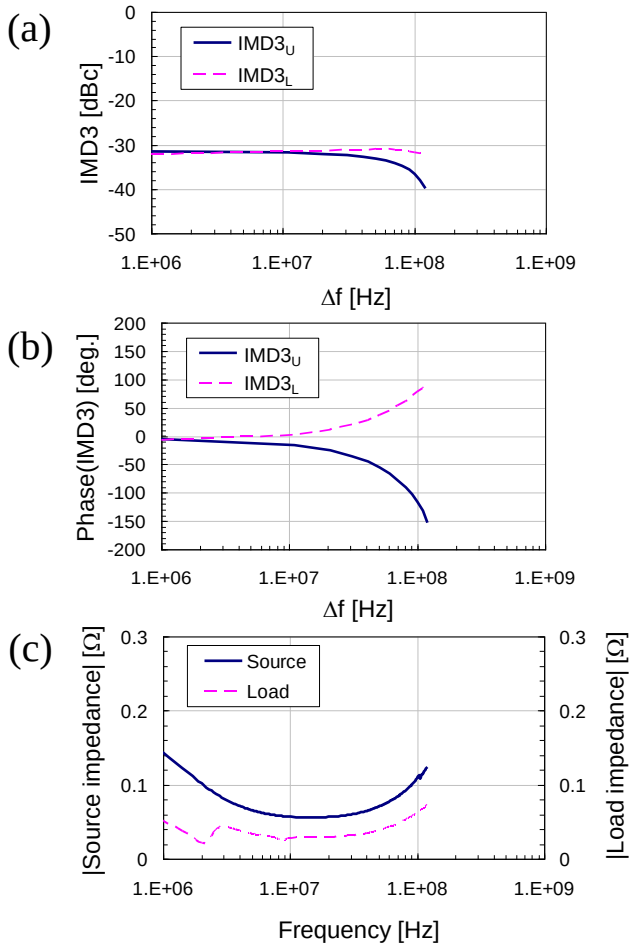


Fig. 4.32 Simulated two-tone CW IMD3 versus Δf characteristics and frequency dependence of baseband-impedance in the case of equipping the difference frequency short-circuits at both the gate and the drain electrodes. (a) Magnitude of IMD3 versus Δf characteristics. (b) Phase of IMD3 versus Δf characteristics. (c) Frequency dependence of source and load baseband impedance.

As shown in Fig. 4.33, the difference frequency gate voltage is reduced to less than 5 mV, which doesn't affect the bias point. It can be said that both the load and the source baseband impedances must be reduced sufficiently in wide frequency range to eliminate IMD asymmetries against the wide Δf.

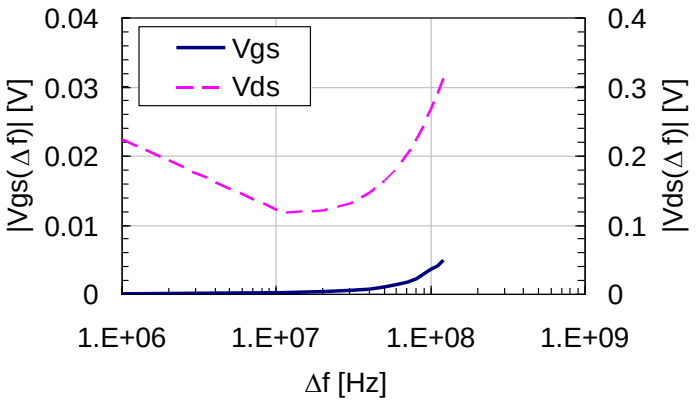


Fig. 4.33 Simulated difference frequency gate and drain voltage in the case of equipping the difference frequency short-circuits at both the gate and the drain electrodes.

4.7.3 Implementation Results

The GaAs HJFETs amplifier having the source and the load baseband termination circuits has been developed. Figure 4.34 shows the internal view and the equivalent circuits of developed 28-V-operation 200-W push-pull HJFETs. The capacitors of the source difference frequency termination circuits were placed between the two chips and were connected to the gate electrodes by the bonding wires. The capacitors of the load difference frequency termination circuits were arranged between the drain electrodes and the source electrodes through the bonding wires and the through-holes formed on the alumina substrates of the output internal matching circuits.

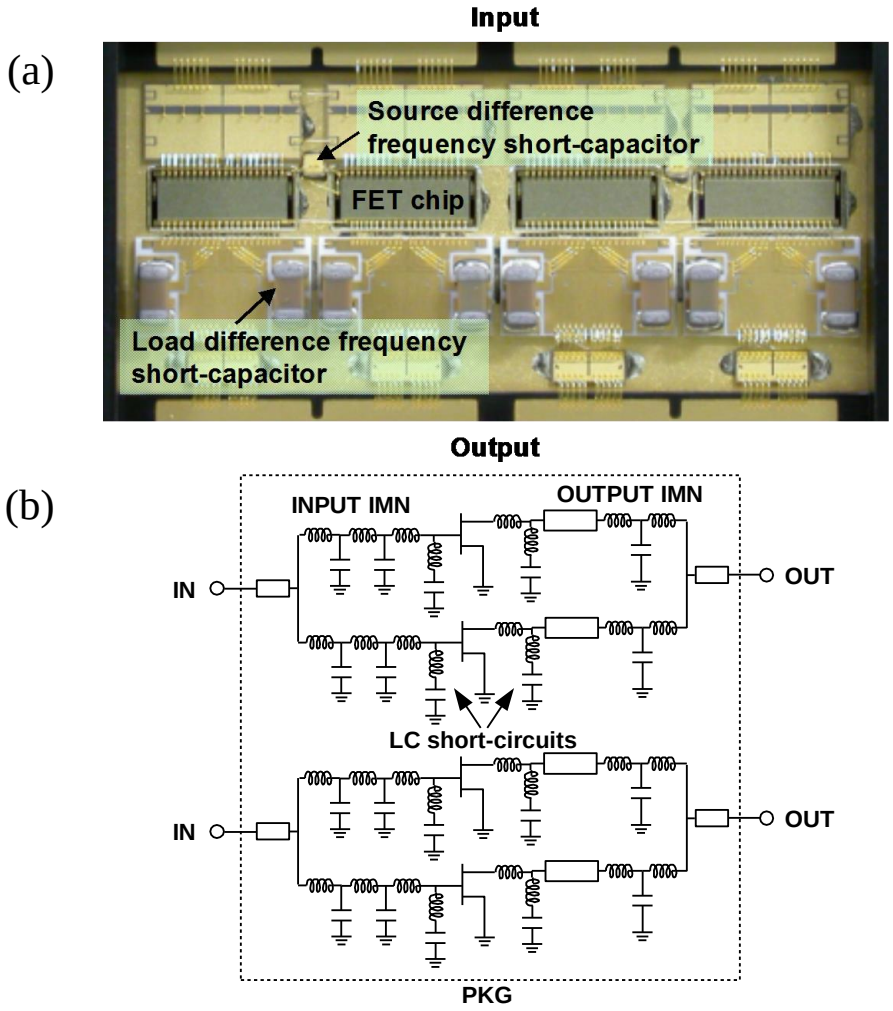


Fig. 4.34 (a) Internal view and (b) equivalent circuits of developed 28-V-operation 200W push-pull HJFETs.

Figure 4.35 shows the measured and the simulated two-tone CW IMD characteristics against the Δf with the center frequency of 2.14 GHz at constant P_{out} of 40 dBm about the 200-W push-pull GaAs HJFETs amplifier without and with the source difference frequency termination circuits at the gate electrodes, equipping the load difference frequency termination circuits at the drain electrodes. It is biased at the V_{ds} of 28 V and the quiescent drain current (I_{dq}) of 1.6 A of Class-AB operation. Without the source difference frequency termination circuits, the IMD3 asymmetries begin to occur from the Δf of around 10 MHz and the magnitude characteristics of IMD3 begin to deteriorate from the Δf of around 30 MHz. On the other hand, with the source difference frequency termination circuits, the deterioration of IMD3 doesn't occur up to the Δf over 100 MHz. The IMD3 characteristics against the Δf of 100 MHz are improved by around 14 dB applying the source and the load difference frequency termination circuits. The fifth-order intermodulation distortion (IMD5) and the seventh-order intermodulation distortion (IMD7) also represent flat characteristics

without deterioration against the Δf. To author's knowledge, there is no report that exhibits flat IMD characteristics against the Δf over 100 MHz in high power transistors [4.20].

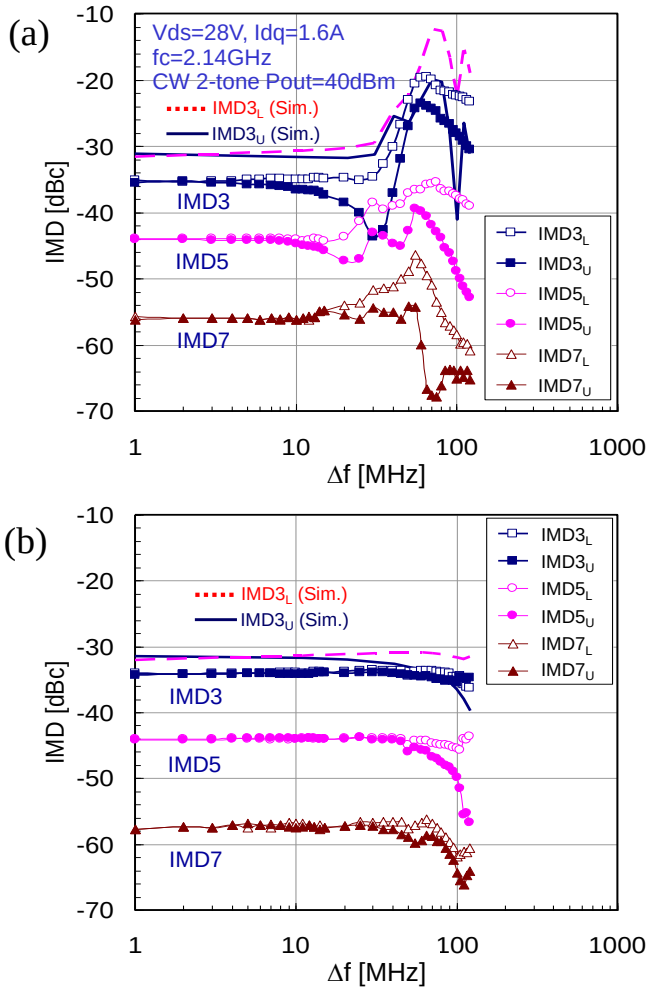


Fig. 4.35 Measured two-tone CW IMD versus Δf characteristics of 200-W GaAs HJFETs amplifier (a) without and (b) with source difference frequency termination circuits at gate electrodes, equipping load difference frequency termination circuits at drain electrodes. Simulated characteristics are shown for comparison.

Figure 4.36 shows the modulated signal performance of the developed 28-V-operation 150-W single-ended GaAs HJFETs amplifier having the source and the load difference frequency termination circuits under the two-carrier W-CDMA signals of 2.1325 GHz and 2.1475 GHz of 15-MHz carrier-spacing. The W-CDMA signal condition is a 3GPP test model 64ch with a peak-to-average power ratio (PAR) of 8.5 dB at 0.01% on the complementary cumulative distribution function (CCDF). The IMD3 characteristics under two-carrier W-CDMA signals were measured in 3.84-MHz channel bandwidth at ±15-MHz offset. The upper and the lower components of IMD3, IMD5, and IMD7, respectively exhibited little deviation. Employing the proposed difference frequency termination techniques, it was enabled that there was no degradation of the IMD3 characteristics under

two-carrier W-CDMA signals in the maximum career-spacing of 15 MHz, which is required for W-CDMA system.

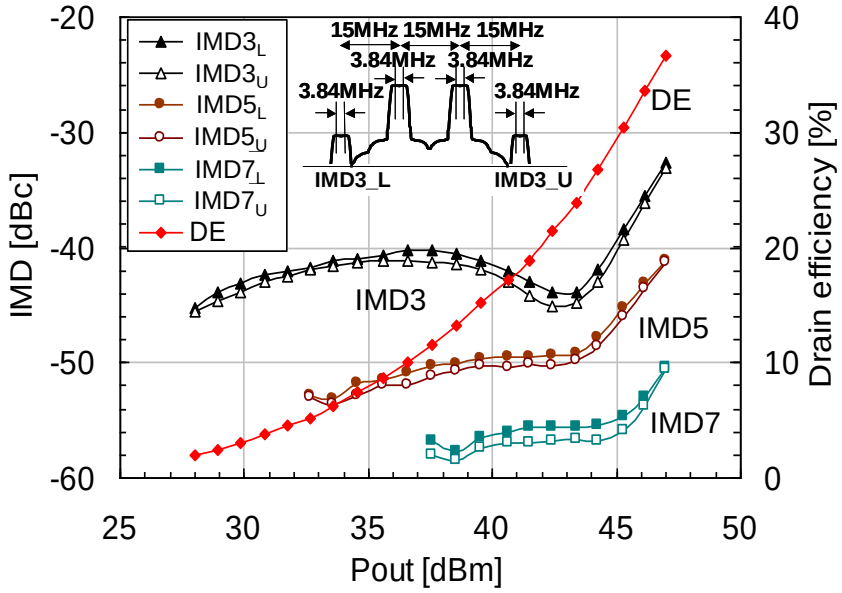


Fig. 4.36 Measured two-carrier modulated signal IMD and drain efficiency (DE) versus P_{out} characteristics of 150-W GaAs HJFETs amplifier having source and load difference frequency termination circuits with the two-carrier W-CDMA signals of 2.1325GHz and 2.1475GHz of 15-MHz carrier-spacing.

4.8 Summary

Chapter 4 described the study on low distortion microwave high power amplifiers. It is necessary to clarify the policy of device structure optimization and circuit design in order to achieve low distortion characteristics. What has been demonstrated is as follows.

Focusing on *gm*-profile of GaAs HJFET, it was found that HJFET with shallow threshold voltage (V_{th}) and steep *gm*-profile has small third-order coefficient of *gm* (gm_3) at deep Class-AB, and exhibits low distortion characteristics.

Furthermore, the influence of second harmonic and difference frequency impedance on third-order distortion characteristics was investigated using Volterra analysis.

The circuit configuration terminating source- and load-second harmonics with short impedance was newly proposed.

An L/S-band 150-W GaAs HJFET employing the second harmonic termination circuits realized low third-order intermodulation distortion (IM3) characteristics less than −40 dB.

In addition, the source- and load-difference frequency termination circuits in package as well as the technique lowering drain bias circuit impedance were proposed.

The proposed techniques realized low distortion characteristics without degradation over 100-MHz frequency-spacing (Δf). The result is the widest bandwidth and low distortion characteristics so far, and the deployment to next-generation communications such as a fourth generation (4G) can be expected.

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Chapter 5

Inverted Doherty high-power amplifiers with high efficiency and low distortion

5.1 Introduction

Both high efficiency and low distortion are strongly required for multi-carrier amplifiers used in modern mobile communication base stations. In present base station systems with a high peak factor such as W-CDMA signals, a feed-forward and a digital pre-distortion have been main linearization methods. In addition, various efficiency enhancement techniques such as Class-F, Doherty, envelope elimination and restoration, Chireix outphasing, and envelope tracking have been investigated for practical use [5.1]–[5.4]. Among these circuit investigations, Doherty configuration is one of the most promising candidates for this purpose due to the advantages of circuitry simplicity, wide bandwidth, and high stability. In recent years, the Doherty amplifiers applying a feed-forward and a digital pre-distortion have been actively studied [5.5], [5.6]. However, the Doherty configuration using a Class-C peak amplifier has a common problem to deteriorate distortion characteristics compared to the Class-AB operation because of non-constant gain and phase behavior. So far, many publications have been reported for Doherty amplifier performance, but the design methodology has not yet been clearly reported for high efficiency and low distortion performance [5.7]-[5.9].

A Doherty amplifier combines the output power of a Class-AB main amplifier and a Class-C peak amplifier using the quarter-wave length transformers. In this study, a distortion-cancelled Doherty amplifier due to the distortion cancellation at the vector combination of the main and the peak amplifiers in Doherty configuration was newly proposed. Optimizing the main and the peak load impedance shift, a 330-W Doherty 28-V GaAs heterojunction FET (HJFET) amplifier with high efficiency and low distortion has been successfully developed

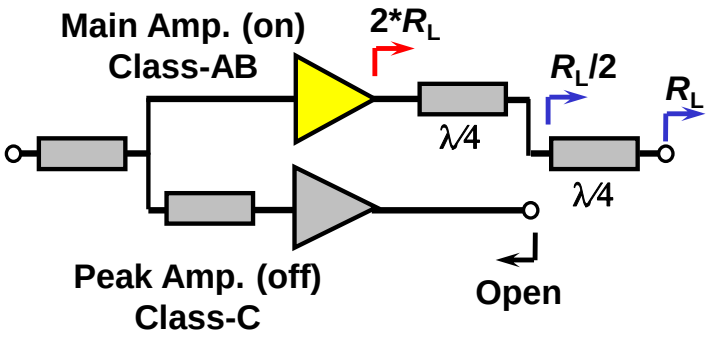
[5.10]. Furthermore, in order to clarify the distortion improvement mechanism, the evaluation technique to obtain each amplitude-to-amplitude modulation (AM-AM) and amplitude-to-phase modulation (AM-PM) characteristics of the main and the peak amplifiers in actual Doherty amplifier operation was proposed. For the first time, it was experimentally proved that the distortion cancellation of the main and the peak amplifiers contributes to improve the distortion characteristics in Doherty configuration. In addition, Doherty amplifier has the problem that IMD asymmetries occur due to the frequency characteristics of the power combining circuits in addition to the difference frequency influence. This study [5.11] analyzes the IMD3 asymmetries of the Doherty amplifier through the IMD3 vector combination of the main and the peak amplifiers by eliminating the difference frequency influence due to source and load baseband termination circuit technique. A newly developed 28-V-operation 200-W GaAs HJFET Doherty amplifier with source and load baseband terminations presents flat IMD3 characteristics against the Δf over 50 MHz.

5.2 Operation principle of Doherty amplifier

5.2.1 Basic operation of a 2-way Doherty amplifier

Figure 5.1 explains the basic operation of a 2-way Doherty amplifier. A 2-way Doherty amplifier combines the output power of a Class-AB main amplifier and a Class-C peak amplifier using the quarter-wave length transformers. At low input power level, since the peak amplifier is turned off, the peak amplifier side seems to be open. At that time, the main amplifier operates with two-times as high as load impedance due to the impedance inverter effect of the quarter-wave length transformer connected to the main amplifier. According to the increase of input power level, since the peak amplifier is turned on, the peak amplifier seems to be connected. Then the main amplifier load impedance shifts to be a half. As a result, the Doherty amplifier is expected to provide high efficiency operation in 6dB back-off region. In this way, the Doherty amplifier can provide high efficiency operation in large back-off region maintaining high output power. This is well-known Doherty operation. However, the Doherty configuration using a Class-C peak amplifier commonly has poor distortion characteristics problem because of non-constant gain and phase behavior. In this study, this problem has been overcome.

(a) Low input power level (Peak-OFF)



(b) High input power level (Peak-ON)

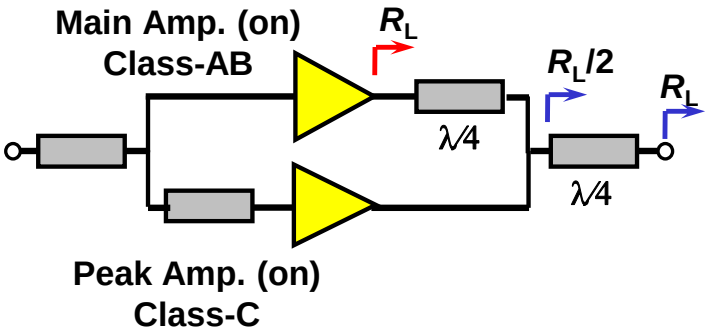


Fig. 5.1 Operation principal of a Doherty amplifier. (a) Low input power level and (b) high input power level.

5.2.2 Function of a Doherty network

As shown in Fig. 5.2, the two-way Doherty network composed of the two quarter-wave lines with the characteristics impedance of Z_1 and Z_2 is considered. Regarding the Doherty amplifier combining the main and the peak amplifiers with which the termination impedances are R_{L1} and R_{L2} at the high input level, respectively, the power-combining condition at the high input level, i.e., the peak amplifier is ON, is expressed as the following formula (5.1) with the system impedance of Z_0.

$$\frac{\frac{Z_1^{\,2}}{R_{L1}}R_{L2}}{\left(\frac{Z_1^{\,2}}{R_{L1}}+R_{L2}\right)}=\frac{Z_2^{\,2}}{Z_0} \tag{5.1}$$

Furthermore, when the two-way Doherty network is the equipartition circuit satisfying the condition (5.2) to combine the output power of the main and the peak amplifiers in equal ratio,

$$\frac{Z_1^{\,2}}{R_{L1}} = R_{L2} \tag{5.2}$$

the characteristic impedances of the two quarter-wave lines is represented as the following expressions (5.3), (5.4), respectively.

$$Z_1 = \sqrt{R_{L1} \cdot R_{L2}} \tag{5.3}$$

$$Z_2 = \sqrt{\frac{Z_0 \cdot R_{L2}}{2}} \tag{5.4}$$

Since it is assumed that the output impedance (R_{L2}) of peak amplifier is high enough at the low input level, i.e., the peak amplifier is OFF, the equivalent circuit as shown in Fig. 5.2 (b) is considered. Therefore, the termination impedance X of the main amplifier at the low input level is expressed as the formula (5.5).

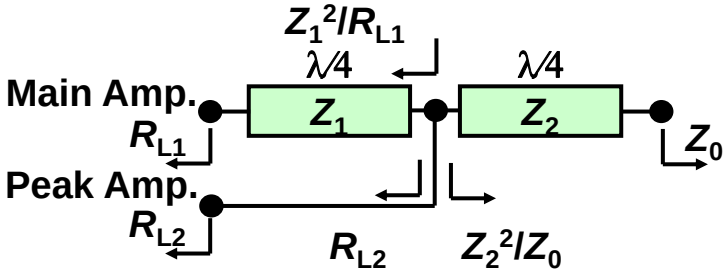
$$X = \frac{Z_1^{\,2}}{Z_2^{\,2}} Z_0 \tag{5.5}$$

Substituting the formula (5.3) and (5.4) to (5.5), the equation (5.6) is obtained.

$$X = 2R_{L1} \tag{5.6}$$

When the two-way Doherty network is configured with the equipartition circuit, the load impedance shift ratio n of the main amplifier against the ON/OFF of the peak amplifier is 2. In other words, the load impedance of the main amplifier shifts from high impedance to low impedance according to the increase of input level as shown in Fig. 5.3. Thereby, high efficiency operation at near the output power level of 6-dB back-off from the saturation output power of the amplifier can be expected as the case of n = 2 shown in Fig. 5.4.

(a) High input power level (Peak-ON)



(b) Low input power level (Peak-OFF)

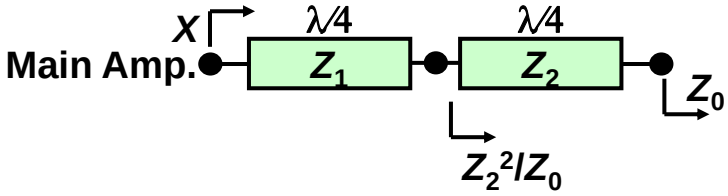


Fig. 5.2 Two-way Doherty network. (a) High input power level and (b) low input power level.

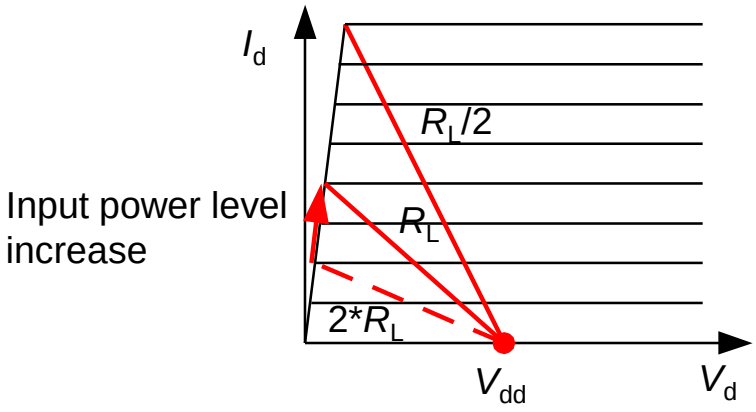


Fig. 5.3 Load impedance shift in Doherty amplifier.

Moreover, when the two-way Doherty network is the unequal distribution circuit, satisfying the power-combining conditions of (5.1), Z_1 and Z_2 become the following formula, (5.7), (5.8), respectively. Where n is the load impedance shift ratio of the main amplifier against the ON/OFF of the peak amplifier.

$$Z_1 = \sqrt{(n-1)\cdot R_{L1}\cdot R_{L2}} \tag{5.7}$$

$$Z_2 = \sqrt{\frac{(n-1)\cdot R_{L2}}{n}} \tag{5.8}$$

Here,

$$X = \frac{Z_1^{\,2}}{Z_2^{\,2}} Z_0 = nR_{L1} \tag{5.9}$$

is assumed.

When the back-off amount x is defined as the ratio of the output voltage V_0 and the saturation output voltage $V_{\max}$, the relation of the drain efficiency and the back-off in the two-way Doherty amplifier is represented as the following expressions using the maximum efficiency of Class-B operation and the n.

$$\eta_d = \frac{\pi}{4} n \cdot x, \qquad 0 < x < \frac{1}{n} \tag{5.10}$$

$$\eta_d = \frac{\pi}{4} \frac{n}{n+1} \cdot \frac{x^2}{x-1}, \qquad \frac{1}{n} < x < 1 \tag{5.11}$$

By $n = 3$, the efficiency near 9.5 dB back-off level can be improved as shown in Fig. 5.4.

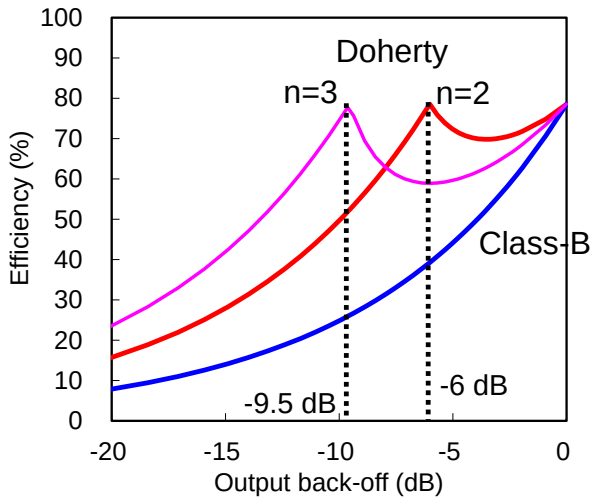


Fig. 5.4 Drain efficiency versus output back-off.

In contrast, as shown in Fig. 5.5, the input network constitutes an inverted Doherty network of which a quarter-wave impedance line is connected to the peak amplifier opposite to the Doherty network. If both of the power-combining condition (5.12) and the equipartition condition (5.13) are imposed on the inverted Doherty network, the load impedance shift ratio of the input-side of the main amplifier becomes 1/2.

$$\frac{\frac{Z_1^{\ 2}}{R_{L2}}R_{L2}}{(\frac{Z_1^{\ 2}}{R_{L2}}+R_{L1})}=\frac{Z_2^{\ 2}}{Z_0} \tag{5.12}$$

$$\frac{Z_1^{\ 2}}{R_{L2}}=R_{L1} \tag{5.13}$$

The following formulas are obtained.

$$Z_1=\sqrt{R_{L1}\cdot R_{L2}} \tag{5.14}$$

$$Z_2=\sqrt{\frac{Z_0\cdot R_{L1}}{2}} \tag{5.15}$$

$$X=\frac{Z_2^{\ 2}}{Z_0}=\frac{R_{L1}}{2} \tag{5.16}$$

That is, when the input network is an equipartition circuit, an amplifier will always be in the state of input-mismatching at a small signal condition. Therefore, the Doherty amplifier composed of an equipartition circuit has a problem that the small-signal gain decreases.

In the inverted Doherty network, the following formulas (5.17), (5.18), (5.19) are obtained supposing to fulfill only the power-combining condition. Where n is the load impedance shift ratio of the main amplifier against the ON/OFF of the peak amplifier.

$$Z_1=\sqrt{\frac{n\cdot R_{L1}\cdot R_{L2}}{(1-n)}} \tag{5.17}$$

$$Z_2=\sqrt{n\cdot R_{L1}\cdot Z_0} \tag{5.18}$$

$$X=\frac{Z_2^{\ 2}}{Z_0}=nR_{L1} \tag{5.19}$$

At this time, $0<n<1$ is necessary. That is, when the inverted Doherty network is used for the output side, the load impedance of a main amplifier shifts from low impedance to high impedance according to the increase of input level. This presents the shift opposite to the Doherty network.

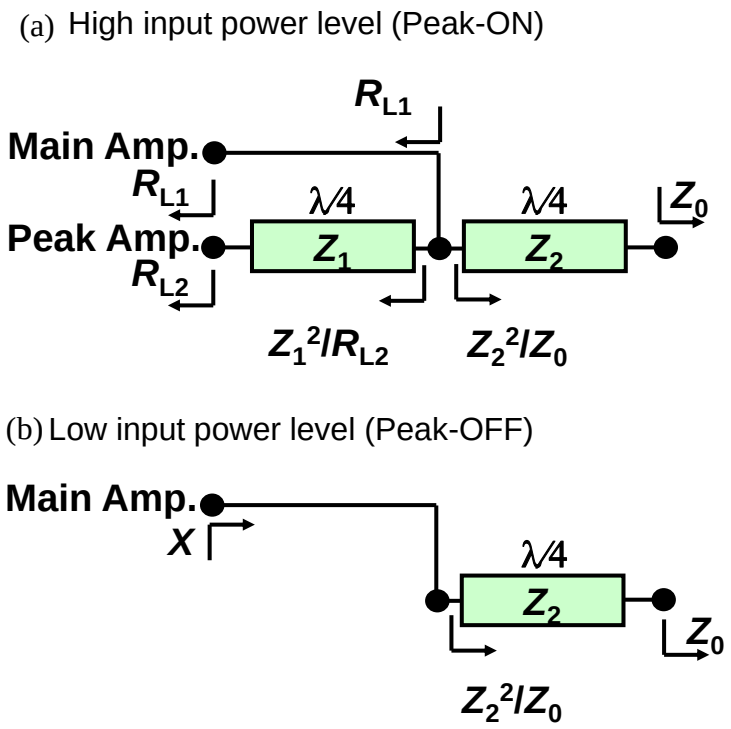


Fig. 5.5 Inverted Doherty network. (a) High input power level and (b) low input power level.

5.3 28-V-operation 150-W single-ended GaAs HJFETs

The device structure of 28-V-operation AlGaAs/InGaAs/AlGaAs HJFET [5.12] was described in Section 3.6.1. Figure 5.6 shows the top view of newly developed 28-V-operation 150-W single-ended HJFETs. The gate width (W_g) of a chip with 20 unit cells was 82 mm. The unit finger width was 1000 μm. Three Dual-FPFET chips (i.e. total $W_g = 3 \times 82$ mm) were mounted on a single plastic package with pre-matching circuits. The package size is 21.7×34 mm^2. Figure 5.7 shows the equivalent circuit of a 150-W GaAs HJFET. The internal matching circuits employ the harmonic termination techniques described in Chapter 3 for high efficiency operation. The internal input matching circuit consists of two-stage *LC* low pass filter networks in order to realize short condition for the second harmonic source impedance, and the internal output matching circuit consists of transmission lines and one-stage *LC* low pass filter networks in order to realize open condition for the second harmonic load impedance.

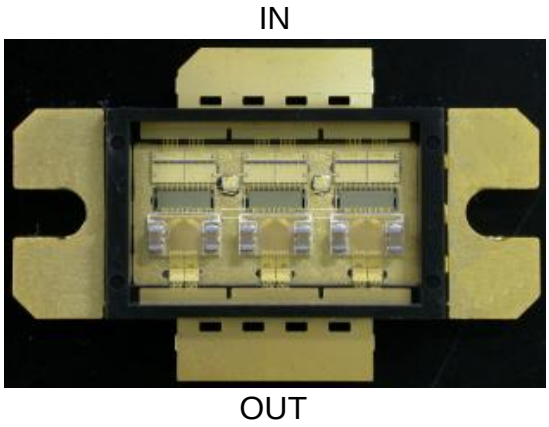


Fig. 5.6 Top view of a newly developed 28-V-operation 150-W GaAs HJFET.

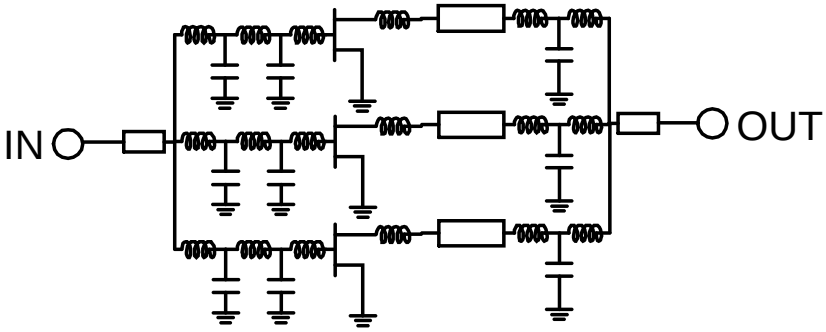


Fig. 5.7 Equivalent circuit of a 150-W GaAs HJFET.

5.4 High efficiency and low distortion circuit design of a Doherty amplifier

5.4.1 Circuit design strategy of Doherty amplifier

As shown in Fig. 5.8, both of the Class-AB main amplifier and the Class-C peak amplifier on a Doherty configuration are not isolated each other. Therefore, it is serious problem to robustly design the optimum load impedance shift presented to both the FETs for high efficiency and low distortion [5.8]. Figure 5.9 shows our circuit design strategy. First, for more accurate design, using the load-pull measurement, the optimum load impedance of the FETs was confirmed as a function of input power level in Class-AB and Class-C, respectively. Next, utilizing large signal simulation, the load impedance shift presented to the main and the peak amplifier FETs was simultaneously optimized as a function of input power level.

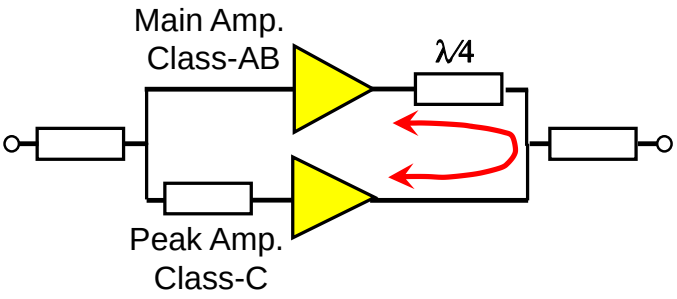


Fig. 5.8 Doherty configuration.

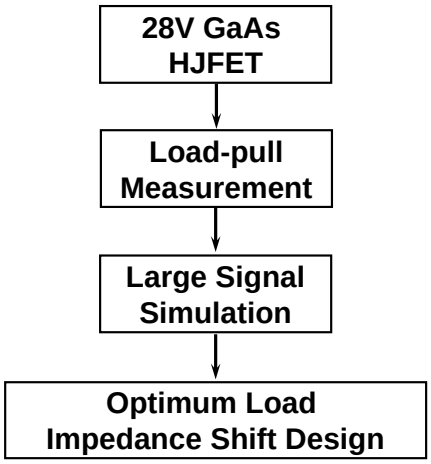


Fig. 5.9 Circuit design strategy.

5.4.2 Main amplifier design

For a main amplifier design, the load-pull characteristics were measured as a function of input power level in Class-AB. Figure 5.10 shows measured power-added efficiency (PAE) contours and measured output power (P_{out}) contours at the 2-dB gain compression point under a continuous wave (CW) of 2 GHz for a unit cell FET. In order to achieve high efficiency operation, the main amplifier load impedance should be designed to change from maximum PAE (PAE_{max}) point to maximum P_{out} ($P_{out,\ max}$) point as an arrow in Fig. 5.10 according to the increase of input power level. Furthermore, Fig. 5.11 shows measured adjacent leakage power ratio (ACPR) contours at the constant P_{out} of around 10-dB output back-off (B.O.) under a W-CDMA signal of 2 GHz. As shown in Fig. 5.11, PAE matching point is close to the low distortion matching point. Therefore, low distortion operation can be expected in addition to high efficiency operation for main amplifier.

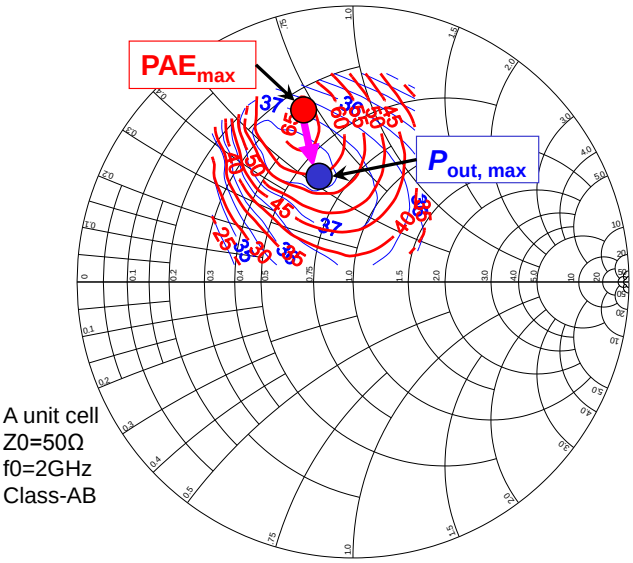


Fig. 5.10 Measured PAE contours and P_{out} contours at the 2-dB gain compression point in Class-AB under a CW of 2 GHz for a unit cell FET.

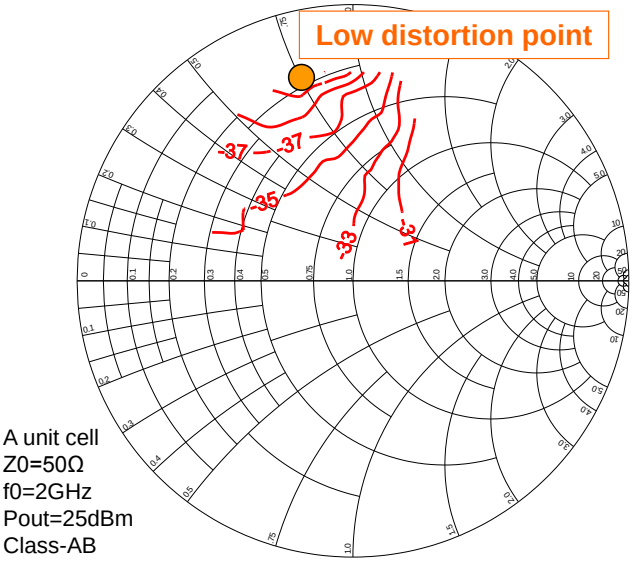


Fig. 5.11 Measured ACPR contours at the constant P_{out} of around 10-dB output B.O. in Class-AB under a W-CDMA signal of 2 GHz.

5.4.3 Peak amplifier design

Next, for a peak amplifier design, the gain contours were measured as a function of input power level in Class-C. Figure 5.12 shows measured gain contours at the small signal and the saturated output power (P_{sat}) level in Class-C for a unit cell FET under a CW of 2 GHz. The maximum gain point (Gain$_{max}$) at the P_{sat} level in Class-C moves to the same point as the $P_{out, max}$ point in Class-AB. Figure 5.13 (a) and (b) show measured AM-AM and AM-PM characteristics at the small signal Gain$_{max}$ point and the $P_{out, max}$ point in Class-C at 2 GHz. The small signal Gain$_{max}$ point shows very small AM-AM and AM-PM variation,

compared to the $P_{out,\,max}$ point. Therefore, in order to minimize the gain expansion of the peak amplifier, the peak amplifier load impedance should keep the small signal $Gain_{max}$ point in Class-C according to the increase of input power level. Finally, the peak amplifier load impedance should shift to the $P_{out,\,max}$ point to gain the P_{sat} as an arrow in Fig. 5.12 according to the increase of input power level. Thus, low distortion operation can be expected by minimizing the gain expansion of the peak amplifier.

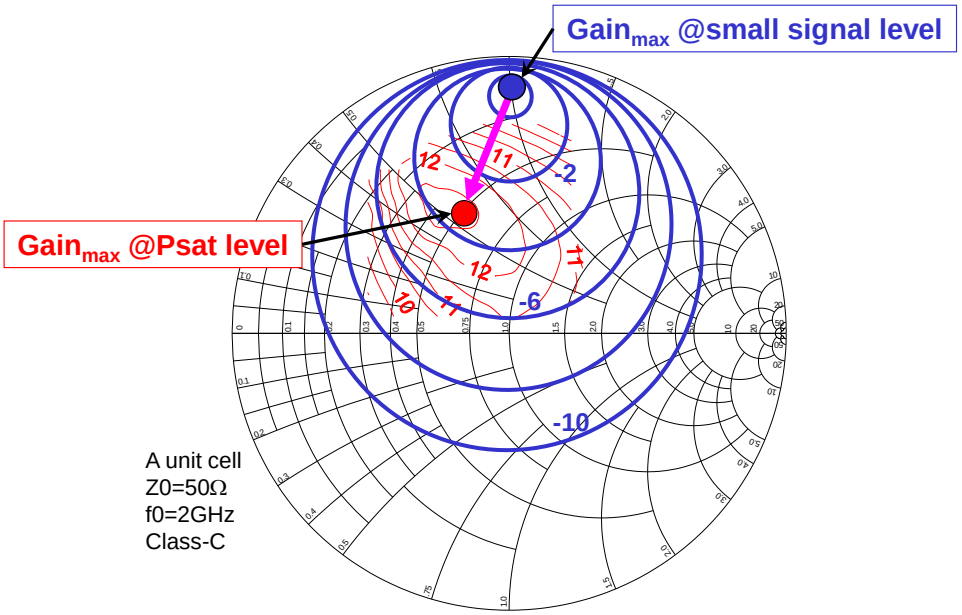


Fig. 5.12 Measured gain contours at the small signal and the *P*sat level in Class-C for a unit cell FET under a CW of 2 GHz.

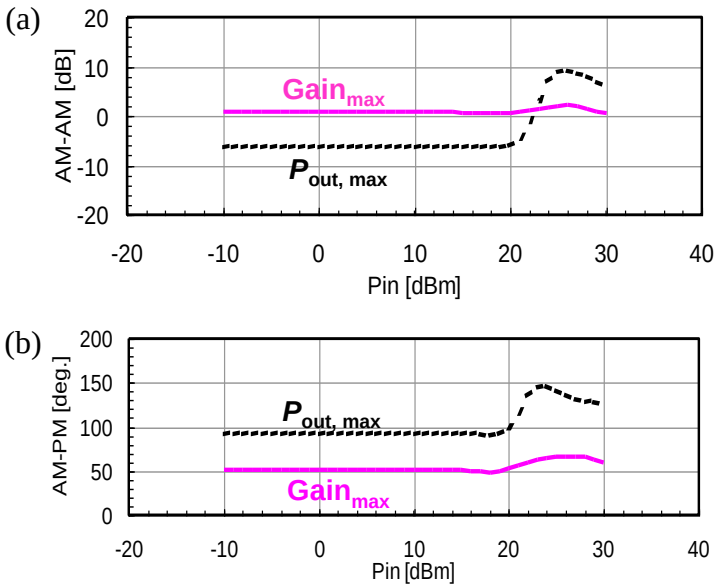


Fig. 5.13 Measured (a) AM-AM and (b) AM-PM characteristics at the small signal gain matching point and the maximum P_{out} point in Class-C at 2 GHz.

5.4.4 Selection of inverted Doherty circuit configuration

From the load-pull measurement for a unit cell, it was presented that, in order to obtain high efficiency and low distortion, the main amplifier load impedance should change from the PAE_{max} point to the $P_{out,\ max}$ point at Class-AB, and the peak amplifier load impedance should shift from the small signal $Gain_{max}$ point in Class-C to the $P_{out,\ max}$ point, according to the increase of input power level. Figure 5.14 shows the location of measured PAE_{max} point and measured $P_{out,\ max}$ point for a unit cell 28-V HJFET in order to select the Doherty circuit configuration. It is found that the PAE_{max} impedance is lower than the $P_{out,\ max}$ impedance. In this case, as shown in Fig. 5.14 (a), the inverted Doherty configuration of which the quarter wave length ($\lambda/4$) transformer is connected to the output of the peak amplifier is suitable to realize the load impedance shift from low impedance to high impedance according to the increase of input power level. As mentioned in the operation principle of the original Doherty configuration shown in Fig. 5.14 (b), the load-line of the main amplifier changes from high impedance to low impedance according to the increase of input power level. As shown in Fig. 5.14, although the real part of the impedance in the region (A) is lower than that of $P_{out,\ max}$ point, the load-line introduced by the *RC* parallel model is higher than that of $P_{out,\ max}$ point. That is to say, on the load impedance shift from the PAE_{max} point to the $P_{out,\ max}$ point for 28-V HJFET according to the increase of input power level, the load-line changes from high impedance to low impedance in the same way as the Doherty operation principle.

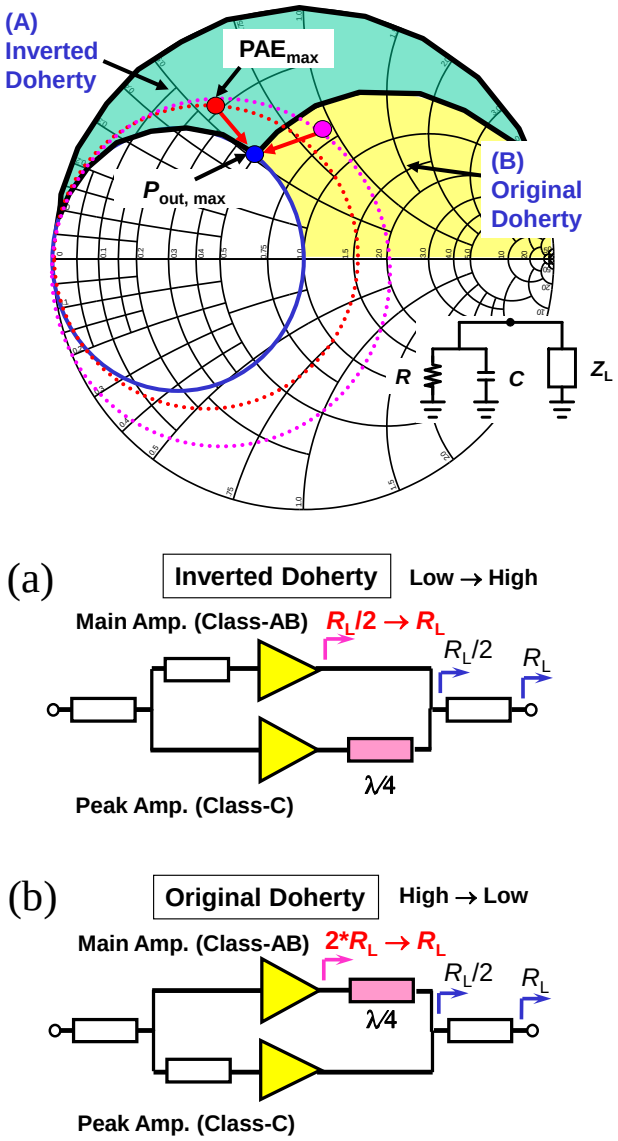


Fig. 5.14 Location of measured PAEmax point and measured P_{out}, max point to select the Doherty circuit configuration. (a) Inverted Doherty configuration. (b) Original Doherty configuration.

5.4.5 Optimum load impedance shift design

Figure 5.15 shows the basic configuration of the developed Doherty amplifier. Note that the main and the peak amplifiers of Fig. 5.15 are replaced up and down against the principle configuration of Fig. 5.1. This Doherty amplifier is composed of a main amplifier and a peak amplifier employing a pair of developed 150-W 28-V GaAs HJFETs. The output power of the main and the peak amplifiers was combined employing the inverted Doherty network with the λ/4 transformers of 50 Ω and 35 Ω. A 90°-hybrid coupler is used in the input circuits to achieve the distortion bandwidth characteristics improvement isolating each other's input signals of the main and the peak amplifiers. The load impedance shift of the

main and the peak amplifiers affects each other. Therefore, utilizing large signal model (EEHEMT1), the output matching circuits with the internal matching networks (IMNs) and the external matching networks (EMNs) were designed in order to simultaneously optimize the load impedance shift presented to both the main and the peak amplifier FETs as a function of input power level.

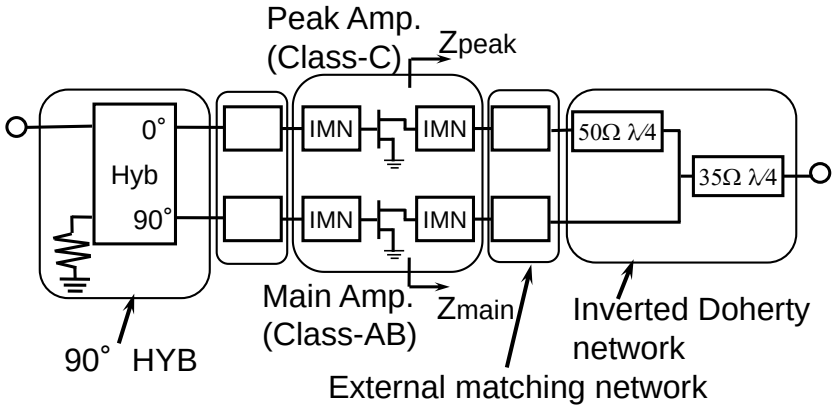


Fig. 5.15 Basic configuration of the developed Doherty amplifier.

As shown in Fig. 5.16, the initial output circuit parameters were determined to simultaneously satisfy the optimum impedance of both the small signal and the large signal condition minimizing the output return loss. The phase-adjusting lines of 50 Ω were inserted between the EMNs and the Doherty network in order to be easy to match.

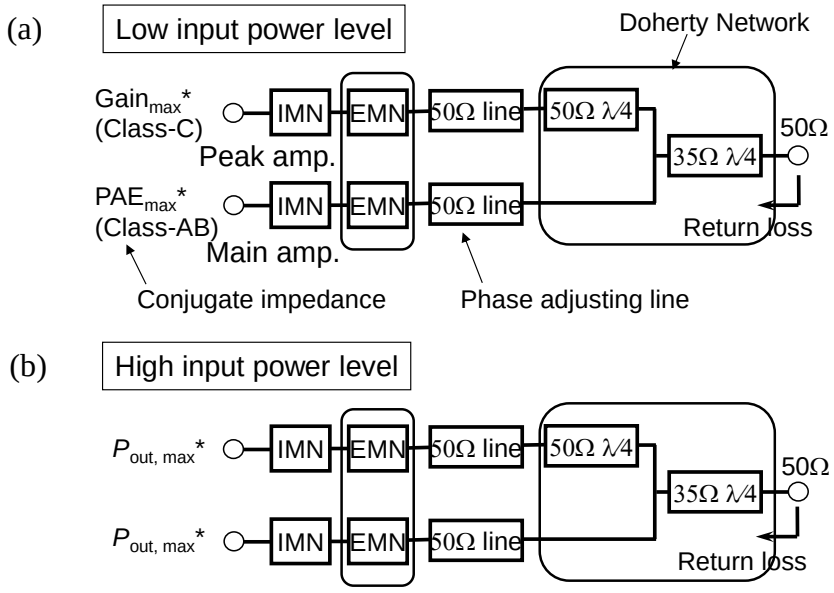


Fig. 5.16 Initial output circuit parameter optimization at (a) low input power level and (b) high input power level.

Figure 5.17 shows the results of simulated optimum load impedance shift for a unit cell. The load impedance of the Class-AB main amplifier FETs is changed from the PAE_{max} point to the $P_{out, max}$ point according to the increase of input power level. The Class-C peak

amplifier FETs load impedance shift is changed from the $Gain_{max}$ point to the $P_{out,\,max}$ point according to the increase of input power level.

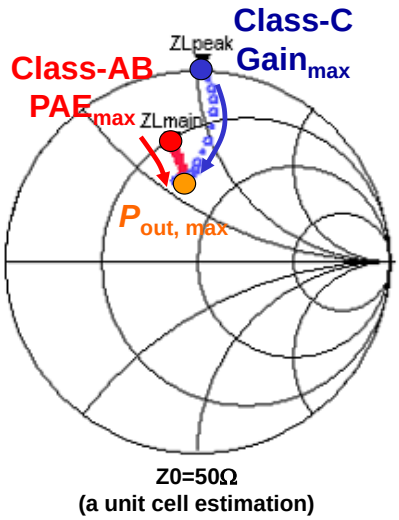


Fig. 5.17 Simulated optimum load impedance shift of the main and the peak amplifier FETs changing input power level.

Figure 5.18 shows AM-AM and AM-PM characteristics calculated against the main and the peak amplifier FETs. Above all, suppressed AM-AM and AM-PM variation of the peak amplifier FETs is effective to low distortion characteristics of overall amplifier. Behaviors around the 8-dB back-off level are crucial under the W-CDMA signal conditions.

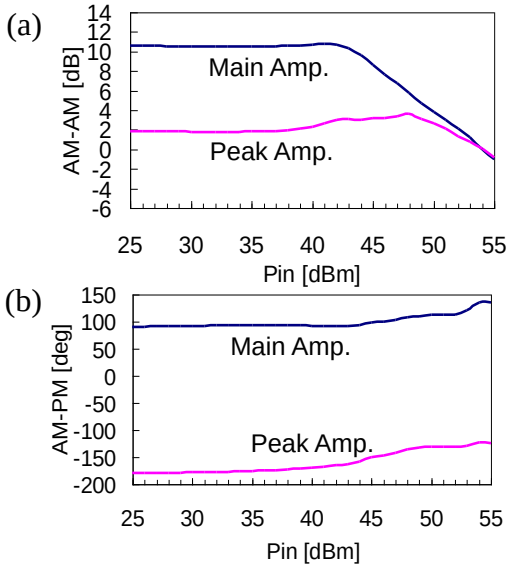


Fig. 5.18 Simulation results of (a) AM-AM and (b) AM-PM characteristics about the main and the peak amplifier FETs.

Figure 5.19 shows the load-line simulated about the main and the peak amplifier FETs at the input power levels of the 8-dB back-off level and the P_{sat} level. It is found that the load-

line of the main amplifier FETs changes from high impedance to low impedance in the inverted Doherty amplifier according to the increase of input power level.

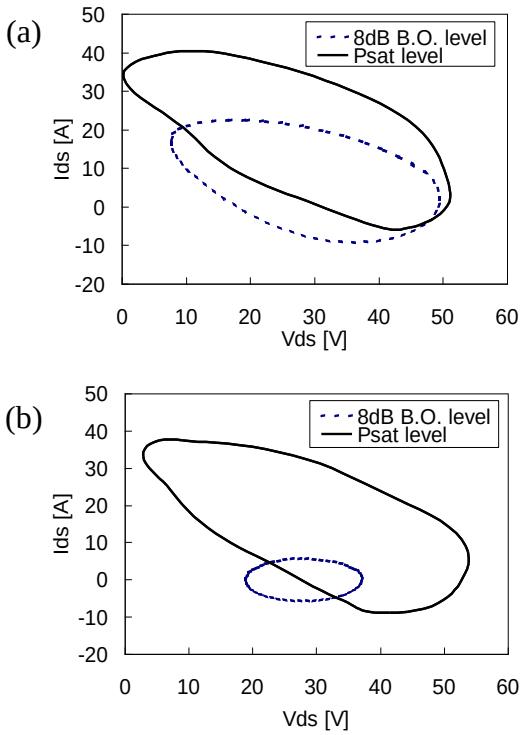


Fig. 5.19 Simulated load-line about the main and the peak amplifier FETs at the input power levels of the 8dB B.O. level and the *P*sat level. (a) Load-line of the main amplifier FETs. (b) Load-line of the peak amplifier FETs.

5.5 Measured RF performance of distortion cancelled Doherty amplifier

A photograph of the developed Doherty amplifier is shown in Fig. 5.20. External circuits including Doherty networks and bias circuits were formed on a printed Teflon board with thickness of 0.8 mm. A ceramic chip 90º-hybrid coupler was used at the input circuits. The main amplifier was biased at a drain-source voltage (V_{ds}) of 28 V with a quiescent drain-source current (I_{dsq}) of 1.2 A. The bias condition of the peak amplifier was a V_{ds} of 28 V and a gate-source voltage (V_{gs}) of −1.2 V, which is Class-C bias condition. W-CDMA signal condition is 3GPP test model 64ch with a peak-to-average power ratio (PAR) of 8 dB at 0.01% on the complementary cumulative distribution function (CCDF).

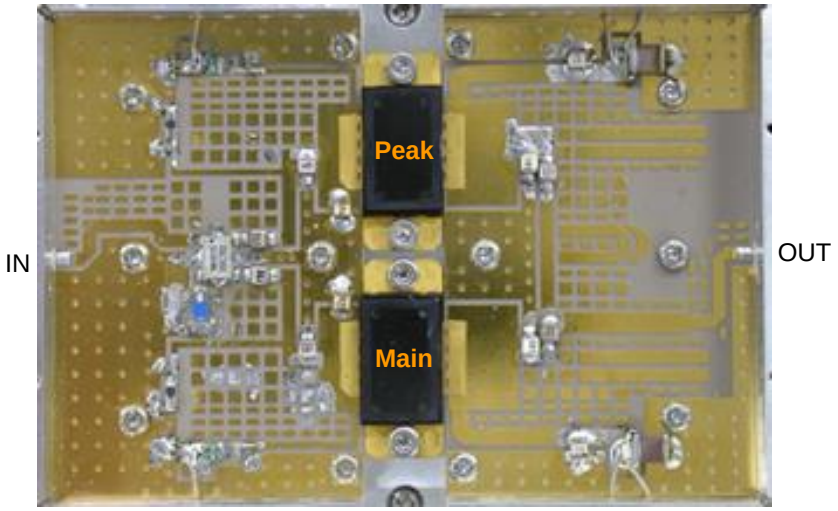


Fig. 5.20 Photograph of the developed Doherty amplifier.

Figure 5.21 shows the P_{out} versus the input power (P_{in}) characteristics under the pulsed CW condition with the pulse-width of 8 μsec and the pulse-period of 1msec within the UMTS band (2.11 GHz to 2.17 GHz). The developed Doherty amplifier attained superior output-power bandwidth characteristics. It demonstrated a P_{sat} of 55.2 dBm (P_{in} = 45 dBm) and a 14-dB linear gain (P_{in} = 30 dBm) at 2.14 GHz.

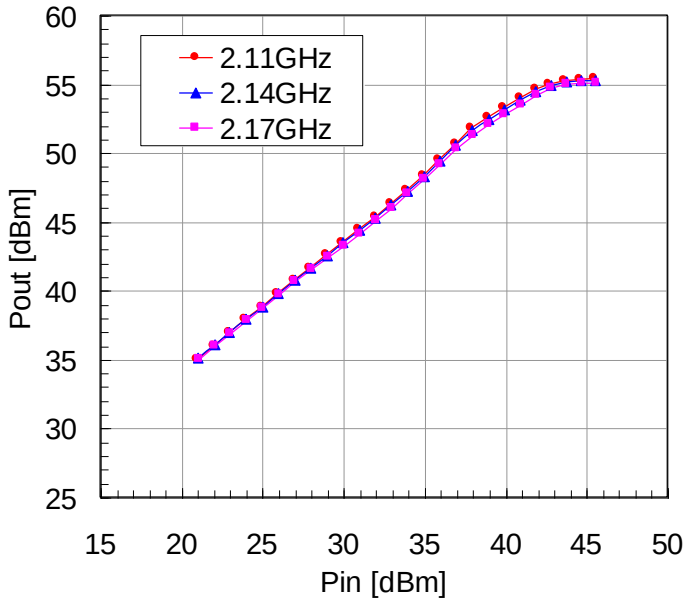


Fig. 5.21 Pulsed CW performance of the developed Doherty amplifier within the UMTS band (2.11 GHz to 2.17 GHz).

Figure 5.22 also presents the performance of the developed Doherty amplifier with the two-carrier W-CDMA signals of 10-MHz carrier spacing at three center-frequencies of 2.12 GHz, 2.14 GHz, and 2.16 GHz. Under the W-CDMA signal conditions, excellent bandwidth characteristics of distortion and efficiency were obtained in the UMTS band. The amplifier exhibited low third order intermodulation (IM3) characteristics of less than

−37.5 dBc with a 37% drain-efficiency at an average P_{out} of 47 dBm around the 8-dB B.O. output power level using two-carriers of 2.135 GHz and 2.145 GHz. It also revealed low fifth order intermodulation (IM5). Moreover, at an average P_{out} of 49 dBm around the 6-dB B.O. level, it delivered a 42% drain-efficiency maintaining −37-dBc IM3. To author's knowledge, these are the best values ever reported among the simple high power FET amplifiers for W-CDMA base stations [5.13]-[5.15].

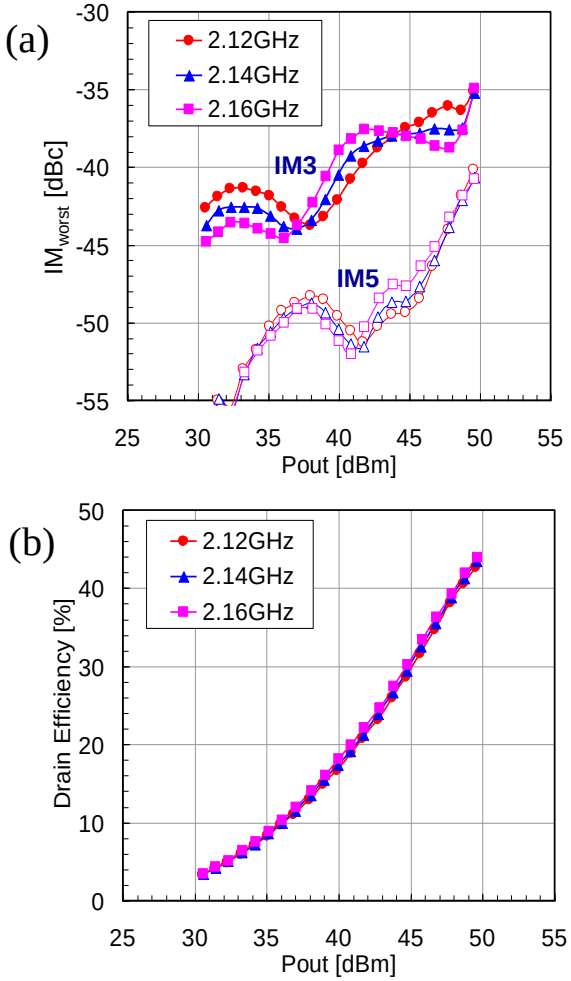


Fig. 5.22 Performance of the developed Doherty amplifier with the two-carrier W-CDMA signals of 10-MHz carrier spacing at three center-frequencies (2.12 GHz, 2.14 GHz, and 2.16 GHz). (a) IM3 and IM5 versus P_{out}. (b) Drain efficiency versus P_{out}.

Figure 5.23 shows the peak amplifier V_{gs} dependence of the two-carrier W-CDMA signals performance with 10-MHz carrier spacing (2.135 GHz and 2.145 GHz). Biasing the peak amplifier V_{gs} in −1.3 V, the amplifier reached a 43.5% drain-efficiency at an average P_{out} of 49 dBm with no degradation in distortion.

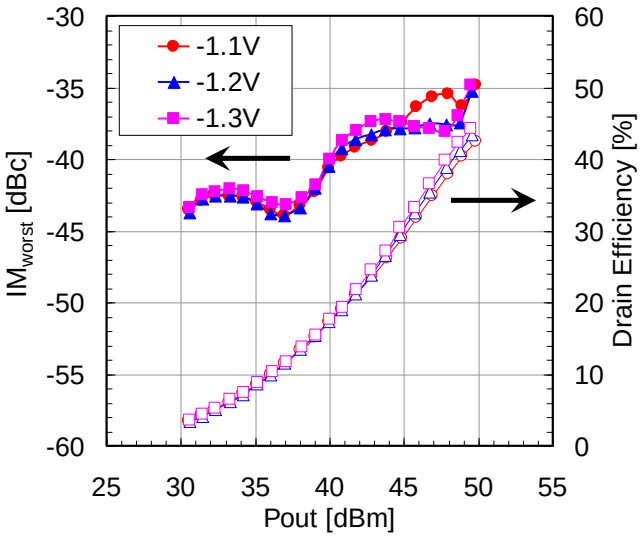


Fig. 5.23 Peak amplifier *V*gs dependence of the two-carrier W-CDMA signals performance with 10 MHz carrier spacing (2.135 GHz and 2.145 GHz).

Figure 5.24 shows the correlation between IM3 and drain efficiency with two-carrier W-CDMA signals of the Doherty amplifier versus the Class-AB push-pull configuration. The developed Doherty amplifier greatly improved trade-off between distortion and efficiency. It has the capability to provide both high efficiency and low distortion characteristics.

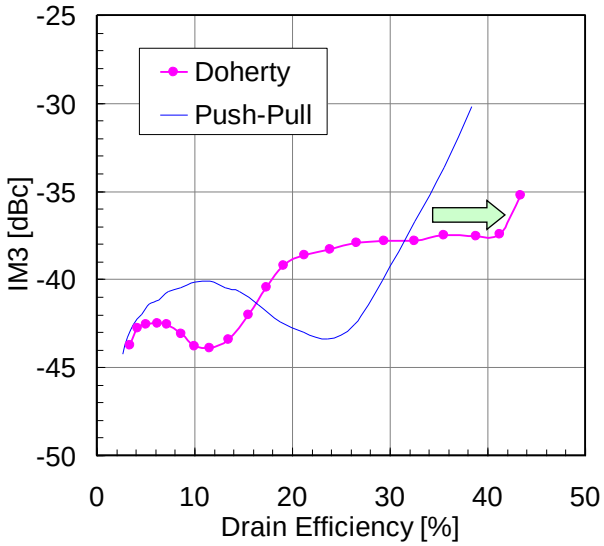


Fig. 5.24 Correlation between IM3 and drain efficiency with two-carrier W-CDMA signals of the Doherty amplifier and the push-pull amplifier.

5.6 Verification of the distortion improvement mechanism on a Doherty amplifier

Developed GaAs FET Doherty amplifier could improve efficiency with no degradation of distortion characteristics. Figure 5.25 shows the distortion improvement mechanism due to the distortion cancellation at the vector combination of the main and the peak amplifiers in Doherty configuration. If the distortion cancellation of the main and the peak amplifiers contributes to the distortion improvement, the extremely flat AM-PM characteristics are expected to be obtained without the phase deviation at the vector combination of the main and the peak amplifiers output voltage.

The voltage amplitude (r_d) and the phase (Φ_d) of the combination vector can be expressed as follows (5.20).

$$r_d = \sqrt{r_m^{\,2} + r_p^{\,2} + 2r_m r_p \cos(\Phi_m - \Phi_p)}$$
$$\tan\Phi_d = \frac{r_m \sin\Phi_m + r_p \sin\Phi_p}{r_m \cos\Phi_m + r_p \cos\Phi_p} \tag{5.20}$$

where r_m and Φ_m are the amplitude and the phase of the main amplifier output voltage, respectively, r_p and Φ_p are the amplitude and the phase of the peak amplifier output voltage, respectively.

Here, it is necessary to pay attention that each AM-AM and AM-PM characteristics of the main and the peak amplifiers cannot be evaluated isolating each other of the main and the peak amplifiers so that the load impedance shifts of the main and the peak amplifiers are in need of the injection signals from each other.

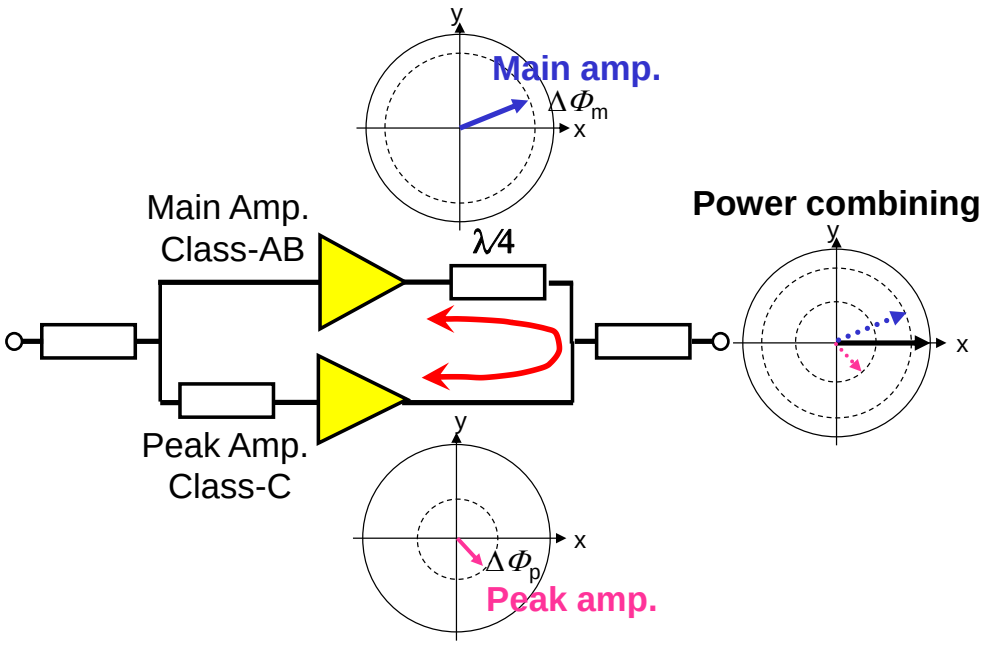


Fig. 5.25 Distortion improvement mechanism on a Doherty amplifier.

In order to verify the distortion improvement mechanism, the evaluation technique was proposed to obtain each AM-AM and AM-PM characteristics of the main and the peak amplifiers in actual Doherty amplifier operation. Figure 5.26 shows the measurement system employing three 90º-hybrid couplers in the input circuits without isolating each other of the main and the peak amplifiers. Operating the Doherty amplifier by inputting the large signal of f_1 = 2.141 GHz (P_{in} = 22~47 dBm) to one 90º-hybrid coupler, the forward transducer gain characteristics of the main and the peak amplifiers, respectively, were obtained by inputting the small signal of f_2 = 2.14 GHz (P_{in} = 2~27 dBm) from a vector network analyzer (VNA) to the other 90º-hybrid couplers.

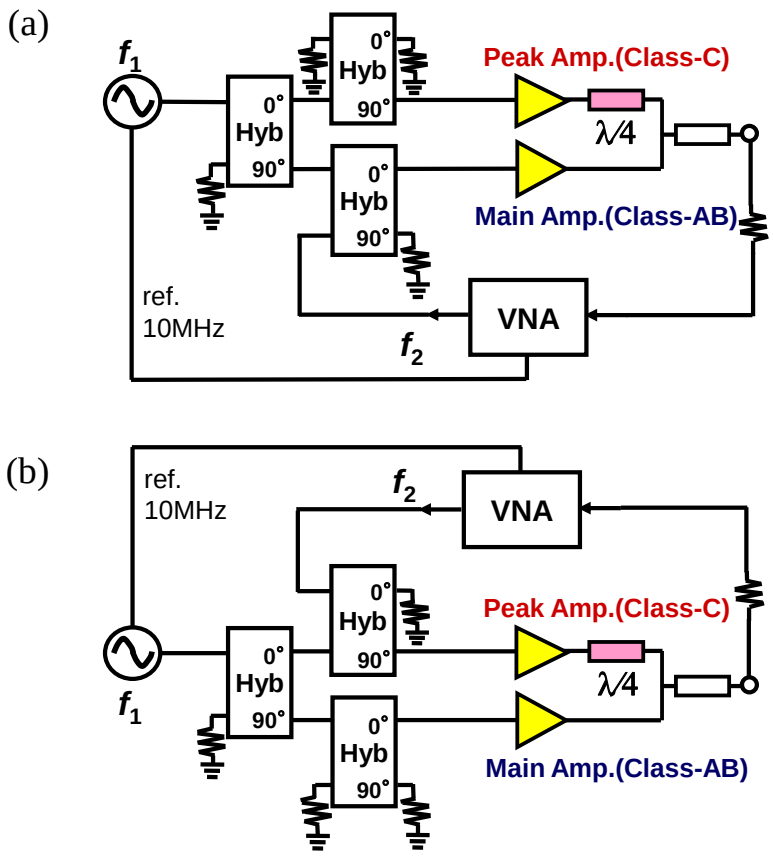


Fig. 5.26 Measurement system of AM-AM and AM-PM characteristics of the main and the peak amplifier in an operating Doherty amplifier. (a) Main amplifier measurement configuration. (b) Peak amplifier measurement configuration.

Figure 5.27 shows the measured AM-AM and AM-PM characteristics of the main and the peak amplifiers, and the vector combination calculated from the formula (5.20). In particular, it was observed that the AM-PM characteristics of the main and the peak amplifiers on an actual Doherty amplifier are significantly different from the results of the Class-AB and the Class-C single-ended device shown in Fig. 5.28. Furthermore, as shown in Fig. 5.27, the output voltage combination of the main and the peak amplifiers exhibited flat AM-PM characteristics in accordance with the results of the overall Doherty amplifier. From these results, it was confirmed that the distortion cancellation of the main and the peak amplifiers contributes to the distortion improvement. It also can be said that the optimum load impedance shift condition estimated about the main and the peak amplifiers is equivalent to the distortion cancellation condition of the main and the peak amplifiers on a GaAs FET Doherty amplifier.

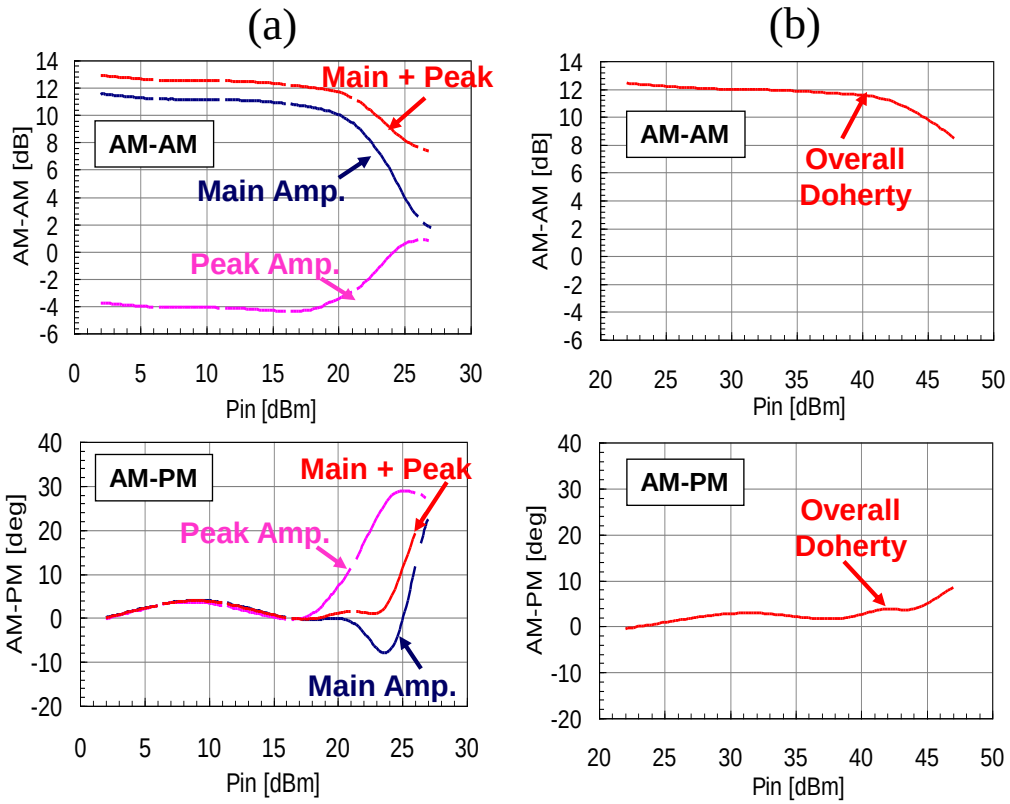


Fig. 5.27 Measured AM-AM and AM-PM characteristics of (a) the main and the peak amplifiers, the vector combination, and (b) the total Doherty amplifier.

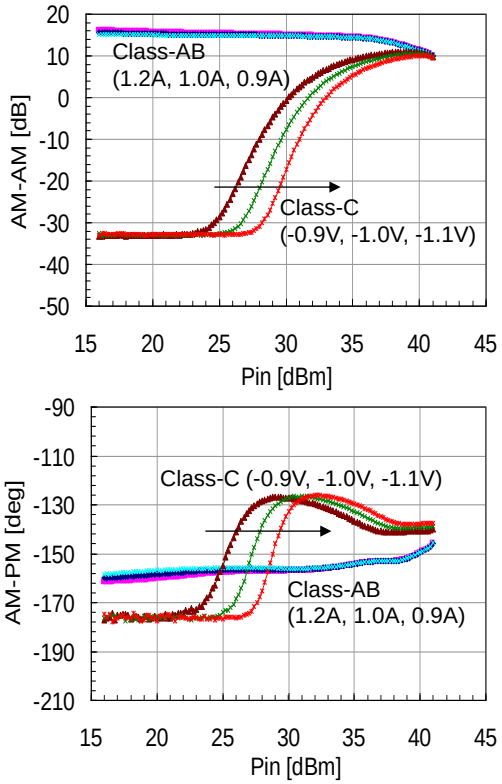


Fig. 5.28 Measured AM-AM and AM-PM characteristics of the Class-AB and the Class-C single-ended device (power-matched).

5.7 IMD asymmetries of a Doherty amplifier

Doherty amplifier combines a Class-AB main amplifier and a Class-C peak amplifier with mutually different distortion characteristics. Therefore, it has the problem that IMD asymmetries occur due to the frequency characteristics of the power combining circuits in addition to the difference frequency influence. The IMD3 asymmetries of the Doherty amplifier were analyzed through the IMD3 vector combination of the main and the peak amplifiers by eliminating the difference frequency influence due to source and load baseband termination circuit technique described in Section 4.7.

5.7.1 IMD3 vector combination of main and peak amplifiers

As shown in Fig. 5.29, Doherty amplifier combines the output power of a Class-AB main amplifier and a Class-C peak amplifier through a λ/4 transformer which is related to the load impedance (R_L) shift of the main amplifier. In the same way, the distortion components of Doherty amplifier are expressed as the distortion vector combination of the main and the peak amplifiers, concerning the frequency characteristics of the output power combining circuits composed of λ/4 transformers with output power dependence. Here, each of the amplifiers in Doherty amplifier is assumed to present no IMD3 asymmetries alone. Figure 5.30 shows the schematic diagrams of the distortion vector combination of the main and the peak amplifiers having different distortion components each other.

The upper and the lower IMD3 vector components of a main amplifier are expressed as

$$IMD3_U(main) = \vec{a}_1,\ IMD3_L(main) = \vec{a}_2 \tag{5.21}$$

The upper and the lower IMD3 vector components of a peak amplifier are expressed as

$$IMD3_U(peak) = \vec{b}_1,\ IMD3_L(peak) = \vec{b}_2 \tag{5.22}$$

Here, the phase angles between the IMD3 vectors of the main and the peak amplifiers are expressed as θ_1 and θ_2 in the upper and the lower part, respectively. If the phase deviation $\Delta\theta$ between the upper IMD3 and the lower IMD3 occurs by the combination of the main and the peak amplifiers, θ_1 and θ_2 are expressed as follows:

$$\theta_1 = \theta_0 + \Delta\theta\,,\ \theta_2 = \theta_0 - \Delta\theta \tag{5.23}$$

where θ_0 is the original phase deviation of the main and the peak amplifiers before combination.

Then, the magnitude difference |ΔIMD3| of the upper and the lower IMD3 is expressed as

$$|\Delta IMD3| = \sqrt{\frac{|\vec{a}_1|^2 + |\vec{b}_1|^2 + 2|\vec{a}_1|\cdot|\vec{b}_1|\cos(\theta_0 + \Delta\theta)}{|\vec{a}_2|^2 + |\vec{b}_2|^2 + 2|\vec{a}_2|\cdot|\vec{b}_2|\cos(\theta_0 - \Delta\theta)}} \tag{5.24}$$

Furthermore, if the magnitude deviation $\Delta\gamma$ of the upper and the lower IMD3 occurs by the combination of the main and the peak amplifiers as follows:

$$|\vec{a}_1| = \Delta\gamma\,|\vec{a}_2|,\ |\vec{b}_1| = \Delta\gamma\,|\vec{b}_2| \tag{5.25}$$

, |ΔIMD3| is represented as

$$|\Delta IMD3| = \Delta\gamma\sqrt{\frac{|\vec{a}_2|^2 + |\vec{b}_2|^2 + 2|\vec{a}_2|\cdot|\vec{b}_2|\cos(\theta_0 + \Delta\theta)}{|\vec{a}_2|^2 + |\vec{b}_2|^2 + 2|\vec{a}_2|\cdot|\vec{b}_2|\cos(\theta_0 - \Delta\theta)}} \tag{5.26}$$

Thus, the IMD asymmetries of Doherty amplifier occur by the frequency characteristics of the output power combining circuits even if it is composed of the main and the peak amplifiers having no second-order distortion.

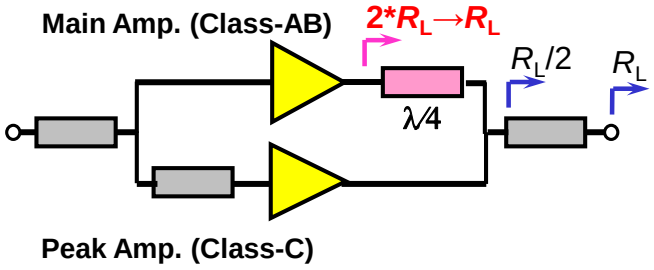


Fig. 5.29 Basic configuration of Doherty amplifier.

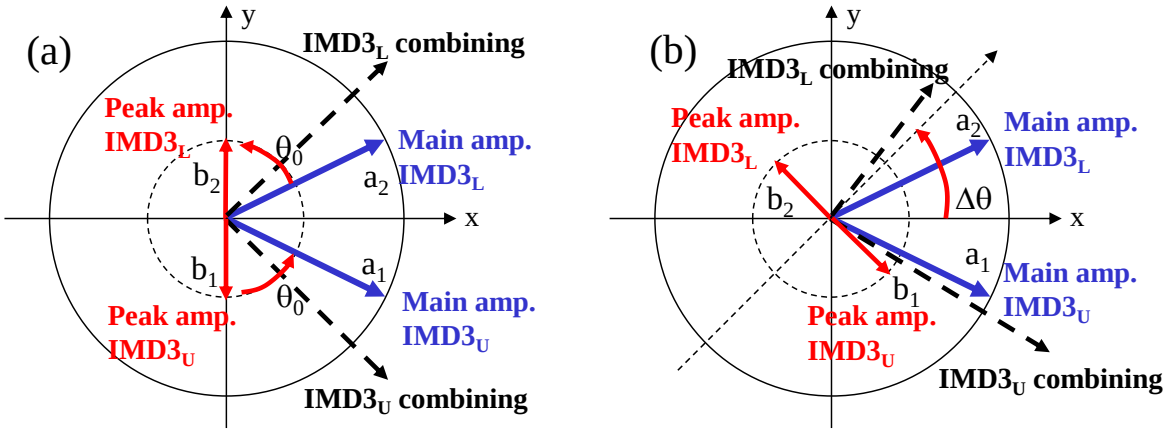


Fig. 5.30 Schematic diagrams of the distortion vector combination of the main and the peak amplifiers having different distortion components each other. (a) Equal phase combination. (b) Different phase combination.

5.7.2 Relationship between IMD3 asymmetries and circuit characteristics in a Doherty amplifier

In order to examine the relationship between IMD asymmetries and output circuit frequency characteristics in Doherty amplifier, the two-tone CW IMD3 versus $\Delta f = |f_1 - f_2|$ (the difference-frequency of two-tone) characteristics of the 2.2-GHz 28-V-operation 200-W GaAs HJFET Doherty amplifier having the source and the load difference frequency termination circuits were simulated as shown in Fig. 5.31. In addition, Fig. 5.32 shows the simulated fundamental frequency drain voltage of the FETs versus Δf characteristics against the main and the peak amplifiers and their vector combination in the Doherty amplifier in comparison with the case of the Class-AB push-pull amplifier with AMP1 and AMP2 at constant P_{out} of 40 dBm. Thereby, the frequency characteristics of the output power combining circuits can be confirmed under the large signal operation in the amplifier. In spite of equipping the source and the load difference frequency terminations, the IMD3 versus Δf characteristics of the Doherty amplifier revealed the deterioration and the asymmetries at the Δf over 10MHz. Also, the magnitude and the phase deviations of the fundamental frequency drain voltage vector combination between the main and the peak amplifiers become large at the Δf over 10 MHz. This accords with the occurrence of IMD3 asymmetries at the Δf over 10 MHz. On the other hand, in the push-pull amplifier obtaining flat IMD3 characteristics against the Δf over 100 MHz with the source and the load difference frequency termination circuits, the magnitude and the phase of fundamental frequency drain voltage vector combination exhibit no deviation according to the increase of Δf. From these results, it is

found that the frequency-characteristics of the vector combination between the main and the peak amplifiers affect the IMD3 characteristics against the Δf in Doherty amplifier.

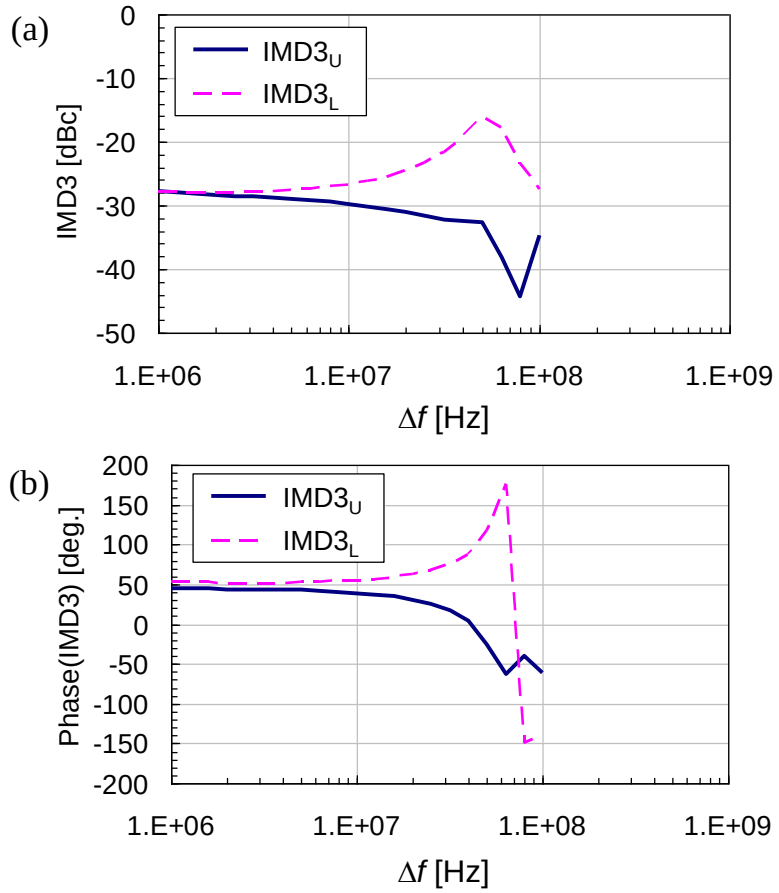


Fig. 5.31 Simulated two-tone CW IMD3 versus Δf characteristics of Doherty amplifier having source and load difference frequency termination circuits. (a) Magnitude of IMD3 versus Δf characteristics. (b) Phase of IMD3 versus Δf characteristics.

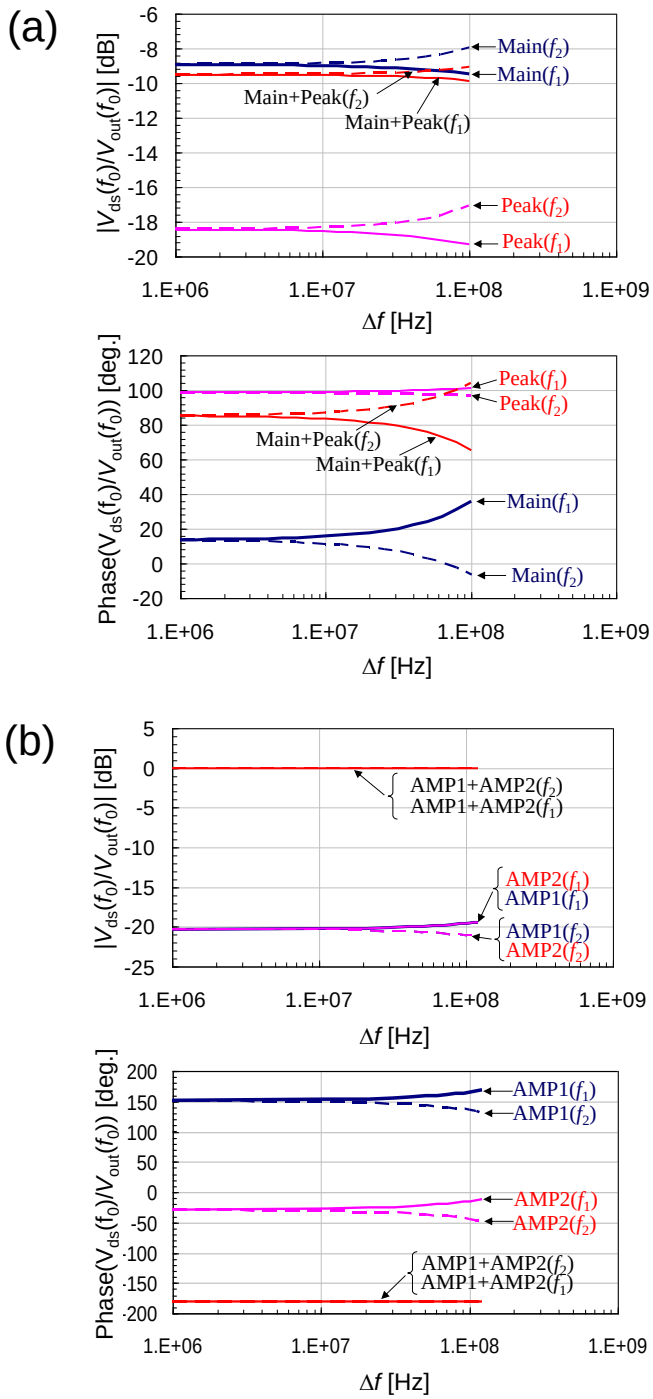


Fig. 5.32 Simulated fundamental frequency drain voltage of the FETs versus Δf characteristics against (a) the main and the peak amplifiers and the vector combination of Doherty amplifier in comparison with (b) the case of Class-AB push-pull amplifier with AMP1 and AMP2.

Figure 5.33 shows the simulated output circuit frequency characteristics of the magnitude and the phase deviation between the main and the peak amplifiers of the Doherty amplifier at the low and the high input power level. They were evaluated using the circuit configuration with the optimally designed load impedance shift as shown in Fig. 5.34. The circuit frequency characteristics of the magnitude and the phase largely change so that the

load impedances of the main and the peak amplifiers shift according to the input power level. Figure 5.33 means the magnitude deviation $\Delta\gamma$ and the phase deviation $\Delta\theta$ of the vector combination between the main and the peak amplifiers as described in Section 5.7.1. The $\Delta\gamma$ and the $\Delta\theta$ exhibit 7 dB and 35º with the Δf of 100 MHz from 2.1 GHz to 2.2 GHz at high input power level respectively. In this way, in Doherty amplifier, it tends to be difficult to lower the magnitude and the phase deviation of the vector combination between the main and the peak amplifiers for wide frequency bandwidth and wide input power range under the optimum load impedance shift design.

To resolve this problem, the proposal of a high efficiency amplifier using the power-combining circuits without quarter-wavelength lines is needed. In the future, if improvement in the speed of envelope amplifier is realized, an envelope-tracking amplifier will be a promising candidate [5.1].

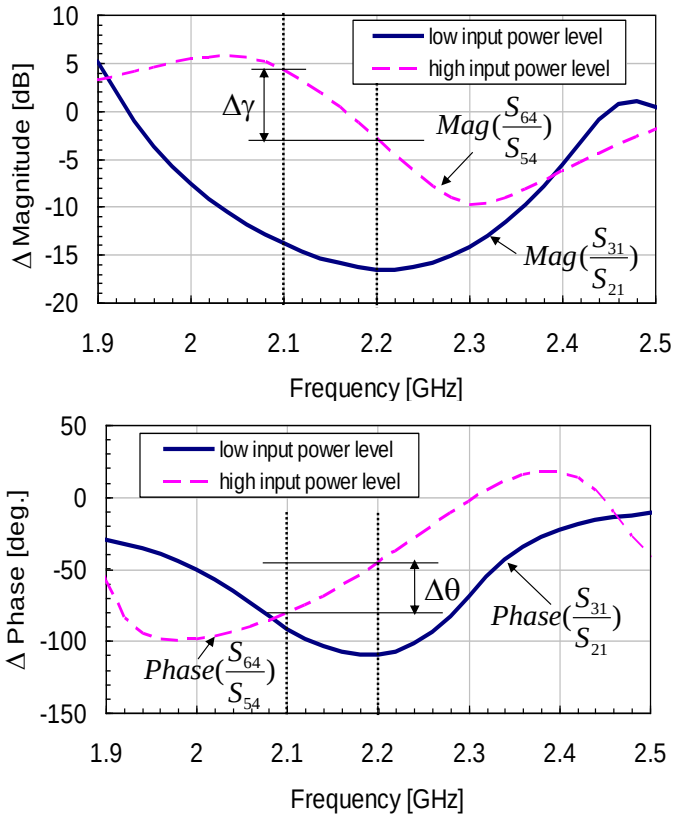


Fig. 5.33 Simulated output circuit frequency characteristics of the magnitude and the phase deviation between the main and the peak amplifiers of Doherty amplifier at low and high input power level.

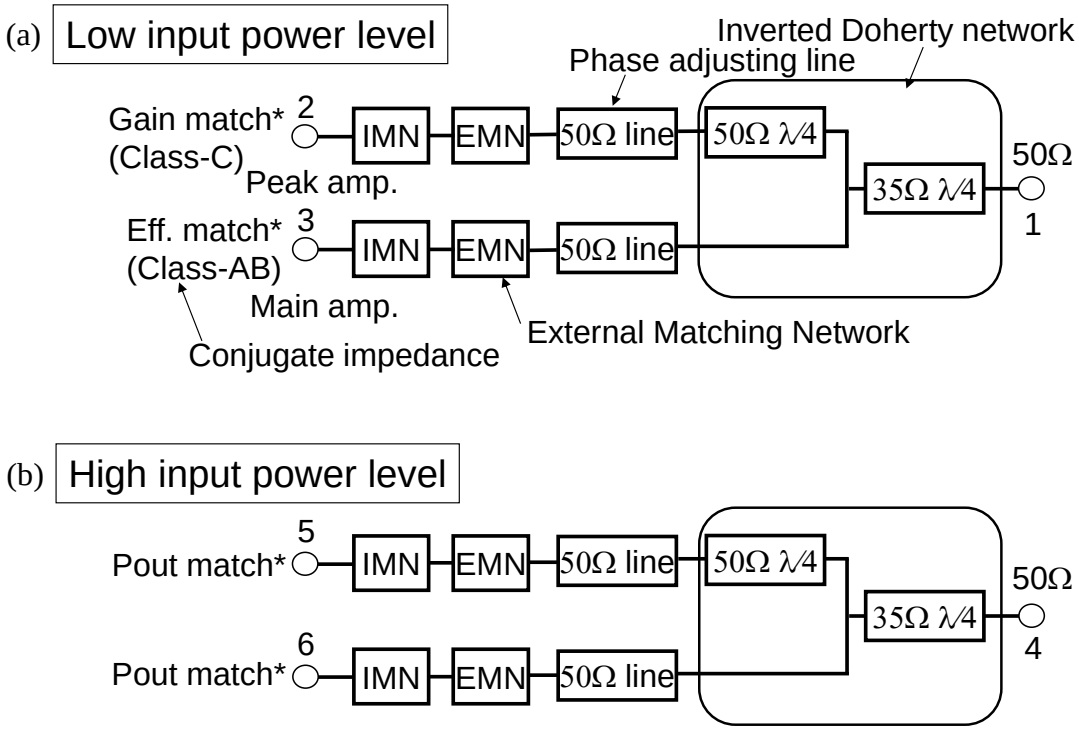


Fig. 5.34 Output circuit parameter optimization at (a) low input power level and (b) high input power level.

5.7.3 Measured IMD versus Δf characteristics of Doherty amplifier

A photograph of developed 28-V-operation 200-W GaAs HJFETs Doherty amplifier is shown in Fig. 5.35. The Doherty amplifier uses the each side of the push-pull type transistor shown in Fig. 5.35 as the main and the peak amplifiers. The amplifier is equipped with *LC* series resonant circuits at the gate and the drain electrodes of the transistor dies in the package as shown in Fig. 5.35. The output power of the main and the peak amplifiers is combined employing the inverted Doherty network with the λ/4 transformers of 50 Ω and 35 Ω. A 90º-hybrid coupler is used in the input circuits.

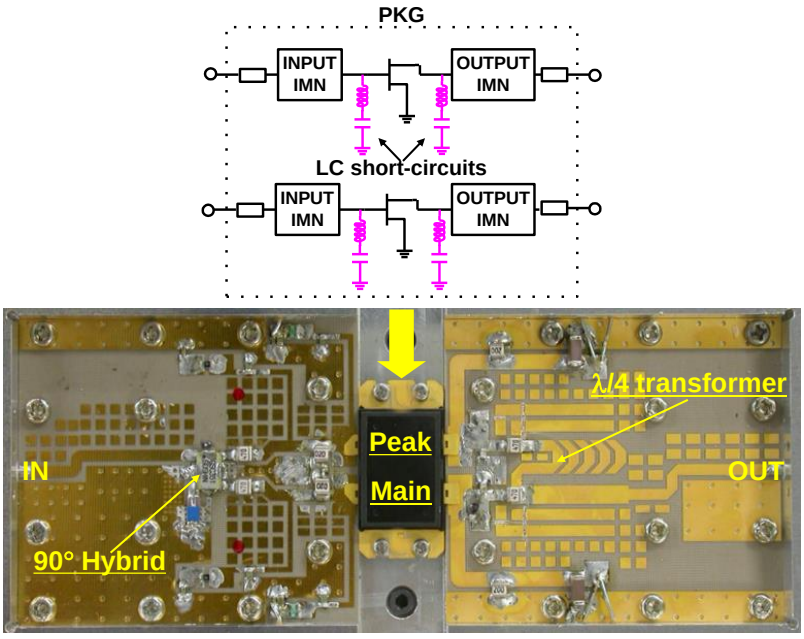


Fig. 5.35 Photograph of developed 28-V-operation 200-W GaAs HJFETs Doherty amplifier.

Figure 5.36 shows the P_{out} versus the input power (P_{in}) characteristics under the pulsed CW condition with the pulse-width of 8 μsec and the pulse-period of 1 msec at 2.14 GHz. It demonstrated a P_{sat} of 54.0 dBm (P_{in} = 43 dBm) and a 13-dB linear gain (P_{in} = 30 dBm) at 2.14 GHz.

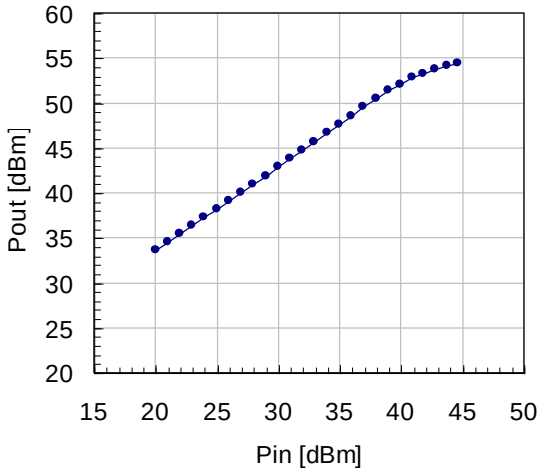


Fig. 5.36 Pulsed CW performance of the developed Doherty amplifier at 2.14GHz.

Figure 5.37 presents the IMD versus P_{out} characteristics under the two-tone CW signals of 2.1325 GHz and 2.1475 GHz. In addition, Fig. 5.38 shows the two-tone CW IMD versus Δf characteristics at the P_{out} of 35 dBm and 46 dBm at the center frequency of 2.14 GHz. At the P_{out} of 35 dBm, the deterioration and the asymmetries of IMD3, IMD5 and IMD7 don't occur up to the Δf of 100 MHz. At the P_{out} of 46 dBm, the magnitude characteristics of IMD3 begin to deteriorate from the Δf of around 50 MHz.

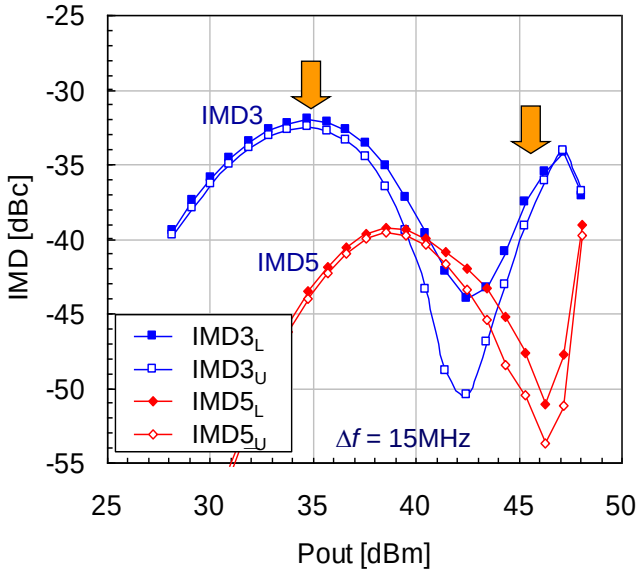


Fig. 5.37 Two-tone CW IMD versus P_{out} characteristics of the Doherty amplifier under the two-tone CW signals of 2.1325 GHz and 2.1475 GHz.

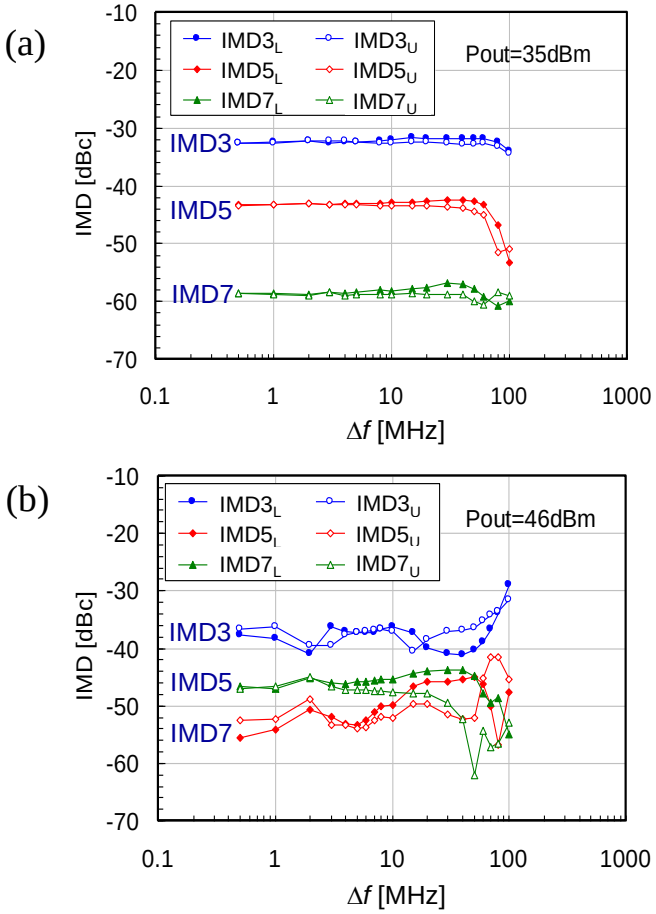


Fig. 5.38 Two-tone CW IMD versus Δf characteristics of the 200-W Doherty amplifier at P_{out} of (a) 35 dBm and (b) 46 dBm at the center frequency of 2.14 GHz.

Figure 5.39 shows the modulated signal performance under the two-carrier W-CDMA signals of the Δf of 15 MHz. The amplifier exhibits low IMD3 characteristics less than −36.5 dBc with a 37% drain-efficiency at an average P_{out} of 46 dBm around the 8-dB back-off output power level under the two-carrier modulated signals of 2.1325 GHz and 2.1475 GHz. The drain efficiency of the Doherty amplifier is significantly improved over the Class-AB push-pull amplifier. Moreover, up to the Δf of 15 MHz, the upper and the lower components of IMD3 and IMD5 exhibit small deviation less than 2 dB. Thus, for modern mobile communication base station system, the developed Doherty amplifier demonstrates wide frequency range characteristics sufficiently. Also, the proposed circuit technique to directly connect *LC* series resonant circuits to the gate and the drain electrodes of the transistor dies in a package proves to be effective for improving the IMD asymmetries under wide carrier-spacing signals in high power amplifier applications.

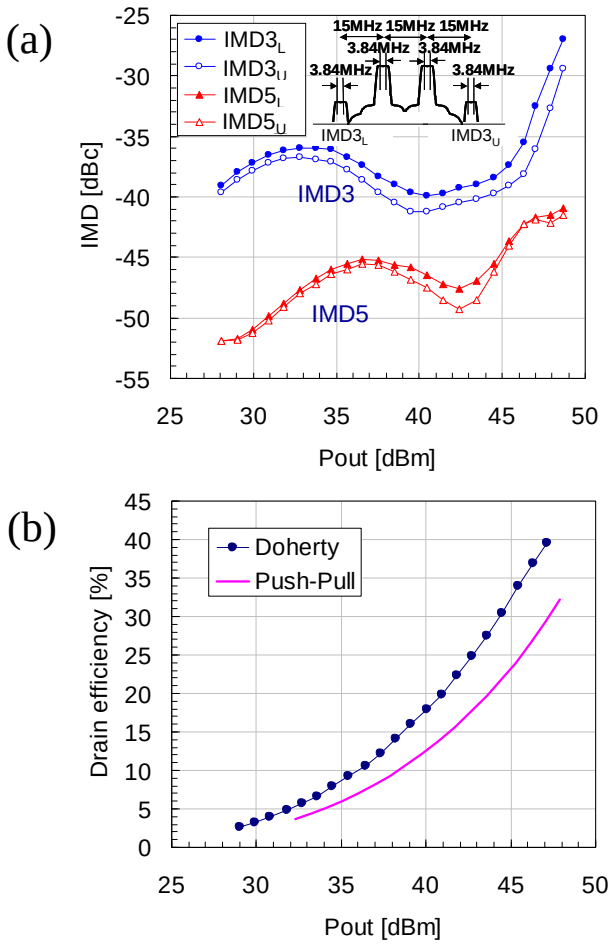


Fig. 5.39 Modulated signal performance of the Doherty amplifier under the two-carrier W-CDMA signals of 2.1325 GHz and 2.1475 GHz of 15-MHz carrier spacing. (a) Two-carrier modulated signal IMD versus P_{out} characteristics of Doherty amplifier. (b) Drain efficiency versus P_{out} characteristics of Doherty amplifier in comparison with push-pull configuration.

5.8 Summary

Chapter 5 described the study on low distortion and high efficiency Doherty amplifiers. In this study, it was clarified that the optimal configuration of Doherty amplifier is present based on the impedance of the device load-pull characteristics. The design approach to perform the distortion compensation in Doherty amplifier was proposed using the distortion cancellation effect of the main and the peak amplifier in power-combining. What has been demonstrated is as follows.

An L/S-band 330-W distortion-cancelled Doherty GaAs FET amplifier has been successfully developed using two 150-W single-ended amplifiers.

The amplifier demonstrated, under a two-carrier W-CDMA condition, low IM3 of less than −37 dBc with a 42% drain-efficiency at a P_{out} of 49 dBm. It achieved significant improvements in efficiency without degradation in linearity.

In addition, the evaluation techniques of each AM-AM and AM-PM characteristics of the main and the peak amplifiers in an operating Doherty amplifier were proposed, and the distortion cancellation of the main and the peak amplifiers in Doherty amplifier linearity was experimentally proved for the first time.

Furthermore, the IMD asymmetries of Doherty amplifier were analyzed through the IMD vector combination of the main and the peak amplifiers. A developed 28-V-operation 200-W GaAs HJFET Doherty amplifier with source and load baseband terminations delivered flat IMD characteristics against the Δf over 50 MHz.

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Chapter 6

Broadband low distortion and high efficiency GaN FET high power amplifiers

6.1 Introduction

Chapter 6 describes the study on broadband, high efficiency, and low distortion microwave high-power amplifiers using GaN FETs on Si substrate. GaN on Si FETs have been developed for cellular base station amplifiers and cable television (CATV) power amplifiers. The GaN FETs on low resistivity (LR) Si substrate were employed for cellular base station amplifiers to improve high temperature operation characteristics. On the other hand, the GaN FETs on high resistivity (HR) Si substrate were used for CATV power-amplifiers of which the output power is comparatively small to improve capacitance nonlinearity.

Since the wide bandgap semiconductor, GaN has high saturation electron velocity and high dielectric breakdown voltage and also can realize high sheet electron concentration according to the hetero-junction structure of AlGaN/GaN, it is expected to be a material suitable for high frequency, high voltage, and high-output power transistors. Taking advantage of the features, GaN field-effect transistors (FETs) on semi-insulating SiC substrate have so far been produced commercially for mobile communication base station amplifier applications [6.1]-[6.3]. However, currently, SiC substrates are very expensive, and SiC substrates cannot meet the needs of cost reduction due to small-size substrate. Namely, it is necessary to eliminate the cost barrier for the further spread of GaN FETs.

In contrast, GaN FET formed on Si substrate is one of the most promising candidates to achieve high performance and low cost. Recently, intensive development competition of GaN FETs on Si substrate is carried out among companies aiming for power management devices [6.4], [6.5]. The GaN FETs for power management employ an LR Si substrate that is

commonly used in Si devices. On the other hand, in RF devices, since it is necessary to improve the loss of RF operation, the GaN FETs on HR Si substrate have taken the lead in development [6.6], [6.8]. However, the GaN FETs on HR Si substrate have a problem that the substrate loss increases in high-temperature operation because the resistivity of Si substrate decreases due to the increase of intrinsic carriers. In the previous report [6.9], this problem has been addressed by the thermal design of the device, but it has not yet become a fundamental solution of the temperature characteristics.

In order to improve temperature characteristics, high-power and high-efficiency microwave amplifiers using GaN FET on LR Si substrate have been developed for the first time. In this work, high performance comparable to GaN FET on HR substrate has been achieved by optimizing the device structure and the circuit configuration.

In CATV power amplifier, high power performance is strongly demanded due to progress of high-speed, large capacity, broadband CATV communication system. Higher output power of amplifier makes it possible to cover the same area with a small number of repeater amplifiers. Recently, the researches of the broadband amplifier using GaN field-effect transistor (FET) are actively reported [6.2], [6.10]. This study aims at the deployment to a broadband low distortion amplifier as further possibility of GaN FET. In the CATV systems that require broad bandwidth more than 1 GHz, distortion compensation circuit techniques are not necessarily effective. The broadband amplifiers need distortion reduction in a device-level. There are derivative superposition methods with multi-gate biasing using multi-transistors as distortion compensation techniques in a device-level [6.11], [6.12]. However, this is the linearization method to create the zero crossing of third-order transconductance coefficient (gm_3) by operating each transistor on different gate bias conditions. Due to that, not only do the circuit and transistor composition become complicated, but also it is difficult to use in a wide bias- and temperature-region. It may be impossible to meet the specifications required for a CATV system.

The devices for CATV amplifiers employing AlGaN/GaN hetero-structure FET (HFET) which has high output capability, for high voltage operation of 24 V have been developed [6.13]. In CATV power amplifiers with a comparatively small output-power, since greater importance was attached to the low distortion characteristics than the high temperature operation characteristics, the GaN FETs on HR Si substrate were applied considering the improvement of nonlinear capacitance. To realize low distortion characteristics required for modern CATV system, low distortion cascode configuration composed of GaAs hetero-junction FET (HJFET) for first stage and GaN FET for final stage

was investigated. Previous report had taken the approach of focusing on only the linearity improvement of gate-to-drain capacitance (C_{gd}) of GaN FET by optimizing the AlN mole fraction of the epitaxial structure [6.2]. This study shows that, from the Volterra distortion analysis on a load-line based on the pulsed *I-V* characteristics, the third-order distortion improvement is possible by using the distortion cancellation effect of high transconductance (*gm*) GaAs HJFET and GaN FET. As the result of the *gm*-profile optimization about GaAs HJFET for first stage, developed CATV power amplifier attained the lowest composite triple beat (CTB) performance at low drain current condition.

6.2 Potential of GaN FET

6.2.1 Problems of GaN FET on HR Si substrate

Here is described about the problems on the temperature characteristics of GaN FET on HR Si substrate. The GaN FETs on HR Si substrate have a problem that the substrate loss increases at high-temperature operation because the resistivity of Si substrate decreases due to the increase of intrinsic carriers.

6.2.1.1 Degradation of efficiency at high-voltage operation

Figure 6.1 (a) shows the drain-efficiency as a function of the back-off from the pulsed saturation output power (P_{sat}) and the drain-to-source voltage (V_{ds}). Measurements were carried out under a WCDMA signal of 2.14 GHz using the peak envelope power (PEP) 300-W GaN FET formed on the HR Si substrate with the total gate-width (W_g) of 2 × 38 mm. The resistivity of the HR Si substrate is about 6000 Ω·cm. The drain-efficiency under a WCDMA signal input decreases abruptly as V_{ds} increases from 38 V to 45 V. P_{sat} was 53 dBm at V_{ds} of 38 V. P_{sat} at V_{ds} of 45 V reached to 55 dBm. In addition, Fig. 6.1 (b) shows the estimated channel temperature at RF operation using the thermal resistance (R_{th}) of 1.0 ºC/W determined from the channel temperature measurement by the infrared microscope. The decrease in efficiency under modulation signal input at 45-V-operation is found to occur in channel temperature (T_{ch}) more than 180 ºC. Thus, the GaN FET on HR Si substrate has a problem that the efficiency characteristics of the device drop at high temperature operation. Next, in order to know the mechanism of efficiency degradation of the GaN FET on HR Si

substrate at the high temperature operation, the temperature characteristics of the RF loss of the drain pad electrode in the GaN FET on Si substrate were investigated.

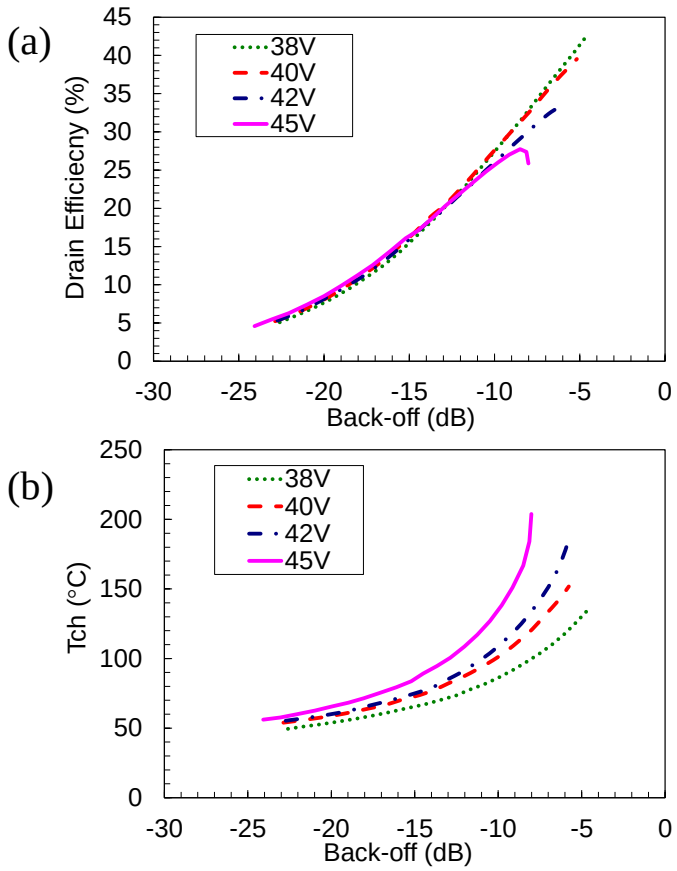


Fig. 6.1 Measured V_{ds} dependence on (a) back-off from pulsed *P*sat versus drain-efficiency under a WCDMA signal of 2.14 GHz and (b) back-off from pulsed *P*sat versus estimated *T*ch under a WCDMA signal in the PEP 300-W GaN FET formed on the HR Si substrate with the total W_g of 2 × 38 mm.

6.2.1.2 Temperature dependence of substrate loss

The structure of the drain pad electrode region in GaN FET on Si substrate is shown in Fig. 6.2 (a). The temperature dependence of the transmission loss of 100-μm square drain electrode pad formed on GaN/Si substrate was examined. The transmission loss was calculated from the following formula (6.1) that expresses the insertion loss subtracting the impedance mismatch loss of the input signal port by measuring the one-port *S*-parameter of the drain pad as shown in Fig. 6.2 (b).

$$Loss = \frac{S_{21} \cdot S_{21}^{*}}{1 - S_{11} \cdot S_{11}^{*}} \tag{6.1}$$

* denotes the complex conjugate.

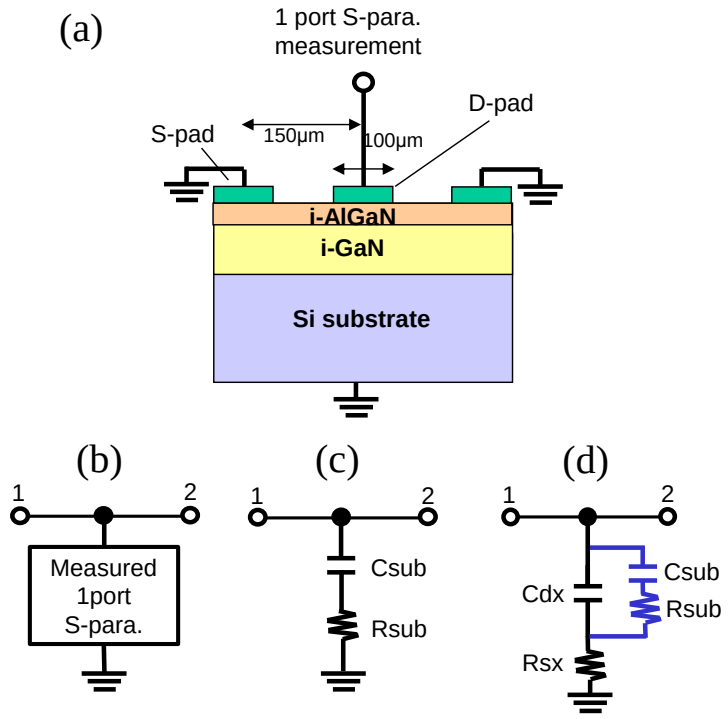


Fig. 6.2 (a) Drain pad structure, (b) transmission loss estimation, (c) equivalent circuit for pad on GaN/LR Si substrate, (d) equivalent circuit for pad on GaN/HR Si substrate.

Figure 6.3 shows the comparison of temperature dependence of the pad transmission loss at 2.2 GHz against the GaN-on-HR Si substrate and the GaN-on-LR Si substrate. In Fig. 6.3, the port impedance is fixed to 50 Ω. The temperature of the stage for placing the sample was changed by using a temperature-controlled heater. The pad loss of the GaN-on-HR Si substrate increased rapidly at more than 180 ºC. On the other hand, the pad loss of the GaN-on-LR Si substrate becomes slightly larger than the GaN-on-HR Si at room temperature, but there was no increase in the loss up to 250 ºC.

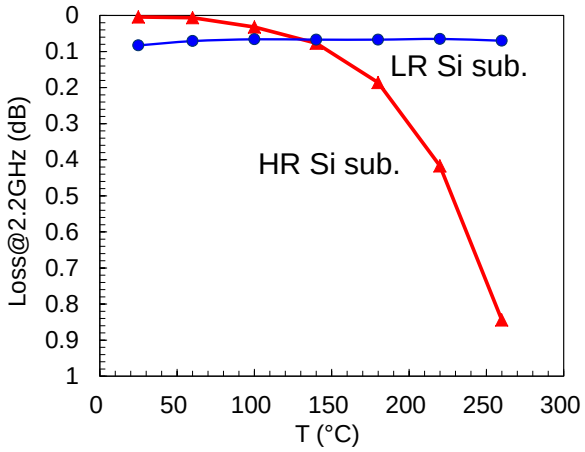


Fig. 6.3 Comparison of temperature dependence of the pad transmission loss at 2.2 GHz against GaN-on-HR Si substrate and GaN-on-LR Si substrate.

Figure 6.4 (a), (b) shows the temperature characteristics of equivalent substrate resistance and pad capacitance, respectively, obtained by using the equivalent circuit of Fig. 6.2 (c), (d). Against the pad on GaN/HR Si substrate, the equivalent circuit of Fig. 6.2 (d) was used for parameter fitting accuracy improvement. The substrate capacitance and resistance (C_{sub}, R_{sub}) with temperature-dependence is added in parallel to the pad parasitic component at room temperature (C_{dx}, R_{sx}) without temperature-dependence. Here, C_{dx} was 0.06 pF, and R_{sx} was 3.9 Ω. Since semi-insulating characteristics can be obtained by AlGaN and GaN epi-layers under the electrode, the series *RC* circuit is suitable for the equivalent circuit.

Figure 6.5 shows the fitting results of the measured 1-port S_{11} and the circuit model for the pad on GaN/HR Si substrate and GaN/LR Si substrate as a function of temperature. The circuit models agree well with measurement results. In the GaN-on-HR Si substrate, substrate resistance decreased rapidly at more than 180 ºC. The pad capacitance also increased with it. On the other hand, in the GaN-on-LR Si substrate, the temperature dependences of substrate resistance and pad capacitance were hardly observed. These results correspond to the relationship that the resistivity of HR Si substrate is greatly reduced at high temperature due to the increase of Si intrinsic carrier, and, in contrast, the resistivity of LR Si substrate has almost no temperature dependence [6.14]. In this way, an increase of the RF loss at high temperature in the GaN-on-HR Si substrate is due to a rapid decrease of the substrate resistance. The reason why the transmission loss of the GaN-on-HR Si substrate and the GaN-on-LR Si substrate is reversed in the high-temperature side more than 150 °C is explained in the Section–6.2.1.3.

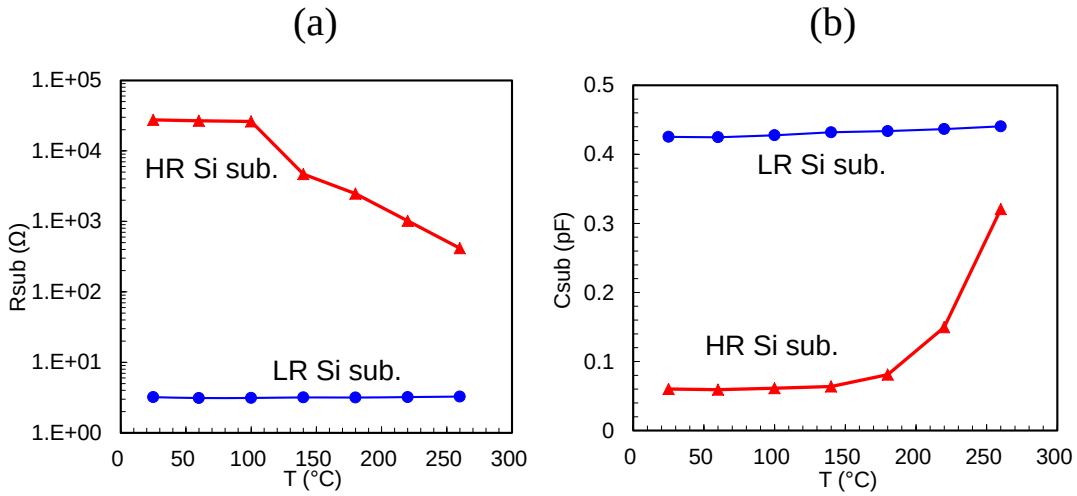


Fig. 6.4 Temperature characteristics of (a) equivalent substrate resistance and (b) pad capacitance obtained by the equivalent circuit of drain-pad.

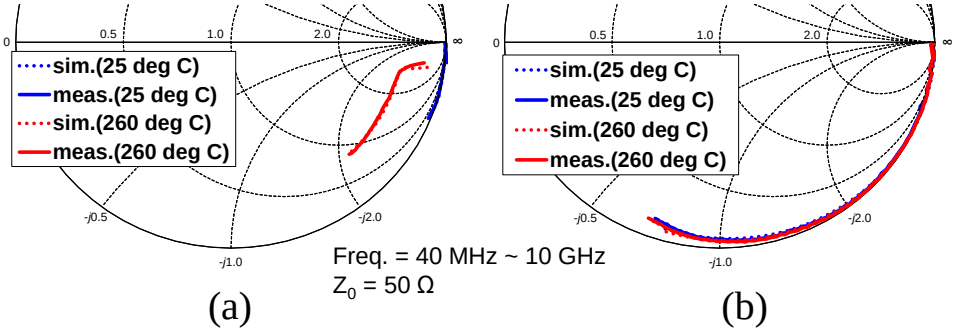


Fig. 6.5 Fitting results of the measured 1-port S_{11} and the circuit model for the pad on (a) GaN/HR Si substrate and (b) GaN/LR Si substrate as a function of temperature.

6.2.1.3 Temperature dependence of device efficiency

Then, the effects of temperature dependence in the substrate resistance on the efficiency characteristics of the device were investigated. The modeling of the measured temperature characteristics of *S*-parameter for the GaN FET on HR Si substrate with W_g of 2.4 mm was carried out using the equivalent circuit shown in Fig. 6.6. The parasitic resistance (R_{db}) and capacitance (C_{db}) that occurs through Si substrate resistance were connected to drain-to-source of the intrinsic equivalent circuit of FET. Also, the parasitic capacitance of the drain and gate pad was expressed in the form including the substrate resistance component. The circuit loss resulting from the series *RC* circuit consisting of C_{db} and R_{db} is denoted by the following formula (6.2) against the load impedance of R_L, substituting $S_{21} = 2Z/(2Z+R_L)$, $S_{11} = -R_L/(2Z+R_L)$, $Z = R_{db}+1/j\omega C_{db}$ for formula (6.1).

$$Loss_{RC} = \frac{1}{1+\dfrac{\omega^2 C_{db}{}^2 R_{db} R_L}{1+\omega^2 C_{db}{}^2 R_{db}{}^2}} \tag{6.2}$$

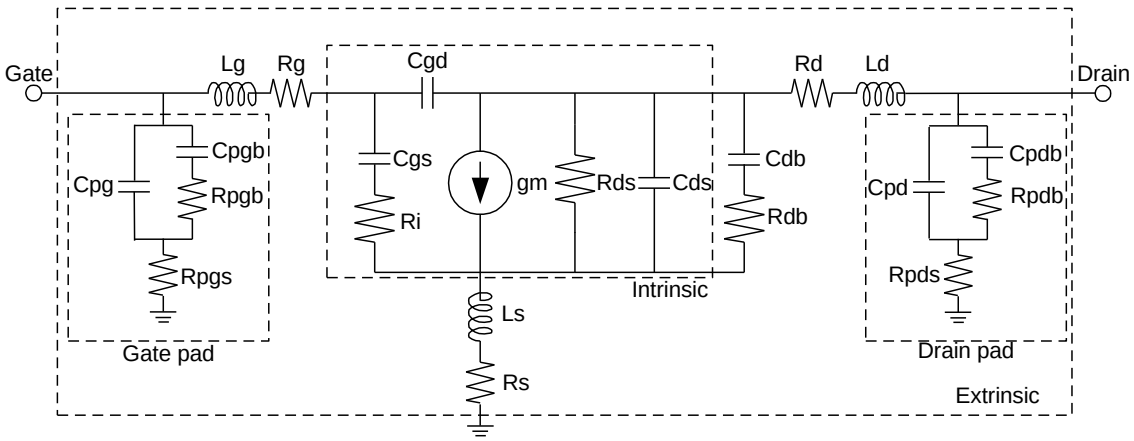


Fig. 6.6 Small-signal equivalent circuit for GaN FET on HR Si substrate.

Figure 6.7 shows the temperature characteristics of the *RC* loss at 2.2 GHz and R_{db} obtained from the temperature dependence of small-signal *S*-parameter measurements at 48 V and 24 mA for a unit cell of W_g of 2.4 mm in GaN FET on HR Si substrate. From the temperature characteristics of the FET, a rapid reduction of the parasitic substrate resistance component of R_{db} with an increased *RC* loss at the T_{ch} more than 180 ºC was confirmed again.

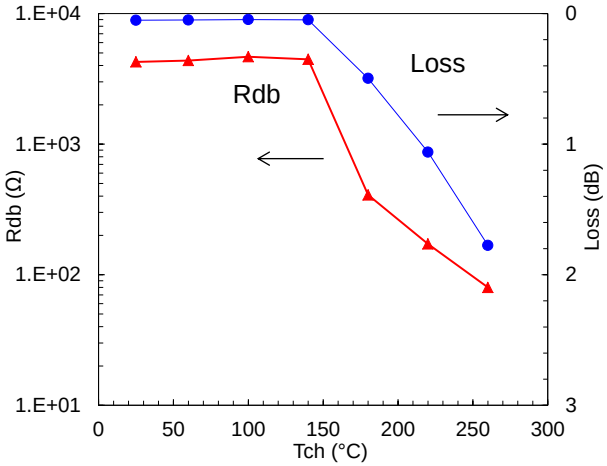


Fig. 6.7 Temperature characteristics of the *RC* loss at 2.2 GHz and *R*db obtained from the temperature dependence of small-signal *S*-parameter measurements at 48 V and 24 mA for a 2.4-mm unit cell in GaN FET on HR Si substrate.

Figure 6.8 shows the temperature dependence of the drain efficiency characteristics under a CW signal condition of 2 GHz in a 2.4-mm unit cell about the GaN FET on HR Si substrate and the GaN FET on LR Si substrate. The T_{ch} was changed by using a temperature-controlled heater and estimated by the R_{th} determined from IR measurement. The GaN FET on HR Si substrate shows large temperature dependence compared to the GaN FET on LR Si substrate.

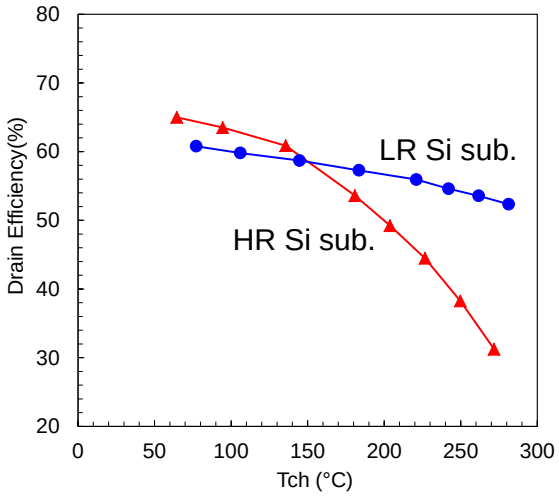


Fig. 6.8 Temperature dependence of the drain efficiency characteristics at 2 GHz in a 2.4-mm unit cell about the GaN FET on LR Si substrate and the GaN FET on HR Si substrate.

Figure 6.9 shows *RC* loss (in%) of formula (6.2) at 2 GHz and R_L of 50 Ω by the dependence of C_{ds} and substrate resistance. It turns out that the *RC* loss increases locally against the resistance. The *RC* loss becomes maximum at the resistance value of the following condition.

$$R = \frac{1}{\omega \cdot C_{ds}} \tag{6.3}$$

The reason why the transmission loss of the GaN-on-HR Si substrate becomes larger than that of the GaN-on-LR Si substrate at more than 150 °C as shown in Fig. 6.3 is because the substrate resistance of the GaN-on-HR Si substrate decreases toward the resistance of formula (6.3) with temperature increase.

Figure 6.9 also includes the points at the low temperature of 25 ºC and the high temperature of 260 ºC about the 2.4-mm unit cell of the GaN FET on HR Si substrate and the GaN FET on LR Si substrate. After all, the reason of the efficiency degradation at high temperature in the GaN FET on HR Si substrate is because the *RC* loss increases by decreased substrate resistance and increased capacitance at high temperature under the conditional expression (6.3) that the *RC* loss becomes maximum. In contrast, the efficiency of GaN FET on LR Si substrate does not deteriorate at high temperature because of having a sufficient low resistance.

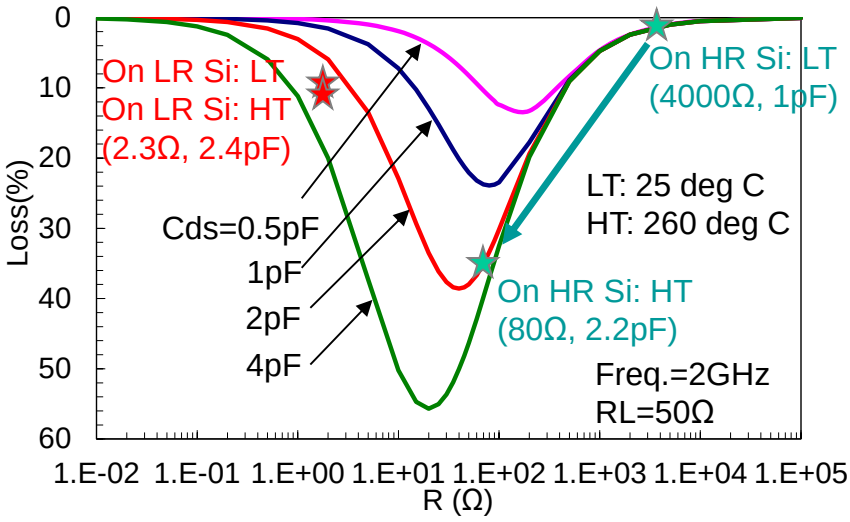


Fig. 6.9 *RC* loss (in%) of formula (2) by the dependence of C_{ds} and substrate resistance.

By perturbation method shown in Fig. 6.10, the impact on efficiency characteristics due to self-heating under a continuous-wave (CW) operation at PEP 200-W GaN FET was verified. By employing the temperature dependence of the output power and the efficiency characteristics obtained from the unit cell shown in Fig. 6.8, CW operation characteristics

were estimated from the characteristics of a pulsed CW operation at 2.14 GHz with the pulse-width of 8 μs and the pulse-period of 1 ms on the PEP 200-W GaN FET. Supposing the state of pulsed CW condition to be the initial state, the initial T_{ch} is changed to T_{ch}' using the temperature dependence of ΔP_{out} and $\Delta Eff.$ determined from a unit-cell measurement, and the T_{ch}' is changed to T_{ch}" using ΔP_{out}' and $\Delta Eff.$' determined from T_{ch}'. This process is continued.

As can be seen from Fig. 6.11 (a), the slump of efficiency does not occur in the CW operation at the moderate temperature dependence of the GaN FET on LR Si substrate, but the slump of efficiency occurs in the CW operation as shown in Fig. 6.11 (b) at the large temperature dependence of GaN FET on HR Si substrate. In this way, the GaN FET on HR Si substrate has an efficiency degradation mechanism due to self-heating in the RF operation through the substrate loss because of the large temperature dependence of the substrate resistance.

$Pout(pulse)$
$Eff.(pulse)$ } Non-perturbation term

$\rightarrow Tch = \Delta Tch + Ta$

$\downarrow$ Ta : Ambient Temp.

$Pout' = Pout(pulse) + \Delta Pout(Tch)$

$Eff.' = Eff.(pulse) \times \Delta Eff.(Tch)$

$\rightarrow Tch'$

$\downarrow$

$Pout'' = Pout(pulse) + \Delta Pout'(Tch')$

$Eff.'' = Eff.(pulse) \times \Delta Eff.'(Tch')$

$\rightarrow Tch''$

$\downarrow$

$\cdots$

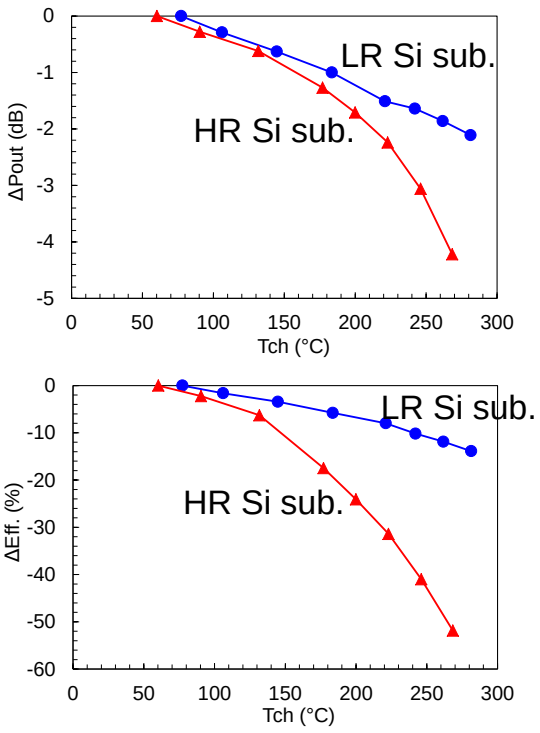


Fig. 6.10 Verification of impact on efficiency characteristics due to self-heating under CW operation by perturbation method.

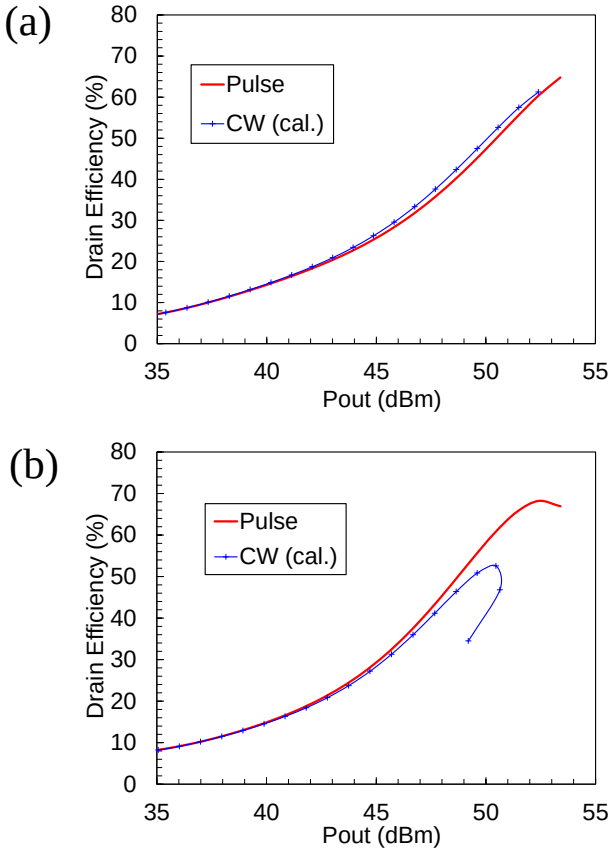


Fig. 6.11 Estimated output power and efficiency characteristics of CW operation from the output power and efficiency characteristics of pulsed CW operation at 2.14 GHz with pulse-width of 8 μs and pulse-period of 1 ms about the PEP 200-W GaN FET (a) on LR Si substrate and (b) on HR Si substrate.

6.2.2 Device structure optimization of GaN on LR Si

LR Si substrate is adopted in order to improve the efficiency at high temperature operation for high-voltage and high-power applications. However, a reduction in RF loss is essential because capacitance against ground is larger than the HR Si substrate at low temperature side. This RF loss is the substrate loss through C_{ds} expressed by formula (6.2). The method to reduce *RC* loss is to make substrate resistance small and to reduce C_{ds} as indicated in Fig. 6.9.

Figure 6.12 shows the schematic cross-section of newly developed GaN FET on LR Si substrate. For high voltage operation, dual field-plates (FP) technology in which one of the FP electrodes (Gate-FP) is connected to the gate and the other (Source-FP) to the ground was employed [6.15]. An i-GaN buffer layer and an i-AlGaN barrier layer are prepared on LR Si substrate, and an i-GaN cap layer is provided in the top layer. The resistivity of Si substrate is 0.02 Ω·cm. The thickness is thinned to 150 μm. The developed GaN FET has the maximum drain current (I_{max}) more than 800 mA/mm, the gate-to-drain breakdown voltage (BV_{gd})

beyond 200 V, and the threshold-voltage (V_{th}) of −2.5 V. For C_{ds} reduction, we considered the thickening of the buffer layer, and the shortening of the Source-FP electrode length, the drain electrode width and the drain pad size.

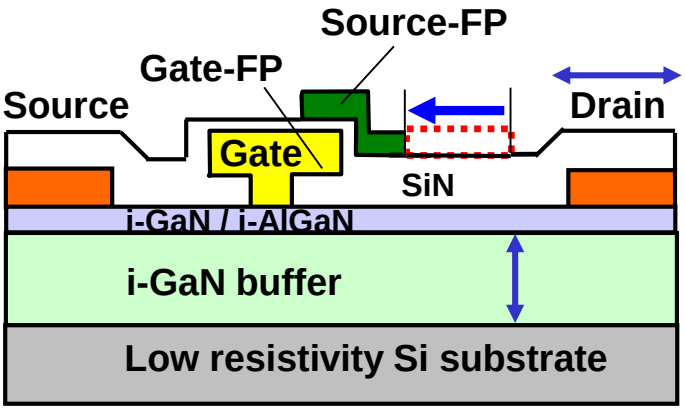


Fig. 6.12 Schematic cross-section of developed GaN FET on LR Si substrate.

Figure 6.13 (a) shows the Source-FP length dependence of the C_{ds} measured at a unit cell of W_g of 2.4 mm, and the maximum drain efficiency obtained by the load-pull measurement for a 0.8-mm unit cell at 48 V and 0.8 mA at 2 GHz. Although C_{ds} could be reduced by shortening Source-FP length, the Source-FP length is to be more than 0.6 μm by concerning the influence of current-collapse. In addition, the gate-length (L_g) and the gate-to-drain length (L_{gd}) are 0.6 μm and 3.5 μm, respectively. Figure 6.13 (b) shows the buffer thickness dependence of the C_{ds} for a 2.4-mm device and the maximum drain efficiency by the load-pull measurement for a 0.8-mm device at 48 V and 0.8 mA at 2 GHz. The capacitance of the intrinsic part and the pad part could be reduced by thickening buffer layer, and the buffer thickness was taken as 6.6 μm. It is necessary to note that too thick buffer layer influences the bow of wafer, or the thermal resistance. The relationship between the C_{ds} and the drain efficiency is shown in Fig. 6.13 (c). The measurement result is in good agreement with the simulation result considering the RF loss due to C_{ds} and substrate resistance. The validity of the improvement strategy was confirmed.

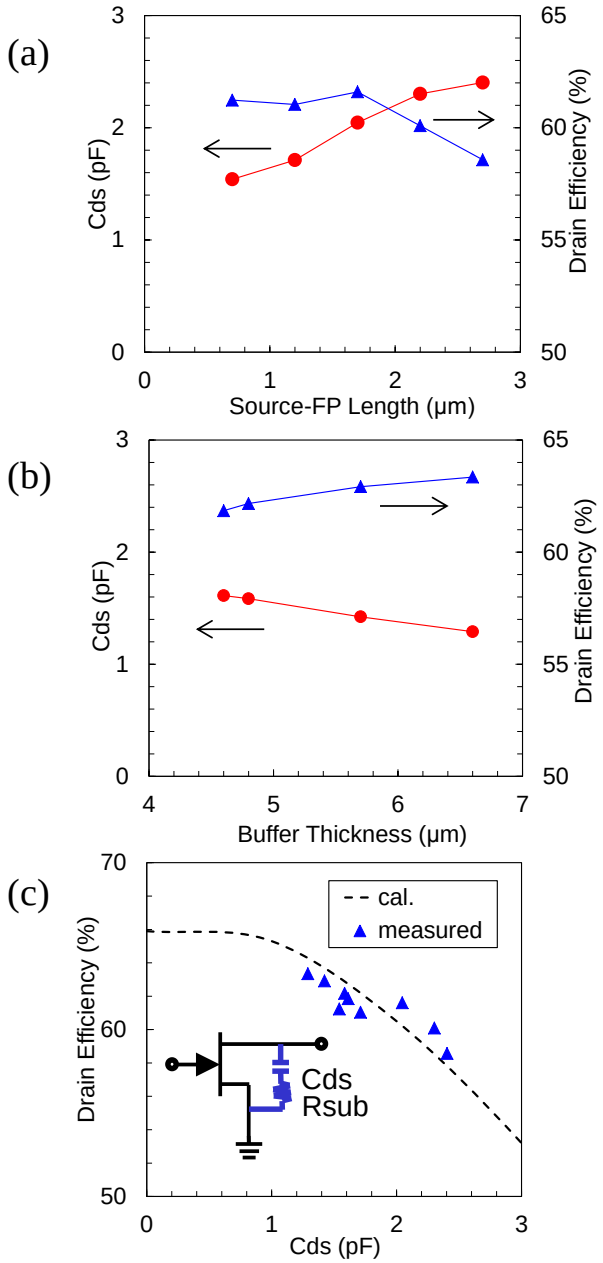


Fig. 6.13 (a) Source-FP length dependence, and (b) buffer thickness dependence of the C_{ds} measured at a 2.4-mm unit cell, and the maximum drain efficiency obtained by the load-pull measurement for a 0.8-mm device at 48 V and 0.8 mA at 2 GHz. (c) relationship between the C_{ds} and the drain efficiency of measurement results and simulation results (dash line).

Figure 6.14 compares the V_{ds} dependence of the output capacitance (C_{out}) of the GaN FET on HR Si substrate and the GaN FET on LR Si substrate about a unit cell of W_g of 2.4 mm. Here, C_{out} defines as C_{out} = C_{ds} + gate-to-drain capacitance (C_{gd}). The C_{out} of GaN FET on LR Si substrate is about 1.5 times larger than that of the GaN FET on HR Si substrate, but the voltage dependence is similar.

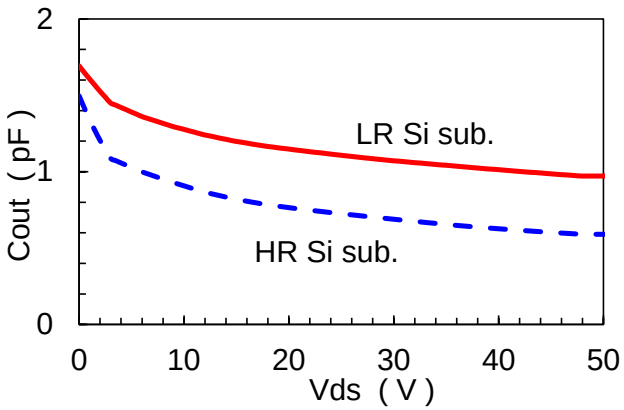


Fig. 6.14 Comparison of the V_{ds} dependence of the C_{out} of the GaN FET on HR Si substrate and the GaN FET on LR Si substrate about a unit cell of W_g of 2.4 mm.

Figure 6.15 shows the voltage dependence of the P_{sat} and the maximum drain efficiency at efficiency matching condition by load-pull measurement at a 0.8-mm device for the GaN FET on HR Si substrate and the GaN FET on LR Si substrate. The load-pull measurement was performed by each V_{ds}. The P_{sat} of the GaN FET on LR Si substrate was extended in proportion to V_{ds} up to 48 V, and it exhibited the P_{sat} of 7 W/mm and the drain efficiency of 64% at V_{ds} of 48 V. By the RF loss improvement of the C_{ds} reduction, the developed GaN FET on LR Si substrate acquired the power density and efficiency characteristics comparable to the GaN FET on HR Si substrate.

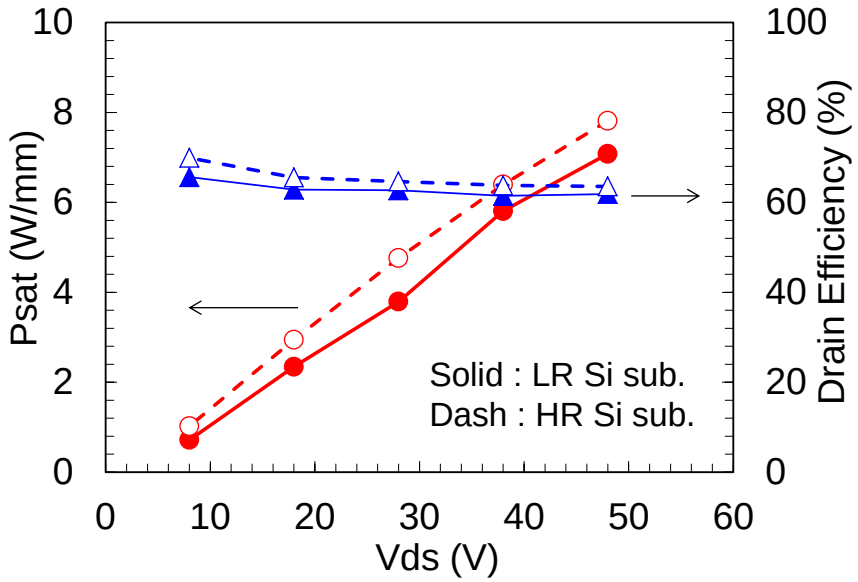


Fig. 6.15 Voltage dependence of the *P*sat and maximum drain efficiency at efficiency matching condition by load-pull measurement at a 0.8-mm device for the GaN FET on HR Si substrate and the GaN FET on LR Si substrate.

6.3 L/S-band GaN on Si FET high power amplifiers

6.3.1 250-W GaN FET on LR Si substrate amplifier

A circuit design and the prototype evaluation results of 250-W single-ended amplifier using the GaN FET on LR Si substrate technology are presented. Figure 6.16 shows the drain-efficiency (η_d) contours and the P_{out} contours under a CW of 2 GHz for a 0.8-mm FET about the GaN FET on LR Si substrate and the GaN FET on HR Si substrate. The maximum efficiency point and the maximum power point of the GaN FET on LR Si substrate are located on more inductive side (in the meaning with larger value of X/R) compared to the GaN FET on HR Si substrate. This indicates that the GaN FET on LR Si substrate has larger capacitive component under the large signal operation. In addition, by replacing the complex conjugate of the load impedance by an equivalent parallel RC circuit, the maximum efficiency point of the GaN FET on LR Si substrate is represented as R of 270 Ω and C of 0.8 pF, and the GaN FET on HR Si substrate is represented as R of 250 Ω and C of 0.4 pF. The R here indicates the load-line resistance. The capacitance under the large signal operation of the GaN FET on LR Si substrate is to be about twice larger than the GaN FET on HR Si substrate.

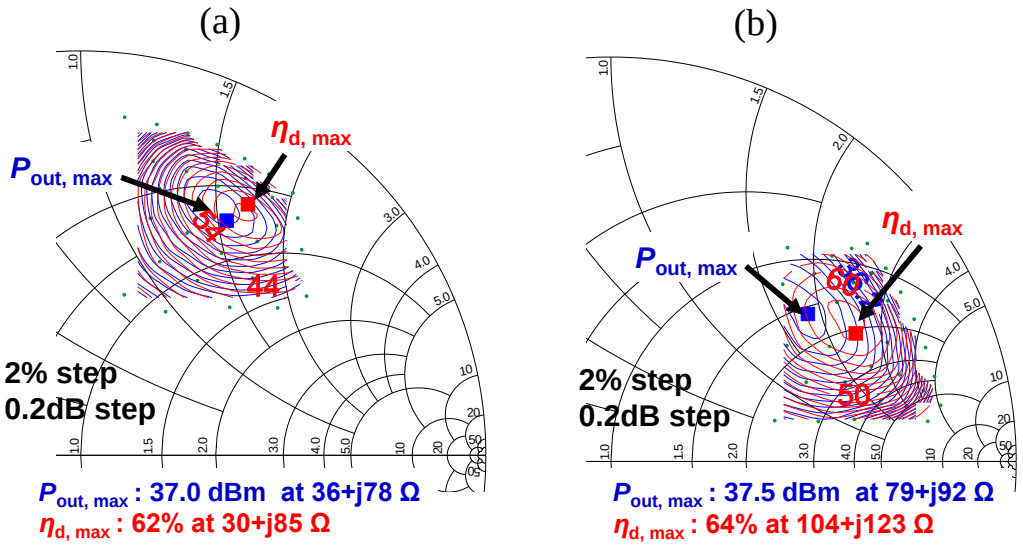


Fig. 6.16 η_d contours and P_{out} contours under a CW of 2 GHz for the 0.8-mm FET about (a) the GaN FET on LR Si substrate and (b) the GaN FET on HR Si substrate.

Figure 6.17 shows the results of the second harmonic load pull simulation for the GaN FET on LR Si substrate and the GaN FET on HR Si substrate using the table-data based large

signal model for a 2-mm FET. From this result, the circuit configuration to open the second harmonic load impedance is optimal.

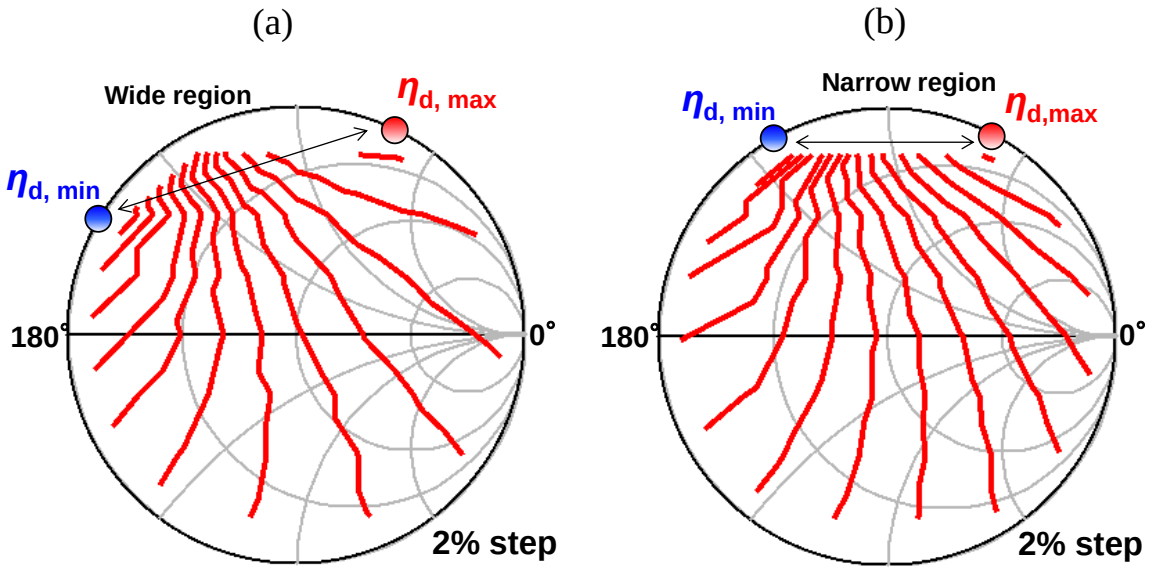


Fig. 6.17 Results of the second harmonic load pull simulation for (a) GaN FET on LR Si substrate and (b) GaN FET on HR Si substrate using table-data based large signal model for a 2-mm FET.

The circuit configuration and the internal photograph of the developed 250-W GaN FET are shown in Fig. 6.18 and Fig. 6.19, respectively. The internal output matching circuit consists of transmission lines and one-stage *LC* low pass filter networks in order to realize both load second harmonic open termination and load fundamental efficiency matching condition [6.16]. As shown in Fig. 6.14, since the GaN FET on LR Si substrate has larger C_{ds} than the GaN FET on HR Si substrate, the load second harmonic impedance region to worsen the efficiency is in a short circuit side than the GaN FET on HR Si substrate. In other words, since the maximum efficiency point is in the almost same position at both, with respect to load second harmonic impedance, the GaN FET on LR Si substrate having large C_{ds} can efficiently use wide impedance region. Thus, the GaN FET on LR Si substrate is easily able to realize load fundamental matching condition and load second harmonic open termination simultaneously. The internal input matching circuit consists of two-stage *LC* low pass filter networks. Source fundamental impedance is set to gain-matching condition and source second harmonic impedance is to be short circuit condition. The photograph of a developed GaN FET chip is shown in Fig. 6.20. The W_g of a chip was 24 mm. The unit finger width was 400 μm. The chip size is 5.3×0.95 mm^2. The two GaN FET chips (i.e. total $W_g = 2 \times 24$ mm) were mounted on a single plastic molding package with internal matching circuits. The package size is 24×17.4 mm^2. The gate pitch is 75 μm. The thermal resistance

from FET channel to case for parallel two chips is designed to be 1.0 ºC/W. The single-ended amplifier consists of the external circuit including the bias circuit as shown in Fig. 6.21. The simulated input- and output-circuit impedance (Z_S, Z_L) locus in the frequency range from 10 MHz to 10.01 GHz is shown in Fig. 6.22. The normalized impedance is 50/20 Ω. The points and values of the impedance of the fundamental frequency (f_0), the second harmonic frequency ($2f_0$), and the third harmonic frequency ($3f_0$) are also indicated in Fig. 6.22.

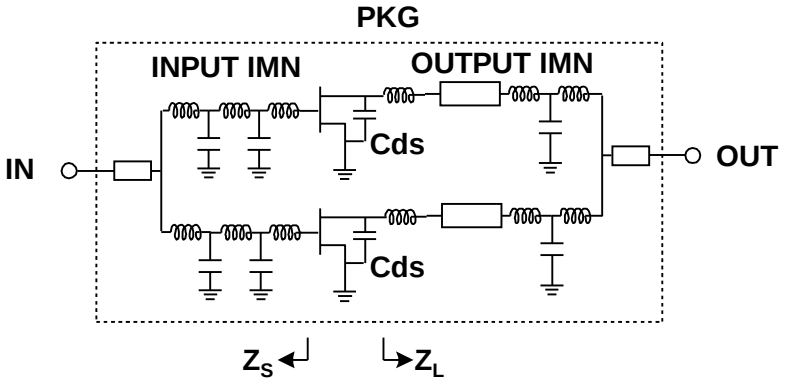


Fig. 6.18 Circuit configuration of developed 250-W GaN FET.

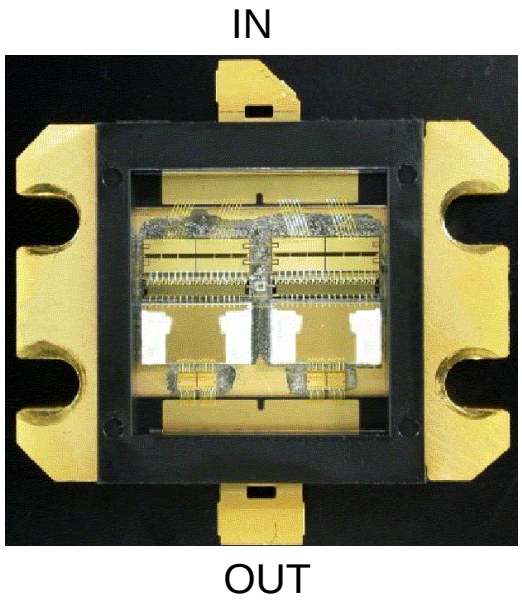


Fig. 6.19 Internal view of developed 250-W GaN FET.

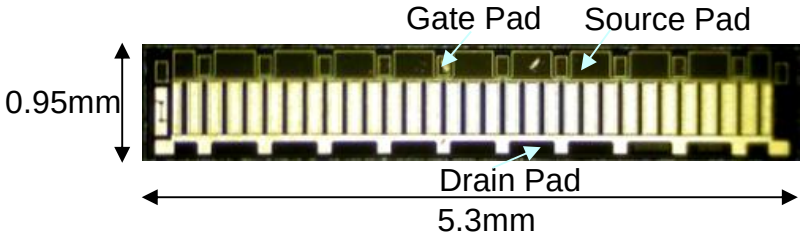


Fig. 6.20 Photograph of a developed GaN FET chip.

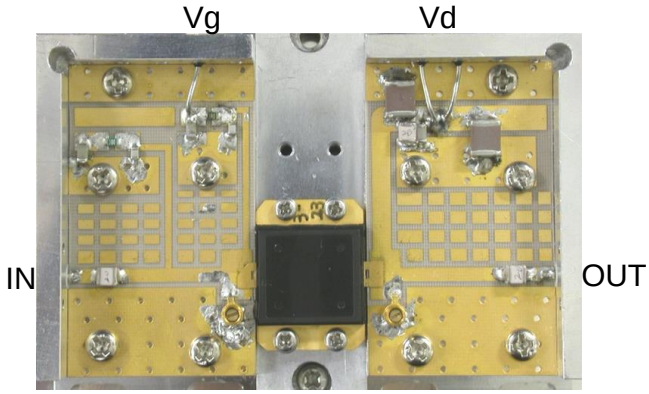
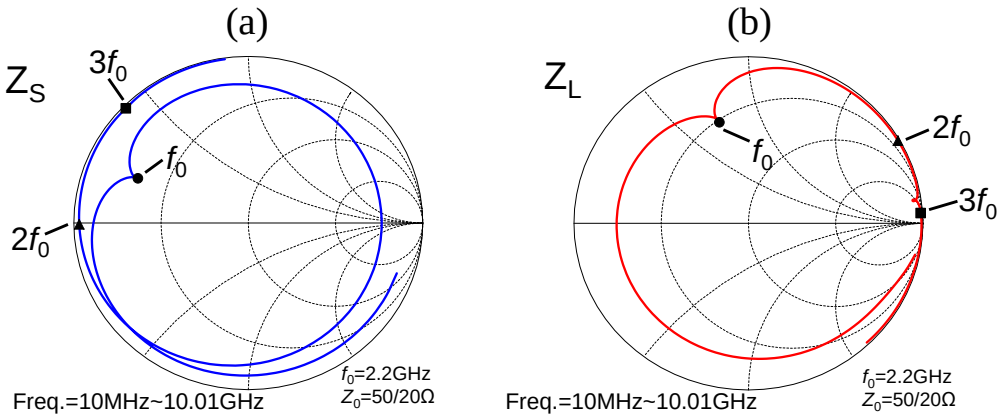


Fig. 6.21 Top view of developed single-ended amplifier.



	$Z_S(\Omega)$ Z_0=50/20Ω
f_0	0.19+j0.20
$2f_0$	0.02-j0.00
$3f_0$	0.01+j0.41

	$Z_L(\Omega)$ Z_0=50/20Ω
f_0	0.35+j0.70
$2f_0$	0.07+j3.72
$3f_0$	5.19+j31.5

Fig. 6.22 Simulated (a) input- and (b) output-circuit impedance (Z_S, Z_L) locus in the frequency range from 10 MHz to 10.01 GHz.

Figure 6.23 shows the P_{out} versus the input power (P_{in}) characteristics under a pulsed CW condition with the pulse-width of 8 μsec and the pulse-period of 1 msec within the UMTS band (2.11 GHz to 2.17 GHz). The drain efficiency was measured on Class-B condition by a pulsed CW signal of 2.14 GHz with the pulse width of 200 μs and the pulse period of 2 ms (duty cycle = 10%). The developed GaN FET amplifier attained the linear gain (GL) (P_{in} = 30 dBm) of 19 dB at 2.14 GHz and the P_{sat} of 54 dBm (250 W) from 2.11 GHz to 2.17 GHz on a 50-V-operation and the quiescent drain current (I_{dq}) of 0.3 A. The drain peak efficiency reached to 70% at 2.14 GHz on a 50-V-operation. Figure 6.24 shows the drain efficiency and the adjacent channel leakage power ratio (ACLR) versus average output power under a WDCMA signal condition (3GPP test-model 64ch, 47.5% clipping). Frequency is from 2.11 GHz to 2.17 GHz. Bias conditions are the V_{ds} of 50 V and the I_{dq} of 0.3 A. The amplifier exhibited superior high efficiency characteristics of a 33% drain-efficiency with the ACLR characteristics of less than –31.5 dBc at an average P_{out} of 46 dBm

around the 8 dB back-off output power level. The adoption of low resistivity Si substrate whose resistivity is less sensitive over temperature enabled the modulation signal continuous operation at 50-V-operation.

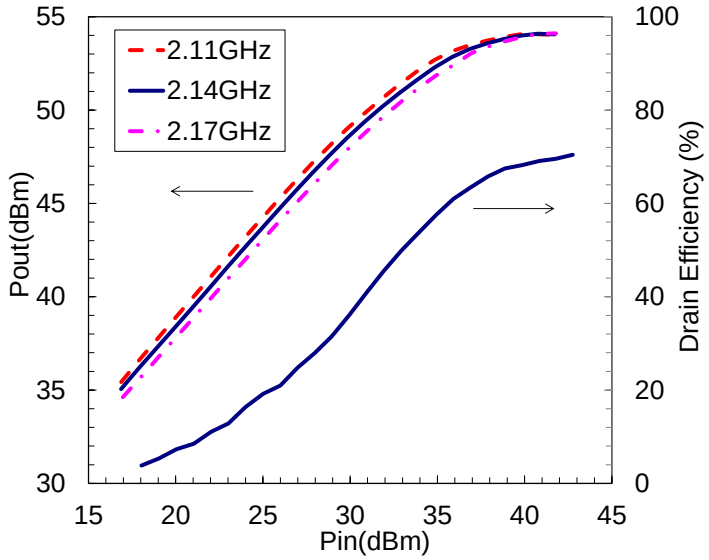


Fig. 6.23 P_{out} versus P_{in} characteristics under a pulsed CW condition with the pulse-width of 8 μsec and the pulse-period of 1 msec within the UMTS band (2.11 GHz to 2.17 GHz).

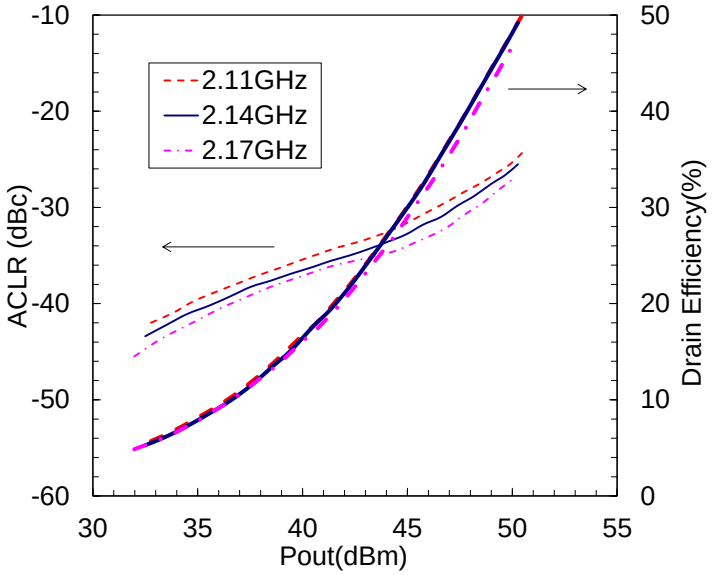


Fig. 6.24 Drain efficiency and ACLR versus average P_{out} under a WDCMA signal condition (3GPP test-model 64ch, 47.5% clipping).

6.3.2 537-W two-way inverted Doherty amplifier

The circuit design and the experimental evaluation results for 537-W two-way inverted Doherty amplifier using 250-W GaN FETs on LR Si substrate are demonstrated. The discussion focused on the positional relationship between the impedance of the maximum power point ($P_{out,\,max}$) and that of the maximum drain efficiency point ($\eta_{d,\,max}$) for a 2.4-mm

unit-cell GaN FET on LR Si substrate as shown in Fig. 6.25. As shown in the following formulas (6.4) and (6.5), although the real part of the circuit impedance in $\eta_{d,\,max}$ point ($\mathrm{Re}\{Z_L(\eta_{d,\,max})\}$) is lower than that of $P_{out,\,max}$ point ($\mathrm{Re}\{Z_L(P_{out,\,max})\}$), the real part of the load-line resistance ($1/\mathrm{Re}\{Y_L(\eta_{d,\,max})\}$) determined replacing the complex conjugate of the load impedance by an equivalent parallel *RC* circuit is higher than that of $P_{out,\,max}$ point. As shown in Fig. 6.26, the difference in C_{out} on a load line can explain such a difference. This is because the C_{out} on the load line at the $\eta_{d,\,max}$ point with high load-line resistance (R = 187 Ω) is larger than that at the $P_{out,\,max}$ point with low load-line resistance (R = 87 Ω). For the most efficient operation, the main amplifier load impedance in a Doherty amplifier should be shifted from $\eta_{d,\,max}$ point to $P_{out,\,max}$ point as an arrow in Fig. 6.25 according to the increase of input power level. In the case of the positional relationship of the $\eta_{d,\,max}$ point and the $P_{out,\,max}$ point as the formulas (6.4) and (6.5), in order to shift the circuit impedance from low impedance to high impedance contrary to an original Doherty amplifier, the inverted Doherty configuration of which the quarter wave length (λ/4) transformer is connected to the output of the peak amplifier is suitable for miniaturization of circuit because it is possible to shorten the phase adjusting line [6.17]. The load-line of the main amplifier in the inverted Doherty amplifier changes from high impedance to low impedance as with the operation principle of Doherty amplifier because of satisfying the impedance condition of (6.5).

$$\mathrm{Re}\{Z_L(P_{out,\ max})\} > \mathrm{Re}\{Z_L(\eta_{d,\ max})\} \tag{6.4}$$

$$\frac{1}{\mathrm{Re}\{Y_L(P_{out,\ max})\}} < \frac{1}{\mathrm{Re}\{Y_L(\eta_{d,\ max})\}} \tag{6.5}$$

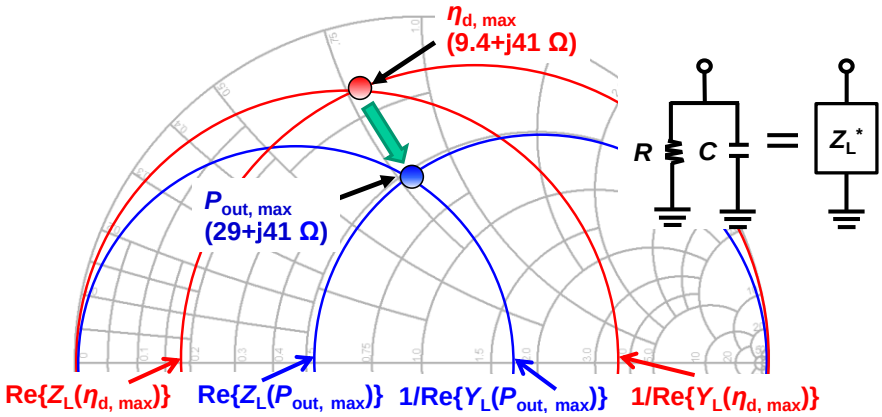


Fig. 6.25 Positional relationship of the impedance of $P_{out,\,max}$ and $\eta_{d,\,max}$ about a 2.4-mm GaN FET on LR Si substrate with parallel *RC* load-line model.

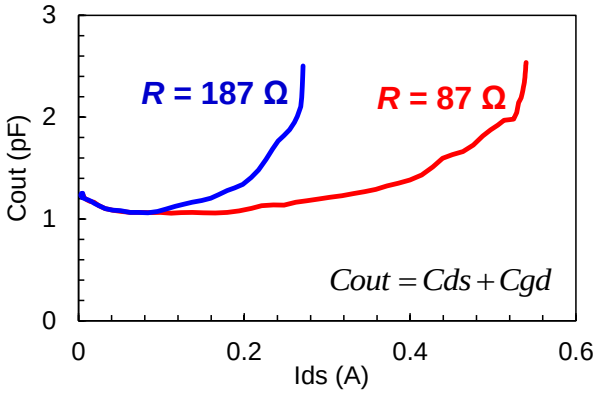


Fig. 6.26 C_{out} on the load-line versus I_{ds} at the $\eta_{d,\,max}$ point with load-line resistance R of 187 Ω and the $P_{out,\,max}$ point with R of 87 Ω.

Figure 6.27 (a) and (b) show the circuit configuration and the photograph of a developed 2-way inverted Doherty amplifier using the 250-W GaN FETs on LR Si substrate, respectively. The λ/4 transmission lines, the bias circuits, and so on are formed on a Teflon substrate (εr = 2.6, t = 0.8 mm).

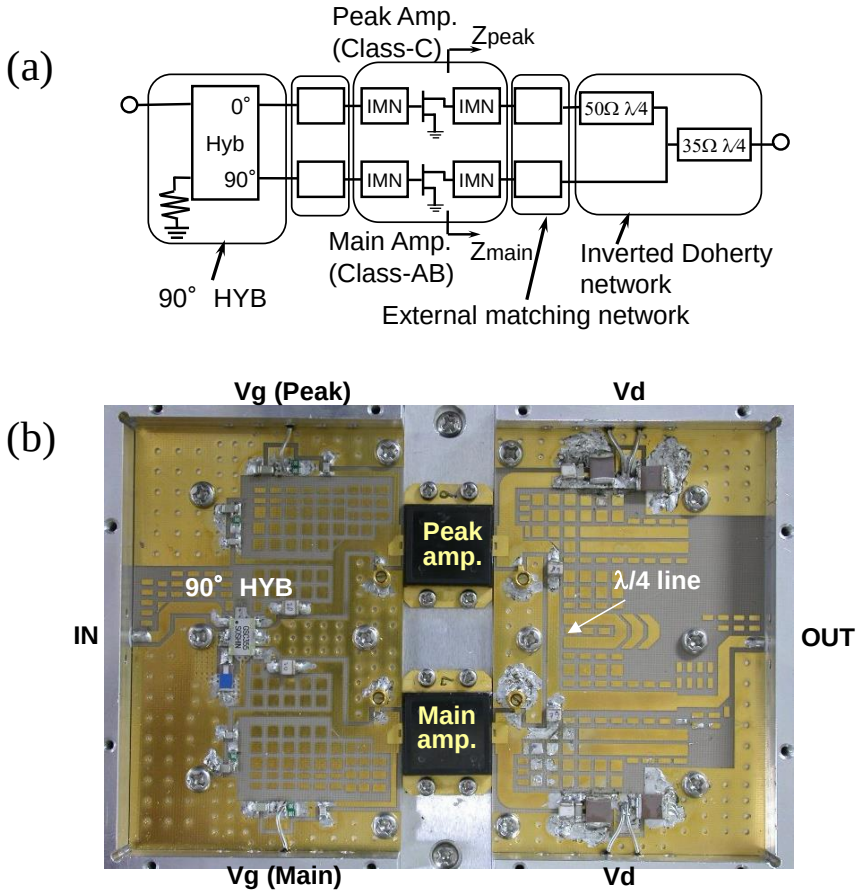


Fig. 6.27 (a) Circuit configuration and (b) photograph of a developed 2-way inverted Doherty amplifier using the 250-W GaN FETs on LR Si substrate.

Figure 6.28 shows the P_{out} versus P_{in} characteristics under a pulsed CW condition with the pulse-width of 8 μsec and the pulse-period of 1 msec at 2.14 GHz. The developed Doherty amplifier exhibited a P_{sat} of 57.3 dBm (537 W) and a 15.5-dB linear gain (P_{in} = 30 dBm) at the V_{ds} of 50 V and the I_{dq} of 0.4 A with gate-voltage (V_g) of the peak amplifier of –5.4 V.

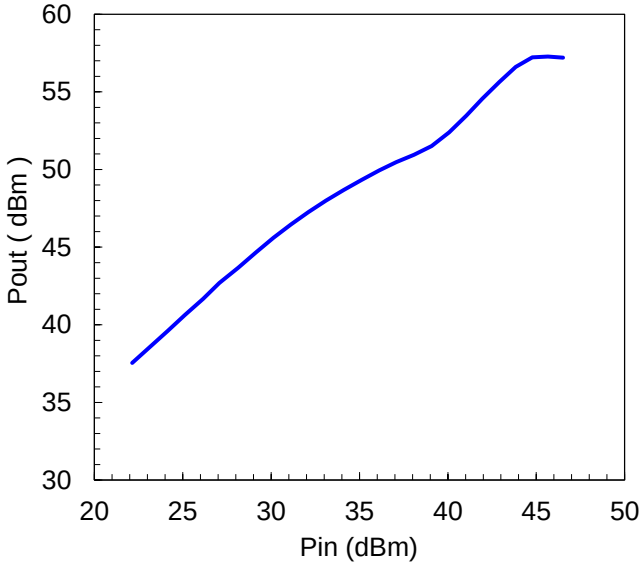


Fig. 6.28 P_{out} versus P_{in} characteristics under a pulsed CW condition with the pulse-width of 8 μsec and the pulse-period of 1 msec at 2.14 GHz.

Figure 6.29 shows the drain efficiency and the upper and lower components of ACLR ($ACLR_U$, $ACLR_L$) versus average P_{out} under a WDCMA signal condition (3GPP test-model 64ch, 47.5% clipping) of 2.14 GHz. The amplifier obtained excellent high efficiency characteristics of a 46.8% drain-efficiency with the ACLR characteristics of less than –25.7 dBc at an average P_{out} of 49.3 dBm of the 8-dB back-off from the peak output power. Furthermore, in the digital pre-distortion (DPD) application experiment (employing Optichron OP4400 evaluation board) under a WCDMA signal (peak-to-average ratio (PAR) = 7.3 dB), the amplifier showed high distortion compensation capability of about 30 dB and achieved the drain efficiency of 48% and the ACLR of –55 dBc at average P_{out} of 50 dBm. Table 6.1 summarizes the measured amplifier performances and compares them with other state-of-the-art GaN FET amplifiers. These results are comparable to the best performance of the GaN on SiC FET high-power amplifiers [6.18]. As described above, newly developed GaN FET on LR Si substrate technology contributes to the coexistence of high performance and low cost in the high-power microwave GaN device.

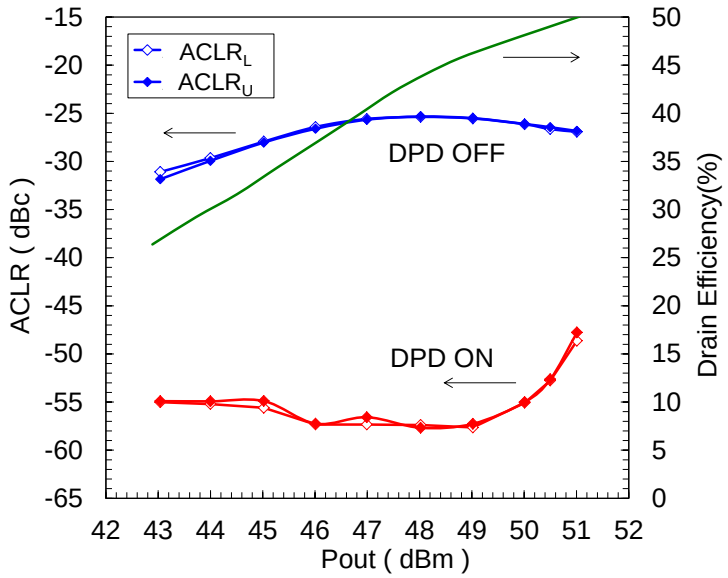


Fig. 6.29 Drain efficiency and ACLR versus average P_{out} under a WDCMA signal condition (3GPP test-model 64ch, 47.5% clipping) of 2.14 GHz without and with DPD linearization.

Table 6.1 Comparison of State-of-the-Art GaN FET Amplifiers Performances.

Reference	Device	f_0 (GHz)	GL (dB)	P_{sat} (dBm)	$\eta_{d,max}$ (%)	$\eta_{d,avg}$* (%)	ACLR DPD OFF (dBc)	ACLR DPD ON (dBc)	Circuit
This work	GaN/LR-Si	2.14	19, 15.5	54, 57.3	70, –	33, 48	−31.5, −25.7#1	–, −55#1	S.E., Doherty
[6.18]	GaN/i-SiC	2.6	–, 13.5	55, 57.3	61.8, –	–, 48	–, −30#2	–, −50.6#2	S.E., Doherty
[6.19]	GaN/i-SiC	2.14	18, 15	49.3, 52.3	71, –	–, 50	–	–	S.E., Doherty
[6.7]	GaN/HR-Si	2.14	17	51.6	73.8	–	–	–	S.E.
[6.8]	GaN/HR-Si	2.15	14	52.3	70	–	–	–	S.E.

* $\eta_{d,avg}$ is drain-efficiency at 7-dB output back-off.
#1 modulation signal condition is a WCDMA signal with PAR of 7.3 dB.
#2 modulation signal condition is WCDMA1111 4-carrier signal with PAR of 6.2 dB.

6.4 Broadband low distortion GaAs HJ and GaN FET cascode amplifier

Here is described about the deployment to a broadband low distortion amplifier as further possibility of GaN FET.

6.4.1 Distortion cancellation technique in device level

Figure 6.30 shows the device configuration and proposed distortion cancellation technique in cable television (CATV) amplifier. A CATV amplifier takes the cascode configuration which combines the common-source transistor and common-gate transistor in

cascade, in order to obtain broadband low distortion characteristics. This is because the common-gate transistor in a cascode configuration has an impedance transformation effect and impedance matching and the drain-conductance (*gd*) can be improved. In order to attain a higher output power, GaN FET with high-voltage operation is used for the final stage, and the first stage consists of GaAs HJFET with low-voltage operation. For the distortion improvement in cascode configuration, the distortion cancellation technique that the first stage takes gain expansion so as to cancel the gain compression of final stage is proposed as shown in Fig. 6.30. The discussion pays attention to the relationship between *gm*-profile and AM-AM characteristics to acquire the desired AM-AM cancellation.

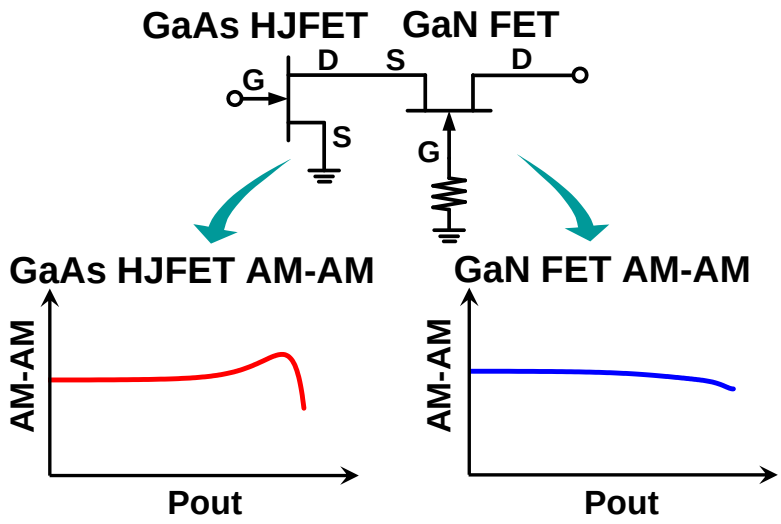


Fig. 6.30 Device configuration and distortion cancellation technique in CATV amplifier.

6.4.2 Volterra distortion analysis on load-line

Supposing RF operation, Volterra distortion analysis on a load-line which is different from the conventional Volterra series analysis described in Chapter 4 is performed. Volterra distortion analysis is a useful method in estimating the distortion characteristics directly from *I-V* characteristics [6.20], [6.21]. First, the expression of the relations of the drain-current (I_d), gate-voltage (v_g) and drain-voltage (v_d) is found from the *gm*, *gd* and the load (Z_L) of the equivalent circuit shown in Fig. 6.31. In a weak nonlinear region, the drain current model of a transistor can be expressed by the power-series expansion of two variables of v_g and v_d as follows [6.22].

$$I_d(v_g, v_d) = \sum_{n=0}^{\infty} \sum_{k+l=n} \frac{\partial^{k+l} I_d}{\partial {v_g}^k \partial {v_d}^l} \frac{{v_g}^k}{k!} \frac{{v_d}^l}{l!} \tag{6.6}$$

If the conditional expression (6.7) that operates on the Z_L is substituted for a formula (6.6), I_d on the Z_L can be found and it will become a polynomial of v_g as shown in (6.8).

$$v_d = -\frac{Z_L \cdot gm}{1 + Z_L \cdot gd} v_g \tag{6.7}$$

$$I_d(v_g) = \sum_{n=0}^{\infty} gm_n \frac{{v_g}^n}{n!} \tag{6.8}$$

where gm_n is gm on the Z_L, and is defined as follows.

$$gm_n = \frac{\partial^n I_d}{\partial {v_g}^n} \tag{6.9}$$

AM-AM characteristics can be found from the coefficient of fundamental current wave by expanding (6.8) up to 12th-order as (6.10).

$$\begin{aligned} i_d(\omega_1) = {} & gm_1 \cdot A + \frac{9}{4}\frac{gm_3}{3!} \cdot A^3 + \frac{25}{4}\frac{gm_5}{5!} \cdot A^5 \\ & + \frac{1225}{64}\frac{gm_7}{7!} \cdot A^7 + \frac{3969}{64}\frac{gm_9}{9!} \cdot A^9 + \frac{53361}{256}\frac{gm_{11}}{11!} \cdot A^{11} \end{aligned} \tag{6.10}$$

Also, 3rd-order intermodulation distortion (IM3) characteristics can be expanded as the following formula (6.11).

$$\begin{aligned} i_d(2\omega_1 - \omega_2) = {} & \frac{3}{4}\frac{gm_3}{3!} \cdot A^3 + \frac{25}{8}\frac{gm_5}{5!} \cdot A^5 \\ & + \frac{735}{64}\frac{gm_7}{7!} \cdot A^7 + \frac{1323}{32}\frac{gm_9}{9!} \cdot A^9 + \frac{38115}{256}\frac{gm_{11}}{11!} \cdot A^{11} \end{aligned} \tag{6.11}$$

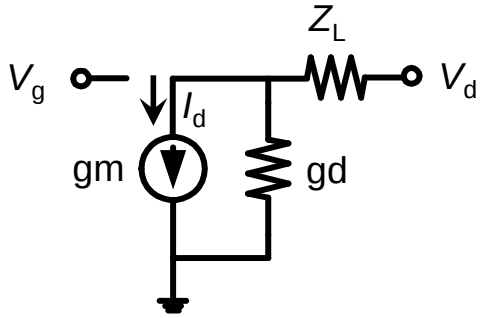


Fig. 6.31 Equivalent circuit performed Volterra distortion analysis on a load-line.

Moreover, using the circuit configuration shown in Fig. 6.32, capacitance analysis on the Z_L can be similarly performed from measured *S*-parameters for high frequency distortion

characteristics [6.23]. The current source data were obtained by pulsed *I*-*V* measurement. C_{gs} (v_g, v_d), C_{gd} (v_g, v_d), and C_{ds} (v_g, v_d) show the gate-to-source capacitance, gate-to-drain capacitance, and drain-to-source capacitance, respectively, extracted by voltage sweep measurement of *S*-parameters. In the circuit configuration of Fig. 6.32, v_d sweeps on the Z_L due to the self-bias effect as the v_g sweeps. Capacitance analysis on a load line can be conducted by performing small-signal analysis simultaneously with this operation.

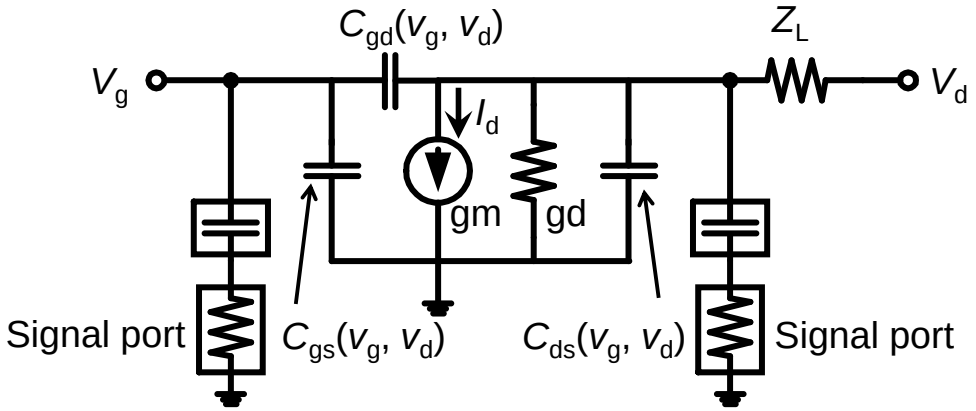


Fig. 6.32 Equivalent circuit performed capacitance analysis on a load-line from measured *S*-parameters.

6.4.3 Investigation of relationship between gm-profile on load-line and gain characteristics

To understand the relationship between *gm*-profile on a load-line and gain-characteristics, the gain characteristics were investigated by performing Volterra distortion analysis with various *gm*-profiles expressed as the following model formula.

$$gm = gm1 + gm2 \tag{6.12}$$

$$gm1 = \frac{1}{4} gm01 \cdot \left(1 + \tanh(-\alpha 11 \cdot (v_{gs} - v_g 11))\right) \cdot \left(1 + \tanh(\alpha 21 \cdot (v_{gs} - v_g 21))\right) \tag{6.13}$$

$$gm2 = \frac{1}{4} gm02 \cdot \left(1 + \tanh(-\alpha 12 \cdot (v_{gs} - v_g 12))\right) \cdot \left(1 + \tanh(\alpha 22 \cdot (v_{gs} - v_g 22))\right) \tag{6.14}$$

where $gm01$, $gm02$, $\alpha 11$, $\alpha 21$, $\alpha 12$, $\alpha 22$, $v_g 11$, $v_g 21$, $v_g 12$, $v_g 22$ indicate the constants.

The *gm*-profile expressions correspond to the relational expression of an Angelov-model [6.24], [6.25]. It is expressed with the sum of two *gm*-profiles (= *gm*1 + *gm*2) to give a

flat-*gm* point near the bias point. The *gm*2 was added to *gm*1 in order to show the expansion of *gm*.

Figure 6.33 (a), (d) shows *gm*-profile and the calculation results of the gain versus input power (P_{in}) characteristics, respectively. Figure 6.33 includes the 3rd-order coefficient of *gm* (gm_3) and (*gm*1, *gm*2) profiles. The *gm*-profile type -a and -b have the flat-*gm* point near the bias point and show expansion of *gm*. The gm_3 is positive. At that time, the calculated gain characteristics become expansion. The *gm*-profile type -c, -d, and -e without flat-*gm* point near the bias point or with *gm* compression turn out to be gain compression characteristics. Then, the gm_3 is negative. Thus, the behavior of gain characteristics can be adjusted by the *gm*-profile design.

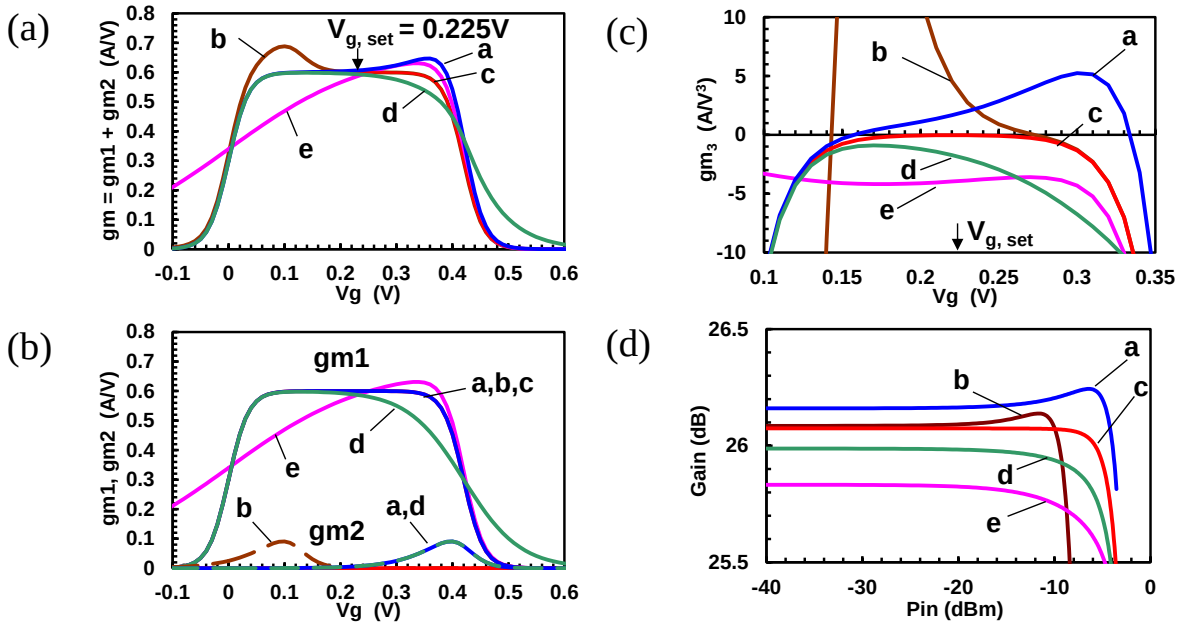


Fig. 6.33 (a) *gm*-profile expressed as model formula, (b) *gm*1 and *gm*2 profile, (c) gm_3-profile, and (d) calculation results of gain characteristics.

6.4.4 Optimization of device structure

6.4.4.1 GaAs HJFET for first stage of cascode configuration

The schematic cross-section of GaAs HJFET for first stage is shown in Fig. 6.34. High *gm* characteristics can be obtained applying double-doped double-hetero structure. Gate-length (L_g) is 0.5 μm. Gate-width (W_g) is 1.6 mm. In cascode configuration, to compensate the gain compression of final stage device, the first stage device needs to have

the gain expansion characteristics slightly at near Class-A operation. In order to obtain desired gain expansion characteristics, the doping concentration and the thickness of the upper and lower AlGaAs supply layer were optimized.

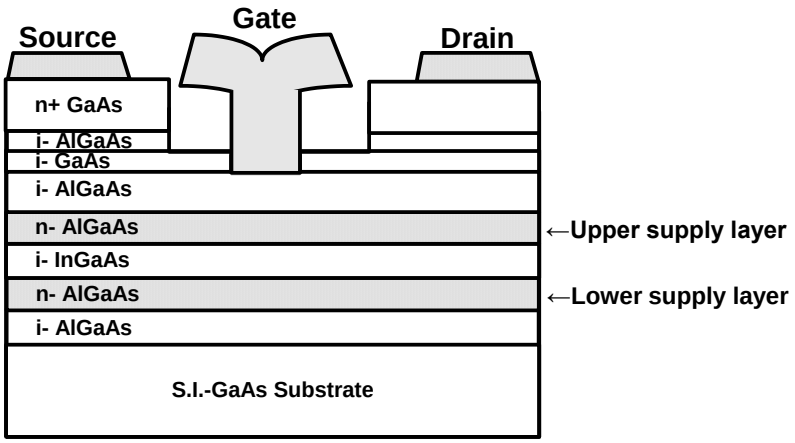


Fig. 6.34 Schematic cross-section of GaAs HJFET for first stage.

Table 6.2 shows the doping concentration and the thickness of upper supply layer and lower supply layer before and after the optimization which are shown in (A) and (B), respectively. The conventional structure (A) has the same doping concentration in the upper supply layer and the lower supply layer. On the other hand, the improved structure (B) was designed to have higher doping concentration and thinner thickness in the upper supply layer than the lower supply layer. The threshold-voltage (V_{th}) of both structures is −0.3 V. Figure 6.35 shows comparison of the measured pulsed *I-V* from DC-stress of 4 V and 100 mA/mm against the structure (A) and the structure (B).

Table 6.2 Doping concentration and thickness of supply layer.

Type	Upper supply layer	Lower supply layer
(A)	2.5×10^{18} cm^{-3} / 130 Å	2.5×10^{18} cm^{-3} / 50 Å
(B)	1.5×10^{19} cm^{-3} / 35 Å	1×10^{18} cm^{-3} / 100 Å

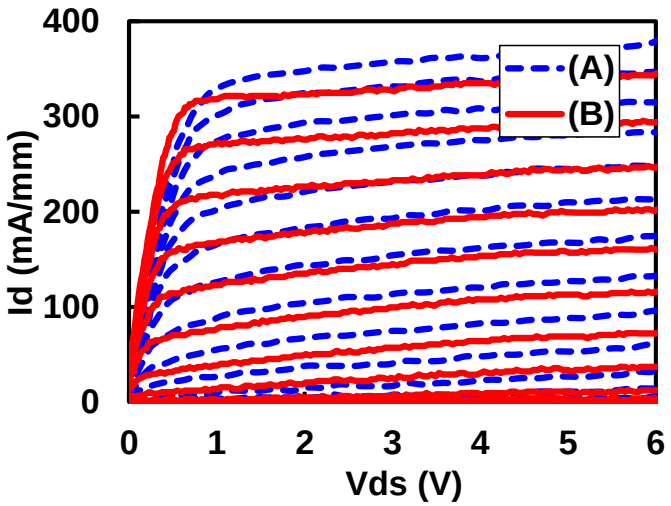


Fig. 6.35 Comparison of the pulsed *I-V* from DC-stress of 4 V, 100 mA/mm before (A) and after (B) the optimization of epitaxial structure.

Figure 6.36 shows comparison of *gm*-profile and gm_3-profile on $Z_L = 30\ \Omega$ estimated from the pulsed *I-V*. Furthermore, the measurement results and the calculated results of the gain versus output power (P_{out}) characteristics ($f_0 = 1$ GHz) at $Z_L = 30\ \Omega$ are shown in Fig. 6.37. Bias conditions are $V_d = 4$ V and $I_d = 200$ mA. As shown in the figures, the measurement result is comparatively well in agreement with the tendency of Volterra distortion analysis. With the conventional device (A), the pulse *gm*-profile on the load-line becomes "mountain-type" around the bias point of 200 mA. The value of gm_3 was negative around 200 mA. The gain characteristic becomes the gain compression. In an improved device (B), a flat-*gm* point is seen near the bias point of 200 mA because the pulse *gm*-profile on a load-line has the expansion of *gm* at the high-current and low-current side around the bias point. That is to say, it shows *gm*-profile with "double humps". The gm_3 showed positive value around 200 mA. The structure (B) with high aspect ratio is advantageous to obtain high *gm* at low current bias point. Thereby, the gain characteristic becomes the gain expansion characteristic as designed.

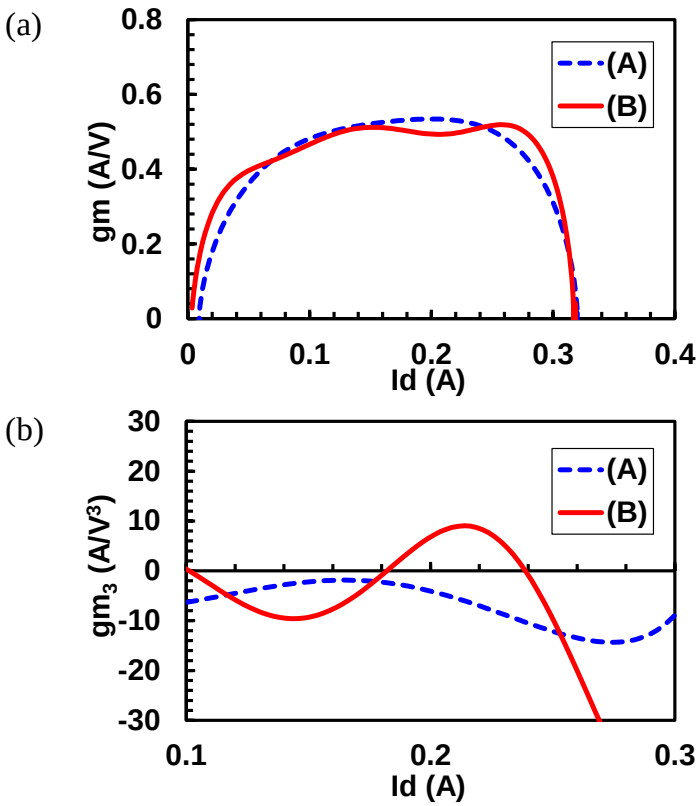


Fig. 6.36 Comparison of (a) measured *gm*-profile and (b) gm_3-profile on Z_L = 30 Ω.

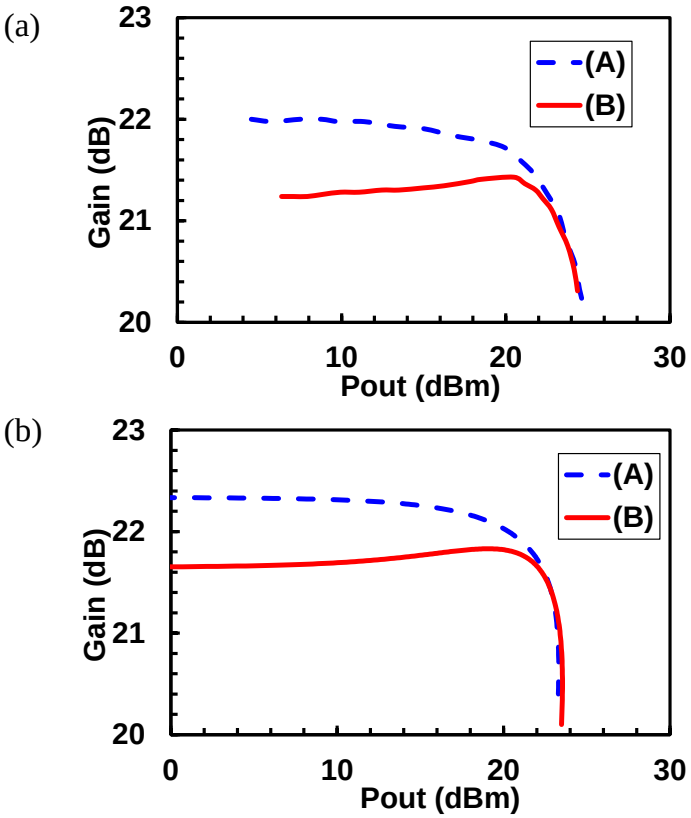


Fig. 6.37 (a) Measurement results and (b) calculated results of the gain characteristics at Z_L = 30 Ω, V_d = 4 V, and I_d = 200 mA.

6.4.4.2 GaN FET for final stage of cascode configuration

The schematic cross-section of GaN FET for final stage is shown in Fig. 6.38. In order to realize the high output power, high reliability, and also cost reduction, the AlGaN/GaN hetero-structure FET (HFET) formed on the HR Si substrate was developed, because greater importance was attached to the low distortion characteristics than the high temperature operation characteristics in CATV power amplifiers of which the output-power is small compared to base station amplifiers. For high voltage operation, dual field-plates (FP) technology in which one of the FP electrodes (Gate-FP) is connected to the gate and the other (Source-FP) to the ground was employed. L_g is 0.6 μm. W_g is 1.6 mm. V_{th} is −2V. In cascode configuration, a final device is common-gate.

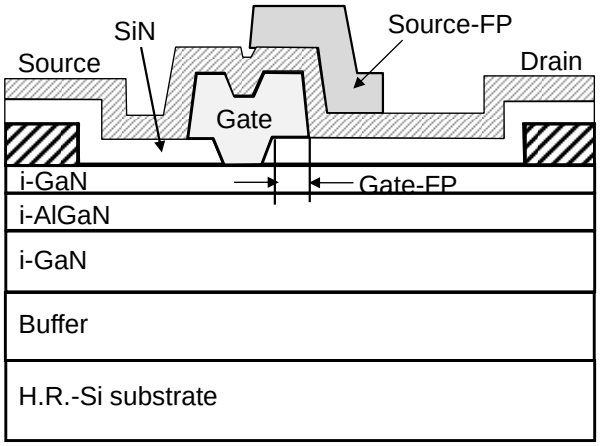


Fig. 6.38 Schematic cross-section of GaN FET for final stage.

Figure 6.39 shows the measured *gm*-profile and gm_3-profile on the load-line of 84 Ω and the AM-AM characteristics estimated from the *gm*-profile about common-gate GaN FET. The common-gate GaN FET has negative gm_3-profile around the bias point of 200 mA (note the reversed vertical axis) and it shows the gain compression characteristics. Thus, without frequency-dependence, the gain expansion of first-stage GaAs HJFET can cancel the gain compression of final-stage GaN FET. However, for high frequency distortion characteristics, the capacitance nonlinearity must be considered. The nonlinearity of C_{gd} of a final stage transistor influences the high frequency distortion characteristic as nonlinear output capacitance in a cascode configuration shown in Fig. 6.40. The linearity improvement of C_{gd} of GaN FET was considered. Figure 6.40 shows the measurement results of Gate-FP length dependence (0.1 μm and 0.3 μm) of C_{gd} versus I_{ds} on Z_L = 84 Ω about GaN FET. It is found that the nonlinearity of C_{gd} can be improved by shortening Gate-FP length.

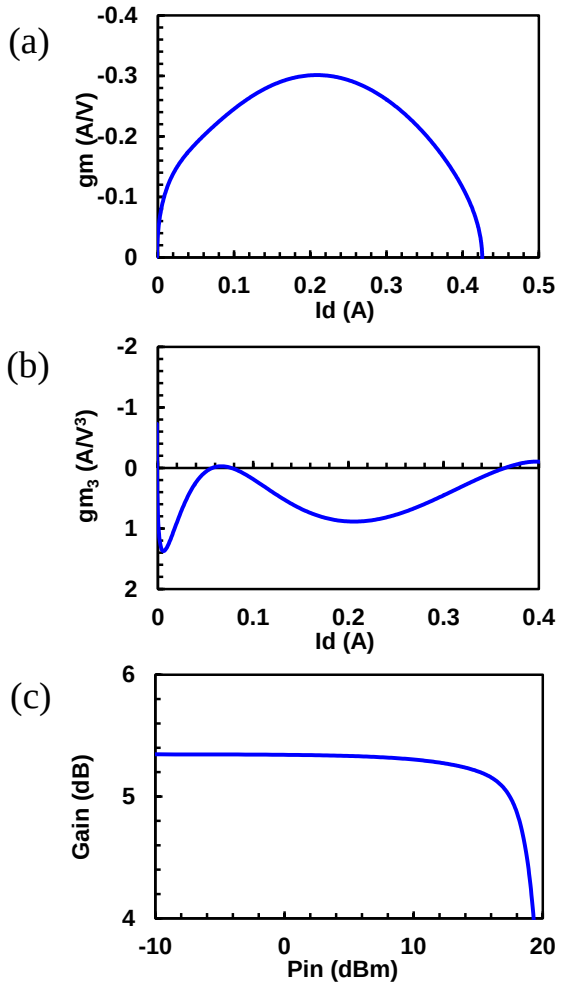


Fig. 6.39 (a) Measured *gm*-profile and (b) gm_3-profile on Z_L = 84 Ω and (c) AM-AM characteristics estimated from *gm*-profile about common-gate GaN FET.

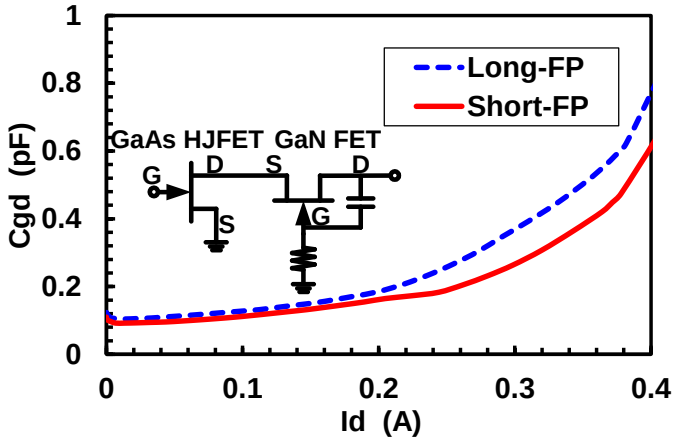


Fig. 6.40 Measurement results of Gate-FP length dependence of C_{gd} versus I_{ds} on Z_L = 84 Ω about GaN FET.

6.4.5 Circuit optimization

To achieve AM-AM cancellation to a broad bandwidth in GaAs/GaN cascode configuration, the design of W_g and inter-stage impedance is described.

6.4.5.1 W_g design of cascode configuration

Changing the W_g of a first stage FET is equivalent to varying the appearance of the load on the *IV* characteristic of the first stage transistor. Figure 6.41 shows the IM3 characteristics in cascode configuration (Z_L = 84 Ω, V_d = 24 V, I_d = 200 mA) obtained using Volterra distortion analysis as described in Section 6.4.2. The W_g dependence against the structure (A) and structure (B) of first stage GaAs HJFET is shown. The W_g of final stage GaN FET is 1.6 mm. The cascode amplifier using the structure (A) for first stage GaAs HJFET which shows gain compression characteristics has no room to improve the IM3 versus P_{out} characteristics by W_g dependence. On the other hand, the cascode amplifier with the structure (B) for the first stage GaAs HJFET which shows gain expansion characteristics has a point to improve the IM3 versus P_{out} characteristics by W_g dependence. This indicates that the optimization of broadband distortion cancellation is also possible by *gm* adjustment by W_g if the first stage transistor operates in gain expansion without frequency dependence. The 1.6 mm as the W_g of the GaAs HJFET was chosen.

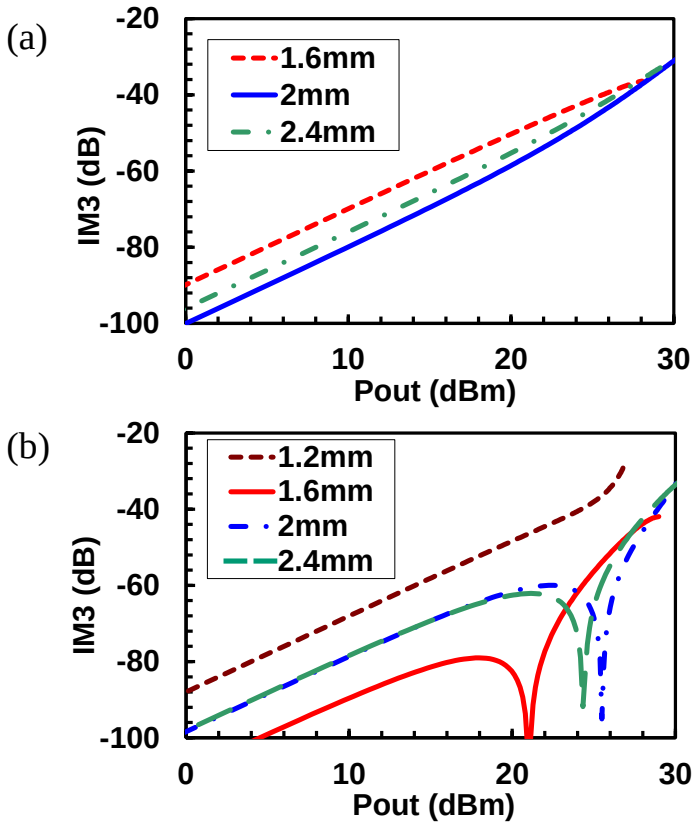


Fig. 6.41 IM3 characteristics in cascade configuration (Z_L = 84 Ω, V_d = 24 V, I_d = 200 mA) obtained by Volterra distortion analysis as a function of W_g against (a) structure (A) and (b) structure (B) of first stage GaAs HJFET.

6.4.5.2 Inter-stage impedance design of cascode configuration

The design of the inter-stage impedance of cascode configuration for broadband and low distortion characteristics is described. In cascode configuration, to acquire stability and bandwidth characteristics, the gate side of the common gate transistor is grounded through the resistance. In the cascode configuration, the load impedance for first stage FET, namely, input impedance of common gate final stage FET ($Z_{\text{in, CG}}$) is expressed as the following formula (6.15) using the equivalent circuit in Fig. 6.42 (a). The gate resistance (R_{g}) of common gate final stage FET influences the load impedance characteristics in high frequency for first stage FET through the gate capacitance (C_{gs}) of final stage FET.

$$Z_{in,\ CG} = \frac{gm + \omega^2 \cdot {C_{gs}}^2 \cdot R_g + j\omega \cdot C_{gs} \cdot \left(R_g \cdot gm - 1\right)}{gm^2 + \omega^2 \cdot {C_{gs}}^2} \tag{6.15}$$

where *gm* shows the transconductance of final stage common-gate FET.

The frequency dependence of the load impedance for first stage transistor becomes a factor which worsens the bandwidth characteristics of the distortion characteristic in the entire amplifier. In the cascode configuration with 1.6-mm GaAs HJFET for first stage transistor and 1.6-mm GaN FET for final stage transistor, the frequency characteristics (40 MHz to 1.2 GHz) of the load impedance for first stage transistor are calculated in Fig. 6.42 (b) for three gate resistances of final stage transistor ($R_{\text{g, ex}}$). The C_{gs} and *gm* of 1.6-mm GaN FET are 4.4 pF and 300 mS, respectively. In the case of high gate resistance, the load impedance of a first stage transistor becomes high at high frequency side through the gate capacitance of a final stage transistor. The load impedance at low frequency side for a first stage transistor becomes approximately 1/*gm* (in this case, low value of about 3 Ω) of a final stage transistor. Thus, since the load impedance of a first stage transistor has large frequency dependence if gate resistance is high, the low distortion characteristics cannot be obtained to a broad bandwidth. To acquire broadband low distortion characteristics, the gate resistance is necessary to be as small as possible in the range which can ensure the stability. The 30 Ω as the $R_{\text{g, ex}}$ of the GaN FET was chosen.

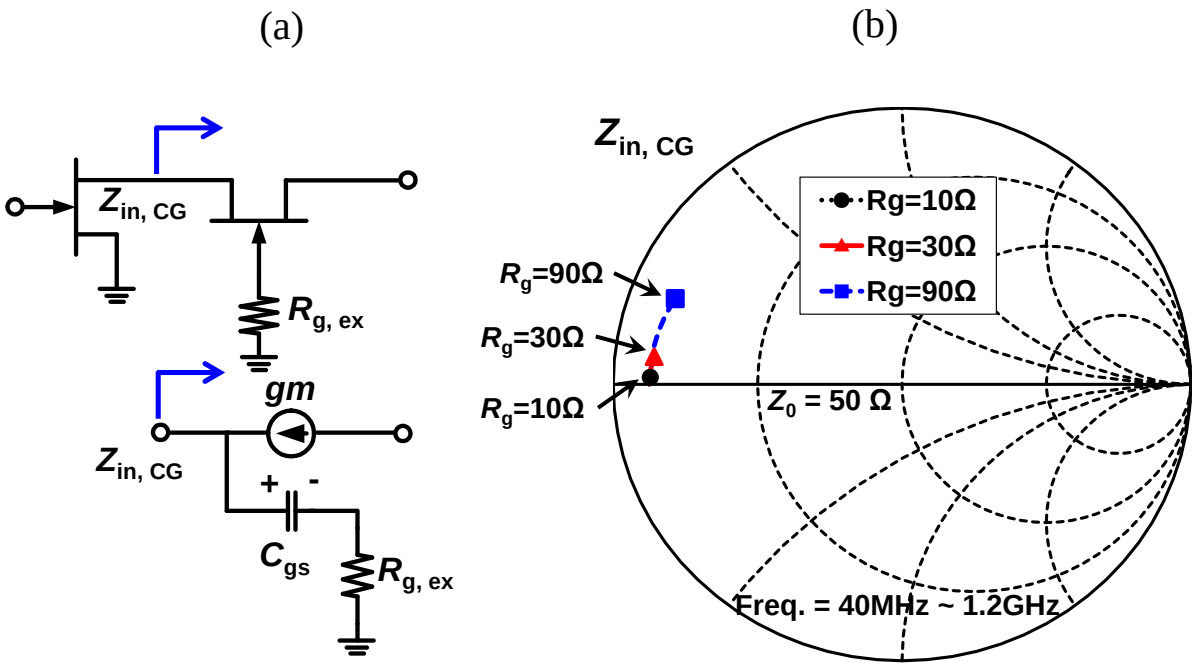


Fig. 6.42 (a) Equivalent circuit of common gate FET and (b) calculated frequency characteristics (40 MHz to 1.2 GHz) of input impedance of common gate FET for three gate resistances.

6.4.6 Amplifier performance

Figure 6.43 and 6.44 show the equivalent circuit and photograph of the developed CATV amplifier, respectively. The input and output power of the GaAs HJFET/GaN FET cascode amplifier are combined in push-pull configuration with balun circuits. The impedance transformation ratio of input balun is 1:1. Output balun consists of a two-stage transformer with the transformation ratio of 4:9 and 1:1. The GaAs HJFET and GaN FET chips were mounted on a plastic package. System impedance of all measurements is 75 Ω.

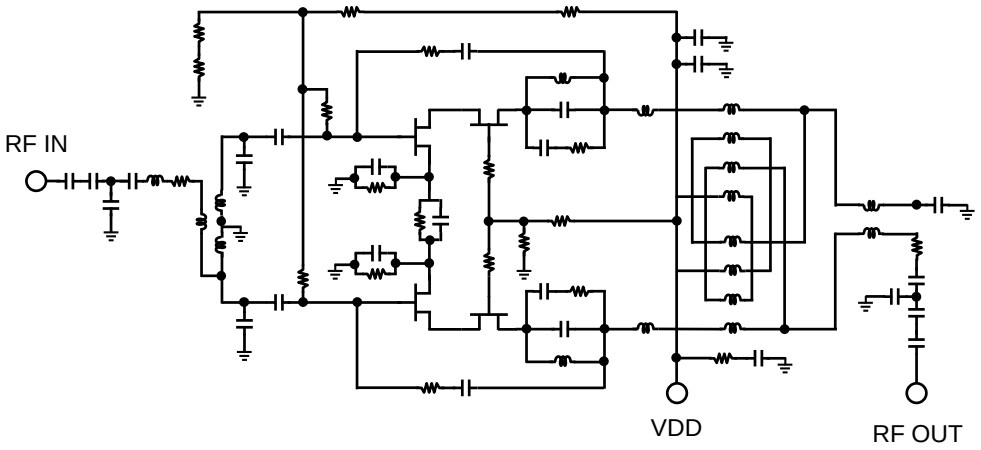


Fig. 6.43 Equivalent circuit of developed CATV amplifier.

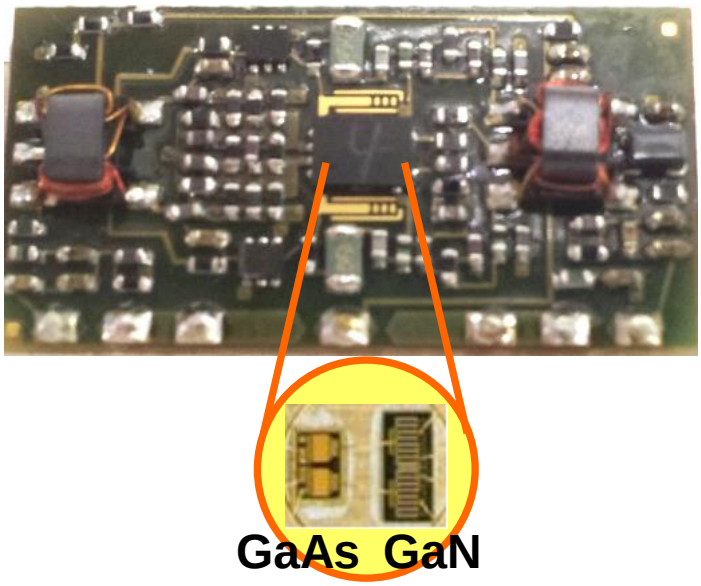


Fig. 6.44 Photograph of developed CATV amplifier and FET chips.

As shown in Fig. 6.45, the amplifier keeps the high linear-gain of more than 22 dB and the good return-loss of less than −20 dB with broad bandwidth from 40 MHz to 1 GHz.

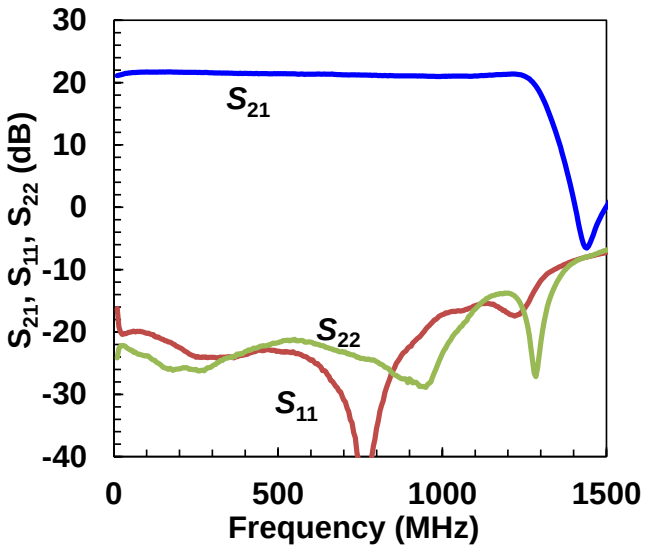


Fig. 6.45 S-parameters of CATV amplifier.

Figure 6.46 shows the composite-triple-beat (CTB) performance with the multi-carrier signal of 6-MHz-carrier-spacing, 132 ch, 11.7-dB-tilt, 53.7 dBmV at 865.25 MHz about the CATV amplifier before (A) and after (B) the epi-structure optimization of GaAs HJFET for the first stage described in Section-6.4.4.1. By using GaAs HJFET with gain expansion characteristics for first stage, CTB characteristics were significantly improved more than 10 dB from around 200 MHz to around 500 MHz.

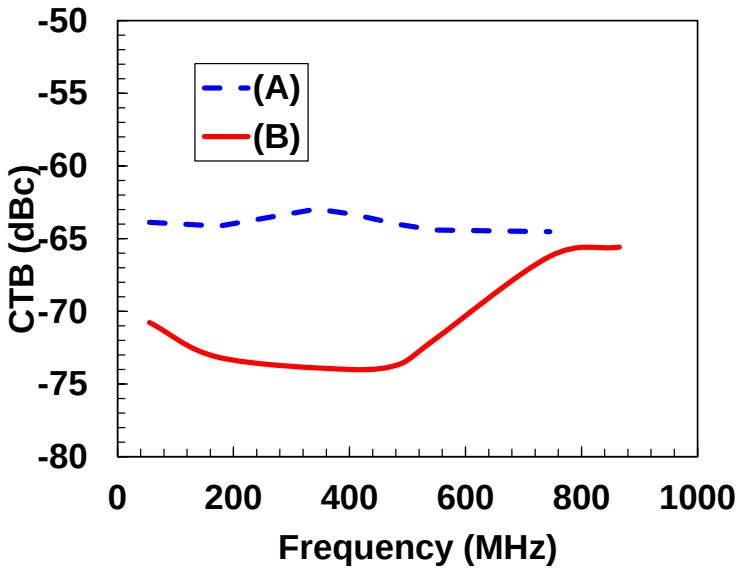


Fig. 6.46 CTB performance about CATV amplifier before (A) and after (B) the optimization of GaAs HJFET for the first stage.

Furthermore, as shown in Fig. 6.47, by shortening Gate-FP length of the final stage GaN FET, the CTB at high frequency side was improved more than 5 dB, and the developed amplifier attained the low CTB characteristics less than −72 dB at V_{ds} of 24 V and low quiescent drain current (I_{dq}) of 380 mA. Figure 6.48 shows CTB versus frequency characteristics for different I_{dq}. Low CTB characteristics less than −70 dBc at a wide I_{dq} condition from 360 mA to 420 mA were confirmed. The CTB versus P_{out} characteristics are shown in Fig. 6.49, and the amplifier delivered the crash point (CP) of P_{out} more than 58 dBmV with 132 ch multi-carrier signals.

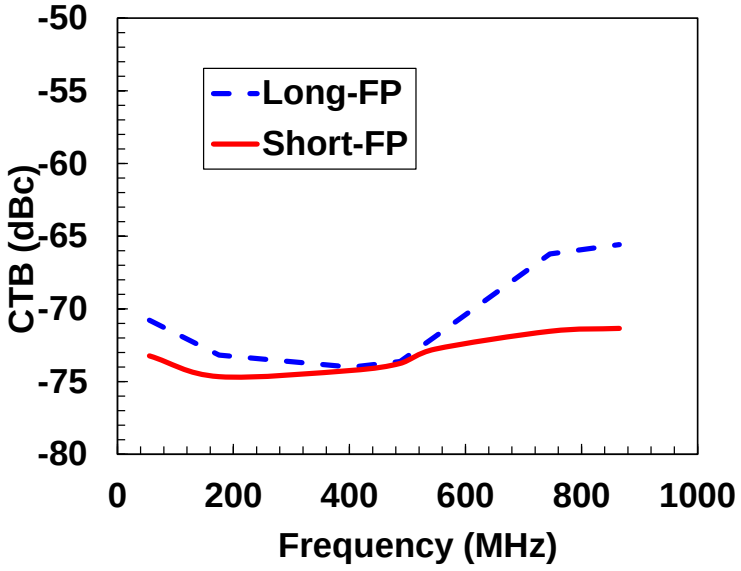


Fig. 6.47 CTB performance as the function of Gate-FP length of the final stage GaN FET.

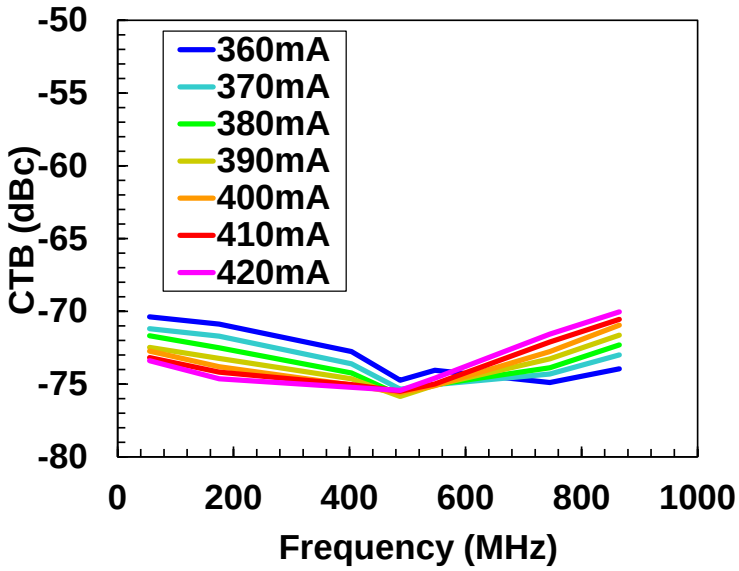


Fig. 6.48 CTB versus frequency characteristics for different *I*dq.

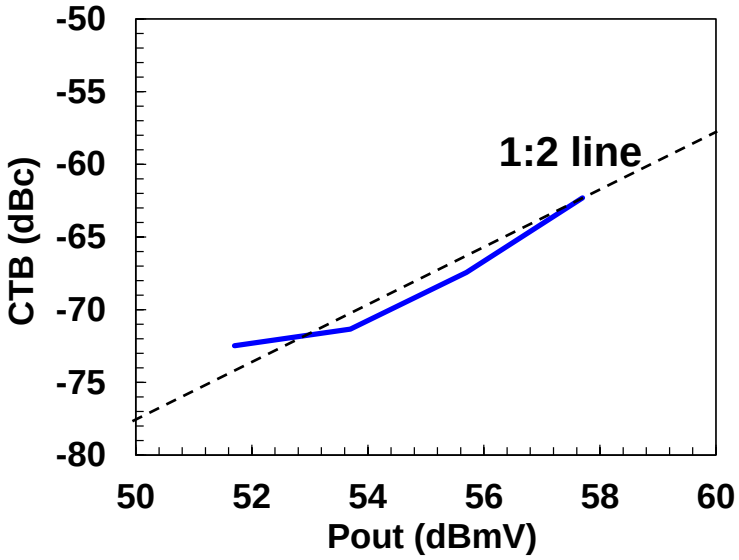


Fig. 6.49 CTB versus P_{out} characteristics of developed amplifier.

In Fig. 6.50, the CTB versus I_{dq} characteristics of this work to other products were compared [6.26], [6.27], converting into the same output power condition of 53.7 dBmV at 865.25 MHz with 132 ch and 11-dB-tilt. Low distortion characteristics with lower drain current compared with the other reports can be realized. These results demonstrate the deployment to the broadband, efficient, and low distortion amplifier of GaN FET, and proposed distortion cancellation technique contributes to the significant advance of a CATV system.

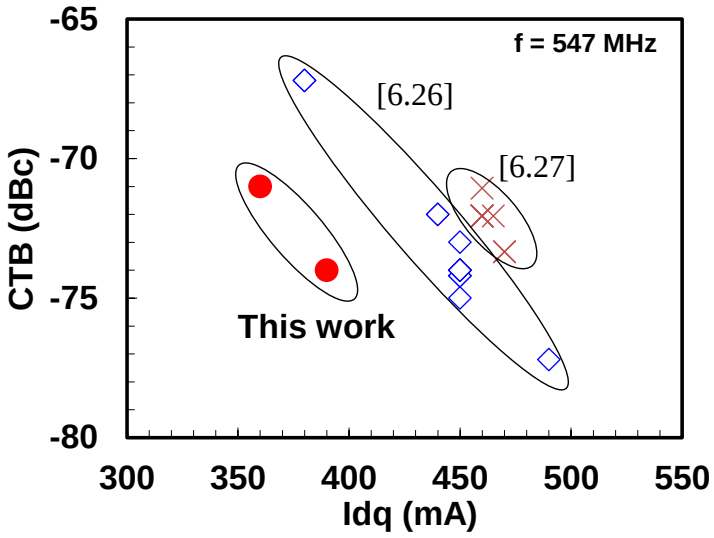


Fig. 6.50 CTB versus *I*dq characteristics comparison.

6.5 Summary

Chapter 6 described the study on broadband, high efficiency, and low distortion microwave high-power amplifiers using GaN FETs. Employing the GaN FETs of high voltage operation and high power density, the realization of high performance that cannot be achieved with conventional devices was aimed in this study. What has been demonstrated is as follows.

High efficiency and high power microwave amplifiers using GaN FET on LR Si substrate have been successfully developed for the first time.

By adopting low resistivity Si substrate whose resistivity is less sensitive over temperature, the efficiency characteristics in high temperature operation were significantly improved.

For efficiency improvement issue of GaN FET on LR Si substrate, it was aimed to improve RF loss by lowering resistance of the substrate and reducing C_{ds}.

High efficiency characteristics were realized by optimizing the buffer structure and electrode structure. In addition, the efficiency improvement by second harmonic termination of GaN FET on LR Si substrate was examined.

The single-ended amplifier realized the P_{sat} of 54 dBm, the GL of 19 dB, and the high efficiency of 33.5% at 8-dB back-off output power level under a WCDMA signal condition of 2.14 GHz at a 50-V-operation.

The Doherty amplifier delivered the P_{sat} of 57.3 dBm with the GL of 15.5 dB under a pulsed CW signal condition of 2.14 GHz, and demonstrated the DPD linearization characteristics with the high efficiency of 48% and the ACLR of −55 dB at a 50-dBm output power level under a WCDMA signal condition of 2.14 GHz.

Newly developed GaN FET on LR Si substrate technology contributes to the coexistence of high performance and low cost in the high-power microwave GaN device.

The broadband CATV amplifier with the lowest CTB performance less than −72dB has been successfully developed using the distortion cancellation technique of GaAs HJFET and GaN FET cascode amplifier.

For the distortion improvement in cascode configuration, the distortion cancellation technique that the first stage GaAs HJFET takes gain expansion to cancel the gain compression of final stage GaN FET was proposed employing Volterra distortion analysis on the load-line for *gm*-profile optimization.

The developed amplifier demonstrates broadband, low current and low distortion characteristics for a modern CATV system.

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Chapter 7

Conclusions

7.1 Summary of this dissertation

This study-achievement is related to the unique and practical studies of the matching circuit and the power combiner circuit which make it possible to maximize the performance of the microwave transistors used in the high power amplifiers. This dissertation summarized the results having contributed to significant performance improvements of microwave high-power FET amplifiers used for communication systems.

Chapter 1 described the history and technology trends of microwave high-power device development as a background of this study. Next, the composition of a microwave high power amplifier and the problem of the device and circuit technique in high power amplifier were described. Then, the purpose and meaning of a main subject were described and the composition of a main subject was shown.

Chapter 2 described a study on the push-pull power combining circuit and the stability analysis under the large-signal operation for microwave high-power amplifiers. An L/S-band high-power and low-distortion AlGaAs/GaAs HFET push-pull amplifier has been developed using a low-loss microstrip balun. At 2.2 GHz, an output power of 140 W has been obtained with 11.5-dB linear gain and 42% power-added efficiency. Under two-tone test conditions (2.2 GHz, 2.201 GHz), the amplifier exhibited low intermodulation distortion characteristics of less than −30 dBc at two-tone total output-power of 46 dBm. The developed HFET amplifiers are promising for improving RF power handling capability of digital cellular base station systems. In order to determine the loop gain occurring in the FET and the circuit at the large signal operation, the large signal loop gain analysis technique that combines the *S*-Probe circuit and the harmonic balance simulation was proposed. The proposed technique was

applied to the oscillation analysis at the large-signal operation in the internally-matched C-band 60-W power-FET. The simulation result well reproduced the actual oscillation phenomenon, and the effectiveness of this analysis was confirmed.

In Chapter 3, the harmonic termination techniques in the matching circuits were examined to achieve high efficiency characteristics in high power amplifiers. The voltage waveforms were observed using a large signal simulation and Electro Optical Sampling (EOS). The high efficiency termination condition of load second harmonic was found out to be open condition opposite to conventional Class-F. By clarifying the effect of the termination condition of source second harmonic, it was confirmed that the nonlinear gate-to-source capacitance (C_{gs}) affects the overlap of the voltage and the current waveforms. An L/S-band highly efficient 320-W GaAs FET amplifier has been developed by employing the second-harmonic termination technique in both the input and output matching circuits. At 2.12 GHz, an output power of 320 W has been obtained with 62% drain-efficiency and 14-dB linear gain. Under a two-carrier W-CDMA signal condition, the amplifier exhibited low IM3 performance of less than –37 dBc with high drain-efficiency of 30% at an output-power of 47.5 dBm. The developed GaAs HJFETs are promising for the 3rd generation digital cellular base station applications.

Chapter 4 described the study on low distortion microwave high power amplifiers. It is necessary to clarify the policy of device structure optimization and circuit design in order to achieve high efficiency and low distortion characteristics. Focusing on *gm*-profile of GaAs HJFET, it was found that HJFET with shallow threshold voltage (V_{th}) and steep *gm*-profile has small third-order coefficient of *gm* (gm_3) at deep Class-AB, and exhibits low distortion characteristics. Furthermore, the influence of second harmonic and difference frequency impedance on third-order distortion characteristics was investigated using Volterra analysis. The circuit configuration terminating source- and load-second harmonics with short impedance was newly proposed. An L/S-band 150-W GaAs HJFET employing the second harmonic termination circuits realized low third-order intermodulation distortion (IM3) characteristics less than −40 dB. In addition, the source- and load-difference frequency termination circuits in package as well as the technique lowering drain bias circuit impedance were proposed. The proposed techniques realized low distortion characteristics without degradation over 100-MHz frequency-spacing (Δf). The result is the widest bandwidth and

low distortion characteristics so far, and the deployment to next-generation mobile communications such as a fourth generation (4G) can be expected.

Chapter 5 described the study on low distortion and high efficiency Doherty amplifiers. In this study, it was clarified that the optimal configuration of Doherty amplifier is present based on the impedance of the device load-pull characteristics. The design approach to perform the distortion compensation in Doherty amplifier was proposed using the distortion cancellation effect of the main and the peak amplifier in power-combining. An L/S-band 330-W distortion-cancelled Doherty GaAs FET amplifier has been successfully developed. The amplifier demonstrated, under a two-carrier W-CDMA condition, low IM3 of less than −37 dBc with a 42% drain-efficiency at a P_{out} of 49 dBm. It achieved significant improvements in efficiency without degradation in linearity. In addition, the evaluation techniques of each AM-AM and AM-PM characteristics of the main and the peak amplifiers in an operating Doherty amplifier were proposed, and the distortion cancellation of the main and the peak amplifiers in Doherty amplifier linearity was experimentally proved for the first time. Furthermore, the IMD asymmetries of Doherty amplifier were analyzed through the IMD vector combination of the main and the peak amplifiers. A developed 28-V-operation 200-W GaAs HJFET Doherty amplifier with source and load baseband terminations delivered flat IMD characteristics against the Δf over 50 MHz.

Chapter 6 described the study on broadband, high efficiency, and low distortion microwave high-power amplifiers using GaN FETs. Employing the GaN FETs of high voltage operation and high power density, the realization of high performance that cannot be achieved with conventional devices was aimed in this study. High efficiency and high power microwave amplifiers using GaN FET on LR Si substrate have been successfully developed for the first time. By adopting low resistivity Si substrate whose resistivity is less sensitive over temperature, the efficiency characteristics in high temperature operation were significantly improved. For efficiency improvement issue of GaN FET on LR Si substrate, it was aimed to improve RF loss by lowering resistance of the substrate and reducing C_{ds}. High efficiency characteristics were realized by optimizing the buffer structure and electrode structure. In addition, the efficiency improvement by second harmonic termination of GaN FET on LR Si substrate was examined. The single-ended amplifier realized the P_{sat} of 250 W, the GL of 19 dB, and the high efficiency of 33.5% at 8-dB back-off output power level under

a WCDMA signal condition of 2.14 GHz at a 50-V operation. The Doherty amplifier delivered the P_{sat} of 537 W with the GL of 15.5 dB under a pulsed CW signal condition of 2.14 GHz, and demonstrated the DPD linearization characteristics with the high efficiency of 48% and the ACLR of −55 dB at a 50-dBm output power level under a WCDMA signal condition of 2.14 GHz. Newly developed GaN FET on LR Si substrate technology contributes to the coexistence of high performance and low cost in the high-power microwave GaN device. The broadband CATV amplifier with the lowest CTB performance less than −72 dB has been successfully developed using the distortion cancellation technique of GaAs HJFET and GaN FET cascode amplifier. For the distortion improvement in cascode configuration, the distortion cancellation technique that the first stage GaAs HJFET takes gain expansion to cancel the gain compression of final stage GaN FET was proposed employing Volterra distortion analysis on the load-line for *gm*-profile optimization. The developed amplifier demonstrates broadband, low current and low distortion characteristics for a modern CATV system.

Finally, Table 7.1 summarizes the performance of high-power amplifiers in this study. The results of this study contributed to the rapid progress of mobile communication system.

Table 7.1 Summary of the performance of the high power amplifiers in this study.

Type	Circuits	Devices	P_{sat}	GL	$\eta_{d,\,max}$	IMD3	Chap.
High-efficiency Amp.	Microstrip-balun $2f_0$ open Push-Pull	GaAs 28-V HJFET Dual-FP	320 W	14 dB	62%	–	2, 3
Low distortion Amp.	$2f_0$ short Difference-short Push-Pull	GaAs 12-V HJFET *gm*-profile	150 W	13 dB	–	−40 dBc (Δf > 100 MHz)	4
Doherty Amp.	Inverted-Doherty Cancellation	GaAs 28-V HJFET	330 W	14 dB	42%*	−37 dBc#1	5
GaN FET Amp.	Single-End Inverted-Doherty +DPD	GaN 50-V HFET	250 W 537 W	19 dB 15 dB	48%*	−55 dBc#2	6

* Drain-efficiency at 7-dB output back-off.
#1 IMD3 under a two carrier W-CDMA with 10-MHz carrier spacing.
#2 ACLR after DPD under a WCDMA signal with PAR of 7.3 dB.

7.2 Future issues and prospects

As stated so far, the advancement of microwave transistor amplifier technology has played a major role in the remarkable progress of today's large-capacity and high-speed communication system. The future issues and prospects are described based on the newest research and development trend in both sides of the device and the circuit techniques which constitute the microwave transistor amplifiers.

In mobile communications, it is predicted that by the spread of smart-phones and tablet-computers, mobile traffic increases to more than 1000 times in 2020 after 2010 [7.1]. The capacity enlargement of the wireless communication system has been an important issue. Against this, in order to correspond to the increase of traffic, increasing the density of network has been studied in the plan for the 5 G (the 5th generation) communication used as the next-generation telecommunications standard of LTE or LTE-Advanced. It is scheduled to improve the cost and coverage by installing a number of small cells whose transmission distance is short in place of the conventional macro-cell. Furthermore, in the LTE-advanced, the carrier aggregation (CA) technology which communicates using several LTE careers simultaneously is already introduced for effective use of broad bandwidth. By using the several frequency bands, the load distribution of base station and the stabilization of information communication are attained. To use the wide bandwidth of 1 GHz at the high-frequency band of 20 GHz is also examined [7.1].

More importance demanded for microwave amplifiers comes to be placed on high frequency, broadband, high efficiency, low distortion, and high reliability rather than the conventional higher output power demand to the trend of such a communication system. As the latest circuit techniques of microwave amplifiers, the research and development of not only Doherty and Envelope-Tracking amplifiers but also Class-D switching-mode [7.2], [7.3] and Outphasing amplifiers [7.4] are active. These circuit techniques have become a fierce competition to realize high efficiency to a broadband at high frequency. The techniques corresponding to CA or dual-band have been announced.

On the other hand, in the device, the high performance potential of GaN FET which is a wideband gap semiconductor has so far been demonstrated. The technical development of GaN FET focuses on the research of enhancement (normally-off) for high frequency switching devices. There are some normally-off AlGaN/GaN HEMT techniques as follows; utilizing the epitaxial growth of non-polar plane such as the m-plane and the a-plane [7.5], [7.6], canceling the polarization charge by providing a GaN or InGaN cap layer on the

AlGaN barrier layer [7.7], using the junction gate structure inserting a p-type GaN under the gate [7.8], [7.9], using a MOS structure employing a gate oxide film such as SiO_2 or Al_2O_3 [7.10], and so on. In order to overcome the Si device market, cost reduction and higher reliability are indispensable. The reports of 8-inch GaN-on-Si have been presented up to now [7.11], [7.12], and developments of larger diameter wafer are progressing. In the reliability, the relation between the inverse piezoelectric effect which generates the internal stress for the electric field stress of AlGaN/GaN HEMT, and the degradation mode continues to become clear [7.13], [7.14]. In addition to the optimization of the electrode structure and the AlN mole fraction, the research of InAlN/GaN HFET using a barrier layer of InAlN which is lattice-matched to GaN also has progressed [7.15]. As the newest GaN technology trends, there is a progress of the heterogeneous integration technology which accumulates the GaN and the control circuits of silicon-on-insulator (SOI) complementary metal-oxide-semiconductor (CMOS) on Si substrate targeting the microminiaturization of the system [7.16]. There is another problem of the heat dissipation in the integration of GaN. The Near Junction Thermal Transport (NJTT) technology which radiates the heat generating in the channel employing the diamond having a high thermal conductivity for a bonding-substrate [7.17] or a via-hole [7.18] has been attracting attention. If the E/D mixed-loading GaN HEMT development [7.19] and the device development for power managements [7.20] proceed, the GaN envelope-tracking amplifier which the GaN power amplifier and the GaN envelope amplifier are fabricated within one chip may be able to be realized in the near future.

In the future, the author would like to attempt the advancement of circuits and the microfabrication of devices in microwave power amplifiers, aiming at the both of higher efficiency and lower distortion in order to exceed more than 60% efficiency barrier rather than higher output-power. At present, the combination of envelope tracking amplifier and microfabricated GaN HEMT is one of the most promising candidates.

The circuit designers think to achieve the high performance of the system using the newest high-performance device. It is necessary to strive to maximize the device performance. Moreover, the device designers have to propose the optimal device structure suitable for the circuits. What is the reason which cannot bring out the device performance completely? Is there any method to control the frequency-dispersion and the thermal temporal change in the device? The unknown frontiers are left in the boundary region of the device and the circuit still more. The author has approached from both sides of the devices and the circuits for high-performance microwave amplifier. This dissertation is concluded wishing to be connected with the further development to unite the boundary of the device and the circuit.

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Appendix A. *S*-probe circuit

As shown in Fig. A.1, S-probe is the circuit with six ports which consist of large resistance (*R*s, *R*v) and a voltage dependent power supply with the coefficients of M_3 and M_4, and the circuit to measure the reflection coefficient is connected to the port 1 and the port 2. It is assumed that the impedances of Z_1 and Z_2 are connected to the port 1 and the port 2, respectively. These impedances are determined from the transmission characteristics from the port 5 and the port 6 to the port 3 and the port 4.

Due to *R*s and *R*v being very large resistance, a current hardly flows to the ports 6, 5, 3, and 4, and they do not affect the circuits of Z_1 and Z_2. Moreover, insertion loss can be ignored because R which connects Z_1 and Z_2 in series is set to a very small value.

As shown in Fig. A.1, if the current which flows to the circuit of Z_2 is expressed as i_2 when the voltage of the port 6 is given as V_6, the voltages of V_A and V_B in the nodes of A and B at the both ends of the resistance R are represented as the following formulas.

$$V_A = V_B + i_2 R = \frac{V_B (Z_2 + R)}{Z_2} \tag{A.1}$$

$$V_B = i_2 Z_2 \tag{A.2}$$

Moreover, the voltage V_3 at the port 3 and the voltage V_4 at the port 4 are represented as the following formulas.

$$V_3 = M_3 V_R = M_3 (V_A - V_B) = \frac{V_A M_3 R}{(Z_2 + R)} \tag{A.3}$$

$$V_4 = M_4 V_B \tag{A.4}$$

Therefore, the transmission characteristic from the port 6 to the ports 3 and 4 is expressed as the following formulas.

$$S_{36} = \frac{V_3}{V_6} = \frac{V_A M_3 R}{V_6 (Z_2 + R)} \tag{A.5}$$

$$S_{46} = \frac{V_4}{V_6} = \frac{M_4 Z_2 V_A}{V_6 (Z_2 + R)} \tag{A.6}$$

Similarly, as shown in Fig. A.2, if the current which flows to the circuit of Z_1 is set to i_1 when the voltage of the port 5 is given as V_5, the voltage of V_A and V_B in the nodes of A and B at the both ends of the resistance R are represented as the following formulas.

$$V_A = i_1 Z_1 \tag{A.7}$$

$$V_B = V_A + i_1 R = \frac{V_A (Z_1 + R)}{Z_1} \tag{A.8}$$

Moreover, the voltage V_3 at the port 3 and the voltage V_4 at the port 4 are represented as the following formulas.

$$V_3 = M_3 V_R = M_3 (V_A - V_B) = -\frac{V_B M_3 R}{(Z_1 + R)} \tag{A.9}$$

$$V_4 = M_4 V_B \tag{A.10}$$

Therefore, the transmission characteristic from the port 5 to the ports 3 and 4 is expressed as the following formulas.

$$S_{35} = \frac{V_3}{V_5} = -\frac{V_B M_3 R}{V_5 (Z_1 + R)} \tag{A.11}$$

$$S_{45} = \frac{V_4}{V_5} = \frac{M_4 V_B}{V_5} \tag{A.12}$$

Thus,

$$\frac{S_{46}}{S_{36}} = \frac{M_4 Z_2}{M_3 R} \tag{A.13}$$

$$\frac{S_{45}}{S_{35}} = -\frac{M_4 (Z_1 + R)}{M_3 R} \tag{A.14}$$

Here, if the conditional expression of

$$\frac{M_4}{M_3 R} = 1 \tag{A.15}$$

is selected, the following formulas are obtained.

$$Z_1 = -\frac{S_{45}}{S_{35}} \qquad (R \to 0) \tag{A.16}$$

$$Z_2 = \frac{S_{46}}{S_{36}} \tag{A.17}$$

In this way, the impedance of Z_1 and Z_2 can be found from the transmission characteristics from the ports 5 and 6 to the ports 3 and 4.

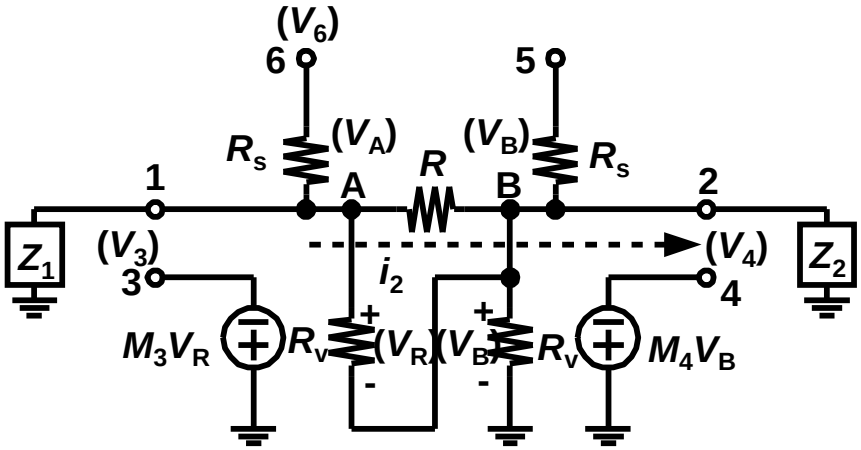

Fig. A.1 *S*-probe circuit when the voltage is given to V_6.

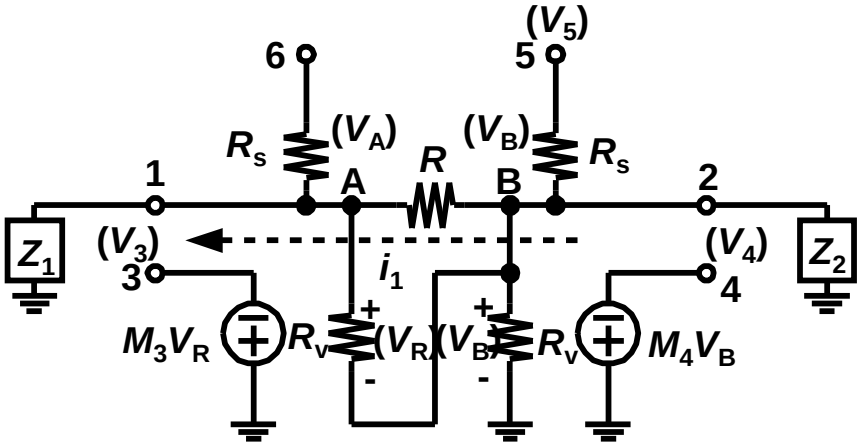

Fig. A.2 *S*-probe circuit when the voltage is given to V_5.

Appendix B. IMD3 asymmetries analysis in consideration of source- and load- difference frequency

As shown in Fig. B.1, in addition to IMD3 generated by third-order nonlinear processes, IMD3 also occurs by second-order nonlinear processes that mix the differential frequency and second harmonics with the fundamental frequencies. IMD3 asymmetries are caused by the termination impedances of the differential frequency and second harmonics [1]. In this study, the IMD3 analysis formula is expressed introducing the baseband and the second harmonic impedances of input circuits as well as output circuits by using Taylor-series approximation model with current and charge nonlinearity. The perturbation method is employed for IMD3 analysis instead of Volterra series analysis [2].

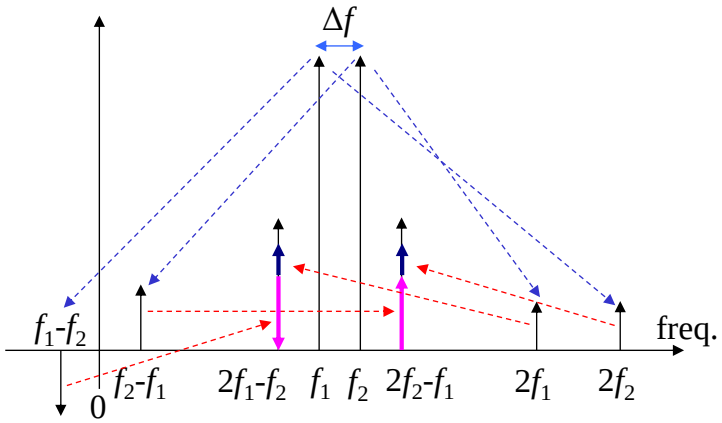

Fig. B.1 IMD3 asymmetries generation mechanism by second-order nonlinearity.

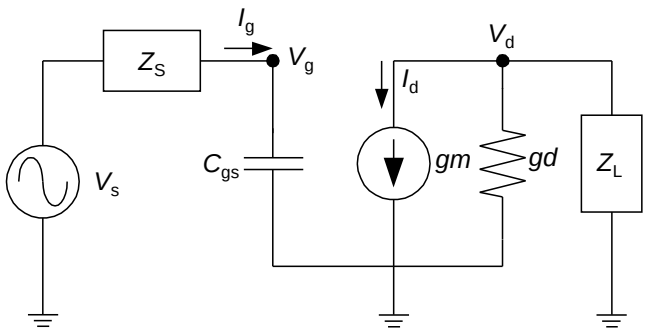

Fig. B.2 FET equivalent circuit used for analysis.

Figure B.2 shows the FET equivalent circuit used for analysis. If employing a two-tone signal of ω_1 and ω_2 ($\omega_1<\omega_2$) for the input signal V_s, the RF input signal initially occurs in the high frequency gate voltage v_g as follows.

$$v_g = A(\cos\omega_1 t + \cos\omega_2 t) \tag{B.1}$$

High frequency gate current *ig* is similar to the third-order term as a polynomial expression of gate-source nonlinear capacitance C_{gs} and v_g [3].

$$i_g = \frac{d}{dt}(C_{gs1}v_g + C_{gs2}v_g{}^2 + C_{gs3}v_g{}^3) \tag{B.2}$$

Again, v_g can be substituted for V_g expressed as follows using the fundamental frequency gate currents $i_{g,\,\omega1}$, $i_{g,\,\omega2}$, differential frequency gate current $i_{g,\,\omega2-\omega1}$, second harmonic gate currents $i_{g,\,2\omega1}$, $i_{g,\,2\omega2}$, and sum frequency gate current $i_{g,\,\omega1+\omega2}$, derived from (B.1) and (B.2) considering up-to second-order nonlinearities, and their source termination impedances Z_S.

$$\begin{aligned} V_g = {} & Z_{S,\,\omega1}\cdot i_{g,\,\omega1} + Z_{S,\,\omega2}\cdot i_{g,\,\omega2} + Z_{S,\,\omega2-\omega1}\cdot i_{g,\,\omega2-\omega1} \\ & + Z_{S,\,2\omega1}\cdot i_{g,\,2\omega1} + Z_{S,\,2\omega2}\cdot i_{g,\,2\omega2} + Z_{S,\,\omega1+\omega2}\cdot i_{g,\,\omega1+\omega2} \end{aligned} \tag{B.3}$$

Here,

$$i_{g,\,\omega1} = -(AC_{gs1} + \frac{9}{4}A^3C_{gs3})\omega_1 \sin\omega_1 t \tag{B.4}$$

$$i_{g,\,\omega2} = -(AC_{gs1} + \frac{9}{4}A^3C_{gs3})\omega_2 \sin\omega_2 t \tag{B.5}$$

$$i_{g,\,\omega2-\omega1} = -A^2C_{gs2}(\omega_2-\omega_1)\sin(\omega_2-\omega_1)t \tag{B.6}$$

$$i_{g,\ 2\omega1} = -A^2 C_{gs2} \omega_1 \sin 2\omega_1 t \tag{B.7}$$

$$i_{g,\ 2\omega2} = -A^2 C_{gs2} \omega_2 \sin 2\omega_2 t \tag{B.8}$$

$$i_{g,\ \omega1+\omega2} = -A^2 C_{gs2} (\omega_1 + \omega_2) \sin(\omega_1 + \omega_2) t \tag{B.9}$$

Next, as the first approximation, high frequency drain current i_d can be represented to the third-order term as a polynomial expression of transconductance g_m and v_g.

$$i_d = g_{m1} v_g + g_{m2} {v_g}^2 + g_{m3} {v_g}^3 \tag{B.10}$$

Also, high frequency drain voltage V_d can be expressed as follows using the fundamental frequency drain currents $i_{d,\ \omega1}$, $i_{d,\ \omega2}$, differential frequency drain current $i_{d,\ \omega2-\omega1}$, second harmonic drain currents $i_{d,\ 2\omega1}$, $i_{d,\ 2\omega2}$, and sum frequency drain current $i_{d,\ \omega1+\omega2}$, derived from (B.1) and (B.10) considering up-to second-order nonlinearities, and their load termination impedances Z_L.

$$\begin{aligned} V_d = {} & Z_{L,\ \omega1} \cdot i_{d,\ \omega1} + Z_{L,\ \omega2} \cdot i_{d,\ \omega2} + Z_{L,\ \omega2-\omega1} \cdot i_{d,\ \omega2-\omega1} \\ & + Z_{L,\ 2\omega1} \cdot i_{d,\ 2\omega1} + Z_{L,\ 2\omega2} \cdot i_{d,\ 2\omega2} + Z_{L,\ \omega1+\omega2} \cdot i_{d,\ \omega1+\omega2} \end{aligned} \tag{B.11}$$

Where,

$$i_{d,\ \omega1} = (A g_{m1} + \frac{9}{4} A^3 g_{m3}) \cos \omega_1 t \tag{B.12}$$

$$i_{d,\ \omega2} = (A g_{m1} + \frac{9}{4} A^3 g_{m3}) \cos \omega_2 t \tag{B.13}$$

$$i_{d,\ \omega2-\omega1} = A^2 g_{m2} \cos(\omega_2 - \omega_1) t \tag{B.14}$$

$$i_{d,\ 2\omega1} = \frac{1}{2} A^2 g_{m2} \cos 2\omega_1 t \tag{B.15}$$

$$i_{d,\ 2\omega2} = \frac{1}{2} A^2 g_{m2} \cos 2\omega_2 t \tag{B.16}$$

$$i_{d,\ \omega1+\omega2} = A^2 g_{m2} \cos(\omega_1 + \omega_2) t \tag{B.17}$$

For example, if the fundamental frequencies, differential frequency and second-harmonic band are terminated in load impedance R_L, inductance L_{ind1}, and inductance L_{ind2}, respectively, their drain voltages can be expressed as follows.

$$V_{d,\ \omega} = -R_L(i_{d,\ \omega 1} + i_{d,\ \omega 2}) = -R_L(Ag_{m1} + \frac{9}{4}A^3 g_{m3})(\cos\omega_1 t + \cos\omega_2 t) \tag{B.18}$$

$$V_{d,\ \omega 2-\omega 1} = -L_{ind1}\frac{di_{d,\ \omega 2-\omega 1}}{dt} = L_{ind1}(\omega_2 - \omega_1)A^2 g_{m2}\sin(\omega_2 - \omega_1)t \tag{B.19}$$

$$\begin{aligned} V_{d,\ 2\omega} &= -L_{ind2}\frac{d(i_{d,\ 2\omega 1} + i_{d,\ 2\omega 2})}{dt} \\ &= \frac{1}{2}A^2 g_{m2}(2\omega_1 L_{ind2}\sin 2\omega_1 t + 2\omega_2 L_{ind2}\sin 2\omega_2 t) \end{aligned} \tag{B.20}$$

$$V_{d,\ \omega 1+\omega 2} = -L_{ind2}\frac{di_{d,\ \omega 1+\omega 2}}{dt} = L_{ind2}(\omega_1 + \omega_2)A^2 g_{m2}\sin(\omega_1 + \omega_2)t \tag{B.21}$$

Again, i_d can be expanded to I_d written in a two-variable Taylor-series approximation to the third order as [4]

$$\begin{aligned} I_d &= g_{m1}V_g + g_{m2}V_g{}^2 + g_{m3}V_g{}^3 + g_{d1}V_d + g_{d2}V_d{}^2 + g_{d3}V_d{}^3 \\ &\quad + g_{md11}V_g V_d + g_{md21}V_g{}^2 V_d + g_{md12}V_g V_d{}^2 \end{aligned} \tag{B.22}$$

where the g_d is drain conductance and g_{md} shows cross conductance. Mixing terms are introduced by this expression.

Substituting the V_g and V_d introducing baseband and second harmonic band into an expression (B.22), the coefficient terms about the lower and the upper side of IMD3 drain current components $IM3_L$, $IM3_U$ can be compiled.

$$
\begin{aligned}
IM3_L = {} & \frac{3}{4}g_{d3}L^3 - \frac{3}{4}g_{d3}L\cdot L_{21}{}^2 + \frac{9}{2}g_{d3}L\cdot L_{21}\cdot L_{22} + \frac{15}{2}g_{d3}L\cdot L_{22}{}^2 + \frac{1}{2}g_{md11}L_{21}\cdot S \\
& + \frac{1}{2}g_{md11}L_{22}\cdot S + \frac{1}{4}g_{md21}L\cdot S^2 - \frac{1}{2}g_{md12}L\cdot L_{21}\cdot S_{21} \\
& + \frac{3}{2}g_{md12}L\cdot L_{22}\cdot S_{21} + g_{m2}S\cdot S_{21} - \frac{1}{4}g_{md21}L\cdot S_{21}{}^2 + \frac{3}{2}g_{md12}L\cdot L_{21}\cdot S_{22} \\
& + 5g_{md12}L\cdot L_{22}\cdot S_{22} + g_{m2}S\cdot S_{22} + \frac{3}{2}g_{md21}L\cdot S_{21}\cdot S_{22} + \frac{5}{2}g_{md21}L\cdot S_{22}{}^2 \\
& + i\begin{bmatrix}
g_{d2}L\cdot L_{21} - g_{d2}L\cdot L_{22} - \frac{1}{4}g_{md12}L^2\cdot S + \frac{1}{4}g_{md12}L_{21}{}^2\cdot S \\
+\frac{3}{2}g_{md12}L_{21}\cdot L_{22}\cdot S - \frac{5}{2}g_{md12}L_{22}{}^2\cdot S - \frac{3}{4}g_{m3}S^3 + \frac{1}{2}g_{md11}L\cdot S_{21} \\
+\frac{1}{2}g_{md21}L_{21}\cdot S\cdot S_{21} + \frac{3}{2}g_{md21}L_{22}\cdot S\cdot S_{21} + \frac{3}{4}g_{m3}S\cdot S_{21}{}^2 \\
-\frac{1}{2}g_{md11}L\cdot S_{22} + \frac{3}{2}g_{md21}L_{21}\cdot S\cdot S_{22} - 5g_{md21}L_{22}\cdot S\cdot S_{22} \\
+\frac{9}{2}g_{m3}S\cdot S_{21}\cdot S_{22} - \frac{15}{2}g_{m3}S\cdot S_{22}{}^2
\end{bmatrix}
\end{aligned}
\tag{B.23}
$$

$$
\begin{aligned}
IM3_U = {} & \frac{3}{4}g_{d3}L^3 - \frac{3}{4}g_{d3}L\cdot L_{21}{}^2 - \frac{9}{2}g_{d3}L\cdot L_{21}\cdot L_{22} + \frac{15}{2}g_{d3}L\cdot L_{22}{}^2 - \frac{1}{2}g_{md11}L_{21}\cdot S \\
& + \frac{1}{2}g_{md11}L_{22}\cdot S + \frac{1}{4}g_{md21}L\cdot S^2 - \frac{1}{2}g_{md12}L\cdot L_{21}\cdot S_{21} \\
& - \frac{3}{2}g_{md12}L\cdot L_{22}\cdot S_{21} - g_{m2}S\cdot S_{21} - \frac{1}{4}g_{md21}L\cdot S_{21}{}^2 - \frac{3}{2}g_{md12}L\cdot L_{21}\cdot S_{22} \\
& + 5g_{md12}L\cdot L_{22}\cdot S_{22} + g_{m2}S\cdot S_{22} - \frac{3}{2}g_{md21}L\cdot S_{21}\cdot S_{22} + \frac{5}{2}g_{md21}L\cdot S_{22}{}^2 \\
& + i\begin{bmatrix}
-g_{d2}L\cdot L_{21} - g_{d2}L\cdot L_{22} - \frac{1}{4}g_{md12}L^2\cdot S + \frac{1}{4}g_{md12}L_{21}{}^2\cdot S \\
-\frac{3}{2}g_{md12}L_{21}\cdot L_{22}\cdot S - \frac{5}{2}g_{md12}L_{22}{}^2\cdot S - \frac{3}{4}g_{m3}S^3 - \frac{1}{2}g_{md11}L\cdot S_{21} \\
+\frac{1}{2}g_{md21}L_{21}\cdot S\cdot S_{21} - \frac{3}{2}g_{md21}L_{22}\cdot S\cdot S_{21} + \frac{3}{4}g_{m3}S\cdot S_{21}{}^2 \\
-\frac{1}{2}g_{md11}L\cdot S_{22} - \frac{3}{2}g_{md21}L_{21}\cdot S\cdot S_{22} - 5g_{md21}L_{22}\cdot S\cdot S_{22} \\
-\frac{9}{2}g_{m3}S\cdot S_{21}\cdot S_{22} - \frac{15}{2}g_{m3}S\cdot S_{22}{}^2
\end{bmatrix}
\end{aligned}
\tag{B.24}
$$

Where,

$$
S = -Z_{S,\ \omega 1}(AC_{gs1} + \frac{9}{4}A^3C_{gs3})\omega_1 \approx -Z_{S,\ \omega 2}(AC_{gs1} + \frac{9}{4}A^3C_{gs3})\omega_2 \tag{B.25}
$$

$$S_{21} = -Z_{S,\ \omega 2-\omega 1} A^2 C_{gs2} (\omega_2 - \omega_1) \tag{B.26}$$

$$\begin{aligned} S_{22} &= -Z_{S,\ 2\omega 1} A^2 C_{gs2} \omega_1 \approx -Z_{S,\ 2\omega 2} A^2 C_{gs2} \omega_2 \\ &\approx -\frac{1}{2} Z_{S,\ \omega 1+\omega 2} A^2 C_{gs2} (\omega_1 + \omega_2) \end{aligned} \tag{B.27}$$

$$L = -R_L (A g_{m1} + \frac{9}{4} A^3 g_{m3}) \tag{B.28}$$

$$L_{21} = (\omega_2 - \omega_1) L_{ind1} A^2 g_{m2} \tag{B.29}$$

$$L_{22} = 2\omega_1 L_{ind2} \frac{1}{2} A^2 g_{m2} \approx 2\omega_2 L_{ind2} \frac{1}{2} A^2 g_{m2} \approx \frac{1}{2} (\omega_1 + \omega_2) L_{ind2} A^2 g_{m2} \tag{B.30}$$

These are the coefficients to be related to the source and the load termination impedances of the fundamental frequency, differential frequency, and second harmonic band.

The difference of the lower and the upper side of IMD3 drain current components can be written as

$$\begin{aligned} IM3_L - IM3_U = {} & 9 g_{d3} L \cdot L_{21} \cdot L_{22} + g_{md11} L_{21} \cdot S + 3 g_{md12} L \cdot L_{22} \cdot S_{21} \\ & + 2 g_{m2} S \cdot S_{21} + 3 g_{md12} L \cdot L_{21} \cdot S_{22} + 3 g_{md21} L \cdot S_{21} \cdot S_{22} \\ & + i \begin{pmatrix} 2 g_{d2} L \cdot L_{21} + 3 g_{md12} L_{21} \cdot L_{22} \cdot S + g_{md11} L \cdot S_{21} \\ + 3 g_{md21} L_{22} \cdot S \cdot S_{21} + 3 g_{md21} L_{21} \cdot S \cdot S_{22} + 9 g_{m3} S \cdot S_{21} \cdot S_{22} \end{pmatrix} \end{aligned} \tag{B.31}$$

$$\approx g_{md11} L_{21} \cdot S + 2 g_{m2} S \cdot S_{21} + i(2 g_{d2} L \cdot L_{21} + g_{md11} L \cdot S_{21}) \tag{B.32}$$

In (B.31), all the terms concerning the second harmonic band termination impedances of S_{22} and L_{22} contain the term concerning the differential frequency termination impedances of S_{21} or L_{21}. This means that the second harmonic band frequencies contribute to IMD3 asymmetries through the differential frequency by third-order nonlinear processes. However, the terms concerning the second harmonics band have higher order nonlinearities than seventh-order, and they are very small components. Therefore, neglecting them, only the terms concerning the differential frequency remain as shown in (B.32). Thus, the differential frequency play major role in IMD3 asymmetries. By these analysis formulas, it is shown that IMD3 deteriorates and IMD3 asymmetries occur if the source or the load termination impedances of the differential frequency concerning the terms of S_{21} or L_{21} are finite. In other words, the analysis reveals that the baseband impedances of both the output and the input

circuits must be simultaneously terminated in short-circuit condition to eliminate the IMD asymmetries.

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