



Title	A Study on VLSI Reliability Enhancement by Aging Mitigation and Fault Avoidance
Author(s)	郡浦, 宏明
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## 論文内容の要旨

氏名 ( 郡浦 宏明 )	
論文題名	A Study on VLSI Reliability Enhancement by Aging Mitigation and Fault Avoidance (劣化緩和と故障回避による VLSI 高信頼化に関する研究)
論文内容の要旨	

This thesis discusses VLSI reliability enhancement by aging mitigation and fault avoidance. Larger integration of transistors owing to the advancement of semiconductor manufacturing process has improved performance and functionality of information systems in the last several decades, and people and society have been more and more dependent on information systems provided by VLSI systems. On the other hand, designers have a significant duty to guarantee the high reliability of VLSI over a long period of time. In contrast, scaled transistors have been more sensitive to aging effects, such as negative bias temperature instability (NBTI), and they are becoming more likely to cause faults. In various aging effects, NBTI focused in this thesis causes a delay increase due to threshold voltage degradation of p-channel MOSFETs (PMOSs), and it is one of the most serious concerns of circuit designers. Especially, for implementing mission-critical applications such as space and electricity systems that tolerate aging effects, designers are eager to develop highly reliable VLSI systems that can extend device lifetime. This thesis studies reliability enhancement of VLSIs to overcome aging effects. To accomplish this objective, three processes are focused on; estimation of NBTI-induced delay degradation, NBTI mitigation, and fault avoidance using spare elements in reconfigurable devices.

First, this thesis provides a gate-level estimation method of delay degradation due to NBTI taking each aging process of individual transistors into account. NBTI has a property that its degradation proceeds back and forth through stress phase and recovery phases, and long-term PMOS threshold voltage degradation highly depends on the rate of stress phase (stress probability). Depending on input vectors and circuit structure, some PMOSs would experience long stress and have a significant delay increase, which could cause a timing error. In the past, however, the non-uniformity of stress probabilities was not carefully considered when the long-term delay degradation was evaluated, and uniform stress to all the PMOSs was often assumed. Therefore, this thesis first evaluates the importance of transistor-level stress probability computation. Evaluation results show that transistor-level stress probability calculation is indispensable to avoid optimistic path delay estimation, especially under the situations when a circuit continues the same operation or receives the same inputs for a long time. Furthermore, this thesis proposes a gate-level timing analysis method that annotates a single individual value of threshold voltage degradation to each gate based on a transistor-level stress probability calculation. Evaluation results reveal that the proposed method can achieve almost the same level of delay estimation accuracy compared to transistor-level timing analysis.

Second, this thesis proposes an NBTI mitigation method by inputting random scan-in vectors in standby mode. The aim of this method is to recover internal PMOSs suffering from long-term stress by exploiting a short standby time when a circuit temporally stops the operation. While a conventional method that gives multiple test vectors to primary inputs of a circuit requires preparing and storing large amount of test vectors, the proposed method utilizes commonly embedded scan chains and injects simple random test vectors to save area. Experimental results show that giving random scan-in vectors attains up to 71% reduction of delay degradation. Moreover, this thesis clarifies that 8-bit linear feedback shift register (LFSR), which consumes small area and leakage power, is enough to generate random scan-in vectors for NBTI mitigation.

Third, this thesis shows a quantitative evaluation of fault avoidance methods on reconfigurable devices in the viewpoint of lifetime enhancement. Due to highly scaled and integrated VLSI technology, non-recurring engineering (NRE) cost to develop application specific integrated circuits (ASICs) is elevating. To save NRE cost, reconfigurable VLSIs typified by field programmable gate arrays (FPGAs) are utilized to implement and verify applications. Reconfigurable devices consist of an array of basic elements, and a part of these elements remain unused even when an application is mapped. Conventionally, focusing on these redundant elements, fault-avoidance methods, such as using pre-allocated spare elements according to pre-determined policy and using unused elements dynamically by partial reconfiguration, are proposed. As VLSI manufacturing process advances and aging faults emerge more often in the future, faults elimination would be widely required. At that time, circuit designers have to comprehensively figure out properties of fault-avoidance methods to achieve longer or more stable lifetime enhancement coping with aging faults. Therefore, to indicate characteristics of fault-avoidance methods, this thesis performs fault-avoidance simulations taking consecutive aging faults into account, and evaluates lifetime extension quantitatively focusing on representative five fault-avoidance methods under the same architecture and the same evaluation setup. Evaluation results indicate that methods of row-directional shift and dynamical partial reconfiguration can achieve up to 70% of lifetime enhancement compared with ideal upper limit of that. This thesis also shows that dynamical partial reconfiguration depends on initial placement and routing results, and points out that there is a room to improve the lifetime enhancement efficiency of dynamic partial reconfiguration.

As a conclusion, this thesis provides comprehensive evaluations and proposals on (1) how the performance degradation should be evaluated, (2) how the aging process can be delayed, and (3) how faulty aged elements can be eliminated, which are required for lifetime extension of VLSI devices. These evaluation results strongly contribute to future designs of highly reliable VLSIs.

## 論文審査の結果の要旨及び担当者

氏名(郡浦宏明)	
	(職)
論文審査担当者	主査 教授 尾上孝雄
	副査 教授 今井正治
	副査 教授 佐藤高史(京都大学)
	副査 准教授 橋本昌宜

## 論文審査の結果の要旨

本論文は、劣化緩和と故障回避によるVLSI高信頼化に関する研究の成果をまとめたものであり、以下の主要な結果を得ている。

## 1. トランジスタレベルのストレス確率計算によるNBTI起因の遅延増加予測

PMOSトランジスタの経年劣化現象の1つである負バイアス温度不安定性(NBTI)では、ストレス状態とリカバリ状態を繰り返しながら徐々に回路性能が劣化する。NBTI起因の遅延予測では個々のPMOSがストレス下にある確率(ストレス確率)を見積もる必要があるが、ストレス確率計算に必要な精度は明らかでない。本論文では、回路/ゲート/トランジスタレベルでストレス確率を計算してタイミング解析を行い、NBTI起因のパス遅延増加量を評価している。その結果、楽観的な遅延見積もり回避のためのトランジスタレベルストレス確率計算の必要性を示している。また、トランジスタレベルのストレス確率算出結果を用いてゲートレベルで閾値電圧を設定する手法を提案し、トランジスタレベルのタイミング解析と比べて誤差12.6%で遅延増加量を予測可能であることを示している。

## 2. スタンバイ時間中の乱数スキャン入力によるNBTI起因の遅延増加抑制

NBTIによる劣化進行はストレス確率に依存する。ストレス確率が高いPMOSにリカバリ状態を経験させることで遅延増加の抑制が期待できる。本論文では、乱数スキャン入力を用いた低コストなNBTI起因の遅延増加抑制手法を提案している。提案手法の評価結果より、10%のスタンバイ時間で最大71%の遅延増加抑制効果が得られることを明らかにしている。また、劣化緩和用の乱数生成器を小面積・低消費電力の小規模LFSRで実装できることを示している。

## 3. 故障回避手法に関する寿命延長効果の定量的評価

故障回避と親和性の高いデバイスとして、冗長な基本構成要素の二次元行列から構成される再構成可能デバイスが注目されている。これまで、再構成可能デバイスの再構成機能を利用した故障回避機構が複数提案されている。回路設計者はこれらの手法を選択する際、より長く、または安定した回路寿命を達成可能な手法について事前に把握する必要がある。本論文では、5つの故障回避手法で実現されるデバイス寿命延長効果について、故障回避シミュレーションにより定量的に比較評価している。評価結果より、各故障回避手法について寿命延長効果やスペア回路の使用効率などの特徴を明らかにしている。また、動的部品再構成を用いた故障回避による寿命延長効果が初期マッピングに依存することを示している。

以上のように、劣化緩和と故障回避によるVLSI高信頼化に関する研究は、VLSI微細化・高集積化により顕在化する劣化故障の除去を実現するという点において非常に有用である。本成果は、ユーザに信頼性の問題を意識されることなく長期間継続使用可能な高信頼性デバイスの実現に寄与するものと期待できる。従って、博士(情報科学)の学位論文として価値のあるものと認める。