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論 文 内 容 の 要 旨

氏 名 （ 原田 諒 ）	
論文題名	A Study on Experimental Characterization of Radiation-Induced Soft Errors for Low Voltage VLSI Circuits （低電圧回路における放射線起因ソフトエラーの実験的評価に関する研究）

論文内容の要旨

This thesis discusses radiation- (neutron- and alpha-) induced soft errors which prevent reliability-demanding electron devices from pursuing low voltage and low power operation. Voltage scaling, which is aggressively utilized in subthreshold/near-threshold computing, accompanied with device miniaturization leads to a drastic decrease in the minimum charge to cause soft errors, and could elevate soft error rate (SER) to a level at which even consumer product would suffer from soft errors. To estimate SER of very large scale integration (VLSI) circuits, SER of basic components composing a chip, such as static random access memory (SRAM), flip-flops (FF) and combinational cells, must be characterized. Here, soft errors that occur in these components include a temporal upset in a memory element (single event upset; SEU), a temporal pulse in a combinational cell (single event transient; SET), multiple cell upsets (MCU) in memory elements, and multiple pulses in combinational cells (single event multiple transients; SEMT). To evaluate chip-level SER, each soft error phenomenon must be comprehended, and each soft error rate must be accurately characterized. Meanwhile, silicon on thin buried oxide (SOTB) device, which is one of FD-SOI fully-depleted silicon on insulator (FD-SOI) devices, is being developed for pursuing 0.4 V operation. In putting such a low voltage operation with SOTB to practical use, assuring soft error immunity is one of major tasks, but soft error characterization of SOTB device has not been performed.

For the characterization of soft error components, accelerated irradiation test with fabricated test chips is performed to obtain SER and to do a calibration between hardware measurements and simulation results. The measured SER is the baseline for reliability assurance, and it must be accurately measured in irradiation experiments. To enable accurate chip-level SER estimation, this thesis studies experimental characterization of SET, SEMT, SEU and MCU occurring in SRAM, FFs and combinational cells. To accurately evaluate the impact of SET on digital sequential circuits, measurement circuits to obtain precise SET pulse-width distribution and to observe SEMT are devised and used for SET and SEMT measurement under irradiation. In addition, SEU and MCU of ultra-low voltage SRAM are measured and their voltage dependency is clarified for both bulk and SOTB devices.

This thesis first discusses characterization of SET pulse-width, which determines whether SET causes a bit flip in a memory element or not. To measure the pulse-width with fine time resolution, two novel pulse-to-digital converters and a pulse generator for calibrating die-to-die and within-die process variation are proposed and confirmed to operate as expected. Next, an overall composition of SET measurement circuit including the proposed pulse-to-digital converter is proposed to measure SET pulse-width without undesired pulse-width modulation and process variation effects. The proposed structure on a 65 nm test chip successfully obtained a pulse-width distribution of neutron-induced SET in low voltage operation with fine time resolution and eliminated the impact of process variation on SET pulse-width. Moreover, pulse-width modulation due to negative bias temperature instability (NBTI), which gradually degrades the circuit performance, is discussed with measurement results of a test chip. Evaluation results show that static stress condition of pulse-width measurement circuits could overestimate SER of SET by 20 %.

This thesis next describes SEMT characterization with voltage scaling and body biasing. A circuit structure for measuring SEMT distribution is devised, where it consists of adjacently placed inverter array whose elements are individually connected to counters. From the accelerated neutron test, neutron-induced SEMT is confirmed to increase its ratio to all transients by 40.0 % in 0.7 V operation and reverse body biasing (RBB). Moreover, SEMT simultaneously generates six transients within the same well region. The measurement results point out that SEMT characterization in low voltage operation is indispensable.

This thesis then characterizes the angular dependency of neutron-induced MCU focusing on generation and transport of secondary ions. To evaluate the dependency of MCU on the neutron incident angles in ultra-low voltage operation, accelerated neutron test was performed using a test chip including 10T subthreshold SRAMs. It is observed that the ratio of MCUs at the angles of 60° to that at 0° is 1.13 while 60° incident halves the total amount of incident neutrons. Monte-Carlo simulation considering the generation and transport of secondary ions reproduces the tendency of measurement results, so that the angular dependency of neutron-induced MCU can be explained by the behavior of secondary ions.

This thesis also characterizes the soft error immunity of SOTB device in comparison with bulk device fabricated from the same GDS data. Accelerated alpha tests are performed with SOTB and bulk test chips implementing 6T SRAM. Measurement results of leakage current indicate that SOTB device can widely control leakage current with adaptive body biasing. The number of SEUs on SOTB SRAM is 0.22 times smaller than that on bulk SRAM in 0.4 V operation, so that SOTB is SEU-immune device. On the other hand, the number of SEUs in 0.4 V operation is 5.0 times larger than that at 1.0 V operation.

Integrating these accomplishments, this thesis summarizes which soft error component is dominant in chip-level SER. From the measured and calculated results, SEU mitigation is the first step to improve the circuit reliability, and this tendency is the same at ultra-low and nominal voltages. On the other hand, neutron-induced SET and SEMT increase its portion with higher clock frequency. While still 1/10 to 1/100 of neutron-induced SEU and MCU at over 1 GHz clock frequency, SET and SEMT could become dominant factors when SEU and MCU are mitigated by two and three orders of magnitude at 1 GHz operation, respectively. SET and SEMT mitigation becomes necessary for a chip that cannot satisfy given reliability requirements only with radiation-hardened SRAM and flip-flop.

様式7

論文審査の結果の要旨及び担当者

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論文審査の結果の要旨

本論文は、低電圧回路における放射線起因ソフトエラーの実験的評価に関する研究の成果をまとめたものであり、以下の主要な結果を得ている。

1. パルス幅変動成分を抑制した正確なSETパルス幅の測定

組み合わせ回路のSERを算出するためには放射線起因一過性パルス(SET)のパルス幅分布を解明する必要がある。しかし、既存のパルス幅測定回路は時間分解能などに課題があり、また製造ばらつきや負バイアス温度不安定性（NBTI）がパルス幅を変動させるため、正確なパルス幅分布を取得することは困難である。本論文では、高井時間分解能を持つパルス幅測定回路を新たに提案している。また、製造ばらつきによるパルス幅変動効果を除去可能な機構を提案し、正確な中性子起因SETのパルス幅分布を測定している。また、NBTIによるパルス幅変動効果を測定し、NBTIによるパルス幅変動効果が、SERを20%過大評価することを明らかにしている。

2. 中性子起因SEMTの電源電圧・基板バイアス依存性測定

低電圧化に伴い、組み合わせ回路に複数のパルスを発生させる放射線起因一過性複数パルス(SEMT)の発生が予測されるが、これまで測定事例は報告されていない。本論文では、SEMT測定回路を提案し、中性子起因SEMTの電源電圧や基板バイアスに対する依存性と、SEMTの空間的な分布を測定している。SETに占めるSEMTの割合は電源電圧の低下で最大40%に達し、SEMTが最大6個のインバータに同時にパルスを発生させることを確認している。

3. 中性子起因MCUの角度依存性評価

加速放射線試験では、一般的にチップに対して垂直にビームを照射する。一方で、中性子起因一過性複数反転(MCU)が照射角度によって変化するとの報告もある。本論文では、低電圧動作させたメモリ回路(SRAM)に異なる角度から中性子を照射し、MCUの角度依存性を測定している。チップに対して斜めから照射することで、垂直の場合と比較してMCUが増加することを確認している。一方で、デバイスシミュレーションからも同様の傾向を確認し、中性子の衝突で発生する二次イオンの前方散乱性が、角度依存性を生じていることを解明している。

4. 薄膜BOX-SOI(SOTB)を用いた低電圧SRAMにおけるα線起因SEU測定

低消費電力化を目指し、低電圧動作と高い基板バイアス制御性を持つ薄膜BOX-SOI(SOTB)デバイスが研究されているが、SOTBデバイスのソフトエラー耐性は解明されていない。本論文では、SOTBデバイスを用いた低電圧SRAMにてα線起因一過性反転(SEU)を測定している。結果をバルクデバイスのものと比較し、SOTB SRAMは電源電圧0.4VでもバルクSRAMの1.0V相当のソフトエラー耐性を有することを確認している。

以上の成果より、放射線・ソフトエラー・チップの素子ごとのSERを取得し、電源電圧やクロック周波数に対するチップレベルのSERを正確に算出することができる。これにより、半導体デバイスの性能や要求に応じた信頼性の最適化に貢献するものと期待できる。従って、博士（情報科学）の学位論文として価値のあるものと認める。