A Study on Modeling and Characteristics Validation of On-chip Signal and Power Noise Based on Measurement

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Abstract

This thesis discusses modeling and characteristics validation of on-chip noises based on in-situ measurement results. Our targets of modeling and characteristics validation are crosstalk noises on interconnects and power supply noises. Importance of crosstalk noises has been growing up because of shrinking interconnect width, height, and spacing, relative increase of interconnect delay, and sharper signal transition. Seriousness of power supply noise is rising because of lowering supply voltage, increasing current consumption, and magnifying instantaneous current, that is dI/dt. Modern physical designers of VLSI (Very Large Scale Integration) need effective methods to estimate and mitigate these issues. This thesis aims to establish a modeling method for accurate and/or fast simulation, to clarify noise characteristics, and to validate noise reduction techniques.

In this thesis, an impact of inductive coupling noise in a bus structure is measured. The measurement results verify the equivalent circuit models and characteristics of inductive coupling noise. A test chip is fabricated in an advanced 90nm CMOS (Complementary Metal Oxide Semiconductor) process to clearly observe inductive coupling noise. RLC distributed constant model is built for simulation with a 3D-field solver. The simulated delay variation of interconnect is consistent with the measured delay variation, and adequacy of the constructed simulation model is verified. Measurement results with several TEGs (Test Element Group) reveal the validity of several noise reduction techniques and a long-range coupling effect, and characteristics of inductive coupling noise are observed on silicon. An approximation method of the noise effect by multiple aggressors is also validated with measurement results. Though there are tremendous number of switching patterns in case of multiple aggressors, this approximation method can estimate the noise impact on timing of a switching pattern by summing up delay variation due to each individual aggressor.

Next, impacts of capacitive and inductive coupling noises in future processes are quantitatively predicted based on simulation. The simulation model verified with the measurements in this thesis is used for evaluation. The prediction result indicates that capacitive coupling noise dominates inductive coupling noise according to shrink of interconnect dimension. On the other hand, on an assumption that the interconnect scale is kept constant to maintain the interconnect performance, inductive coupling noise becomes significant in advanced processes. The former prediction result also implies that narrowing and thinning interconnect might be used as a reduction method of inductive coupling noise. The tradeoff of reducing interconnect cross-sectional area between delay and delay variation is evaluated. The evaluation result reveals that inductive coupling effect can be eliminated with small delay overhead

by carefully choosing interconnect cross-section.

This thesis measures power supply noise on silicon from two different aspects. The first measurement focuses on gate delay variation due to power supply noise. The measurement results validate adequacy of developed full-chip simulation model and effectiveness of delay estimation with average voltage drop. The developed variable switch model for full-chip simulation can reduce the computational cost by 94%. The measurement results with ring oscillators well correlate with simulation results with the variable switch model. Similar circuit delays are observed under different waveforms with the same average drop. This measurement result clarifies that circuit delay strongly depends on average voltage drop rather than waveform shape of power supply.

The second measurement focuses on waveform measurement, and an all-digital measurement circuit for dynamic power supply noise waveform is proposed. The measurement results with the proposed circuit are used to evaluate the characteristics of decoupling capacitance on silicon. The proposed circuit consists of standard cells and is suitable for embedding in digital circuits. The dynamic noise waveform is observed with the proposed circuit on a test chip. Voltage resolution and sampling rate of the proposed circuit measured on a test chip were 10-20mV and 2-3G samples per second respectively. The channel length of decoupling capacitance and distance between operating circuit and capacitance are discussed based on measurement results. The long channel length improves area efficiency of capacitance. On the other hand, too long channel length worsens the RC time constant of decoupling capacitance. Low impedance between operating circuit and decoupling capacitance is necessary to immunize power supply noise.

This thesis demonstrates to designers the notable impact of inductive coupling noise in 90nm process on silicon and the trend of capacitive and inductive coupling noises in future processes. The modeling and reduction methods of inductive coupling noise validated in this thesis enable accurate delay estimation in high performance bus design. Accurate and fast estimation of power supply noise effect is brought by the full-chip simulation method and delay dependence on average voltage drop. The proposed gated oscillator can easily monitor the distribution of power supply noise waveform, and enables verification of power supply network. Finally, this thesis enables designers to reduce the delay uncertainty of circuits and interconnects due to interconnect and power supply noise at the physical design stage, and contributes to the reduction of the design margin, improvement of the yield, and design of high performance circuits and interconnects in the state of the art processes.

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Chapter 1

Introduction

This chapter describes the research motivation and contribution of this thesis. This thesis deals with interconnect and power supply noises. Interconnect and power supply noises are emerging as an serious issue in shrunk fabrication process. The focuses of this thesis are modeling of these noises for accurate noise simulation in acceptable simulation time, and its application for prediction and reduction of noises. The following section discusses the noise problems and past works in physical design considering interconnect and power supply noise problems in modern VLSI.

1.1 Problems of technology scaling on VLSI

CMOS fabrication process has been competitively developed for a past few decades, and the advancement is expected to continue [1]. The CMOS process scaling shrink the channel length, transistor width, oxide thickness, and wire width. Supply voltage and threshold voltage of transistors are lowered, and dopant density of substrate increases. These physical improvements bring several merits such as smaller area, faster operation speed, and lower power consumption of a circuit. Advancement of fabrication process has provided these steady improvements for past decades.

However, recent fabrication technology is confronted with many obstacles that deteriorate the merit of process advancement. One of the representative problems is process variation [2–5]. Process variation is caused by several factors. For example, the limit of lithography technology, which prints circuit pattern on silicon wafer, brings variation of channel and wire pattern. Larger process variation means performance uncertainty of a fabricated chip. As a result, hardware vendors must accept decrease of chip yield or large design margin reluctantly. Leakage current of transistor is also a major issue for designers [6–11]. Leakage current flows even while circuits are not operating, and static power consumption due to leakage current has become comparable with dynamic power consumption due to circuit operation. Subthreshold leakage is caused by lowered threshold voltage, and is a main factor of leakage current. Gate leakage arises from extremely thin oxide thickness of transistor in recent process, and is considered to be serious in the future processes.

Performance variation caused by the above problems can be called "static" because performance degradation is decided when chips are fabricated, and is not changed by circuit operation. On the other hand, there are problems that we here call "dynamic" such as interconnect and power supply noises, which cause delay variation of circuit depending on circuit operation. A main factor of an interconnect noise is capacitive and inductive coupling noises [12, 13]. Capacitive coupling noise arises from inter-wire capacitance and inductive coupling noise is ascribed to mutual inductance between interconnects. Power supply noise is caused by current flow on power supply line which has resistance(R) and inductance(L). Supply noise due to resistance and inductance and called IR drop and L·dI/dt drop respectively. These noises are current and prospective design issue in VLSI design. The difficulty of these problems is not only in development of their solutions but also still in simulation and modeling of devices for estimation of the their effects. To estimate the impact of these noises, circuit simulation in a practical or the worst-case operational condition is needed. Reproduction of power supply noise requires simulation of large scale circuits in a whole chip or the same power domain. For this purpose, an adequate model which enables fast and accurate enough simulation is also required.

Accurate and fast estimation of noise effect is very important for industrial VLSI design. Development of modern VLSI product is competitive, and the given development period becomes short. Mask cost for VLSI becomes expensive in proportion to the miniaturization of technology node and the number of mask layers on a chip. Design problems found in test chip fabrication originating from physical design are critical, and physical design which assures correct operation and acceptable yield of fabricated chips is required. On the other hand, specifications on area, circuit delay, and power consumption are also strictly given in present VLSI design, and large noise margin to ensure correct circuit operation is difficult to be allowed. Consequently, accurate noise simulation and device modeling are required to minimize the noise margin while keeping correct circuit operation. Simulation time is also important because VLSI chips fabricated with state-of-the-art process are large scale circuits, and feedback from simulation to design through repetitive simulation is required.

Following sections describe the detail of interconnect and power supply noises, and explains the problems on these noises in physical design of VLSI with recent fabrication processes.

1.1.1 Interconnect noise

Interconnect delay was very small in comparison with the gate delay in 0.5μm and above processes. However, interconnect delay does not follow the decrease of gate delay due to process scaling. We here assume that device dimension is scaled with the ratio $S(0 < S < 1)$ by technology scaling. Cross-sectional area and length of the local interconnect is represented as S^2 and S. Here we model the interconnect as a simple circuit with a lumped interconnect resistance and capacitance shown in Fig. 1.1. Considering an interconnect length and cross-sectional area, interconnect resistance and capacitance(C) are scaled with $1/S$ and S. RC product, which corresponds to interconnect delay, remains 1, which indicates that local interconnect delay is independent of process scaling, and does not increase or decrease.

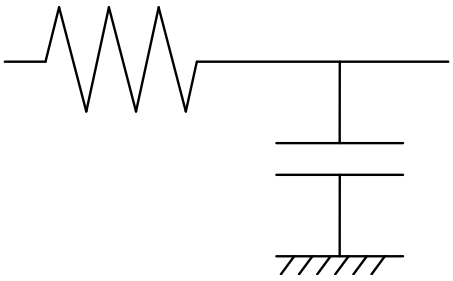

Figure 1.1: RC model of interconnect.

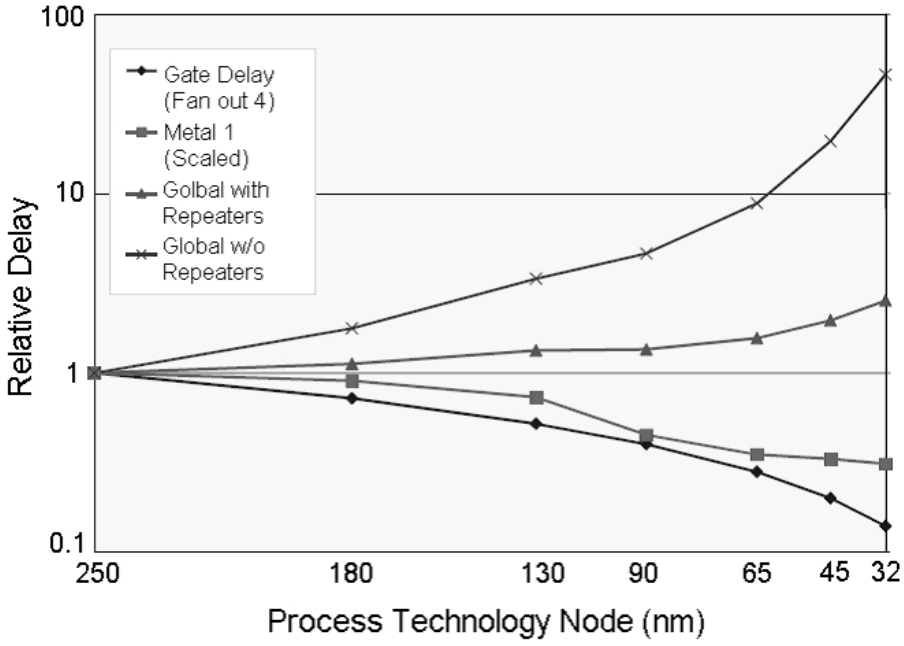

Figure 1.2: Prediction of interconnect delay in ITRS [14].

In recent processes, wire height is scaled slower to suppress the increase of wire resistance and reduce local interconnect delay. In case of global interconnect, interconnect length is not scaled following the process scaling, and remains 1. On the other hand, interconnect cross-sectional area is scaled with $1/S^2$. Global interconnect delay is $1/S^2$ and increases as process advances. In this way, although gate delay decreases according to process scaling, interconnect delay remains unchanged or increases. As a result, impact of interconnect delay on circuit delay will increase.

Development of devices with new materials has been studied for reduction of interconnect delay, that is reduction of interconnect resistance and capacitance. To reduce the resistance, copper interconnect, which has smaller resistivity, is substituted for aluminum interconnect in recent process. Low-k inter-wire insulator which has smaller dielectric constant

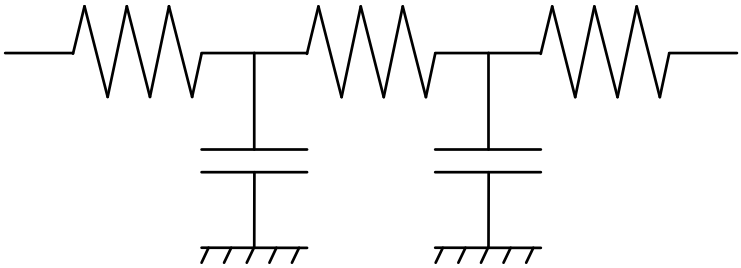

Figure 1.3: RC ladder circuit.

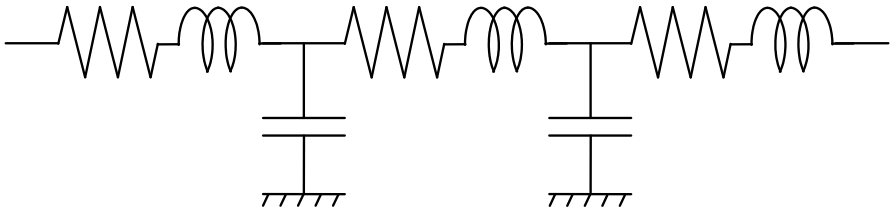

Figure 1.4: RLC ladder circuit.

has been introduced for reduction of interconnect capacitance. However, these solutions have physical limits and face with a difficulty in keeping up with technology advance. Therefore, interconnect delay cannot be reduced sufficiently. Figure 1.2 shows the prediction of interconnect delay by ITRS (International Technology Roadmap for Semiconductors) [14]. Though local interconnect can follow the gate delay, global interconnect delay does not decrease as we discussed.

Interconnect delay must be carefully taken into consideration in circuit design, which means that accurate estimation of interconnect delay becomes important. Most simple estimation of interconnect delay models the interconnect as resistance and capacitance. This estimation can be applied to most interconnects. On the other hand, interconnects whose propagation time is longer than signal rise time must be regarded as transmission lines [12, 13], and interconnect delay is estimated using distributed interconnect models such as RC or RLC ladder circuit shown in Figs. 1.3 and 1.4.

In a practical circuit, especially in global bus lines, delay variation due to interconnect noise is also considered in delay estimation. Main factors of interconnect noise are capacitive and inductive coupling noises. Capacitive coupling noise is caused by inter-wire capacitance, and inductive coupling noise owes to mutual inductance between interconnects. Both coupling noises are caused by signal transitions at neighboring interconnects. A voltage transition of an aggressor line penetrates into a victim line because of electric field, and current flow in the aggressor line causes electromotive force in the victim due to electromagnetic induction to a victim line. Capacitive and inductive coupling noises are considered to

become serious in the future processes. Increase in aspect ratio of interconnects and signal frequency deteriorates capacitive coupling noise, and increase in signal frequency and the unchanged global interconnect structure aggravates inductive coupling noise.

There are many works on accurate and fast capacitance and inductance extraction, interconnect modeling, and circuit simulation considering coupling effects. In a simple structure, capacitance can be computed by solving Poisson equation analytically. However, practical interconnect structures are too complicated to solve the equation analytically, and field solver programs [15, 16] using numerical analysis [12] are often used. Field solvers can achieve the high accuracy, and the extracted values are regarded as the most accurate values as long as the wire structure and boundary conditions are well given to the solver. The disadvantage of field solvers is that long CPU time and large memory are required for extraction, and it is sometimes impractical to extract capacitance from a complicated interconnect structure. The methods commonly adopted for extraction decompose a large complicated structure into many representative primitive structures, and compute capacitance for each primitive structure. The pattern matching is used for the target structure and the capacitance values are approximated using the extracted values of the primitive structure [17–19].

Inductance extraction is more complicated than capacitance extraction, because inductance is defined for a current loop. An interconnect and its current return paths form current loops on the VLSI, and the loop inductance is defined for these current loops. However, current return paths on VLSI are very complicated and the derivation by solving Maxwell equation is impractical. A. Ruehli proposed PEEC(Partial Element Equivalent Circuit) method [20–22] to simulate inductive effect using partial inductance. Partial inductance is defined for each wire segment, not for loop, and easily computed from formulae [23]. Though PEEC method enables us to simulate inductive effect accurately, the circuit matrix tends to be dense and circuit simulation requires large memory and long CPU time. The field solver programs [15, 16] compute the loop inductance with PEEC method. PEEC method enables us to compute the current distribution on signal and power lines on VLSI, and loop inductance of each signal lines is calculated from the current distribution. Loop inductance includes the effect of current return paths, such as complex power grids. Node equation matrix for simulating behavior of interconnects can be reduced with loop inductance because terms of complex current return paths can be omitted.

1.1.2 Power supply noise

Power and ground voltages supplied to operating circuit are not perfectly stable because of voltage variation due to current flow in resistive and inductive power supply lines. This voltage fluctuation is called power supply noise. Power supply noise causes variation of circuit delay in digital circuit and deterioration of performance in analog circuit. IR drop is caused by resistance and L·dI/dt drop arises from inductance of power supply line. Power supply noise is considered to become severer in advanced technologies [24–26]. Though lowered supply voltage in advanced processes brings reduction of power consumption, it makes circuit operation less tolerant to power supply noise. Larger number of gates are implemented in advanced process, and operation frequency becomes high. This causes larger

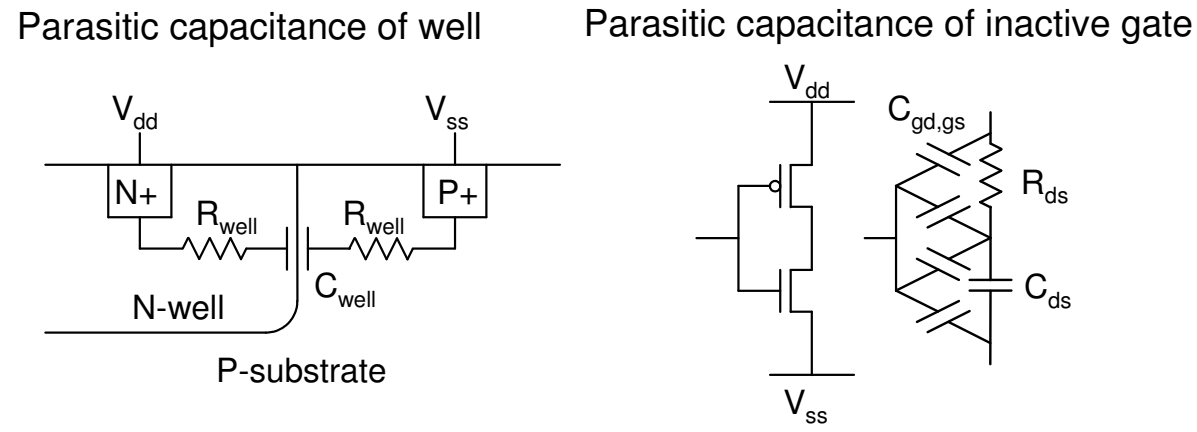

Figure 1.5: Parasitic capacitance in well and an inactive inverter gate. C_{well}, C_{ds}, C_{gs}, and C_{gd} can work as decoupling capacitances.

current consumption, which results in increase of power supply noise. Higher performance transistors increase instantaneous current flow, that is, dI/dt. Consequently, L·dI/dt noise becomes serious.

In physical design, reduction of power supply noise is required. However, it is difficult to eliminate the impact of power supply noise completely, and estimation of circuit performance, that is, delay in digital circuits and circuit behavior in analog circuits, considering power supply noise is also needed. Power supply noise can be reduced with strengthening the power supply lines and inserting decoupling capacitance. Widening power supply lines can mitigate IR-drop, but consumes larger interconnect resource. In other words, reduction of power supply noise with improvement of power grid has a tradeoff between interconnect resource and suppression of noise. Therefore, efficient power grid design, which enables noise suppression with smaller interconnect resource, has been studied [27–29]. Decoupling capacitance works as a temporal current source in an operating circuit, and smoothes current waveform. Reduction of dI/dt due to decoupling capacitance alleviates L·dI/dt noise and peak voltage drop. Parasitic capacitances in a circuit can work as decoupling capacitance. Well junction capacitance and inactive circuit components shown in Fig. 1.5 are representative parasitic capacitance. However, these capacitances are often insufficient, and decoupling capacitance using gate capacitance of MOS transistor is inserted intentionally. [30] discussed the simulation model of gate capacitance for decoupling capacitance, and mentioned the characteristics of gate capacitance based on simulation. On the other hand, gate capacitance consumes area for placement, and the number of capacitance cells which can be placed on a chip is limited. In addition, the effect of capacitance depends on distance between the operating circuit and decoupling capacitance. Thus, effective placement of decoupling capacitance that minimizes the total amount of capacitance is studied [25, 31–33].

To estimate power supply noise, simulation of whole circuits which share the same power

domain is needed, and even full-chip simulation is frequently required. In addition, the worst case noise depends on input vectors, and the number of input vectors can become tremendous for a SoC (System on Chip) and a microprocessor. Simulation of power supply noise requires large computing resource and memory, and simulation time could be impractical. Reduction of simulation costs is studied, such as transistor modeling [25, 34], power grid modeling [35, 36], reduction of input vectors, and vectorless analysis [37].

To analyze the power supply noise, measurement of the noise on a fabricated chip is also necessary because high correlation between simulation and measurement is demanded. A conventional method is probing the power supply network and observing the waveform with an external oscilloscope. However, the parasitic capacitance of a pad and a probe attenuates the supply waveform, and a sharp waveform including high frequency components cannot be measured in this method. [38] presented an on-chip sampling circuit which enables the high sampling rate. Improvements of sampling rate [39, 40], sampling head size [41, 42], and measurement precision [43, 44] are proposed subsequently. Another method is using a ring oscillator. The cycle time of the ring oscillator depends on supply voltage. In other words, the ring oscillator circuit can translate the supply voltage to the cycle count. [45, 46] proposed a circuit using amplifier, switch, and a ring oscillator, and [47] adopted an idea that noise source synchronizes the ring oscillator for measurement. [48, 49] propose a notable circuit which observes dI/dt with inductor. There are also a few works on noise effect on timing [50, 51]. [50] measured noise waveform and noise impact on timing as a clock duty. [51] observed maximum operating frequency of the processor, and verified that reduction effect of power supply noise with on-die decoupling capacitance did not improve operating frequency of tested chips.

1.2 Objectives of this thesis

This thesis focuses on modeling for circuit simulation of noises, on-chip noise measurement, and verification of modeling with measurement. The interconnect and power supply noises are examined in this thesis.

Simulation model is to be developed based on theoretical studies, and is to be validated with experimental results. RLC extraction of interconnects, simulation modeling of inductive effects, and fast simulation methods solving inductance matrix have been proposed as described in Section 1.1.1. As these works are interconnect modeling methods and simulation based theories, verification of the interconnect models with measurement is required to validate these past works. However, measurement of inductive coupling effects in a practical structure is scarcely found because of requirement of high sampling frequency for waveform measurement. Few measurement results of inductive coupling do not measure the practical structure [52], or do not verify the correlation with the simulation model [53]. This thesis measures the inductive coupling effect on a test chip, and validates the simulation model based on measurement results. Our measurement results also confirm the characteristics of inductive coupling effect.

The effect of capacitive and inductive coupling noises increases in future process as men-

tioned in Section 1.1.1 according to qualitative discussion. However, quantitative discussion is required to judge whether capacitive and inductive coupling noises become serious or ignorable. There are quantitative discussions of capacitive coupling noise in future processes. On the other hand, capacitive and inductive coupling noises mutually interfere. The quantitative work of prediction considering both capacitive and inductive coupling noise cannot be found as far as the author knows. The simulation model validated in this thesis is applied for quantitative prediction of coupling noise effect. This prediction result indicated that thinner interconnects do not necessarily increase interconnect delay because delay variation due to inductive coupling noise decreases with thinner resistive interconnects. Therefore this thesis also discusses the tradeoff between interconnect cross-sectional area and interconnect delay considering inductive coupling effect.

As described in Section 1.1.2, many measurement circuits for power supply noise have been proposed, and measurement results of noise waveform are reported. On the other hand, current circuit design requires more effective techniques for stable power distribution and more efficient estimation methods for the impact of power supply noise. Measurement circuits for power supply noise are expected to contribute to verification of simulation methods and alleviation methods for power supply noise. However, studies on such verification are not yet sufficient. In addition, there is a need for further improvement of measurement circuit in terms of performance and usability.

One of hot simulation and certification issues is delay estimation method of large scale integrated circuit under power supply noise. Some of works on measurement of supply noise verified the waveform by comparing simulation results with measurement results. There are few measurement results of noise impact on timing. These works on measurement do not verify simulation method of delay variation due to power supply noise in practical large scale circuit.

Characteristics validation of decoupling capacitance is another issue of concern. Decoupling capacitance insertion is a mitigation method frequently adopted for power supply noise. Though there are several theoretical and/or simulation-based works on simulation model, design parameters, and placement methods of decoupling capacitance as described in Section 1.1.2, the appropriateness of these methods was not verified on fabricated chips. Measurement of supply noise distribution is needed to verify the decoupling capacitance effect, and measurement circuitry suitable for embedding is also one of the challenges. There are past works of the analog sampling and holding circuit [38, 39] for power supply noise as mentioned in Section 1.1.2. Disadvantage of this circuit is routing cost of dedicated stable power and bias lines, which restricts the number and placement of embedded measurement circuit. In addition, complex analog circuit design is needed for implementation of this circuit. Though a ring oscillator based circuit without analog technique [47] was also mentioned in Section 1.1.2, application of this circuit for a practical design is difficult because this circuit assumes that the noise source must synchronize with the clock generated with a ring oscillator for measurement.

This thesis verifies the full-chip simulation method of power supply noise with measurement results of the delay variation due to power supply noise. Our simulation method adopts the linear element model of transistor for full-chip simulation we developed. [54], which

is simulation based work, reported that circuit delay mainly depends on average of power supply voltage, that is, delay variation due to power supply noise can be approximately estimated with average supply voltage without detailed noise waveform. The adequacy of this delay approximation method is validated with measurement results. This thesis also proposes a measurement circuit of dynamic power supply waveform suitable for embedding in cell-based circuits. The proposed circuit is a digital circuit, and does not require any analog power and bias lines and design techniques for analog circuit. The dynamic supply noise waveform is measured with proposed circuit, and the characteristics of decoupling capacitance are verified with measurement results.

The rest of this thesis is organized as follows. Chapter 2 describes measurement of inductive coupling effect. Chapter 3 discusses quantitative prediction of capacitive and inductive coupling noises. Chapter 4 demonstrates the measurement of delay variation due to power supply noise, and verifies full-chip simulation method and delay approximation method. Chapter 5 proposes a measurement circuit for power supply noise and verifies the characteristics of decoupling capacitance. Finally, chapter 6 summarizes and concludes this dissertation.

Chapter 2

Measurement and Analysis of Inductive Coupling Noise in 90nm Global Interconnects

This chapter presents measurement results of the effect of inductive coupling on timing, and demonstrates that inductive coupling noise is a practical design issue in 90nm technology [55–57]. The measured delay change curve is consistent with circuit simulation results for an RLC interconnect model, and clearly different from those for a conventional RC model. A long-range effect, noise reduction caused by ground insertion, and decrease in driver size were clearly observed on silicon. This chapter also examines noise cancellation and superposition effects shown in measurement results and confirms that the summation of delay variation due to each individual aggressor is a reasonable approximation of the total delay variation.

2.1 Introduction

Interconnect noise is becoming an important issue, and capacitive crosstalk noise is a well-known factor in interconnect delay variation. The nano-meter technology regime has raised inductive coupling as a design consideration, and many studies using circuit simulation have been reported [58, 59]. However, simulation models have not been adequately verified, i.e. correlation between simulation and measurement has been reported only in a few papers [52, 53, 60]. Though [52] demonstrated waveform and interconnect delay with TDT/TDR (time domain reflectometry/transmission) and frequency domain measurement, this has limited application because interconnect structures are much different from practical global interconnects. On-chip waveform measurement circuits have been widely studied recently [43, 60–62] with particular focus on power supply noise [43, 61]. Inductive coupling noise is much sharper and includes higher frequency components, and thus it is difficult to use them. [60] implemented on-chip oscilloscope circuits to observe noise waveforms, and observed no inductive coupling effect. [53] observed inductive and capacitive coupling noise

waveforms with sample and hold circuits, however, interconnect modeling for simulation and noise impact on timing were not discussed. [62] observed a waveform that overshot due to self inductance, but did not measure coupling noise. Measurement circuits require a dedicated analog circuit design and a large chip area. None of the previous papers clearly measured the effect of inductive coupling noise on timing in practical operating conditions, though capacitive coupling noise was reported (e.g. [63]).

The contributions of this work with 90nm technology are: 1) measurement of a significant amount of delay variation due to inductive coupling noise in a practical bus structure, 2) verification of an interconnect model for circuit simulation, 3) observation of a long-range effect of inductive coupling, 4) assessment of noise suppression techniques such as increasing ground wires and narrowing the width of signal wires, on silicon, and 5) confirmation of the superposition effect of inductive coupling noise. In our primary work [64], inductive coupling were not able to be observed clearly because capacitive coupling noise dominates inductive coupling noise and the performance and functionality of the measurement circuit are not adequate. For this study, phase interpolators and a bypass circuit were added to the measurement circuitry to make more detailed measurement possible, and wire structures were carefully chosen so that inductive coupling would dominate capacitive coupling.

The remainder of this chapter is organized as follows. Section 2.2 explains features of the inductive coupling effect. Section 2.3 describes measurement circuitry and the interconnect structure. Section 2.4 presents measurement results and discussion. Finally, section 2.5 concludes the chapter.

2.2 Characteristics of inductive coupling noise

This section briefly describes characteristics unique to inductive coupling: dependency on design parameters, long-range effect and waveform shape. The superposition effect of inductive coupling noise is also discussed.

The inductive coupling effect is intensified/alleviated by power lines, driver sizing, and interconnect width. Figure 2.1 shows the dependence of inductive coupling on power lines. Inductive coupling between two signal lines strongly relies on the overlap of current loops. When power lines are wide and close enough, the current loops become small and the inductive coupling to other signal lines becomes weak.

With small drivers, the inductive coupling effect is smaller, because small drivers inject less current. In [52], the ratio of driver output impedance to characteristic impedance of the interconnect is one of the metrics that indicate whether inductive coupling should be considered or not. Narrower interconnects have larger characteristic impedance, and so they reduce current injected by the driver, which results in smaller inductive coupling noise. In addition, a narrow interconnect with high resistivity attenuates coupling noise.

Figure 2.2 depicts the long-range effect of inductive coupling. Capacitive coupling, which is caused by an electric field, is remarkably reduced by distance and signal shield line insertion. Inductive coupling originating from a magnetic field, by contrast, is slowly alleviated by distance and signal line insertion. The graph on the right side of Fig. 2.2 is

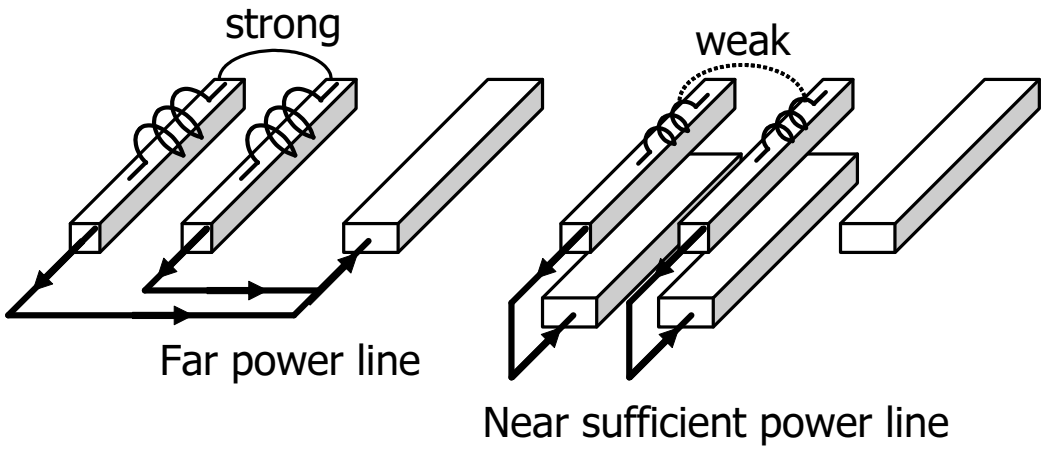

Figure 2.1: Dependence of inductive coupling on power lines.

an example of the coupling coefficient between interconnect 0 and interconnects 1 through 4 in the bus structure shown in Fig. 2.2. Interconnect length, width, thickness, and spacing are set to 1400μm, 4μm, 0.9μm, and 4μm respectively, and the width of the ground wire is 10μm. The interconnects 1 through 4 and the ground interconnects are placed symmetrically on both sides of wire 0. Vertical interconnects are placed in the upper and lower layers in 100% track utilization. Both capacitive and inductive coupling noise waveform can be clearly observed with this structure in simulation. The coupling coefficients are normalized by the coefficient of interconnect 1. The decrease in the inductive coupling coefficient with distance is slower than that of the capacitive coupling coefficient, and the long-range effect of inductive coupling is remarkable. The inductive coupling effect can thus be increased by superposition of noise waveforms from many aggressors.

Figure 2.3 shows an example of a noise waveform considering capacitive and inductive coupling. The interconnect structure is the same as in Fig. 2.2. The size of the interconnect drivers is set to 32X, which corresponds to 120Ω output resistance. A sharp spike mainly caused by inductive coupling first appears in Fig. 2.3, followed by a gentle bump caused by capacitive coupling. The inductive effect is observed in a much shorter time than the capacitive effect, so inductive coupling causes delay variations in the short term range. The sharpness of the spike makes it difficult to measure inductive coupling noise.

Because of the long-range effect, the inductive coupling noises from many aggressors accumulates on a victim and larger noise is observed. Figure 2.4 shows an example of overlapped noise waveforms. The interconnect structure in Fig. 2.2 is used for simulation. Interconnects are driven by 32X(120Ω) inverters and terminate in 4X inverters. The peak noise voltage increases as the number of active aggressors increases. In a linear circuit, the peak noise voltage of an overlapped noise waveform can be computed by summing up each individual noise peak. This superposition holds reasonably well even in a non-linear circuit as long as the noise magnitude is not very large [65, 66].

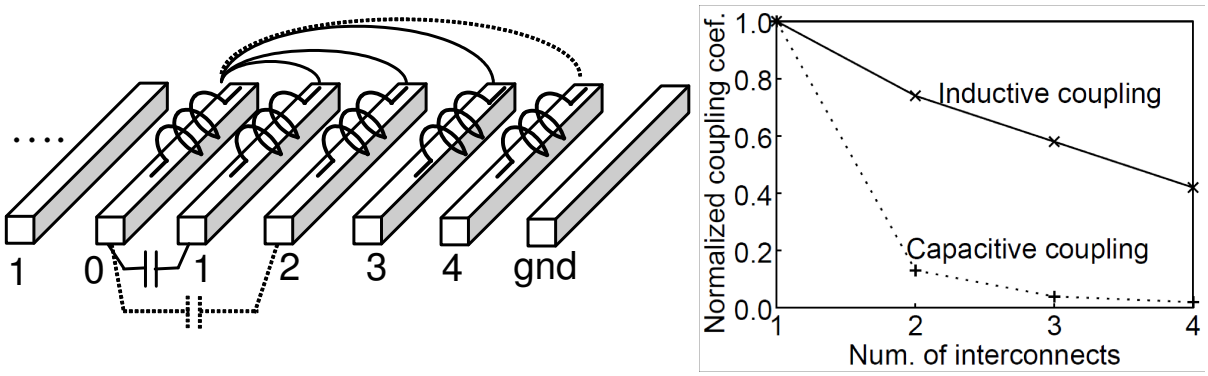

Figure 2.2: Long-range effect of inductive coupling.

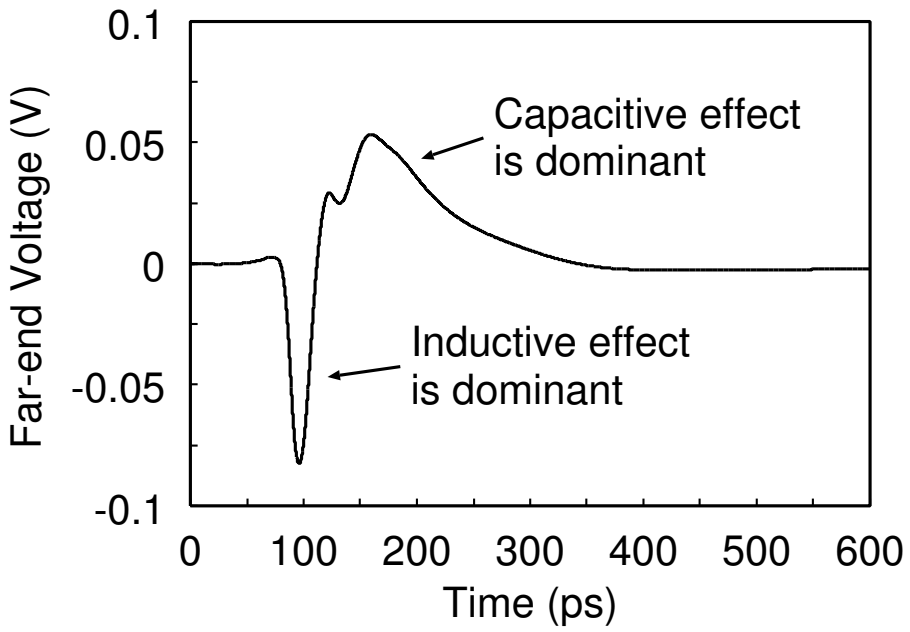

Figure 2.3: A coupling noise waveform.

As with the peak noise voltage, it is expected that the total delay variation due to noise could be estimated by summing up the delay variation caused by each aggressor. This estimate was confirmed experimentally by simulating the circuit on the left of Fig. 2.5. The rise signal waveform with noise is input to the first inverter, and the propagation delay from 10% of the first inverter input to 90% of the second inverter output is observed. The input waveform is depicted on the right side of Fig. 2.5. Three rise input waveforms with different noise injection timings was used. Figure 2.6 shows relations between the peak noise voltage

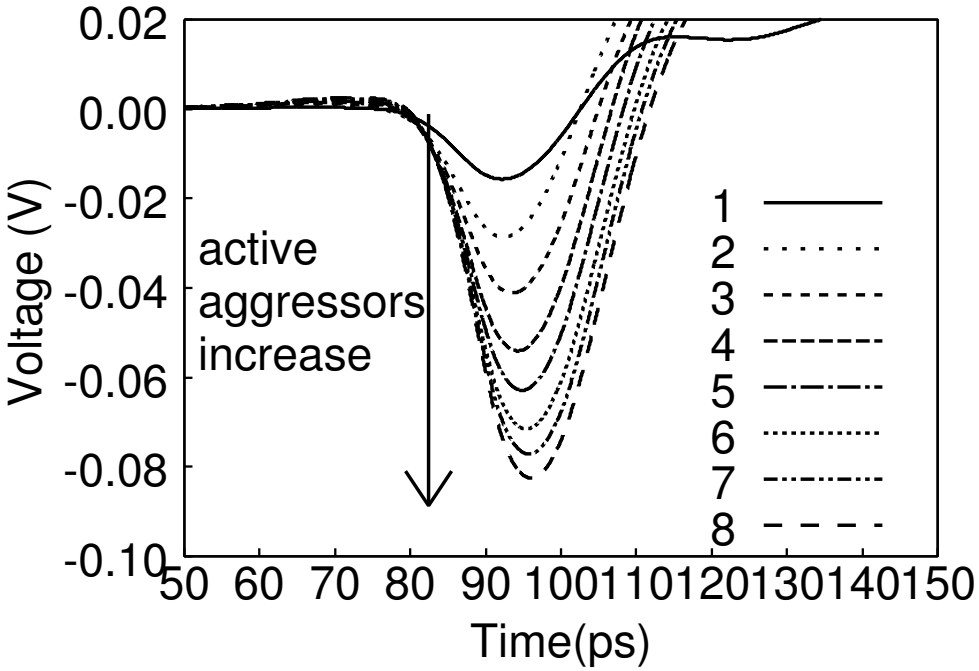

Figure 2.4: Overlapped noise waveform simulated with resistive drivers. Number of key is number of active aggressors. Each aggressor makes rise transition at same timing.

and the propagation delay for each input waveform. These results indicate that the propagation delay increases approximately in proportion to the peak noise voltage. Intuitively, this chapter attributes this to the fact that, in nano-scale devices, the NMOS saturation current is mostly proportional to V_{gs}, i.e. the gate input voltage. Gate delay is the time required to discharge, and the noise reduces its discharging current. Thus the noise area, in other words the integral of noise voltage with respect to time, corresponds to increase in delay. In the current setup, the noise area is proportional to the noise peak voltage, and thus the increase in delay is roughly proportional to the noise peak voltage.

Figure 2.7 shows the actual delay variation due to multiple aggressors and the summation of delay variation caused by each aggressor. The simulation setup is the same as that in Fig. 2.4. The delay variation depends on aggressor and victim transition timing. The maximum delay variation was evaluated. The summation of the delay variation by each aggressor is well correlated with the actual maximum delay variation. A difference above five aggressors is thought to come from nonlinearity of MOS transistors.

The noise superposition can cause the cancellation of noise as well as intensification of noise. When an aggressor makes a rise transition and another aggressor makes a fall transition, the noises from the two aggressors may be cancel each other. Figure 2.8 shows simulation results of the noise cancellation effect. Four aggressors make rise transitions and the other zero to four aggressors make fall transitions. The simulation setup is the same as that in Fig. 2.7. The increase in delay caused by the four rise aggressors is cancelled by the

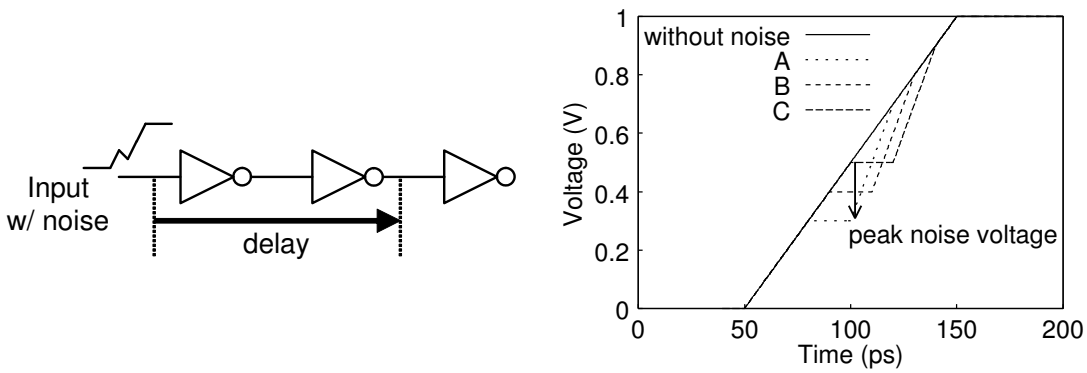

Figure 2.5: Simulation setup of Fig. 2.6. Figure on left is circuit for simulation. All inverters are same size. Graph on right is inverter input voltage waveforms of other three graphs.

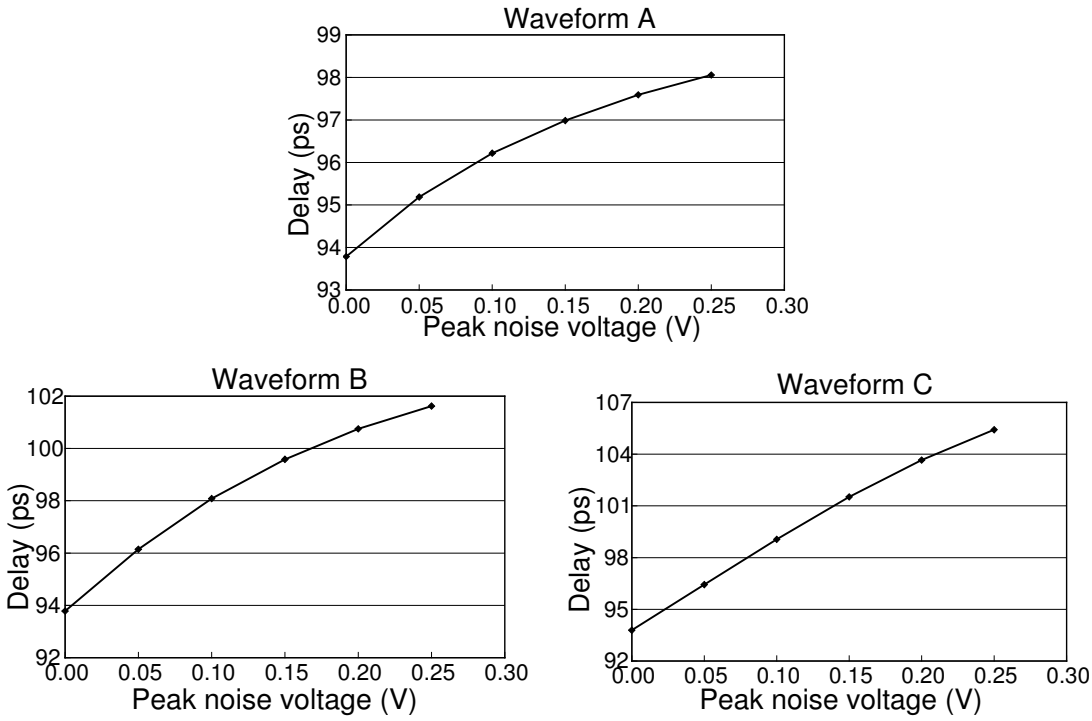

Figure 2.6: Noise peak voltage of inverter input and propagation delay in simulation. X-axis is the peak noise voltage.

fall aggressors, and noise cancellation occurs.

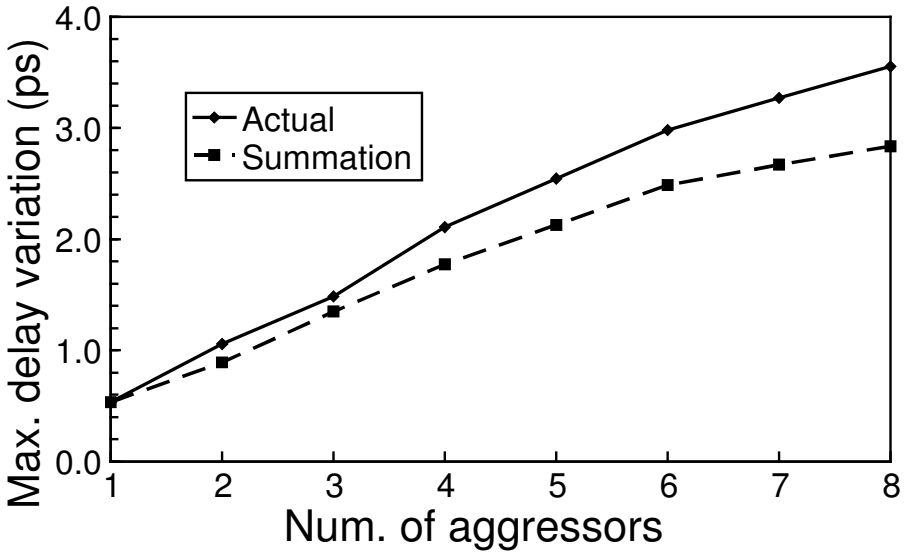

Figure 2.7: Interconnect delay variation due to inductive coupling noise was simulated with MOS drivers. Delay variation of overlapped noise, and summation of delay variation due to each individual noise were compared.

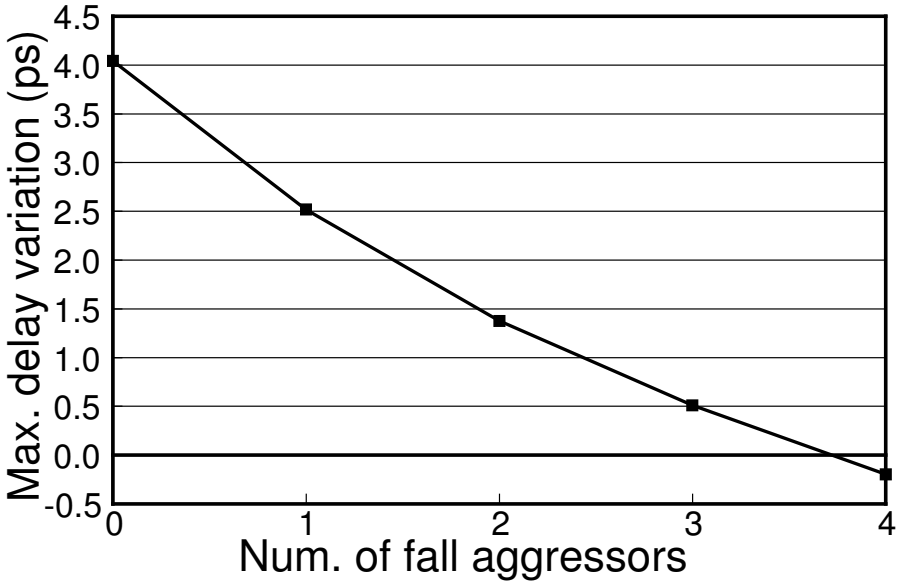

Figure 2.8: Simulated noise cancellation effect.

2.3 Measurement circuit structure

2.3.1 Measurement circuitry

Figure 2.9 shows the circuit designed to measure interconnect delay variation due to inductive coupling noise. The measurement circuit consists of a victim and eight aggressors in a

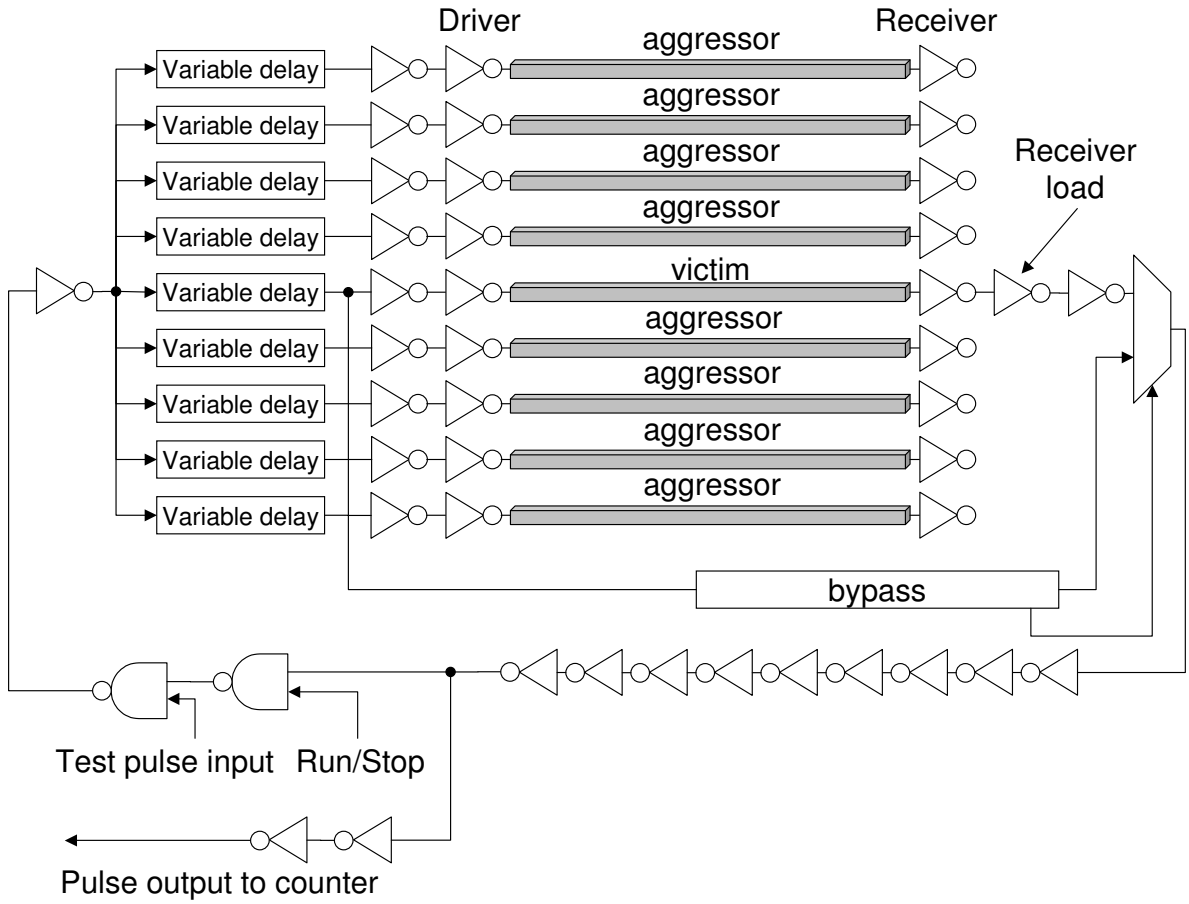

Figure 2.9: Measurement circuit structure.

bus-structure, a ring oscillator, a bypass circuit, a counter, and variable delay circuits.

Delay variation of the victim due to coupling noise is measured by the counter as cycle time variation of the ring oscillator. The victim is embedded in the ring oscillator, and rise and fall signals are input to the victim alternately. The observed ring oscillator cycle includes the average of rise and fall signal delays. By using the bypass circuit (Fig. 2.10), delay variations for rise and fall transition at the victim are measured separately. The bypass circuit generates a bypass delay that is not affected by crosstalk noise. The path selector chooses the main path delay or the bypass delay according to rise/fall transition, and then the only rise or fall delay is captured into the counter and the other is discarded.

Relative transition timing between the victim and aggressors is changed with the variable delay circuits. A variable delay circuit consists of a phase interpolator (Fig. 2.11) [67] and cascaded inverters with a selector. The cascaded inverters insert the delay of up to 15 inverters (about 200 ps), which is a sufficiently wide timing range for the measurement. The delay variation appears in a short timing range because of a sharp spike waveform of inductive

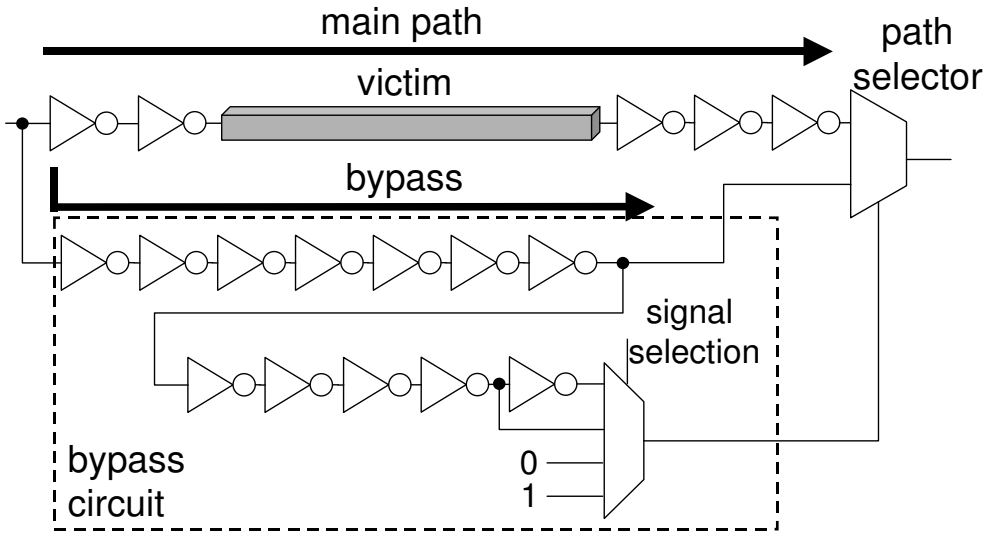

Figure 2.10: Bypass circuit.

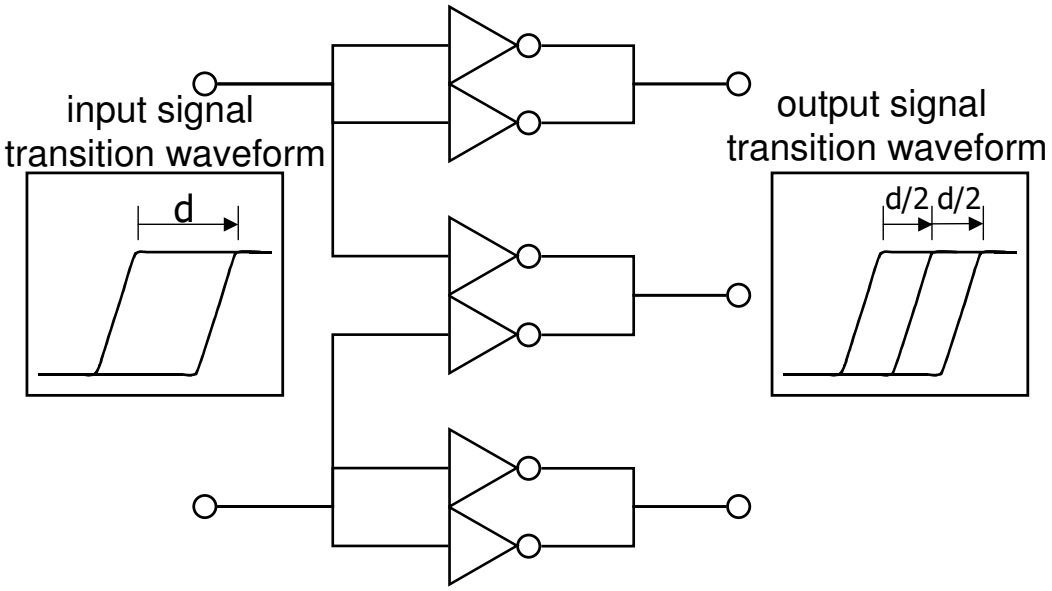

Figure 2.11: Phase interpolator.

coupling noise, and transition timing must be controlled by a small time step. To generate finer aggressor timing than a two-stage inverter delay ($2t_{inv}$), a two-stage phase interpolator that divides $2t_{inv}$ by four was introduced. The aggressor timing can thus be controlled by $t_{inv}/2$.

In our implementation, the control and counter signals are stored in scan-chained flip-

flops. This makes it easy for a pattern generator and a logic analyzer to measure them because all signals are digital and the IO speed of a few MHz is fast enough.

2.3.2 Interconnect structure and TEG variations

Figure 2.12 shows the interconnect cross-section of the bus structure, and summarizes basic parameters. This work based the length and width of our interconnects on those of actual global interconnects with repeater insertion in current use. To clearly observe delay variation due to inductive coupling noise, the parameters were determined such that inductive coupling dominates capacitive coupling. A large enough driver which can increase inductive coupling noise was adopted. To reduce side-wall coupling capacitance, non-thick metal layer (M5) is used for bus lines. An interconnect spacing is set to 4μm which is wide enough to reduce capacitive coupling. Fig. 2.13 shows the relation between coupling coefficients and interconnect spacing. Wide spacing decreases both capacitive and inductive coupling coefficients. However, capacitive coupling is more sensitive to spacing than inductive coupling, and wide spacing relatively increases inductive coupling effect. A large enough width is selected to observe the inductive coupling noise based on circuit simulation with frequency dependent distributed constant interconnect model. The number of aggressors is set to 8 because in this case, inductive coupling coefficient of the farthest aggressor extracted with a 3D field solver is about 1/10 of that of the nearest aggressors. The coupling effect caused by further increment of aggressors is small.

The following summarizes the variations in TEGs (Test Element Group).

TEG_STD
: The basic structure TEG with parameters is shown in Fig. 2.12.

TEG_M2POWERLINE
: Parallel power lines with width=2μm and pitch=5μm are located in the M2 layer.

TEG_NARROWWIRE
: Interconnect width is narrowed to 0.14μm.

TEG_SMALLDRIVE
: Driver size is decreased to 8X.

TEG_LARGELOAD
: Receiver load is increased to 32X.

TEG_NODECAP
: Decoupling capacitances nearby drivers are removed.

TEG_STD is designed to measure clearly the delay variation due to inductive coupling. TEG_M2POWERLINE, TEG_NARROWWIRE, and TEG_SMALLDRIVE are intended to measure the alleviation of the inductive coupling effect. TEG_LARGELOAD is intended to evaluate how the receiver loading affects delay change curve. TEG_NODECAP is intended

Interconnect length	1310 μm
Interconnect width	1 μm
Interconnect pitch	5 μm
Driver size	32X (≒120Ω)
Receiver	4X
Receiver load	1X

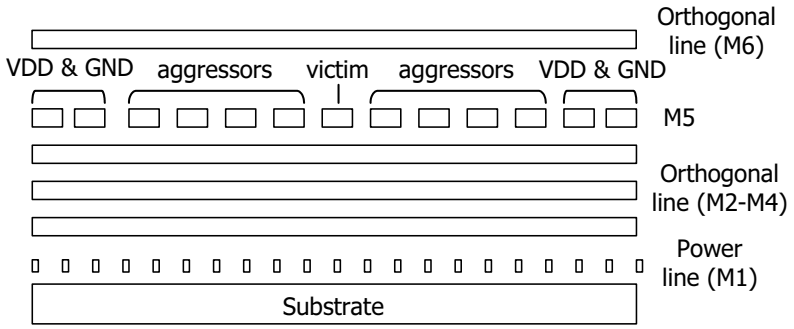

Figure 2.12: Interconnect cross section.

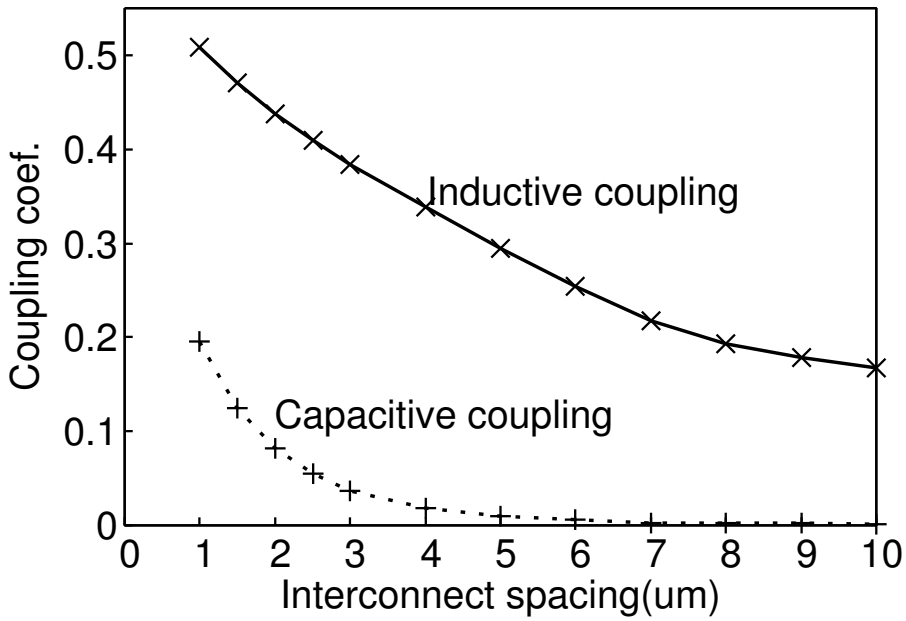

Figure 2.13: Interconnect spacing and coupling coefficient. Inductive and capacitive coupling coefficients are normalized with coefficients at 1μm spacing respectively.

to determine whether existence of decoupling capacitance very close to drivers affects inductive coupling noise.

The chip shown in Fig. 2.14 was fabricated in a 90nm CMOS process with six copper metal layers. Supply voltage of this process is 1.0V.

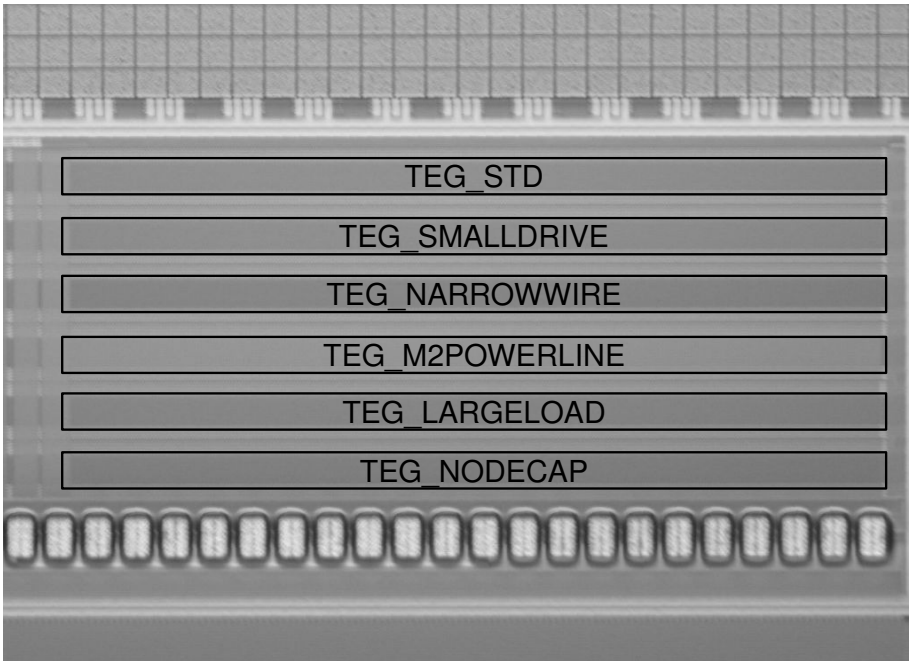

Figure 2.14: Micrograph of fabricated chip.

2.4 Measurement results

2.4.1 Measurement and simulation setup

Delay variation is computed based on the measured ring oscillator cycle. An average of five measurements is adopted for cycle time. The delay variation shown in this chapter represents the averaged results for three chips. The standard deviation of 200 measurement results is 0.355ps, which demonstrates that our measurements have good reproducibility enabling accuracy of several ps of delay variation. The cycle time variation was also measured varying the delay of variable delay circuit in victim without aggressor operation. The relative transition timing of aggressors and victim are computed on the assumption that the delays of variable delay circuits in aggressors are identical to that in victim.

Measurement results were compared with circuit simulation results using three interconnect models: 1) the RLC-distributed constant model with frequency dependency(R(f)L(f)C model), 2) the RLC-distributed constant model without frequency dependency(RLC model), and 3) the RC-distributed ladder model (RC model).

Resistance R, capacitance C, and inductance L of interconnects were extracted by a 3D field solver. Raphael [16] was selected as a 3D field solver, and R and L are extracted with Raphael RI3 program, and C is extracted with Raphael RC3 program. The interconnect structures for RL and C extraction are shown in Figs. 2.15-(a) and 2.15-(b) respectively. Power lines parallel to aggressors and victim at M5 and M1 layers are considered as a current return paths, and M2 lines are also considered in TEG_M2POWERLINE. In capacitance

extraction of TEG_M2POWERLINE, M2 lines are placed parallel to M5 lines. To reduce the extraction time, unnecessary interconnects are removed in RL and C extraction structures. Lines orthogonal to victim and aggressors are ignored in RL extraction because they does not affect the extracted inductance. Substrate is not also considered in RL extraction, because wires in the first layer run in parallel to bus wires, and magnetic field is shielded. M1 lines are omitted in capacitance extraction because they are near to substrate and the impact on the extraction results is small.

For R(f)L(f)C model and RLC model, W-element interconnect model [68, 69] which can model the frequency dependency of the interconnect was adopted. Resistance and inductance are frequency dependent parameters [70], and frequency dependency of R and L is modeled with W-element in R(f)L(f)C model. As for frequency independent parameters, such as R, L and C in RLC model and C in R(f)L(f)C model, interconnects are assumed to have the constant values in all frequency range. R and L values are frequency dependent fundamentally, and R and L values at 17 GHz (significant frequency component of the driver-inputs [12]) were used in the circuit simulations with RLC model. RC model is constructed with a simple ladder model, and the number of ladders is set to 10.

The power supply network is also taken on chip into account, and delay variation of ring oscillator and interconnect due to power supply noise is simulated. The measured package and bonding wire inductance were attached, and the on-chip power/ground wires were carefully modeled as resistance based on the layout pattern.

2.4.2 Verification of inductive coupling effect

Figure 2.16 shows delay variation when all aggressors and victim make a rise transition. The delay variation is the amount of delay increase or decrease from the delay excluding aggressor operation. Relative transition timing between victim and aggressors is changed where all aggressors change simultaneously. In this case, delay variation due to inductive coupling is expected to be observed as a delay increase. Capacitive coupling cause delay decrease in this switching pattern, and the inductive coupling effect can be easily separated from capacitive coupling effect. There is a remarkable difference between RC and RLC/R(f)L(f)C models in the range from 20 to 60ps aggressor timing, which arises from the consideration of inductive coupling. The curve of the measurement result follows the simulation result with the both RLC and R(f)L(f)C model. This result reveals that inductive coupling considerably affects interconnect delay in 90nm technology. Inductive coupling effect in high performance interconnects increases in more advanced processes as will be discussed in Chapter 3, and it will be a serious problem in the future. This result also indicates that the RLC and R(f)L(f)C distributed constant model are effective for noise-aware timing analysis. From now, only simulation results of the RLC model are demonstrated since there is not a significant difference between the RLC and R(f)L(f)C models. Delay variations in the ranges of below 0 ps and over 60 ps aggressor timing are found in both measurement and RLC simulation results. The effect of crosstalk noise does not affect this range, and this delay variation is due to power supply noise by aggressors. Figure 2.17 indicates that increase in delay at aggressor timing = 180 ps, where the aggressor and victim transitions are not overlapped, is

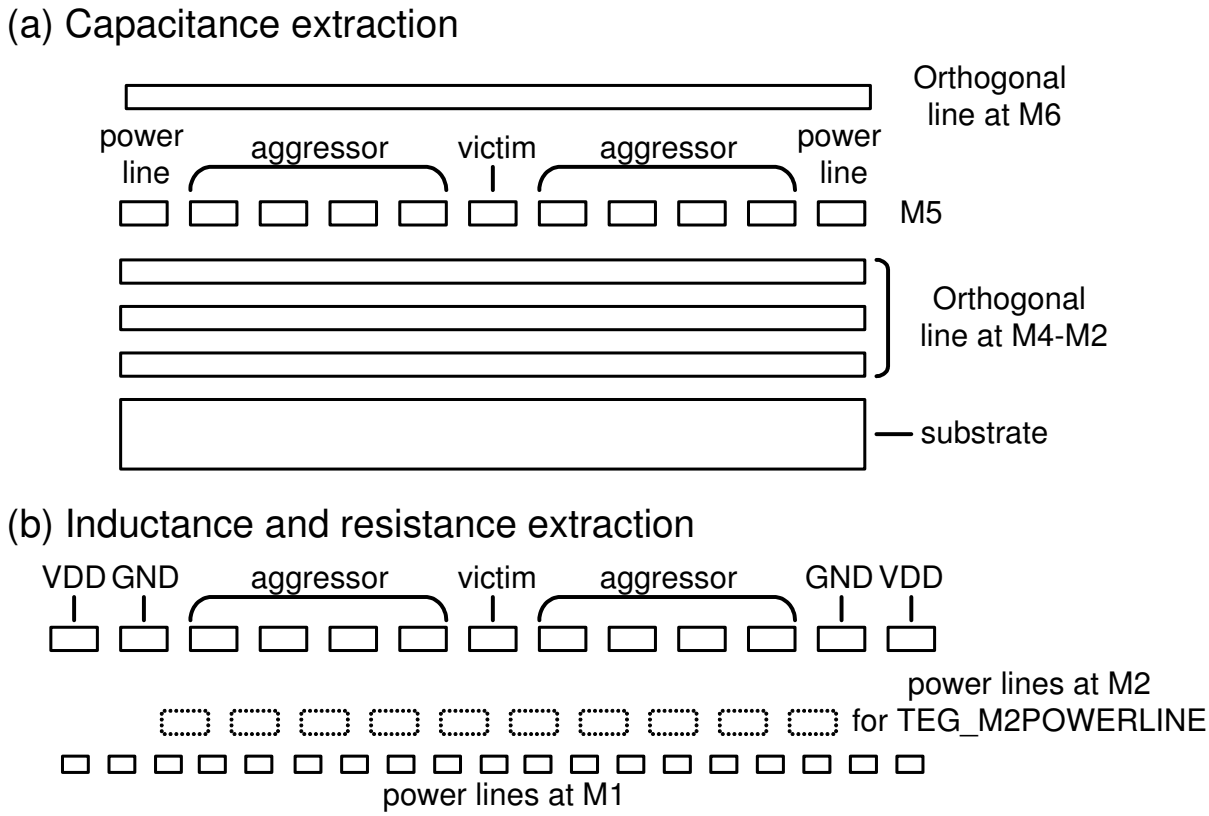

Figure 2.15: Interconnect structure for RLC extraction.

proportional to the number of active aggressors and indicates that delay is slightly increased by power supply noise. The absolute error between simulation and measurement results is sufficiently small. We see 1.5ps delay increase in measurement and 2.8ps delay increase in simulation at aggressor timing = 180 ps. More accurate simulation is difficult since accurate power grid and model with implicit parasitic elements in addition to MOS and wire models is necessary, but it is hardly obtained with available information given from the foundry.

Next, the transition direction between the aggressors and the victim was changed, and measured the delay change curve. Figure 2.18 includes two curves; victim rise and aggressor fall, and victim fall and aggressor rise. As the transition timings approach each other, the delay variation decreases, which is different from Fig. 2.16. This decrease in delay demonstrates that delay variation is caused by inductive coupling, because capacitive coupling and power supply noise should increase delay in this setup. The bypass circuit in Fig. 2.10 enabled us to measure two delay change curves for rise and fall transitions separately. The rise and fall input delays of the variable delay circuit are different. The difference between rise and fall delays causes mismatching of relative timing between aggressors and victim in the ring oscillator measurement where rise and fall signals are input alternately. To solve this problem, separate measurement of rise and fall delays is needed.

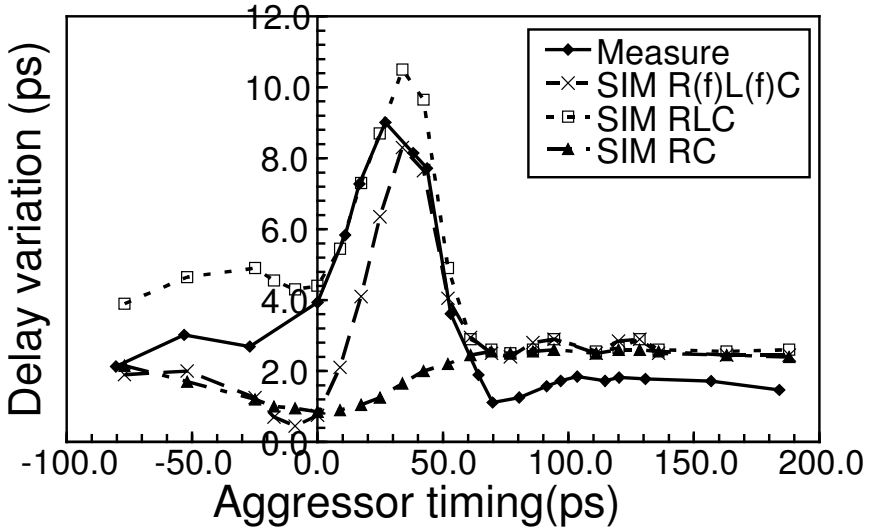

Figure 2.16: Delay change due to coupling noise on TEG_STD.

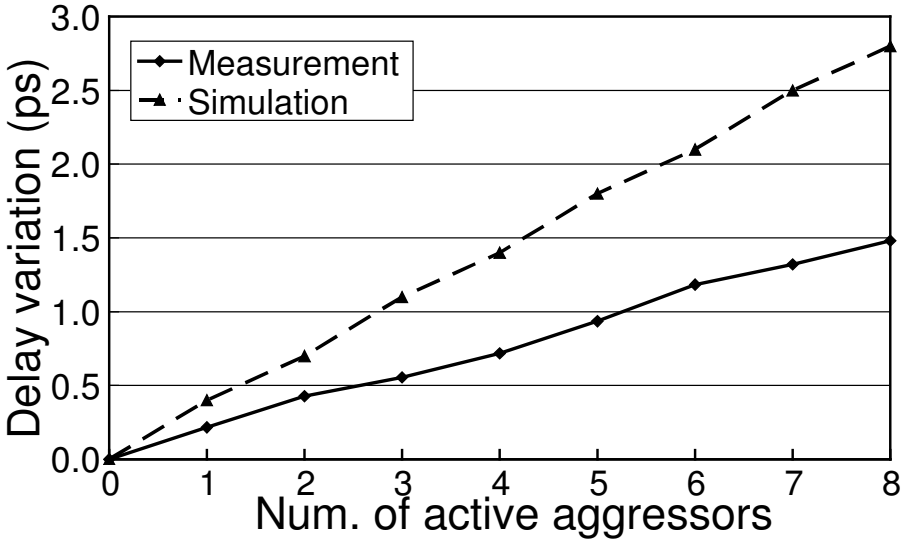

Figure 2.17: Measurement results for delay change on TEG_STD at aggressor timing = 180ps.

2.4.3 Evaluation of inductive coupling characteristics

Figure 2.19 demonstrates the long-range effect of inductive coupling. This figure is the measurement results of the delay variation caused by four active aggressors varying active aggressor positions. As the active aggressors become distant, the delay variation decreases,

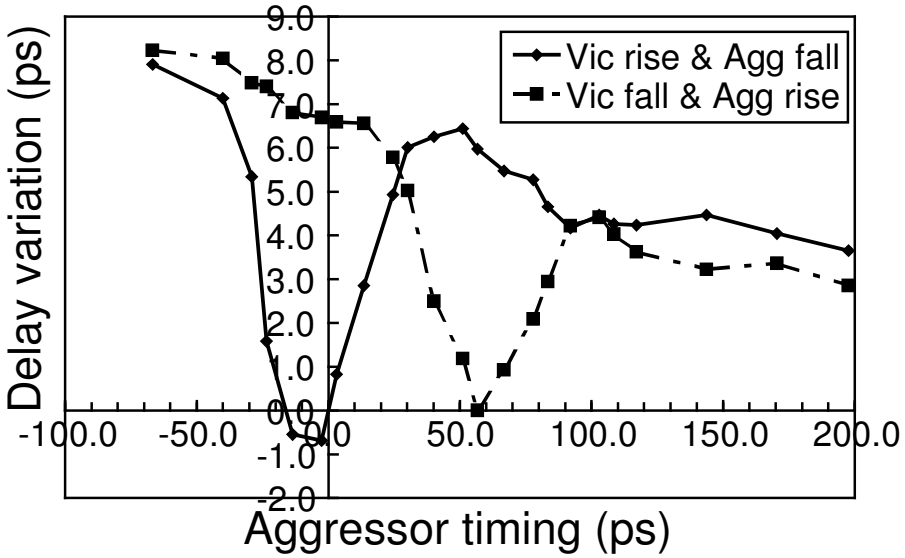

Figure 2.18: Measurement results for delay change on TEG_STD.
Transition directions of aggressors are opposite to those of the victim.

but it decreases slowly. Even when there are two quiet wires between the active aggressors and the victim, the delay variation is only reduced by half, because inductive coupling is not easily shielded by signal lines and is slowly weakened by distance.

Figures 2.20-2.24 demonstrate the degree to which noise suppression techniques and design parameters influence delay variation comparing with TEG_STD.

(a) Adding parallel ground wires in the lower layer (TEG_M2POWERLINE) reduces delay variation by 3ps, because inductive coupling becomes weaker.

(b) Narrowing signal interconnects (TEG_NARROWWIRE) decreases delay variation by 4ps, because higher resistance of narrower wires damps inductive effects.

(c) Reducing driver sizes (TEG_SMALLDRIVE) decreases delay variation, because a driver with high output impedance injects less voltage and current into interconnects.

(d) Enlarging receiver loading (TEG_LARGELOAD) increases susceptive timing range, because a slower receiver transition widens the range of timing that can be affected by inductive noise.

(e) Reducing adjacent decoupling capacitance (TEG_NODECAP) scarcely affect measurement results.

The above measurements (a)-(d) agree with the qualitative discussion and circuit simulation, which shows that noise suppression techniques developed based on simulation will be effective. For a practical use of these techniques, tradeoff between reduction of delay variation and increase of delay or routing cost should be carefully examined.

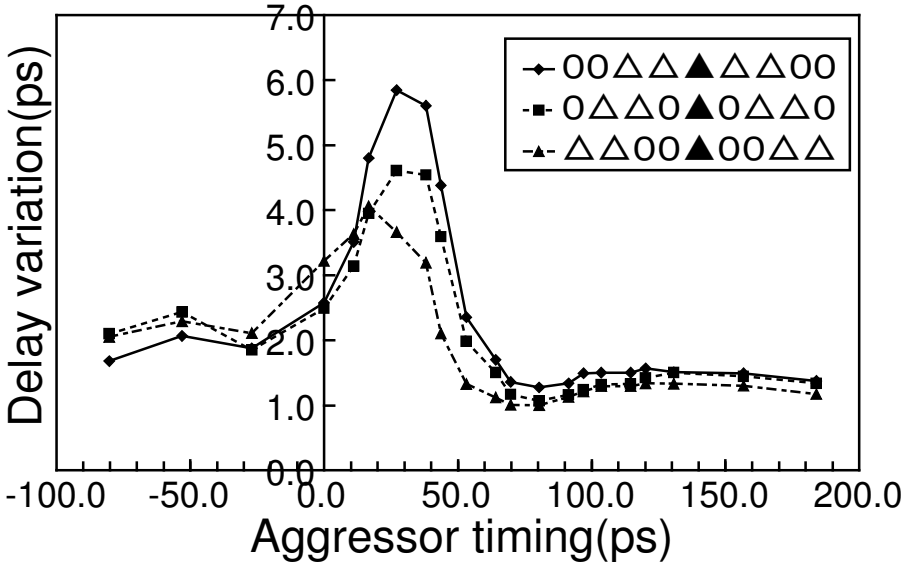

Figure 2.19: Measurement result for delay change when four near/far aggressors are active. ”0” is an inactive aggressor, and ”△” is an active aggressor. ”▲” at the center corresponds to the victim.

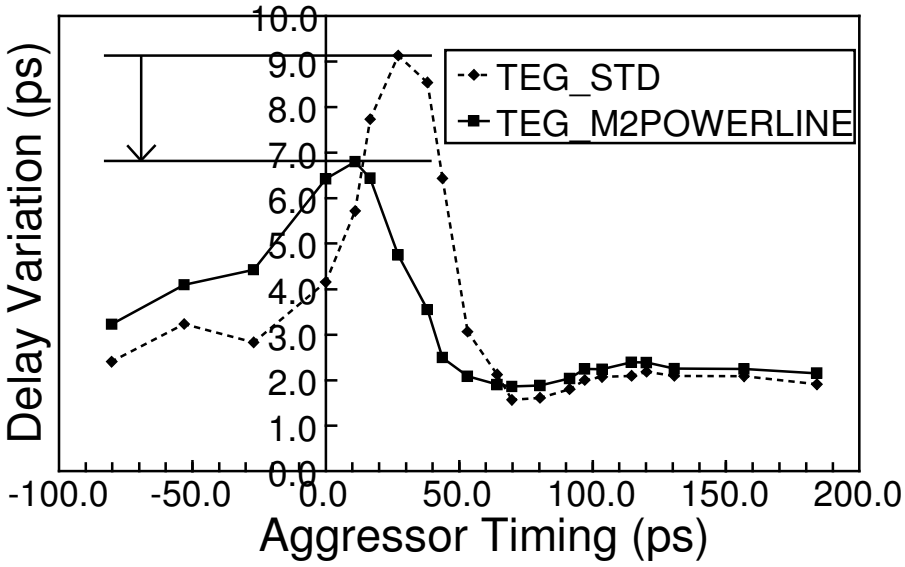

Figure 2.20: Measurement of TEG_M2POWERLINE. Parallel wires in M2 weaken inductive coupling.

Measurement results are also compared with the simulation results on TEG_M2POWERLINE, TEG_NARROWWIRE, TEG_SMALLDRIVE,

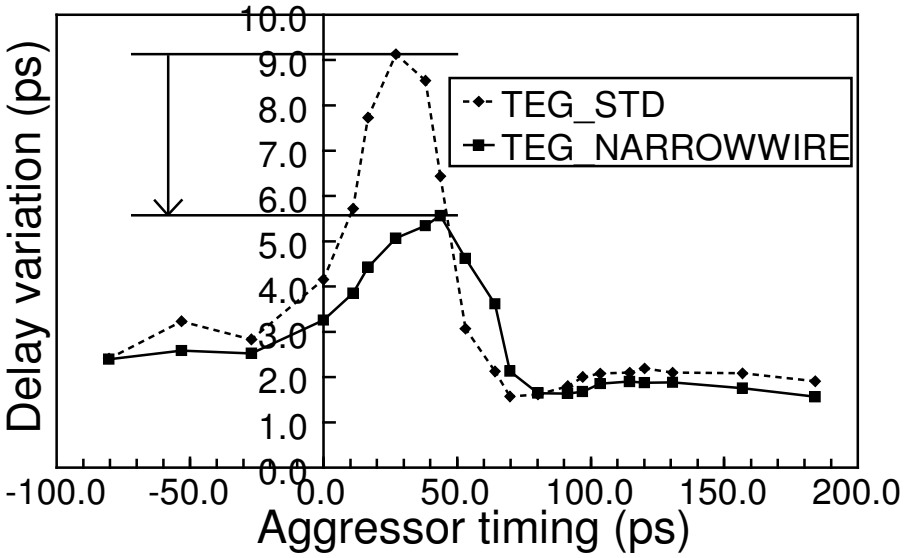

Figure 2.21: Measurement of TEG_NARROWWIRE. Narrow signal wires damp inductive noise.

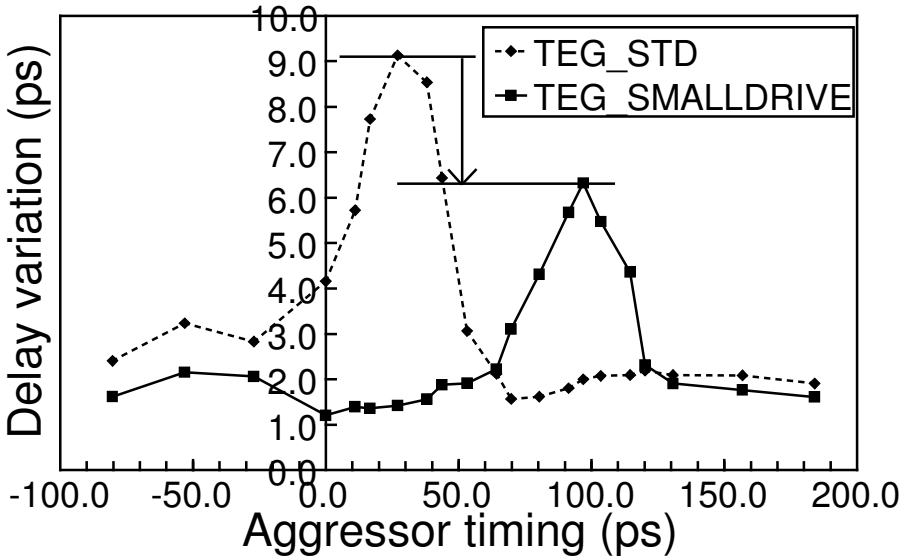

Figure 2.22: Measurement of TEG_SMALLDRIVE. Small driver injects less noise.

and TEG_LARGELOAD, in Figs. 2.25-2.28. RLC model is adopted for interconnect modeling in simulation because the difference between RLC and R(f)L(f)C model were small. In TEG_NARROWWIRE, TEG_SMALLDRIVE, TEG_LARGELOAD, simulation results are consistent with the measurement results, and validity of simulation model are proven. The effect of inductive coupling noise in TEG_M2POWERLINE in simulation is smaller

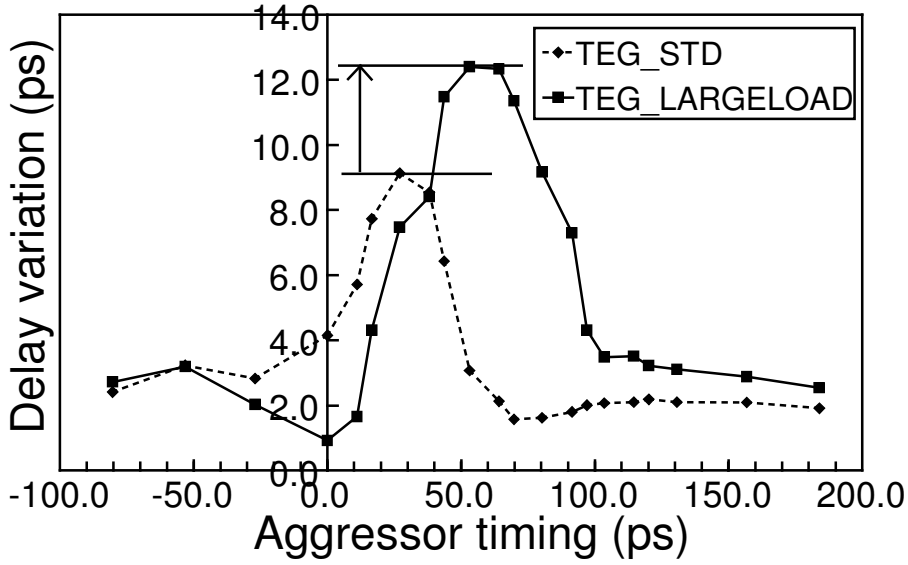

Figure 2.23: Measurement of TEG_LARGELOAD. Large receiver load enlarges noise susceptive timing.

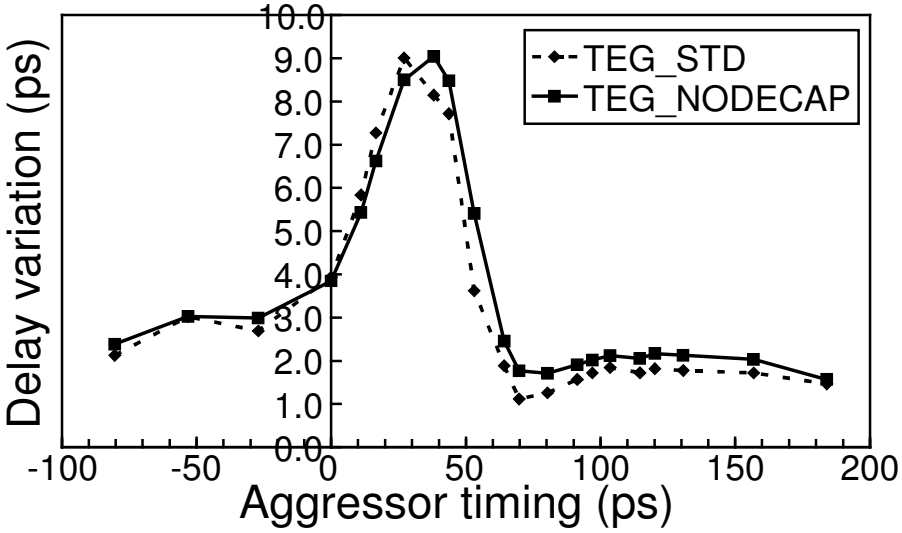

Figure 2.24: Measurement of TEG_NODECAP.

than measurement results. A possibility is that the resistivity of manufactured M2 lines was higher than it is expected. In this case, less return current would flow in the M2 lines, and inductive coupling was not weakened as much as it is expected.

RLC parameters of TEGs have been extracted for simulation, and here the RLC parameters of the TEGs are reviewed. The extracted interconnect parameters are shown in Tab. 2.1. The characteristic impedance is calculated as $\sqrt{|\frac{R+j\omega L}{j\omega C}|}$, where $\omega = 2\pi \times 17GHz$. In-

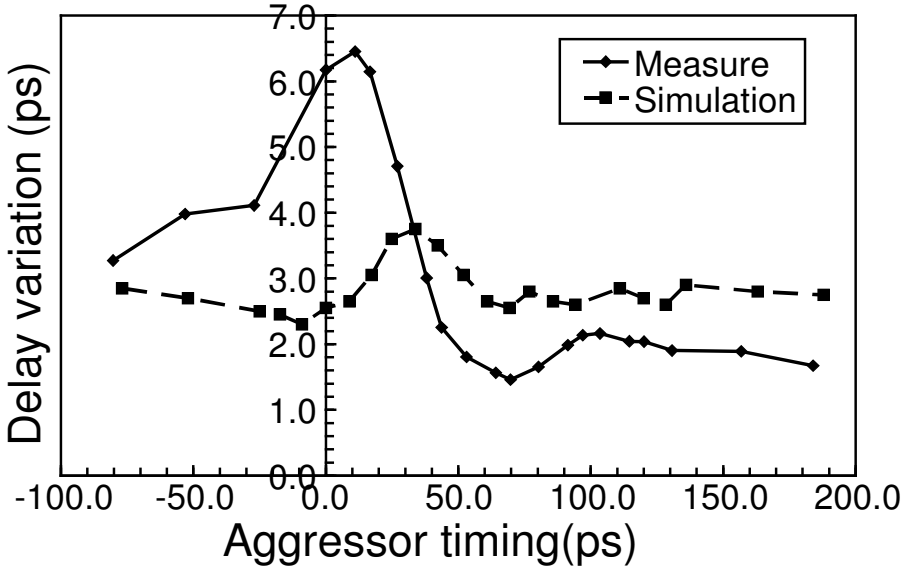

Figure 2.25: Comparison between measurement and simulation results of TEG_M2POWERLINE.

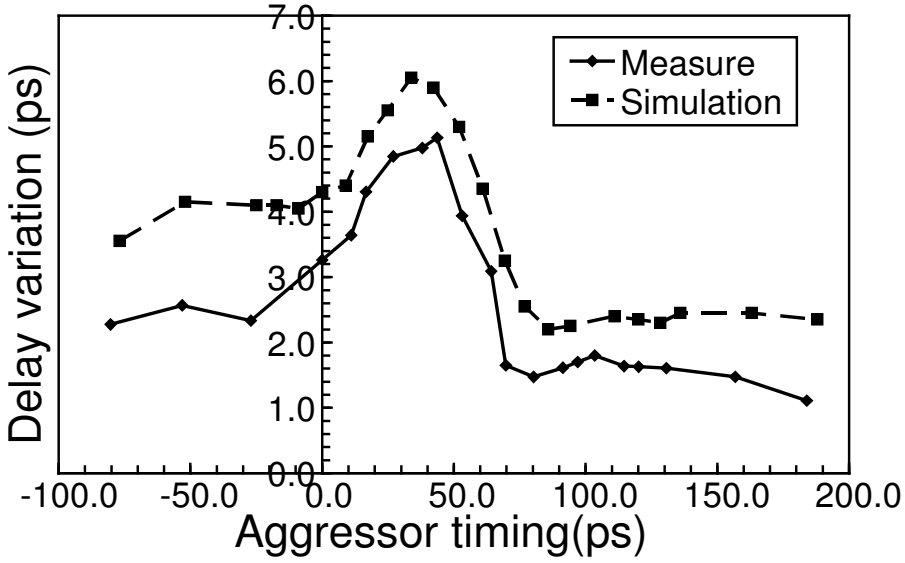

Figure 2.26: Comparison between measurement and simulation results of TEG_NARROWWIRE.

ductive coupling coefficient between a victim and a adjacent aggressor in TEG_STD was 0.338, and was reduced to 0.123 in TEG_M2POWERLINE where inductive coupling effect was reduced. Characteristic impedance Z_0 and resistance R_{wire} of interconnects on TEG_STD was 239Ω and 157Ω respectively. R_{wire} was 994Ω and Z_0 increased to 755Ω in TEG_NARROWWIRE where high R_{wire}/Z_0 ratio reduces the inductive effect [52]. In-

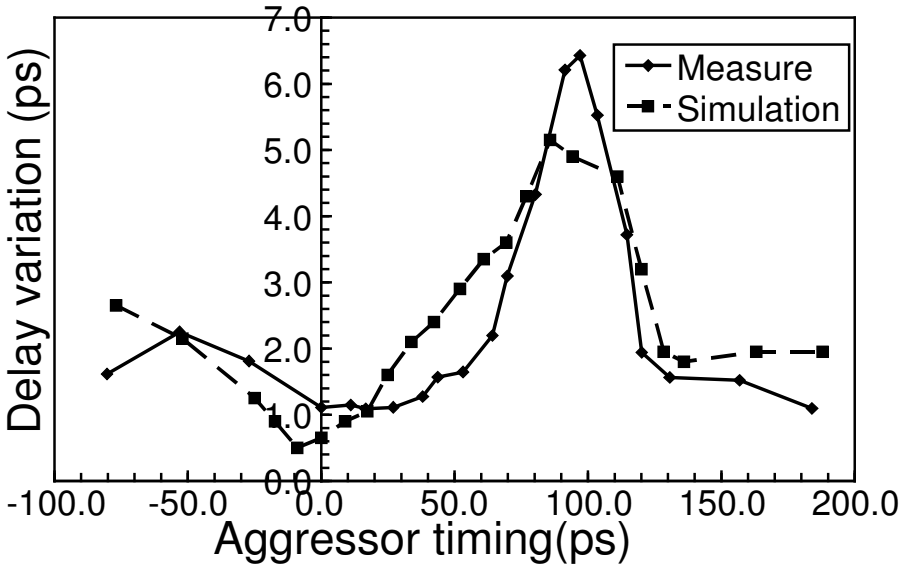

Figure 2.27: Comparison between measurement and simulation results of TEG_SMALLDRIVE.

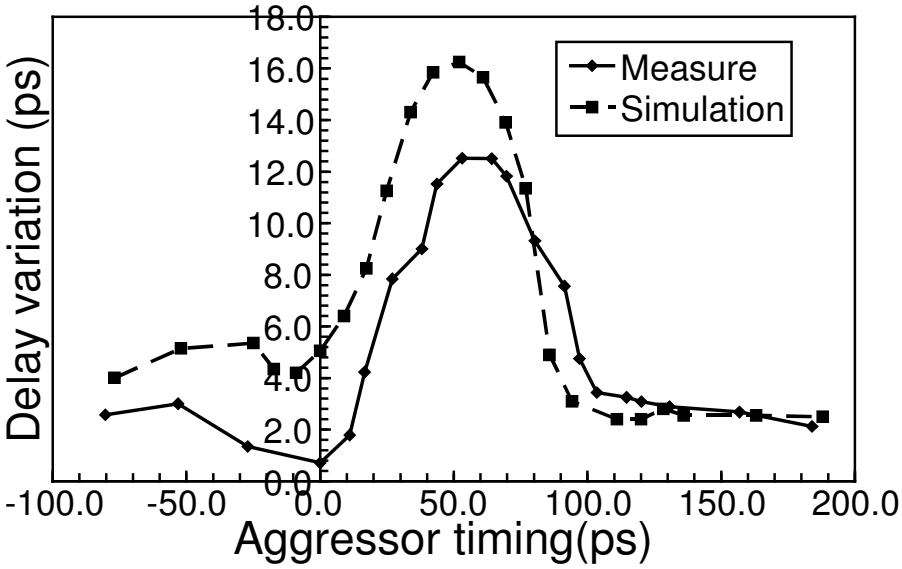

Figure 2.28: Comparison between measurement and simulation results of TEG_LARGELOAD.

crease of L(1.08 to 1.36nH) and decrease of C (163 to 103fF) also slightly contributes the increase of Z_0 in this TEG. In TEG_SMALLDRIVE where small driver restricts current injected to interconnects, driver resistance R_{driver} was increased from 120Ω to 500Ω, and Z_0/R_{driver} was reduced to 2.00 from 0.48. The variation of these interconnect parameters causes the change in inductive coupling noise discussed so far.

Table 2.1: Extracted interconnect parameters. R, L, C, Z_0 are resistance, self-inductance, capacitance, and characteristic impedance of the victim. K_L is inductive coupling coefficient between a victim and an adjacent aggressor.

TEG	R(Ω)	L(nH)	C(fF)	$Z_0(\Omega)$	K_L
TEG_STD	157	1.08	163	239	0.338
TEG_M2POWERLINE	150	0.78	162	233	0.123
TEG_NARROWWIRE	994	1.36	103	755	0.267

2.4.4 Noise superposition

This section discusses the superposition of the inductive coupling effect. Delay variation can be intensified/weakened by multiple aggressors based on their transition directions. This section first shows the cancellation effect by aggressors whose transition directions are opposite. This section next presents measurement results that show that the total timing variation by multiple aggressors can be estimated by the summation of timing variation due to each aggressor.

Cancellation effect

The cancellation effect was observed using the measurement setup in Fig. 2.29. Four aggressors on one side make the same direction transition as the victim, and four aggressors on another side make the opposite transition. The timing of aggressors is fixed, and that of victims is varied. The fall delay variation for victims was measured using the bypass circuit.

Figure 2.30 shows three delay variation curves measured with the TEG_STD on the test chip;
1) Aggressors with the same direction operate,
2) Aggressors with the opposite direction operate,
3) Both same and opposite direction aggressors operate.
The X-axis represents the delay of the victim input signal. It can be seen the delay increase in curve 1) and decrease in curve 2) caused by inductive coupling noise. On the other hand, a smaller delay increase is observed in curve 3), which means the mitigation of inductive coupling noise in the opposite direction transition. A decrease in inductive coupling noise caused by opposite direction transition on silicon was clearly observed.

Figure 2.31 shows three delay variation curves that are very similar to those in Fig. 2.30. The difference is that the transition timing of opposite aggressors is advanced by two-stage inverter delay. Curves 1) and 2) show delay increase and decrease similar to those in Fig. 2.30. As for curve 3), both the delay increase and decrease caused by the same and opposite transition are observed. This is because inductive coupling noises from two sources do not overlap each other because of the timing shift depicted in Fig. 2.29. The timing shift of the two-stage inverter delay corresponds to 25ps, and the noise cancellation occurs only in the narrow timing range.

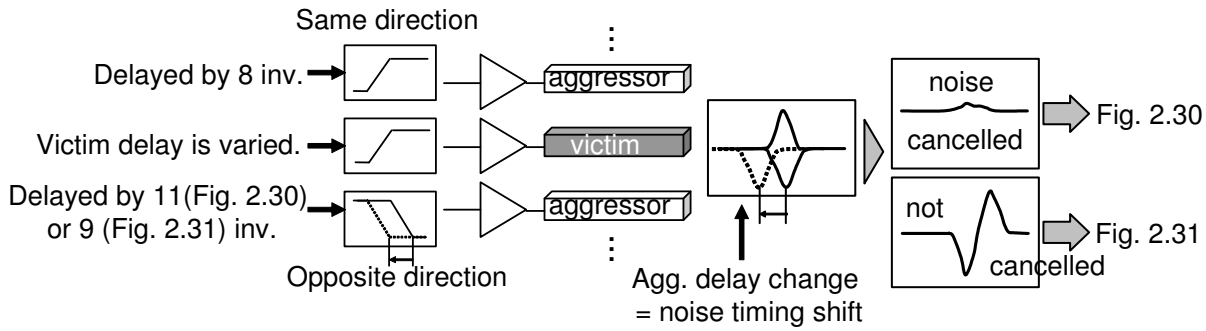

Figure 2.29: Measurement setup of Figs. 2.30 and 2.31. Same and opposite direction transition are input to aggressors to observe noise cancellation effect.

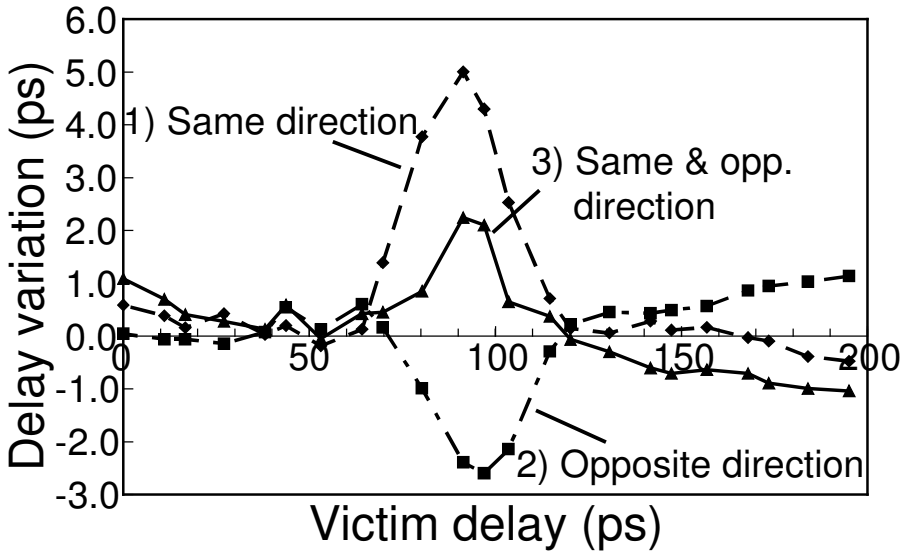

Figure 2.30: Measurement results when aggressors make same and/or opposite direction transition.

Superposition of noise effect

To reduce the capacitive coupling effect, prohibition of particular switching patterns is discussed, and several bus encoding techniques have been proposed [71–73]. However, applying these techniques to inductive coupling is very difficult, because the coupling effect from many far aggressors must be considered. In case of capacitive coupling, only adjacent aggressors are considered, and the number of switching patterns is limited. In contrast, the number of switching patterns for inductive coupling can exponentially increases with respect to the number of aggressors. For example, there are 4^9 switching patterns in a nine-line structure. Though the switching pattern might be reduced due to symmetry, verifying every

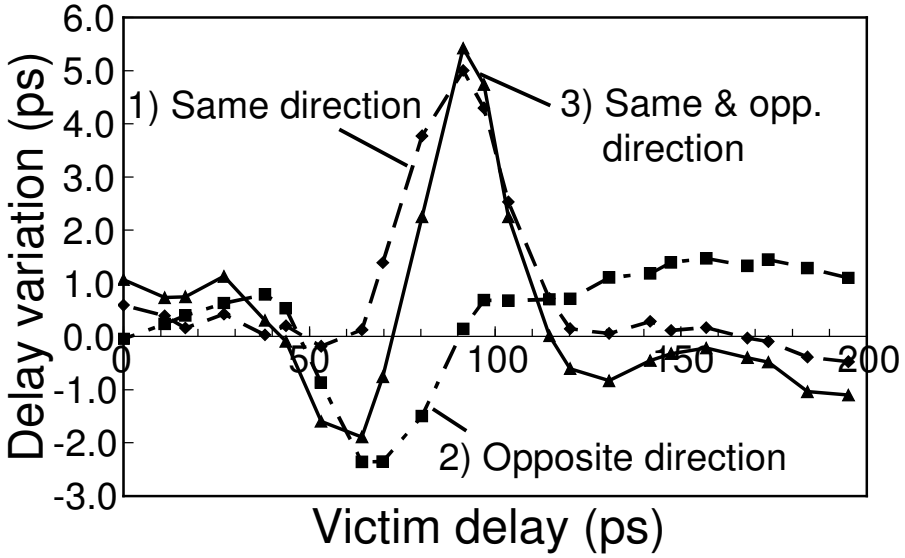

Figure 2.31: Timing of opposite direction transition is shifted from Fig. 2.30.

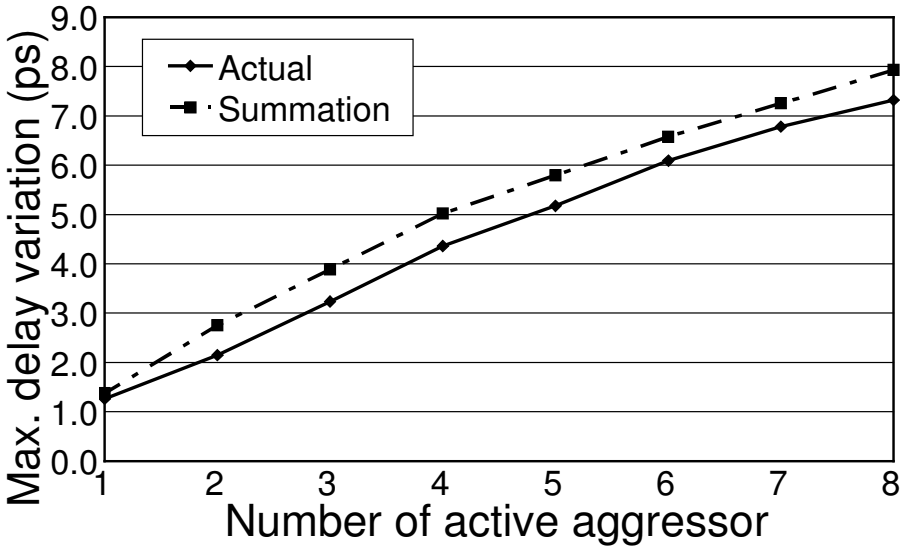

Figure 2.32: Measured maximum delay variation due to inductive coupling. Delay variations of overlapped noise and summation of individual noises are compared.

pattern using circuit simulation is still impractical.

Here, it is demonstrated that the inductive coupling noise effect by multiple aggressors on timing can be reasonably approximated with summation of delay variation due to each aggressor based on measurement results. This approximation enables us to determine which switching pattern may cause unacceptable delay variation. As discussed in section 2.2, the

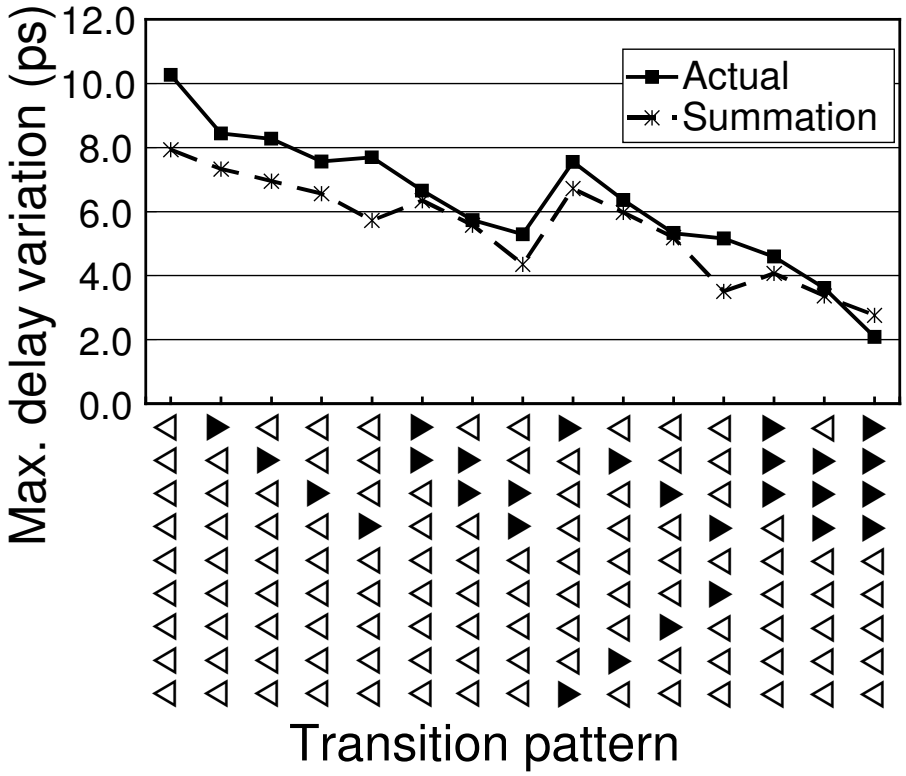

Figure 2.33: Measured maximum delay variation due to inductive coupling including opposite direction transition. Delay variations of overlapped noise and summation of each individual noise are compared.

overlapped crosstalk noise effect is equal to summation of each individual crosstalk noise in a linear circuit, and nonlinearity of MOS characteristics may disrupt this law. However, linear approximation can be effective as long as noise amplitude is small.

Figure 2.32 is a measurement result for delay variation due to inductive coupling. Actual delay variation due to multiple aggressors and summation of delay variation due to each aggressor are compared. We can see that the two curves are well correlated. This result indicates that delay variation due to multiple aggressors can be estimated by summing delay variation by each aggressor with a reasonable accuracy. Figure 2.33 shows the delay variation with various input patterns. The X-axis represents the transition pattern. △ and ▼ are rise and fall transitions, respectively. In each column, the center symbol is the victim, and the other eight symbols correspond to eight aggressors. There are a huge number of switching patterns, and 15 dissimilar and asymmetrical transition patterns were selected and the rise delay variation at the center was measured . The curve of summation finely follows the curve of the actual variation in Fig. 2.33. The measurement results show that the summation of each individual noise effect can approximate the actual noise effect, including the cancellation effect.

2.5 Summary

In summary, this chapter measured a significant effect of inductive coupling on timing in 90nm global interconnects and demonstrated that inductive coupling has become a practical design issue in advanced technologies. This chapter evaluated interconnect models, and RLC-distributed constant model gives a good correlation with measurement results. This chapter also verified characteristics unique to inductive coupling, such as the long-range effect and the shielding effect caused by ground wires on silicon. Mitigation effects of inductive coupling with power lines, driver sizing, and narrowed wire were verified by measurement results. The superposition and cancellation effects were finely observed on silicon, and measurement results indicated that delay variation by multiple aggressors can be estimated with acceptable accuracy based on the summation of delay variation by each aggressor.

Chapter 3

Quantitative Prediction of On-Chip Capacitive and Inductive Crosstalk Noise and Tradeoff Between Wire Cross-Sectional Area and Inductive Crosstalk Effect

Capacitive and inductive crosstalk noises are expected to be more serious in advanced technologies. However, quantitative values of capacitive and inductive crosstalk noises in the future have not been concurrently and sufficiently discussed, though capacitive crosstalk noise has been intensively studied solely as a primary factor of interconnect delay variation. This chapter quantitatively predicts the impact of capacitive and inductive crosstalk in prospective processes, and reveals that interconnect scaling strategies strongly affect relative dominance between capacitive and inductive coupling [74–76]. Our prediction also makes the point that the interconnect resistance significantly influences both inductive coupling noise and propagation delay. This chapter then evaluates a tradeoff between wire cross-sectional area and worst-case propagation delay focusing on inductive coupling noise, and show that an appropriate selection of wire cross-section can reduce delay uncertainty at the small sacrifice of propagation delay [75, 76].

3.1 Introduction

In nano-meter technologies, interconnect delay dominates gate delay and accurate estimation of interconnect delay has become an important design issue. Capacitive and inductive crosstalk is a well-known obstacle for accurate interconnect delay estimation. Capacitive crosstalk is widely considered in current designs, whereas inductive crosstalk noise emerges in recent processes. Qualitative discussion generally shows that both capacitive and inductive crosstalk noises will be more significant as the fabrication processes advance, though a paper

reports that impact of capacitive crosstalk is reduced in most of shortened interconnects [77]. Technology advancement increases capacitive crosstalk noise owning to a larger aspect ratio of interconnects structure and sharper signal transition waveforms. In wide and fat global interconnects, fast transitions including higher signal frequency component strengthen inductive crosstalk effect.

Crosstalk noise has been widely discussed based on formulas and simulations [58, 59, 77], and verified with measurement results [63, 78]. Chapter 2 in this thesis is also one of the works on the measurement results. However, a quantitative prediction considering both capacitive and inductive crosstalk noises in the future has not been reported, as far as the author know, in spite of its increasing importance.

This chapter focuses on 1) predicting capacitive and inductive crosstalk noises in the future processes and 2) revealing that delay uncertainty due to inductive coupling can be mitigated by adjusting wire cross-sectional area with a small delay penalty.

This chapter predicts the impact of capacitive and inductive crosstalk noise in predictive technologies with circuit simulation. Assumption that process parameters, such as transistor performance and power supply voltage, follow ITRS prediction [79, 80] is adopted. Quantitative prediction results indicate whether capacitive or inductive coupling noise become dominant, and show how notable impact it will have in future process.

This chapter also evaluates a tradeoff between wire cross-sectional area and propagation delay focusing on inductive coupling noise, because the prediction suggests that the interconnect resistance significantly influences both inductive coupling noise and propagation delay. There are several past works for crosstalk reduction that discuss adjusting interconnect spacing for capacitive noise [81], differential signaling [58], and noise immunity design in a processor design [82]. This chapter focuses on mitigation of inductive crosstalk effect by narrowing interconnect. A careful selection of wire cross-section reduces inductive coupling without much degrading the worst-case propagation delay. By cross-sectional area tuning, the consideration of inductive coupling, which includes inductance extraction involving large matrix computation [23, 83, 84], becomes unnecessary without modified design procedure and new design tools.

This chapter is organized as follows. Section 3.2 qualitatively discusses crosstalk noise on global interconnects. Section 3.3 describes assumed scenarios of technology advance for crosstalk prediction. Section 3.4 presents quantitative prediction of capacitive and inductive crosstalk. Section 3.5 discusses wire cross-section and crosstalk-induced delay. Finally section 3.6 concludes this chapter.

3.2 Qualitative discussion on crosstalk noise

This section explains transmission line effects of interconnects. The characteristics of capacitive and inductive crosstalk noise and their increase due to process scaling are also described.

3.2.1 Transmission line effects of global interconnects

Transmission line effects should be considered in a long interconnect when signal rise time is short [12]. The interconnect considered as a transmission line is represented as an RC or RLC distributed circuit in circuit simulation, and its current return path has to be appropriately modeled for RL extraction. An approach to determine driver size is impedance matching between driver output resistance and interconnect characteristic impedance. When the characteristic impedance is equal to the driver resistance and the driver is a CMOS gate, 50% of supply voltage is injected to the interconnect. MOS termination, which is open-end when the receiver is a CMOS gate, doubles the voltage at the end of the interconnect, and a sufficient voltage to sense is input to the receiver. Signal attenuation is also an important characteristic for a long interconnect. The injected signal is attenuated to $e^{-\alpha l}$, where α is attenuation constant and l is interconnect length.

3.2.2 Crosstalk noise and process advancement

Capacitive crosstalk arises from a coupling capacitance between interconnects. In the case of two coupled interconnects as shown in Fig. 3.1, a signal transition on one interconnect induces a voltage fluctuation on the other interconnect. The induced noise voltage v_{noise} is roughly expressed as $v_{noise} \propto RC_C \cdot dV/dt$, where C_C is a coupling capacitance between two interconnects, and R is resistance between the noise observation point and the ideal voltage source including interconnect resistance and driver resistance. Improvement of transistor performance by process advancement increases dV/dt, which results in deterioration of capacitive crosstalk noise. In the case of the equivalent circuit of Fig. 3.1, the peak voltage of capacitive crosstalk noise v_{max} is approximately expressed by Eq. (3.1) [85].

$$v_{max} = \frac{RC_C \cdot v_{dd}}{R(C + C_C) + t_r/2}, \tag{3.1}$$

where t_r is the signal rise time at the aggressor. Equation (3.1) shows that the noise peak voltage becomes large, but not drastically with respect to dV/dt (=v_{dd}/t_r) increase. Reduced interconnect spacing and enlarged aspect ratio of interconnects with technology advance increase coupling capacitance. These qualitative arguments indicate that capacitive crosstalk noise will be severer in the future.

Inductive crosstalk comes from a mutual inductance between interconnects. Assuming two coupled symmetric interconnects, current variation on one interconnect causes a voltage fluctuation on the other interconnect, which is explained with an equation $v_{noise} = M \cdot dI/dt$. M denotes mutual inductance. Higher signal frequency due to technology progress, that is larger dI/dt, makes the effect of inductive crosstalk significant. On the other hand, interconnect scaling increases interconnect resistance and characteristic impedance of the interconnect. Large characteristic impedance decreases current flowing in the interconnect and mitigates the effect of inductive crosstalk. Inductive coupling is hardly shielded by signal lines and spreads to wide area, which is different from capacitive coupling. Inductive crosstalk noise is caused by many aggressors, and their noises are superposed, though capacitive crosstalk noise is caused by only adjacent interconnects.

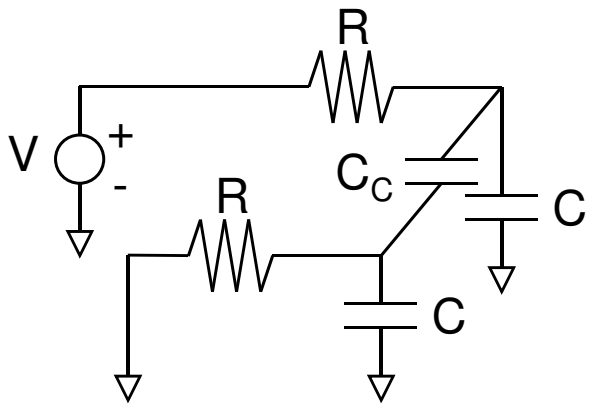

Figure 3.1: Equivalent circuit of two symmetric coupled interconnects.

Figure 3.2 shows an example of noise waveform in the case that capacitive and inductive crosstalk noises simultaneously appear. Supposing two lossless coupled transmission lines, the propagating voltage wave is represented as the sum of even and odd mode waves [59]. The times of flight for capacitive and inductive coupling are given by the Eqs. (3.2) and (3.3) respectively.

$$\begin{aligned} t_{C_C even} &= l\sqrt{CL} \\ t_{C_C odd} &= l\sqrt{(C+2C_C)L} \end{aligned} \tag{3.2}$$

$$\begin{aligned} t_{Meven} &= l\sqrt{C(L+M)} \\ t_{Modd} &= l\sqrt{C(L-M)} \end{aligned} \tag{3.3}$$

where l is interconnect length and L is self inductance of the interconnect. The odd mode wave of inductive coupling travels faster than the other waves and inductive crosstalk appears first as depicted in Fig 3.3. Capacitive and inductive crosstalk noises are opposite in voltage to each other, and they somewhat cancel each other, which results in the waveform that a capacitive crosstalk noise follows an inductive crosstalk noise as shown in Fig. 3.2. In this chapter, the noise waveform where capacitive crosstalk is dominant is called “capacitive crosstalk noise”, and the noise waveform where inductive crosstalk is dominant is called “inductive crosstalk noise”.

3.3 Scenarios of process advance and simulation setup

This chapter predicts influence of capacitive and inductive crosstalk based on circuit simulation. This section shows two scenarios of process scaling. Simulation setup, which includes interconnect structure, is also described.

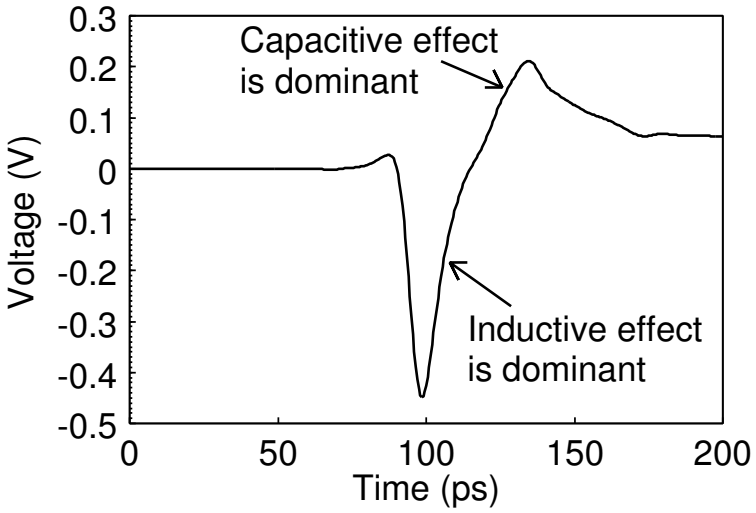

Figure 3.2: An example of crosstalk noise waveform.

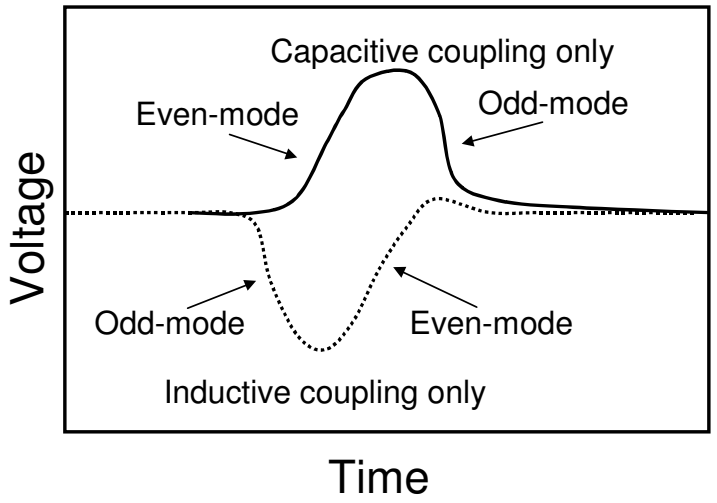

Figure 3.3: Conceptual crosstalk noise waveform considering either only capacitive coupling or only inductive coupling.

3.3.1 Assumed scenarios

This chapter assumes the following two scenarios of process advancement for 90nm, 65nm, 45nm, and 32nm processes.

Scenario 1

Interconnect cross-section, transistor performance, supply voltage, and dielectric constant of insulator follow ITRS [79, 80] prediction.

Table 3.1: Process parameters in Scenario 1.'/' separates the parameters of S=W / S=4W.

Process	90nm	65nm	45nm	32nm
Signal rise time(ps)	25.0	15.6	10.0	6.3
Supply voltage(V)	1.2	1.1	1.0	0.9
Relative dielectric const.	3.3	2.8	2.6	2.2
Interconnect width(μm)	1.00	0.67	0.49	0.35
Interconnect spacing(μm)	1.00/4.00	0.67/2.68	0.49/1.96	0.35/1.39
Interconnect thickness(μm)	0.90	0.64	0.49	0.34
Num. of division	9/9	14/13	21/19	35/30
Characteristic impedance(Ω)	121/138	139/168	149/180	180/214

Scenario 2

Interconnect cross-section is unchanged, whereas transistor performance, supply voltage, and dielectric constant of insulator follow ITRS [79, 80] prediction similarly to Scnenario 1.

Scenario 1 assumes that the process parameters scale down following ITRS roadmap, which is an industrial standard prediction about the progress of the semiconductor technology.

Scenario 2 assumes that a thick metal layer is provided for high-speed interconnection and power distribution. Therefore the wire cross-section is kept unchanged.

Interconnect scaling makes interconnect resistance larger because of narrowing interconnect. Larger resistance leads to longer propagation delay of interconnects, which is a disadvantage for high-performance and long-distance signaling. The assumption of interconnect scaling in Scenario 2 means that an interconnect layer, whose size does not scales down and resistance is low are prepared for long-distance signaling. It is reasonable to suppose that interconnect layers with no scaling or slower scaling than ITRS prediction are provided.

3.3.2 Simulation setup in Scenario 1

In Scenario 1, characteristics of transistor, supply voltage, and dielectric constant come from ITRS prediction. Cross-section of interconnects is scaled down with the ratio described in ITRS roadmap. Both decrease of width and increase of aspect ratio are considered. Table 3.1 summarizes the parameters at each technology node in Scenario 1.

The interconnect structure used for crosstalk noise evaluation is shown in Fig. 3.4. There are eight aggressors and a victim at M6 layer. The victim is placed at the center of aggressors, and power lines locate at both outer sides. In this structure, long-range effect, which is a characteristic unique to inductive coupling, can be evaluated. On a real chip, inductive coupling with parallel wires at other layers also could be a design issue. This thesis only examines the bus structure in which all signal lines are aligned at a single layer, however, a similar prediction can be performed straightforward. Orthogonal lines are placed at M2-M5,

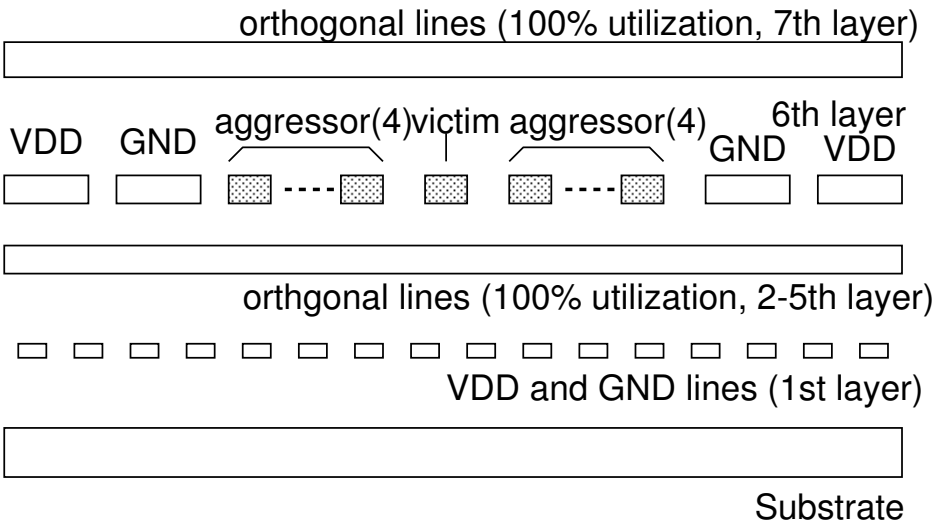

Figure 3.4: Interconnect structure for RLC extraction and circuit simulation.

and M7 layers, and their track utilization ratio is 100%. Power/ground lines at M1 layer run parallel to the bus interconnects. Width and thickness of the bus interconnects are set to 1μm and 0.9μm respectively, and scale in proportion to ITRS prediction at 65-32nm processes. The 1μm-wide interconnects in a 90nm technology correspond to high performance interconnects. As for wire spacing, two parameters are used; S=W and S=4W, where W is interconnect width and S is spacing. In S=W structure, wires are placed densely and capacitive crosstalk noise is significant. On the other hand, in S=4W structure, the spacing is widened so that capacitive crosstalk is suppressed, which is a common technique in current designs. As a result, inductive crosstalk may dominate capacitive crosstalk. The interconnects are 10mm-long and divided with repeaters. The number of division is calculated using Eq. (3.4) [13]. Equation (3.4) gives the division number which makes the propagation delay minimum.

$$k = \sqrt{\frac{0.4 R_{int} C_{int}}{0.7 R_0 C_0}}, \tag{3.4}$$

where k is the number of division, R_{int}, C_{int} are total resistance and capacitance of the interconnect, R_0, C_0 are output resistance and input capacitance of the minimum size inverter in each process.

RLC distributed constant model is adopted as an interconnect model for circuit simulation. Resistance, capacitance, and inductance of interconnects are extracted with a 3D field solver [16]. Orthogonal lines at upper and lower layers and the substrate are considered in capacitance extraction. Return current is assumed to flow only in parallel power/ground lines at M6 and M1 layers in inductance and resistance extraction. Resistance and inductance of interconnects are frequency dependent, and values at significant frequency [12] are chosen. Significant frequencies of 90nm, 65nm, 45nm, and 32nm processes are 13.6GHz,

21.8GHz, 34GHz, and 54GHz respectively. Drivers of interconnects are CMOS inverters, and the size is chosen such that the driver output resistance matches with the characteristic impedance of the interconnect as listed in Table 3.1. Resistance is often ignored in characteristic impedance calculation especially in the case of high frequency. However, resistance term is not negligible for this evaluation, and the characteristic impedance is calculated considering resistance. When evaluating noise peak voltage, the driver is modeled as a resistance for simplicity. Rise signals are input to all aggressors at the same timing and the peak voltage of the victim far-end noise is observed. In propagation delay evaluation, rise signals are input to all aggressors and the victim. The relative transition timing between the aggressors and the victim is changed, whereas all aggressors make transitions at the same timing.

Evaluation in this chapter uses a transistor model for circuit simulation developed so that DC and AC characteristics match with ITRS2004 prediction [86]. Fundamental parameters such as threshold voltage, on-current, input capacitance and gate delay, are consistent with ITRS prediction. Layout parameters of standard cells of a 90nm CMOS technology are shrunk for other technologies according to gate length.

3.3.3 Simulation setup in Scenario 2

In Scenario 2, transistor performance, supply voltage, dielectric constant of insulator are the same with those in Scenario 1. Interconnect width and thickness are set to 1μm and 0.9μm, and spacing is 1 or 4μm at all technology nodes based on the assumption that a high-performance thick interconnect layer will be provided in every technology. Interconnects are 1mm-long and not divided because the interconnect structure is unchanged. Other conditions on interconnects, such as interconnect layer and bus structure, in Scenario 2 are the same as those in Scenario 1.

3.4 Prediction results and discussion

In this section, the impact of capacitive and inductive crosstalk noise at the future technology nodes is estimated based on the assumed scenarios of process advancement explained in Section 3.3.

3.4.1 Scenario 1

Figure 3.5 shows noise peak voltage normalized by supply voltage in Scenario 1. As process advances, the normalized peak voltage of capacitive crosstalk increases, and that of inductive crosstalk decreases. Shrinking interconnect spacing due to scaling enlarges coupling capacitance between interconnects relatively compared with grounded capacitance, which makes capacitive crosstalk significant. On the other hand, narrowing interconnect increases characteristic impedance of interconnects and decreases current, which results in reduction of inductive crosstalk noise. The high wire resistance also damps inductive noise.

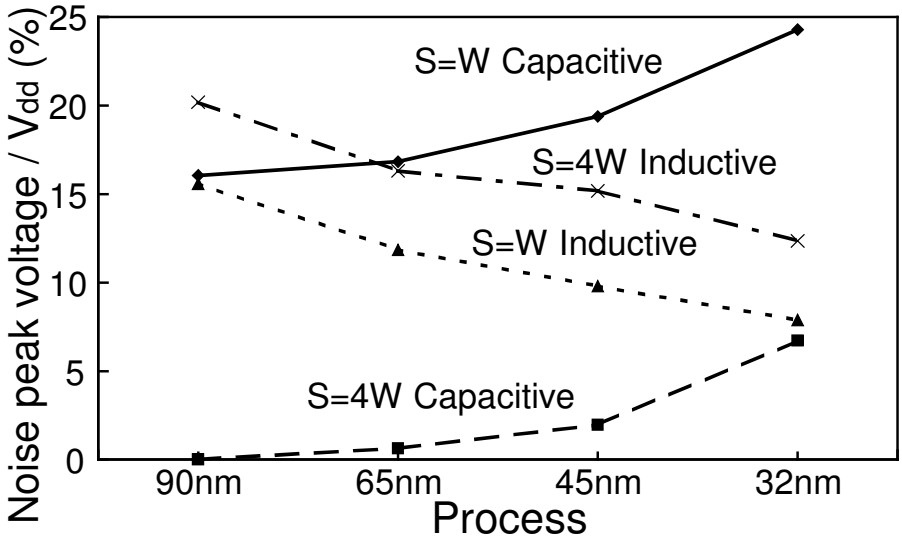

Figure 3.5: Noise peak voltage normalized by V_{dd} in Scenario 1.

Figure 3.6 shows the far-end noise waveforms in S=W structure. A gentle convex bump is caused by capacitive crosstalk and a sharp concave spike comes from inductive coupling. In the 90nm process, both capacitive and inductive crosstalk noises appear. On the other hand, in more advanced processes, capacitive crosstalk becomes dominant in S=W structure and comparable to inductive coupling in S=4W structure.

Figures 3.7 and 3.8 present delay variation rate in Scenario 1. Delay variation rate is defined as D_{var}/D_{silent}, where D_{var} is the delay variation and D_{silent} is the delay when all aggressors are silent, i.e. no transitions at aggressors. The delay between 50% points of driver input and final receiver output is observed. In the current configuration of transition direction, delay increase is caused by inductive crosstalk noise, and capacitive crosstalk noise decreases the delay, because a noise waveform such as Fig. 3.6 is superposed on the rise transition of the victim. In S=W structure, the impact of capacitive crosstalk dominates that of inductive crosstalk as process advances. Inductive crosstalk is notably suppressed by technology progress even in S=4W structure. Delay increase due to inductive coupling noise is hardly found in 32nm technology. This section therefore concludes that inductive coupling will be less important in the future advanced technologies.

3.4.2 Scenario 2

Noise peak voltages normalized by supply voltage in Scenario 2 are shown in Fig. 3.9. The figure indicates that technology progress considerably increases the normalized peak voltage of inductive crosstalk noise because of faster switching speed in advanced processes and the non-scaled interconnect structure in Scenario 2. On the other hand, the effect of capacitive crosstalk is slightly reduced.

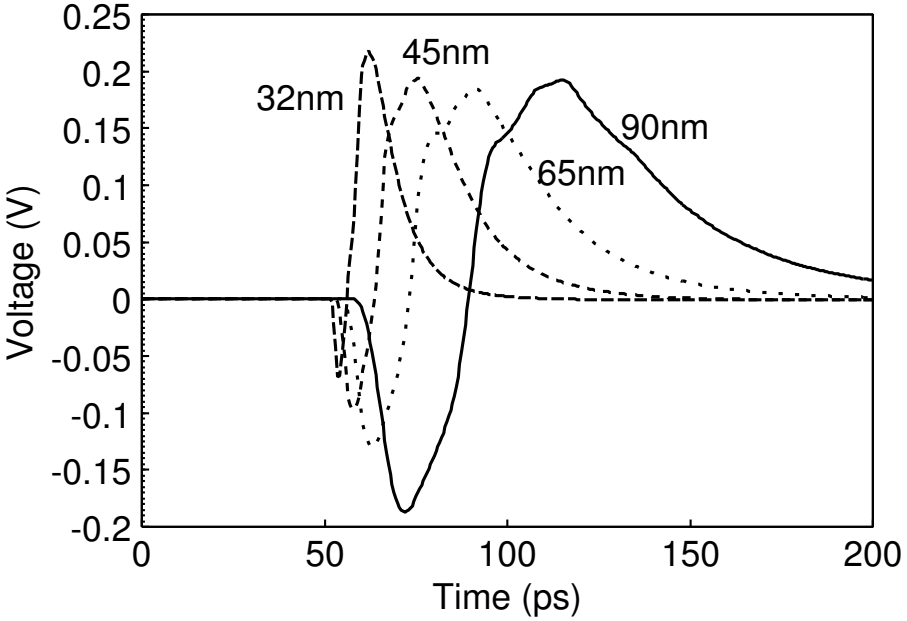

Figure 3.6: Far-end noise waveform in Scenario 1, S=W structure.

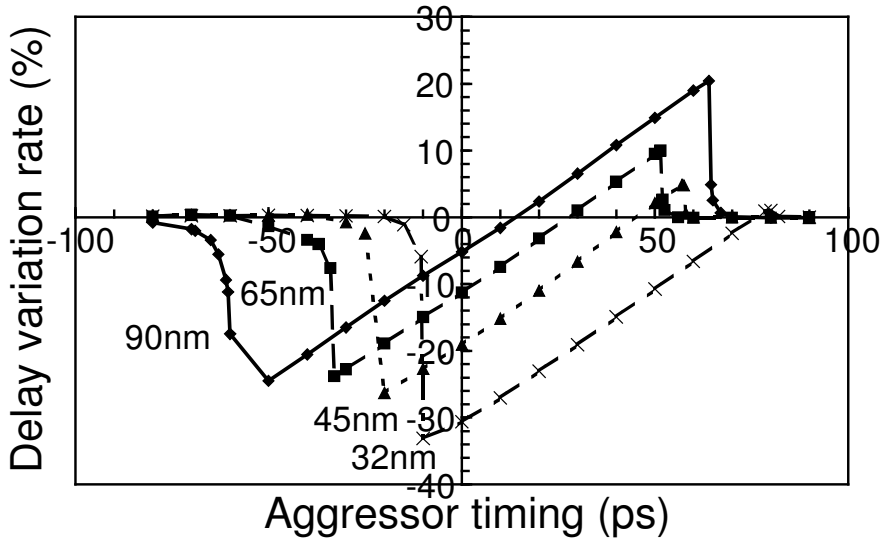

Figure 3.7: Delay variation rate in Scenario 1, S=W structure.

Figure 3.10 compares the normalized peak voltages of capacitive crosstalk noise simulated with RLC ladder model and with RC ladder model. The effect of capacitive crosstalk simulated with RC model increases as seen in Fig. 3.10, which is consistent with the relation between capacitive crosstalk and rise time of aggressor signal [85, 87]. Figure 3.10 implies

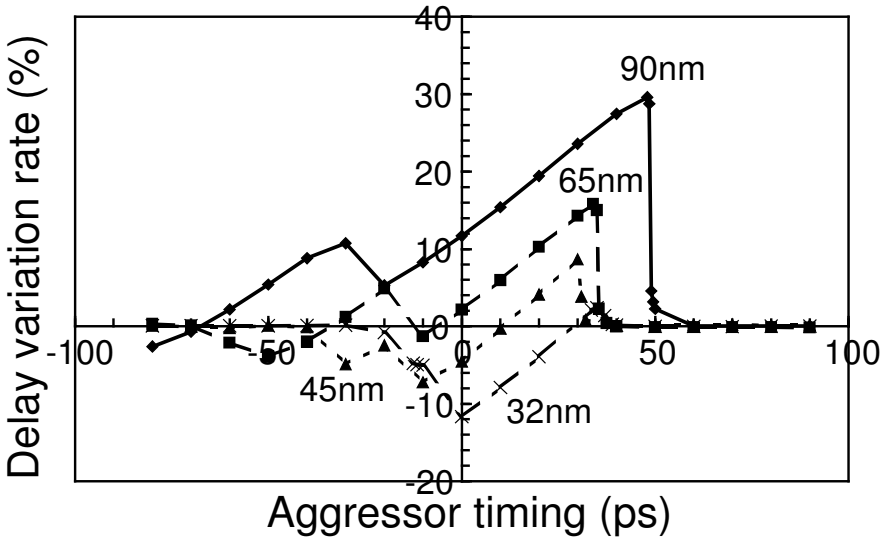

Figure 3.8: Delay variation rate in Scenario 1, S=4W structure.

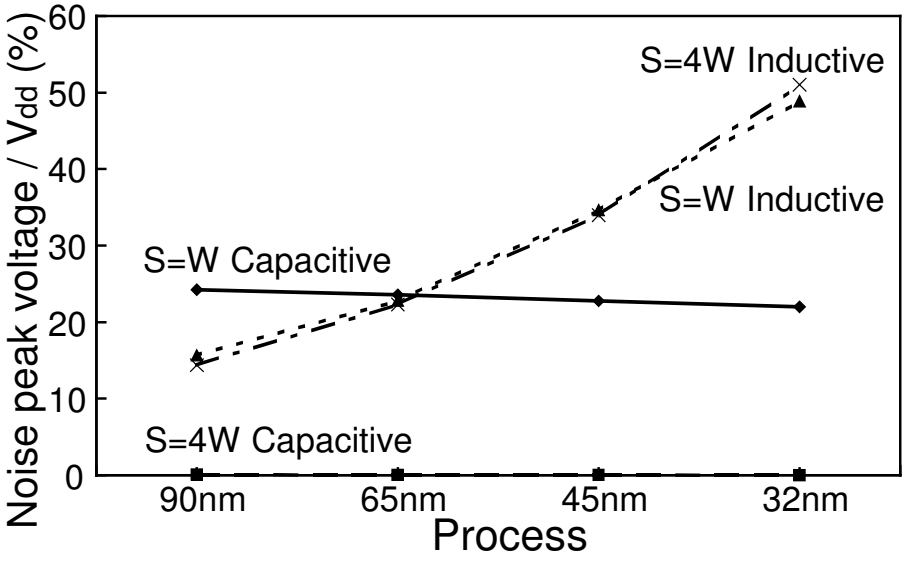

Figure 3.9: Noise peak voltage normalized by V_{dd} in Scenario 2.

that capacitive crosstalk noise is overwhelmed by inductive noise because consideration of inductance mitigates capacitive crosstalk.

Figures 3.11 and 3.12 present delay variation rate in Scenario 2. The impact of inductive crosstalk, which is observed as positive delay variation, is dominative. Though there is considerable increase of noise peak voltage in Fig. 3.9, the maximum delay variation is

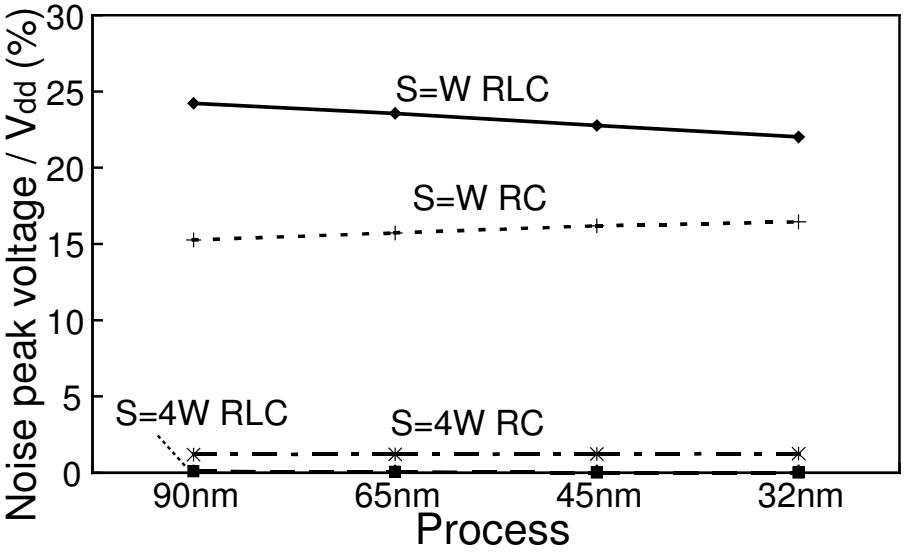

Figure 3.10: Noise peak voltage of capacitive crosstalk normalized by V_{dd} in Scenario 2.

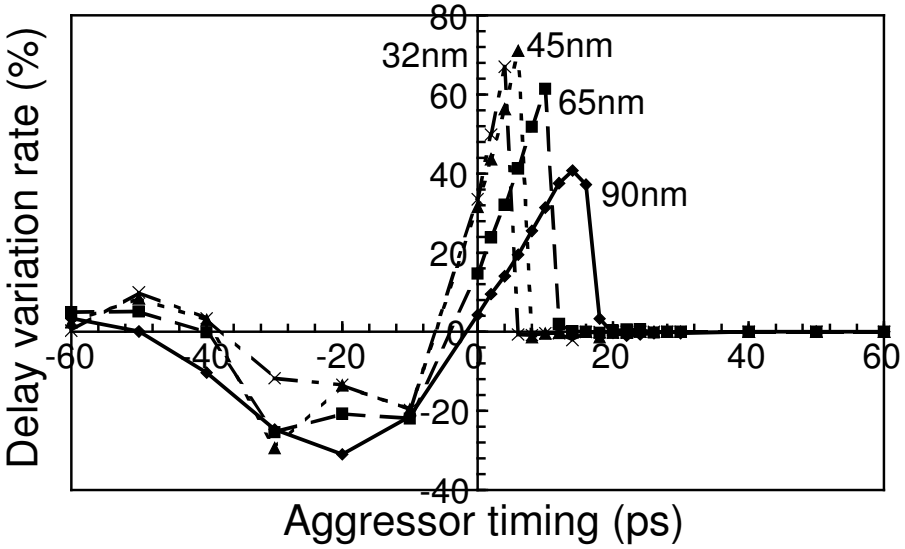

Figure 3.11: Delay variation rate in Scenario 2, S=W structure.

scarcely deteriorated. Increase of noise peak voltage is not tightly reflected in the delay variation. This is because the delay variation due to inductive crosstalk noise depends on both the noise peak voltage and the noise width.

As far as either capacitive or inductive crosstalk extremely dominates the other, the period in which inductive crosstalk noise appears mainly depends on the difference between the times of flight for capacitive and inductive coupling as depicted in Figs. 3.2 and 3.3. A

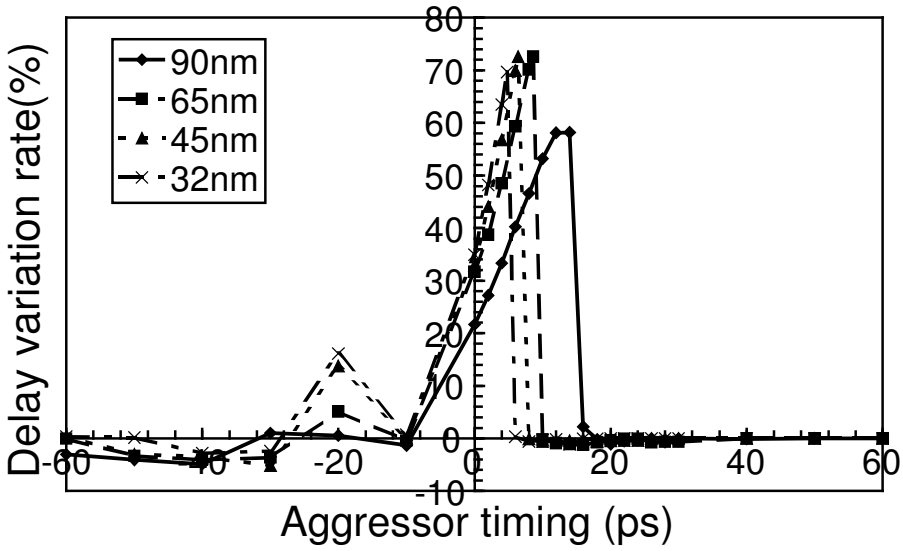

Figure 3.12: Delay variation rate in Scenario 2, S=4W structure.

longer interconnect enlarges the difference of the times of flight, and delay variation due to inductive crosstalk noise increases as shown in Fig. 3.13.

The timing range, when inductive crosstalk effect is dominant, becomes narrower in advanced processes. Figure 3.14 presents the detail of Fig. 3.12 concerning aggressor timing from -10 to 20ps. Inductive crosstalk effect on timing appears when inductive crosstalk noise overlaps signal transition waveform. Advancement of MOS performance shrinks signal rise time, and the overlappable timing range decreases, which results in the narrower timing range in Fig. 3.14.

The second peak of positive delay variation is found near -20 to -30 aggressor timing in Figs. 3.8, 3.11, and 3.12. Figure 3.15 shows the far-end noise waveform in 32nm process, S=4W structure, as an example. There are two concave peaks in the waveform. The second peak of delay variation derives from the second peak of the concave waveform. The second concave peak caused by the difference of the times of flight among even and odd mode of capacitive and inductive coupling.

3.5 Wire cross-sectional area tuning for inductive crosstalk free interconnects

Thick and wide interconnects generally provide short propagation delay, yet consumes large interconnect resource. Our prediction in Section 3.4 demonstrates that thick and wide interconnects in Scenario 2 involve larger inductive crosstalk, which may mean that interconnect delay will not be nicely improved even with thick and wide interconnects in the future if special techniques such as differential signaling and shield insertion are not used. On the other

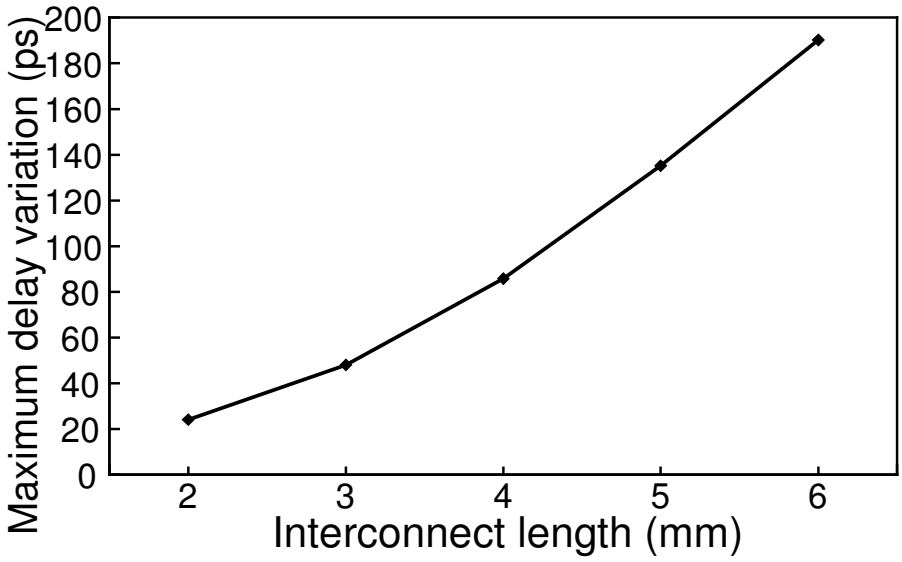

Figure 3.13: Maximum interconnect delay variation vs. interconnect length.

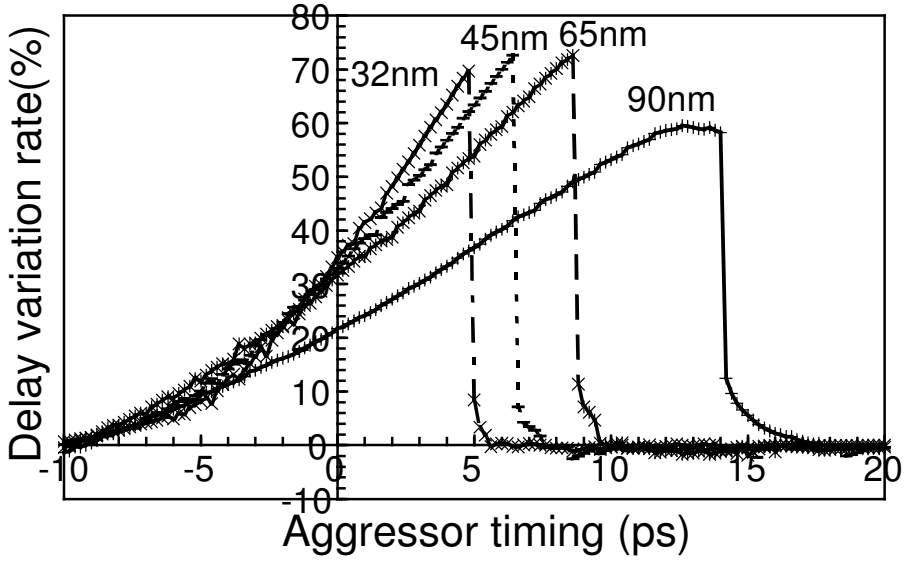

Figure 3.14: The detail of Fig. 3.12 concerning aggressor timing from -10 to 20ps.

hand, narrowing interconnect reduces delay uncertainty due to inductive crosstalk, because it increases wire resistance. However, unfortunately propagation delay also increases. This observation motivates us to explore the tradeoff between the worst-case delay considering inductive coupling noise and interconnect cross-sectional area. This section examines whether there is a wire cross-section that makes inductive coupling ignorable with a small penalty of delay increase. In other words, this section evaluates the maximum performance of intercon-

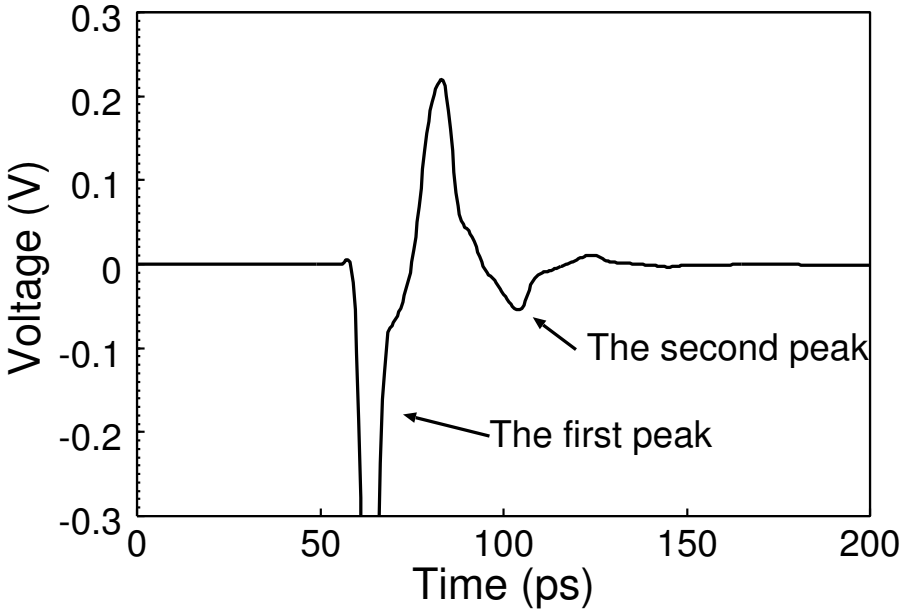

Figure 3.15: Far-end noise waveform in 32nm process, S=4W structure.

nects whose inductive coupling does not have a significant impact on timing design.

3.5.1 Evaluation setup

This section evaluates the interconnect propagation delay varying cross-sectional area from $1\mu m^2$ to $0.05\mu m^2$. The interconnect structure for RLC extraction and evaluation conditions are the same as Scenario 1 in Section 3.3. S=4W structure is evaluated because this section focuses on the effect of inductive crosstalk. Drivers of aggressors and victim are 32X inverters. Scaling of cross-sectional area reduces both of the interconnect width and thickness. Following description explains how the width and thickness, that is, aspect ratio of interconnects are determined.

Determination of aspect ratio

The aspect ratio of interconnect at each cross-sectional area and process is decided such that the worst-case delay considering capacitive crosstalk is minimized. You might think that circuit designers could not change the interconnect thickness. However, the integration of inductive crosstalk free interconnect can be considered as one of the design strategies cooperated by circuit designers and process integrators, and this section determines the aspect ratio for each process and cross-sectional area. The worst-case delay is estimated by circuit simulation with an interconnect structure in Fig. 3.16. Generally, most of interconnects are routed with S=W, and the coupling capacitance is large. This section therefore minimizes the worst-case delay of capacitive crosstalk noise as an metric. Resistance and capacitance

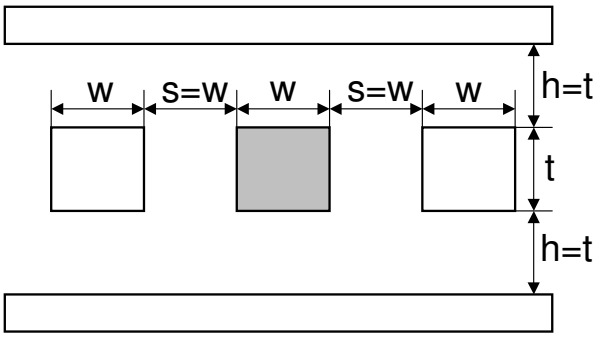

Figure 3.16: Wire structure for determining aspect ratio.

Table 3.2: Determined A/R (aspect ratio).

Cross-sectional area (μm^2)		1.00	0.81	0.64	0.49	0.36	0.25	0.16	0.1	0.07	0.05
90nm	A/R	1.4	1.4	1.4	1.4	1.4	1.4	1.5	1.5	1.4	1.5
	width (μm)	0.845	0.761	0.676	0.592	0.507	0.423	0.327	0.258	0.224	0.183
32nm	A/R	1.4	1.4	1.5	1.5	1.5	1.5	1.5	1.7	1.6	1.6
	width (μm)	0.845	0.761	0.653	0.572	0.490	0.408	0.327	0.243	0.209	0.177

of interconnects are calculated from formulas in [88, 89]. In deriving the aspect ratio, the coupling capacitance is doubled for considering Miller effect of capacitive coupling for simplicity. From these consideration, the aspect ratios are set as shown in Tab. 3.2.

3.5.2 Experimental results and discussion

Figure 3.17 plots the relation between the worst-case delay and delay variation rate with 90nm and 32nm transistor models. In Fig 3.17, points with larger worst-case delay and smaller delay variation correspond to smaller cross-sectional area. The worst-case delay is larger in narrower interconnects even if inductive crosstalk is considered. On the other hand, starting from the smaller worst-case value, i.e. large cross-sectional area, up to a certain point, narrowing interconnect notably reduces delay variation rate despite small degradation of the worst-case delay.

Figure 3.18 presents delay vs. interconnect width, where delay w/o noise is the delay without crosstalk noises, and the worst-case delay means the delay degraded with the maximum delay variation due to inductive crosstalk noise. The delay shown in Fig. 3.18 is normalized by the delay with $1\mu m^2$ cross-sectional area. Please note that shrinking wire cross-section narrows interconnect width, and saves the interconnect resource.

Suppose here that the influence of inductive coupling can be ignored if the delay varia-

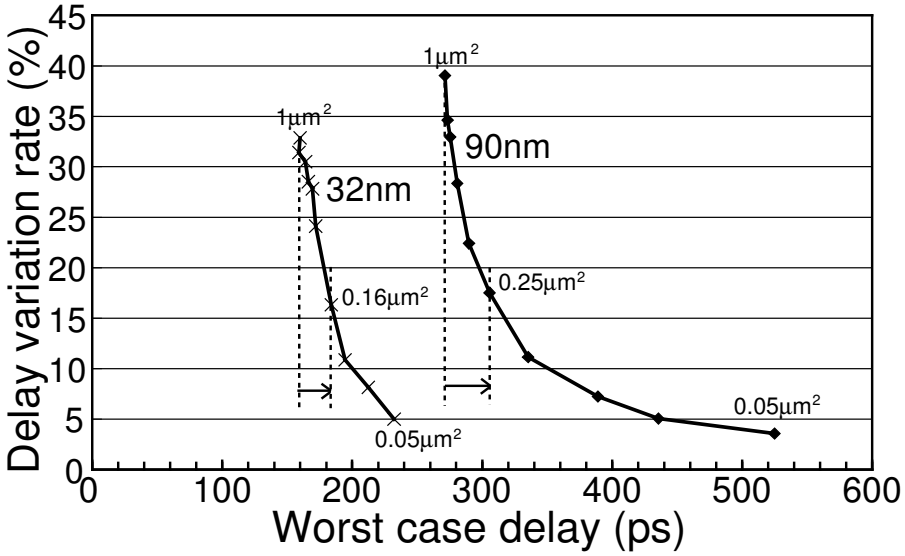

Figure 3.17: The worst-case delay vs. delay variation rate when cross-sectional are is varied.

tion rate is smaller than 15%. The delay variation rate at $0.16\mu m^2$ area is about 15% in 32nm process from Fig. 3.17. Compared with 1μm-wide interconnects, the use of interconnect resource is reduced by 61%. When the crosstalk noise is not considered, shrinking interconnect degrades the delay by 31% in Fig. 3.18. However, as a matter of fact, the worst-case delay considering inductive crosstalk noise increases only by 15%. This result indicates that narrowing cross-sectional area of high-performance interconnects can improve both efficiency of interconnect resource and delay variation due to inductive coupling in spite of small deterioration of the interconnect propagation delay. In addition, narrowed wires make special design effort to care for inductive coupling unnecessary, and reduces the simulation cost of inductive effect.

3.6 Summary

This chapter has presented the prediction of capacitive and inductive crosstalk effect in prospective processes. The peak noise voltage and delay variation due to crosstalk noise are evaluated in two scenarios, where interconnects scale down and do not scale. In the scenario with scaling, capacitive coupling will be more dominant and inductive coupling will be less important as technology advances. On the other hand, in the scenario without interconnect scaling, inductive coupling will be dominant.

The evaluation of the tradeoff between wire cross-sectional area and propagation delay considering inductive coupling noise is also presented. Shrinking the interconnect cross-section increases the propagation delay, but its increasing ratio is much reduced because higher wire resistance mitigates inductive coupling noise. An appropriate selection of inter-

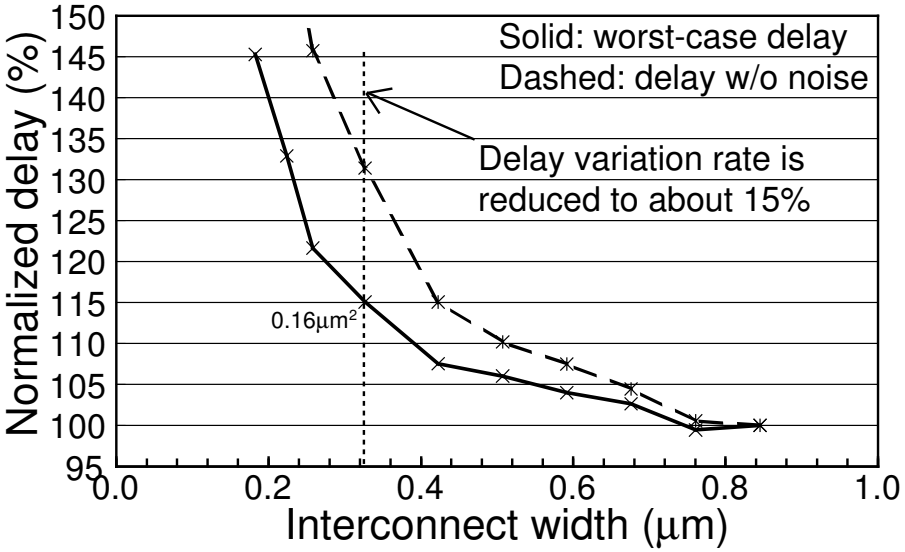

Figure 3.18: Normalized delay vs. interconnect width. Absolute delay values of worst-case delay and delay without noise at $1\mu m^2$ area are 160 and 120ps respectively.

connect cross-sectional area makes consideration of inductive coupling unnecessary with the small sacrifice of propagation delay.

Chapter 4

Validation of a Full-Chip Simulation Model for Supply Noise and Delay Dependence on Average Voltage Drop with On-chip Delay Measurement

Power integrity is a crucial design issue for nano-meter technologies because of decreased supply voltage and increased current. This chapter focuses on gate delay variation caused by power/ground noise, and develops a full-chip simulation current model with a capacitor and a variable resistor to accurately model current dependency on voltage drop [90–92]. Measurement results for 90nm technology are well reproduced in simulation. The error of average supply voltage is 0.9% in average. Measurement results also demonstrate that gate delay depends on average voltage drop.

4.1 Introduction

Power supply noise has become a critical issue in current VLSI design. The power consumption of high-performance chips is still increasing, and supply voltage is decreasing, resulting in a rapid increase in current. Increased current makes power distribution more difficult, and nowadays power supply noise can not be easily eliminated. Moreover, even when the amplitude of power supply noise remains the same, its impact on timing becomes more and more significant as supply voltage decreases. To advance chip design, delay degradation caused by power supply noise must be addressed.

To study on-chip power supply noise, [39–50, 54, 61, 93–95] measured noise waveforms. The effect of noise on timing, however, has been reported in few works [50, 51] and other works have been investigated through simulation [54, 96]. [50] studied transition waveform distortion due to sharp voltage spike. [51] discusses impact of power noise on clock signal.

This chapter discusses the gate delay variation caused by power supply noise, comparing the results from measurement and simulation in a CMOS 90nm technology. Measurement

Table 4.1: Average gate delay with noise in Fig 4.1.

	noise 1	noise 2	noise 3	noise 4
average gate delay (ps)	14.8	14.5	12.0	129.8

results demonstrate that gate delay is mainly dependent on average supply voltage, not on peak voltage, whereas [54,96] discussed with simulation. This chapter also constructs a full-chip simulation model that can accurately reproduce switching current dependence on noise-induced supply voltage. Full-chip simulation results with constructed model finely agree with measurement results. The developed switching current model considerably reduces computational cost, and enables the full-chip simulation of the test chip. For these purposes, ring oscillator is suitably used for the measurement, similarly to [97].

This chapter is organized as follows. Section 4.2 discusses the impact of average voltage drop on gate delay. Section 4.3 presents a full-chip simulation model that translates transistors into linear elements. Section 4.4 describes measurement circuit structure. Section 4.5 presents and discusses the results of our measurements. Section 4.6 concludes the chapter.

4.2 Effect of power supply noise on timing

Peak voltage drop is a serious issue in design of a power distribution network. However, average power supply voltage is more important than peak noise voltage where timing is the principal issue in digital circuit design because timing distortion is more dependent on average supply voltage during gate switching than on peak voltage [54].

This section shows an example of how the impact of power supply noise on timing can be estimated with average supply voltage. The four pseudo V_{dd} noise waveforms shown in Fig. 4.1 are assumed referring to [44]. V_{ss} waveforms are set to be upside down to V_{dd} waveforms. A 90nm CMOS process and an ideal supply voltage of 1.0 V are assumed. 50 cascaded inverter gates operate with the pseudo waveforms, and table 4.1 shows average gate delay. A rise signal was input to the first gate at 0ps, and the average delay of gates through which the signal propagated within 500ps is evaluated. The peak voltage drop of noise 1 is 0.2 V, and supply voltage recovers to 1.0 V in 500 ps. The voltage drop of noise 2 is set to the average drop of noise 1 from 0 to 500 ps. It can be seen that the average gate delay of noise 1 is almost the same as that of noise 2, and the delay difference is only 2.0%

In contrast, though the peak voltage drop of noise 3 is 0.3 V, which is larger than that of noise 1, the average gate delay with noise 3 is smaller because its recovery to 1.0 V is faster. Therefore, the average supply voltage of noise 3 is higher than that of noise 2. If the voltage of the worst-case drop (noise 4) is used, the estimated delay is unrealistically large. Timing estimation based on average supply voltage is more accurate than that based on peak voltage drop. In this way, the path delay depends on average supply voltage rather than the peak voltage drop or the shape of supply waveform.

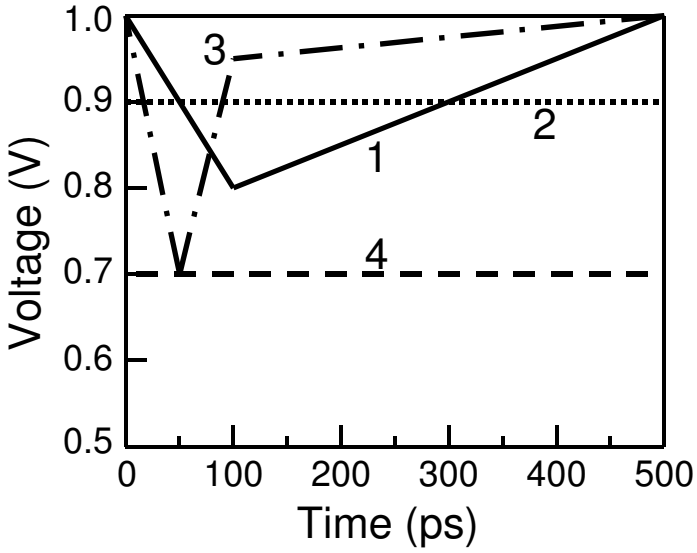

Figure 4.1: Pseudo V_{dd} noise waveforms.

4.3 Switching current model for full-chip simulation

Full-chip simulation of power/ground noise uses a great deal of CPU time and memory because of the tremendous number of elements on a chip. To efficiently simulate noise for a full chip, a switching current model is developed with capacitance and a variable resistor, a so-called variable switch model. This model can reproduce the switching current dependence on noise-induced supply voltage. This section begins by describing the accuracy and computational cost of the variable switch model. The parameter characterization method of the variable switch model is also explained.

4.3.1 Accuracy and simulation cost of linear element models

To make the simulation more efficient, transistor elements are generally replaced with linear circuit models such as current source and switch models [34]. The current source model represents a switching gate consisting of transistors as a voltage-independent current source. The switch model replaces a switching gate with resistance and capacitance [34]. The resistance value is ∞ or on-resistance of the corresponding transistor. Though supply voltage fluctuation changes the switching current, the switch model does not explicitly consider dependence of switching current on noise-induced supply voltage. The current consumption is not well reproduced in this model because the gate delay degradation due to power supply noise is not modeled.

The developed variable switch model has finely-defined variable resistance. The variable switch model is shown in Fig. 4.2. Supposing an inverter gate, a transistor element is

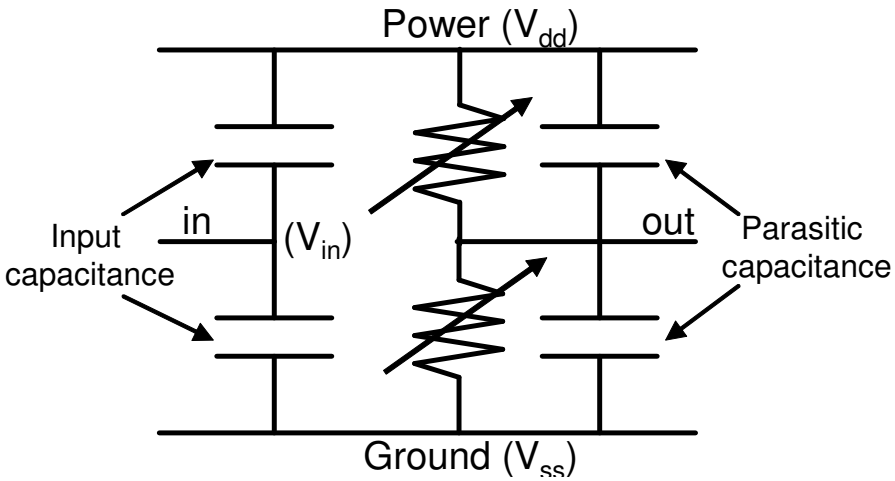

Figure 4.2: Variable switch model.

represented with input gate capacitance, output parasitic capacitance, and variable resistance depending on $V_{in} - V_{ss}$ for NMOS and $V_{dd} - V_{in}$ for PMOS. Rigidly speaking, not only resistance but also capacitance is also dependent on voltage, though this model adopts constant capacitance to simplify the model. Various parasitic capacitances and their variability are compensated by the characterization described in following section. For simulating the test chip, other single state cells, e.g. 2-input NAND, are modeled as Fig. 4.2. Each of the pull-up and pull-down networks are replaced by a single resistor whose resistance depends on V_{in}-V_{ss} for NMOS or V_{dd}-V_{in} for PMOS. There is another detailed approach that replaces each transistor with a single resistor. However, it is not necessary for simulation in this work, and thus it will not be discussed further.

Gate switching delay is accurately modeled in the developed model, which contributes to accurate full-chip simulation of the test chip. To distinguish between models, the conventional model with a constant resistance is called the constant switch model.

Figure 4.3 shows power supply noise waveforms simulated with the transistor model, the current source model, and the two switch models. The circuit for simulation includes 68 cells of 12-stage NAND gates. 400 times inductance of package is attached to the circuit so that the voltage drop becomes comparable to the measured voltage drop that will be demonstrated in Section 4.5. The V_{dd} waveform at the center of the grid is shown in Fig. 4.3. The current source and constant switch models show sharper voltage drop waveforms than the transistor model. On the other hand, the noise waveform of the variable switch model nicely follows that of the transistor model. This is because only the variable switch model can reproduce the gate delay degradation caused by the voltage drop.

Table 4.2 shows normalized simulation time, average of absolute error from the transistor model, and time needed for modeling. As can be seen, using the variable switch model reduces simulation time to 6.3%, which is considerable reduction. Integration of multiple cells into a single cell can further reduce simulation cost. When 68 cells in a grid are merged

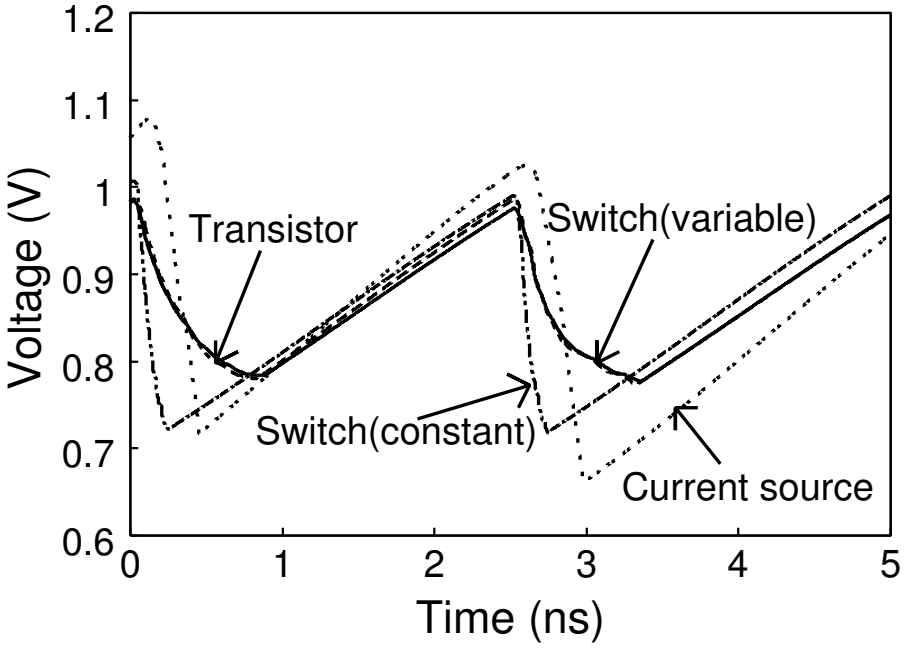

Figure 4.3: Supply noise waveform with transistor model, current source model, and two switch models. The waveforms with transistor and variable switch model are overlapping.

Table 4.2: Simulation time with each models normalized by that with transistor model. Average of absolute error and modeling time are also shown.

	transistor	current source	constant switch	variable switch	variable sw. (merged)
Sim. time	1	0.021	0.043	0.063	0.0059
Avr. error	-	97.3mV	38.2mV	4.3mV	4.0mV
Modeling	-	10sec.	5min.	9min.	9min.

into 4 cells, simulation cost is decreased to 0.59%, without accuracy degradation. Clearly, the variable switch model has reasonable simulation cost and accurately estimates noise waveforms. The modeling time is also acceptable. This model can be used for full-chip simulation, which is discussed in the Section 4.5.

4.3.2 Characterization of variable switch model

This section describes the characterization method for the model. To characterize the variable switch model, parameters such as variable resistances, input gate capacitances, and output parasitic capacitances must be determined. A schematic of the model is shown in Fig. 4.2. Variable resistance can be realized in circuit simulation with G-element [98] or behavioral

description such as in Verilog-A.

The total power consumption and current waveform are adopted for determination of capacitance and resistance in variable switch model. Total power consumption mainly depends on capacitance and is independent of resistance. These are determined in the following two steps: (Step 1) determines capacitance based on total power consumption, and (Step 2) determines resistance based on current waveform. In each step, this work determines parameters by minimizing the following objective functions.

In Step 1, the objective function is the difference between the integrations of current simulated with a variable switch model and of that simulated with a transistor model. Two circuits are shown in Fig. 4.4, which have current values of three voltage sources. These two circuits are used to simulate current because input and output capacitance cannot be computed separately with the upper circuit alone, as shown in Fig. 4.4. Here, C_{in} and C_{out} are input and output capacitance respectively. Total current consumption I_1 for the upper circuit is proportional to $C_{in} + C_{out}$, and C_{in} and C_{out} are indistinguishable. To compute input and output capacitance separately, the lower circuit is used. Output parasitic capacitances are connected to a separate independent voltage source in the lower circuit. I_2 and I_3 are proportional to $(2C_{in} + C_{out})$ and C_{out}, respectively, meaning that C_{in} and C_{out} become distinguishable. Though it is possible to determine parameters with the lower circuit alone, both the upper and lower circuits are used to improve fitting reliability. Input and output capacitances consist of capacitance between power and input/output and that between ground and input/output respectively. The ratio between capacitance to the power and to the ground is fixed to the ratio between PMOS and NMOS widths. This is because these capacitance values cannot be determined separately using the above procedure.

The objective function in Step 2 is the average absolute error of current waveform in Eq (4.1) in the time range from T_1 to T_2. T_1 and T_2 are chosen such that the circuit operation for characterization are fully included in the timing range. $I_{vsw}(t)$ and $I_{tr}(t)$ are current values at time t simulated with a variable switch model and a transistor model, respectively.

$$\frac{1}{T_2 - T_1} \int_{T_1}^{T_2} |I_{vsw}(t) - I_{tr}(t)| dt \tag{4.1}$$

While minimizing Eq. (4.1), resistance values are varied and capacitance values are kept unchanged. Variable resistance is piecewise linear function of $V_{dd} - V_{in}$ or $V_{in} - V_{ss}$. Resistance value at every $V_{dd} - V_{in}$ or $V_{in} - V_{ss}$ sample point is varied in this process.

As initial values of variable resistances, V_{ds}/I_{ds} values when V_{ds} is set to $V_{dd}/2$ are adopted. Initial values of input capacitances are found in the datasheet of a standard cell library or can be calculated with T_{ox} and transistor sizes. Output parasitic capacitance can be computed with peripheral length and area of drain/source, or, for simplicity set to, for example, 20% of the input capacitance. Other common approximation methods for resistance and capacitance of MOS can be used to determine initial values.

Figure 4.5 compares the simulation results for the inverter chain with those for the transistor and variable switch models. A variable switch model is characterized by the procedure described in this section. The feasible sequential quadratic programming (FSQP) algorithm [99] is used for numerical optimization. The current waveform fits well and aver-

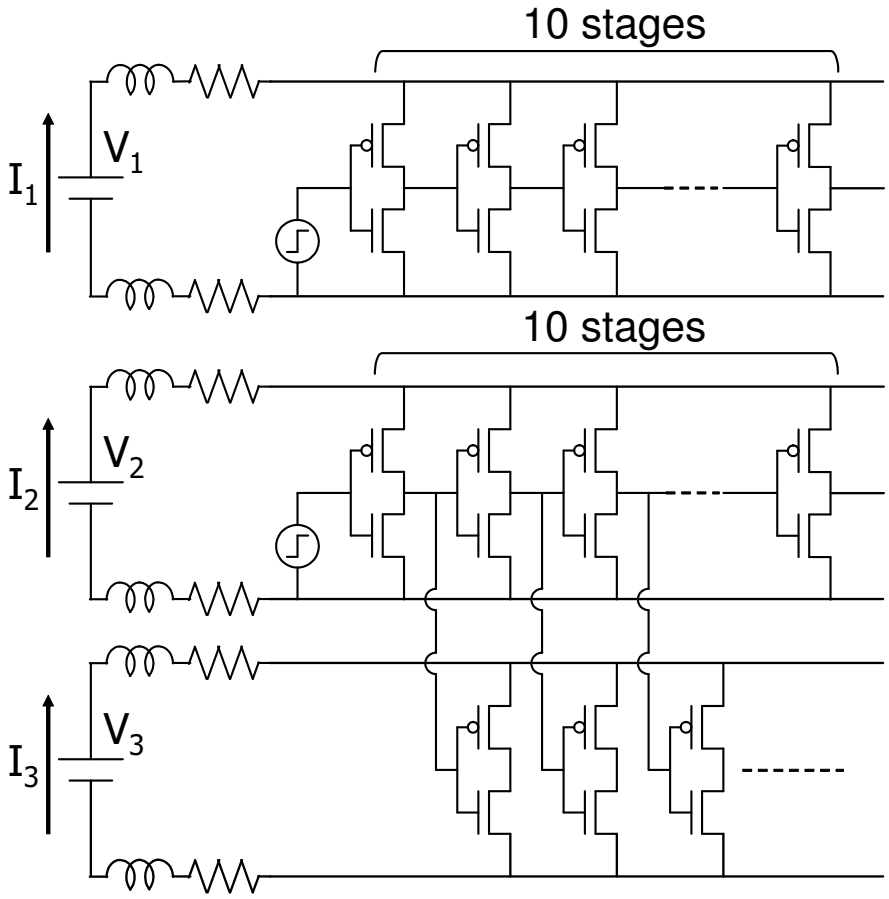

Figure 4.4: Circuits used to characterize variable switch model in case of inverter gate. Supply voltage of ideal voltage source V1, V2, and V3 are the same.

age error is only 2.4% of peak current consumption. It is also found that modeling accuracy is not sensitive to the initial values of numerical optimization.

4.4 Measurement circuit structure

The objective of test chip design is to make possible measurements that can be used as a reference for circuit simulation results. A test circuit was designed so that it can control power supply noise flexibly and measure gate delay variation caused by power supply noise.

Figure 4.6 roughly illustrates the layout of the test circuitry, which consists of a PLL (Phase Lock Loop), shift registers, power grid lines, ring oscillators, and NANDUNIT circuits. $1000\times1500\mu$m area is divided into 20×20 areas by the power grid. To observe power supply noise clearly, the width of the power grid line is intentionally adjusted to cause large power supply drop. The horizontal lines of the grid are 2.5μm width, 50μm pitch, and 0.9μm thickness, and vertical lines are 7.5μm width, 75μm pitch, and 0.3μm thickness. The loca-

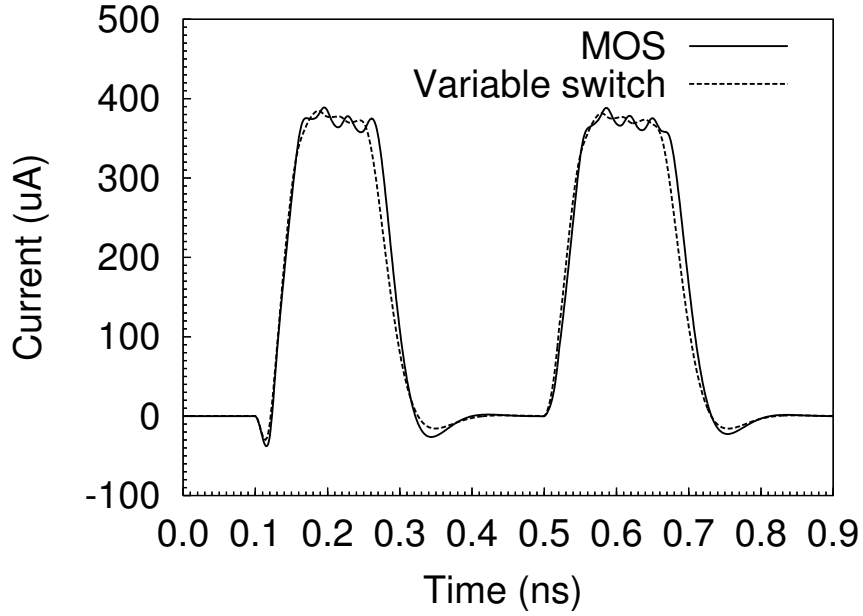

Figure 4.5: Current waveform of 20X size inverter simulated with transistor model and variable switch model. Waveform in this figure is simulated with upper circuit in Fig. 4.4.

tion of grids are represented as (x,y) in this chapter; $0 \leq x \leq 19$, $0 \leq y \leq 19$, leftmost rectangles are x=0, uppermost rectangles are y=0, as indexed in Fig. 4.6.

We implement a chain of NAND gates shown in Fig. 4.7 to cause power supply noise. We here call this circuit 'NANDUNIT'. NANDUNIT circuits (Fig. 4.7) are regularly and densely spaced in every grid. 17×4 NANDUNIT circuits are located in each grid. 75% of a $1000 \times 1500 \mu$m area is occupied by NANDUNIT circuits. The input signals 'clk', 'sel', and 'en1'-'en4' can change the noise waveforms in time, amplitude, and frequency, which will be explained in the following. The control signals of the NANDUNIT circuits, 'en1'-'en4' and 'sel', are input to each 4×4 grid.

A NANDUNIT circuit can operate both as a chain and as a ring oscillator. When 'sel'=0, NANDUNIT operates as a chain, and the clock signal generated by the PLL is input as 'clk' signal. The PLL can generate clock signal from 100 MHz-1 GHz, which is delivered to NANDUNIT circuits with H-tree clock lines. Controlling PLL can change the noise frequency. Figures 4.8 and 4.9 are simulated supply noise waveforms of 68 NANDUNITs in a single grid area with resistive power lines. The number of active gate stages can be changed using 'en2'-'en4' signals, i.e. operating time of the noise source is variable (Fig. 4.8), and noise waveform can be changed in time. The maximum number of stages of NANDUNITs is 12. This relatively short path length makes it possible to implement many NANDUNIT cells. As a result, simultaneous switching of many cells causes larger voltage drop especially in high frequency operation. When NANDUNIT operates as a ring oscillator with 'sel'=1, NANDUNIT circuits run continuously. The operating ratio is defined as the ratio

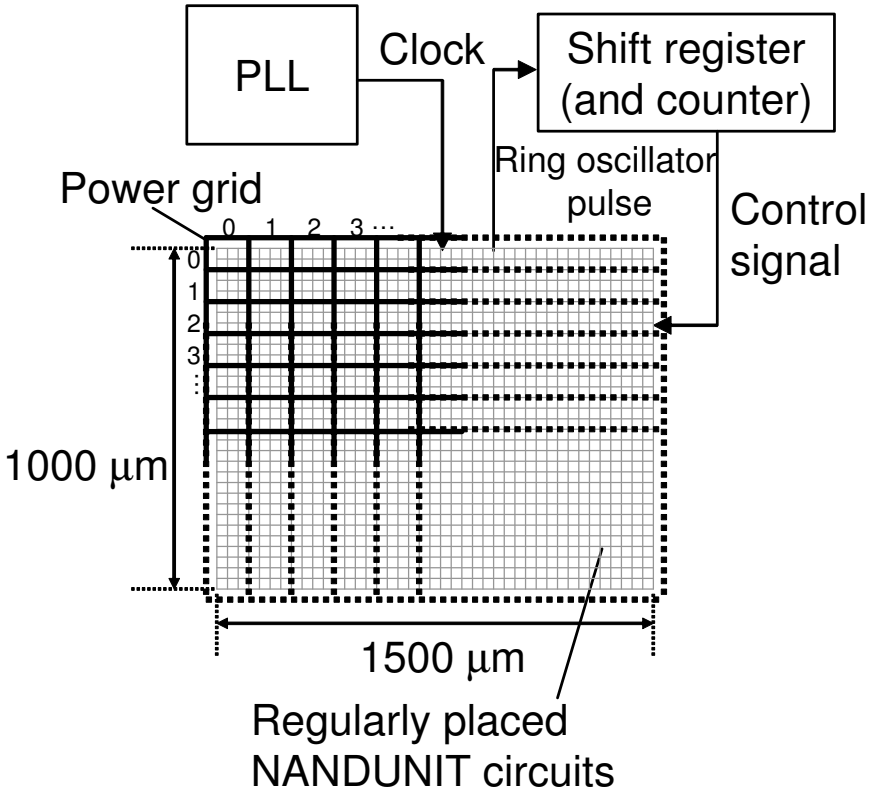

Figure 4.6: Overview of measurement circuit.

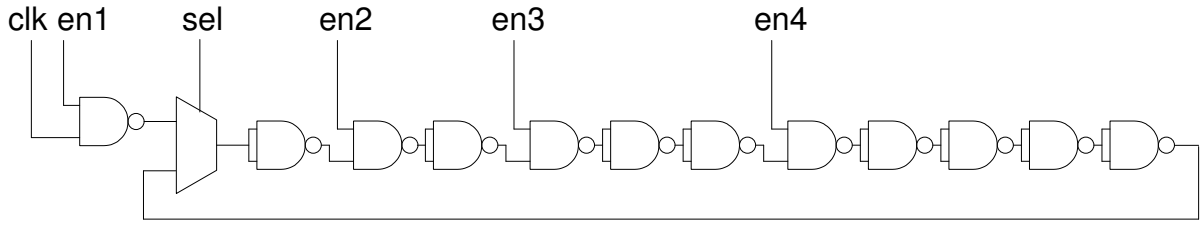

Figure 4.7: NANDUNIT circuit.

of active NANDUNITs with 'en1=1'. A control logic circuit is implemented so that the ratio can be selected from 100%, 50%, 25%, 0% for each 4×4 grid, aiming to control noise amplitude(Fig. 4.9).

NANDUNIT and PLL control signals are stored in the shift register. The counters are included in the shift register and operate both as the shift register and as the counter. Values of the shift register and counters are serially set/read externally.

To measure the variation in delay caused by power supply noise, 100 ring oscillators are uniformly placed at the center of (2n+1,2m+1) grids ($0 \leq n \leq 9$, $0 \leq m \leq 9$). Power/ground

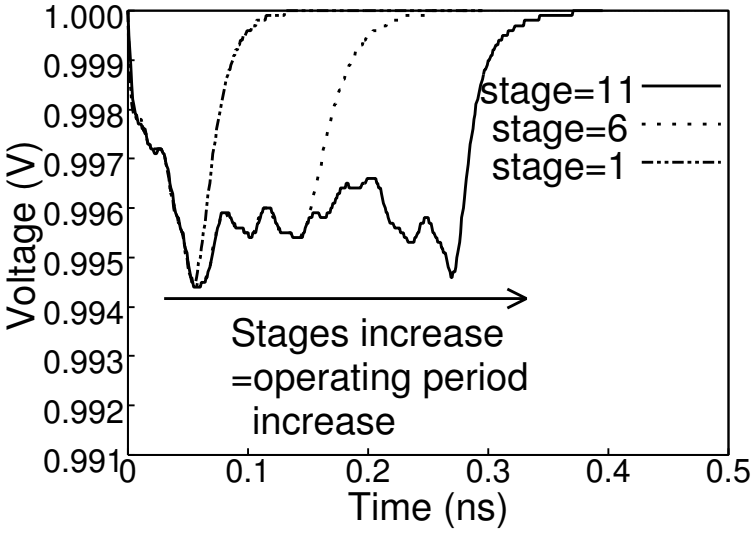

Figure 4.8: Power line noise waveform. Number of active gate stages changes.

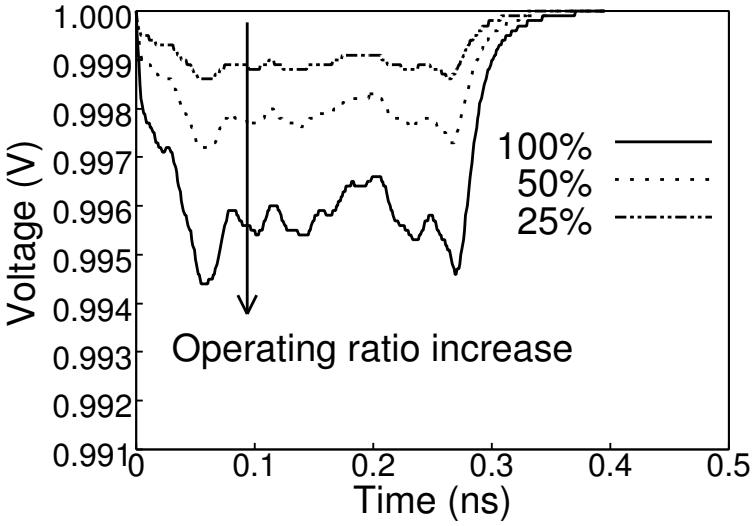

Figure 4.9: Power line noise waveform. Operating ratio changes.

lines are shared by ring oscillators and NANDUNITs, and the generated power and ground fluctuations influence the ring oscillator cycle. The counters counts the time cycle of the ring oscillators. The test chip packaged in a QFP(Quad Flat Package) is mounted on a PCB(Printed Circuit Board). Decoupling capacitance is not inserted inside the package, and then larger dI/dt drop due to the package inductance is observed. All external input and output signals are digital. Measurement is performed with a pattern generator and a logic analyzer. External signal includes input, output, clock of shift registers and several control

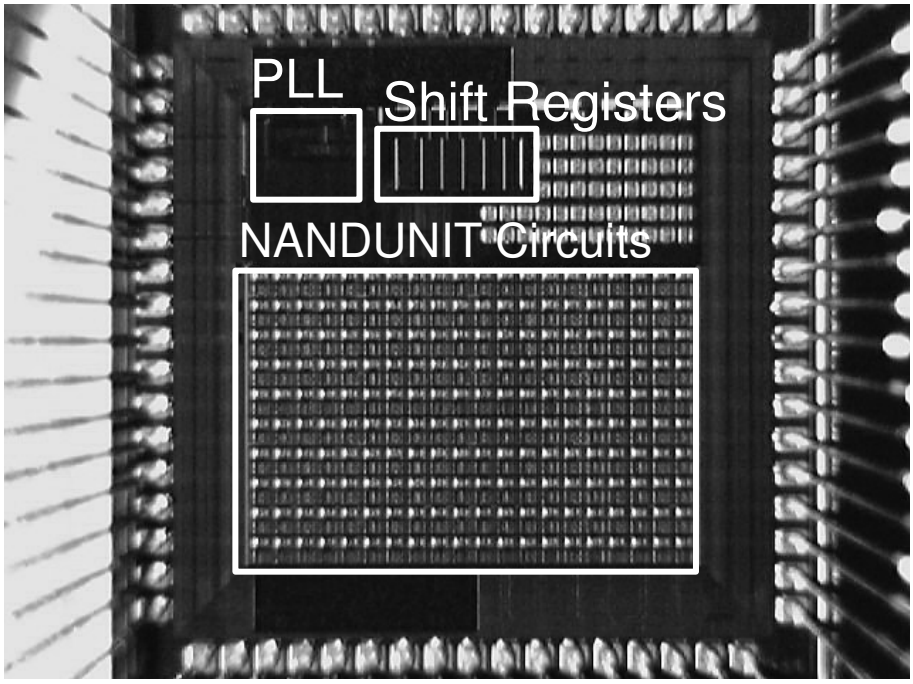

Figure 4.10: Micrograph of fabricated test chip.

signals.

Figure 4.10 is a micrograph of the test chip. The locations of the components, such as PLL, NANDUNIT area, and shift registers are indicated in this micrograph. DC transistor TEGs are placed in the area in the upper right. Measured I-V(Current-Voltage) characteristics of transistors are considered in circuit simulation. Test chip was fabricated in a 90nm six metal layer CMOS technology. The supply voltage of this process is 1.0V.

4.5 Measurement results and discussion

4.5.1 Simulation setup

In our circuit simulation setup, NANDUNIT circuits are replaced by the variable switch model, which enabled us the full-chip simulation. The power/ground wires are carefully modeled as resistance based on the layout pattern. Well junction capacitance is also attached. The inductance of package and bonding are measured and attached between ideal power/ground and chip power/ground pads.

4.5.2 Dependence of gate delay on average voltage drop

In this section, the measurement results demonstrate that our comments in Section 4.2 are correct: the gate delay variation mainly depends on average supply voltage.

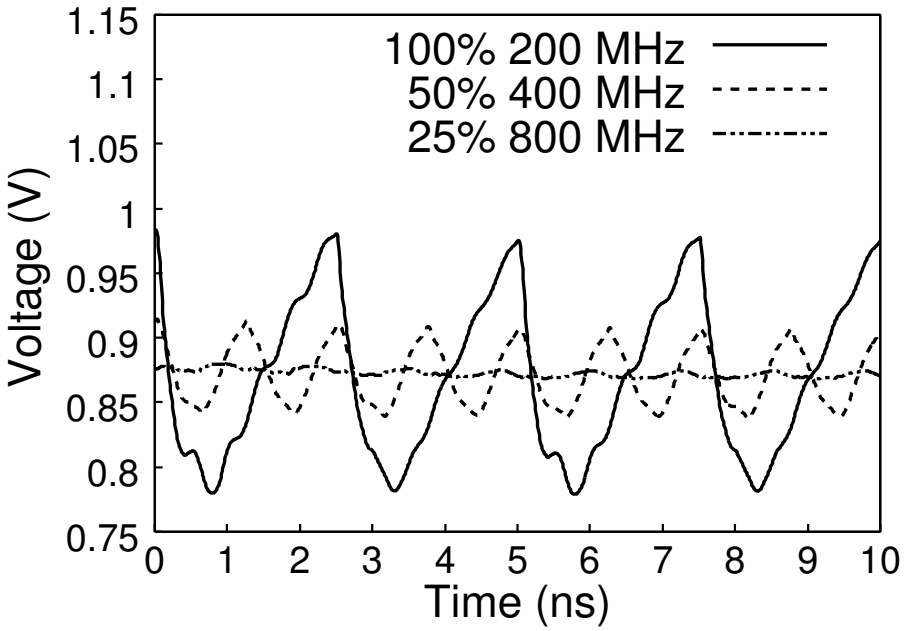

Figure 4.11: Three simulation waveforms whose PLL clock frequency(MHz) $\times$ operating ratio values are equal.

Figure 4.11 shows the noise waveforms in our simulation. The average voltage values of the three waveforms are 0.867V, 0.868V, and 0.870V with 100%, 50%, 25% activity respectively. As can be seen, they are almost equal, even though the noise shapes are different. These waveforms are selected such that the product of PLL clock frequency and the operating ratio of NANDUNITs arrive at the same value. Roughly speaking, as long as the product is identical and the clock distribution is ignored, power consumption stays the same. This is because power consumption is proportional to frequency and the number of active gates. Hence, the averages of the supply voltage are expected to be almost the same as those shown in Fig. 4.11.

T_{noise}/T_{silent} ratio is evaluated; T_{silent} is the ring oscillator cycle when all NANDUNITs are inactive, and T_{noise} is the cycle at the power supply noise caused by NANDUNITs. The ring oscillator cycle is computed from the measured counter value. The cycle time is measured for five times and average of five values are used for discussion. The standard deviation of measurement results is 0.186ps when measurement was operated for 200 times in a same condition, and the reproductivity is adequate.

Figure 4.12 shows plots of T_{noise}/T_{silent} at 100%, 50%, and 25% activity based on measurement results. The x-axis is the product of frequency and activity. When the product is the same, T_{noise}/T_{silent} values are almost the same as it is expected, even though the operating conditions in frequency and activity differ and the peak voltage is estimated to be much different. T_{noise}/T_{silent} value at 100% operating ratio agrees with that of 50% and 25%, and the average error is 4.0%. These measurement results demonstrate that the comments based

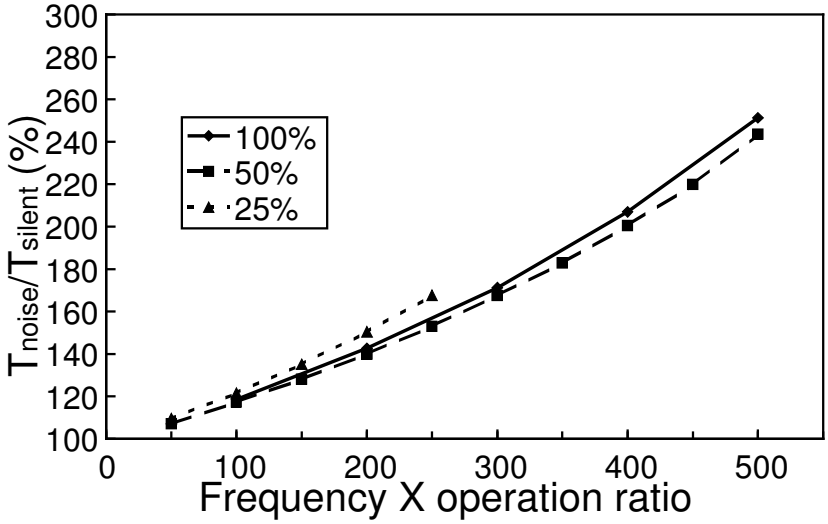

Figure 4.12: Measurement results for T_{noise}/T_{silent} at (9,9). Stage of NANDUNIT is set to 6. X-axis represents PLL clock frequency(MHz) $\times$ operating ratio.

on the simulation in Section 4.2 were accurate, i.e., gate delay strongly depends on average supply voltage, not on the shape of the noise waveform.

4.5.3 Accuracy of simulation model

This section evaluates the appropriateness of the variable switch model in Section 4.3 for power supply noise simulation.

This section compares the average measured voltage drop with the average simulated voltage drop. The measurement results reported in section 4.5.2 indicate that gate delay depends on average voltage drop. This result means that the measured delay increase can be translated into average supply voltage. Oscillation cycles without noise were measured beforehand, varying the supply voltage from 1.0 to 0.5 V in 20 mV steps. These measurements were used for the translation. As for simulation results, the delay increase was first estimated by circuit simulation and then translated into average voltage. In this case, the relation between the oscillation cycle and supply voltage estimated by circuit simulation was used.

Figure 4.13 shows the calculated average voltage drop at (9,9) ring oscillator based on measured and simulated results. In the results shown in Fig. 4.13, the output clock frequency was changed from 100 MHz to 1 GHz, and the ratio of active NANDUNITs was also varied. Simulation results correlate well with measurement results, and the average error is 0.9%. In the range over 600 MHz with 100% activity and over 900 MHz with 50% activity, the counter does not work well due to very high power supply noise, so the results are not plotted in the figure. The good correlation between simulation and measurement results indicates that the simulation model can accurately estimate power supply noise on a real chip.

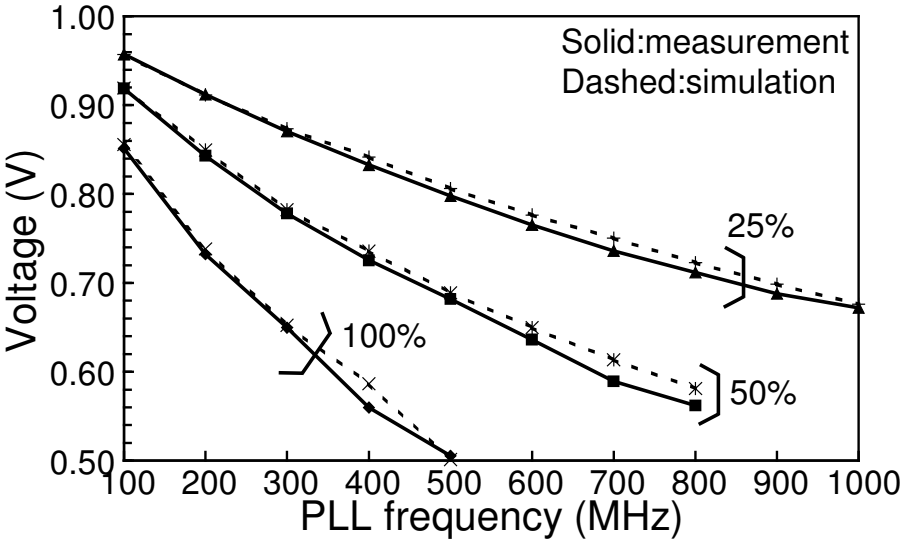

Figure 4.13: Average voltage drop calculated from ring oscillator cycle in measurement and simulation results. 100%/50%/25% of NANDUNITs are uniformly activated by 100MHz-1GHz PLL clock.

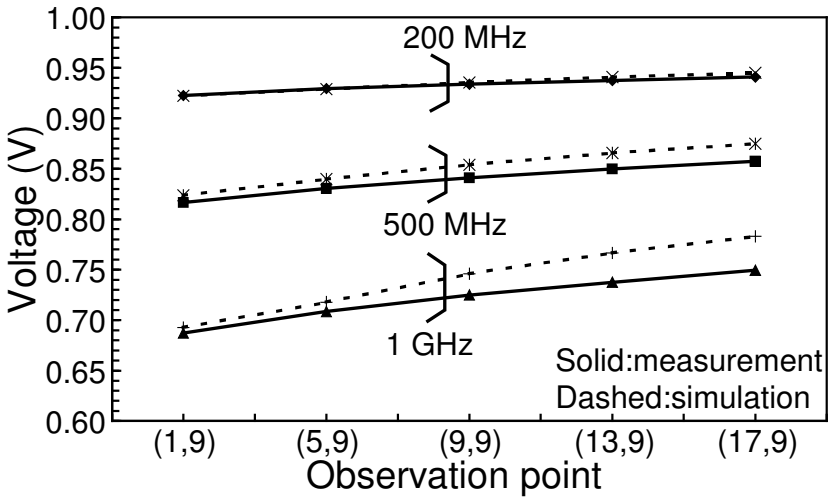

Figure 4.14: Average voltage drop calculated from ring oscillator cycle in measurement and simulation results at (1,9), (5,9), (9,9), (13,9), and (17,9). NANDUNITs in $0 \leq x \leq 3$ area are activated with 200 MHz, 500 MHz, 1 GHz PLL clock.

Spatial distribution of power supply noise is next evaluated. NANDUNITs in $0 \leq x \leq 3$ are operated, and the cycles of the ring oscillators at (1,9), (5,9), (9,9), (13,9), and (17,9) are observed. Figure 4.14 shows the average voltage drop values calculated from the ring oscillator cycles. The simulated voltage drop curves agree well with the measured ones at

all PLL clock frequencies, and the average error is 1.4%. The agreement between simulation and measurement results implies that the spatial distribution of the power supply noise is well reproduced by our circuit simulation.

4.6 Summary

This chapter demonstrated the fidelity of the full-chip circuit simulation model and the dependence of gate delay on average voltage drop based on the measured results.

To conduct a full-chip simulation, a switching current model was developed with capacitance and a variable resistor. This model reproduces the switching current well and reduces simulation time by 94%.

Measurement circuitry was designed to measure the delay degradation caused by power supply noise. The test chip was fabricated in a 90nm CMOS technology. Measurement results agreed well with simulation results, validating the simulation model. Measurement results also demonstrate that gate delay mainly depends on average voltage drop.

Chapter 5

Dynamic Supply Noise Measurement with All Digital Gated Oscillator for Evaluating Decoupling Capacitance Effect

This chapter proposes an all digital measurement circuit called "gated oscillator" for capturing waveforms of dynamic power supply noise [100–102]. The gated oscillator is constructed with standard cells, and thus easily embedded in SoCs. The performance of the gated oscillator is verified with fabricated test chips in a 90nm process. The gated oscillator is suitable for measurement of supply noise distribution, and can be applied for verification of power supply network. In this chapter, characteristics of decoupling capacitance are also discussed focusing on channel length and distance, based on supply noise waveforms measured by the gated oscillator [100, 102].

5.1 Introduction

Power supply noise has become a serious problem in recent processes because of lowered supply voltage and increasing current consumption. Decap (Decoupling capacitance) mitigates dynamic power supply fluctuation [30, 40, 103–105]. However, excessive decoupling capacitance consisting of MOS transistors involves severe gate leakage in advanced technologies [104]. To mitigate the gate leakage problem, efficient decap insertion, that is inserting necessary and sufficient amount of decap to a right place, is highly demanded. Developed decap insertion methods should be verified on silicon in terms of noise suppression efficiency.

For this purpose, a small measurement circuit suitable for embedding in a DUT (Device Under Test) is required. Easiness of circuit and layout design is another important factor to probe any points of interest inside a chip. Comparison of features among the existing measurement circuits are listed in Tab. 5.1. Existing measurement circuits [39–49, 61, 93–95]

Table 5.1: Features of the existing measurement circuits.

	sample & hold	ring osci.	improved ring osci.
waveform	◎	×	○
design	×	◎	○
embedding	△	◎	◎
area		○	○
synchronization with clock	○	×	×

require analog circuit techniques, and need dedicated analog power and bias lines. The additional routing and area costs restrict the number of measurement circuits integrated in a DUT and their allocatable positions. A common ring oscillator measurement such as a Chapter 4, which can be easily implemented, observes not dynamic noise waveform, but averaged supply voltage. Therefore, it cannot be used for evaluation of decoupling capacitance effect.

This chapter proposes an all digital measurement circuit for dynamic noise waveform. Reference [47] proposed a measurement circuit for dynamic noise waveform with only digital circuit components. This circuit, however, has a limitation that DUT operation must synchronize with the clock generated inside the measurement circuit, and an external clock signal can not be given to the DUT. The proposed circuit is also a ring oscillator based circuit, but it accepts any external clock. Features of the proposed circuit are: 1) including only digital standard cells, 2) no need for dedicated analog power supply and reference voltage, 3) small circuit area, and 4) ability to operate with any external clock.

The features are enabled by a new idea that the proposed circuit samples and holds ring oscillator state, whereas conventional circuits sample and hold analog voltage [40, 61]. Implementation of the proposed measurement circuit is very easy because design techniques for analog circuits and dedicated power lines for measurement circuit are not needed. The proposed measurement circuit can be built only with standard cells. Its layout design is compatible with common cell-base design and the size and shape are flexible. As proposed measurement circuit can synchronize with any reference clock, DUT operation frequency is freely changeable.

Several types of TEGs are designed to observe dynamic supply noise waveforms. Measurement results indicate that design of decoupling capacitance influences the peak voltage drop.

This chapter is organized as follows. Section 5.2 explains the proposed measurement circuit and verifies the performance on silicon. Section 5.3 discusses the decoupling capacitance effect based on measurement results. Section 5.4 concludes this paper.

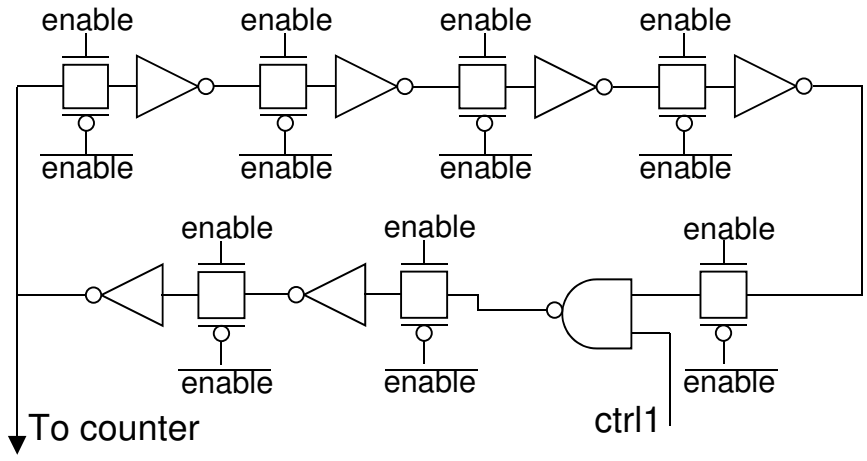

Figure 5.1: Gated oscillator.

5.2 Measurement circuit structure

This section describes the measurement circuit to observe dynamic power supply noise. First, the proposed measurement circuit and the implementation are explained. This section then demonstrates the performance of the measurement circuit with measurement results.

5.2.1 Proposed gated oscillator

Figure 5.1 shows the proposed measurement circuit named “gated oscillator”. The gated oscillator consists of only digital circuit components; inverters, a NAND gate, and transmission gates. Waveforms of dynamic power supply noise can be observed by using the gated oscillator. The gated oscillator is activated during the time period of interest (‘enable’=1), and in the other period (‘enable’=0), the oscillator is frozen by cutting off the transmission line. Conventional circuits sample and hold an analog voltage. However, the proposed circuit runs and holds the ring oscillator operation. Though conventional circuits need analog input/output or analog-to-digital/digital-to-analog converter, the proposed circuit requires only a counter, where the counter is also composed of only digital components.

The operation of the gated oscillator is explained in detail using Fig. 5.2. The gated oscillator operates only while ‘enable’=1, and the oscillating signal is stopped by the transmission gates when ‘enable’=0. Suppose a power supply noise waveform in Fig. 5.2. The cycle count of the oscillator depends on only the power supply voltage while enabled. The supply waveform while ‘enable’=1 is sampled, and the operation of the gated oscillator is hold while ‘enable’=0. The analog voltage of the power supply is translated into the toggle count. Therefore, the gated oscillator can be regarded as a sample and hold circuit with an analog-to-digital converter.

To obtain enough cycle count for accurate measurement, the gated oscillator should be enabled repeatedly at the same timing. It is also needed to measure the cycle count without

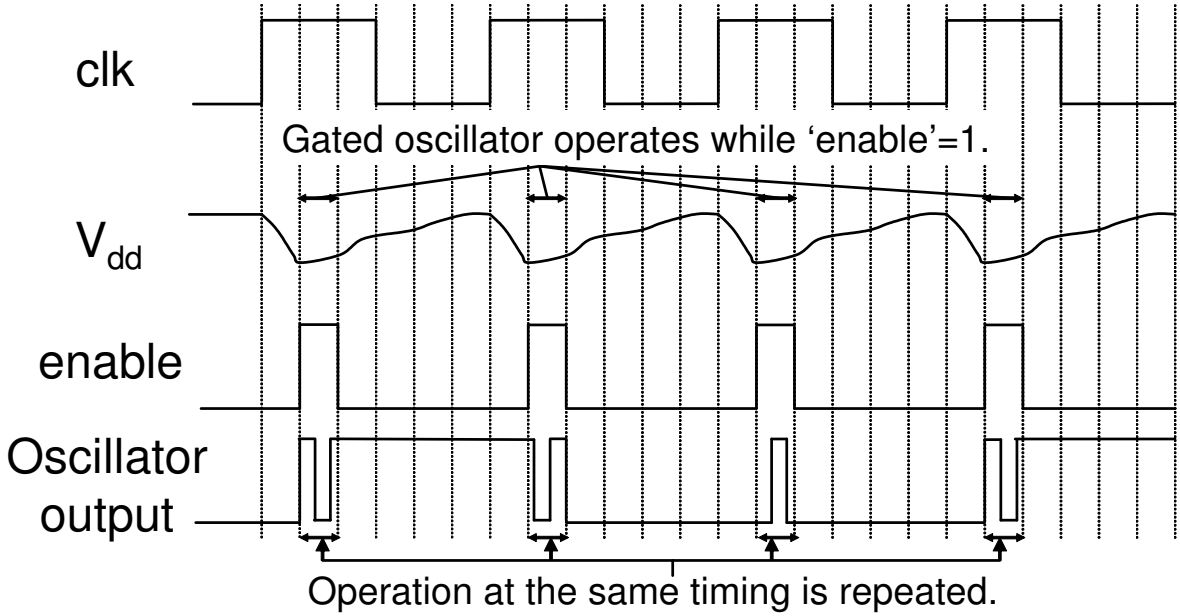

Figure 5.2: Operation of the gated oscillator.

noise varying supply voltage for making a calibration table of voltage vs. cycle count. The sampling timing is swept within a clock cycle and the count is measured at every timing. The voltage is computed from the measured cycle count with the prepared calibration table. And then the dynamic power supply noise is constructed.

An important metric of the measurement circuit is the voltage resolution. In the gated oscillator, the number of transmitting gate while 'enable'=1 is changed by the supply voltage. In addition, the proposed gated oscillator can preserve the intermediate voltage of the transition at the timing when the oscillation is stopped (Fig. 5.3). When 'enable' is set from 1 to 0 while the inverter input is changing from 0 to 1 or 1 to 0, the input voltage is preserved at an intermediate level, whereas rigidly speaking, charge injection through the transmission gate slightly changes the voltage. After 'enable' is restored to 1, the transition restarts from the preserved intermediate level. This intermediate voltage preservation holds the ring oscillator state continuously, which improves the voltage resolution. Figure 5.4 shows the voltage resolution of the gated oscillator evaluated by circuit simulation. X-axis is the stable supply voltage, and Y-axis is the cycle count of the gated oscillator normalized by the count at 1.0V. The period and number of 'enable'=1 are 300ps and 250, respectively. The count increases linearly. The gated oscillator is expected to have a fine resolution of 20mV.

5.2.2 Implementation of measurement circuit

A test chip was fabricated in a 90nm CMOS process. The nominal supply voltage of this process is 1.0V. Figure 5.5 is the micrograph of the test chip. The test chip includes several TEGs, a PLL, and shift registers. The shift registers are written and read by external input

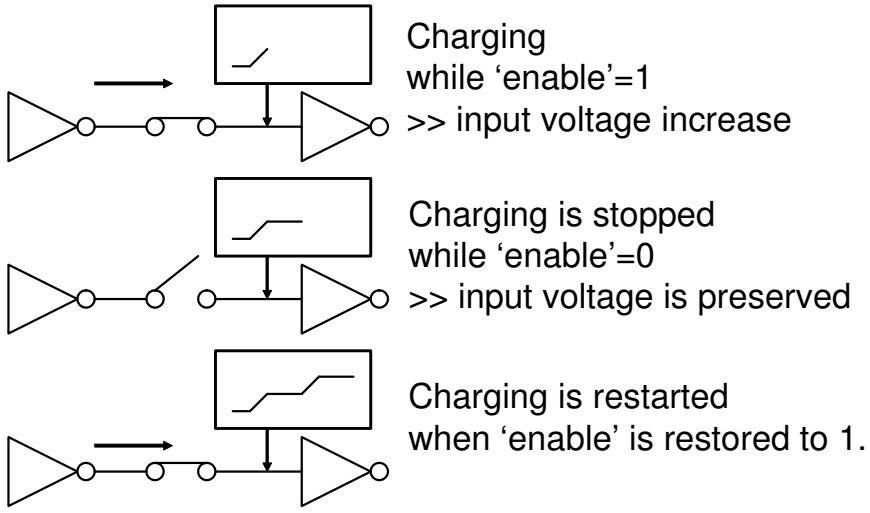

Figure 5.3: Intermediate voltage preservation of gated oscillator.

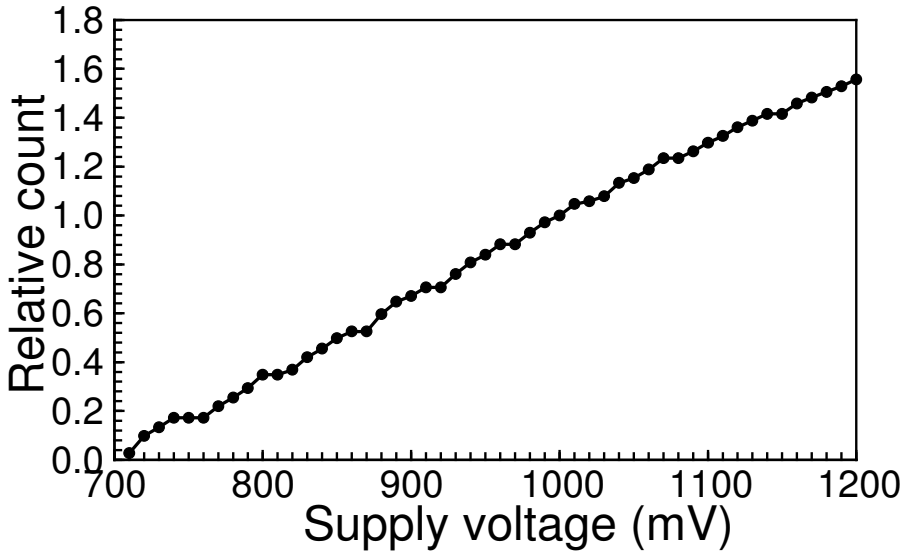

Figure 5.4: Calibration table of gated oscillator in simulation.

and output. Control signals of TEGs and PLL are stored in the shift registers. A part of the shift register also operates as a counter, and counts the toggle of the gated oscillator.

Each TEG includes a DUT and a measurement circuit. The measurement circuit consists of the gated oscillator, and circuits for 'enable' signal generation. 'enable' signal of the gated oscillator should be synchronized with DUT operation clock. A designed 'enable' signal generator in Fig. 5.6 consists of variable delay, XOR gate, AND gates, and a multiplexer. This generator varies the pulse width and timing of 'enable' signal by controlling the variable

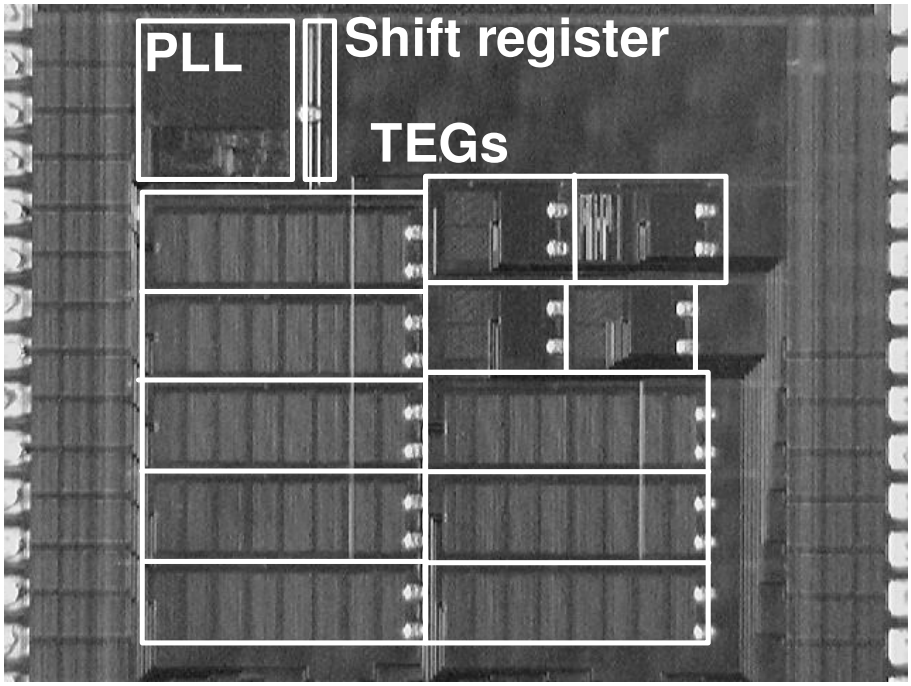

Figure 5.5: Micrograph of the test chip.

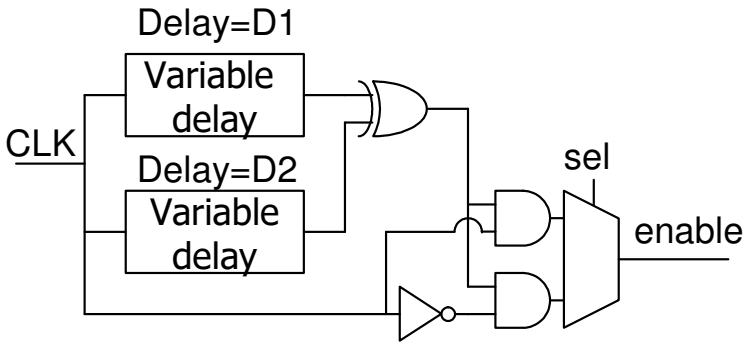

Figure 5.6: Circuit for 'enable' signal generation.

delay circuits. The generated pulse width is $|D1 - D2|$, where $D1$, $D2$ are the delays of variable delay circuits. The pulse timing of 'enable' from 'CLK' edge is changed from $\min(D1, D2)$ to $\max(D1, D2)$. The reference edge of 'CLK' is chosen from rise and fall transition by 'sel' signal. This work adopted variable delay circuit of Fig. 5.7, which consists of buffers and multiplexers. $D1$ and $D2$ vary from 0- to 255-stage buffer delay.

DUT includes switching circuits for noise generation, power supply line, and decoupling capacitance. The circuit for noise generation consists of 12-stage NAND gates. 64×8 cells of 12-stage NAND gates are placed in each TEG. The gated oscillator shares the power

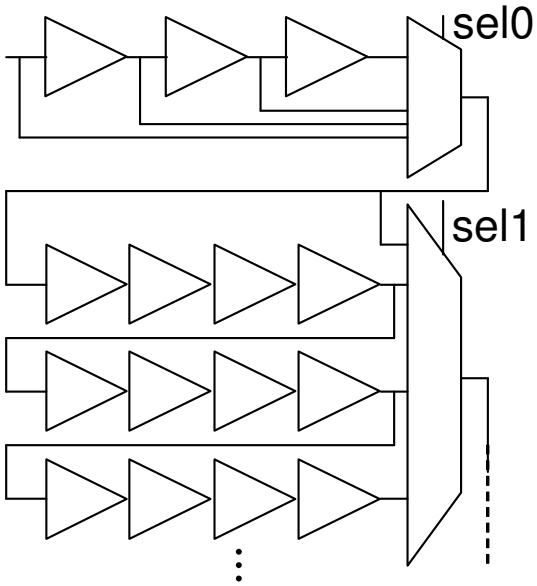

Figure 5.7: Variable delay circuit.

supply line with the noise generator inside a TEG. Each DUT has a dedicated external power supply respectively, and the substrate of each DUT area is isolated by triple-well. External power of each DUT is supplied through one power and ground pair of bonding wires, and package inductance causes dI/dt drop.

The layout size of the gated oscillator is 11.76μm$\times$ 15.12μm, and comparable to the other analog measurement circuits [40,41]. In this work, 4X inverters and transmission gates are used to suppress random process variation. Otherwise, the layout size can be shrunk to roughly one-fourth. The gated oscillator consists of only digital standard cells, which yields layout flexibility and process portability.

5.2.3 Evaluation of proposed measurement circuit

This section evaluates the measurement precision and reproducibility of the proposed gated oscillator based on measurement results. The fabricated test chip was mounted on a QFP package. The external control signals are generated with a pattern generator, and the output signals, which includes the gated oscillator counts, are observed with a logic analyzer. Figure 5.8 shows the measured cycle count of the gated oscillator without noise generation. The pulse width of 'enable' signal is 10-stage buffer delay. The voltage resolution of the gated oscillator is estimated to be 10-20mV below 1.0V, and is sufficient for measurement.

A noise waveform was measured for 1000 times to evaluate the reproductivity. The maximum standard deviation at 10 timing points is 0.98%, and the gated oscillator has fine reproductivity.

Fig. 5.9 compares the voltage resolution varying the pulse width of 'enable' signal. The

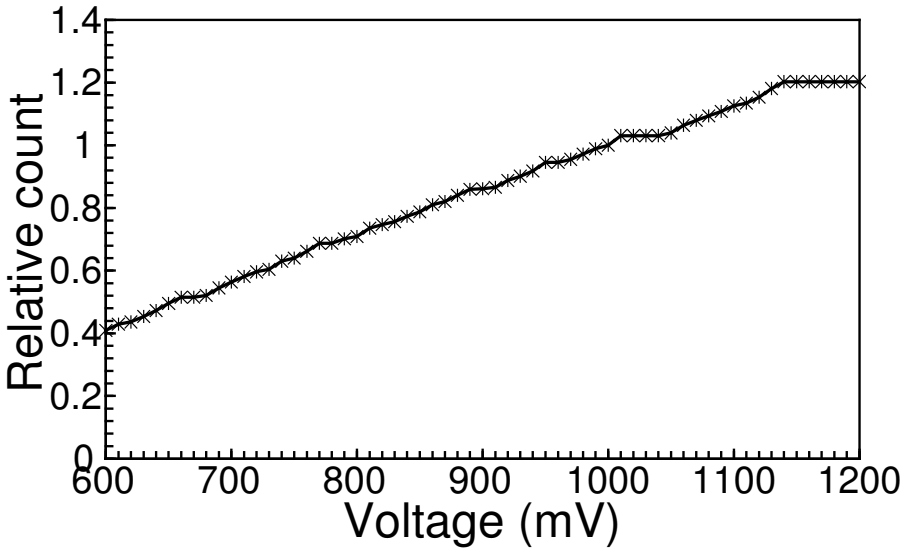

Figure 5.8: Calibration result of the gated oscillator.

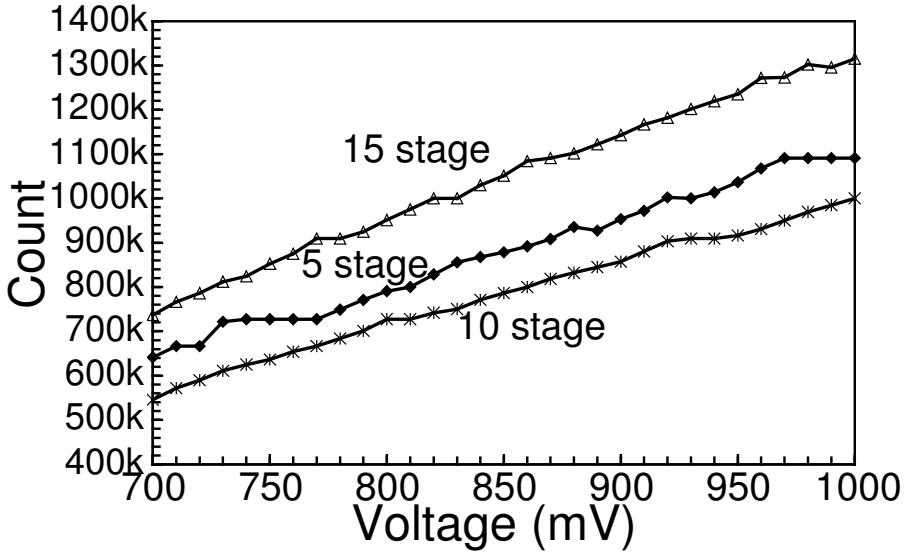

Figure 5.9: Comparison results of calibration results. Timing widths of 'enable' pulse are set to 5, 10, 15 buffer stages.

number of 'enable' pulse whose width is 5-stage buffer delay is 4 million, and in other cases 2 million. The voltage resolutions of 10- and 15-stage pulse width are better and their resolutions are roughly 10mV. In the rest of this chapter, 'enable' signal of which width is 10-stage buffer delay is used. To obtain the actual delay values of variable delay circuits for enable signal generation, $D1$ and $D2$, the ring oscillator circuits were embedded in 'enable' tim-

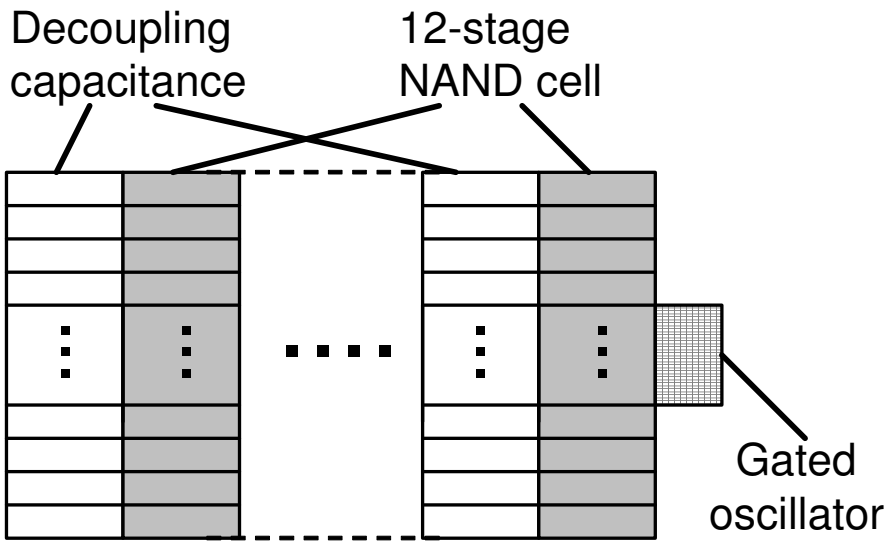

Figure 5.10: Structure of DUT for TEG A-D.

ing generation circuit. The ring oscillator was implemented for each variable delay circuit, and the delay uncertainty due to process variation is also measured. The buffer delays were measured using ring oscillators, and the 10-stage buffer delay is about 300ps-450ps which corresponds to 2-3G sample/s.

5.3 Discussion about decoupling capacitance

This section discusses the effect of decoupling capacitance focusing on the channel length and the resistance between operating circuit and capacitors. The structure of DUT in each TEG is shown in Figures 5.10 and 5.11, and TEG variation is summarized in Table 5.2. The channel length of decoupling capacitance is changed so that the area or the total capacitance becomes unchanged (TEG B-D). The resistance to decoupling capacitance is varied in TEG E and F. One pair of bonding wires supply the power to each TEG and package inductance can cause dI/dt drop on DUT. The resistance load with 250μm length, 1μm width and 0.3μm thickness wire is attached between each power supply line of TEG A-D and pads to suppress dI/dt noise. IR drop dominates the dI/dt drop and DUTs are protected from overshoot due to dI/dt drop. To observe more sensitive change of waveform due to decoupling capacitance, resistance load is not attached to TEG E and F. The cycle of the gated oscillator is measured for five times in the same condition and the average of five values are used for voltage computation. The pulse of the gated oscillator is counted for 20ms, and 'enable' signal is generated every 10ns.

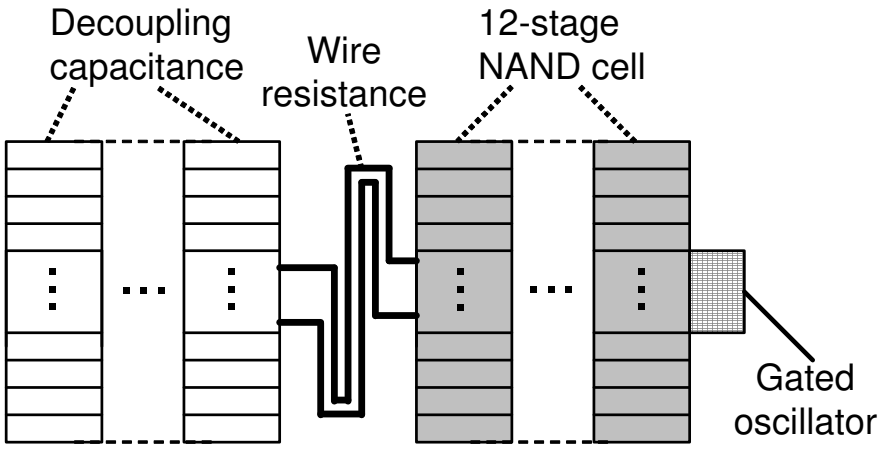

Figure 5.11: Structure of DUT for TEG E and F.

Table 5.2: TEG variation.

TEG	Decap ch. length	Note
A	-	No decap
B1	0.1μm	Decap capacitance is same as TEG C.
B2	0.1μm	Decap area is same as TEG C.
C	1μm	86.6pF
D1	5.98μm	Decap capacitance is same as TEG C.
D2	5.98μm	Decap area is same as TEG C.
E	1μm	Wire R is 1.7Ω. Decap is same as TEG C.
F	1μm	Wire R is 26.7Ω. Decap is same as TEG C.

5.3.1 Effect of decoupling capacitance

This section first compares the noise waveform between TEG without decoupling capacitance (TEG A) and TEG with enough decoupling capacitance (TEG B1) in Fig. 5.12. The minimum supply voltages of TEG A and B1 are 730mV and 800mV. Decoupling capacitance reduces the voltage drop by 70mV.

5.3.2 Channel length of decoupling capacitance

This section next discusses the L (channel length) of decoupling capacitance. Figure 5.13 compares the noises in TEG B1 (L=0.1μm), TEG C (L=1μm), and TEG D1 (L=5.98μm). Total capacitance values of decoupling capacitors in three TEGs are almost equal. The peak voltage drop of TEG D1 is 20mV larger than those of other TEGs, which indicates that long

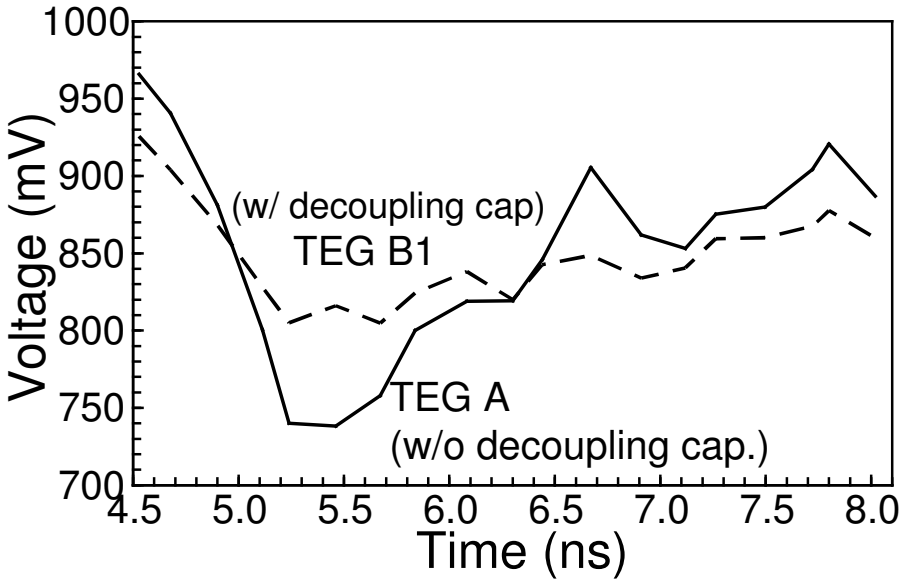

Figure 5.12: Measurement results of TEGs w/ and w/o decap (B1, A).

channel length degrades RC time constant of decoupling capacitance. On the other hand, the peak voltage drop of TEG B1 and C are almost the same, though the channel length is different. RC time constant of L=1μm decap seems to be small enough for noise suppression in this case.

Next the decap area is kept unchanged for different channel lengths, and compare the noises (Fig. 5.14). Generally, larger capacitance can be integrated in the same area by using longer channel transistors. The ratio of total capacitance among TEGs is about B2:C:D2 = $2 : 6 : 9$. The peak voltage drop of TEG B2 is larger because of small total capacitance. On the other hand, the quite similar result is observed in TEG C and D2. Though TEG D2 has 1.5 times larger capacitance than TEG C, the voltage drop did not decrease because of poor RC time constant.

This measurement result confirms that using decoupling capacitance with appropriate channel length can improve the area efficiency without degrading noise suppression effect. On the other hand, when channel length is too large, the performance of decoupling capacitor deteriorates.

5.3.3 Resistance between operating circuit and decoupling capacitance

Figure 5.15 compares the measured supply noise waveforms of TEGs E and F. The resistance difference between operating circuit and decoupling capacitance (1.7Ω and 26.7Ω) corresponds to the distance difference from decoupling capacitance in actual designs (16μm and 250μm). The difference of peak voltage drop between two TEGs is about 80mV. Measurement results have confirmed that wire resistance degrades RC time constant of decoupling

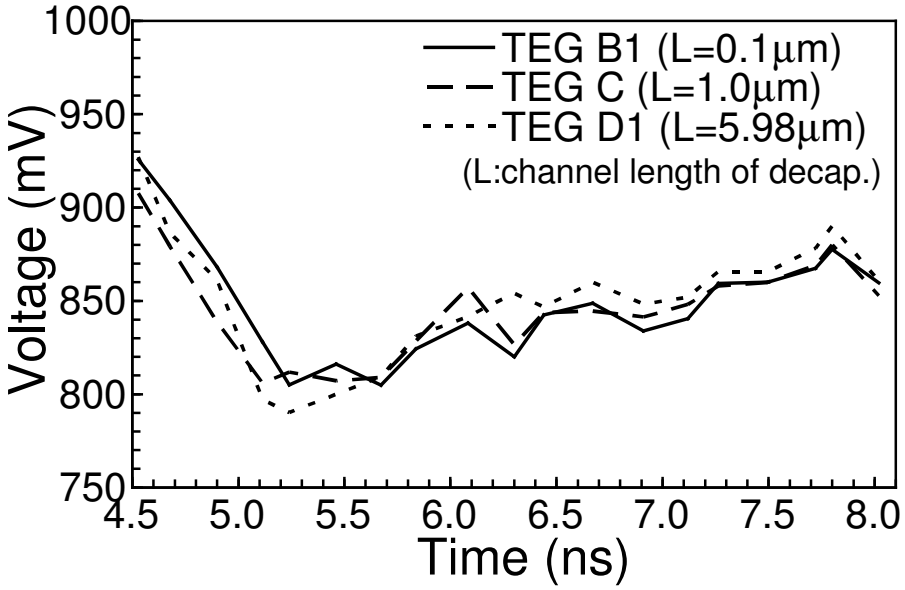

Figure 5.13: Measurements results of TEGs with 0.1(B1)/1(C)/5.98(D1)μm channel length decoupling capacitance. Total capacitance of decoupling capacitance is almost equal.

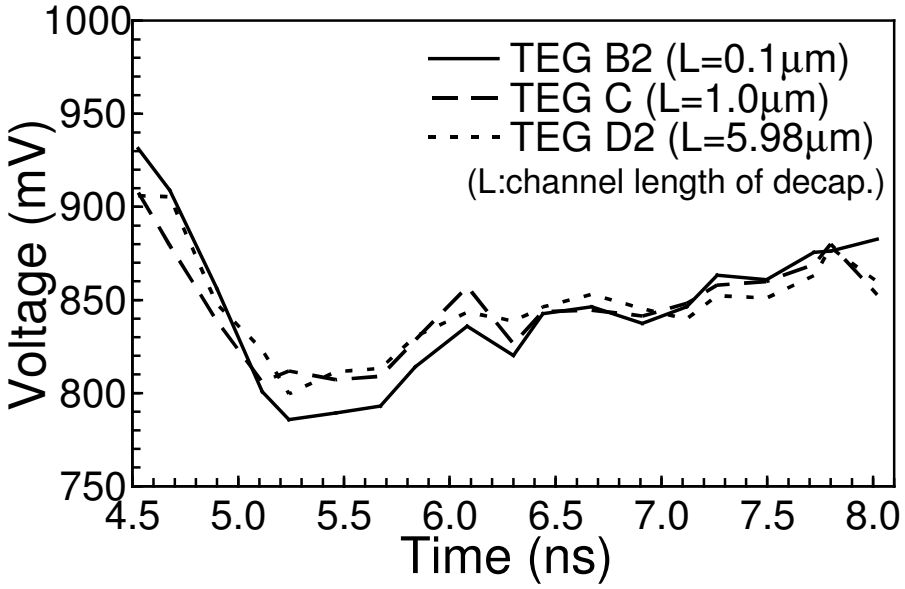

Figure 5.14: Measurements results of TEGs with 0.1(B2)/1(C)/5.98(D2)μm channel length decoupling capacitance. The area of the capacitors is equal.

capacitance and noise suppression effect. The resistance/distance from decoupling capacitance should be carefully examined to avoid unexpected large noise.

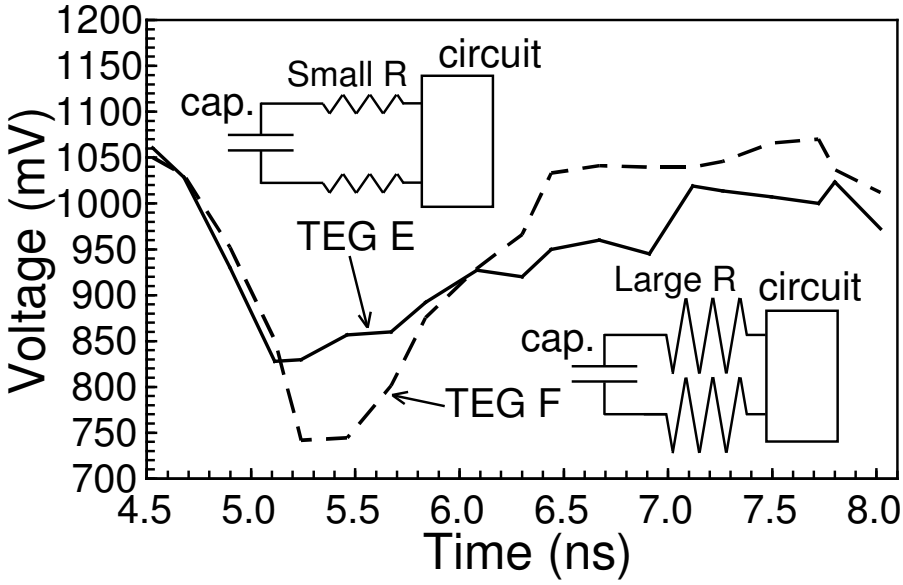

Figure 5.15: Measurements results of TEGs E and F. The wire resistances between operating circuit and decoupling capacitance of TEGs E and F are 1.7 and 26.7Ω respectively.

5.4 Summary

This chapter proposed the gated oscillator that captures dynamic supply noise waveform. The proposed gated oscillator holds the state of the ring oscillator instead of analog voltage. The noise waveform is reproduced from the measured cycle of ring oscillator. The gated oscillator consists of digital standard cells only, and does not require analog circuits dedicated power lines, and reference voltage. Measured voltage value with this circuit is digital counter value, and can be easily observed or fed back to the operating circuit by implementing adequate test mode since the gated oscillator requires the repetitive circuit operation. The voltage resolution and reproductivity of the proposed circuit were confirmed on the test chip fabricated in a 90nm CMOS process.

The characteristics of decoupling capacitance are evaluated with the gated oscillator. The measurement results indicated that the channel length of decoupling capacitance had a tradeoff between area and response, and appropriate channel length could improve area efficiency without response degradation. There were also observation that the resistance between decoupling capacitance and operating circuit deteriorated the effect of decoupling capacitance.

Chapter 6

Conclusion

The performance of VLSI has become sensitive to signal and power integrity in nano-meter technology. Consideration of signal and power supply noises is essential for current VLSI design. This thesis verifies modeling methods, impacts, and reduction techniques of signal and power supply noises with experimental results on silicon. Verification in this thesis contributes to accurate delay estimation methodologies considering crosstalk and power supply noises, and reduction techniques for crosstalk and power supply noises. These are indispensable for successful nano-scale VLSI design satisfying power, area and speed requirements.

In Chapter 2, inductive coupling noise is measured in a 90nm process, and it is confirmed that inductive coupling is a current design issue. Simulation results with R(f)L(f)C and RLC distributed constant models follow the measurement result, and appropriateness of these models are demonstrated. Measurement results also showed the effectiveness of noise reduction techniques, such as narrowing wire, inserting power supply lines, and decreasing driver size. Long-range effects and noise superposition are discussed based on measurement results, and delay variation due to inductive coupling noise caused by multiple aggressors can be approximated by summation of delay variation caused by each individual aggressor. This chapter provides silicon-proofed estimation and reduction methods of inductive coupling effect, which contributes to a high performance bus interconnect design.

Chapter 3 predicts the impact of capacitive and inductive coupling noises in future fabrication processes. Supposing a practical bus interconnects, both capacitive and inductive coupling noises simultaneously caused by aggressors is evaluated. The prediction result shows that capacitive coupling noise becomes more important than inductive coupling noise when interconnect parameters shrink in future technology. On the other hand, inductive coupling noise is predicted to be more significant than capacitive coupling noise when the interconnect parameters do not shrink to maintain the performance of signal propagation in advanced processes. This chapter explained the importance of coupling noises in future process, and reveals that inductive coupling can be eliminated in high performance bus design by adjusting interconnect size with small delay increase.

Chapter 4 evaluates a full-chip simulation method and delay dependence on average power supply drop based on measurement results. A variable switch model is constructed, and characterization of the model is presented. The simulation period of full-chip simulation

is reduced to 6% by using the variable switch model. The accuracy of the model is validated by comparison between full-chip simulation results and measurement results of power supply noise on a test chip. The measurement results show that the similar delay variations are caused by the supply noise waveforms which have the same average drop even if their waveform shapes and peak drops are different. The full-chip simulation method and delay dependence on average voltage drop help designers to estimate the impact of power supply noise effectively, and to achieve required circuit performance with smaller area, interconnect, power, and design costs under serious power supply noise.

Chapter 5 proposes a measurement circuit for dynamic waveform of power supply noise, and discusses the characteristics of decoupling capacitance. The proposed circuit called gated oscillator circuit includes only digital circuit components, and is compatible with cell-based design. The operation of the gated oscillator is confirmed on a test chip. The voltage resolution and sampling rate of the gated oscillator on a fabricated chip is 10-20mV and 2-3G samples per second. The measurement results of supply waveform with the gated oscillator clarified that the channel length of decoupling capacitance has a tradeoff between amount of capacitance and RC response, and that shorter distance between decoupling capacitance and operating circuit is more efficient. The proposed circuit brings designers an easy monitoring and diagnosis method of the power distribution network. This chapter contributes to improving the design of power supply network.

The future work includes discussion on effective supply noise reduction techniques, performance improvement of the gated oscillator by customizing physical layout of standard cells, and verification of power distribution network on the SoC.

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