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博士の専攻分野の名称	博 士（工 学）
学位記番号	第 ２２１１０ 号
学位授与年月日	平成 20 年 3 月 25 日
学位授与の要件	学位規則第４条第１項該当 基礎工学研究科システム創成専攻
学位論文名	Study of Field Effect Transistor Memory Based on Ferroelectric-Insulator Interface Conduction （強誘電体-絶縁体界面伝導を用いた FET メモリに関する研究）
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論 文 内 容 の 要 旨

A new type of FET memory based on ferroelectric-insulator interface conduction has been proposed. This FET has two kinds of structure such as metal-insulator-ferroelectric-metal (MIFM) and metal-ferroelectric-insulator-metal (silicon) (MFIM(S)). This FET consists of source and drain electrodes between ferroelectric ($Pb(Zr_{0.52}, Ti_{0.48})O_3$ (PZT), $SrBi_2Ta_2O_9$ (SBT)), insulator (HfO_2, SiO_2, SiON), and top- and back-gate. Drain current flows along the interface between ferroelectric and insulator layers and need no semiconductor.

In theoretical consideration, the polarization (electric flux density) of ferroelectric was calculated by using the Miller's empirical formula. Voltage distribution applied to ferroelectric and insulator layer was calculated, and the ferroelectric-insulator interface conduction FET can be considered to operate at low voltage. However, the carrier injection to ferroelectric-insulator interface is assumed and calculated, and it can be considered to operate about 5 V. Using the MIS-FET theory, I_D-V_G characteristics of the ferroelectric-insulator interface conduction FET was calculated. ON current increases with increasing the film thickness of ferroelectric. Memory window is enlarged with increase of the insulator thickness. When the insulator dielectric constant is large, ON current become to be large.

Firstly, an interface conduction FET with the MIFM structure was fabricated and its characteristics were investigated. Moreover we have attempted to improve the characteristics. In a Pt/HfO_2/PZT/Pt structure interface conduction FET using a PZT with large remanent polarization and a HfO_2 with high dielectric constant, the characteristics of I_D-V_G and I_D-V_D are similar to conventional MIS-FET, and main carrier is a hole. OFF state current is very small as below 10^{-10} A. Maximum ON/OFF current ratio is about 5×10^5. In order to increase the ON current, a Pt/HfO_2/epitaxial PZT/Pt/MgO structure interface conduction FET in which epitaxial PZT is used. Because, it is thought that remanent polarization of epitaxial PZT is larger than that of randomly orientated films. Maximum ON/OFF current ratio is about 3×10^4. ON/OFF memory current ratio is 3×10^2. However, the grown PZT is not oriented in the direction of perfect c-axis on Pt/MgO substrate and the leakage

current is large. In order to decrease leakage current, interface conduction FET was fabricated as Pt/SiO_2/PZT/Pt structure with smooth surface of PZT by mechanical milling. The leakage current can be decreased. However, the FET characteristics cannot be improved because the PZT surface received damage in the milling. As another method to decrease the leakage, interface conduction FET is fabricated as Pt/HfO_2/PZT/Pt structure with oxidation layer of S/D electrode (Ti). The leakage current can be decreased, however, the FET characteristics cannot be improved because the PZT surface received some damages. In order to make perfectly polarization inversion, interface conduction FET is fabricated as Pt/HfO_2/SBT/Pt structure. Maximum ON/OFF current ratio is about 1×10^4. ON/OFF memory current ratio is 1×10^2. However, the leakage current is large.

The other structure, an interface conduction FET with the MFIM(S) structure was fabricated and its characteristics was investigated. Moreover, we have attempted to improve the characteristics. The leakage current decreased in Pt/SBT/SiO_2/Pt structure interface conduction FET, but the transistor property was not obtained because the leakage current of SiO_2 insulator layer was much increased after annealing of SBT. In a Pt/SBT/SiON･SiO_2/Si interface conduction FET using a thermal oxidation insulator layer with a good thermal stability, the characteristics of I_D-V_G and I_D-V_D are similar to conventional MIS-FET and main carrier is a hole. Maximum ON/OFF drain current ration is about 5×10^4. In ON state, the drain current is almost equal to I_S and leakage current from top-gate and back-gate is small enough in comparison with drain and source current. Therefore, the drain current can be considered to flow at interface between ferroelectric and insulator layer. The drain current has linear dependence to W/L along with conventional MOS-FET. Increase of the thickness of insulator increased the width of the memory window which is consistent with the calculation.

論文審査の結果の要旨

近年急速に発展してきているインターネット、携帯電話、マルチメディア等の情報技術を支える電子装置の中で、電源を切っても記憶がなくならない不揮発性メモリは非常に重要なものである。強誘電体薄膜ゲート FET が非破壊読み出し可能な次世代超高集積化不揮発性メモリとして期待されているが、記憶保持特性が短い。

こういった背景の中で、申請者は強誘電体表面に分極を終端する自由キャリアが表面上を動くことに注目し、強誘電体-絶縁体界面の電流として利用した界面伝導トランジスタを提案した。本素子は、通常の FET でキャリア輸送に用いている半導体を必要としない大きな特徴を持ち、金属、絶縁体、有機物、ガラス等のあらゆる種類の材料の上に作り込めるという画期的なメモリとなる。申請者はこの新規素子の動作について理論的解析から、デバイスの作製と評価についての実験を行った。

まず理論的には、強誘電体の分極ヒステリシスに応じて生じる電荷による界面伝導電流を求め、従来の強誘電体メモリ FET とは異なり、絶縁体膜厚によりメモリウィンドウが制御できることを示した。実験的には、まず強誘電体として PZT（$PbZr_x$-$Ti_{1-x}O_3$）膜と SBT（$SrBi_2Ta_2O_7$）膜、絶縁体として HfO_2 膜、SiON 膜、SiO_2 膜を用いて、様々な組み合わせ構造の FET メモリの試作を行った。M（金属)/HfO_2/PZT/M 構造 FET では、ON/OFF 電流比 5.5 桁、メモリの ON/OFF 電流比 3.5 桁を得た。また M/SBT/SiON/Si 構造 FET では、ドレイン電流が安定で、リーグ電流も小さくなり、明確な特性を得ることができた。このような新構造素子により、界面電流の強誘電体分極による制御とメモリ効果を確認できた。

以上述べたように、本論分は強誘電体-絶縁体界面伝導を用いたメモリ FET につき、特性解析から素子の試作・評価にわたる一連の重要な成果を得ており、学位（工学）論文として価値があるものと認める。