

Title	Study on Bias-temperature Instability in 4H-SiC Metal-oxide-semiconductor Devices
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Osaka University

## Abstract of Thesis

Name ( Atthawut Chanthaphan )	
Title	Study on bias-temperature instability in 4H-SiC metal-oxide-semiconductor devices (4H-SiC MOSデバイスのバイアス温度不安定性に関する研究)
<p>Power electronics are an enabling technology practically used in various applications, e.g. energy production, electricity generation and transmission system, electric/hybrid automotive, electronics and IT appliances. The essential role of power electronics is that they are responsible for regulating the energy flow and converting from sources up to loads. The most concerned topic among societies is that the systems should operate very accurately with high power rating and reduced energy loss. The most important components in every power electronic systems are “power devices”. In 1950s, the first power devices made from semiconductor were firstly introduced to replace vacuum tubes, the traditional power devices. Since then, the power devices, i.e. power diodes and power transistors have taken an important role with “silicon (Si)” serving as the base semiconductor material. However, the development of these “classical” power devices has faced the inevitable obstacles due to physical properties of Si. Therefore, “silicon carbide (SiC)” has recently become a novel semiconductor for realizing next generation power devices. Because of its superior physical characteristics over Si, the SiC power devices can operate in a higher power (&gt; 1 MW) and higher temperature (&gt;300°C) regimes.</p> <p>Nowadays, SiC-based Schottky barrier diodes (SBDs) have already been commercialized with enhanced blocking voltage and reduced leakage current. Power metal-oxide-semiconductor field-effect-transistor (MOSFET) is another type of power devices that have thoughtfully developed in parallel with the SiC-SBDs. The most attractive key factor for realizing SiC-based power MOSFETs is that the thermal oxidation process for producing silicon dioxide (SiO<sub>2</sub>) as the gate insulator can be adopted from the Si technology. A direction of current flows in the power MOSFETs is vertical, and they are commonly produced of “thick drift region” to suppress an enormous electric field. The breakdown field of SiC is 8~10 times higher than that of Si makes the SiC-MOSFETs to handle higher electric fields with reduction in drift region thickness. However, a channel mobility of SiC-MOSFETs is drastically affected by a lot of carbon-related defects in the thermal SiO<sub>2</sub> and at SiO<sub>2</sub>/SiC interfaces. Many techniques have been proposed to reduce the amount of interface trap density, e.g. post-oxidation annealing (POA) in particular gas ambience, i.e. nitric oxides (NO<sub>x</sub>) and hydrogen (H<sub>2</sub>).</p> <p>Most work so far of power SiC-MOSFETs has focused on the increase of mobility in which carbon impurities and other related defects in bulk SiO<sub>2</sub> and at SiO<sub>2</sub>/SiC interfaces play crucial roles on this issue. Many interface passivation methods were introduced to solve this problem. Besides, considering beyond the interface quality, reliability of the SiC devices regarding dielectric breakdown of the gate oxides have become important topics. In order to control the power electronics in the fail-safe applications, it is not allowed that the power devices degrade the performance during operation lifetime of the system. In the field of Si research, threshold voltage (V<sub>TH</sub>) shift induced by carrier injection into the oxides during bias stressing at high temperatures, so-called bias-temperature instability (BTI), has been discussed as the determining factor in reliability of modern Si-based integrated circuits. In addition, mobile ions in gate oxides, such as sodium (Na<sup>+</sup>) and potassium (K<sup>+</sup>) ions, are known to be distinctive origins of the V<sub>TH</sub> instability. The mobile ions are unpredictable and difficult to guess, because these ions diffuse inside the oxide following different circumstances of gate biases and temperatures. Depending on the total number of mobile ions, the V<sub>TH</sub> fluctuation can be wherever from few volts to tens of volts, which may change the device characteristics from “normally-off” to “normally-on”, or vice versa. For many years in the Si-MOS device fabrication, a countermeasure has already been well established against these ionic contaminations by using clean apparatuses, high purity quartz and metals for every processing. Furthermore, the development of fabrication methods respectively for the prevention and removal of mobile ions has been proposed.</p> <p>Although distinct ion-drift phenomena attributable to positive ions have been observed in SiC-MOS devices by</p>	

several groups, they are not yet deeply understood. This is because the correlation between BTI behavior and procedures for gate oxide formation on SiC substrates has not been examined and, even worse, details of the procedures were undisclosed in some literature. The main purpose of my study is to provide the different aspects for better understanding of BTI in SiC-MOS devices. Later, the method to solve BTI was demonstrated based on pioneering mobile ion elimination technique proposed to improve BTI characteristics. Lastly, high-permittivity (high- $k$ ) gate dielectrics used for the advanced SiC-MOS devices were also examined for better performance and electrical stability. This doctoral dissertation is summarized as follows.

In Chapter 2, the fundamental aspects of SiC oxidation were systematically described in order to clarify the physical origin of the electrical degradation of the SiO<sub>2</sub>/SiC interface. Synchrotron radiation x-ray photoelectron spectroscopy (SR-XPS) analysis revealed a near-perfect interface dominated by Si-O bonds, and it was found that atomic scale roughness and imperfection is introduced as oxide thickness increases. These results show that a thick transition layer is ruled out as a cause of electrical degradation and that the elimination of atomistic defects just at the interface and beneath the SiC substrate must be focused on in order to obtain a guideline for future SiC-based devices. This high-resolution XPS study also examines the modulation of energy band alignment between thermally grown SiO<sub>2</sub> layer and 4H-SiC due to post oxidation treatments. Although the hydrogen incorporation into the SiO<sub>2</sub>/SiC interface is effective in improving the interface property, the SR-XPS analysis showed that interface defect passivation induces a reduction of the conduction band offset.

In Chapter 3, studies on BTIs in 4H-SiC MOS capacitors revealed the unusual generation of positive mobile ions in thermal oxides that could be considered as an intrinsic phenomenon in 4H-SiC MOS devices with thermally grown oxides. Charge injection into the electrical traps at/near SiO<sub>2</sub>/SiC interfaces causes BTI typically characterized by a clockwise hysteresis in bidirectional capacitance-voltage (C-V) curves of SiC-MOS capacitors. Forming gas annealing (FGA), POA in diluted H<sub>2</sub> ambient is beneficial in reducing the clockwise C-V hysteresis due to electron injection at room temperature. However, the hysteresis was changed to counter-clockwise at 200°C only for the SiC-MOS capacitors with FGA, indicating the positively charged mobile ion drift. The magnitudes of C-V hysteresis due to mobile ion drift at high-temperature were found to depend on FGA temperatures. The results were also compared with Si-MOS capacitors, but this C-V hysteresis due to mobile ions was not observed in any fabricated Si-MOS capacitor. Thus, common ion contaminations (*i.e.* Na<sup>+</sup>, K<sup>+</sup>) are ruled out to indicate an intrinsic problem of SiC.

In Chapter 4, in order to obtain mobile ion-free SiC-MOS capacitors, the mobile ion removal was proposed based on the negative bias-temperature stress (NBTS). Constant negative gate voltage (V<sub>G</sub>) was applied at typical high-temperature to move all mobile ions to accumulate at the uppermost SiO<sub>2</sub> surface and then perform subsequent etching of a few nm-thick SiO<sub>2</sub> to eliminate the mobile ions. In this time, bidirectional C-V curves of the NBTS sample measured at both room and high temperatures overlap each other without hysteresis. It can be concluded that mobile ions were removed completely while maintaining the excellent interface property attributed to FGA. In addition to NBTS sample, the positive bias-temperature stress (PBTS) with negative V<sub>G</sub> was also applied at the same temperatures to accumulate mobile ions at the bottom SiO<sub>2</sub>/SiC interface with an areal density of several 10<sup>12</sup> cm<sup>-2</sup>.

In Chapter 5, the significant electrical degradation of SiC-MOS capacitors with mobile ions at the interface indicates that these ion species intensely degrade the quality of the SiO<sub>2</sub>/SiC interface. A stretch-out of 1 MHz C-V curves was seen in the gate voltage ranging from flatband to accumulation for both samples. The stretch-out of C-V curves is considered to be due to the electron trapping into interface states near the conduction band edge which do not respond to 1 MHz. Furthermore, the marked difference between 1 MHz and ideal C-V curves for the PBTS sample means that mobile ions at the SiO<sub>2</sub>/SiC interface may induce additional interface states. Next, the densities of slow interface state (D<sub>it</sub>) were evaluated by Terman, conductance and C-ψ<sub>s</sub> methods. Significant increases in D<sub>it</sub> at both near the conduction band edge and below the Fermi level were observed for PBTS sample while NBTS sample did not show significant change in D<sub>it</sub>. These experimental findings show that the interface quality of FGA-treated SiC-MOS structures gets further improvement by removing mobile ions from the SiO<sub>2</sub>/SiC interfaces. Furthermore, a slight increase in the conduction band offset was observed for the samples

containing mobile ions at SiO<sub>2</sub>/SiC interfaces.

In Chapter 6, diffusivity of mobile ions in SiC-MOS devices was examined with deposited gate dielectrics. This study shows that the mobile ions can penetrate from thin thermally grown SiO<sub>2</sub> underlayer into deposited SiO<sub>2</sub> layer which is similar to that for single FGA-treated 40 nm-thick thermal SiO<sub>2</sub>/SiC structures reported in the previous chapters. Nevertheless, significant improvement of BTI characteristics by high-*k* aluminum oxynitride (AlON) dielectrics deposited on thin thermal oxides was demonstrated. The C-V characteristics of AlON samples did not change much by bias stressing due to reduced gate leakage current. AlON/SiO<sub>2</sub> stacked dielectrics were found to be beneficial not only for reducing the leakage current but also for suppressing diffusion of mobile ions, leading to stable SiC-MOS characteristics even under strong electric fields and high temperatures. Finally, diffusivity of the mobile ions inherent to AlON/SiO<sub>2</sub> structures was also investigated by conducting extended BTS experiments.

This doctoral study will further contribute to the power electronics research communities and industries in Japan and overseas for better understanding of fundamental physics in SiC-MOS (FETs). Furthermore, this study will recommend the “next stage” of advance innovation in modern SiC power MOS devices. The engineering of gate stacks and the designing of device architectures for SiC-MOSFETs are indispensable for realizing high-reliability and high-mobility operation. Besides, this study may present the precaution for manufacturer to perfectly fabricate SiC-MOSFETs with more concerns in reliability.

## 論文審査の結果の要旨及び担当者

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## 論文審査の結果の要旨

環境・エネルギー問題の解決に向けて、電気エネルギーの利用効率向上が求められている。電気エネルギーの利用では、発電から消費に至るまでの間に数多くの電力変換を行うが、その際のエネルギー損失を低減するためには、パワーデバイスの性能向上が不可欠である。従来、パワーデバイスにはシリコン半導体がいわれてきたが性能限界に近づきつつある。ワイドバンドギャップ半導体であるシリコンカーバイド (SiC) は高い絶縁破壊電界強度や熱伝導度を有し、次世代のパワーデバイス用材料として注目されている。近年、SiCショットキーバリアダイオードに続き、金属-酸化物-半導体電界効果トランジスタ (SiC-MOSFET) 普及への期待が高まっている。SiC-MOS構造の作製では、Siデバイスと同様にSiC表面の熱酸化によってSiO<sub>2</sub>ゲート絶縁膜を形成可能である。しかし、SiC基板を構成する大部分の炭素は気相中に熱脱離するが、その一部がSiO<sub>2</sub>/SiC界面に偏析し、様々な特性劣化を引き起こす。本論文では、SiC-MOSFETの閾値電圧変動に着目し、熱酸化SiO<sub>2</sub>/SiC界面構造や酸化後の各種の後処理に伴う可動イオンの異常生成現象を明らかにすると共に、その改善策を提示しており、学術的にも産業応用上も優れた業績をあげている。

第1章では、SiC半導体の特徴を紹介すると共に、SiCパワーデバイス導入による効果、さらには高温環境下でのMOSデバイスの閾値電圧変動 (Bias-Temperature Instability: BTI) 現象について述べている。第2章では、放射光光電子分光法を用いて熱酸化SiO<sub>2</sub>/SiC界面の構造を評価し、酸化膜界面には厚い構造遷移層は存在しないが、酸化膜厚の増大に伴って原子レベルでの結合状態の乱れが発生することを示している。第3章では、熱酸化SiO<sub>2</sub>/SiC構造中には正に帯電した可動イオンが存在し、酸化後の高温熱処理によってその多くを取り除くことができるが、高温水素アニールで再び可動イオンが発生し、SiC-MOSデバイスのBTI特性を劣化させることを明らかにしている。第4章では、SiC-MOSデバイスの詳細な評価から、酸化膜中に存在する可動イオンの面密度を求め、 $4.9 \times 10^{12} \text{cm}^{-2}$ もの可動イオンが存在することを明らかにしている。また、SiC-MOS構造中の可動イオン除去を目的として、高温条件下での負バイアス印加と酸化膜エッチングを組み合わせた手法の有用性を実証している。第5章では、SiO<sub>2</sub>/SiC界面に可動イオンが偏析した場合には、界面欠陥準位密度が増大し、MOS界面の電気特性劣化が生じることを報告している。第6章では、SiC-MOS構造中の可動イオンの問題を解決する手段として、窒素添加アルミナ絶縁膜と薄い熱酸化膜との積層構造 (AlON/SiO<sub>2</sub>) を提案し、SiO<sub>2</sub>膜厚を最適化することで、SiC-MOSデバイスの界面電気特性と安定性の向上を同時に実現できることを実証している。

以上のように、本論文では、SiC-MOSデバイスの特性変動の要因となる熱酸化膜中の可動イオンの異常生成現象を詳細に調べ、その改善策を提案し、優位性実証に成功している。これらは、熱酸化SiO<sub>2</sub>/SiC界面物性の理解に加え、産業応用の観点からも極めて重要な研究成果である。よって本論文は博士論文として価値あるものと認める。