Doctoral Dissertation

Study on Bias-temperature Instability in 4H-SiC Metal-oxide-semiconductor Devices

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July 2014

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Contents

List of Abbreviations

Abbreviation	Description
Al_2O_3	aluminum oxide (alumina)
AlON	aluminum oxynitride
Ar-POA	post-oxidation annealing in argon ambient
a-SiN:H	amorphous silicon nitride hydrogen alloys
BTI	bias-temperature instability
BTS	bias-temperature stress
CO_x	carbon oxides
C-V	capacitance-voltage
CVD	chemical vapor deposition
D-SIMS	dynamic secondary-ion mass spectrometry
DMOSFET	double-implanted MOSFET
FET	field-effect transistor
FGA	forming gas annealing
GSMBE	gas-source molecular beam epitaxy
HF	hydrofluoric acid
high-*k*	high relative permittivity
LPE	liquid-phase epitaxy
MEIS	medium energy ion scattering
MOS	metal-oxide-semiconductor
NBTS	negative bias-temperature stress
NBTI	negative bias-temperature instability
NO_x	nitric oxides
O_i	atomic oxygen
PBTS	positive bias-temperature stress
PBTI	positive bias-temperature instability
PDA	post-deposition annealing
POA	post-oxidation annealing
PSG	phosphosilicate glass
PVD	physical-vapor deposition
RCA	the Radio Corporation of America
R.T.	room temperature
SBD	Schottky barrier diodes
SiC	silicon carbide

Abbreviation	**Description**
SiO_2	silicon dioxide
SiO_xN_y	silicon oxynitride
SPring-8	the Super-Photon-ring 8 GeV
SRIM	the Stopping and Range of Ions in Matter
SR-XPS	synchrotron radiation x-ray photoelectron spectroscopy
TEM	transmission electron microscopy
UMOSFET	u-shaped MOSFET
VLD	variation of lateral doping
WBG	wide bandgap
XPS	x-ray photoelectron spectroscopy

List of Symbols

Symbol	Unit	Description
C	F	capacitance
C_{dep}	F	depletion capacitance
C_{it}	F	interface state capacitance
C_{ox}	F	oxide capacitance
C_p	F	probe capacitance
D_{it}	$cm^{-2}\ eV^{-1}$	interface state density
E_B	eV	binding energy of electron
E_c	eV	conduction band edge
E_F	eV	fermi level
E_g	eV	energy band gap
E_i	eV	midgap energy
E_v	eV	valence band edge
E_K	eV	kinetic energy of photoelectron
EOT	nm	equivalent oxide thickness
ΔE_c	eV	conduction band offset
ΔE_v	eV	valence band offset
f	Hz	frequency
G_p	S	parallel conductance
I_{DS}	A	drain current
N_d	cm^{-3}	donor impurity concentration
n_i	cm^{-3}	intrinsic carrier concentration
Q_M	cm^{-2}	mobile ionic charge areal density
Q_{ox}	cm^{-2}	oxide charge areal density
R_C	$m\Omega\ cm^2$	channel resistance
R_D	$m\Omega\ cm^2$	drift region resistance
R_{on}	$m\Omega\ cm^2$	on-resistance
S	cm^2	gate electrode area
T	°C	temperature
t_{ox}	nm	physical oxide thickness
V_{FB}	V	flatband voltage
V_G	V	gate voltage
V_{TH}	V	threshold voltage
ΔV_{FB}	V	flatband voltage shift

Symbol	Unit	Description
ρ_M	cm^{-3}	mobile ionic charge bulk density
ρ_{ox}	cm^{-3}	oxide charge bulk density
ε_{ox}	F/cm	permittivity of oxide
σ	-	standard deviation
τ	s	time constant of the interface states
φ_{sample}	eV	work function of sample
φ_{spec}	eV	work function of photoelectron spectrometer
φ_m	V	work function of gate metal
φ_{ms}	V	work function difference between the gate metal and the semiconductor
φ_s	V	work function of semiconductor
ψ_s	V	surface potential
ω	Hz	angular frequency ($2\pi f$)

Chapter 1 Introduction

1-1 Power Semiconductor Devices and Applications

1-1-1 Semiconductor technology for power electronics

Power electronics are an enabling technology practically used in various applications, *e.g.* energy production, electricity generation and transmission system, electric/hybrid automotive, electronics and IT appliances (Fig. 1-1). The essential role of power electronics is that they are responsible for regulating the energy flow and converting from sources up to loads. The most concerned topic among eco-friendly societies is that the systems should control the electric power very accurately with high power ratings and reduced energy losses.

The essential components in every power electronic systems are “power devices". The power devices operate very accurately, at high power density according to the demand of the load. In 1950s, semiconductor power devices, *i.e.* bipolar transistors and thyristors, were firstly introduced to replace vacuum tubes, the traditional power devices. Since then, the power semiconductor devices have taken an important role with silicon (Si) serving as the base semiconductor material [1]. The advancement of semiconductor and thin film technology accelerates the emergence of the standard Si-based power devices including unipolar and bipolar power devices used nowadays, *i.e.* power diodes, thyristors, power metal-oxide-semiconductor field effect transistors (MOSFETs), and insulated gate bipolar transistors (IGBTs) [2].

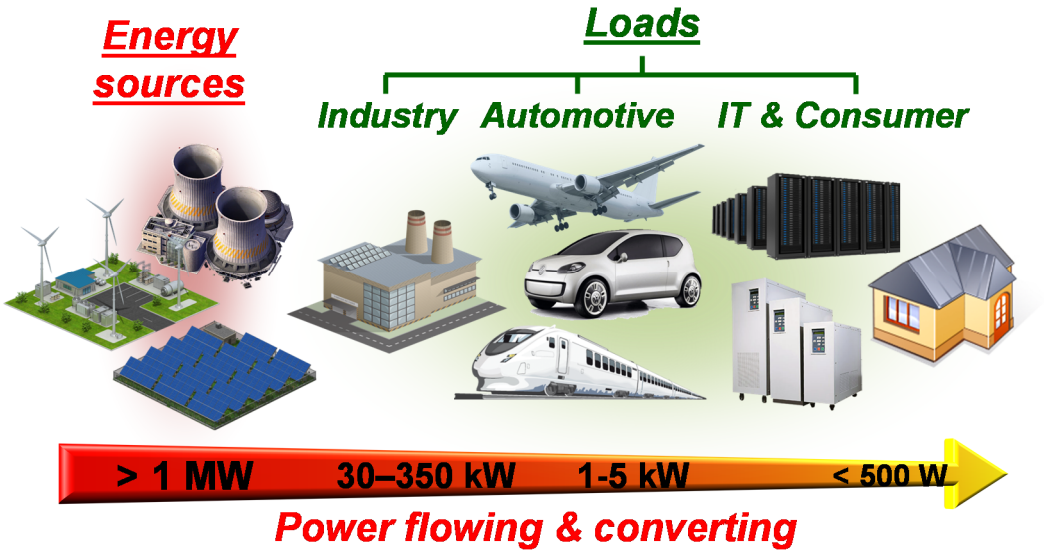

Fig. 1-1 Applications of power electronics with approximate power ratings

Over the past several decades, the development of Si-based power devices has shown impressive progress of providing a higher power rating, a faster switching frequency and reducing in power losses. However, an ineffective switching of Si power devices in higher voltage and current systems significantly generates many energy wastes. Furthermore, it has been widely recognized that the operation of Si devices at high temperature (T > 100°C) leads to prompt electrical degradations [3,4]. Accordingly, cooling systems are primarily composed that conclusively increases the overall weight and size. Therefore, novel semiconductors have begun to draw attention. Silicon carbide (SiC) has become the most promising candidate that considerably needed to substitute Si. By using SiC, the power devices can be functional at higher power density and higher temperatures. In October 2011, the SiC-based power devices have been lately introduced to replace with the Si power devices in the commercial Metro subway trains running on Ginza Line in Tokyo. It shows about 40% energy reduction compared with traditional railcars running on the same line. Moreover, it should be highlighted based on the Engineering Advancement Association of Japan (ENAA) study that if SiC devices replace all conventional Si devices in Japan, the amount of energy conservation will be equal to four nuclear power plants. The green innovations utilizing efficient power electronics could be realized by the emergence of modern power devices.

1-1-2 Wide bandgap semiconductors for power electronics

For the past few years, the development in “classical” semiconductor technology used in the power electronics has faced the inevitable obstacles due to unsuitable material properties of Si. This is because modern power devices should be well operated for applications in very-high-temperature regimes. For examples, the temperature condition for combusting chamber of the engine in some automotive systems commonly is as high as 300°C or more [5]. The temperature ambient closed to the jet engine in the aircrafts can reach 600°C [6]. The efficiency of semiconductor devices used at high temperature can be limited by the drastically increasing of intrinsic carrier concentration (n_i) at high temperature [2-4,7]. While the energy bandgap (E_g) of semiconductors is a function of temperatures (Fig. 1-2), the n_i increases exponentially with temperatures and strongly depends on E_g (Fig. 1-3). Consequently, the devices fail to operate at very high temperatures. To overcome this bottleneck, wide bandgap (WBG) semiconductors have been believed as the key materials [7]. Among the WBG semiconductors, silicon carbide (SiC) is the most promising candidate that considerably required to substitute for Si [8,9]. A low n_i due to WBG energy of SiC allows SiC to maintain semiconductor behavior that in turn permits the “modern” semiconductor device functionality at higher

temperatures than the “classical” power devices. It is also very beneficial for the devices to achieve rapid temperature cooling with very high thermal conductivity of SiC. Furthermore, the main advantage of WBG semiconductors is their very high breakdown voltages and critical electric field which allows the SiC devices to offer lower on-resistance (R_{on}) [7-9].

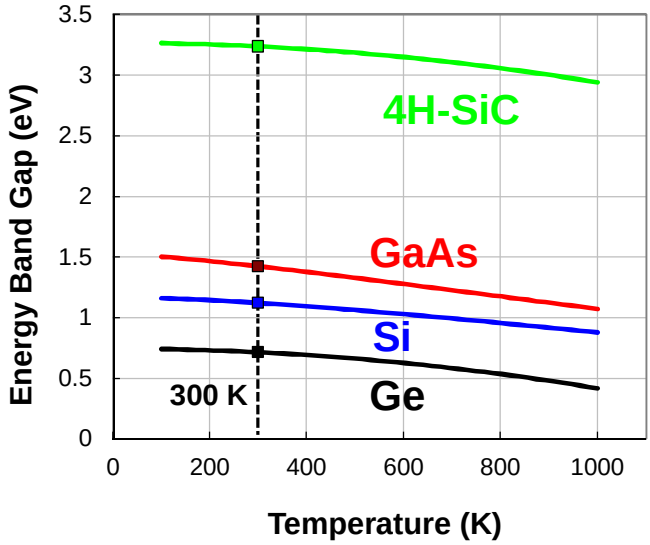

Fig. 1-2 Energy band gap versus temperature

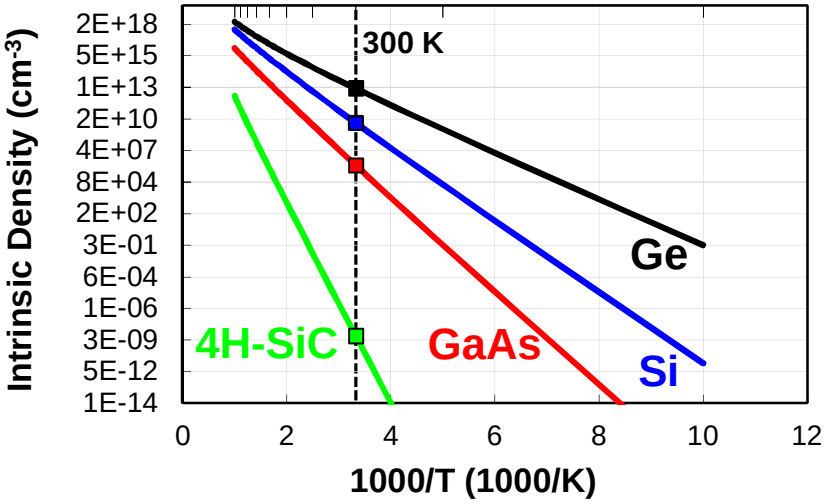

Fig. 1-3 Intrinsic carrier density versus temperature

1-2 General Information for SiC

1-2-1 Crystal structures and polytypes

SiC is a compound semiconductor material composed of bilayers of tetrahedrally bonded silicon and carbon atoms similar diamond. The tetrahedral molecular geometry

of SiC can be illustrated as a central atom of Si surrounded by four C atoms and vice versa. The two neighboring silicon or carbon atoms are separated with the distance of about 3.08 Å for all structures [10].

In general, SiC exists under stoichiometrically equivalent crystalline structures called polymorphs or polytypes [7]. Polytypes are crystals with the same stoichiometry, but bi-atom layers of Si-C pair are differently stacked with repeat sequences along one crystallographic direction (c-axis direction) for achieving hexagonal close packing. If we consider Si-C pairs (see Fig. 1-4(a)), there are three possible bonding sites denoted by A, B and C. The simplest stacking sequences of the ABC… for the "zincblende" structure called 3C-SiC is the only known polytype with a cubic crystal lattice structure in which the number "3" denotes the number of bi-atom layers required for one repetition, and the alphabet "C" is abbreviated "cubic" (see Fig. 1-4(b)). They are also referred to β-SiC. The rest of over 200 polytypes are α-SiC and also called "hexagonal" (the alphabet "H" is abbreviated). They have been reported in varying the material characteristics [11]. However, the commercial availability of large single-crystal wafers is limited to only few hexagonal polytypes, *i.e.* 6H and 4H which are appropriated for the development of SiC power electronics. The stacking sequences for 4H (ABCB…) and 6H (ABCACB…) are shown in Fig. 1-4(c) and (d), respectively.

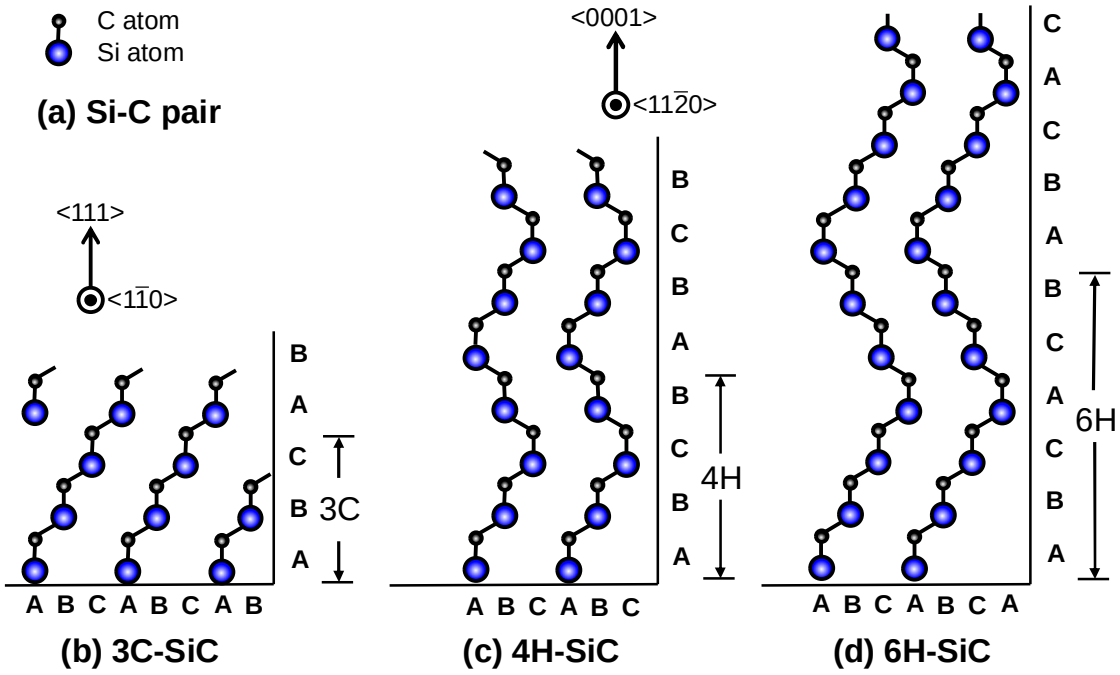

Fig. 1-4 (a) Bi-atom layers of Si and C atoms provide 3 possible bonding sites denoted by A, B and C. The stacking sequence of Si-C pair produces different SiC crystalline polytypes, e.g. (b) 3C-SiC, (c) 4H-SiC, and (d) 6H-SiC.

1-2-2 SiC bulk crystal and epitaxial growth

It is very difficult to obtain high quality SiC bulk single crystals with large diameter because of the thermal and physical stability of SiC. Unlike conventional semiconductor materials (*i.e.* Si and Ge), SiC cannot be easily grown by any traditional techniques of crystal growth, *i.e.* crystal pulling (Czochralski method) and solidification technique from molten [12]. Instead, the well-known process used for growing SiC bulk crystals called “seeded sublimation growth” or “modified Lely method” was introduced by Tairov and Tsvetkov in 1978 [13]. The process relies on physical vapor transport process of sublimated SiC powder placed inside a cylindrical graphite crucible. The SiC monocrystalline crystal growth by sublimation is a very complex process in which the pressure and temperature parameters of the crucible should be carefully controlled. As illustrated in Fig. 1-5, vapor mixtures of different carbon and silicon compounds are produced by the sublimation of polycrystalline SiC in a ring-like shape near the crucible walls at the temperature in a range of 2200-2400°C. The vapors are transferred through porous graphite walls over a controlled temperature gradient. So then it is deposited on a SiC seed crystal with desired crystal orientation installed at the top position of the crucible to preclude contamination by falling particles. Finally, the SiC bulk crystal is sliced to be SiC wafers for fabricating SiC power devices. However, wafer cutting process should be carried out very carefully due to the extremely hard and brittle of SiC crystal.

In the semiconductor electronics industry, low crystal defect densities of micropipes and dislocations in SiC wafers are vital for the production of power devices [14,15]. In additional to the defects in the bulk crystal, SiC wafer cutting, and polishing are critical issues considered for the production of physical-damage-free substrates [16]. Furthermore, control of polytypes and impurity concentrations during growth also challenge. Such an increased scale of development is required for a successful realization of a SiC device industry. Because of the continuing development of SiC crystal growth, such defect densities are getting lower.

Nowadays, almost all the SiC devices are not directly fabricated on the sublimation-grown bulk wafers but are instead fabricated on a thin “epitaxial layer” or “epilayer” on a bulk crystal wafer. High quality epilayers can be grown on SiC wafers using several techniques, *i.e.* liquid-phase epitaxy (LPE) [17], gas-source molecular beam epitaxy (GSMBE) [7], and chemical vapor deposition (CVD) [18]. To dope SiC materials, dopant species have extremely low diffusion coefficients in the SiC bulk crystal [19]. Therefore, it is not feasible to achieve high doping concentration using conventional diffusion techniques which are generally used for doping Si. The standard

n-type dopants are nitrogen (N) and phosphorus (P), and the common p-type dopants are aluminum (Al), and boron (B). In epitaxial growth by CVD, a doping concentration in the epilayers can be controlled by varying in a flow of the dopant gases and Si-source to C-source ratios (Si/C ratios) within the CVD growth reactor [19].

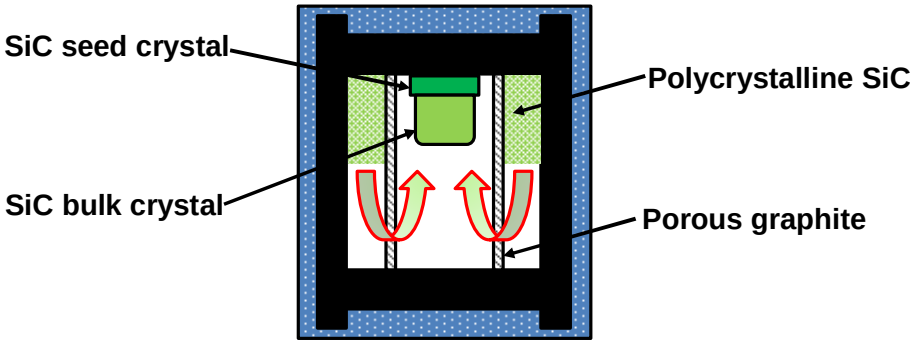

Fig. 1-5 Modified Lely method introduced by Tairov and Tsvetkov [13]

1-2-3 Physical properties

The research in SiC based power devices has been started for several decades. It is expected that the power devices may exhibit excellent performance and reliability due to its superior physical properties. The properties can be varied for different polytypes in which the most significant difference is the bandgap. As summarized in Table 1-1 [1-3,7-10], 4H-SiC shows remarkable properties for power devices due to its wider bandgap (E_g = 3.26 eV) compared with 6H and 3C polytypes which are advantageous for high temperature applications. Despite the fact that, the conventional Si-based power devices provide only ~100°C as the maximum operating temperature, the power devices fabricated on 4H-SiC substrate show higher efficient capability for operating in high-temperature conditions (400~500°C) with less requirement of cooling system. Although the diffusivity of dopant species is extremely low as states earlier [19], the dopants cannot be diffused in SiC at high temperatures due to its thermally stable properties. They are chemically inert and radiation tolerance that make devices suitable for operation in extreme environments. The breakdown field of SiC is 8 to 10 times higher than for silicon makes the devices with a significant reduction of R_{on}.

In addition, SiC is the only WBG material that provides a high quality native oxide, the silicon dioxide (SiO_2) film grown by thermal oxidation as gate insulator layers in "metal-oxide-semiconductor (MOS)" devices. Because of this merit, a SiC-MOS device fabrication process is less complicated in term of gate insulator formation comparing with that in other WBG semiconductors (*e.g.* GaN). According to these remarkable

physical properties of 4H-SiC, the development in power semiconductor devices has been accelerated for progressively pushing forward the achievement of high-efficiency and eco-friendly power devices.

Table 1-1 Comparison of the physical properties of Si, 3C-SiC, 6H-SiC and 4H-SiC [1-3,7-10].

	Si	**GaN**	**3C-SiC**	**6H-SiC**	**4H-SiC**
Bandgap energy (eV)	1.12	3.4	2.4	3.03	3.26
Relative dielectric constant	11.9	9.5	9.72	9.66	9.7
Breakdown field (MV/cm)	0.25	2–3	1.8	2.4	2.2
Thermal conductivity (W/cm.K)	1.5	1.3	3–5	3–5	3–5
Intrinsic carrier concentration (cm^{-3})	1.45×10^{10}	$\sim 10^{10}$	~10	1.6×10^{6}	8.2×10^{9}
Electron mobility ($cm^2/V.s$) at $N_D = 16\ cm^{-3}$	1200	900	800	//c-axis: 60 ⊥c-axis: 400	//c-axis: 900 ⊥c-axis: 800
Hole mobility ($cm^2/V.s$) at $N_A = 16\ cm^{-3}$	420	200	40	90	115
Saturated electron velocity (10^7 cm/s)	1.0	2.5	2.5	2	2
Silicon dioxide (SiO_2) grown by thermal oxidation	Yes	No	Yes	Yes	Yes

1-2-4 Development of SiC power devices

As stated in previous sections, SiC is the key semiconductor for realizing next generation power devices that can be used in higher power applications. The early development of SiC power devices has been notably concerned since the development of SiC-based Schottky barrier diodes (SBDs) in 1990s [20]. Similarly to the general purpose of a p-n junction (PN) diode, the SBDs can regulate the electric current to flow when a certain threshold voltage is biased in only one particular direction (forward bias). Unlike the PN diodes, the SBD is a majority carrier device, which means the flowing of n-type carriers (electrons) into a conduction band of the metal contact is the most important factor determining the standard diode operation. Hence, the SBDs provide much lower turn on voltage and do not present the reverse recovery time because the random recombination of n- and p-type carriers inherent to PN diodes is not affected. As a result, the switching speed of SBDs is very fast which is appropriate for higher-frequency power circuits. However, the reverse blocking voltage is defined below 150 V and leakage current in the reverse-blocking state is very large for the SBDs

fabricated on Si substrates. SiC-based SBDs are consequently very attractive because the high breakdown field of SiC provides the diodes significantly to increase reverse voltage capacity. In addition, a stable operation can be achieved at much higher temperature (T > 200°C). The most basic structure of SiC-SBD consists of a top-side Schottky contact with metal anode (*e.g.* Ni, Ti) and a lightly doped epitaxial drift layer (n^- layer) on a highly doped n^+ bulk SiC substrate (see Fig. 1-6(a)). Itoh *et al.* has proposed the implanted edge termination to reduce the electric field concentrated at the edge of devices (see Fig. 1-6(b)) [21]. As a result, the reverse blocking voltages SiC-SBDs with boron-implanted edge termination are higher than 1100 V. Nowadays, 4H-SiC SBDs have already been commercialized by Cree Inc. with enhanced blocking voltage up to 1700 V and reverse leakage current less than 1 μA [22]. In 2014, Mitsubishi Electric Co. Ltd. acquired 4H-SiC SBDs with the variation of lateral doping (VLD) technique to enhance the blocking capability to be 3300 V [23].

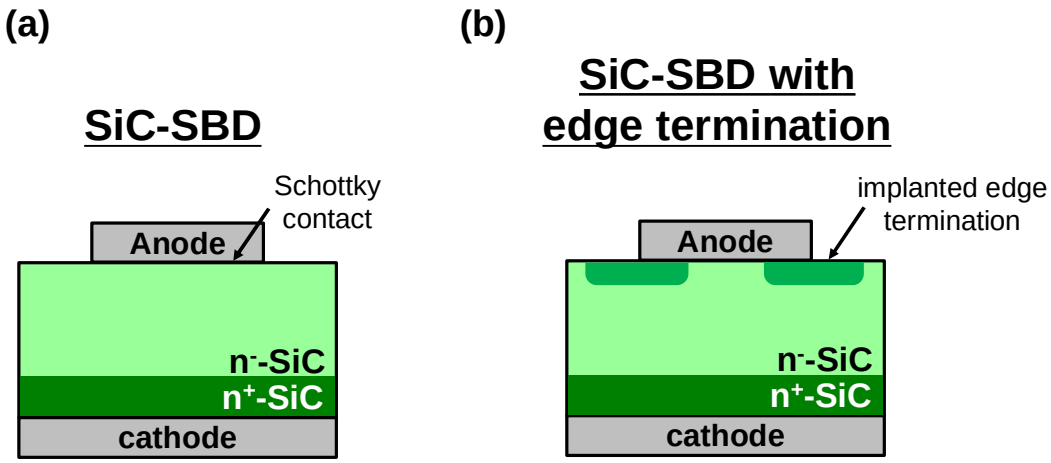

Fig. 1-6 Schematic-cross section of (a) SiC-SBDs and SiC-SBD with implanted edge termination. The implanted edge termination can enhance the reverse blocking voltage by reducing the electric field at the edge of the devices [21].

Power MOSFET is another type of power devices that have thoughtfully developed in parallel with the SiC-SBDs. The most attractive key factor for realizing SiC-based power MOSFETs is that, the thermal oxidation process can be adopted from that used for fabricating Si-MOS devices. Thermal oxidation of SiC will be discussed in Section 1-3-2 of this chapter. However, it should be noted that the MOSFETs used for power electronics is far different from those employed in complementary MOS (CMOS) technology. The direction of current flow in the power MOSFETs is vertical, and they are usually produced of thick drift region to suppress a large electric field. In 1997, the

SiC-MOSFETs utilizing double implanted MOS (DMOS) structures were firstly presented by Shenoy et al. [24]. A cross-section of the simple DMOSFETs is shown in Fig. 1-7. The vertical MOSFETs are usually fabricated on an high-quality n^- drift layer on highly-conductive n^+ substrates. Previously, the DMOS structures are composed in conventional Si-based vertical transistors in which the p-well and n^+ source regions are formed by a double implantation of dopants diffused through a single mask. However, the doping of SiC by conventional impurity diffusion is impractical due to low diffusion coefficient of dopant species in SiC [19]. Therefore, the fabrication of DMOSFETs on SiC substrates requires dopants introduced by double ion implantations with separate masks. The high-temperature annealing process is required to activate the ion-implanted regions. Then, thermal oxidation forms gate oxides. Metal gate and source/drain electrodes are finally deposited. The conductive path between n^+ source and n^- drift regions is formed to turn on the DMOSFETs by applying a positive bias to the gate electrode and source (V_{GS}). The flowing of majority carriers (*i.e.* electron) is driven by applying a positive voltage to the drain region. The mobility of SiC-DMOSFETs is defined by R_{on} in which combines many resistive elements throughout the conductive path. The drift region resistance (R_D) is one of the resistive components that are determined by the thickness of n-drift region. By using SiC, the thickness of drift region

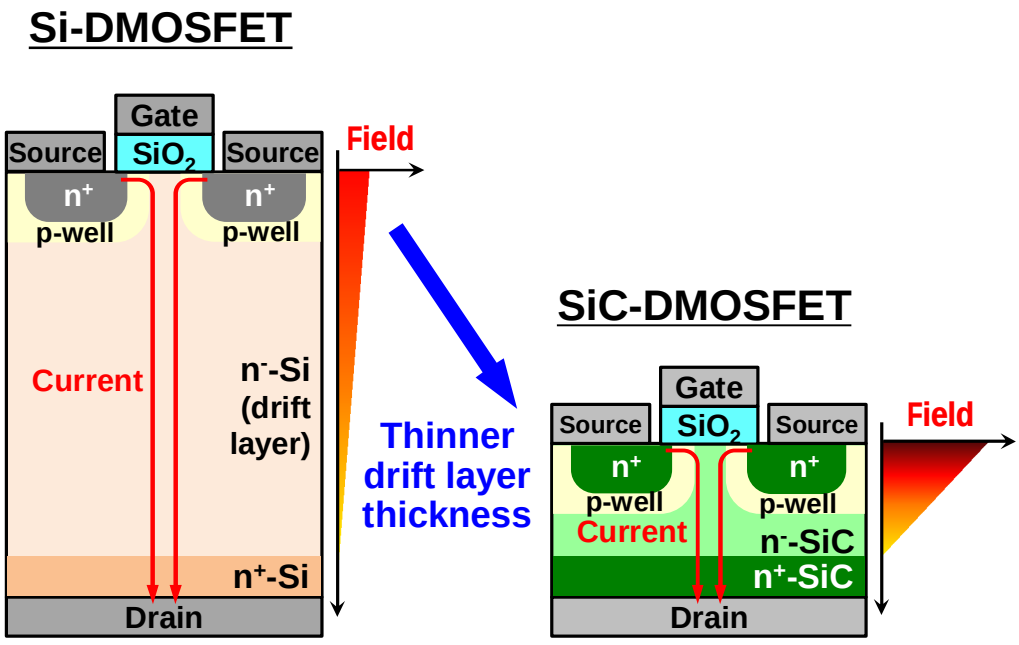

Fig. 1-7 Schematic-cross section of DMOSFETs fabricated on Si (left) and SiC (right) substrates. The thickness of drift (n^-) layer in SiC-DMOSFETs can be reduced with less concerned on large electric fields.

can be reduced by several orders that eventually result in significantly reduced in R_{on}. Regardless of the drastic increase in electric fields due to thinner drift layer thickness, the breakdown voltage of SiC is sufficiently 8-10 times higher than that of Si (see Table 1-1). However, a large channel resistance (R_C) due to weak SiO_2/SiC interfaces compensates the low R_D. Consequently, the R_{on} is majorly governed by the large R_C.

Another vertical power SiC-MOSFETs called U-shape MOSFET (UMOSFET) was firstly introduced by Cree Research Inc. in 1994 [25]. The vertically oriented majority carrier MOSFETs were fabricated on the SiC substrates with a trench structure. Figure 1-8(a) illustrates a structure of fundamental power SiC-UMOSFETs. The U-shape area allows the carrier to flow in MOS channel along the sidewall of a vertical-trench, which is formed by deep reactive-ion etching (RIE). Therefore, the shorter conductive path of the carrier is obtained compared with that of DMOSFETs for further reducing the R_{on}. The $(11\bar{2}0)$ face of the sidewall enables an increase in the channel mobility [26]. The JFET region usually formed by two adjacent p-well regions show less effect on the conductive path in the trench MOSFETs, so the resistance component due to JFET can be omitted from the R_{on} [27]. Furthermore, the SiC-UMOSFETs are attractive because

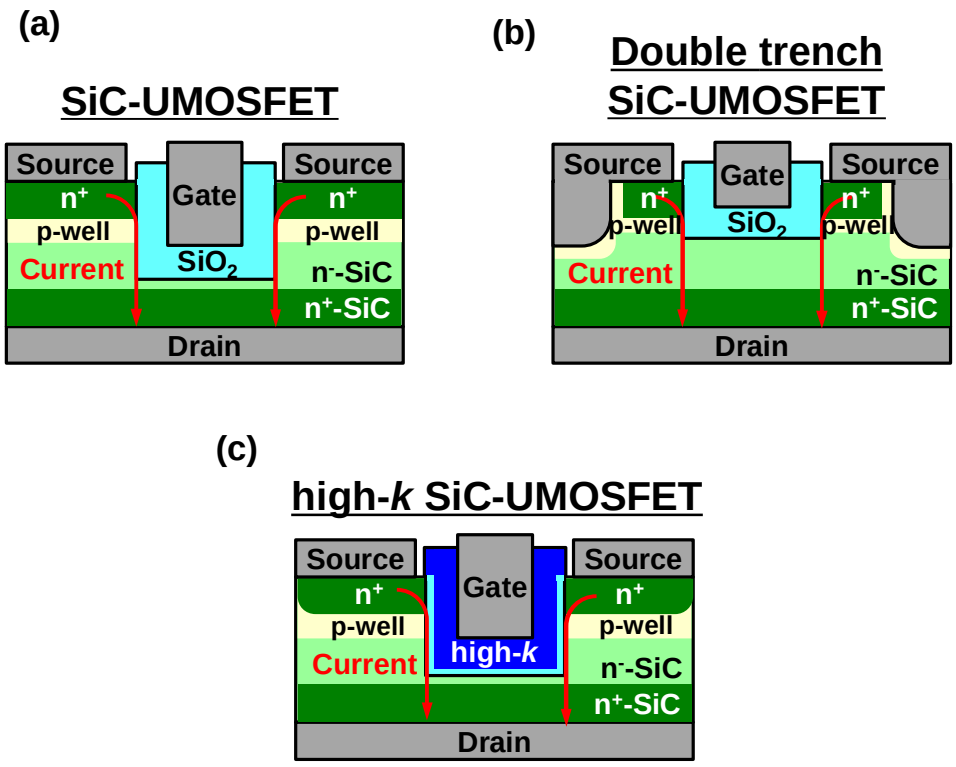

Fig. 1-8 Schematic-cross section of SiC-UMOSFETs, *i.e.* (a) conventional SiC-UMOSFET, (b) double trench SiC-UMOSFET [27], and (c) high-k SiC-UMOSFET [29].

the p-well and n^+ source areas can be epitaxially grown without less requirement of ion implantation or post-implantation annealing [25]. However, a major problem of SiC-UMOSFETs was reported regarding of high electric fields in the oxide located at the trench bottom [27,28]. Hence, the maximum breakdown voltage is strongly limited by the oxide breakdown rather than SiC breakdown. Therefore, the design of the device structure is necessary for making reliable UMOSFETs. The issue can be solved by suppressing the electric field at the gate trench bottoms and/or in the oxides. Increasing oxide thickness and forming an ion-implanted p-region at the trench bottom are the most basic technique proposed to suppress the electric field in SiO_2 [28]. ROHM Co., Ltd. recently proposed to reduce the field at the gate trench bottom by using a double trench structure [27], where the source trench is fabricated deeper than the gate trench as illustrated in Fig. 1-8(b). More recently, Hosoi *et al.* proposed to insert the thick high-*k* layer on the thin SiO_2 for further reduction of the electric field at the gate trench (see Fig. 1-8(c)). For example, the higher relative permittivity of alumina (Al_2O_3) based high-*k* (ε = 6~8) suppresses the oxide field by half compared with single SiO_2 [29].

1-3 SiC Metal-Oxide-Semiconductor (MOS) Devices

1-3-1 SiC-MOS structure

The advancement of thin film technology is a primary key to progress the development of next generation semiconductor devices. Although the thin film technology for electronic devices has been rapidly developed for many decades, MOS structures have still played a crucial role as the most fundamental unit in every MOS devices, such as MOS capacitors and MOSFETs [2]. MOS capacitors are the simplest MOS device because the fabrication process is straightforward. The MOS capacitor structure shown schematically in Fig. 1-9(a) can be made by only depositing a gate metal on the SiO_2/SiC structures. Energy levels of metal (*e.g.* Al)/SiO_2/4H-SiC structure and the band offsets, *i.e.* conduction and valence band offsets (ΔE_c and ΔE_v) between SiO_2 and 4H-SiC are illustrated in Fig. 1-9(b). Essential information related directly to characteristics and properties especially the details about oxides and oxide-SiC interfaces can be deduced from MOS capacitor studies without fabricating a complete SiC-MOSFET.

In the SiC-based MOS devices, one of the merits compared with other WBG semiconductors is that the fabrication technology can be borrowed from that used for Si, because these two semiconductors provide similar native oxides or SiO_2 grown by thermal oxidation. This makes SiC to be very attractive in research especially for the

experts who previously worked in the field of Si-based devices. Although outstanding performance and reliability of SiC-MOS devices are promising based on theoretical aspects, they are limited by the low quality of thermal oxides and SiO_2/SiC interfaces.

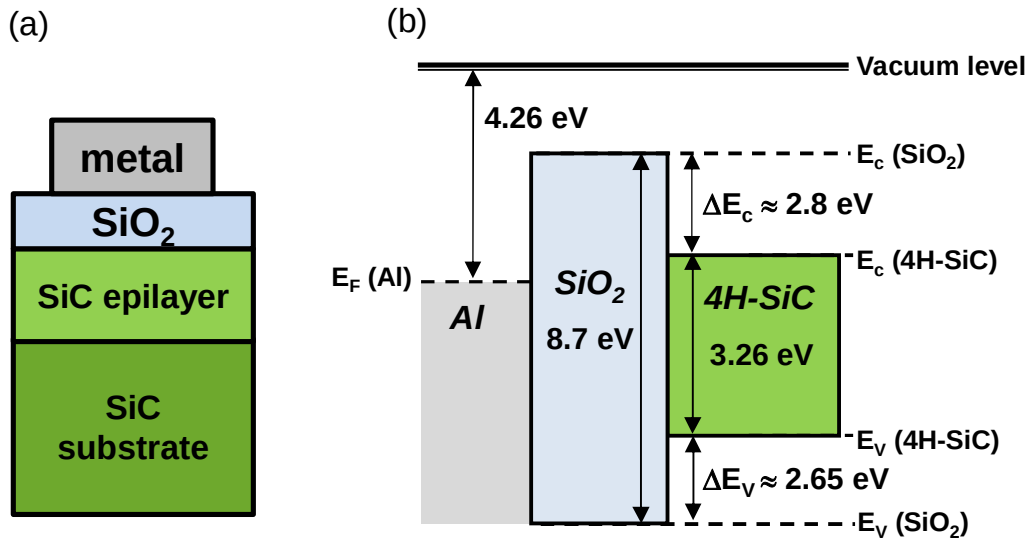

Fig. 1-9 Two-dimensional diagrams for metal-oxide-semiconductor (MOS), such as (a) simple 4H-SiC MOS capacitors and (b) band offsets of Al/SiO_2/4H-SiC structures.

1-3-2 Thermal oxidation of SiC

As mentioned earlier, the most significant merit of SiC is that, an insulating SiO_2 film can be formed on SiC by thermal oxidation. Although thermal oxidation of SiC can be performed in either dry (O_2) or wet (H_2O) oxidants [30], in fact, it is required much higher temperature (T = 1000°C~1400°C) and longer time than that of Si to achieve. Regardless of the crystal face independence oxidation rates in the case of Si, the oxidation kinetics of SiC is largely dependent of crystal orientation [31]. Meaning that the mechanism of thermal oxidation for SiC is far different from what occurs in Si. The oxidation mechanisms for Si and SiC are summarized in Table 1-2.

To explain the chemical reaction during dry oxidation of SiC substrate, Si-C bonds are firstly broken in rich gas conditions of oxidizing oxidants at typical high temperatures. This allows the reaction between Si atoms and the ambient oxidants to form SiO_2 layers on the SiC substrates while release the excess carbon impurities as the by-products in forms of carbon oxides (CO_x) diffused out from SiO_2. Many theoretical models such as the “Deal-Grove model” [32] and its modifications [31,33,34] were proposed to describe the oxidation kinetics of SiC.

Table 1-2 Comparison of the physical properties of Si and SiC

	Si	**SiC**
Temperature (°C)	700–1100	1000–1400
Oxidant	O_2 (dry), H_2O (wet)	O_2 (dry), H_2O (wet)
Reaction	$Si+O_2 \rightarrow SiO_2$	$2SiC+3O_2 \rightarrow 2SiO_2+2CO\uparrow$
Crystal face dependency	No	Yes

In the modified Deal-Grove models, the growth kinetics of SiO_2 on SiC substrate can be divided into two regimes, the reaction-limited regime (*a.k.a.* the linear regime) of the thin oxides and diffusion-limited regime (*a.k.a.* the parabolic regime) of the thick oxides. At the beginning of thermal oxidation, the physical oxide thickness (t_{ox}) is quickly increased as a linear function of oxidation time. The activation energy for surface reaction in thin oxide only about 1.3 eV was estimated for the thermal oxidation of 4H-SiC [31,35], which is lower than that of Si (~2 eV) reported by Deal and Grove [32]. First principle studies suggested that an atomic oxygen (O_i) is the main oxidant rather than a molecular oxygen (O_2). The calculated energy barrier of about 1.2 eV is enough for the reaction of O_i to oxidize at thin SiO_2/4H-SiC interfaces while the barrier for the interface reaction of O_2 is much higher [36]. The concrete evidence for the O_i generation and abnormally enhanced growth in the linear regime are vaguely understood at present stage.

In later diffusion-limited regime, the oxidation kinetics are then encountered a transition stage when t_{ox} increases to be a certain nm-thick (< 10 nm). The in-diffusion of oxidants and out-diffusion of CO_x in SiO_2 are considered for determining the growth rate in this regime. It should be noted that the large activation energy of about 3.8 eV was recently reported for the oxidation of 4H-SiC in this regime [37]. Regardless of the lower energy barrier required for molecular O_2 diffusion in SiO_2 (~1.2 eV) [38,39], the rate limiting process of SiC oxidation does not depend on the O_2 concentration in SiO_2, but rather the delicate reaction at the interfaces. Furthermore, the number of carbons remained in the SiO_2 is also expected to be slight [40], because the barrier only 2 eV is required for CO_x out-diffusion [41]. The marked reduction in the oxidation rate is probably because of chemical state changes at SiO_2/SiC interfaces.

1-3-3 SiO_2/SiC interface properties

The performance of SiC-MOSFETs can be inferred from the mobility that corresponds with the number of inverted carriers transported in the channel under the SiO_2/SiC interfaces. In general, a channel mobility of MOS devices can be affected by many scattering manners due to atomic and/or macro defects at the interfaces [2]. A presence of large interface defect densities does not only degrades the channel mobility directly by scattering effects but can likewise produce a large number of "electron/hole states" in bulk SiO_2 layers and at SiO_2/SiC interfaces as illustrated in Fig. 1-10. The interface states act to be the "traps" to capture carriers and then enhance Coulomb scattering of mobile carriers in the channel to degrade the effective mobility.

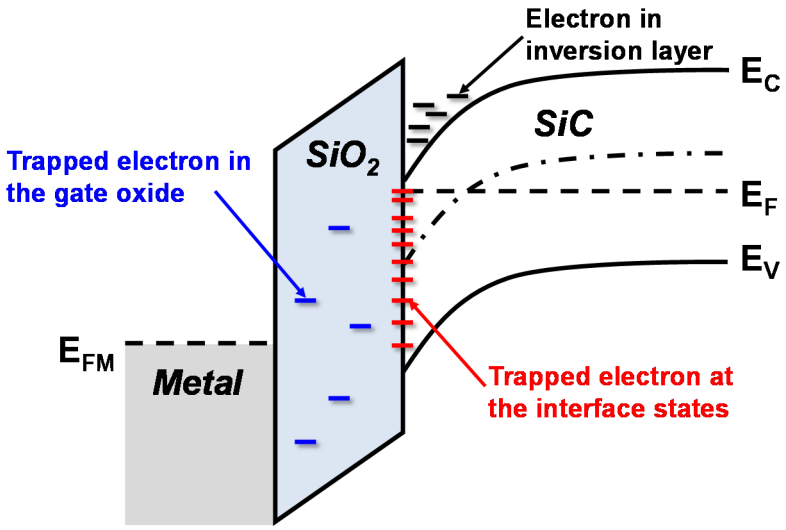

Fig. 1-10 Band diagram of MOS structures in an n-channel SiC-MOSFET biased to strong inversion shows electron trapping in SiO_2 and at SiO_2/SiC interface with the high trap states density near the conduction band edge (E_c) of SiC.

The lack of SiO_2/SiC interface quality results in the drastic electrical degradations of SiC-MOSFETs. Previously, the origin of large interface states density (D_{it}) is usually assigned to the imperfect growing of SiO_2 during thermal oxidation that is the formation of Si dangling-bonds at SiO_2/Si interfaces [2]. However, this mechanism has been strongly argued for determining the D_{it} only from the dangling-bond defects for SiC-MOS structures, but rather due to the number of interstitial carbons and C-related defects remained within bulk SiO_2 and at SiO_2/SiC interfaces after thermal oxidation [40,42]. For example, carbon clusters (C-C bonds) with different sizes and chemical structures presented near SiO_2/SiC interfaces are one of the obstacles. Afanasev *et al.* reported that these larger graphitic structures associated with the production of accepter

like states at the interfaces (negative charge when captured with electrons) [31]. Thermally grown SiO_2/SiC structures generally exhibit large D_{it} near the conduction band edges (E_c). The trap density is typically more than 10^{13} cm^{-2} eV^{-1} for the as-oxidized SiO_2/4H-SiC structures, which is much higher than that occurred at SiO_2/Si interfaces (~10^{10} cm^{-2} eV^{-1}). This strongly suggests an unacceptable performance of SiC-MOSFETs without any interface defect passivation [43,44].

1-3-4 Interface quality improvement by post-annealing treatments

In order to reduce the number of trap density at SiO_2/SiC interfaces, various interface treatments have been proposed to reduce the number of trap states. Post-oxidation annealing (POA) in gas ambient, *e.g.* nitric oxide, NO_x [45]; nitrogen, N_2 [46]; ammonia, NH_3 [47] hydrogen, H_2 [48], is the most fascinated methods that efficiently alleviate the problem by neutralizing the trap states.

The pioneering work on nitridation for thermal SiO_2/SiC systems reported by Li *et al.* suggested that POA in NO [45] is beneficial for reducing density of trap states, but POA in N_2O increase the density (see Fig. 1-11). Nevertheless, Kimoto *et al.* suggested that direct oxidation in N_2O improves the interface quality [49]. Recently, the nitridation has been popularly included as the standard procedure for the commercial SiC-based power MOS devices.

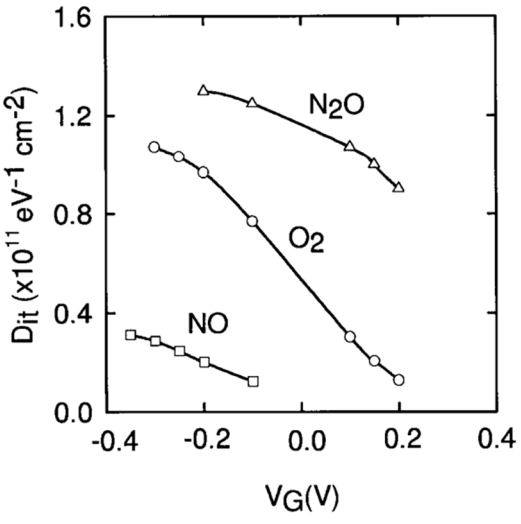

Fig. 1-11 Interface state density estimated by conductance method versus gate voltage of the SiC-MOS capacitors with thermal oxides grown in dry O_2. The samples were treated with post-annealing in N_2O or NO [45].

Additionally, H_2 has received attention because of its ability to reduce in trap densities. Post-annealing in H_2 at moderate annealing temperatures around 400°C is very effective to passivate the Si dangling bonds by forming Si-H bonds at SiO_2/Si interface [2]. The well-known POA in diluted H_2 ambient (H_2/N_2) so-called "forming gas annealing (FGA)" is commonly used to treat interface traps in conventional fabrication of Si-MOS devices. FGA has been recently adapted to use for the interface treatment of thermal SiO_2/SiC interfaces [48,50,51]. However, in fact, H_2 annealing at mild temperature as used for Si case is ineffective to decrease trap states due to the C-related and other complex defects at SiO_2/SiC interfaces. Previous studies on the effect of H_2 annealing in 4H-SiC MOS devices suggested by Fukuda *et al.* that the D_{it} in SiC-MOS devices decrease as the annealing temperature increases and saturates around 800 - 1000°C (see Fig. 1-12) [48]. The D_{it}, typically less than 10^{12} cm^{-2} eV^{-1} at the shallow energy level, E_c-E > 0.3 eV was obtained after the high-temperature FGA. A report on the mechanism for H_2 passivation in 4H-MOS devices suggests that H_2 molecules dissociate in SiO_2 and reacts with interfacial carbon residues, *e.g.* carbon clusters (C-C bonds). This process finally, produces C-H fragments in SiO_2 and/or at SiO_2/SiC interfaces [52]. The fragment sizes are believed to be smaller than their original C-C clusters resulting in the reduction of trap density. However, the reduction in D_{it} is still slight compared to that in the case of SiO_2/Si interfaces. The breakthrough improvement in the inversion mobility of SiC-MOSFETs is a most serious challenge for the SiC community. In order to achieve this, the deeper understanding of chemical configuration at thermally grown SiO_2/SiC interfaces is necessary.

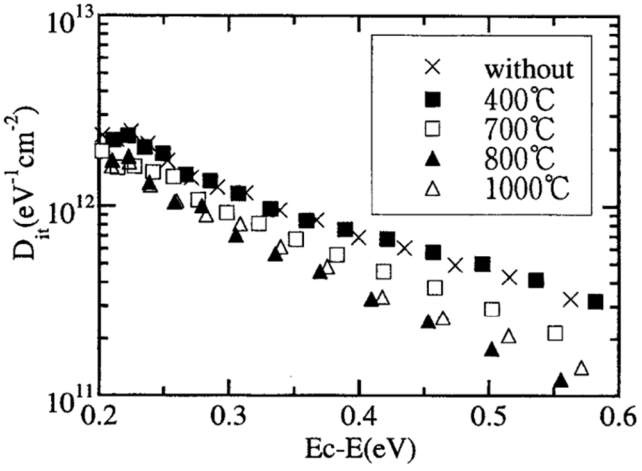

Fig. 1-12 Hydrogen annealing temperature dependence of D_{it} as a function of energy from the conduction band edge (E_c) by the high-low technique at probe frequency (f = 100 kHz) [48].

1-3-5 Deposited gate stacks for SiC-MOS devices

To simply avoid the defect complication in thermally grown SiO_2 and at SiO_2/SiC interfaces, the use of “deposited gate insulators” with “less importance of thermal oxidation” is considered to be a hope for the next generation SiC-MOS devices. It is previously mentioned that the oxidation of SiC requires much higher temperatures than that of Si to grow SiO_2 but the reaction rate is terribly slow. Hence, the processing time for device fabrication can be also reduced by using deposited insulators that are very attractive for mass-production of commercial devices. Some research groups have recently begun to develop SiC-MOS devices using deposited insulators. As shown in Fig. 1-13, a significant reduction in D_{it} and increase in effective mobility of SiC-MOSFETs can be achieved by using deposited SiO_2 followed by NO [53-56] or N_2O annealing [54,56]. These kinds of devices also slightly improve dielectric breakdown characteristics and show less dependence on defects in SiC substrates.

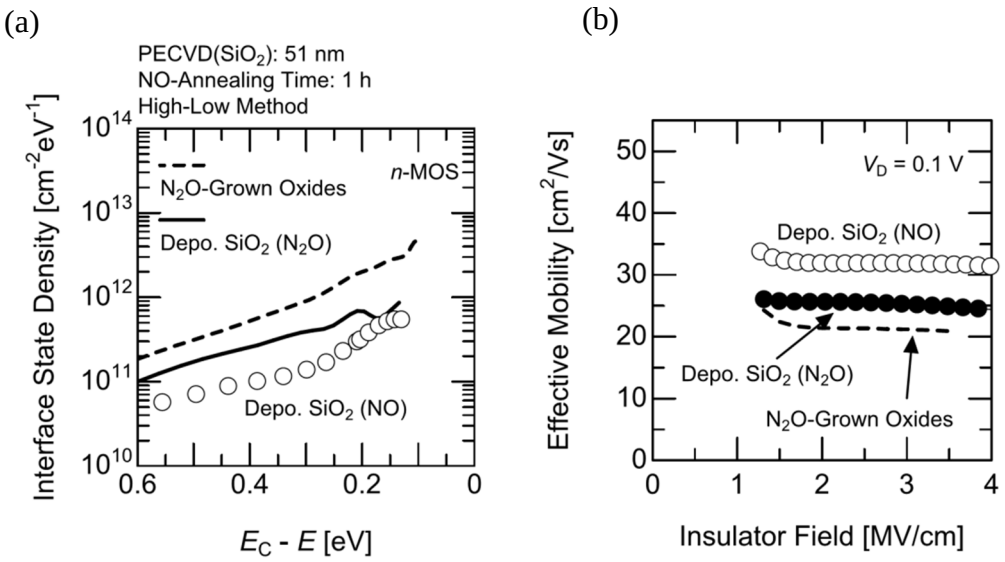

Fig. 1-13 (a) Distribution of D_{it} of SiC-MOS structures near the conduction band edge and (b) effective mobility as a function of insulator fields of SiC-MOSFETs with deposited SiO_2 annealed in NO or N_2O at 1300°C [56].

However, a degraded reliability for SiC-MOSFETs due to a large leakage current must be concerned, because the strong electric field in SiO_2 determines gate leakage current and thus poor gate reliability. Therefore, deposited dielectrics with high relative permittivity (high-*k*) may be replaced with the conventional SiO_2 to reduce the electric field across the gate insulators and also a leakage current [57]. Al-based high-*k* dielectric is a potential candidate because of its high thermal stability and wide band gap.

Aluminum oxide (Al_2O_3) is the most common dielectric that is extensively studied. However, the devices have been suffering from high density of electron traps in the deposited Al_2O_3 layer that result in threshold voltage (V_{TH}) instability in SiC-MOSFETs [58].

Our research group recently proposed to solve this problem by using SiC-MOS structures with stacked insulators of aluminum oxynitride or alumina (AlON) on thin thermal SiO_2 underlayer [29,58,59]. According to the benefit of nitrogen to passivate defect stages in an insulator layer, the SiC-MOSFETs fabricated with AlON/SiO_2 gate dielectrics shows reduced fixed charges. Figure 1-14(a) shows the flatband voltage (V_{FB}) of SiC MOS capacitors with Al_2O_3/SiO_2 and AlON/SiO_2 gate dielectrics plotted against the applied positive gate voltage. Electron injection from SiC substrates was significantly suppressed by using the AlON dielectrics. The suppressed V_{FB} shift for the AlON/SiO_2 sample revealed that N incorporation into Al_2O_3 significantly reduces not only the fixed charges but also the electron traps [45]. Moreover, as shown in Fig. 1-14(b), since the accumulation of residual carbon impurities is considered to be a possible cause for interface degradation, a D_{it} reduction in the AlON/SiO_2 device may attribute to the thin SiO_2 underlayer [40].

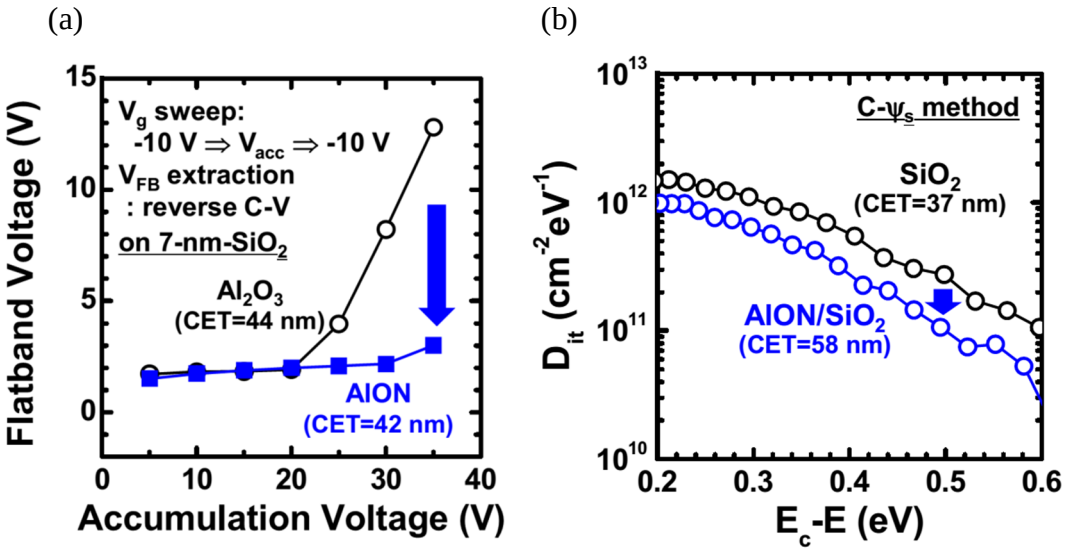

Fig. 1-14 (a) Flatband voltage of 4H-SiC MOS capacitors with stacked gate dielectrics consisting of 65-nm-thick Al_2O_3 or AlON layer and 7-nm-thick SiO_2 interlayer as a function of accumulation voltage. (b) Energy distribution of interface state density estimated for planar MOS capacitors with SiO_2 single and AlON/SiO_2 stacked gate dielectrics. The smaller D_{it} was obtained for AlON/SiO_2 devices [29].

1-4 Bias-temperature Instability (BTI) in SiC-MOS Devices

1-4-1 Overview of BTI studies

Most work so far of power SiC-MOSFETs has focused on the increase of mobility in which carbon impurities and other related defects in bulk SiO_2 and at SiO_2/SiC interfaces play crucial roles on this issue. Many interface passivation procedures were introduced to solve this problem. Besides, considering beyond the interface quality, reliability of the SiC devices at high-temperature have lately become attractive topics. To control the power electronics in the fail-safe applications e.g. aircrafts, railways, and automobile, it is not allowed that the power devices degrade the performance during operation lifetime of the system. It should be confirmed that the devices must be well-operated without serious failures under a wide range of environmental stresses. So far, bias-temperature instability (BTI) is one of the general reliability issues in Si-based MOS devices. This term describes the induced generations of oxide charges and interface traps under the gate biases at high temperatures. The traps and mobile ions in the oxides have been pointed out to be the main causes for BTI in Si-MOS. The mobile ions causing BTI will be explained in the next section.

Considering the trapped charge buildups, either hole or electron trappings due to induced carrier injection at high temperature originate distinct voltage shifts, *i.e.* V_{TH} shift in MOSFETs, V_{FB} shifts in MOS capacitors. So far, it has been affirmed that the magnitude of V_{TH} shifts in Si-based planar MOSFETs increases as a function of applied gate biases [60]. The V_{TH} of n-channel Si-MOSFETs is shifted toward the negative direction when the negative voltage stress is applied at 200°C (see Fig. 1-15). Nearly all intrinsic trap states existed in Si-MOS structures are identified as the Si dangling bonds

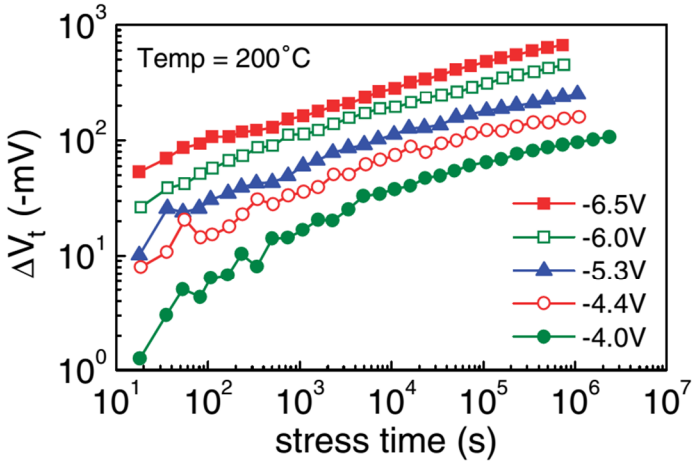

Fig. 1-15 Threshold voltage shift versus stress time of Si-based p-MOSFETs under various stressed gate voltages at 200°C [60].

that can be efficiently passivated by hydrogen annealing. However, the operation of these devices at high temperatures leads to the regeneration of oxide and interface traps due to hydrogen dissociation. The degradation mechanism is assumed that the gate bias stresses at high temperatures enhances the releasing of hydrogen atoms from the passivated Si dangling bonds (Si-H bonds), thus severe deterioration of interface quality [61-64]. Therefore, the operation of the Si-MOSFETs at high temperature leads to an increase in leakage current and decrease in mobility.

Notwithstanding the fact that the prompt reliability degradation due to BTI in Si-based MOS devices has been extensively studied for decades, the investigation in the field of SiC was still infancy and required to be further explored. There are few studies on BTI in SiC-MOS devices that have advised the mechanisms of BTI in SiC-MOS devices. Most of the researchers have considered that mechanisms do much differently from that BTI in Si. It was started in 1999 since Bassler *et al.* reported BTI characteristics of n- and p-type 6H-SiC MOS capacitors [65]. They found that, a

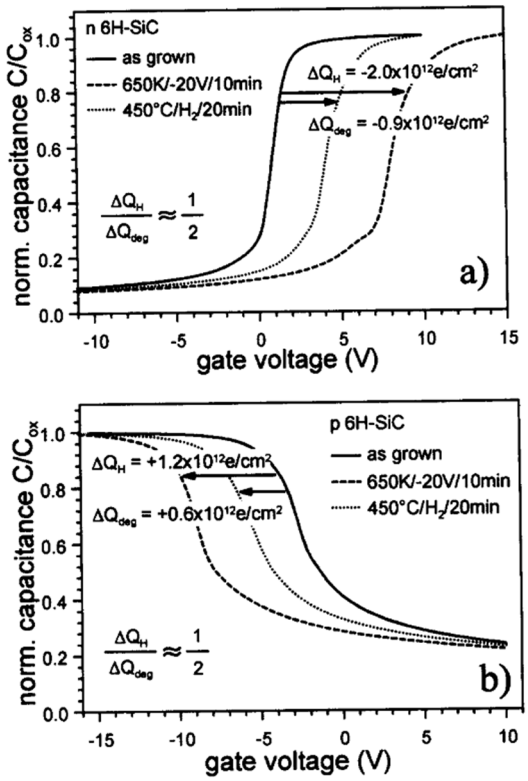

Fig. 1-16 C-V characteristics for (a) an n-type and (b) a p-type 6H-SiC MOS capacitor. Three experimental conditions are observed: as-grown (solid curve), stressed (dashed) and stressed with subsequent hydrogen passivated (dotted). As shown in the figure almost half of the fixed charge is passivated independent of the sign of the charge [65].

negative bias-temperature stress (NBTS) at temperature T > 600 K originating the V_{FB} shifts in capacitance-voltage (C-V) characteristics due to the creation of fixed charges in thermal oxides, *i.e.* positively fixed charge for n-type MOS capacitors or negatively fixed charges for p-type MOS capacitors (see Fig. 1-16). In addition to these results, they reported that the FGA in diluted H_2 (5% H_2/N_2) annealing at 450°C for 20 min further, remove approximately half amount of the total generated fixed charges. From this point of view, the negative-bias-temperature instability (NBTI) of 6H-SiC MOS devices is susceptible to Si dangling bonds similar to those in the Si devices. In other words, the fixed charges can be partly passivated by hydrogen annealing with the typical annealing temperatures (400~450°C) as used for SiO_2/Si systems. However, influences of the settled interface defects induced by NBTS that could not be only defined as Si dangling bonds were not clearly described in this study.

More recently, Marinella *et al.*, represented extra evidences of NBTI in MOS capacitors fabricated on n-type 4H-SiC substrates [66]. Based on the NBTI mechanism reviewed by Schroder and Babcock [64], the NBTI in Si-MOS devices with hydrogen passivation requires a sufficient number of holes to interact with Si-H bonds at SiO_2/Si interfaces to recreate the interface traps due to hydrogen dissociation. Similarly, they claimed that the NBTI in n-type SiC-MOS devices is also considered to be caused by the sufficient amount of holes at the SiO_2/SiC interfaces. However, the n_i is relatively low in the case of MOS devices fabricated on n-type SiC substrates (see Fig. 1-3), corresponding to the negligible number of electron-hole pair generation at the measurement temperature up to around 200°C. Therefore, because of the absence of

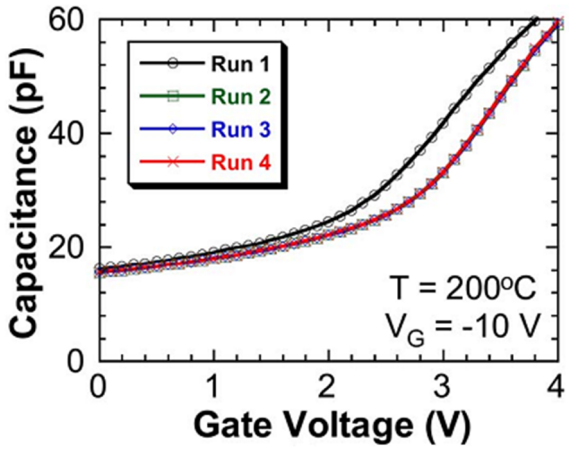

Fig. 1-17 the C-V curves obtained at room temperature before (Run 1) and after consequently applied NBTS at 200°C (Run 2 to 4). The NBTI is not apparent in these results. However, positively shifted V_{FB} was observed instead due to positively charge mobile ion drift [66].

holes at T < 200°C, the interface state generation produced by NBTI is considered very difficult to not be addressed. More interestingly, as illustrated in Fig. 1-17, this study observed the unusual positive V_{FB} shift in C-V cures measured after negative bias stressing at 200°C. They attributed this V_{FB} shift to the effect of mobile ion drift in thermal oxide at high-temperature. However, there is no supporting conclusion addressing the origin of these mobile ions.

Furthermore, Okayama *et al.* performed an extensive work on the positive-bias-temperature instability (PBTI) of n-channel 4H-SiC DMOSFETs [67]. They observed the shifts of V_{TH} and drain current (I_{DS}) with positive BTS at various temperatures up to 130°C. At the room temperature, positive V_{TH} shifts were dominant with PBTS due to the capture of injected electrons by the traps in thermal oxides and/or at SiO_2/4H-SiC interfaces. However, the negative V_{TH} shifts were apparently observed after applying positive gate bias stresses at high temperatures (see Fig. 1-18). They claimed that the instability of V_{TH} at high-temperature be attributed to the existence of positively charged mobile ions in the thermal oxide, which may be some contaminants from the molybdenum gate metal or may be hydrogen ions from device passivation film. Although the mobile ions presented in SiO_2 cannot move by the applied gate biases at room temperature, they are able to move only at high temperatures. If the mobile ions move toward the SiO_2/SiC interface, the increasing number of interface charges can severely affect the MOSFET characteristics.

Even though, some evidences of the BTI in SiC-MOS device have been heretofore reported, the origins of BTI and mobile ion phenomena have been lacking and needed further explanation.

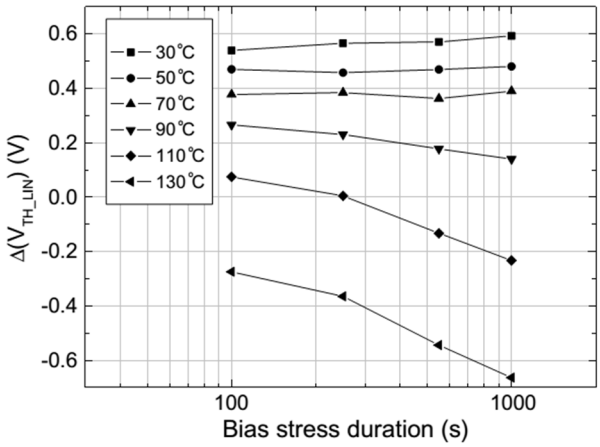

Fig. 1-18 Shift in V_{TH} with positive gate bias stress time at different temperatures ranging from 30 to 130°C [67].

1-4-2 Mobile ion causing BTI

In the field of Si-MOS technology, the BTI caused by mobile ions in Si-MOS devices have been widely known for decades that the typical mobile ions are alkaline ions (K^+, Na^+), hydrogen ions (H^+), and some organic contaminations [2,68]. The mobile ion drift was remarkable because an increase in a number of positive charges near the SiO_2/SiC interface under applied positive gate bias that is opposite from the voltage shift by carrier injection (see Fig. 1-19). Besides, the mobile ions are supposed to be unpredictable and difficult to guess. This is because these ions diffuse inside the gate oxide following different circumstances of gate biases and temperatures. Depending on the total number of mobile ions inside the oxide, the gate voltage fluctuation can be wherever from few volts to tens of volts, which results in unreliability of device performances and features. This effect is particularly severe for the V_{TH} shift of MOSFET, possibly changing the device operating characteristics from "normally-off" to "normally-on", or vice versa.

For many years in the semiconductor device fabrication, surpassing precaution has been perceived to avoid extrinsic mobile ions by using clean apparatuses, high purity quartz and metals for every processing. Furthermore, the development of fabrication methods respectively for the prevention and removal of mobile ions has been proposed, for instance, ion trapping in phosphosilicate glass (PSG) films on SiO_2 [69], utilizing silicon oxynitride (SiO_xN_y) [70] and capping SiO_2 by plasma-deposited amorphous silicon nitride hydrogen alloys (a-SiN:H) [71]. Hence, the simple ionic contamination through device fabrication is assumed to be neglect in a recent fabrication of semiconductor devices. Despite these various methods were developed for Si-MOS technology to eliminate and/or limit the alkaline mobile ions in the gate oxide, a suitable method to prevent the mobile ions in SiC-MOS devices has not been introduced.

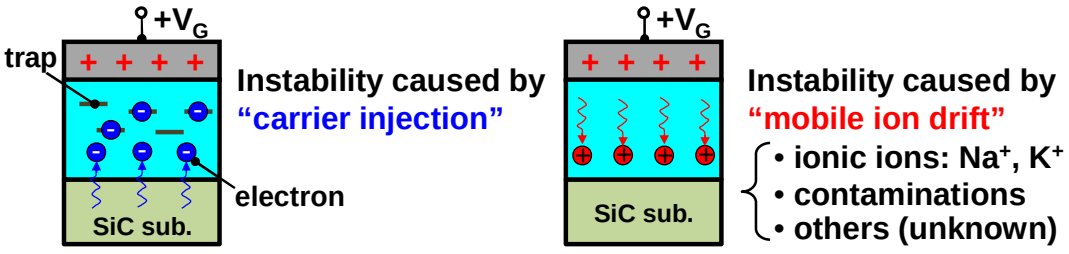

Fig. 1-19 Schematic illustration represents BTI in SiC-MOS devices. The two main origins for BTI such as carrier injection (left) and mobile ion drift (right) at high temperature change the distribution and amount of charge density in the oxides.

Moreover, the solid evidences, *i.e.* the sources of mobile ions in the thermal oxide on SiC are still uncertainly known.

As a stable power devices with acceptable operating characteristic are concerned for utilizing in the fail-safe operations, *e.g.*, fail-safe design in automobiles, safety operation in power conversion equipment. The manufacturer should perfectly fabricate devices with reducing in the mobile ion influences.

1-5 Purpose of This Study

As mentioned earlier in this introduction chapter, silicon carbide (SiC), a wide-bandgap semiconductor with superior physical properties have been extensively focused on the advancement of SiC-based power MOS devices that are going to be employed in the real-life applications, in the near future. Still, there are some remained issues needed to investigate their principal evidences especially on BTI, and then find the efficient strategies for solving these difficulties. For decades, BTI have been extensively studied for Si-based MOS technology. Nevertheless, only few studies of BTI in SiC-MOS devices have been reported nowadays. Even though, it is firmly believed that the mechanisms of BTI in SiC are considered to differ from that in Si, more studies are needed to disclose supported evidences especially the mobile ion drift phenomena in SiC-MOS devices. The main purpose of the study is to manifest for better understanding and providing the different aspects for BTI in SiC-MOS devices. This doctoral dissertation is summarized based on our journal publications with the connection of each section shown in Fig. 1-20.

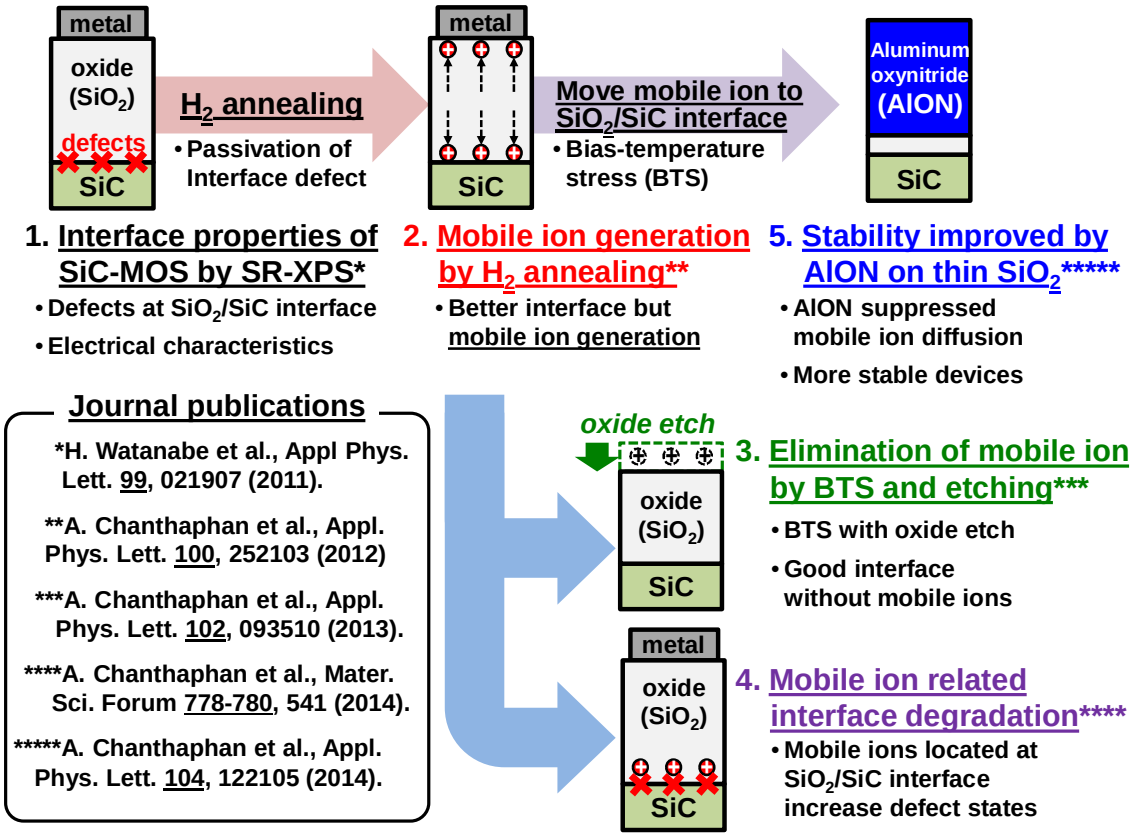

Fig. 1-20 The overview of this doctoral dissertation that is illustrated based on the international journal publications.

Chapter 2 discusses about the intrinsic interface defects formed by thermal oxidation of 4H-SiC. Chemical bonding states very closed to the thermal SiO_2/SiC interface are studied by synchrotron radiation photoelectron x-ray photoelectron spectroscopy (SR-XPS) together with electrical measurements of SiC-MOS capacitors. The C-rich transition layer is examined by means of core-level spectra of Si 2p and C 1s before and after *in situ* annealing. Moreover, the physical and electrical interface degradations of SiC-MOS devices, such as intermediate chemical states and fixed charge just at the oxide interface, are found to be introduced as a function of the oxide thickness. Lastly, the band alignments of SiO_2/SiC systems with high-temperature FGA are evaluated in term of reliability.

Chapter 3 focuses on unusual mobile ion formation and its impacts on BTI in 4H-SiC MOS devices. Although the defects reported in Chapter 2 can be passivated by high-temperature FGA, the C-V characteristics of these devices show mobile ion drift phenomena at high-temperature measurement. To identify the crucial factors in the mobile ion generation, we perform an extensive investigation on the electrical characteristics of 4H-SiC MOS capacitors fabricated with varying in Ar-POA and FGA conditions. The BTS experiment for evaluating the mobile ion concentration is then conducted to estimate the amount of mobile ion concentration. Finally, depth profiles of carbon and hydrogen atomic concentration were analyzed for the SiO_2/SiC samples showing mobile ion effects by secondary-ion mass spectrometry (SIMS) to clarify the formation mechanism of mobile ions.

Chapter 4 provides a better understanding the mobile ion effects in thermally grown SiO_2 on 4H-SiC substrates. The unique generated mobile ions by FGA showed in Chapter 3 are further controlled their polarity, density, and distribution. This chapter represents mobile ion elimination method based on BTS combining with terrace shape oxide etching. The fabricated SiC-MOS capacitors with or without mobile ion elimination provide insight into the BTI features.

A stretch-out of 1 MHz C-V curves due to the electron trapping into interface states is observed only for samples containing mobile ions at the SiO_2/SiC interfaces in the Chapter 4. In Chapter 5, impacts of mobile ions on interface properties are further examined for both samples with and without mobile ions. Based on several techniques such as Terman, conductance, C-ψ_s method for D_{it} estimation, it was found that mobile ions at the interfaces degrade the quality of SiO_2/SiC interfaces. Lastly, the modulation of band offsets by mobile ions is again shown by analyzing the SR-XPS spectra.

In Chapter 6, significant improvement of BTI characteristics is shown with AlON dielectrics deposited on thin thermal oxides. Diffusivity of the mobile ions inherent to

FGA-treated SiO_2/SiC structures is investigated in deposited SiO_2 and high-*k* AlON gate dielectrics. The AlON/SiO_2 stacked dielectric is found to be beneficial not only for reducing gate leakage current but also for suppressing diffusion of mobile ions. As a result, the devices exhibit stable electrical characteristics even under strong electric fields and high temperatures.

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Chapter 2 Synchrotron X-ray Photoelectron Spectroscopy Study and Its Correlation with Electrical Performance

In this chapter, intrinsic atomic defects at as-oxidized SiO_2/4H-SiC(0001) interfaces were investigated for understanding the electrical degradation of thermally grown SiC-MOS devices. The correlation between atomic structure and the electrical properties by synchrotron x-ray photoelectron spectroscopy (XPS) together with electrical measurements of SiC-MOS capacitors will provide insight into the mechanism of electrical degradation. We found that the oxide interface was dominated by Si-O bonds and that there existed no distinct C-rich layer beneath the SiC substrate despite literature. In contrast, intermediate oxide states in Si core-level spectra attributable to atomic scale roughness and imperfection just at the oxide interface increased as thermal oxidation progressed. Furthermore, the relationship between defects and band alignments of the SiO_2/SiC structures were also studied based on XPS analysis.

2-1 Introduction

Silicon carbide, which exhibits a wider band gap as well as a superior breakdown field and thermal conductivity over conventional Si, has gained considerable attention for future power electronics [1]. Among the various types of power devices, metal-oxide-semiconductor field-effect transistors (MOSFETs), which provide a normally-off characteristic should become an essential component for next generation green electronics. As stated, with the exception of Si, SiC is the only compound semiconductor that yields SiO_2 insulators with thermal oxidation. This makes the device fabrication process easier compared with those for other wide band gap semiconductors. Carbon impurities within the oxides diffuse out in the form of carbon oxides during high temperature oxidation, but a small amount of carbon impurities remains within the oxide and at the SiO_2/SiC interface. Consequently, the electrical degradation of SiC-MOS devices is the most crucial obstacle to the implementation of SiC-based power electronics.

The fundamental aspects of Si oxidation have been intensively investigated because of their importance in controlling growth kinetics and the electrical properties of

Si-MOS devices [2-6]. Despite its simplicity, understanding Si oxidation has required considerable efforts, in which advanced characterization methods, such as high-resolution transmission electron microscopy (TEM) [2,3] and x-ray photoelectron spectroscopy (XPS) [4,5], have been used. It was proven that the thermal oxidation of Si surfaces proceeds in a layer-by-layer manner and yields an abrupt interface in terms of composition and atomic bonds [5,6]. Owing to the low interface state density (D_{it}) and small fixed oxide charge density (Q_{ox}), sufficiently high carrier mobility has been achieved even for modernly scaled Si-MOSFETs.

Unlike mature Si-MOS technology, a plausible oxidation model of a SiC surface and practical method for terminating electrical defects at the SiO_2/SiC interface have yet to be established. High-resolution TEM observation indicated several nm-thick transition layers with an extremely high excess carbon concentration around 20% beneath the SiO_2/SiC interface, which is on the SiC bulk side [7-9]. Although the non-stoichiometric bulk region seems to account for the mobility degradation of SiC-MOSFETs [9], cross-sectional TEM analysis sometimes suffered from difficulties in sample preparation, and a recent report based on an ion scattering technique pointed out a near-perfect stoichiometric SiC region [10]. High-resolution XPS experiments using synchrotron radiation also detailed the interface bonding features and chemical composition of the SiO_2/SiC system, but most previous literature focusing on the initial stages of SiC oxidation [11,12] provide no direct information on the above mentioned. Furthermore, the presence of carbon-related adsorbates makes it difficult to determine the bonding structure at the SiO_2/SiC interface because the carbon core level signal from the surface adsorbate overlaps with that from the interface. In this study, we re-examined the thermal oxidation of a 4H-SiC(0001) surface by high-resolution synchrotron radiation XPS. By using *in-situ* vacuum cleaning, direct insight into the bonding features of the SiO_2/SiC interface was obtained, and its correlation with the electrical properties of SiC-MOS capacitors was examined. Lastly, we also discuss an impact of interface defect passivation by hydrogen incorporation on the band offset modulation at SiO_2/SiC interface in order to gain a guideline for developing high-performance and highly reliable power devices.

2-2 Experimental

2-2-1 Preparation of thermally grown SiO_2/SiC samples for XPS

The procedure to prepare the thermal SiO_2/SiC samples is described in Fig. 2-1. The starting substrate used in this study was as-grown 4°-off-angle 4H-SiC(0001) wafer

with an n-type epitaxially grown layer. After RCA and subsequent native oxide removal with a diluted hydrofluoric acid (HF) solution, thermal oxidation was conducted in dry oxygen ambient using a conventional tube furnace at 1100°C. Thin and thick thermal oxides ranging from a few to 40 nm were prepared by changing the oxidation time.

Synchrotron XPS analysis was performed using photon energy of 686.5 eV at BL23SU in the SPring-8 (Super-Photon-ring 8 GeV) [13]. The photoelectron take-off angle was normal to the sample surface (TOA=90°). A thick thermal oxide was thinned using an HF solution prior to XPS analysis while a thin oxide sample was directly examined after dry oxidation. To remove surface contamination due to air exposure and wet treatment, some of the samples were annealed *in situ* in an analysis chamber under an ultra-high vacuum condition. Corresponding SiC-MOS capacitors were fabricated with the top aluminum electrode evaporated through a shadow mask after post oxidation annealing at 900°C in argon ambient. Electrical properties, such as the D_{it} and Q_{ox} of the SiO_2/SiC interface, were extracted from the high-frequency capacitance-voltage (C-V) characteristics of SiC capacitors. The D_{it} value was extracted with the Terman method, and the Q_{ox} was deduced from the flatband voltage (V_{FB}) shift that depends on the oxide thickness [14].

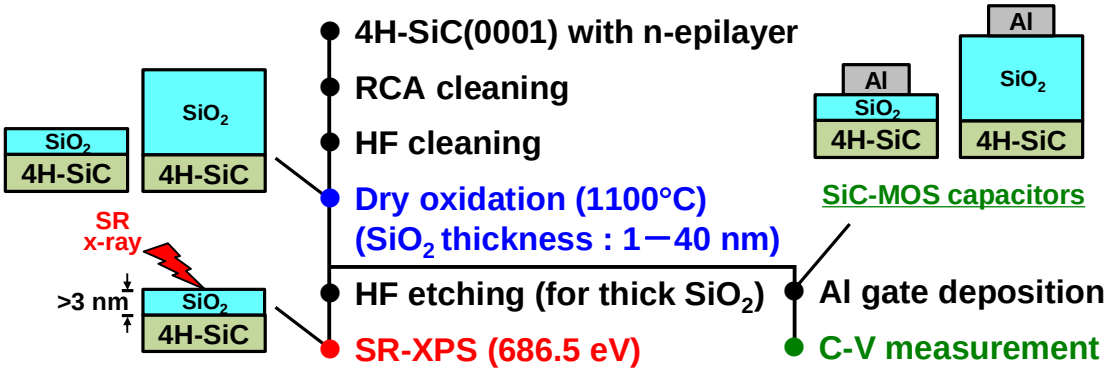

Fig. 2-1 Process diagram representing SiO_2/SiC sample preparation for XPS and SiC-MOS capacitors fabrication for electrical characterization. A few nm to 40 nm-thick thermal oxides were formed by dry oxidation at the same temperature (1000°C). Some samples were subjected to deposit Al gate electrodes for C-V measurements. In order to perform XPS, the thick oxides were etched by HF solution resulting in thin oxides with thickness less than 3 nm.

2-2-2 X-ray photoelectron spectroscopy (XPS)

2-2-2-1 Basic principles

X-ray photoelectron spectroscopy (XPS) is a spectroscopic technique used for analyzing a material surface based on the detection of electrons produced by the photoelectric effect. An incident x-ray photon with constant energy bombards with the electron at the inner shell levels (*a.k.a.* core levels) to release from the materials as photoelectrons. Regarding the x-ray source, Mg Kα (hν = 1253.6 eV) and Al Kα (hν = 1486.6 eV) are frequently used to excite the shallow core-level electrons. A kinetic energy distribution of photoelectrons ejected from the top surface to a few nanometers (less than 10 nm) inside the materials is measured by using a spectrometer that is the combined electron energy analyzer and detector system. XPS spectra provide the information of the specimen on the chemical state and state density of the core electrons. Figure 3.14 shows the energy relationships in the photoelectron spectrum. The kinetic energy of photoelectron (E_K) governing the interaction of monoenergetic x-ray source (hν) with a core electron is explained by:

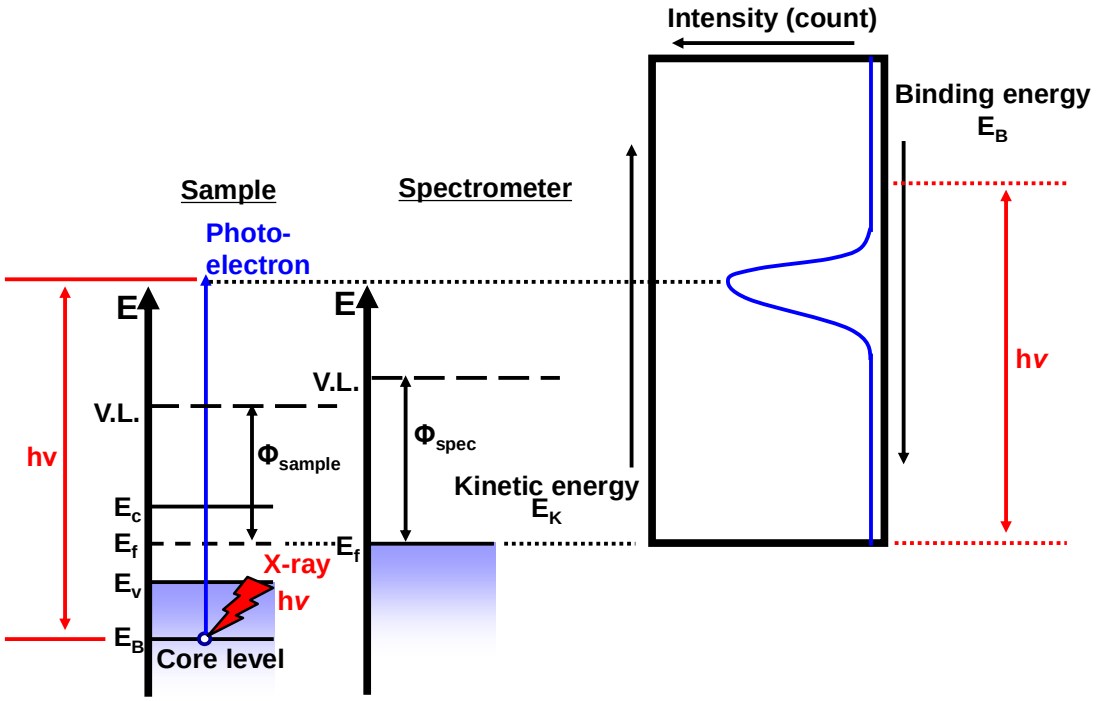

Fig. 2-2 The energy diagram corresponding the x-ray photoelectron spectrum. The incident x-ray photon excites the electron at the core level to escape from the sample surface with kinetic energy. The photoelectron is then detected by the spectrometer to generate XPS spectrum.

$$E_K = h\nu - E_B - \varphi_{spec}, \quad (2.1)$$

where E_B is the binding energy of the core electrons and φ_{spec} is the work function of photoelectron spectrometer. Since XPS spectrum is very sensitive to the chemical state of inner-shell electrons, it is possible to observe a change in the energy peak position when the state is altered, which is called chemical shifts. Hence, XPS is regularly employed to examine the chemical defects and their bonding configurations at SiO_2/SiC interfaces [11,12].

2-2-2-2 Energy bandgap evaluation by energy loss spectra

The energy bandgap (E_g) of the insulating film can be determined by using loss energy signal of core-level spectra. It is possible for photoelectrons to lose their kinetic energies when escaping from the inner core levels because of some inelastic scattering processes, *i.e.* plasmon (collective oscillation) and interband transition (band-to-band)

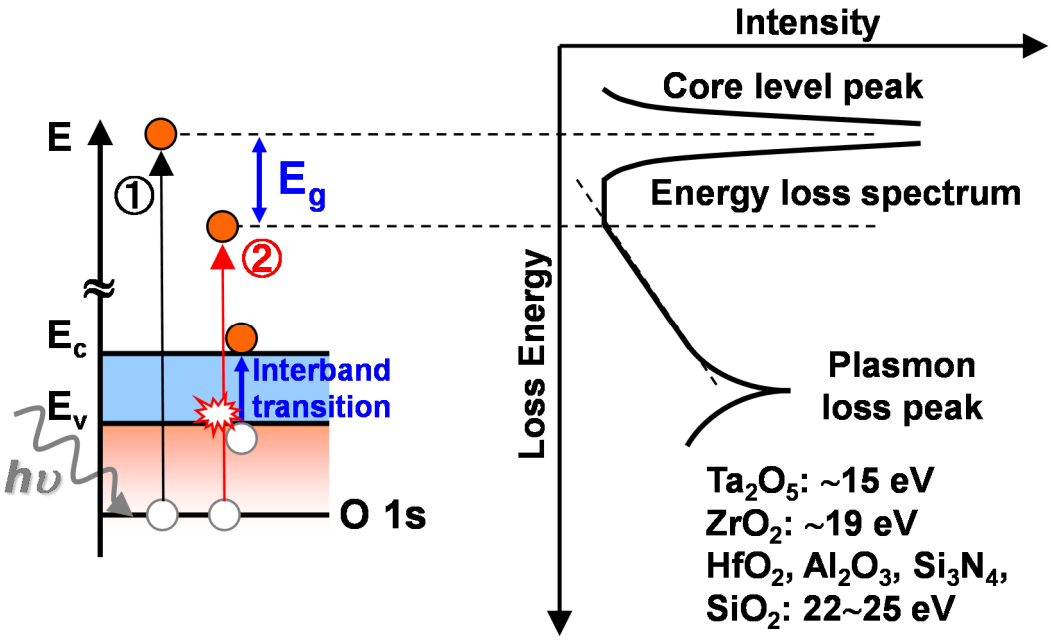

Fig. 2-3 Relation of the energy diagram with the O 1s photoelectron energy loss spectrum subtracted by the O 1s core level peak (denoted by ①). The energy bandgap (E_g) of oxide materials is estimated by interpolating straight line on low binding energy side of the energy loss spectrum and then determining the threshold loss energy equivalent to E_g (denoted by ②). The plasmon loss peak is centered around 15 eV for Ta_2O_5, 19 eV for ZrO_2 and 22~25 eV for HfO_2, Al_2O_3, Si_3N_4, and SiO_2 [15].

excitation. For example, the energy loss spectrum for O 1s photoelectrons provides further understanding on the E_g of oxides on Si [15]. As shown in Fig. 2-3, the energy loss peak by plasmon excitation is approximately 22 ~ 25 eV for the HfO_2, Al_2O_3, Si_3N_4 and SiO_2 film which is apparently greater than the excitation energy for interband transition. Therefore, the E_g is equal to the threshold energy of O 1s loss spectrum where the loss energy phenomena due to the band-to-band excitation begin to be more pronounced than one due to plasmon excitation.

2-2-2-3 Evaluation of energy band diagram

As mentioned in the introduction chapter, the charge trapping into the gate oxides causing gate voltage shifts can be suppressed by two approaches: reducing bulk oxide traps and minimizing the leakage current passing through the gate oxides. In SiO_2/SiC structures, a large leakage current is determined by a small energy barrier for electron injection, so-called conduction band offset (ΔE_c) (see Fig. 1-6(b)). Even though, the evaluation of ΔE_c of SiO_2/SiC by using spectroscopy of internal photoemission (IPE) was previously studied [16], the leakage current through the defects at SiO_2/SiC interfaces directly alters the measurement accuracy. By using XPS spectra, it is possible

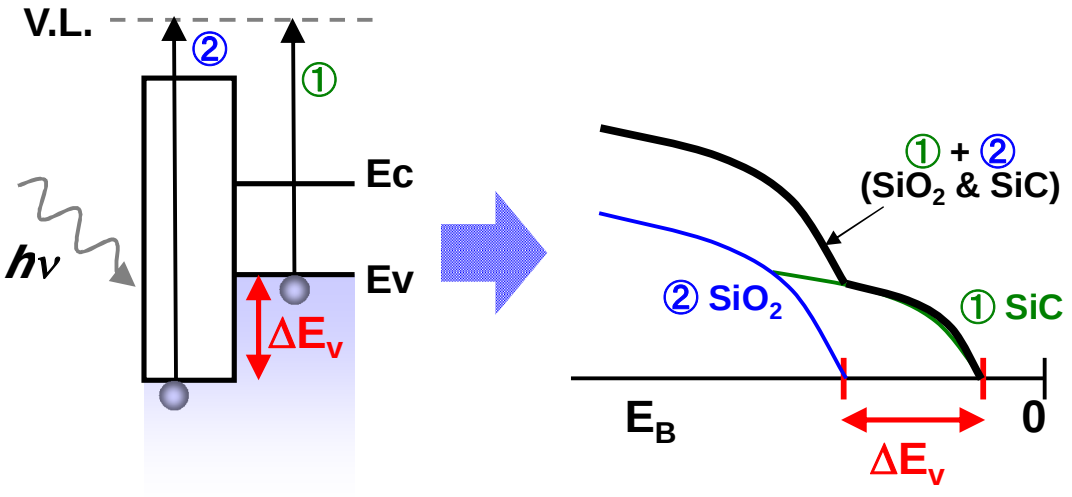

Fig. 2-4 Relation of the energy diagram with valence band spectra obtained from the photoelectrons excited in the valence bands of separated structures: the SiC substrate (denoted by ①) and the bulk SiO_2 (denoted by ②). In fact, the bulk SiO_2 valence spectrum is indirectly obtained by subtracting the combined intensity of SiO_2/SiC heterojunction (denoted by ①+②) with intensity from the SiC substrate. The difference in threshold energy signal in the lower E_B side provides the valence band offset (ΔE_v) that is then inferred the ΔE_c as described in Fig. 2-5.

to determine the band offsets based on valence band spectrum analysis without limitations on this challenge.

As shown in Fig. 2-4, the ΔE_c of SiO_2/SiC heterojunction structures can be indirectly evaluated by analyzing the photoelectrons released from the valence bands [15]. According to the valence spectra obtained separately for the SiO_2/SiC system and the SiC substrate, the signal components of bulk SiO_2 can be predicted by deconvoluting the combined signals. The uppermost valence energy difference of separated valence spectra coming from SiO_2 and SiC is equivalent to the valence band offset (ΔE_v). Finally, all required parameters *i.e.* E_g of SiO_2 and ΔE_v obtained from XPS analysis mentioned above are used to calculate ΔE_c by:

$$\Delta E_c = E_{g,SiO_2} - \Delta E_V - E_{g,SiC} \qquad (2.2)$$

where the theoretical value of energy bandgap of 4H-SiC ($E_{g,SiC}$) is 3.26 eV (Fig. 2-5).

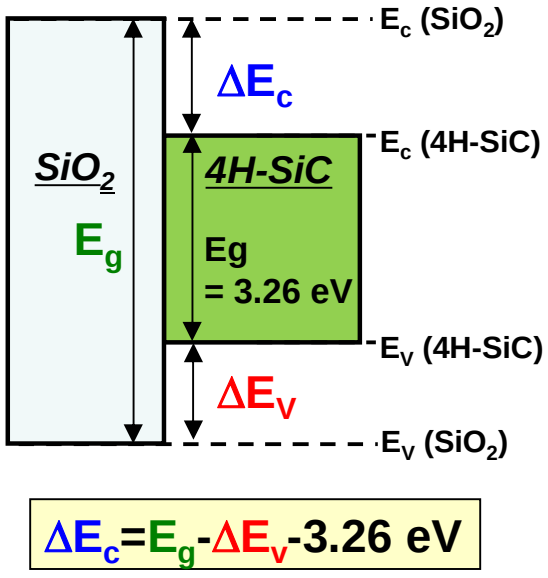

Fig. 2-5 Band diagram of SiO_2/4H-SiC structures represents parameters required for estimating ΔE_c by using Eq. 2.2 where the E_g of SiO_2 estimated by core energy loss spectra (see Fig. 2-3) and ΔE_V estimated by the valence band spectrum analysis (see Fig. 2-4).

2-2-2-4 Synchrotron radiation XPS

In order to investigate the surface states of the thermal oxide film of SiC in oxide/SiC interfaces in detail, a synchrotron radiation XPS (SR-XPS), high resolution

XPS technique was carried out using the apparatus for surface reaction dynamics studies utilizing soft x-ray beamline (BL23SU). The apparatus shown in Fig. 2-6 was installed by Japan Atomic Energy Agency (JAEA) at SPring-8, the biggest SR radiation facility in Japan [13]. The sensitivity of high-resolution XPS analysis is increased with the use the SR source because the optimum excitation energy can be precisely controlled. Furthermore, the rapid measuring is possible with better quality of XPS spectra because of high intensity x-ray incident, expressed as large photon density of several orders of magnitude higher than that of conventional x-ray source [17].

In this study, monochromatic incident x-ray with photon energy of 686.5 eV was chosen to detect core-level spectra, *i.e.* Si 2p, O 1s and C 1s. The photoelectron take-off angle was 90°.

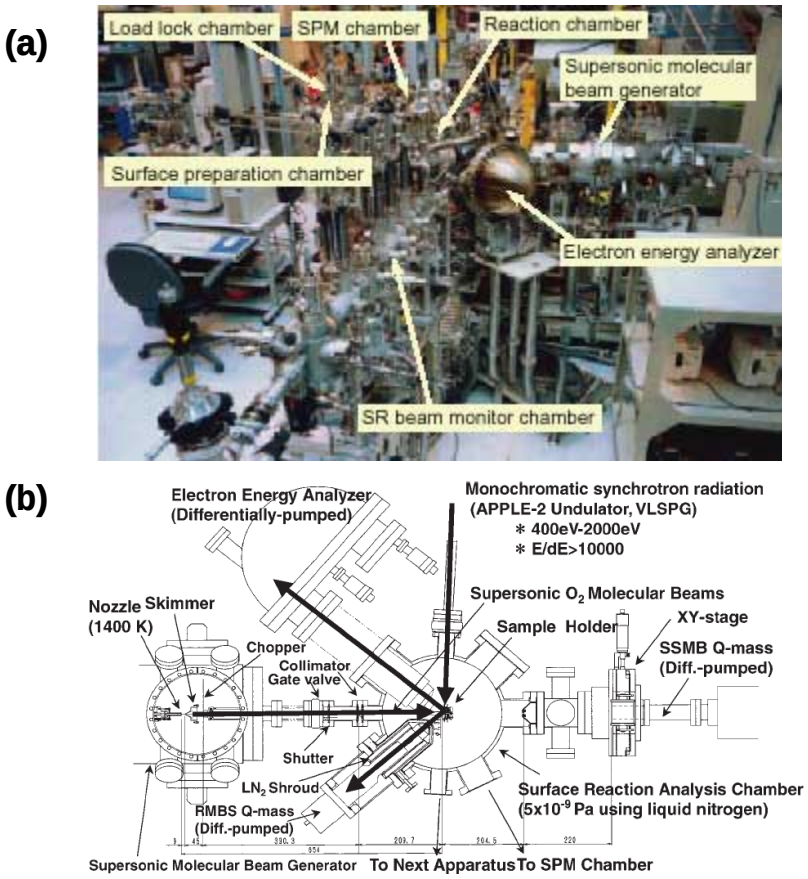

Fig. 2-6 (a) The apparatus for XPS studies using soft x-ray beamline (BL23SU) constructed at SPring-8. (b) The illustration shows the apparatus setup for synchrotron XPS analysis. The SR beam is introduced into the surface reaction analysis chamber and then collide with a sample surface. Photoelectrons from the sample surface are detected by an electron-energy analyzer [13].

2-3 Results and Discussion

2-3-1 Core-level spectra and effects of *in situ* vacuum annealing

Figure 2-7 represents changes in photoelectron spectra as dry oxidation progresses on the 4H-SiC(0001) surface at 1100°C. Peak intensity was normalized with the bulk signal, that is, the Si-C or C-Si bonds originating from SiC substrates. In addition, C-V measurement of the corresponding Al/SiO_2/SiC capacitors revealed that oxidation for 10 and 30 min yielded roughly 3.5 and 5.7-nm-thick oxides, respectively. Oxide growth on the SiC surfaces was confirmed with an increase in both the chemical shift component in the Si 2p core-level spectra at around 104.5 eV (Fig. 2-7(a)) and the O 1s signal (Fig. 2-7(b)). As previously reported, ideal hydrogen passivation of the SiC surface with a HF solution was barely obtained, and the initial sample surface after wet cleaning was

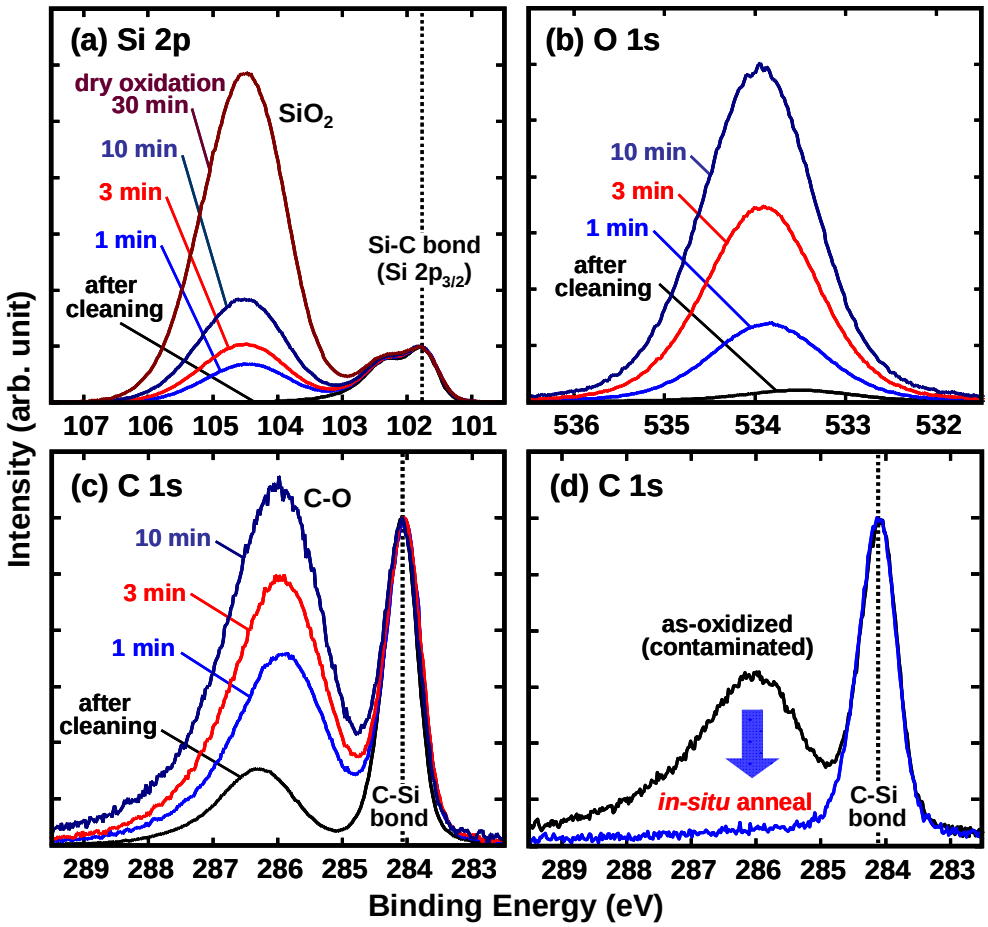

Fig. 2-7 Core-level spectra obtained from the cleaned and oxidized 4H-SiC(0001) surfaces with synchrotron radiation of 686.5 eV. Change in fine spectra of (a) Si 2p, (b) O 1s, and (c) C 1s core levels before and after oxidation. (d) C 1s spectra recorded before and after *in situ* vacuum annealing at 500°C.

partially oxidized and contaminated with adsorbates [18]. This implies that a chemical shift component of C 1s spectra involves unavoidable signals due to surface contamination (Fig. 2-7(c)). To overcome this obstacle, *in situ* vacuum annealing was conducted prior to XPS analysis in the analysis chamber. Consequently, as shown in Fig. 2-7(d), the C 1s chemical shift component originating from carbon-oxides was totally removed by vacuum annealing at 500°C. Since stable chemical bonds existing at the SiO_2/SiC interface are hard to decompose under a moderate temperature, we attributed the carbon-oxide signal to surface contamination. The results shown in Fig. 2-7(d) clearly demonstrate that atomic bonding at the thermally grown SiO_2/SiC(0001) interface is dominated by Si-O bonds and that carbon impurity with its oxide form located near the interface is below the detection limit of XPS analysis (about sub-1 atomic percent in general). Moreover, a carbon-rich layer including (Si-)O-C bonds can be ruled out as the dominant physical origin of the transition layer near the SiO_2/SiC interface.

2-3-2 Amounts of intermediate oxide states at SiO_2/SiC interfaces

To further investigate atomic bonding feature, a Si 2p signal was analyzed by taking into account spin-orbit splitting. Figure 2-8(a) shows typical deconvoluted Si $2p_{3/2}$ and $2p_{1/2}$ peak components obtained with the manner adopted in the previous research on SiO_2/Si interfaces [4,5]. The Si $2p_{3/2}$ spectra taken from SiO_2/SiC were deconvoluted into five components originating from bulk SiC and SiO_2 portions together with intermediate oxide states (Si^{1+}, Si^{2+}, Si^{3+}). High-resolution XPS analysis allows us to detect a small amount of intermediate states from an atomically abrupt oxide/substrate interface, and, in addition, these intermediate components can be a good indicator of structural imperfection at SiO_2/SiC interfaces. As shown in Figs. 2-8(b) and 2-8(c), we obtained a reasonable curve fitting with these components and confirmed that the total amount of the intermediate states is sufficiently small compared with that of thin thermal oxides (for example, 3.5-nm-thick for 10 min of oxidation, see Fig. 2-8(c)). From these results, it is concluded that the physical thickness of the transition layer is as thin as a few atomic layers, which corresponding to areal density of Si-O bonds in the range of a few times 10^{15} cm^{-2}. This indicates the formation of a near-perfect SiO_2/SiC interface and coincides well with a recent report based on high-resolution medium energy ion scattering (MEIS) [10]. However, unlike in the SiO_2/Si interface, which exhibits a perfect interface regardless of oxide thickness, we observed a slight increase in the total amount of intermediate oxide states for the SiO_2/SiC interface (Fig. 2-8(d)).

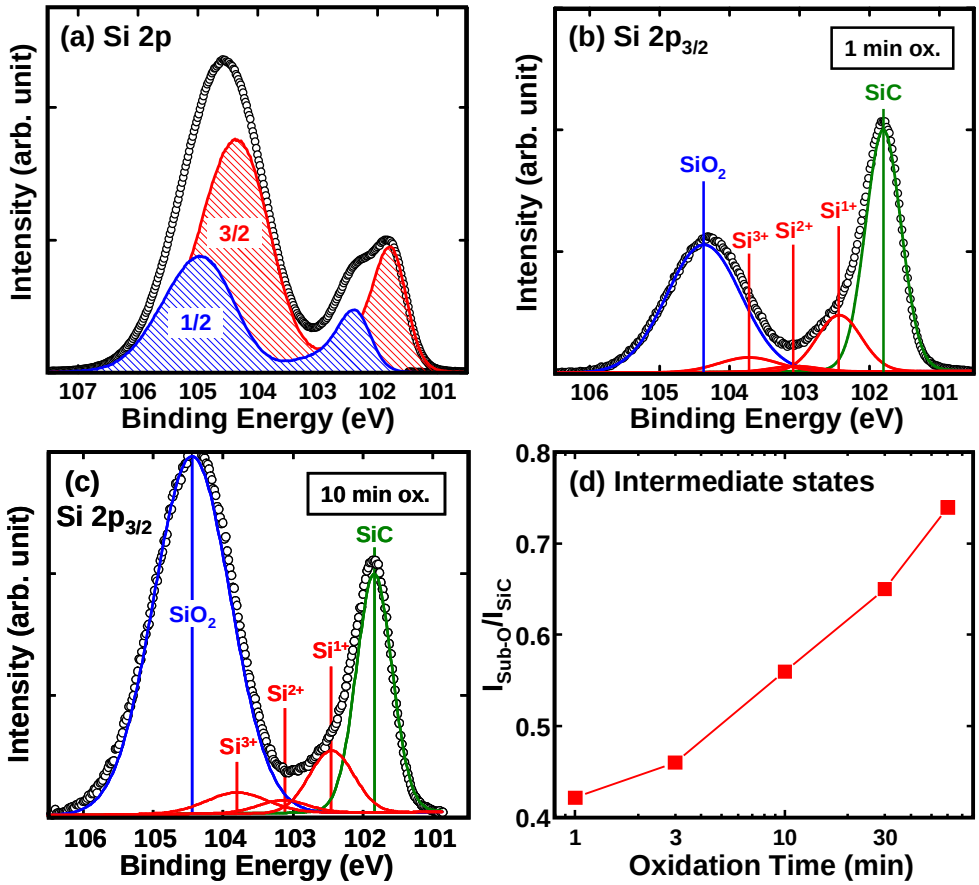

Fig. 2-8 Characterization of Si 2p core-level spectra by taking into account spin-orbit splitting. (a) Example of peak deconvolution with $2p_{3/2}$ and $2p_{1/2}$ components. (b) and (c) show results of curve fitting of Si $2p_{3/2}$ core-level spectra with bulk SiC and SiO_2 signals and intermediate oxide states for SiO_2/SiC samples prepared by 1-min and 10-min oxidation, respectively. (d) Change in the total amount of intermediate oxide states in Si $2p_{3/2}$ spectra, in which the intensity ratio between the intermediate state and the bulk signal was plotted as a function of oxidation time.

2-3-3 Atomic composition of oxide interface

The interface structure beneath the 40-nm-thick thermal oxide (1100°C, 12 h) was also examined by wet etching the thick oxide with an HF solution and subsequently measuring it by SR-XPS. Figure 2-9(a) shows C 1s and deconvoluted Si $2p_{3/2}$ core-level spectra taken after wet etching. The measured intensity was normalized by Si-C peak signals (C^{0+}). As shown in the inset table of Fig. 2-9(a), the Si $2p_{3/2}$ spectra obtained

before (as-epi.) and after thermal oxidation (thick oxide) revealed a comparable near-perfect interface with minimum composition of intermediate oxide states ([Si^{1+}]/[C^{0+}]). Furthermore, with the exception of a dominant C-Si bulk signal and broad oxide component from the surface contamination shown in Fig. 2-9(b), no distinct peak

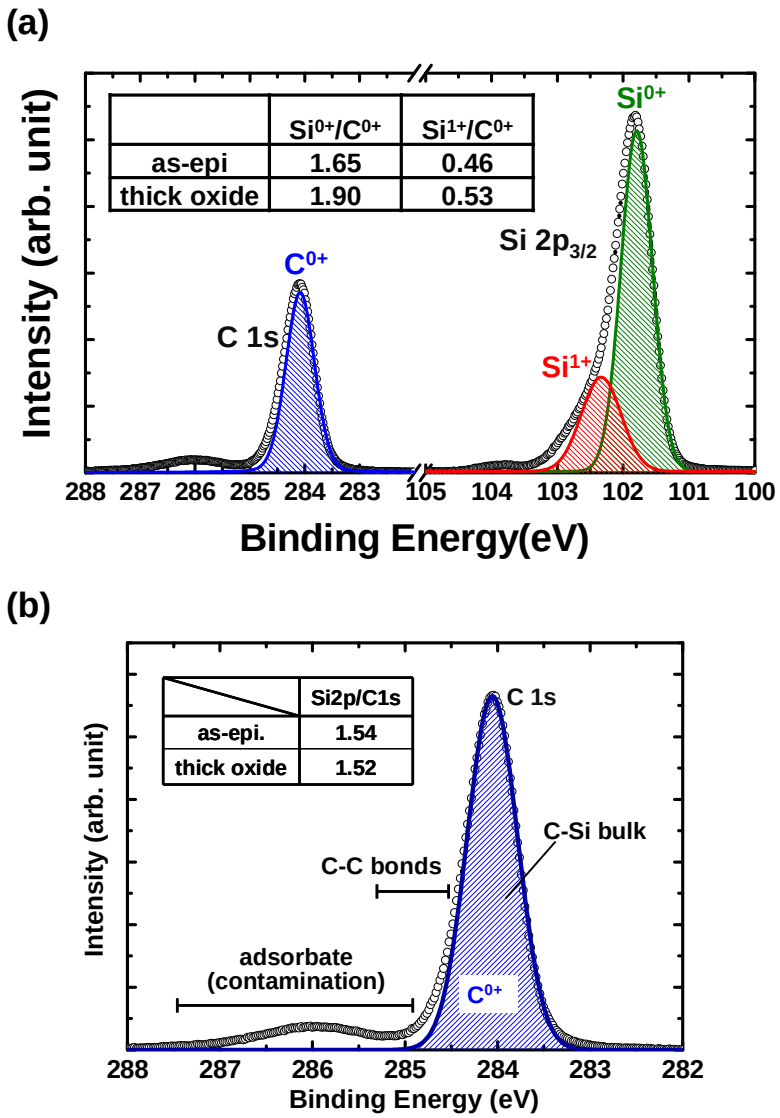

Fig. 2-9 The core-level spectra of (a) C 1s and Si $2p_{3/2}$ obtained after removal of 40-nm-thick thermal oxide by using wet etching. The inset shows intensity ratios between intermediate oxide states (Si^{1+} and Si^{0+}) and C-Si bonds (C^{0+}) peak signals before (as-epi.) and after thermal oxidation (thick oxide). Detail spectrum of only (b) the C 1s is shown with the hatched area to indicate C-Si bonds from the SiC bulk portion. The expected binding energy position originating from the surface adsorbate and C-C bonds is indicated. The inset also shows the intensity ratio between the Si 2p and C 1s signals.

assigned to carbon clusters (C-C bonds) was identified even for the thick oxide interface. The composition of the bulk SiC region estimated from the intensity ratio ([Si 2p]/[C 1s]) was almost identical to that of the initial as-grown SiC surface as listed in the inset of Fig. 2-9(b). These experimental results mean that, despite previous literature based on TEM observation, there exists no thick carbon-rich layer of a high atomic percentage at the SiO_2/SiC interface and that a near-perfect interface dominated by Si-O bonds is formed even for the thick thermal oxidation of the SiC(0001) surface.

2-3-4 Correlation between electrical and atomic bonding properties

Next, the electrical properties of the corresponding SiO_2/SiC interfaces were evaluated from the C-V characteristics of SiC-MOS capacitors with various oxide thicknesses. Figure 2-10 summarizes the changes in D_{it} and V_{FB} values. Since post-treatment, such as nitrogen and hydrogen incorporation, was not conducted in this experiment, high D_{it} over 10^{12} cm^{-2} eV^{-1} was extracted at an energy level of E_c - E = 0.36 eV (E_c: conduction band bottom). The high D_{it} value indicates degradation of the electrical properties of the SiO_2/SiC interface, especially for thick thermal oxides. In addition, the positive V_{FB} shift in the C-V curves implies the existence of a negative fixed charge within the gate oxides. Assuming that the fixed charge is located at the SiO_2/SiC interface, the Q_{ox} of the SiC-MOS devices was estimated to be 2.3 x 10^{11} cm^{-2} for oxides thinner than 15 nm and 1.2 x 10^{12} cm^{-2} for thick oxides, meaning that the fixed charges also accumulated at the interface as dry oxidation progressed.

The correlation between electrical degradation and the atomic bonding feature of the SiO_2/SiC interfaces shown in Figs. 2-8(d) and 2-10 raises the intrinsic problem of SiC oxidation. This is consistent with the common understanding of SiC-MOS devices, whereas our synchrotron XPS analysis excludes the several-nm-thick transition layer having excess carbon [7-9] as a physical origin of the electrical degradation. Instead, we think that the electrical defects at the interface, such as D_{it} and Q_{ox}, are partly ascribed to the atomic scale roughness and imperfection identified with the intermediate oxide states in the Si 2p spectra. Moreover, considering the significant mobility reduction in SiC-MOSFETs, we should take into account the various forms of carbon interstitials forming local C-C dimers located on the SiC bulk side as a possible origin of the electrical defects [19]. Therefore, it is concluded that, for improving the performance of SiC-based MOS devices, we should focus our attention on the atomic bonding feature and carbon impurities within the channel region rather than the thick transition layer near the SiO_2/SiC interface.

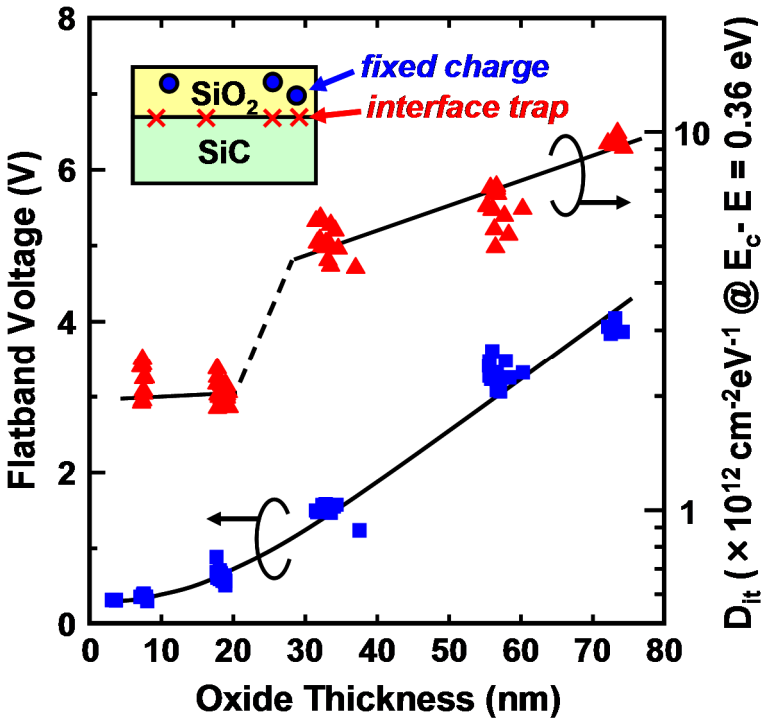

Fig. 2-10 Summary of electrical properties of SiC-MOS capacitors fabricated by dry oxidation at 1100°C. Horizontal axis represents oxide thickness extracted from measured maximum capacitance. The D_{it} values were estimated from high-frequency C-V curves using the Terman method. The Q_{ox} of the SiC capacitors was deduced from the V_{FB} shift in the C-V curves [14].

2-3-5 Changes in band offset due to passivation of interface defects

As mentioned earlier, ΔE_c between SiO_2 and SiC is inherently smaller than that between SiO_2 and Si, leading to considerable gate leakage and reliability degradation. Furthermore, it has also been reported that ΔE_c depends on the substrate orientation [20] and hydrogen incorporation [21]. In this section, the energy band alignments of thermally grown SiO_2/SiC structures were investigated by means of SR-XPS. Additional XPS samples were fabricated as follows. After the 40-nm-thick SiO_2 layer was thermally grown on 4H-SiC(0001) at 1150°C for 4 h, POA was performed in Ar ambient at 1150°C for 1 h. High-temperature FGA in 3% H_2/ N_2 ambient was done at 800°C for 30 min and then at 450°C for 30 min. For SR-XPS measurements, SiO_2 layer was thinned down to 3 nm by dipping in a diluted HF solution. To determine the energy band alignments of SiO_2/SiC structures, bandgaps of the SiO_2 layers and valence band offsets at the interface were examined by analyzing of core-level loss and valence band spectra.

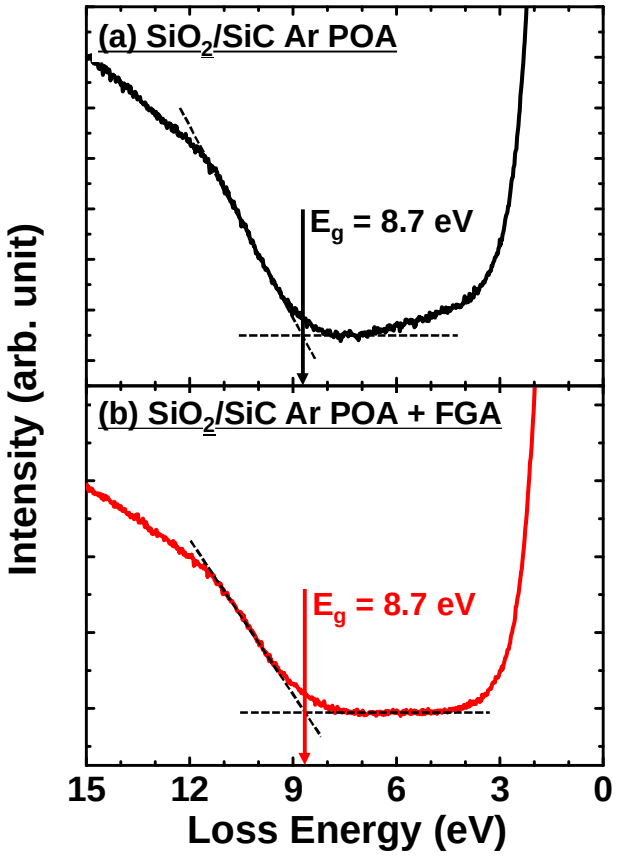

Fig. 2-11 O 1s energy loss spectra for SiO_2/4H-SiC structures (a) without and (b) with FGA at 800°C. The onset of the excitation from the valence to conduction bands (bandgap) can be determined from the loss spectra.

Figure 2-11 shows O 1s energy loss spectra taken from SiO_2/SiC structures with and without FGA and from a reference SiC surface. Since some of the photoelectrons from the sample were subjected to energy loss due to band to band excitation, energy loss spectra were observed at the higher binding energy (lower kinetic energy) from O 1s core-level. Energy bandgaps of these oxides deduced from O 1s energy loss spectra were identical (8.7 eV), indicating the negligible impact of FGA on bulk properties of the SiO_2 layer. Figure 2-12 shows valence band spectra taken from the same samples. In the measured valence spectra for the SiO_2/SiC structures, photoelectrons from SiO_2 layers overlapped with those from SiC substrates. Therefore, the deconvoluted valence band spectra for SiO_2 were determined by subtracting the reference SiC spectra from the SiO_2/SiC spectra. ΔE_v at SiO_2/SiC interface corresponds to the difference in the valence band maximum between SiO_2 and SiC determined by linear extrapolation of the leading edges of the measured SiC and deconvoluted SiO_2 valence band spectra. The obtained ΔE_c at SiO_2/SiC interface with FGA was found to be 0.05 eV smaller than that without

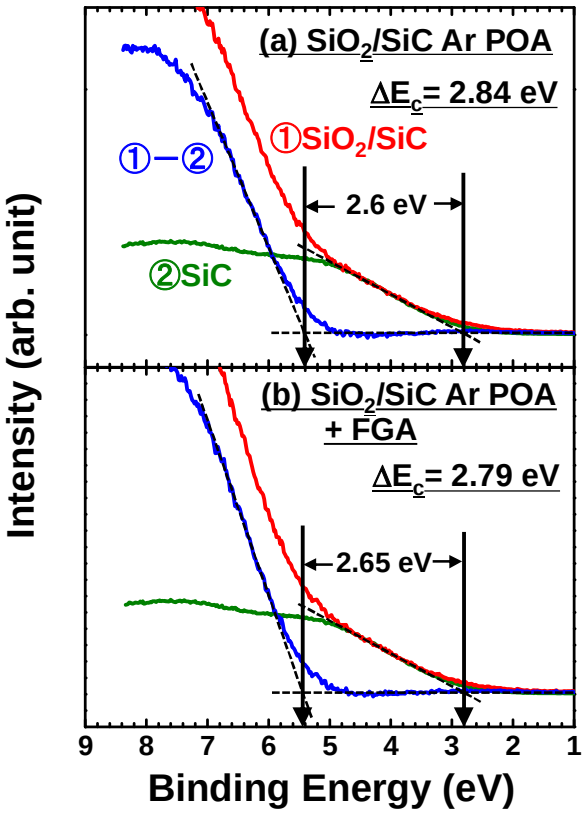

Fig. 2-12 Deconvoluted valence band spectra for SiO_2/4H-SiC(0001) structures (a) without and (b) with FGA at 800°C. Since valence band spectra were the sum of SiO_2 layer and SiC bulk, spectral deonvolution was performed using valence band spectrum taken from the reference SiC substrate.

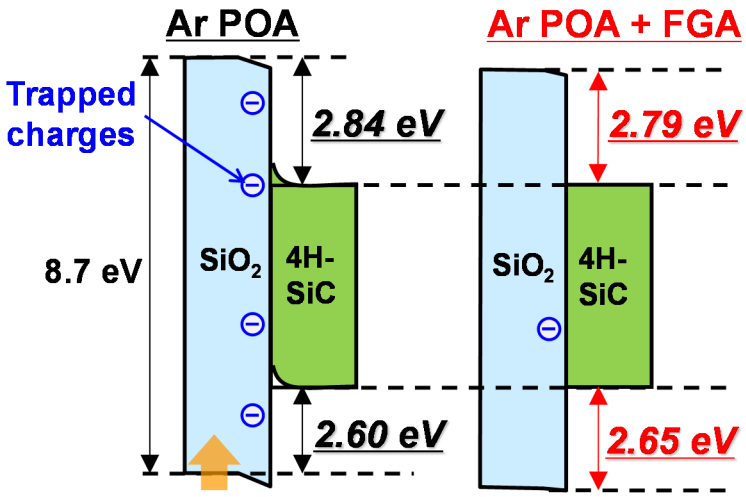

Fig. 2-13 Energy band alignments of thermally grown SiO_2/4H-SiC(0001) structures with high-temperature FGA at at 800°C determined by SR-XPS.

FGA. Thus, we can speculate that passivation of negatively charged defects by FGA caused a reduction in ΔE_c, as depicted in Fig. 2-13. From these results, it can be concluded that the tradeoff between interface quality and conduction band offset for thermally grown SiO_2/SiC structure needs to be considered for developing SiC MOS devices.

2-4 Summary

In summary, the fundamental aspects of thermal oxidation and oxide interface grown on SiC substrates were investigated by means of XPS using synchrotron radiation together with electrical measurements of SiC-MOS capacitors. High-resolution XPS analysis allows us to detect a small amount of intermediate states (Si^{1+}, Si^{2+}, Si^{3+}) from an atomically abrupt SiO_2/SiC interface and, in addition, these intermediate components can be a good indicator of structural imperfection at the interfaces. A reasonable curve fitting with these components in Si $2p_{3/2}$ spectra suggested that the total amount of the intermediate states be sufficiently small compared with that of thin thermal oxides. From these results, it is concluded that the physical thickness of the transition layer is as thin as a few atomic layers. Furthermore, C 1s core-level spectra taken from the oxidized SiC surface before and after removal of surface contamination by *in situ* vacuum annealing at 500°C indicate that atomic bonding at the thermally grown SiO_2/SiC(0001) interface is dominated by Si-O bonds and that carbon impurity with its oxide form located near the interface is below the detection limit of XPS analysis. This indicates the formation of a near-perfect SiO_2/SiC interface from a physical analysis point of view. The change in energy band alignment of thermally grown SiO_2/4H-SiC structures due to an interface defect passivation treatment was also investigated by using synchrotron radiation XPS. Although both negative fixed charge and interface state density in SiO_2/SiC structures were effectively reduced by high-temperature FGA, the ΔE_c at the SiO_2/SiC interface was decreased.

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Chapter 3 Investigation of Unusual Mobile Ion Generation in Thermal SiO_2 on 4H-SiC

In this chapter, generation and elimination of mobile ions in thermally grown SiO_2 on 4H-SiC(0001) were systematically investigated by electrical measurements of MOS capacitors. Although a tiny amount of carbon residues and related defects remained in as-oxidized SiO_2/SiC structures was observed in the previous chapter, the intrinsic positive mobile ions were additionally found to exist, leading to significant instability of SiC-MOS devices at high-temperatures. Post-oxidation annealing in Ar ambient mostly eliminates the mobile ions, but they are generated again by subsequent high-temperature forming gas annealing (FGA) in diluted hydrogen ambient despite the improved interface quality. The density of the mobile ions was determined to be several 10^{12} cm^{-2}. Possible physical origins of the mobile ions are discussed on the basis of the experimental findings.

3-1 Introduction

For the past several years, the development of Si-based power devices has been approaching its theoretical limit due to its inherent properties unsuitable for high-power and high-temperature operation. Because of this, silicon carbide (SiC), a wide-bandgap semiconductor material with superior physical and electrical properties, is required to substitute for Si [1]. In fact, SiC-based Schottky barrier diodes (SBDs) have already been commercialized, and its applications are expanding. In addition, SiC has another advantage in achieving power switching devices on the basis of metal-oxide-semiconductor (MOS) structures, because SiC is the only wide-bandgap semiconductor that can grow silicon dioxide (SiO_2) by thermal oxidation. However, severe carrier mobility degradation and reduced gate oxide reliability in SiC-based field-effect transistors (FETs) are serious issues, which may result from residual carbon impurities and other related defects in SiC-MOS structures [2,3]. As shown in Chapter 2, large amounts of interface trap charges were observed for SiC-MOS devices regardless of a few defect states in the as-oxidized SiO_2 and/or at as-oxidized SiO_2/SiC interfaces. Recently, many defect passivation techniques, such as high-temperature post-oxidation annealing in an inert gas [4,5] and nitric oxide (NO_x) ambient [6–8], were proposed to alleviate these problems.

In addition to the reliability issue regarding dielectric breakdown of the gate oxides,

instability of SiC-MOSFETs causing threshold voltage (V_{TH}) change has been pointed out, especially under high-temperature operation [9,10]. In the field of Si research, mobile ions in gate oxides, such as sodium and potassium, are known to be distinctive origins of the V_{TH} instability, and a countermeasure has already been well established against these ionic contaminations. Moreover, V_{TH} shift induced by carrier injection into the oxides during bias stressing at high temperatures, so-called bias-temperature instability (BTI), has been considered as the determining factor in reliability of modern Si-based integrated circuits [11].

On the basis of this knowledge, BTI in SiC-MOS devices has recently been studied, and its similarity and/or discrepancy with Si-based devices have been discussed. Due to the large number of electrical defects in SiC-MOS structures, V_{TH} shift, as well as flatband voltage (V_{FB}) shift in MOS capacitors, induced by charge injection becomes a primary concern even under the room-temperature operation [12–15]. Furthermore, it has been suggested that significant V_{TH} shift under high temperatures be governed by thermally activated majority carriers injected from SiC substrates into the oxides depending on the substrate type [15]. More recently, the presence of mobile ions has become evident in SiC-MOS structures leading to V_{TH} change in the opposite direction to that for carrier injection [9,10,16,17]. Although distinct ion-drift phenomena attributable to positive ions have been seen mostly for gate oxides with post-oxidation NO_x annealing, they are not yet deeply understood. This is because the correlation between BTI behavior and methods for gate oxide formation on SiC substrates has not been examined and, even worse, details of the methods were undisclosed in some literature. In this study, we, therefore, systematically investigated instability of thermally grown SiC-MOS devices under different stressing and measurement conditions, and obtained BTI characteristics after step-by-step post-oxidation treatments. Our results clearly demonstrate that intrinsic mobile ions exist in as-oxidized SiC-MOS structures and that they are eliminated or regenerated with specific post-oxidation treatments.

3-2 Experimental

3-2-1 Fabrication of 4H-SiC MOS capacitors with varying POA conditions

This chapter explains the BTI characteristics of 4H-SiC MOS devices fabricated with post-oxidation annealing (POA) in argon and subsequent forming gas annealing (FGA), a typical annealing process performed after thermal oxidation of SiO_2. Figure

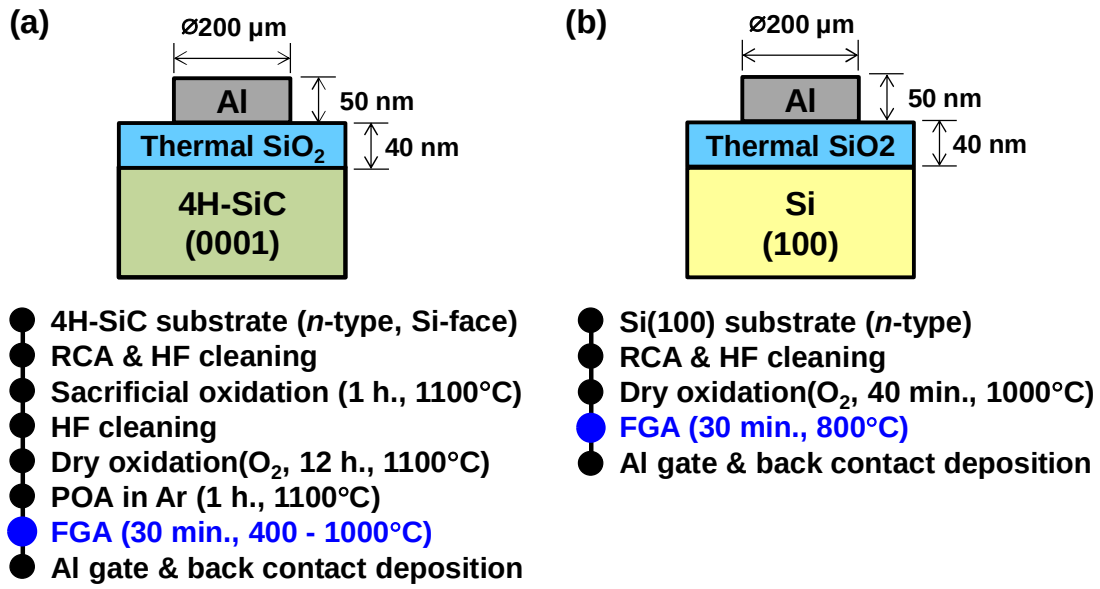

Fig. 3-1 Process flow of (a) 4H-SiC MOS capacitors, and (b) Si-MOS capacitors. These samples were passivated by FGA with varying in annealing temperatures.

3-1(a) shows the fabrication process flow and schematic illustration of 4H-SiC MOS capacitors with thermally grown SiO_2 as an insulator. Basic 4H-SiC MOS capacitors were fabricated on as-grown 4°-off-angle 4H-SiC(0001) substrates with an n-type epilayer ($N_d = 1\times10^{16}$ cm^{-3}). Firstly, the 4H-SiC substrates were cleaned by conventional RCA cleaning process for removing unwanted organic (1:1:5 solution of NH_4OH:H_2O_2:H_2O at 70°C) and ionic contaminations (1:1:5 solution of HCl:H_2O_2:H_2O at 70°C), following by striping of native oxide layer with 5% hydrofluoric acid (HF) solution at room temperature for 15 min. After that, sacrificial oxidation of 4H-SiC substrates was done in a traditional tube oxidation furnace with flowing dry-O_2 at 1100°C for 1 h., resulting in a thin sacrificed oxide layer with a thickness of about 10 nm or less. Removal of sacrificed oxide on 4H-SiC substrates with 5% HF solution were performed just before introducing 4H-SiC substrates into the oxidation furnace. Thermal oxidation was conducted at 1100°C for 12 hours in dry-O_2 ambient to produce a 40-nm-thick thermal oxide. Some samples are subjected to post-oxidation treatments under different conditions and sequences. Post-oxidation annealing in argon ambient (Ar-POA) was performed at 1100°C for 1 hour by changing ambient gas just after dry oxidation in the same furnace tube had finished. We also examined the impact of hydrogen gas (3% H_2 diluted by N_2) annealing; that is, forming gas annealing (FGA), on BTI behavior in these SiC-MOS devices. It is well known that, unlike hydrogen passivation of electrical defects at SiO_2/Si interface, much higher temperature, typically over 800°C, is required to improve SiO_2/SiC quality [18]. Although there is still some

debate about the mechanism of the hydrogen passivation, its benefit for achieving low interface state density (D_{it}) in SiC-MOS are widely accepted. Thus, we examined combination treatments with high-temperature POA and FGA. As illustrated in Fig. 3-2, high-temperature FGA was performed on SiO_2/4H-SiC structures with an annealing condition that separated into two main parts, *i.e.* annealing at high-temperature for 30 min., and post-passivation annealing at 450°C for 30 min. Note that, SiC-MOS devices explored in this study contain a negligible amount of nitrogen atoms in SiO_2/SiC structures. For electrical measurements, Al circular gate electrodes 200 μm in diameter and back contact were made by vacuum evaporation to form SiC-MOS capacitors.

Bidirectional C-V curves were obtained by gate bias swing from -10 V to +10 V, and back to -10 V, under different measurement temperatures. The C-V measurements were carried out at a frequency of 1 MHz. D_{it} values of SiC-MOS devices were determined using a traditional high-low method. Moreover, to examine the impact of extrinsic contaminations originating from the equipment, reference Si-MOS capacitors were also fabricated on *n*-type Si substrates with the same equipment shown in Fig. 3-1(b).

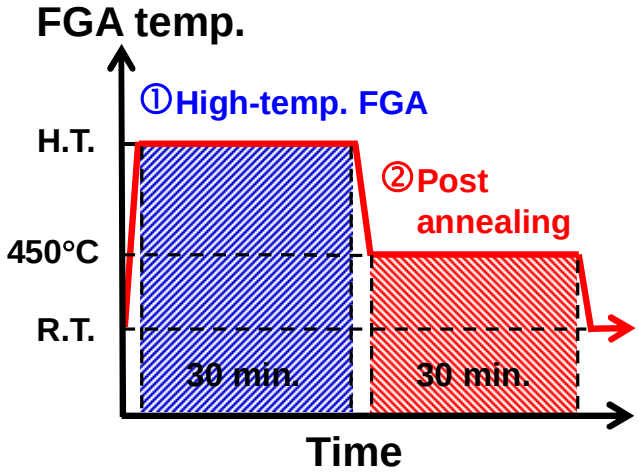

Fig. 3-2 Annealing condition for FGA used in this study. The FGA at high temperatures (T > 800°C) is conducted for 30 min to passivate the C-related defects followed by post annealing for 30 min without changing the ambient to passivate the Si-dangling bonds.

3-2-2 Bias-temperature stress experiment for mobile ion detection

In order to detect mobile ion phenomena, bidirectional C-V curves were firstly measured at room temperature. After heating up the samples to 200°C, positive and negative BTS (V_G = ±10 V) were simultaneously applied to two different capacitors for

2 minutes. Then, the samples were cooled down to room temperature by keeping the stress bias, as illustrating in Fig. 3-3. Positive mobile ions are supposed to move toward SiO_2/SiC and Al/SiO_2 interfaces under positive and negative gate bias at high-temperature, respectively, and then they are immobilized after cooling down (see Fig. 3-3). Finally, bidirectional C-V measurements of the stressed capacitors were performed again at room temperature, in order to examine the mobile ion, causing V_{FB} shifts from the original C-V measured without BTS. Assuming that all mobile ions were completely moved and fixed at the interfaces by negative or positive BTS, total mobile ionic charge areal density, Q_M can be estimated by these equations.

$$\text{Since} \quad \Delta V_{FB} = \frac{Q_M}{C_{ox}}, \tag{3.1}$$

$$\text{then} \quad Q_M = C_{ox} \times \Delta V_{FB} = C_{ox} \times |\, V_{FB}(\text{PBTS}) - V_{FB}(\text{NBTS}) \,|, \tag{3.2}$$

where C_{ox} is the oxide capacitance, V_{FB}(PBTS) and V_{FB}(NBTS) are the calculated V_{FB} from the room temperature C-V curves measured after PBTS or NBTS, respectively.

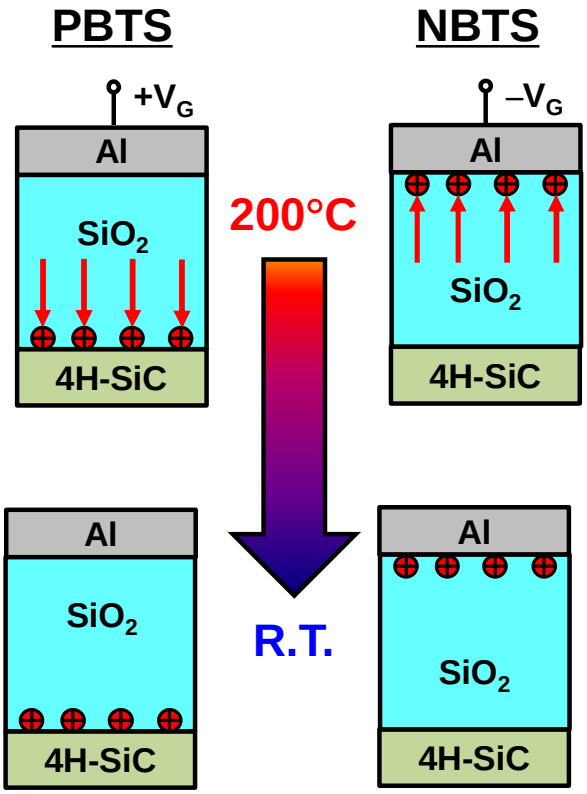

Fig. 3-3 Illustration describes mobile ion drifts corresponding to PBTS or NBTS performed at 200°C, and immobilization of mobile ions at R.T.

3-3 Results and Discussion

3-3-1 Unusual generation of mobile ions in thermal oxides on 4H-SiC by FGA

Figure 3-4(a) shows bidirectional C-V curves taken from a SiC-MOS capacitor with an as-oxidized SiO_2 measured at room temperature (black open squares) and 200°C (red open triangles). At room temperature, a clockwise C-V hysteresis approximately equal to 0.5 V was clearly observed. This coincides well with previous reports and indicates that electrons, majority carriers of n-type SiC substrate, were injected into the oxide during an accumulation bias condition. Furthermore, the poor interface quality is recognized from the stretch-out shape of the C-V curve, possibly due to carbon-related defects as discussed in the literature [2,3]. Note that when measured temperature is increased to 200°C, the direction of C-V hysteresis inversely changes to counter-clockwise. An extremely large hysteresis of about 2.2 V and a negative V_{FB} shift with respect to the ideal V_{FB} position (0.27 V at 200°C) indicate the existence of positive mobile ions in the SiC-MOS device. After the temperature was ramped down to room temperature, the bidirectional C-V curve measured on the same capacitor completely returned to the clockwise direction, meaning that the mobile ion effect is prominent only at high temperatures as expected.

We have also characterized Si-MOS capacitors with a thermal oxide of the identical thickness (equivalent oxide thickness (EOT): 40 nm) formed by using the same furnace tube at 950°C. As shown in Fig. 3-4(b), while thermally generated carriers in the bulk Si substrate resulted in increased inversion capacitance under the negative bias, bidirectional C-V curves of the Si-MOS capacitor exhibited a minor clockwise hysteresis originating from electron injection. In addition, the counter-clockwise hysteresis was not observed at high-temperatures for the Si-MOS capacitors with a thermal oxide grown at higher oxidation temperatures (above 1100°C) and/or with high-temperature annealing in Ar ambient for 12 hours (data not shown). These results demonstrate that extrinsic contaminations are ruled out as a physical origin of the ion-drift phenomenon in SiO_2/SiC structure and that the intrinsic mobile charged species self-generated in SiO_2 during thermal oxidation may be involved in BTI in SiC-MOS.

High-temperature POA is one of the standard measures to improve electrical property of SiO_2/SiC interface [4,5], in which a reasonable explanation for the improvement so far is thermal diffusion of carbon impurities accumulated at the interface. Bidirectional C-V curves of the SiC-MOS capacitor subjected to POA at

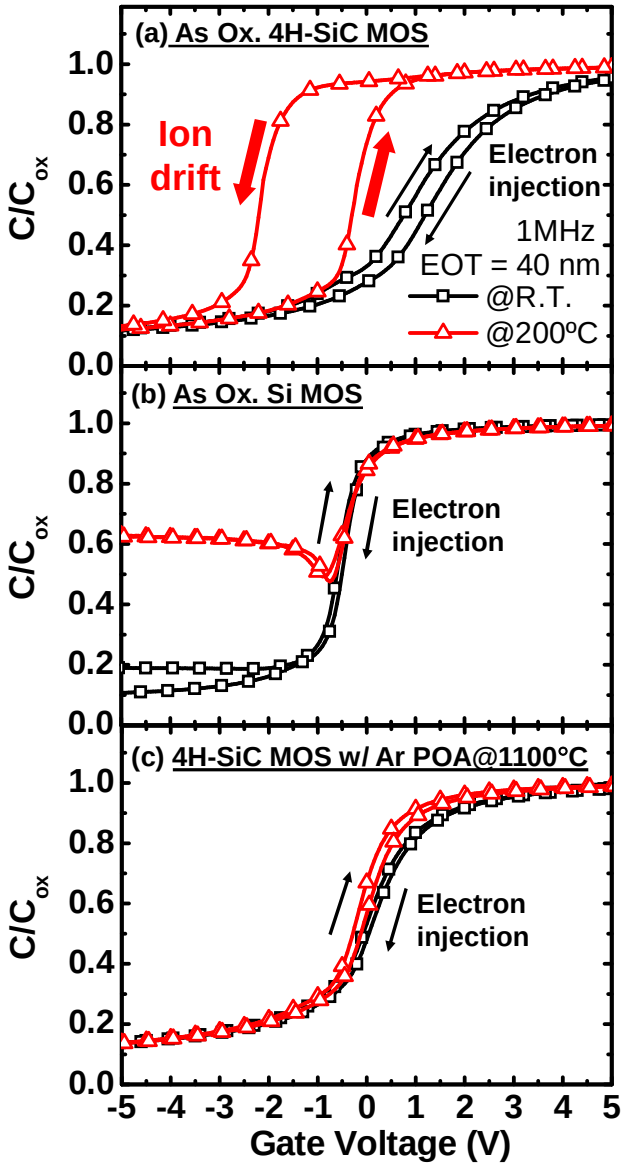

Fig. 3-4 Bidirectional C-V curves obtained from (a) a SiC-MOS capacitor with an as-oxidized thermal oxide, (b) reference capacitor formed on a Si substrate using the same equipment and identical EOT, and (c) SiC-MOS capacitor with a thermal oxide subjected to high-temperature POA at 1100°C. The oxide of these capacitors was about 40 nm thick. C-V measurements were carried out at room temperature (black open squares) and 200°C (red open triangles). The measurement frequency was 1 MHz for all cases.

1100°C are shown in Fig. 3-4(c). Interestingly, small charge injection (clockwise) C-V hysteresis was observed regardless of measured temperature. This implies that the high-temperature POA is beneficial to eliminate intrinsic mobile ions in SiO_2/SiC structure. Also, judging from the reduced clockwise hysteresis and steep slope in C-V

curves, we can confirm improved electrical property of SiC-MOS by high-temperature POA. Thus, in this sense, a positive correlation was identified between mobile ions and interface defects.

3-3-2 Temperature-dependent BTI in 4H-SiC MOS capacitors

Next, we investigated effects of high-temperature FGA on BTI in SiC-MOS devices. For this purpose, we made another capacitor subjected to the combination treatment with high-temperature POA at 1100°C and two-step FGA at 800°C for 30 min followed by the second annealing at 450°C for 30 min in order to finalize hydrogen passivation of Si-dangling bonds. As indicated by black open squares in Fig. 3-5(a), improved C-V characteristics with a steep slope and negligible C-V hysteresis were obtained at room temperature. Figure 3-5(b) shows the energy distribution of D_{it} for various SiO_2/SiC structures. Electrical defects at the as-grown SiO_2/SiC interface were further reduced by the combination treatment with high-temperature POA and FGA. However, despite the improved interface quality, a counter-clockwise C-V hysteresis of about 1.25 V was apparently seen once again at 200°C (see Fig. 3-5(a)). This result means that high-temperature FGA regenerates positive mobile ions in SiO_2/SiC structures, even though they were mostly eliminated or deactivated by POA treatment.

Figure 3-6 summarizes our systematic study of BTI behavior in SiC- and Si-MOS capacitors with various post-oxidation treatments, in which changes in the direction and magnitude of C-V hysteresis are plotted as a function of the measurement temperature. The results are categorized into clockwise (positive) and counter-clockwise (negative) behaviors originating from electron injection and ion-drift effects, respectively. Regarding the reference Si-MOS capacitors, both as-oxidized sample (As ox. Si-MOS) and that with FGA at 800°C (Si-MOS+FGA) exhibited negligible clockwise C-V hysteresis. Therefore, we can again exclude effects of ion contaminations caused by high-temperature FGA, as well as the furnace oxidation mentioned above. Among the SiC-MOS capacitors, the as-oxidized SiC-MOS sample (As ox.) showed the most significant counter-clockwise hysteresis, indicating a large number of mobile ions exists. Moreover, considering both the marked negative shift at around 100°C and subsequent saturation behavior, positive mobile ions in the as-oxidized sample were considered to drift quickly at low temperatures. Although high-temperature POA of SiC-MOS suppressed ion-drift phenomenon, following high-temperature FGA regenerated a substantial number of positive mobile ions in the oxides (see POA+FGA). Our detailed study also revealed that the number of regenerated mobile ions increased as FGA

temperature increased up to 800°C and, then, slightly decreased at higher temperatures (see Fig. 3-6, but detailed data are not shown). Furthermore, when trends in ion-drift phenomena are compared, it seems that a drift of the regenerated ions induced by the external field has not yet completed during a bidirectional bias swing and that the diffusion coefficient of the regenerated mobile ions is certainly different from that in the as-oxidized sample.

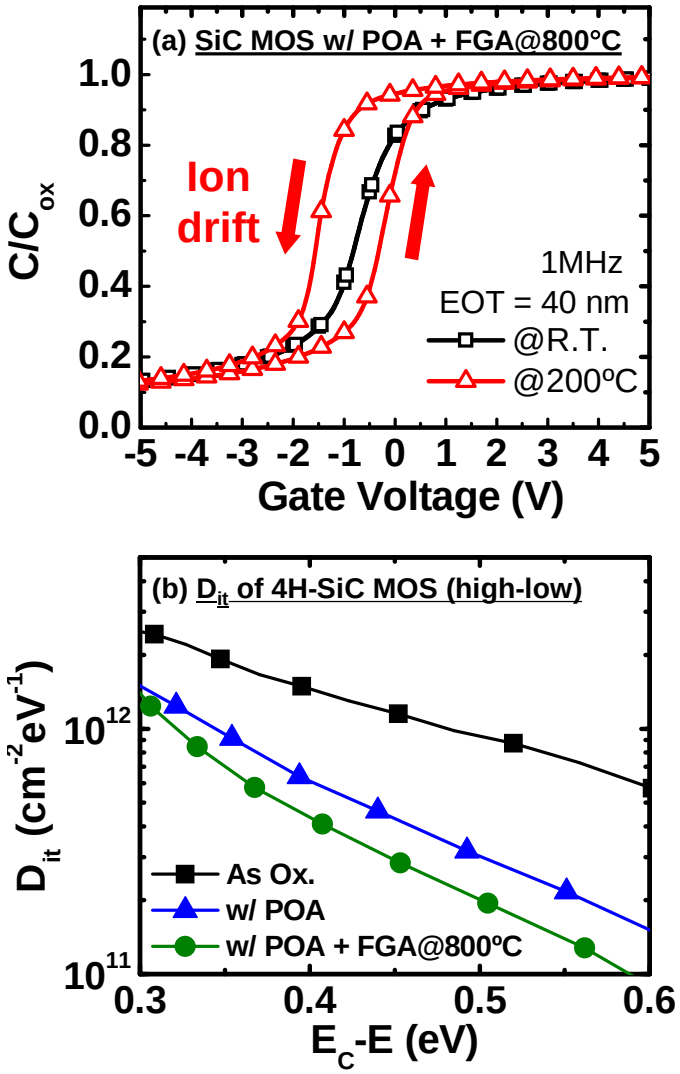

Fig. 3-5 Electrical characterizations of SiC-MOS capacitors with thermally grown oxides subjected to various post-oxidation treatments. (a) Bidirectional C-V curves taken with a thermal oxide treated by the combination treatment with POA and 800°C-FGA. (b) Energy distribution of D_{it} for SiO_2/SiC interface of the as-grown thermal oxide and that treated with POA and FGA.

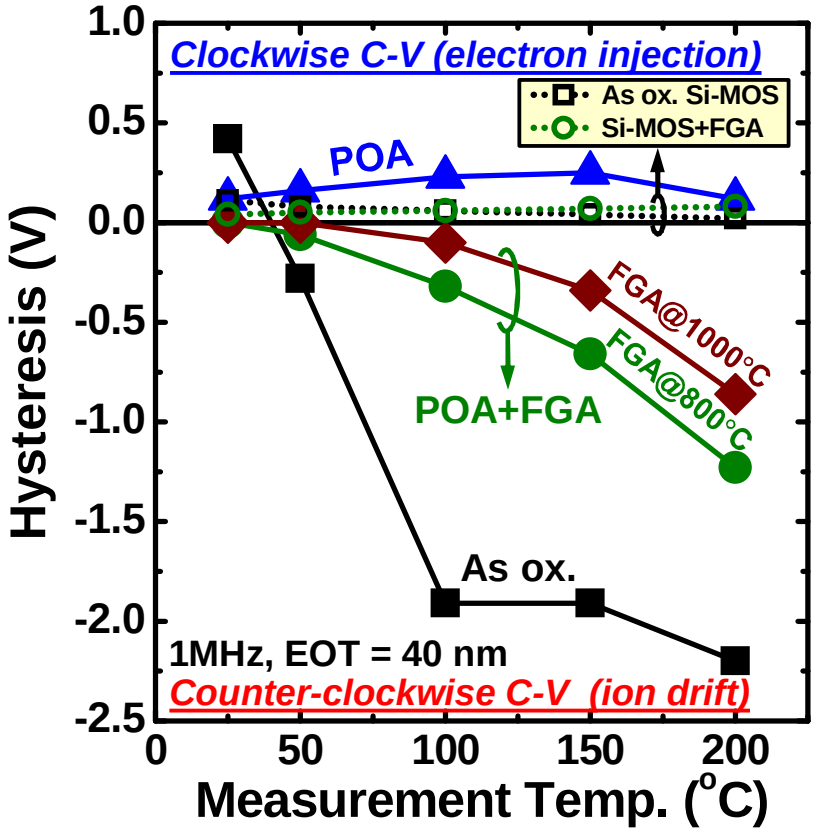

Fig. 3-6 Temperature dependent C-V hysteresis of SiC-MOS capacitors (solid lines with filled symbols) and reference Si-MOS capacitors (dotted lines with open symbols). Horizontal axis represents measurement temperature. Vertical axis shows the magnitude of bidirectional C-V hysteresis, in which positive direction denotes clockwise hysteresis corresponding to electron injection and negative direction denotes counter-clockwise hysteresis corresponding to ion drift. Results are summarized from the as-oxidized SiC capacitor (As ox.), those treated only with POA at 1100°C (POA), and with combination treatments with the 1100°C-POA and high-temperature FGA at different maximum temperatures (FGA@800°C and FGA@1000°C), together with results from the as-oxidized Si-MOS capacitor (As ox. Si-MOS) and that subjected to FGA at 800°C (SiC-MOS+FGA).

3-3-3 Estimated amounts of mobile ions generated in thermal oxides

Density of the regenerated mobile in SiO_2/SiC structures was extracted from bias-temperature stress (BTS) experiments for POA-treated SiC-MOS capacitors with and without FGA at 800ºC. As illustrated in Fig. 3-3, after the samples were heated up to 200°C, positive and negative BTS (gate bias: ±10 V) were simultaneously applied to

the SiC-MOS capacitors for 2 min. Then, the samples were cooled down to room temperature while the stress biases were kept to freeze mobile ions, and bidirectional C-V curves were acquired. Positive mobile ions are supposed to be accumulated at SiO_2/SiC and Al/SiO_2 interfaces under positive and negative gate bias at the elevated temperature, respectively (see Fig. 3-3). Figure 3-7 shows bidirectional C-V curves obtained from these SiC-MOS capacitors with and without BTS. As shown in Fig. 3-7(a), neither C-V hysteresis nor V_{FB} shift due to BTS were observed for the sample without FGA (only POA), corresponding to the absence of mobile ions and negligible charge injection by stressing. In contrast, for the sample with 800ºC-FGA (Fig. 3-7(b)), V_{FB} shift induced by ion drift was clearly seen, in which positive and negative BTS resulted in negative and positive V_{FB} shift, respectively. Areal density of the regenerated

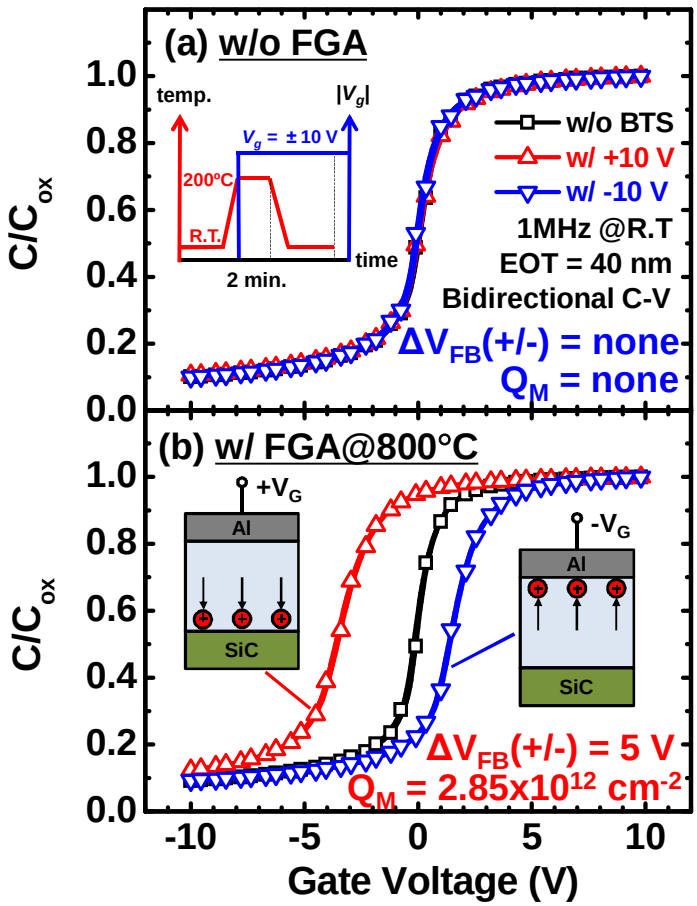

Fig. 3-7 Comparison of bidirectional C-V curves before (black open squares) and after BTS at 200°C with positive (upward red triangles) and negative (downward blue triangles) gate bias at 10 V. POA-treated SiC-MOS capacitors were examined (a) without FGA and (b) with FGA at 800°C. The inset in Fig. (a) represents procedure for BTS. Figure (b) depicts motions of the positive mobile ions.

positive mobile ions (Q_M) calculated from the difference in V_{FB} was 2.85 x 10^{12} cm^{-2}. Besides, a stretch-out in the C-V curves was observed after stressing, especially for the FGA-treated capacitor. This is probably due to electrical degradation of MOS interfaces caused by the electrical stressing.

3-3-4 Discussion of possible origins of mobile ions in SiC-MOS

Previously, extrinsic effects, such as metal contaminations from the gate metal and hydrogen ions from the device passivation films, have been considered to be possible origins of mobile ions in SiC-MOS devices [9,10,17]. However, in the current study, the former candidate is ruled out, thus indicating an intrinsic problem of SiC oxidation as stated above. Hydrogen ions cannot only account for ion-drift phenomena because high-temperature FGA itself did not cause counter-clockwise C-V hysteresis in Si-MOS capacitors (see Fig. 3-6). On the basis of these experimental results, we think that carbon-related complexes and/or a peculiar SiO_2 network formed by SiC oxidation might be involved in significant BTI in SiC-MOS devices. Besides, the reason for mobile-ion regeneration by FGA could be hydrogen-induced modification of SiO_2/SiC interface that creates carbon-related complexes.

To identify accumulated possible carbon-related species after the positive and negative BTS, we conducted dynamic secondary ion mass spectrometry (D-SIMS) analysis of SiC-MOS capacitors examined with thick thermal oxides (EOT = 80 nm). After stressing in the same manner shown in Fig. 3-7(a), Al top electrodes were removed in order to reduce the background signal of carbon concentration, as well to improve the detection limit of D-SIMS. Figure 3-8 shows that the background signal of C concentration in this structure was significantly decreased to roughly 10^{17} – 10^{18} cm^{-3}, which shows the improvement of the detection limit. Yet, we failed to observe marked differences in depth profiles of carbon and hydrogen impurities in the oxide depending on the bias polarity. This is because a small number of the mobile ions with an areal density of a few 10^{12} cm^{-2}, which corresponds to a bulk density of several 10^{17} cm^{-3}, is hard to distinguish from the background signals. Thus, further study based on techniques that are more sophisticated is required to obtain direct evidence of the mobile species. Basically, the advancement of physical characterization techniques with improved sensitivity and higher special resolution will be realized in the near future. Moreover, judging from the distinct temperature dependence of V_{FB} shift on post-oxidation treatment (see Fig. 3-6), it can be concluded that the coefficient of thermal diffusivity for mobile ions in the as-grown oxide is much higher than that in the FGA-treated oxide. This raises further questions over physical origins and diffusion

mechanism of the mobile ions in SiC-MOS devices that need to be solved to develop highly reliable SiC-MOSFETs under high-temperature operation.

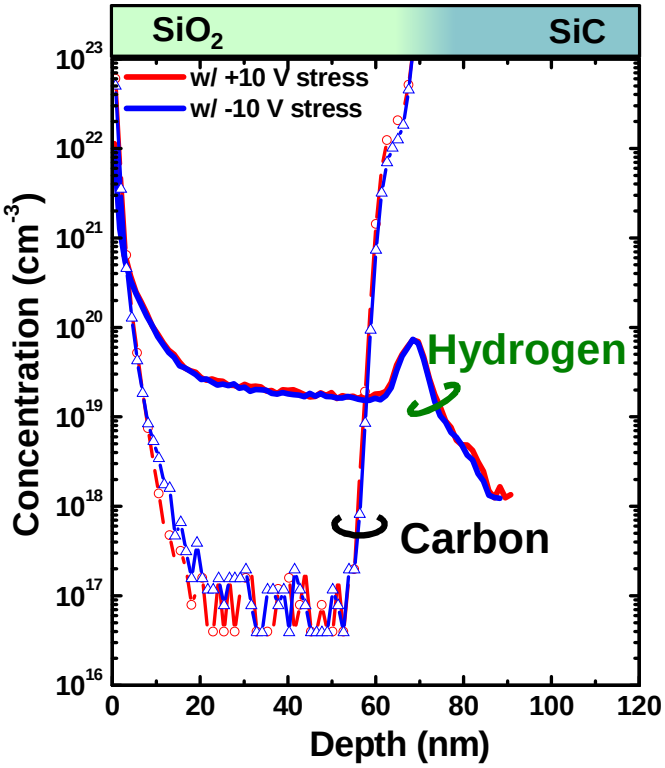

Fig. 3-8 Depth profiles of C and H concentration measured by SIMS throughout FGA-treated SiO_2(80 nm)/4H-SiC structure.

We performed an additional analysis to understand how significant of carbon impurities involved in mobile ion effect in SiC-MOS structure with thermally grown oxide. As the set hypothesis of carbon impurities involved in mobile ion generations, we intended to inject extrinsic carbons into SiO_2 thermally grown on conventional Si substrate, aiming to simulate the phenomena that occur in SiC-MOS devices. The fabricated SiO_2/Si structure with implanting reasonable amount of carbon into SiO_2 may also demonstrate mobile ion drift at high-temperature.

Si-MOS capacitors with carbon-ion implanted into SiO_2 were used in this study. Thermal oxidation of the *n*-type Si substrates was done in a tube furnace with dry-O_2 ambient at 1000°C for 70 min., resulting in an approximately 65 nm-thick SiO_2 layer. The expected carbon atomic concentration was determined based on the depth profiles in as-oxidized SiO_2/SiC structures measured by D-SIMS as shown in Fig. 3-9(a), which is about 1×10^{20} cm^{-3}. The ion energies for C-ion implantations were calculated by using SRIM (the Stopping and Range of Ions in Matter), a software used for simulating the ion trajectories and concentrations with respect accelerating energy [19]. In this

calculation, we expected 60 nm-long, measured from the distance from SiO_2 surface to inside SiO_2 layer as the farthest range of ion trajectories. The proposed accelerating energy for carbon-ion implantation equally to 6 keV agrees with peak concentration of about 2×10^{20} cm^{-3} in Gaussian distribution in SiO_2 shown Fig. 3-9(b).

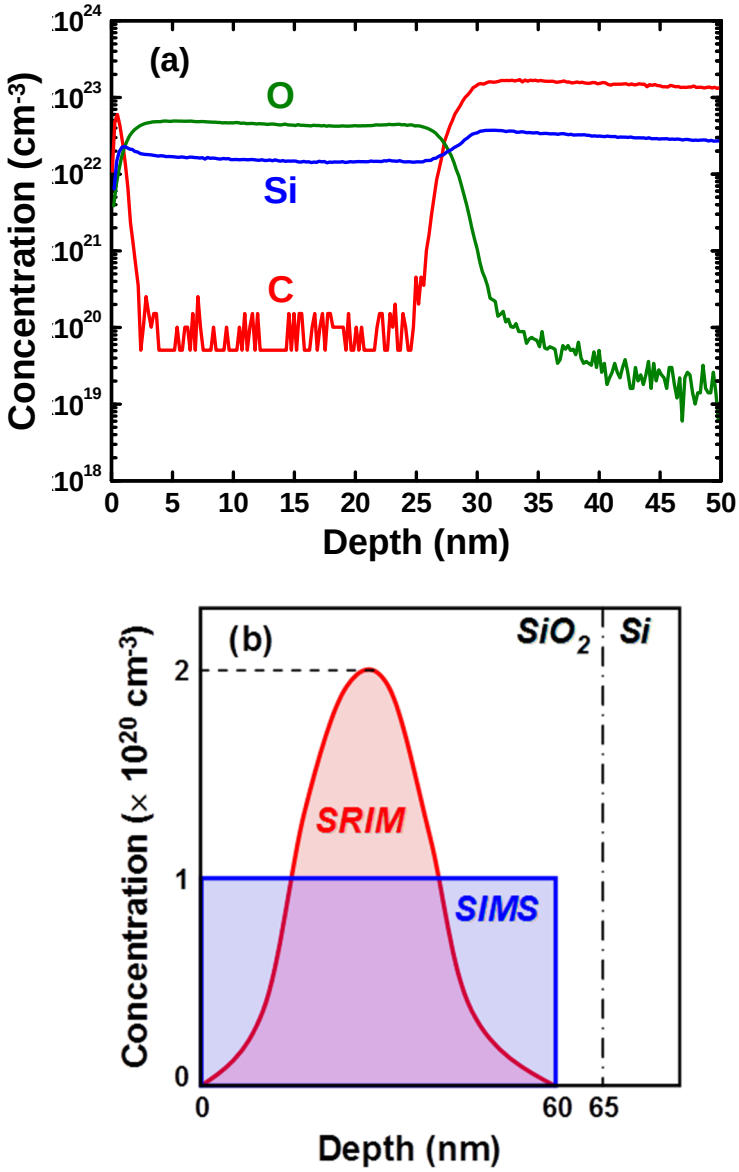

Fig. 3-9 (a) Depth profiles of O, Si and C concentration measured by SIMS throughout thermally grown SiO_2/4H-SiC structure. (b) Expected distribution of carbon atomic concentration in SiO_2 calculated by SRIM, in which the peak concentration is twice of the C concentration measured in thermal oxide of 4H-SiC by D-SIMS.

Figure 3-10 shows bidirectional C-V curves measured at room and high-temperature (200°C) of fabricated Si-MOS capacitors. The as-implanted samples show excellent C-V curves without any mobile ion effect (see Fig. 3-9(a)). In contrast, regardless of the absence of mobile ions the conventional Si-MOS capacitors with high-temperature FGA shown in Fig. 3-10(b), the small amount of counter-clockwise C-V hysteresis measured at 200°C was illustrated only for the C-implanted sample with subsequent FGA at

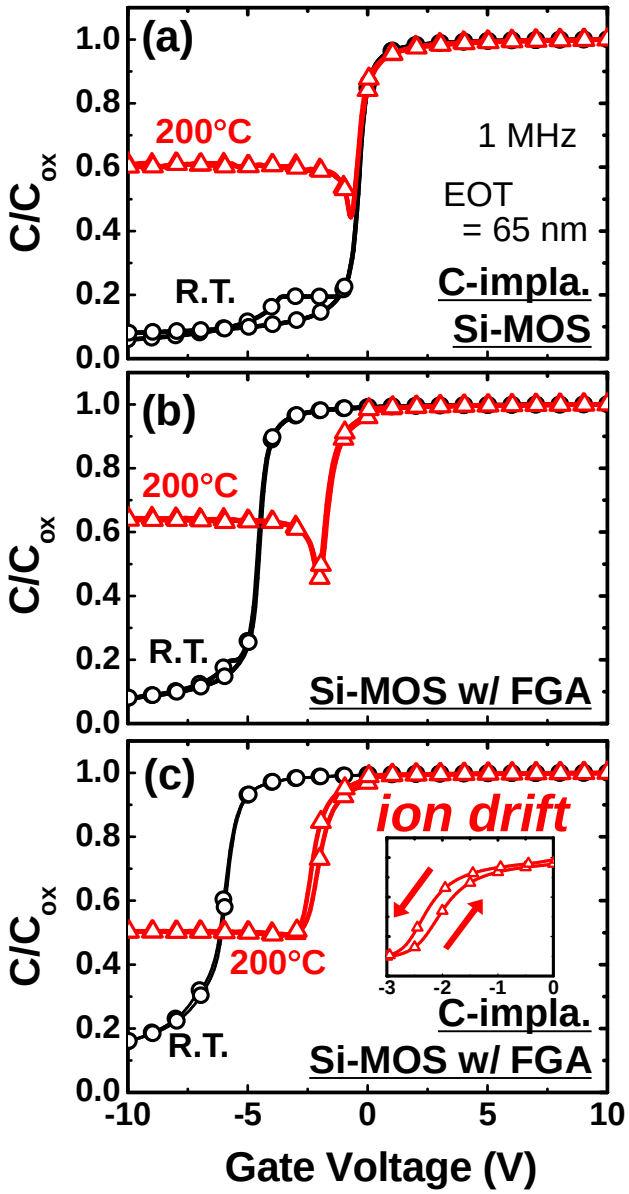

Fig. 3-10 Comparison of bidirectional C-V curves derived from (a) C-ion implanted, (b) FGA-treated without C-ion implanted, and (c) FGA-treated with C-ion implanted Si-MOS capacitors. The measurements were done at R.T. and 200°C

800°C shown in Fig. 3-10(c). The magnitude of C-V hysteresis approximately 0.35 V (see the inset of Fig. 3-10(c)) may support the proof of typical unusual mobile ion generation as occurred in SiC-MOS devices. In other words, hydrogen may interact with some implanted carbon species at the SiO_2/Si interfaces and then generates some mobile charged species, which are able to diffuse under the electric field at elevated temperature. Though, based on the magnitude of C-V hysteresis, the number of mobile ions formed in SiO_2 on Si is considerably smaller than that existed in SiC cases, carbon interstitials and/or other C-related species in SiO_2 are supposed to be indispensable for mobile ion generation.

3-4 Summary

Unusual ion drift phenomena in SiC-MOS capacitors were investigated. We observed positive mobile ions spontaneously generate in thermally grown oxides, which could be considered as an intrinsic problem in SiO_2/SiC structures. The number of the mobile ions and their nature were found to depend on post-oxidation treatments. Although the mobile-ion effects can be alleviated by high-temperature POA, passivation of interface defects by high-temperature FGA recreates additional mobile ions despite the improved interface quality. Much controversy exists over the physical origin of mobile ions, but our research provides insights into mobile ions and sheds light on concerns about BTI in SiC-MOS devices through which we need to work to develop advanced SiC-based devices.

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Chapter 4 Controlling of Mobile Ions in Thermal SiO_2 on 4H-SiC by Utilizing Bias-Temperature Stress

In this chapter, unusual behavior of bias-temperature instabilities in SiC metal-oxide-semiconductor (MOS) devices is further investigated. Electrical measurements of SiC-MOS capacitors are used to examine details of self-generated mobile ions in thermal oxides on 4H-SiC(0001) substrates previously demonstrated in Chapter 3, such as their polarity, density, distribution and impact on interface properties. It is found that positive bias-temperature stress (BTS) which is the applied bias gate voltages at high temperatures accumulates self-generated positive mobile ions at the bottom SiO_2/SiC interface with an areal density of several 10^{12} cm^{-2}, and that they induce additional electron trap formation at the interface. Using this knowledge, we demonstrate effective removal of the positive mobile ions with a combination of negative BTS and subsequent etching of the oxide surface.

4-1 Introduction

In addition to interface issues, considerable attention has been given to bias-temperature instability (BTI) causing significant changes in flatband voltage (V_{FB}) in SiC-MOS capacitors and threshold voltage (V_{TH}) in SiC-MOSFETs, because it determines the reliability and lifetime of MOS devices [1,2]. There are two possible physical origins of BTI phenomena: trapped charges and mobile ions in the oxides. Charge injection into the electrical defects at and/or near poor SiO_2/SiC interfaces causes BTI typically characterized by a clockwise hysteresis in bidirectional capacitance-voltage (C-V) curves of MOS capacitors. On the other hand, the presence of charged mobile ions in SiC-MOS devices has been pointed out by several groups [2–5]. According to longstanding Si research, alkaline ions (Na^+, K^+) are the most common origins of mobile ions causing BTI in MOS devices [6,7], in which charged ions can move at elevated temperatures depending on the external electric field to cause counter-clockwise C-V hysteresis. Since high-temperature annealing is necessary for gate stack and Ohmic contact formation, metal contaminations originating from process equipment could be the cause of mobile ions in SiC-MOS devices. In Chapter 3, we have reported unusual generation of mobile ions in thermally-grown SiC-MOS structures [8]. Our systematic study revealed that the mobile ions (other than extrinsic metal contaminations) are self-generated by dry oxidation of SiC substrates, and that

carrying out POA under a diluted hydrogen ambient, the so-called forming gas annealing (FGA) at around 800°C also causes mobile ion generation in SiC-MOS devices, although the interface property is improved by hydrogen passivation. Since BTI induced by unusual mobile ions in thermal oxides was definitely found to be an intrinsic problem for SiC-MOS structures, it is essential to acquire a deep understanding of the mechanism of self-generated mobile ions. Moreover, although many techniques have been developed for Si-MOS technology to remove and/or prevent mobile alkaline ions in the oxides [9–11], no appropriate method has yet been found to suppress BTI phenomena in SiC-MOS devices. In this chapter, we therefore investigated the nature of FGA-induced mobile ions and tried to control BTI phenomena in SiC-MOS devices. We also discussed the harmful impact of mobile ions on SiO_2/SiC interface properties.

4-2 Experimental

4-2-1 Fabrication of 4H-SiC MOS capacitors with slope-shaped oxides

We fabricated SiC-MOS capacitors on 4H-SiC(0001) Si-face substrates with an n-type epilayer ($N_d = 1 \times 10^{16}$ cm^{-3}). After sacrificial oxidation and subsequent removal with hydrofluoric acid (HF) solution, a 40-nm-thick SiO_2 layer was formed by thermal oxidation in dry-O_2 ambient at 1100°C for 12 h, followed by POA in Ar ambient (Ar-POA) at 1100°C for 1 h. High-temperature FGA in 3% H_2/N_2 ambient was performed at 800°C for 30 min and combined with mild-temperature FGA at 450°C for 30 min in order to passivate Si-dangling bonds at the SiO_2/SiC interface. As we previously demonstrated, while a reference Si-MOS device that received identical thermal budget in the same furnace did not exhibit mobile-ion-induced BTI, intrinsic mobile ions were self-generated in the thermal oxide grown on the SiC substrate [8]. In order to investigate the nature of the mobile ions in detail, slope-shaped oxides (see Fig. 4-1) were prepared by wet etching after applying positive or negative bias-temperature stress (PBTS or NBTS). For the first step, large rectangular Al pads (6×8 mm^2) were deposited to cover almost the whole surface of the thermal SiO_2. Then, PBTS and NBTS were separately applied to two samples at 200°C for 2 min with an electric field of about $\pm 2.5 \times 10^8$ V m^{-1} to move the mobile ions towards the samples' SiO_2/SiC and Al/SiO_2 interfaces. Constant bias stresses were continually applied while ramping down to room temperature to freeze the ions at the interfaces. Next, after removing the Al pads by wet etching, the samples were partially dipped into 1% HF solution, resulting in a slope-shaped SiO_2 with physical thicknesses ranging from 15 – 35 nm. Finally, small

Al gate electrodes (200-μm-diameter) and back contacts were deposited.

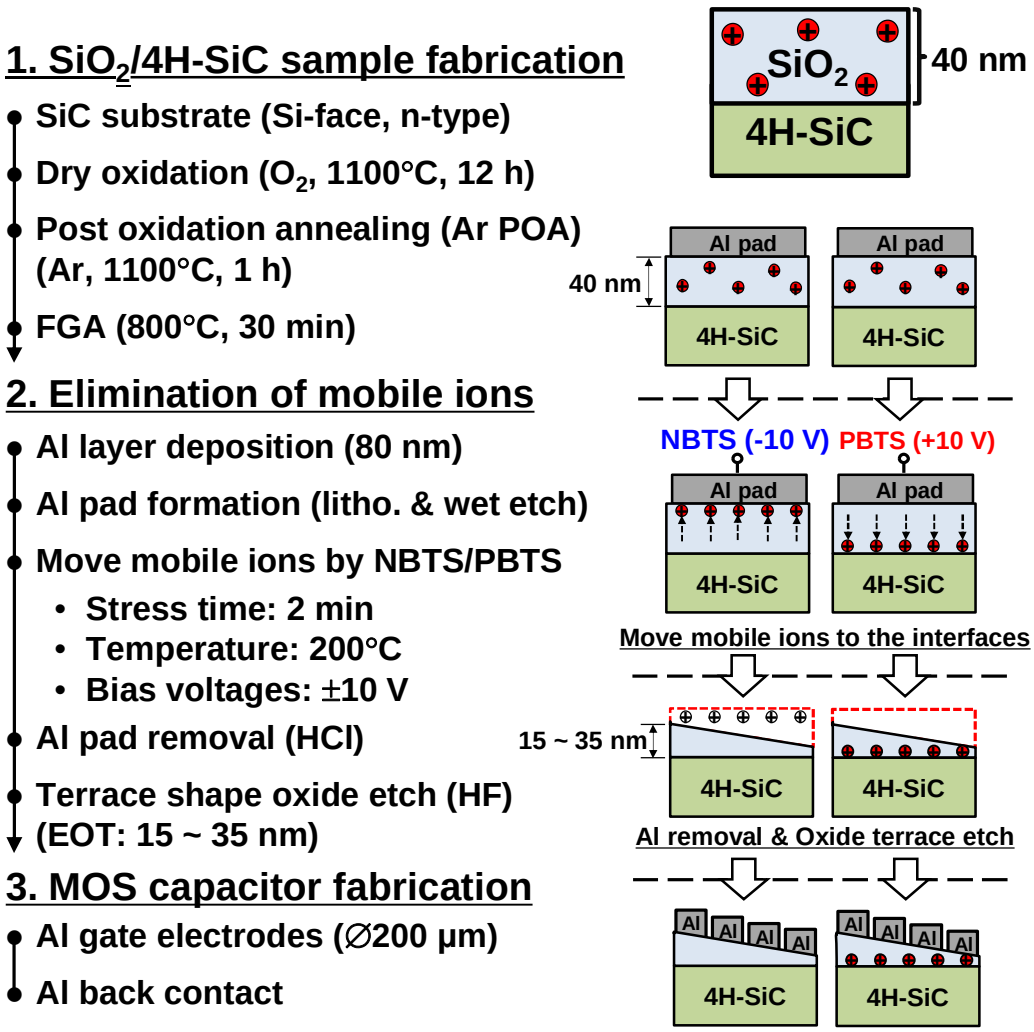

Fig. 4-1 Procedure for fabricating SiC-MOS capacitors with slope-shaped gate oxides. NBTS and PBTS were respectively applied at 200°C for 2 min to samples with large rectangular Al pads to accumulate mobile ions at the top and bottom interfaces. After the Al pad removal, the gate oxides were partially etched by dipping the samples into HF solution to form slope-shaped oxides. Finally, small Al electrodes were deposited to produce a number of MOS capacitors.

4-2-2 Method to estimate oxide charge density and distribution

The flatband voltage (V_{FB}) corresponds to a particular gate voltage (V_G) which is applied to the MOS capacitors that produce flats in the energy bands in the semiconductors. When the charges disappear in the oxide or at the oxide-semiconductor interfaces, the theoretical V_{FB} value only denoted by the following equation:

$$V_{FB,ideal} = \varphi_{ms} = \varphi_m - \varphi_s , \qquad (4.1)$$

where φ_{ms} is the work function difference between the gate metal (φ_m) and the semiconductor (φ_s). Besides, the V_{FB} of real MOS structures is, however, affected by the existence of charges in the oxides or at the oxide-semiconductor interfaces. For an oxide charge areal density, Q_{ox}, settled closed to the oxide-semiconductor interfaces, and an oxide charge density, ρ_{ox}, scattered inside the oxide, the V_{FB} is given by:

$$V_{FB} = V_{FB,ideal} - \frac{Q_{ox}}{\varepsilon_{ox}} t_{ox} - \frac{1}{\varepsilon_{ox}} \int_0^{t_{ox}} \rho_{ox}(x) x dx , \qquad (4.2)$$

where the second term is the shifted voltage due to Q_{ox} and the third term is due to ρ_{ox}. ε_{ox} and t_{ox} represent the permittivity and thickness of the oxide, respectively. Moreover, the actual calculation of the V_{FB} is further complicated by the fact that additional sheet

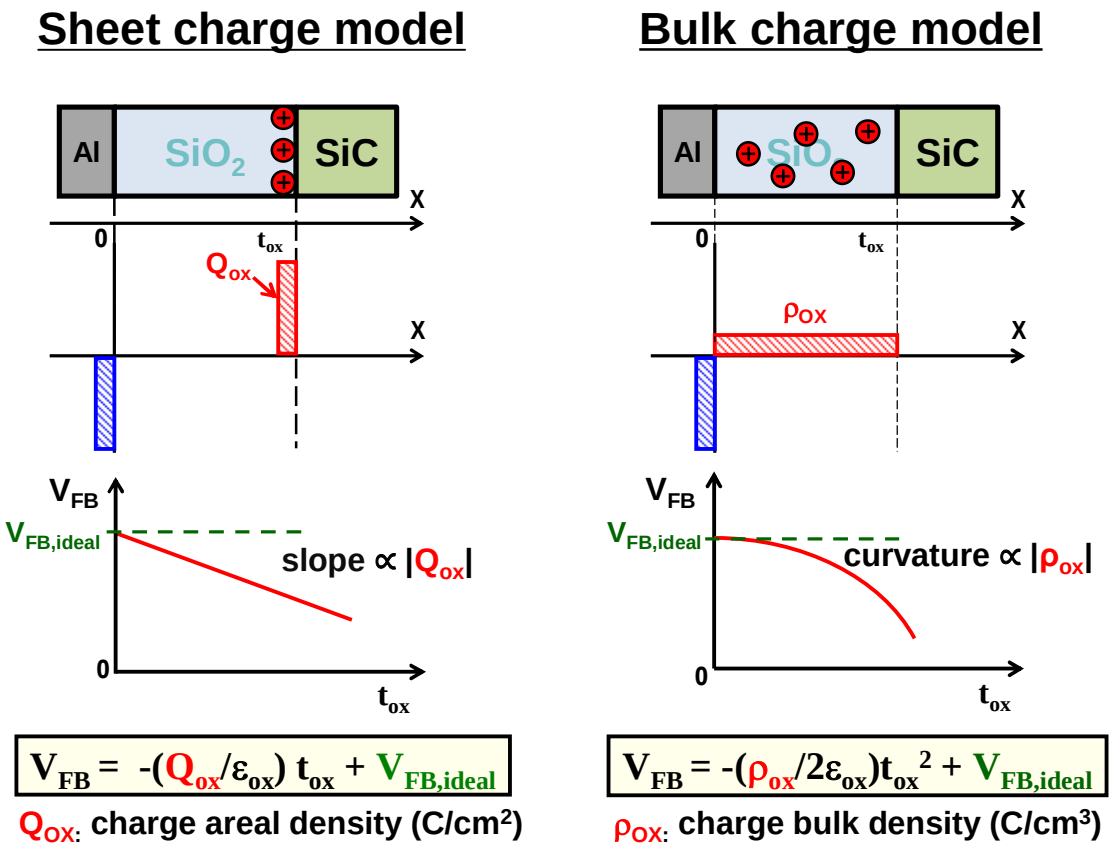

Fig. 4-2 The oxide charge model distribution separated in two categories, *i.e.* sheet charge and bulk charge models. The relation is that the measured V_{FB} is changed as a function of the areal density (Q_{ox}) or bulk density (ρ_{ox}) of oxide charges, and oxide thickness (t_{ox})

charges due to mobile ions (Q_M) can move within the oxides. As shown in Fig. 4-2, the models used for describing the oxide charge density and distribution can be classified into two kinds: bulk charge and sheet charge model. In order to simplify the Eq. 4.2, the relationships of V_{FB} versus t_{ox} for these models are expressed by following equations:

$$V_{FB} = -\frac{Q_{ox}}{\varepsilon_{ox}} t_{ox} + V_{FB,ideal} \tag{4.3}$$

by assuming $\rho_{ox}(x) = 0$ for the sheet charge model,

and $V_{FB} = -\frac{1}{2\varepsilon_{ox}} t_{ox}^{\ 2} + V_{FB,ideal}$ (4.4)

by assuming $\rho_{ox}(x) = \rho_{ox}$ and $Q_{ox} = 0$ for the bulk charge model.

Distribution and density of oxide charges in the SiC-MOS capacitors can be estimated from the plot of correlation between V_{FB} and equivalent oxide thickness (EOT). The C-V characteristics of MOS capacitors provide the actual V_{FB} values. The EOT can be also achieved based on the oxide capacitance (C_{ox}). The slope-shaped oxides make it easy to extract plots of V_{FB} versus EOT of SiC-MOS devices.

4-3 Results and Discussion

4-3-1 Elimination of mobile ions by BTS procedures

Figure 4-3 shows typical bidirectional C-V curves of SiC-MOS capacitors that received BTS and slope etching. In both cases the estimated electrical oxide thickness, *i.e.*, the equivalent oxide thickness (EOT) of the remaining oxide was 26 nm. It should be noted that, as shown in Fig. 4-3(a), the well-behaved C-V curves obtained at room and high temperatures overlap each other, and that the V_{FB} of these capacitors is close to the ideal value. These results imply that positively charged mobile ions in the as-fabricated SiC-MOS structure were accumulated by applying NBTS at the electrode interface and that they were completely removed by wet etching as expected (see Fig. 4-1). All capacitors fabricated on the slope-shaped oxide (EOT: 15 - 35 nm) exhibited a negligible V_{FB} shift and C-V hysteresis at room and high temperatures (see Fig. 4-4), indicating that the positive ions that moved toward the upper surface of SiO_2 by applying NBTS were confined within a tiny portion less than 5 nm in depth and were completely removed by wet etching. On the other hand, the SiC-MOS capacitors that

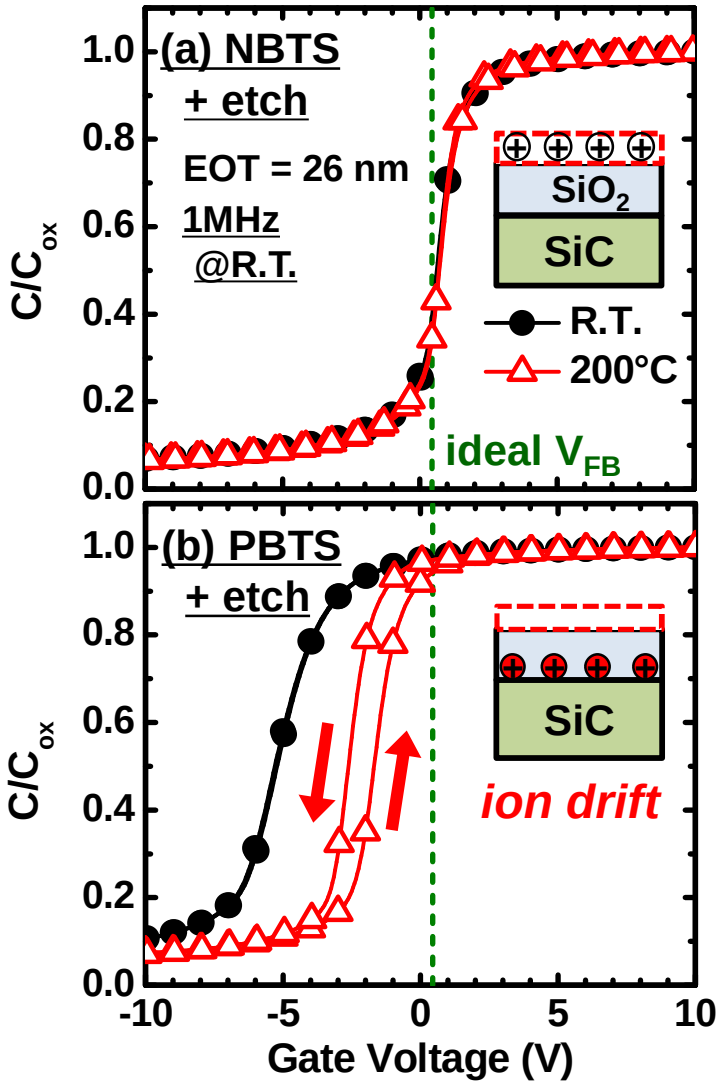

Fig. 4-3 Bidirectional C-V curves of SiC-MOS capacitors with BTS and following oxide etching. The capacitors are (a) one treated by a combination of NBTS and subsequent wet etching and (b) one treated by a combination of PBTS and subsequent etching. The C-V measurements were performed at f = 1 MHz. The vertical axis was normalized by maximum capacitance. Comparable EOT values of the measured capacitors are approximately 26 nm.

received PBTS before wet etching exhibited a marked negative V_{FB} shift and counter-clockwise C-V hysteresis comparable to that of the as-fabricated capacitor (Fig. 4-3(b)). This suggests that almost all the mobile ions remained in the oxide. Therefore, we conclude that unusual counter-clockwise C-V hysteresis in SiC-MOS devices is attributable to diffusion of positively charged ion species and that a combination of NBTS and subsequent removal of the uppermost oxide is quite beneficial for achieving BTI-free SiC-MOS devices. As shown in Fig. 4-4, all PBTS capacitors show the

magnitude of counter-clockwise C-V hysteresis at 200°C of about 1 V, which is comparable to the as-fabricated sample (data not shown). This indicates that almost all mobile ions remained in the oxide.

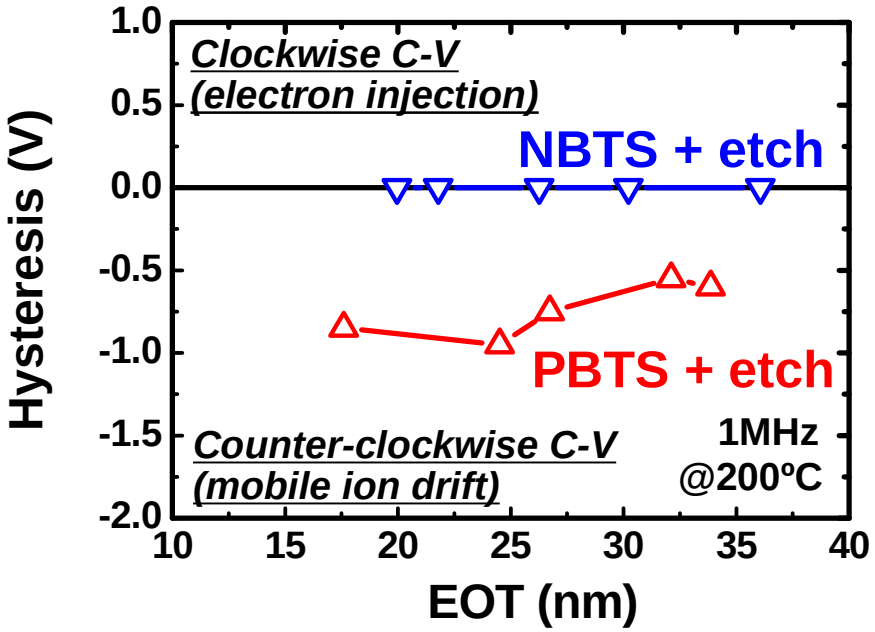

Fig. 4-4 Oxide thickness dependent C-V hysteresis of SiC-MOS capacitors with NBTS (blue downward triangles) and PBTS (red downward triangles) with subsequent etching. Horizontal axis represents the EOT from C-V curves. Vertical axis shows the magnitude of C-V hysteresis, in which positive direction denotes clockwise hysteresis corresponding to electron injection and negative direction denotes counter-clockwise hysteresis corresponding to ion drift.

4-3-2 Distribution and density of mobile ions

Distribution and areal density of the positive mobile ions in the SiC-MOS capacitors were evaluated from the relationship between V_{FB} and EOT [12]. The V_{FB} positions of the capacitors were estimated from high-frequency (1 MHz) C-V curves taken at room temperature, and were cross-checked with $1/C^2$ versus V_G plots at depletion states in order to determine accurate V_{FB} values [7,13] for the case when shallow defects near the conduction band edge (E_c) lead to the significantly stretched-out C-V curve shown in Fig. 4-3(b). The slope-shaped oxide makes it easy to extract the EOT versus V_{FB} relationship of SiC-MOS capacitors fabricated under various conditions (see Fig. 4-5). Positive V_{FB} values of as-oxidized samples without POA

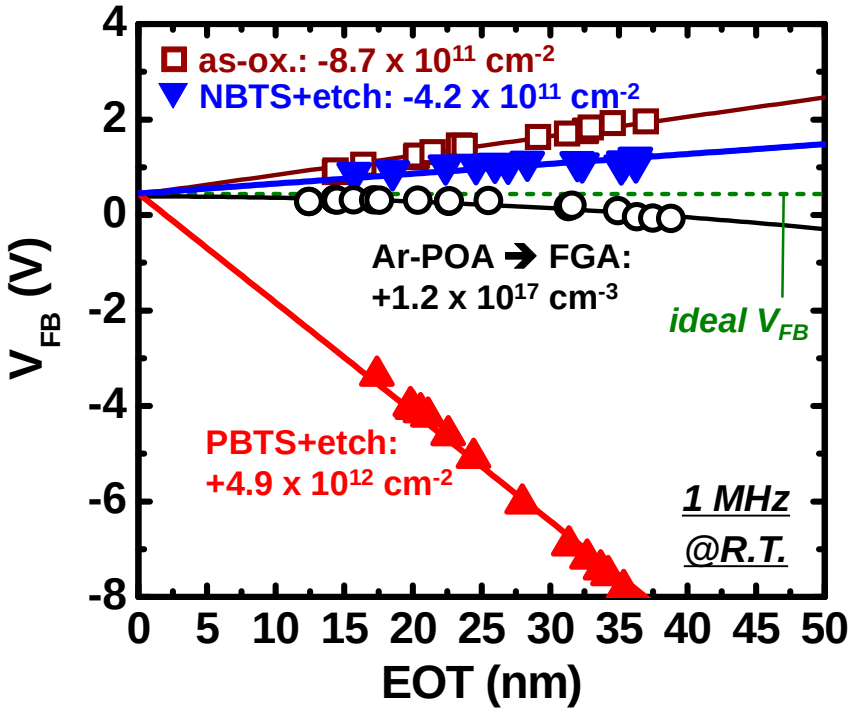

Fig. 4-5 Relationship between V_{FB} and EOT values of fabricated SiC-MOS capacitors. The V_{FB} positions were estimated from high-frequency C-V curves and cross-checked with $1/C^2$ versus V_G plots at depletion state. The amount of fixed charges localized at SiO_2/SiC interfaces was estimated by fitting data with linear lines for the as-oxidized (brown open squares), NBTS with subsequent etching (blue filled triangles), and PBTS with subsequent etching (red filled triangles) samples. Downward parabolic fitting was used for the as-fabricated (Ar-POA and FGA-treated) sample to extract the volume density of positive charges distributed throughout the SiO_2 layer. The obtained areal and volume densities of fixed charges in the gate oxides are shown. The ideal V_{FB} position (0.44 V) of the SiC-MOS capacitor is depicted with a green dashed horizontal line.

treatment (as-ox.; brown open squares) are a distinctive feature of thermal oxides grown on SiC substrates containing negative fixed charges probably due to carbon related defects [14]. The EOT versus V_{FB} plots are fitted well with a linear line having a positive slope and a Y-intercept of about 0.4 V that is close to the ideal V_{FB} of the SiC-MOS capacitor. These results reveal that negative fixed charges with areal density of about 8.7×10^{11} cm^{-2} were located at the SiO_2/SiC interface. It has been previously reported, the large amount of interface fixed charges accounts for the poor quality of as-oxidized SiO_2/SiC interfaces. Moreover, while a combination treatment of Ar-POA and FGA passivated the negative fixed charges, it resulted in a slight negative V_{FB} shift

from the ideal position (see black open circles in Fig. 4-5). In this case, a parabolic curve rather than a linear line reproduced the obtained data, which implies uniformly distributed positive charges with volume density of 1.2×10^{17} cm^{-3} throughout the oxide (newly generated positive mobile ions). As demonstrated, NBTS and subsequent wet etching of the uppermost SiO_2 layer is an effective way to eliminate positive mobile ions generated by the high-temperature FGA. Judging from the EOT versus V_{FB} plots of the corresponding capacitors (NBTS + etch, blue filled triangles), we found that almost half of the negatively charged defects (4.2×10^{11} cm^{-2}) could not be passivated by the combination treatment of Ar-POA and FGA, and still remained at the SiO_2/SiC interfaces. In other words, the V_{FB} positions of the Ar-POA and FGA-treated SiC-MOS capacitors were balanced by the unpassivated negative charges at the SiO_2/SiC interface and the newly generated positive mobile ions in the oxide. In contrast, after pushing all the mobile ions to the bottom interface by applying PBTS, the significant negative V_{FB} values (red filled triangles) were fitted well by a linear line with negative slope, which corresponds to positive charges of about 4.9×10^{12} cm^{-2} at the bottom interface. Furthermore, since the Y-intercept of all fitted lines is identical to the ideal V_{FB} position, we conclude that BTI phenomena in the SiC-MOS devices are explained by both the unpassivated negative fixed charges at the SiO_2/SiC interface and the positive mobile ions, and that, therefore, the modulation of energy band offset at SiO_2/SiC interface induced by electrical stressing and an interface dipole has a minor impact on BTI phenomena in SiC-MOS devices.

4-3-3 Additional BTS experiment on mobile ion free SiC-MOS

In order to establish the validity of the above explanation and the proposed method for eliminating self-generated mobile ions, we conducted an additional BTS experiment. After fabricating SiC-MOS capacitors by BTS and subsequent oxide etching in the same manner as shown in Fig. 4-1, additional BTSs with opposite biasing polarities were applied. Figure 4-6 shows a comparison of high-frequency C-V curves of SiC-MOS capacitors treated by applying additional BTSs in the opposite order. As shown in Fig. 4-6(a), when the positive mobile ions were completely eliminated from the oxide by NBTS and subsequent etching, the C-V curves of the NBTS-applied capacitor (NBTS) and that with the subsequent PBTS (NBTS + PBTS) showed sufficient electrical stress stability, indicating that the removal of positive mobile ions from the gate oxide is an extremely effective measure for solving the unusual BTI problem of SiC-MOS devices. In contrast, NBTS was applied on the PBTS capacitor

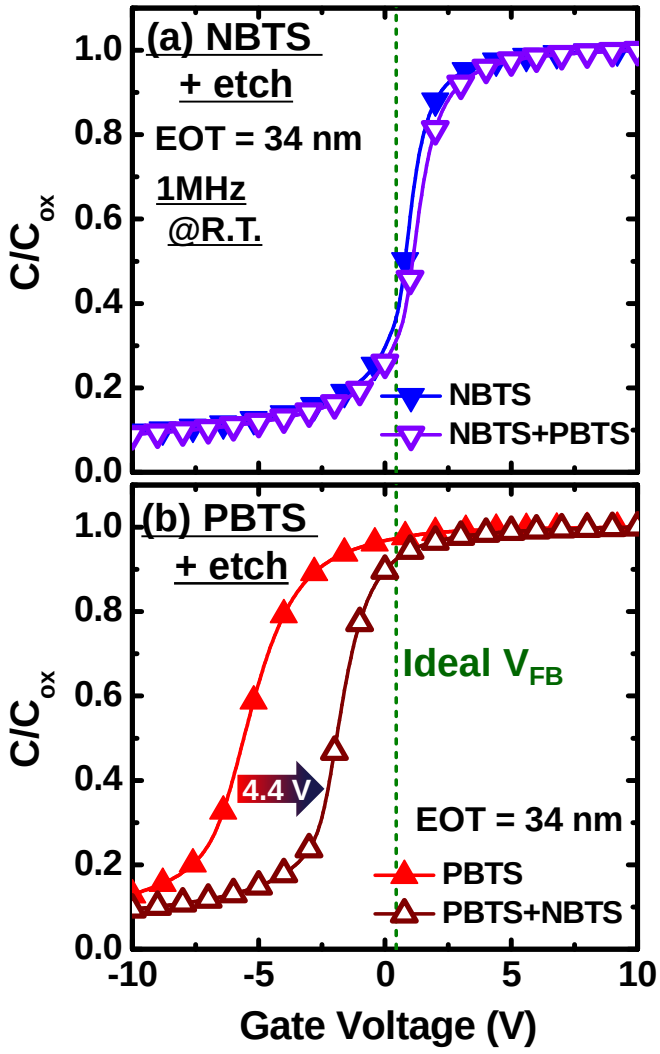

Fig. 4-6 Comparison of high-frequency C-V curves obtained before (filled symbols) and after additional BTSs with opposite stressing polarities (open symbols) on the stressed SiC-MOS capacitors. MOS capacitors with NBTS and subsequent oxide etching (w/o mobile ions) and with PBTS and subsequent etching (mobile ions at SiO_2/SiC interface) were prepared using the procedure shown in Fig. 4-1. Then, additional (a) PBTS (+10 V) and (b) NBTS (-10 V) were applied at 200°C to the NBTS and PBTS capacitors, respectively. EOT of the measured SiC-MOS capacitors was 34 nm for both cases.

with mobile ions at SiO_2/SiC interface. Figure 4-6(b) indicates a significant V_{FB} shift (ΔV_{FB} = 4.4 V) toward the theoretical value. Meaning that, the remaining mobile ions at the SiO_2/SiC interface of PBTS-applied capacitor were found to move upward with the subsequent negative gate biasing (PBTS + NBTS). These results validate our explanation for BTI in SiC-MOS devices caused by self-generated mobile ions in the

thermally grown oxides. In addition, the improvement of C-V shape was observed. These results demonstrate the recovering of the device characteristics after mobile ions were moved apart from the SiO_2/SiC interfaces.

4-3-4 Evidences of interface degradation by mobile ions

Considering the interface property of the stressed samples showing in Fig. 4-7, the interface state density (D_{it}) estimated by conventional high-low method did not change after performing NBTS and subsequent etching (no mobile ion), but rather significantly increased by PBTS (mobile ions at SiO_2/SiC interfaces). This suggests that some of the mobile ions may act as electron traps at SiO_2/SiC interface. In addition, the recovery of D_{it} value was observed for the PBTS capacitor with additional NBTS (PBTS+NBTS in Fig. 4-7). Furthermore, the NBTS sample indicates that the density of interface traps near conduction band edge (E_c-E: 0.3 – 0.45 eV) is much lower than the as-fabricated

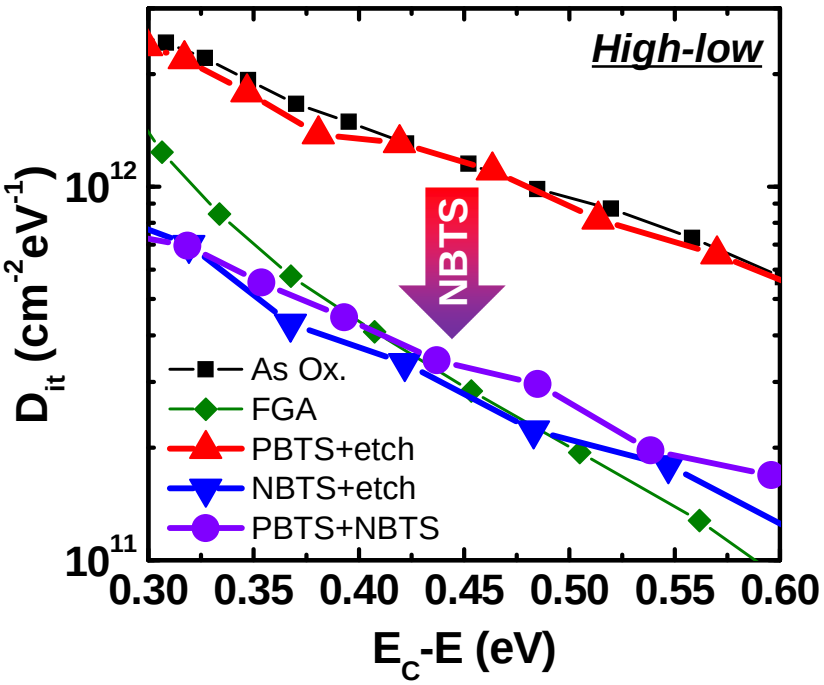

Fig. 4-7 Energy distribution of interface state density (D_{it}) estimated by conventional high-low method for the SiC-MOS capacitors. Regardless of the decreased D_{it} by high-temperature FGA, mobile ion elimination (NBTS + etch) further reduced interface traps at the energy levels near conduction band edge (Ec-E: 0.3-0.45 eV). On the other hand, accumulated mobile ions at SiO_2/SiC interfaces (PBTS + etch) drastically increase D_{it}. Nevertheless, the D_{it} value could be further decreased by performing NBTS (PBTS + NBTS).

sample. Meaning that, by eliminating all mobile ions from the oxide and mobile ions near the passivated SiO_2/SiC interface, the interface property got further improvement as compared with the initial FGA-treated sample which contains mobile ions. Although a supported evidence on near-interfacial mobile ion affecting SiO_2/SiC interface properties has not yet been reported, based on the preliminary results, may these positive mobile ions are one of the important factors which alter a carrier trapping/detrapping at the interface. Further evidences are discussed in chapter 5.

4-4 Summary

We reported in Chapter 3 that the extrinsic metal contaminations originating from process equipment can be ruled out as a possible cause of mobile ions. In addition, with physical analyses such as dynamic secondary ion mass spectrometry (D-SIMS) and x-ray photoelectron spectroscopy (XPS) we were unable to detect such a small amount of mobile ion species in the oxide. At present, we believe that carbon-related complexes exhibiting positive fixed charge in the gate oxide induce structural changes in SiC-MOS interfaces to increase D_{it}. In any case, the problem of intrinsic mobile ions causing interface degradation and V_{FB} shift in SiC-MOS systems is an urgent issue that should be earnestly addressed in the actual production of high-mobility and reliable SiC-MOSFETs.

In chapter 4, we have investigated additional evidences of BTI phenomena in SiC-MOS devices. Our extended work has revealed that FGA treatment generates positive ions spreading throughout the thermal oxide and that they move at elevated temperatures by applying gate bias. It was found that positive mobile ions with an areal density of several 10^{12} cm^{-2} were accumulated by PBTS at the bottom SiO_2/SiC interface and severely deteriorated the interface quality of SiC-MOS devices, indicating adverse effects of mobile ions on both the reliability and performance of SiC-MOSFETs. Moreover, we demonstrated complete removal of the harmful self-generated mobile ions with the NBTS and subsequent oxide etching and improved the reliability and interface quality of SiC-MOS devices.

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Chapter 5 Degradation of Thermal SiO_2/SiC Interface Properties due to Mobile Ions

In this chapter, the impact of mobile ions intrinsically generated in thermally grown SiO_2 by high-temperature forming gas annealing (FGA) on the SiO_2/4H-SiC interface properties was studied by means of electrical characterization of SiC metal-oxide-semiconductor (MOS) capacitors. Unlike Si devices, mobile ions located at the interfaces were found to create a remarkable stretch-out of capacitance-voltage (C-V) curve near the accumulation condition, and the degree of stretch-out was more pronounced with increasing probe frequency. This suggests that the interface states with a long emission time constant are formed near the conduction band edge due to the mobile ions. To clarify this unusual phenomenon, several characterization techniques to evaluate interface state densities (D_{it}), including Terman, conductance, and C-ψ_s methods, were employed. The D_{it} values estimated for SiO_2/SiC interfaces with mobile ions were a few times as large as those without mobile ions.

5-1 Introduction

In the Chapters 3 and 4, we have found positively charged mobile ions which intrinsically contained in thermal oxides after dry oxidation of SiC substrate, and POA under diluted hydrogen ambient so called forming gas annealing (FGA) [1,2]. Moreover, it is found that these mobile ions may involve in shallow defect generation near the conduction band edge (E_c). The interface degradation due to mobile ions was pointed out in Chapter 4 by stretch-out shapes of C-V curves and increase interface state density (D_{it}) estimated by the conventional high(1 MHz)-low method (see Fig. 4-7). However, the complexity of the trap behaviors such as time constants can not be understood by this traditional method. Additional interface characterization is necessary for further disclosing the trap generation mechanism.

In this chapter, we investigated the impact of mobile ions on interface properties in FGA-treated SiO_2/4H-SiC structures by utilizing bias-temperature stress to control the distribution of mobile ions in the oxides. The density of generated interface traps was characterized by various techniques including Terman, conductance, and C-ψ_s methods.

5-2 Experimental

5-2-1 Fabrication of 4H-SiC MOS capacitors with elimination of mobile ions

We fabricated SiO_2/SiC capacitors with or without mobile ions in thermally grown SiO_2 on 4H-SiC(0001) substrates with an n-type epilayer ($N_d = 1 \times 10^{16}$ cm^{-3}). After the SiC substrate was cleaned by a conventional RCA procedure, a sacrificial oxide was grown at 1100°C for 1 hour and then stripped by hydrofluoric acid (HF) solution. 40-nm-thick SiO_2 was formed by thermal oxidation in dry-O_2 ambient at 1100°C for 12

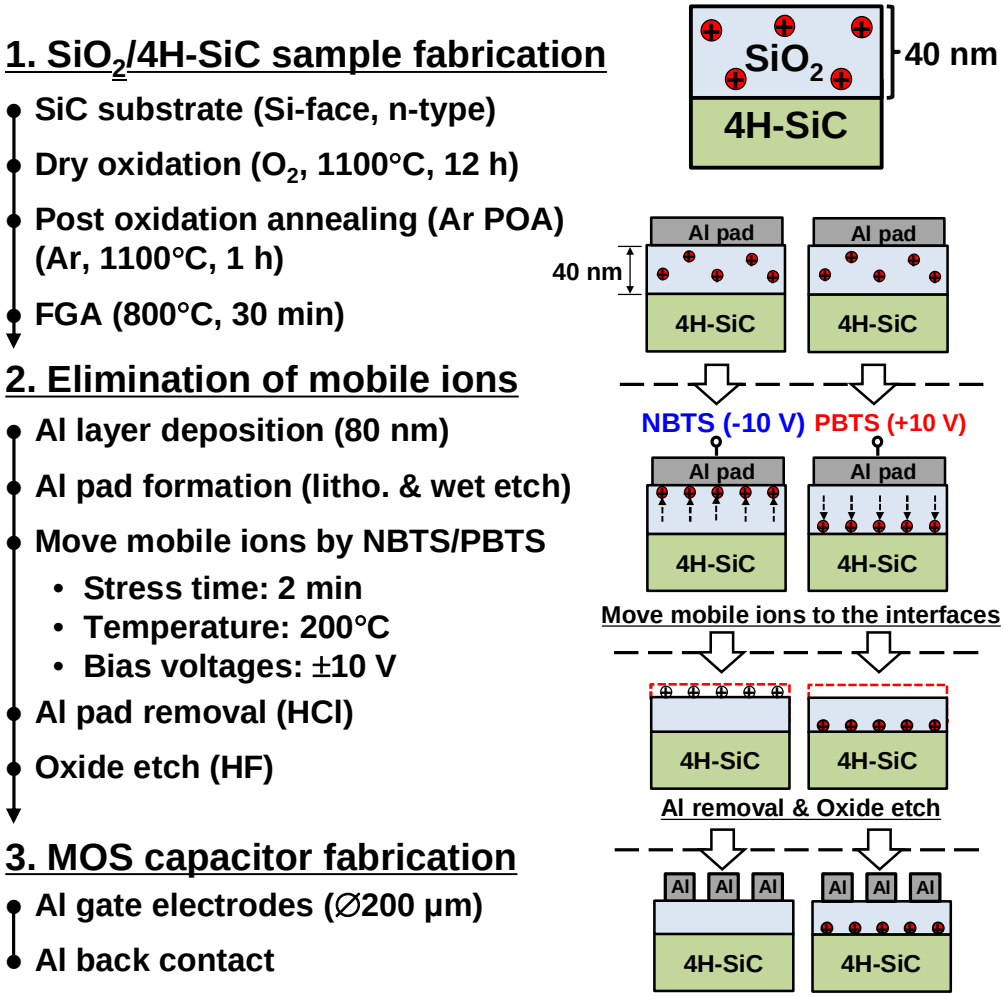

Fig. 5-1 Procedure for fabricating SiC-MOS capacitors with/without mobile ions. NBTS and PBTS were applied at 200°C for 2 min with large rectangular Al pads and kept during cooling down to room temperature to accumulate mobile ions at the top and bottom interfaces. Then, the gate oxides were etched by dipping into 1% HF solution. Finally, small Al electrodes were deposited to produce a number of MOS capacitors.

h followed by POA in Ar ambient at 1100°C for 1 h. Subsequently, high-temperature FGA in 3% H_2/N_2 ambient was performed at 800°C for 30 min and then at 450°C for 30 min similarly to previous chapters. Mobile ions were assumed to be generated in the SiO_2 layers despite the improved interface quality due to the hydrogen passivation.

To control the amount and distribution of mobile ions in SiC-MOS capacitors, we employed the following technique for eliminating mobile ions proposed in Chapter 4. After forming large Al pads on SiO_2 films, positive and negative bias-temperature stresses (PBTS and NBTS) of constant ±10 V were applied at 200°C for 2 min to move mobile ions towards SiO_2/SiC and Al/SiO_2 interfaces, respectively. Mobile ions were immobilized by keeping the bias stresses while cooling down to room temperature (R.T.). After removing the Al pads, the samples were dipped into a 1% HF solution for a short time, resulting in oxide layers with and without mobile ions depending on the BTS condition. Finally, Al gate electrodes and back contacts were deposited to fabricate SiC-MOS capacitors.

5-2-2 Evaluation of interface state density

There is a broad variety of procedures that are commonly used to obtain the information about interface trap states for Si-based MOS devices. Nevertheless, as discussed in the introduction chapter, the C-related defects are believed to be the main reason for performance degradation of SiC-MOS devices. Hence, a larger number of trap states is supposed to exist at SiO_2/SiC interfaces compared to that in the Si devices. Furthermore, the nature of traps, *i.e.* time constants is likely to be much different from the conventional traps due to Si-dangling bonds. A suitable method should be able precisely to detect the broadest cross section of trap state time constants. Several techniques were recently applied and modified to estimate the D_{it} and its distribution in the bandgap of SiC. In this chapter, the energy distributions of D_{it} were obtained based on Terman, conductance, and C-ψ_s methods.

5-2-2-1 Terman method

Terman method is one of the traditional techniques for determining interface trap density of Si-based MOS devices [3]. The core basis of this method relies on high-frequency capacitance-voltage (C-V) measurement at room temperature of MOS capacitors. The scheme was introduced under the assumption that the interface traps cannot response under sufficiently high frequency probe oscillation. In other words, if

the response of interface states is relatively slow under the measurement frequency, the traps cannot emit the captured carriers to be then detectable by the probe measurement. This slow-responded interface trap phenomenon cannot contribute to increasing in probe capacitance (C_p) of high-frequency C-V curves, but rather, these significant number of interface traps can cause a non-parallel V_G shift of C-V curves shown by marked "stretch-out" (see Fig. 5-2).

The theoretical C-V curve is necessary for the calculation of D_{it} at a given surface potential (ψ_s). The D_{it} can be deduced by the following equation:

$$D_{it} = \frac{C_{ox}}{e^2 \frac{d\Delta V_G}{d\psi_s}}, \tag{5.1}$$

where the voltage shifts (ΔV_G) between the experimental high-frequency C-V and the theoretical curve is compared as given by V_G–V_{ideal}. C_{ox} is the oxide capacitance, and e is the elementary electric charge. The detection of Terman method is limited to the shallow energy states of $D_{it} > 10^{10}$ cm^{-2} eV^{-1}, in which the time constant is considerably slow with respect to high frequencies. The quality of high-frequency C-V characteristics determines the accuracy of D_{it} estimation. Moreover, the measurement frequency should be adequate to capture sufficient traps.

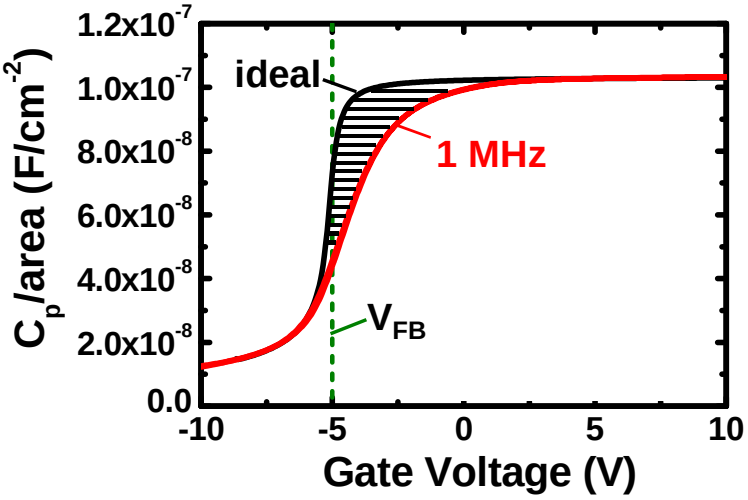

Fig. 5-2 Comparison between high-frequency (1 MHz) and ideal C-V curves measured on SiC-MOS capacitors. The traps do not respond to increase C_p, but parallel shift the V_{FB} to cause a stretch-out C-V curve.

5-2-2-2 Conductance method

The conductance change of the MOS capacitors is another signal that can infer to the capture and emission phenomena of carriers in the interface traps [3]. The conductance method has been one of the most promising techniques applied to detect the trap states in SiC-MOS capacitors. The benefit of this approach is that the voltage shifts due to slow-responded traps and majority carrier injection are considerably neglected because the D_{it} is estimated in the depletion and weak inversion mode.

The process is begun with the measurement of equivalent parallel conductance (G_p) at an angular frequency ($\omega=2\pi f$). The experimental G_p/ω versus ω curve shown in Fig. 5-3 is fitted with theoretical curve given by the following equation [4,5]:

$$G_p/\omega = e^2 S D_{it} \int_{-\infty}^{+\infty} \frac{\ln(1+(\omega\tau\exp(\eta))^2)}{2\omega\exp(\eta)} \times \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(\frac{\eta^2}{2\sigma^2}\right) d\eta , \qquad (5.2)$$

where the D_{it}, the time constant of the interface states (τ), and the standard deviation (σ) are well-defined as the fitting parameters. S is the gate electrode area. It should be

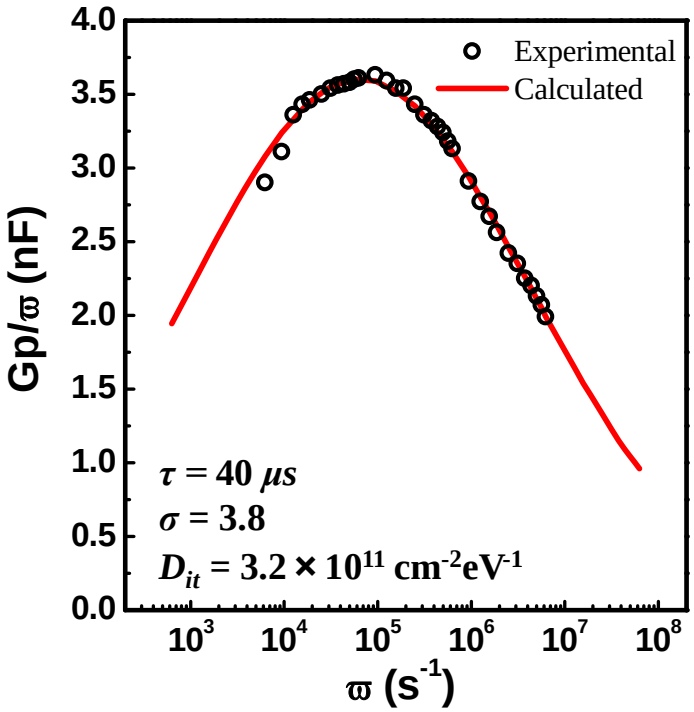

Fig. 5-3 The plots of relationship between G_p/ω and ω of the experimental result of SiC-MOS capacitors (black circle). The calculated curve (red line) is fitted by Eq. 5.2 with the parameters such as time constant (τ), standard deviation (σ), and interface state density (D_{it}).

noticed that the approximate expression of D_{it} according to the bell-shaped peak (D_{it} = $2.5/e(G_p/\omega)_{max}$) cannot be assumed for the SiC-MOS structures because high density of interface defects with different time constants causes the broader peak. Moreover, the measurement frequency should be highly enough to capture particular interface states with very fast time constant. For example, the unknown interface states generated by annealing in NO_x can be only recognized by conductance measurement with frequency near 100 MHz [6].

5-2-2-3 C-ψ_s methods

The generation of interface traps with a broad range of time constants due to existed complex carbon defects at SiO_2/SiC interfaces cannot be completely detectable by conventional methods, *e.g.* high-low, Terman, conductance. In order to capture very fast states in the shallow energy level under the E_c, the measurement frequency (*f*) must be higher than that is usually used to characterize Si-MOS devices. For examples, the conventional high-low method cannot completely emit the trapped carriers from the interface states of as-oxidized SiO_2/SiC by *f* = 1 MHz, therefore, trap density is underestimated (see Fig. 5-4).

The conventional high-low method assumes the theoretical curves based on probe capacitances measured at 1 MHz in which the interface state capacitance (C_{it}) cannot completely excluded in the following equation:

$$D_{it} = (C_s + C_{it})_{QS} - (C_s + C_{it})_{high-low} / Se^2, \quad (5.3)$$

where C_s is the semiconductor capacitance. Although the actual D_{it} value for the SiO_2/SiC systems is possible by increasing *f* to around 100 MHz (dash line in Fig. 5-4), the accuracy of very high frequency measurement is drastically degraded by an increase in probe parasitic impedances [6,7]. Nevertheless, the capture of total trap density is possible by the C-ψ_s method which was recently proposed by Yoshioka *et al.* (bold line in Fig. 5-4) [7]. The method provides accurate values for the surface potential (ψ_s) and the sum of semiconductor and interface state capacitance (C_s + C_{it}) based on the depletion capacitance (C_{dep}) as given by:

$$1/C_{dep}^2 \approx 1/(C_s + C_{it})^2 = -2\psi_s / S^2 \varepsilon_{SiC} e N_d, \quad (5.4)$$

where N_d is the donor concentration of the SiC substrate. Unlike high-low method, the D_{it} value is deduced from discrepancy between low-frequency (quasi-static) and ideal (theoretical) C-V curves. Therefore, the all interface traps including very fast states (>1 MHz) can be evaluated precisely as described in the following equation:

$$D_{it} = (C_s + C_{it})_{QS} - C_{s,theory} / Se^2 . \quad (5.5)$$

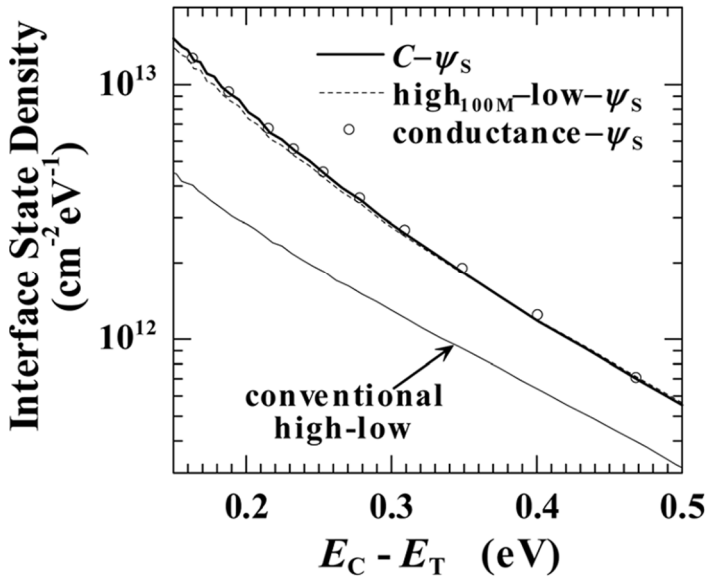

Fig. 5-4 Distributions of the interface state density evaluated by various methods for the same n-type SiC-MOS capacitor with a 32-nm-thick oxide formed by dry oxidation at 1300°C [7].

5-3 Results and Discussion

5-3-1 Stretch-out of capacitance-voltage (C-V) curves

As shown in Fig. 5-5, the preliminary mobile ion effects were again confirmed by bidirectional capacitance-voltage (C-V) curves measured at R.T. (black circle) and 200°C (red triangle). The applied gate voltage (V_G) was swept forward from depletion (–10 V) to accumulation (10 V) and then backward to depletion (–10 V). C-V curves of the sample with NBTS and subsequent etching measured at both temperatures overlap each other without hysteresis (Fig. 5-5(a)). This means that mobile ions were removed from the oxide while maintaining the good interface property attributed to FGA. In

contrast, the PBTS sample exhibits a large negative V_{FB} shift and counter-clockwise C-V hysteresis at high temperature (Fig. 5-5(b)), indicating that positively charged mobile ions remained at the SiO_2/4H-SiC interface after PBTS and moved again at 200°C.

Figures 5-6(a) and (b) show the high-frequency and ideal C-V curves (black line) for NBTS and PBTS samples. The V_{FB} positions (green dashed lines) were determined based on $1/C^2$ versus V_G plots under the depletion condition. A stretch-out of 1 MHz C-V curves was observed in the V_G ranging from flatband to accumulation for both samples. The stretch-out of C-V curves is considered to be due to the electron trapping into interface states with long emission time constants near the conduction band edge. Note that this trap responds very slowly to the probe frequency (f = 1 MHz), thus contributing not to the increase of additional capacitances but to the shift of C-V curves. The difference between 1 MHz and ideal C-V curves for the PBTS sample (Fig. 5-6(b)) is larger than that for the NBTS sample, meaning that the mobile ions at the SiO_2/4H-SiC interfaces may induce a generation of additional interface states. Figure 5-6(c) shows the frequency dispersion of C-V curves for the PBTS sample containing mobile ions. It should be noted that the measured C-V curve still exhibits stretch-out even for a lower frequency, indicating that there is not enough time for the trapped electrons to emit from interface states even at 1 kHz. Thus, we can conclude that mobile ions in FGA-treated SiC-MOS structures mainly lead to the generation of slow interface states near the E_c.

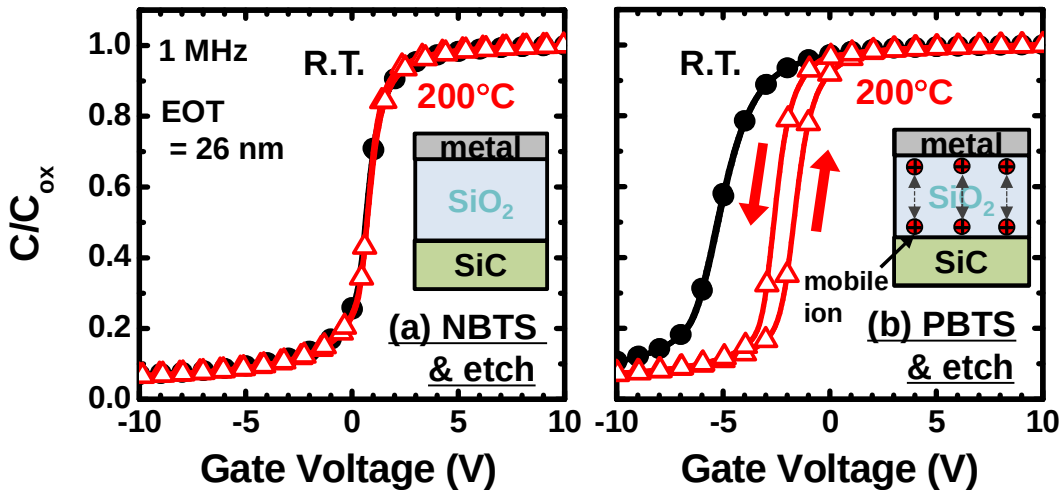

Fig. 5-5 Bidirectional C-V curves of SiC-MOS capacitors with (a) NBTS and (b) PBTS and subsequent SiO_2 etching measured at R.T. (black circle) and 200°C (red triangle). The EOT of these samples is about 26 nm.

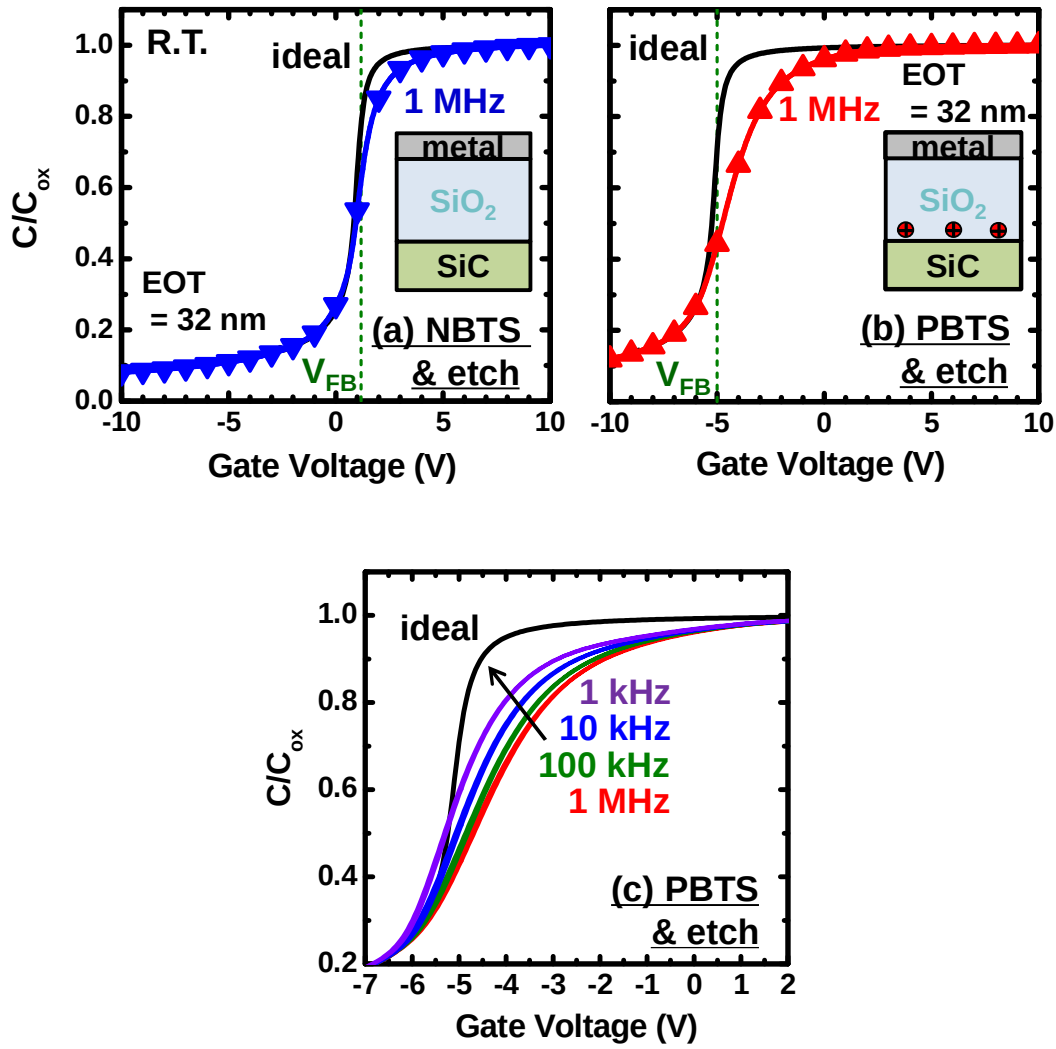

Fig. 5-6 High-frequency (1 MHz) C-V curves measured at R.T together with the calculated ideal curves for SiC-MOS capacitors with (a) NBTS and (b) PBTS and subsequent SiO_2 etching. (c) Frequency-dependent C-V characteristics of the PBTS sample. The EOT of these samples is 32 nm.

5-3-2 Slow trap density distribution

Next, we evaluated the D_{it} by the Terman method based on the C-V measurement in Fig. 5-6. The density of slow electron traps can be estimated by Eq. 5.1 based on voltage shifts between ideal and 1 MHz C-V curves. The accurate V_{FB} positions of the ideal C-V curves were deduced from $1/C^2$ versus V_G plots at depletion states of the corresponded 1 MHz C-V curves. As shown in Fig. 5-7, an increase in D_{it} near the conduction band edge, especially above the Fermi level (E_F) or E_c-E < 0.19 eV, was

observed for the PBTS sample containing mobile ions at SiO_2/SiC interfaces (PBTS & etch). Although fast interface states contributing to an additional capacitance may cause an underestimation of the density of slow interface states, the trap density was estimated to be approximately 2×10^{12} cm^{-2} eV^{-1} at the E_c. In contrast, the NBTS sample (NBTS & etch) did not show any significant change in D_{it} compared to the sample without BTS (FGA only), and the estimated D_{it} values are about half of that for the PBTS samples. These results indicate that the interface quality of FGA-treated SiC-MOS structures is drastically degraded by mobile ions at the SiO_2/SiC interfaces.

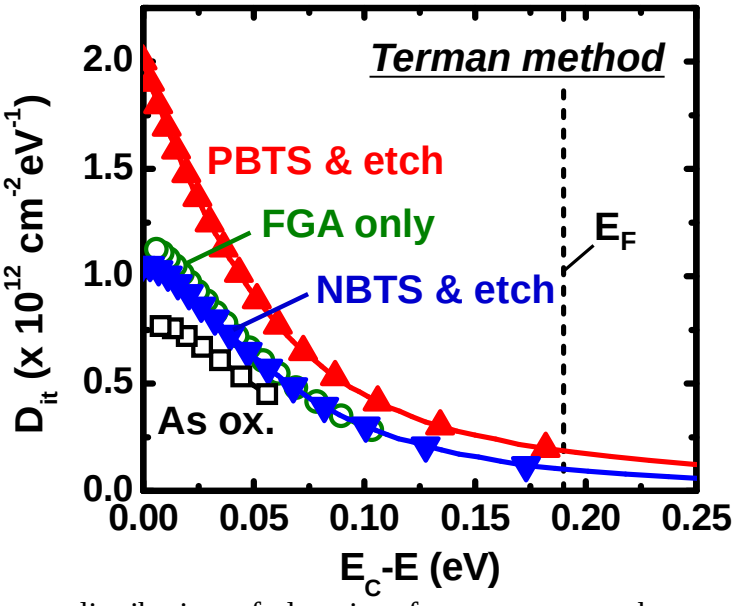

Fig. 5-7 Energy distribution of slow interface states near the conduction band edge (E_c) estimated by Terman method for the SiO_2/SiC interfaces with and without BTS. The SiC-MOS capacitors containing mobile ions (PBTS & etch) show the increase in trap density above the Fermi level (E_F).

5-3-3 Density and time constant of interface states

To further examine the effect of mobile ions on the SiO_2/4H-SiC interface properties, we conducted other D_{it} extractions based on the conductance method. These methods usually provide the D_{it} distribution at deeper energy levels typically below E_F. Figure 5-8 shows the experimental curve fitting of relationships between G_p/ω and ω with respect to Eq. 5.2. The G_p/ω peak intensity of a Gaussian curve indicates the traps density and the peak position of the curve represents the emission time characteristic.

The energy distributions of the fitting parameters, *i.e.* D_{it}, time constant (τ), and standard deviation (σ) are illustrated in Figs. 5-9(a), (b), and (c), respectively. In Fig.

5-9(a), after mobile ion elimination by NBTS and subsequent oxide etch (NBTS & etch), the trap density was significantly lower than the PBTS samples (PBTS & etch). In contrast, the interface quality of PBTS SiC-MOS structures was degraded after moving mobile ions to the bottom interfaces. The conductant method could significantly detect newly-generated interface traps at E_c-E from 0.3 to 0.5 eV. Furthermore, the time constant of ion-induced interface states at E_c-E around 0.3 eV were approximately three times faster than that of trap states at FGA-treated SiO_2/SiC interfaces without mobile ion (Fig. 5-9(b)). The time constants of the states at similar energy levels below E_c were roughly 20 times decreased by mobile ions as compared with those at the as-oxidized SiO_2/SiC interfaces (Fig. 5-10) [7]. This result indicates that the mobile ions may affect the electron trapping/emitting at interface states. Nevertheless, as shown in Fig. 5-9(c), the values of σ are approximately 3 – 4 for the SiC-MOS capacitors regardless of BTS polarities and similar to those for as-oxidized SiC-MOS capacitors (see Fig. 5-10). We could imply that the interface defect centers for the unusual generated mobile ions may be originated from the same origins for the common defects at SiO_2/SiC interfaces.

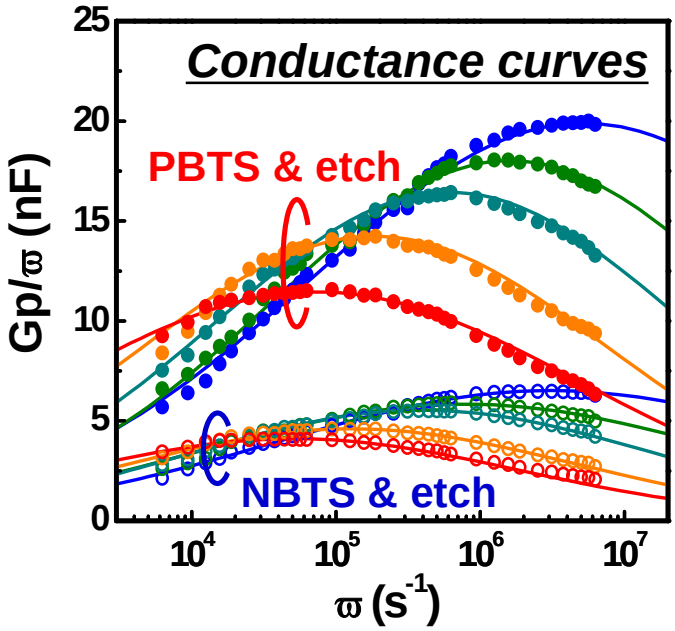

Fig. 5-8 Curve fittings of the experimental G_p/ω versus ω plots for the SiC-MOS capacitors with (PBTS & etch) and without mobile ion (NBTS & etch). The peak intensities and positions are varied by the amount and the time constant of trap states at SiO_2/SiC interfaces.

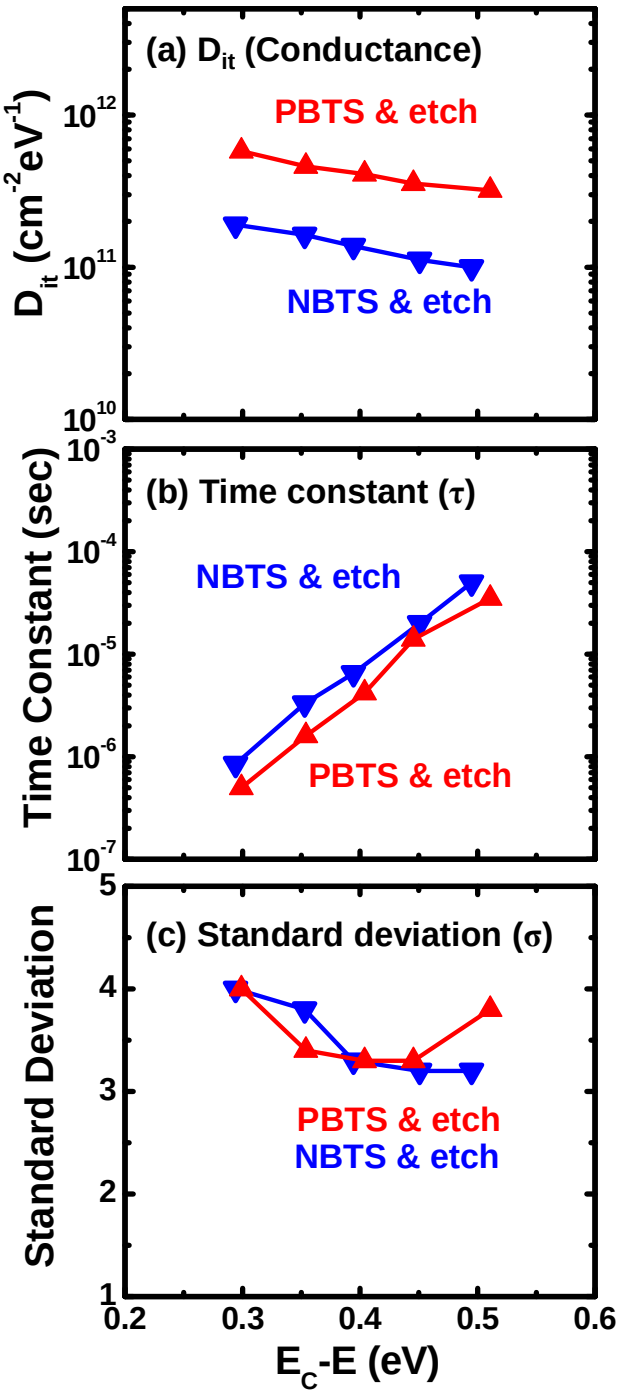

Fig. 5-9 Fitting parameters *i.e.* (a) interface state density (D_{it}), (b) time constant (τ), and (c) standard deviation (σ) as a function of E_c-E of the NBTS and PBTS samples. These parameters are optimized to fit the experimental G_p/ω versus ω plots by Eq. 5.2 (see Fig. 5-8).

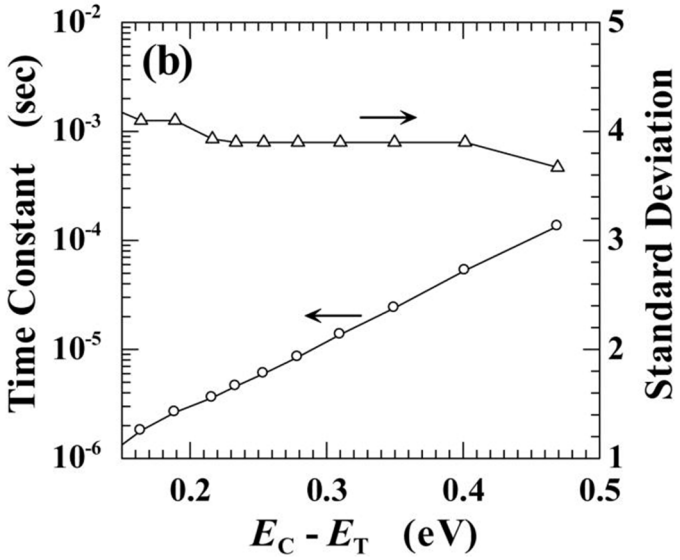

Fig. 5-10 Energy distribution of fitting parameters *i.e.* time constant (τ), and standard deviation (σ) of the as-oxidized capacitors reported by Yoshioka et al. [7]. The parameters were obtained by fitting G_p/ω versus ω plots.

5-3-4 Total interface trap density

Although the conventional methods were used to extract the D_{it} of MOS devices, the accurate estimation of total interface states at SiO_2/SiC interfaces is very difficult because of very fast interface traps which respond to very high-frequency (over 1 MHz) bias oscillation. In this part, we, therefore, used a recently proposed C−ψ_S method described at the beginning of this chapter to estimate total density of interface traps. Figure 5-11 represents the energy distribution of D_{it} estimated by using the C−ψ_S method for SiC-MOS capacitors. The D_{it} of as-oxidized sample (as-ox.) decreased by post annealing in FG (Ar-POA→FGA). After eliminating the mobile ions by NBTS and subsequent oxide etching, the density of the interface traps apparently decreased especially for traps near the conduction band edge (see NBTS & etch). This result demonstrates that the interface quality of FGA-treated SiC-MOS structures got further improvement by removing mobile ions from the thermal oxides. However, mobile ions at the SiO_2/SiC interfaces increased density of interface states (see PBTS & etch). These experimental findings clearly indicate that the mobile ions are a crucial cause of interface degradation in SiC-MOS devices. Furthermore, mobile ion elimination with NBTS and subsequent oxide etching is beneficial for further improving SiC-MOS interfaces.

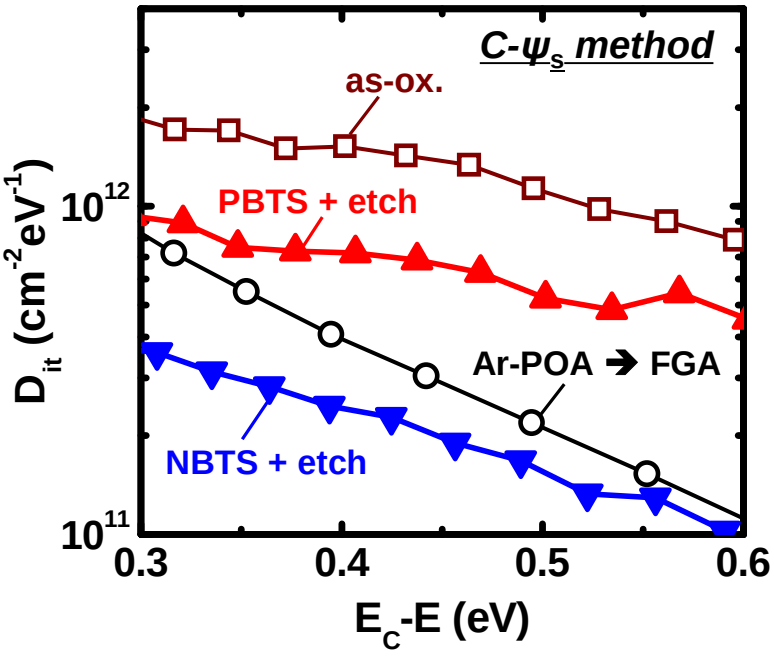

Fig. 5-11 Energy distribution of D_{it} for the SiC-MOS capacitors evaluated in Fig. 5-6. The D_{it} values were extracted by using the C−ψ_S method [7]. Thermal oxide grown on SiC substrate (as-ox.) was first treated with Ar-POA and FGA (Ar-POA →FGA). Then, NBTS or PBTS was applied before wet etching the oxide surface. Positive mobile ions were removed by NBTS and subsequent oxide etching (NBTS + etch), whereas mobile ions remain at the bottom interface for the SiC-MOS capacitor treated with PBTS and subsequent etching (PBTS + etch).

5-3-5 Discussion on interface trap generation induced by mobile ions

As illustrated in Fig. 5-12, energy distributions of D_{it} are summarized from the results obtained in this chapters. Regardless of evaluation methods, the D_{it} values estimated for the PBTS sample containing mobile ions at the interfaces were larger than that for the NBTS sample. Especially for the C-ψ_s method, which can detect entire interface states regardless of capture/emission time constants, it is suggested that the mobile ions located at the interfaces generate additional interface states with various time constants. The slightly lower D_{it} for the conductance method than for the C-ψ_s method would be due to the presence of slow traps. In contrast, the sample after NBTS and subsequent etching shows a smaller amount of D_{it}, indicating the excellent interface quality. It should be noted that the significant interface trap buildup due to PBTS-induced damages was not observed in the capacitors without mobile ions. Even though, further studies are needed to reveal the mechanism of the mobile ions causing

interface degradation, our experimental findings suggest that positively charged mobile ions located at SiO_2/SiC interfaces may form interface defects or act as the electron traps.

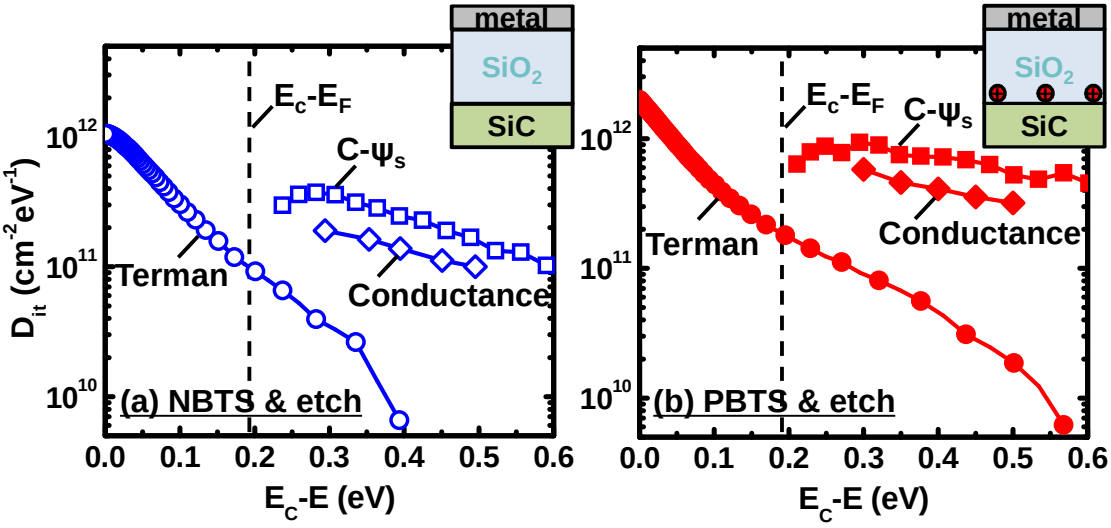

Fig. 5-12 Comparison of energy distribution of D_{it} estimated by Terman, conductance, and C-ψ_s methods for SiC-MOS capacitors fabricated with (a) NBTS and (b) PBTS with subsequent etching.

5-3-6 Energy band alignment modulation induced by mobile ions

Many evidences of unusual mobile ion generation in thermal oxides on SiC were reported in this thesis. As mentioned in previous chapters, positively charged mobile ions were intrinsically contained within the thermal oxides with a density of several 10^{12} cm^{-2} after performed interface treatment by high-temperature FGA. Although the improved interface quality due to hydrogen passivation was clearly observed shown by reduced in C-V hysteresis and D_{it} (see Fig. 3-5), it is considered that the electrical characteristics at high-temperatures of the same FGA-treated samples exhibit severe reliability degradation due to mobile ion drift. In this section, the further demonstration of mobile ions affected energy band alignment of SiO_2/SiC structures were done based on synchrotron XPS at SPring-8 [8] similarly to those performed in Chapter 2. The thermal oxides with thickness of about 40 nm were grown on 4H-SiC(0001) in dry O_2 at 1150°C for 4 h followed by subsequent Ar-POA at the same temperature for 1 h. Mobile ions were intrinsically formed in the oxide by FGA at 800°C for 30 min as similar to previous studies. Then, mobile ions were controlled by positive or negative bias-temperature stress (PBTS or NBTS) to be accumulated at the SiO_2/SiC interfaces

or to entirely be removed from the SiO_2 with subsequent oxide etching (referred to Fig. 5-1). The wet etching was conducted with 1% HF solution to remain 3 nm-thick oxides which is suitable for XPS analysis.

Regardless of mobile ions, the oxide energy bandgaps were equally 8.7 eV estimated based on O 1s energy loss spectra (Fig. 5-13). This indicates that the bandgap of thermal oxides is not a function of mobile ions. Furthermore, the estimation of ΔE_c of these PBTS and NBTS samples were also achieved based on valence band spectrum analysis shown in Fig. 5-14. The increase in ΔE_c of 0.05 eV in PBTS sample from that of FGA samples observed in Chapter 2 (Fig. 2-12(b)) is probably due to the mobile ions at SiO_2/SiC interfaces (Fig. 5-14(a)). We suggest that the mobile ions may generate the interface traps subsequently to capture electrons. On the other hand, the elimination of mobile ions resulted in a better interface quality thus decrease the ΔE_c of 0.1 eV (Fig. 5-14(b)) compared with the PBTS samples. The tradeoff between the improved interface quality and poor gate reliability due to band offset reduction was again demonstrated.

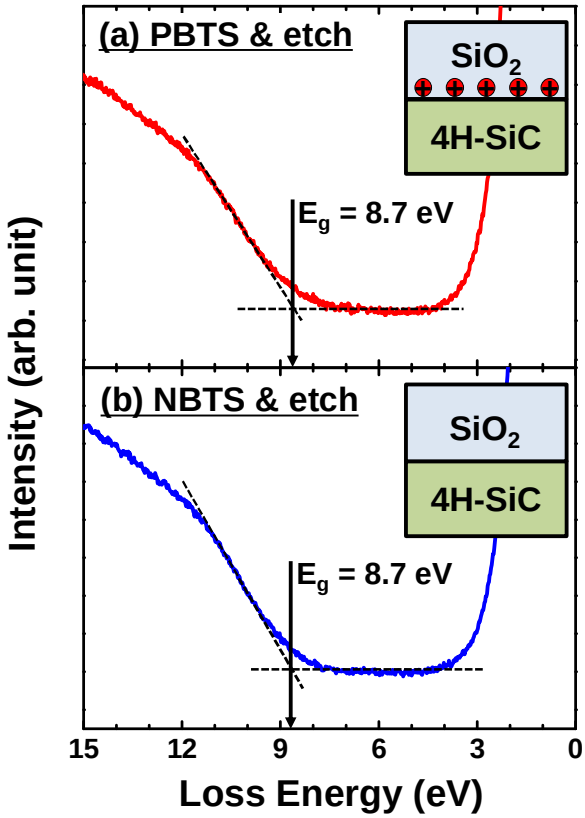

Fig. 5-13 O 1s energy loss spectra for SiO_2/4H-SiC structures (a) with (PBTS & etch) and (b) without mobile ions (NBTS & etch). The onset of the excitation from the valence to conduction bands (bandgap) can be determined from the loss spectra.

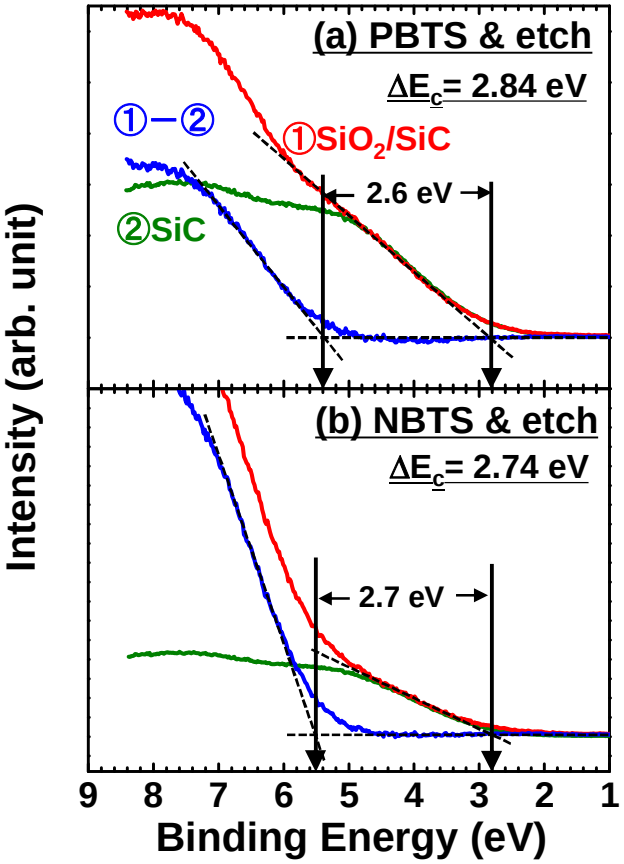

Fig. 5-14 Deconvoluted valence band spectra for SiO_2/4H-SiC(0001) structures (a) with (PBTS & etch) and (b) without mobile ions (NBTS & etch). Since valence band spectra were the sum of SiO_2 layer and SiC bulk, spectral deonvolution was performed using valence band spectrum taken from the reference SiC substrate.

5-4 Summary

Several electrical characterizations were conduced for SiC-MOS capacitors with/without the mobile ions to understand their effects on SiO_2/SiC interface properties. Although well-behaved high frequency C-V curves were observed for the SiC-MOS capacitors without mobile ion, the samples with mobile ions at the interface exhibited serious stretch-out C-V curves, especially near the accumulation condition. This suggests that a large amount of slow interface states near the conduction band edge was formed by mobile ions at the SiO_2/4H-SiC interfaces. In addition, an increase in D_{it} with various time constants due to mobile ions was confirmed by the Terman, conductance and C-ψ_s methods. Moreover, the mobile ions at SiO_2/SiC interfaces partially recover

the ΔE_c. As a result, we suggest the tradeoff between interface quality and ΔE_c for thermally grown SiO_2/SiC MOS structures.

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Chapter 6 Improvement of BTI Characteristics in SiC-MOS Devices by Deposited Gate Dielectrics

In this chapter, significant improvement of bias-temperature instability (BTI) characteristics in SiC-based metal-oxide-semiconductor (MOS) devices was demonstrated with high-permittivity aluminum oxynitride (AlON) dielectrics deposited on thin thermal oxides. AlON/SiO_2 stacked dielectrics were found to be useful not only for reducing gate leakage current but also for suppressing diffusion of positively charged ions, leading to stable SiC-MOS characteristics even under strong electric fields and high temperatures. Unlike the prompt electric-field-induced ion migration in thermally grown and sputter-deposited SiO_2 dielectrics, the ion drift for the stacked gate dielectrics was confined within the thin SiO_2 underlayers owing to low ion diffusivity in AlON layers. Impacts of mobile ions on interface properties of SiC-MOS devices and effects of intentional ion trapping within the AlON layers were also systematically investigated.

6-1 Introduction

Considering the accumulation of carbon-related defects at thermal-oxide/SiC interfaces [1,2], one might think that deposited oxides could improve interface properties. Several groups have recently reported SiC-MOS devices using SiO_2 deposition followed by NO or N_2O annealing [3–7]. Devices of this kind exhibit interface quality improvement to some extent, but the large leakage current due to the small conduction band offset at SiO_2/SiC interfaces precludes further improving the reliability of gate stacks with deposited SiO_2 films. Consequently, we think that conventional SiO_2 will be replaced with high-permittivity (high-*k*) dielectrics reducing the electric field across the gate insulators [8]. Aluminum based oxides are widely studied for wide bandgap semiconductor application, but the most common Al-based oxide, alumina (Al_2O_3), has suffered from a fatal problem relating to intrinsic electron traps in the film, especially under strong electric fields. Thus, although Al_2O_3 reduces the leakage current, serious BTI is inevitable in SiC-MOS devices with Al_2O_3 dielectrics.

Previous research on high-*k* gate dielectrics has found nitrogen incorporation to be effective for passivating electron traps in Al_2O_3 films [9] and we have recently reported the use of aluminum oxynitride (AlON) gate dielectrics in SiC-MOS devices in which

thin thermal SiO_2 underlayers were inserted to avoid direct contact between the deposited high-*k* films and SiC substrates (AlON/SiO_2/SiC gate stacks) [10–12]. On the basis of our physical characterizations [2] and numerical simulation [12], thin SiO_2 underlayers ranging from 5 to 10 nm thick were used in the stacked gate dielectrics on SiC with the intention of improving interface quality and reducing gate leakage current under the wide range of gate bias conditions. As expected, AlON/SiO_2 gate stacks improved reliability by reducing the leakage current and making the dielectric breakdown field higher. Although the proposed high-*k* stacked dielectric is advantageous for improving BTI by reduced charge injection into the gate oxides, its merit (or drawback) in terms of ion drift phenomena has not been addressed yet.

In this chapter, the ion drift phenomena were compared in SiO_2 dielectrics with those in AlON/SiO_2 stacked gate dielectrics by taking FGA-induced mobile ions as a practical example of SiC-MOS devices. We investigated ion diffusivity in thermal SiO_2 and deposited AlON layers together with deposited SiO_2 films. Moreover, details of ion drift phenomena were evaluated by changing the bias-stressing conditions and the thickness of the SiO_2 underlayers of the stacked gate dielectrics.

6-2 Experimental

6-2-1 Aluminum oxynitride

As mentioned earlier, reliability improvement is expected by using high-*k* materials, because the electric field in gate dielectric can be reduced. In general, higher permittivity dielectrics have a smaller band gap. Therefore, Al_2O_3, an Al-based high-*k* dielectric is promising due to its wide band gap and high thermal stability. Moreover, it has been reported that the suitable amount of nitrogen incorporation in an alumina film can eliminate the negative fixed charges [9] and electron traps [13]. This motivated this study to use AlON dielectrics.

In this study, the AlON layer was deposited by reactive sputtering of an Al target in N_2/O_2 gas mixtures, and then post-deposition annealing at 800°C was carried out to improve dielectric properties. The stoichiometric analysis of the deposited AlON layer on Si substrates by using x-ray photoelectron spectroscopy (XPS) suggests that the nitrogen content be about 18%, and its distribution was nearly uniform throughout the layer (see Fig. 6-1(a)). From the O 1s photoelectron energy loss spectrum of the AlON film on 4H-SiC substrates shown in Fig. 6-1(b), the energy bandgap was estimated to be 6.6 eV [10].

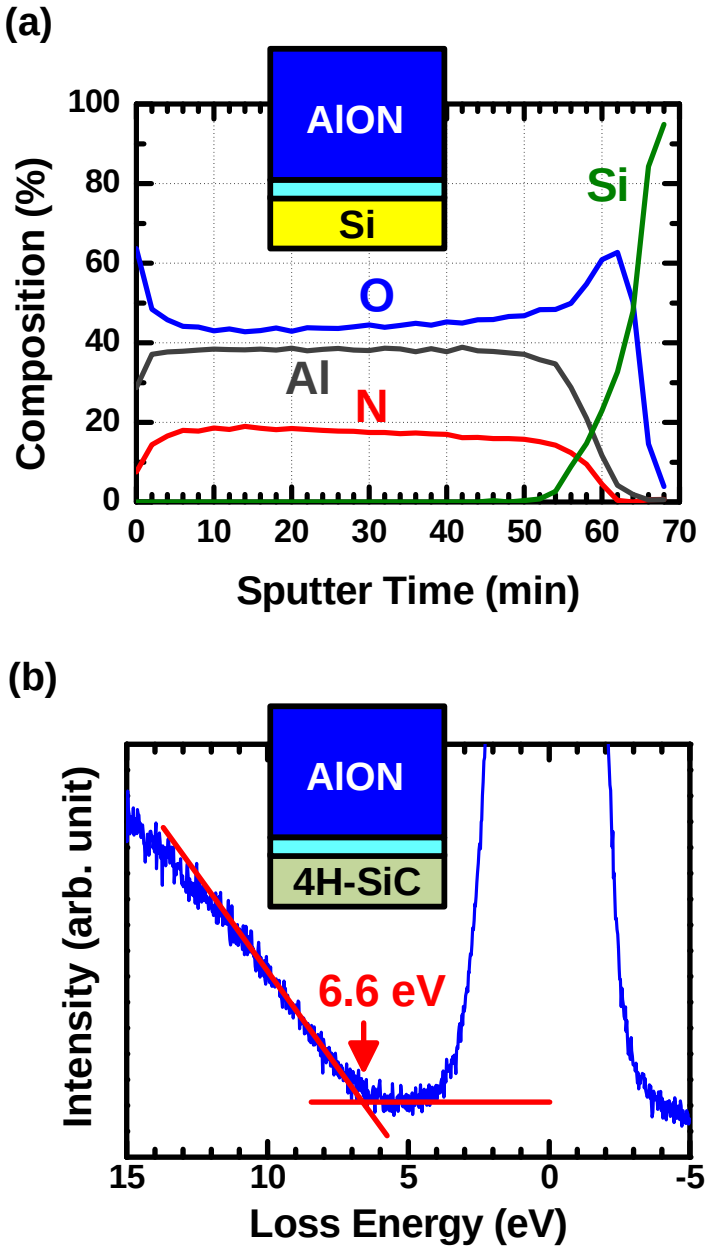

Fig. 6-1 (a) XPS depth profile of AlON layer on SiO_2/Si(100) structure. Nitrogen atoms were uniformly incorporated in AlON layer with an atomic composition of about 18%. (b) O 1s energy loss spectra for AlON film on SiC substrate give AlON band gap of 6.6 eV [10].

6-2-2 Fabrication of stacked gate dielectrics

SiC-MOS capacitors were fabricated with physical-vapor-deposited (PVD) SiO_2 and AlON films grown on thin thermal SiO_2 underlayers (see Fig. 6-2). First, 4H-SiC(0001) substrates with n-type epilayers (N_d = 1 × 10^{16} cm^{-3}) were prepared by

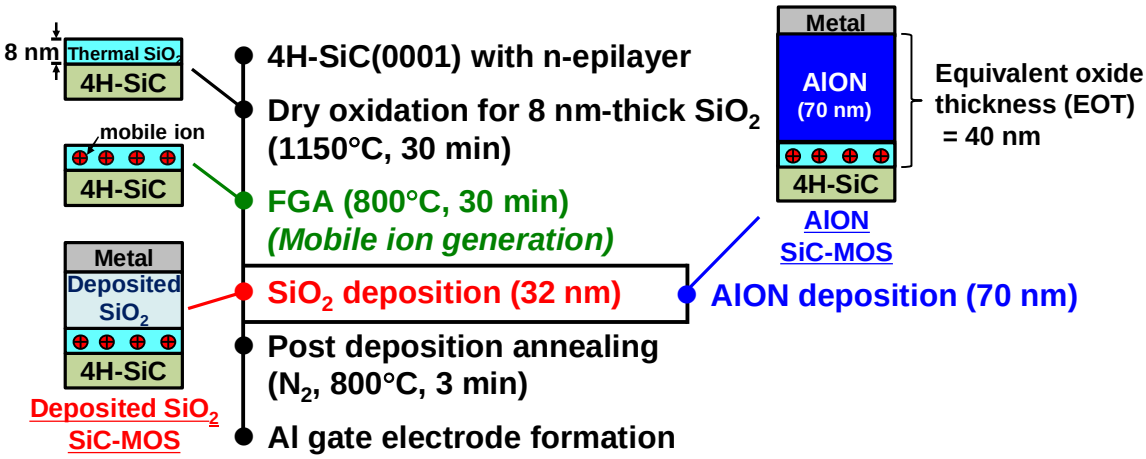

Fig. 6-2 Fabrication procedure used to make SiC-MOS capacitors with PVD SiO_2 and AlON layers grown on FGA-treated SiO_2 underlayers. After the 8-nm-thick thermal SiO_2 layer on a SiC substrate was annealed in forming gas to generate mobile ions, either a 32-nm-thick SiO_2 or 70-nm-thick AlON film was deposited on it to obtain an EOT of about 40 nm. A SiC-MOS capacitor with 40-nm-thick thermal oxide was also fabricated as a reference.

using Piranha (H_2SO_4 + H_2O_2) and RCA cleaning to remove extrinsic contaminations. After sacrificial oxidation and wet removal, 8-nm-thick SiO_2 layers were formed by thermal oxidation at 1150°C for 30 min in dry oxygen (O_2) ambient, followed by POA at 1150°C for 1 h in argon ambient. Then, in light of the result of previous chapters [14,15], high-temperature FGA in diluted (3%) H_2/N_2 ambient was carried out at 800°C for 30 min in order to intentionally produce mobile ions in the thermal SiO_2 and passivate C-related defects with hydrogen [16]. Then, one of two different gate insulators, 32-nm-thick SiO_2 or 70-nm-thick AlON film, was sputter-deposited on the thin SiO_2 underlayer. The equivalent oxide thickness (EOT), about 40 nm, was the same for all of the capacitors. A N_2/O_2 gas mixture with the 0.4% O_2 partial pressure and Al target were used for AlON deposition, and the AlON film was subjected to post-deposition annealing (PDA) at 800°C for 3 min in N_2 ambient [10,11]. Finally, Al gate electrodes and back contacts were deposited by vacuum evaporation. Reference SiC-MOS capacitors with 40-nm-thick thermal oxides were prepared using the same dry oxidation conditions (1150°C) and the same POA and FGA treatments. Capacitance-voltage (C-V) measurements of the SiC-MOS capacitors were conducted using a probe station combined with equipment for rapid heating and cooling. BTI characteristics were evaluated from high-frequency (HF, 1 MHz) C-V hysteresis and flatband voltage (V_{FB}) shift measured after stressing the capacitors with positive and

negative gate bias conditions at 200°C. Details of bias-temperature stress (BTS) procedures will be described later. The density of interface states of SiC-MOS capacitors were extracted from quasi-static (QS) C-V curves by using the recently proposed C- ψ_s method (see Section 5-2-2-3) [17,18].

6-3 Results and Discussion

6-3-1 Mobile ion drift in deposited SiO_2

First of all, ion drift phenomena were studied in SiO_2 gate dielectrics deposited on SiC. Figures 6-3(a) and 6-3(b) show normalized bidirectional HF C-V curves of

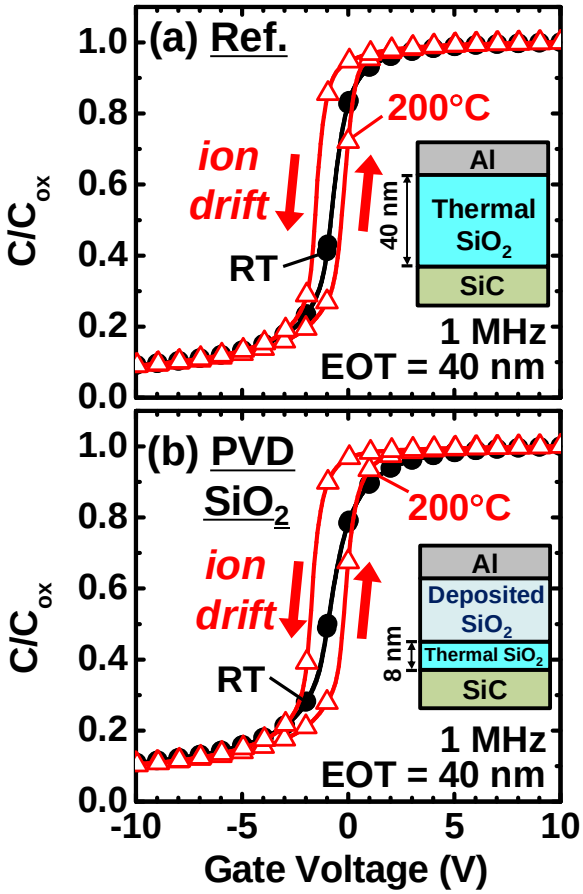

Fig. 6-3 Bidirectional HF C-V curves of SiC-MOS capacitors with (a) thermally grown 40-nm-thick SiO_2 (Ref.) and (b) deposited SiO_2 (PVD SiO_2). Gate voltage was swept from −10 V (depletion) to 10 V (accumulation) and then back to depletion at room temperature (filled black circles) and 200°C (open red triangles). The capacitance values were normalized by the maximum capacitance (C_{OX}). The EOT was the same for all capacitors (about 40 nm).

SiC-MOS capacitors with either a reference 40-nm-thick thermal SiO_2 film or sputter-deposited SiO_2 film on 8-nm-thick thermal oxide underlayer (PVD SiO_2) (see insets in Fig. 6-3). The measurements were conducted at room temperature and 200°C, and the gate bias was swept from −10 V (depletion condition) to +10 V (accumulation condition) and then back to −10 V. As shown in Fig. 6-3(a), while well-behaved C-V curves with negligible hysteresis were obtained in the measurement at room temperature, apparent counter-clockwise hysteresis of 1.32 V was observed in the results obtained at 200°C, indicating mobile ion diffusion in the thermal oxide as same as in previous chapters. It should be noted that counter-clockwise C-V hysteresis was also observed in the results obtained from the PVD SiO_2 sample at 200°C (see Fig. 6-3(b)). The ion drift induced hysteresis shows slightly larger magnitude (1.55 V), meaning that the PVD SiO_2 allows the diffusion of mobile ions from the thermal oxide underlayer and slightly enhanced the mobile ion effect. This indicates that the activation energy for mobile ion diffusion in the PVD SiO_2 seems to be slightly smaller than or equivalent to thermal SiO_2. Nevertheless, PVD SiO_2 film is not an effective barrier to the diffusion of charged ions and is penetrated by mobile ions from the thermal oxide underlayer.

6-3-2 V_{FB} instability in SiC-MOS with deposited SiO_2

Mobile ion diffusion in the SiO_2 gate insulators was further examined by applying positive and negative BTSs (PBTS and NBTS) to the SiC-MOS capacitors, using the method previously described in the third chapter (see Fig. 3-3). After the samples were heated to 200°C, constant gate biases of ±10 V were applied to two capacitors on each sample for 2 minutes. Then the samples were rapidly cooled to room temperature while maintaining the stress bias to freeze mobile ions. Bidirectional HF C-V curves were measured before and after BTSs. As shown in Figs. 6-4(a) and 6-4(b), the bidirectional C-V curves obtained at room temperature exhibited negligible hysteresis, so the generation of carrier trapping site due to BTSs could be ignored. On the other hand, the apparent shift in C-V curves depending on the BTS polarity were observed both for the thermal and PVD SiO_2 samples, which is attributable to diffusion of positively charged mobile ions in the gate oxides. Assuming that most of the charged mobile ions were completely accumulated at the top electrode/oxide and bottom oxide/SiC interfaces with NBTS and PBTS, respectively, we can estimate the sheet charge density from the difference in V_{FB} value. By extracting accurate V_{FB} value based on $1/C^2$ plots in the depletion region [19], we calculated the areal densities of mobile ions (Q_M) in the reference 40-nm-thick thermal oxide and PVD-SiO_2 (32 nm)/thermal-SiO_2 (8 nm) stacked structures to be 2.8×10^{12} and 2.0×10^{12} cm^{-2}, respectively. Because we know

that the PVD SiO_2 layer contains negligible amount of extrinsic mobile ion impurities responsible for the V_{FB} shift, it is concluded that the total amounts of intrinsic mobile ions in the thermal oxides were almost identical regardless of the physical thickness. This suggests that pre-existing defects causing unusual mobile ion generation are mostly localized at thermal-oxide/SiC interfaces, meaning that PVD-SiO_2/thermal-SiO_2 stacked dielectrics are ineffective reducing the number of mobile ions in SiC-MOS structures.

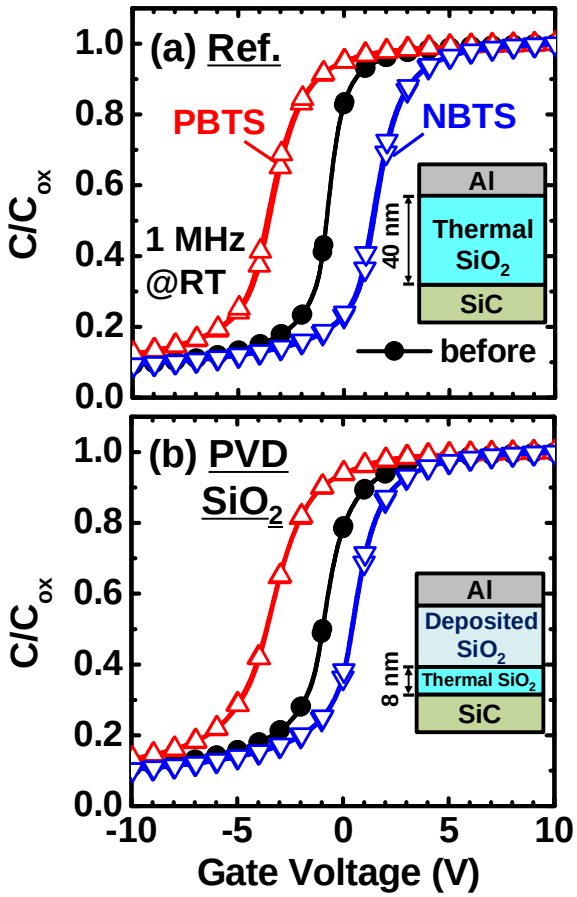

Fig. 6-4 BTI characteristics of SiC-MOS capacitors with (a) thermal and (b) deposited SiO_2 dielectrics examined in Fig. 6-3. Constant positive or negative gate bias of ±10 V was applied to the SiC-MOS capacitors at 200°C for 2 min and it was maintained while the sample cooled to R.T. Then, bidirectional C-V curves were acquired after applying positive or negative BTS.

6-3-3 BTI characteristics improved by using AlON

Next, the reliability of SiC-MOS capacitors with AlON films deposited on thermal oxide underlayers was examined in the same manner. Figure 6-5 shows normalized

bidirectional C-V curves for the AlON sample (AlON (70 nm)/ SiO_2 (8 nm)) which exhibit excellent characteristics at both temperatures. Because the relative permittivity (ε_r) of AlON film (8.5) is higher than that of SiO_2 film (3.9), the same EOT of about 40 nm was obtained with the physically thicker gate insulator. Consequently, gate leakage current was reduced by a few orders of magnitude, especially under strong electric fields [10−12]. Moreover, in contrast to what was observed with SiC-MOS capacitors having thermal and sputter-deposited SiO_2 insulators (Fig. 6-3), the forward and reverse curves completely overlapped each other even at 200°C. This indicates that the deposited AlON layer acted as an effective diffusion barrier and that ion drift was mainly restricted to the thin SiO_2 layer. Considering atomic-scale intermixing between the AlON layer and SiO_2 underlayer during sputter deposition and high-temperature PDA at 800°C, we conclude that the diffusion distance of the charged ions was much less than the initial physical thickness of the SiO_2 underlayer (less than 8 nm). This explains the ideal C-V curves, without any sign of ion drift, obtained for the AlON/SiO_2 stack. In other words, a thin underlayer about 8 nm thick seems to be the most plausible solution to the problem of making reliable SiC-MOS devices.

BTS experiments using the same procedure as those performed for thermal and deposited SiO_2 were also conducted for the AlON/SiO_2 stack. As we expected, moderate BTS (±10 V for 2 min) had only a small effect on the C-V characteristics of a SiC-MOS capacitor with AlON/SiO_2 stacked gate dielectrics (Fig. 6-6). Note that whereas NBTS caused no remarkable change in the C-V curves as compared with the reference device,

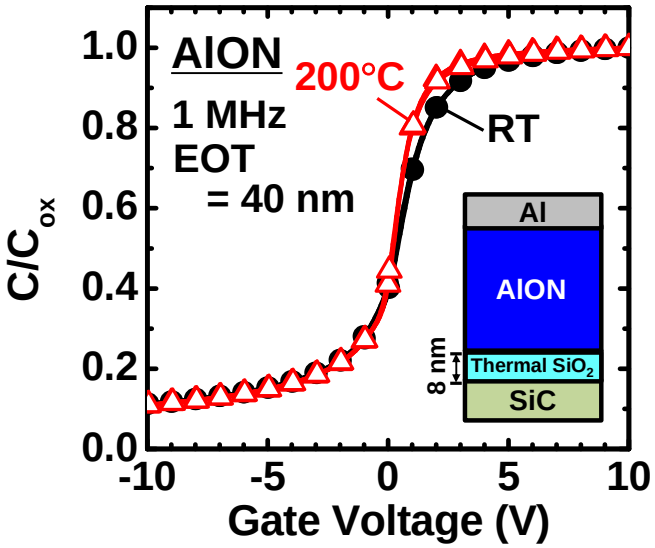

Fig. 6-5 Bidirectional C-V curves of SiC-MOS capacitors with deposited AlON/thermal-SiO_2 (8 nm) stacked gate dielectrics measured at room temperature and 200°C

PBTS resulted in a small V_{FB} shift in the direction opposite that seen when the SiC-MOS capacitor had thermal and PVD SiO_2 insulators (see Fig. 6-4). This positive V_{FB} shift is attributable to slight electron injection that occurred only under the PBTS conditions. Despite this slight electron injection, these BTS experiments demonstrate the superior reliability of SiC-MOS devices with AlON/SiO_2 stacked dielectrics.

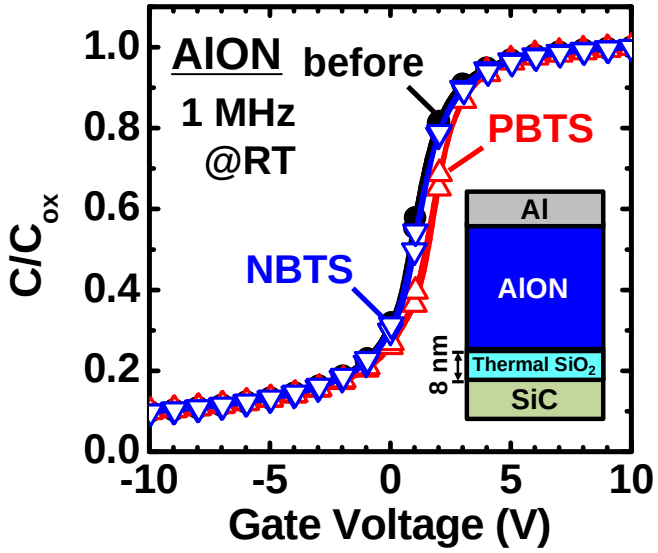

Fig. 6-6 Results of BTS experiments of SiC-MOS capacitors with deposited AlON high-*k* dielectrics using the same procedure as previously described in Chapter 3 (see Fig. 3-3).

6-3-4 Optimized underlayer thicknesses for mobile ion suppression

Furthermore, we investigated ion drift in the AlON/SiO_2 stacked dielectrics and evaluated the effect of accumulated mobile ions on the interface electrical properties in detail. For that purpose, we fabricated additional AlON/SiO_2 samples with physically thicker SiO_2 underlayers (20 nm) and thinner PVD AlON films (50 nm) by only changing the oxidation and deposition times (see Fig. 6-7). Figure 6-8 shows bidirectional C-V curves obtained using the AlON sample with the thicker underlayer, for which a small counter-clockwise C-V hysteresis of 0.35 V was again observed at 200°C, as shown in the inset. This small hysteresis related to the underlayer thickness (compare with results in Fig. 6-3(a), which show a C-V hysteresis of 1.32 V for the 40-nm-thick thermal oxide) means that intermixing at the AlON/SiO_2 interface further restricts the diffusion distance of mobile ions in SiC-MOS structures.

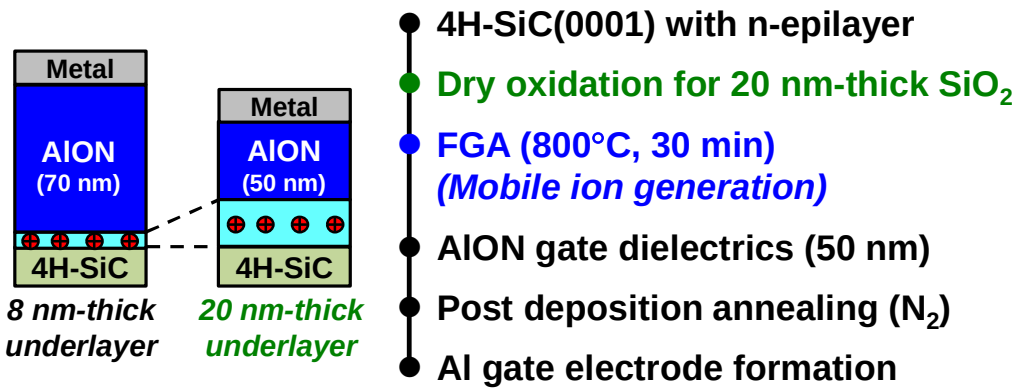

Fig. 6-7 Fabrication procedure used to make AlON SiC-MOS capacitors with increase in thickness of FGA-treated SiO_2 underlayers to enhance mobile ion drift phenomena. The thick underlayer (20 nm) with the deposited AlON (50 nm) stacked dielectrics produced the same EOT of about 40 nm.

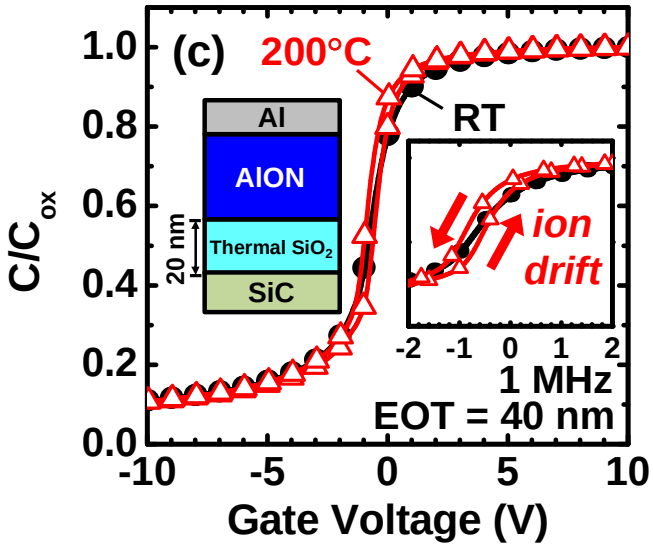

Fig. 6-8 Effects of a relatively thick (20 nm) SiO_2 underlayer on BTI characteristics. The fabrication of the AlON SiC-MOS capacitors with increase in underlayer thickness are described in Fig. 6-7. The inset is an enlargement showing the counter-clockwise C-V hysteresis caused by mobile ion drift within the thick underlaver.

6-3-5 Diffusivity of mobile ions in AlON

Details of ion diffusivity in the stacked dielectrics and the resulting change in interface properties were studied by using the AlON samples with 20-nm-thick SiO_2 underlayers (see Fig. 6-7) and extending the BTS conditions to as much as 10 min showing in Fig. 6-9.

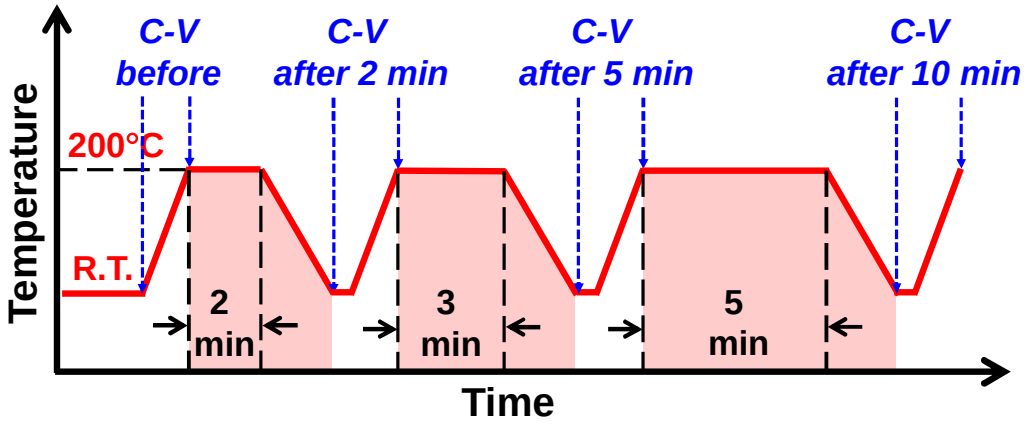

Fig. 6-9 The extended BTS experiments applied for characterizing AlON samples with 20-nm-thick SiO_2 underlayers. The conditions were modified from the inset of Fig. 3-7 by repeating the BTSs for 3 times but the stress times were consecutively changed to be 2 min, 3 min, and 5 min (total stress time is 10 min). After each round, bidirectional C-V curves were obtained at the room temperature and 200°C.

Bidirectional C-V curves of the capacitors obtained at room temperature and 200°C after applying PBTS and NBTS for periods ranging from 2 to 10 minutes is shown in Fig. 6-10. To understand these results, the changes in magnitude of C-V hysteresis, V_{FB}, and D_{it} values with increased BTS time are summarized in Fig. 6-10. The magnitude of C-V hysteresis measured at 200°C after each BTS step is shown in Fig. 6-11(a), where counter-clockwise hysteresis caused by mobile ion drift was seen for all BTS conditions except 10-min NBTS. With PBTS, nearly identical counter-clockwise C-V hysteresis was seen regardless of the BTS time. With NBTS, on the other hand, counter-clockwise hysteresis gradually decreased with each NBTS step and completely disappeared after 10 min of NBTS. Moreover, as shown in Fig. 6-11(b), the tendency of the change in V_{FB} value estimated from $1/C^2$ plots of room temperature C-V curves obtained after BTS was similar to that of the change in C-V hysteresis (Fig. 6-11(a)). These results suggest that at 200°C, while positive ions frozen at the bottom SiO_2/SiC interface by PBTS can again diffuse within the SiO_2 underlayer to cause C-V hysteresis, they slowly penetrate

into the upper AlON layer when long-period NBTS is applied. The positive ions captured within the AlON layer do not contribute to C-V hysteresis anymore. Therefore, it can be concluded that most of the mobile ions in the SiO_2 underlayer diffuse into the upper AlON layer with 10-min NBTS, and they were captured there. Movement of the charge centroid toward the upper gate electrode can be inferred from the change in V_{FB} position approaching the ideal value (0.44 V) after the long-period NBTS (see Fig.

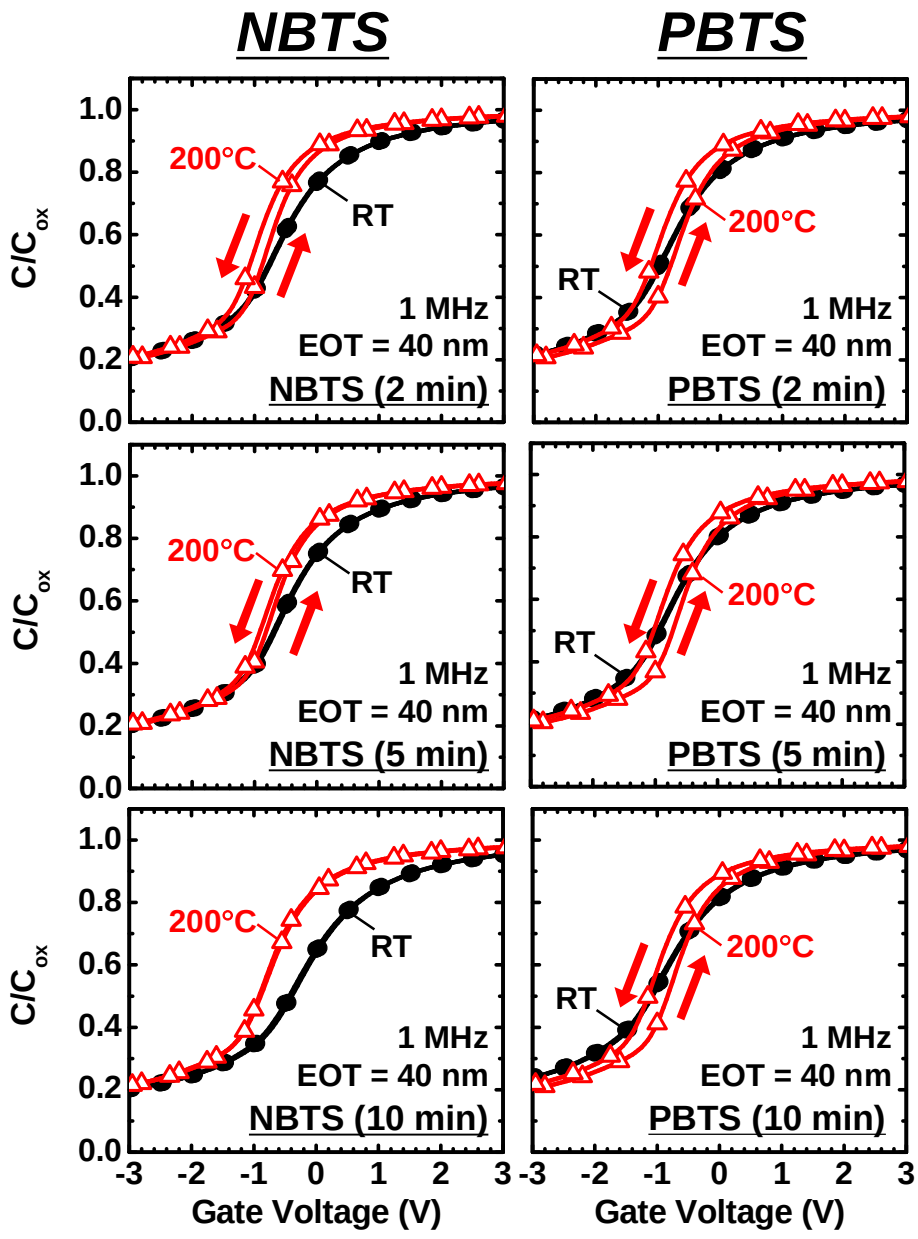

Fig. 6-10 Bidirectional C-V curves at room temperature (filled black circles) and 200°C (open red triangles) observed for the AlON/SiO_2 samples with physically thicker SiO_2 underlayers (20 nm) after performing extended negative and positive BTS process in Fig. 6-9. The probe frequency for C-V measurement was 1 MHz.

6-11(b)). The gently improved BTI characteristics could not be observed in any Ref. samples. As illustrated in Fig. 6-12, we conclude that the mobile ions can diffuse into the deposited AlON layers, but the diffusion coefficient should be significantly small. By continuously performing NBTS, mobile ions can be removed from the bottom oxide layers.

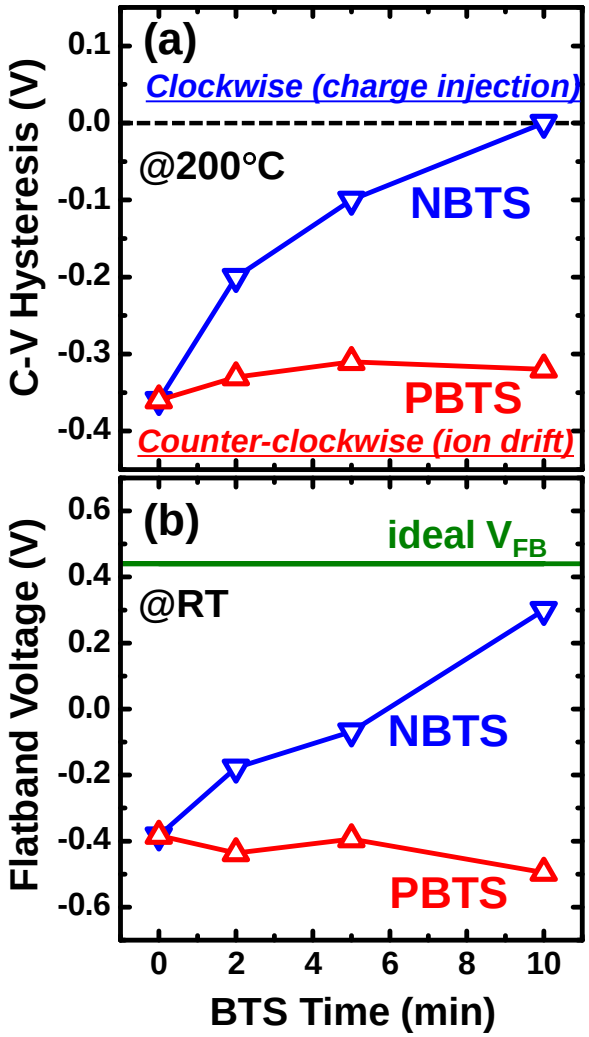

Fig. 6-11 Relation between BTS time and (a) C-V hysteresis and (b) V_{FB} position of SiC-MOS capacitors with AlON/SiO_2 (20 nm) stacked gate dielectrics. PBTS (upward red triangles) or NBTS (downward blue triangles) was applied at 200°C for a certain period and then bidirectional C-V curves were measured at room temperature and 200°C as shown in Fig. 6-9. In Fig. 6-10(a), the vertical axis shows the magnitude of bidirectional C-V hysteresis at 200°C, and the positive and negative values indicate clockwise and counter-clockwise hysteresis, respectively. The ideal V_{FB} position of the SiC-MOS capacitors is indicated in Fig. 6-10(b).

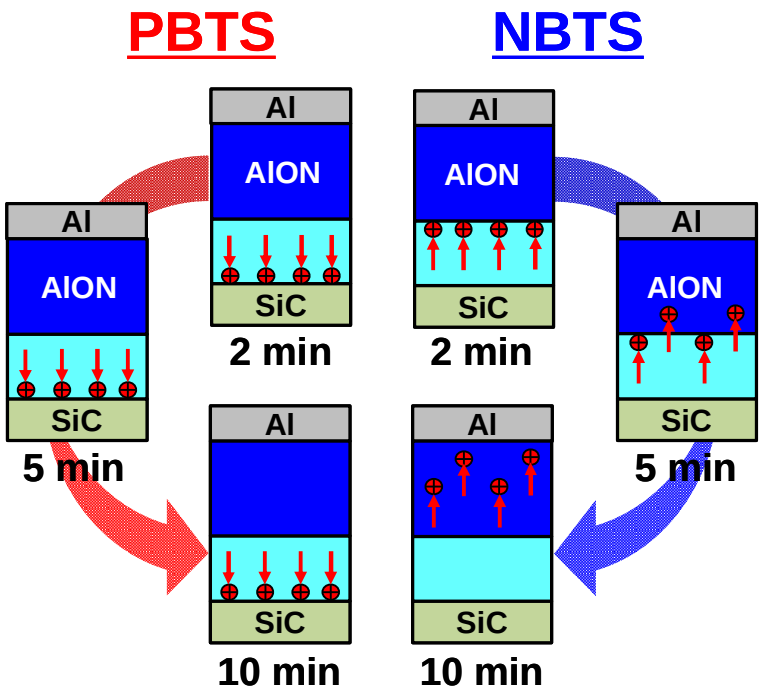

Fig. 6-12 The simple illustration to describe mobile ion diffusion in stacked insulators of AlON/20 nm-thick SiO_2 in SiC-MOS capacitors. The PBTS-applied capacitors exhibit the unchanged number of mobile ions at SiO_2/SiC interfaces. In contrast, although the NBTS-applied capacitors allow the mobile ion penetration into the AlON layers, the mobile ions are then captured within the layer due to the slow diffusion coefficient in AlON.

Finally, the interface properties of the AlON/SiO_2 (20 nm) stacks were characterized after each BTS round by obtaining QS C-V characteristics at room temperature. Base on the C–ψ_s method [17,18], the total trap densities at SiO_2/SiC were evaluated as shown in Fig. 6-12. The increase (or decrease) in D_{it} from the original value by the PBTS (or NBTS) implies that the interface trap generation by mobile ions was again observed [20]. As shown in Fig. 6-14, D_{it} values at E_c–E = 0.3 and 0.6 eV deduced from Fig. 6-13 are plotted as a function of BTS time. Applying PBTS to the AlON/SiO_2 stacked structure apparently increased D_{it} within 2 min. This shows both rapid mobile ion diffusion within the SiO_2 underlayer and additional carrier response in the C-V measurements, that is, carrier trapping and detrapping at the SiC-MOS interface. In addition, a further increase in D_{it} at shallow energy level with extending PBTS was probably due to degradation of the hydrogen-passivated SiO_2/SiC interface induced by significant gate leakage current under the severe PBTS conditions [21]. This conclusion coincides well with the positive V_{FB} shift originating from the charge trapping into

interface defects caused by PBTS, as illustrated in Fig. 6-11(b). NBTS, in contrast, removed the mobile ions from the SiO_2 underlayer and improved the interface properties as shown in Fig. 6-13 and 6-14.

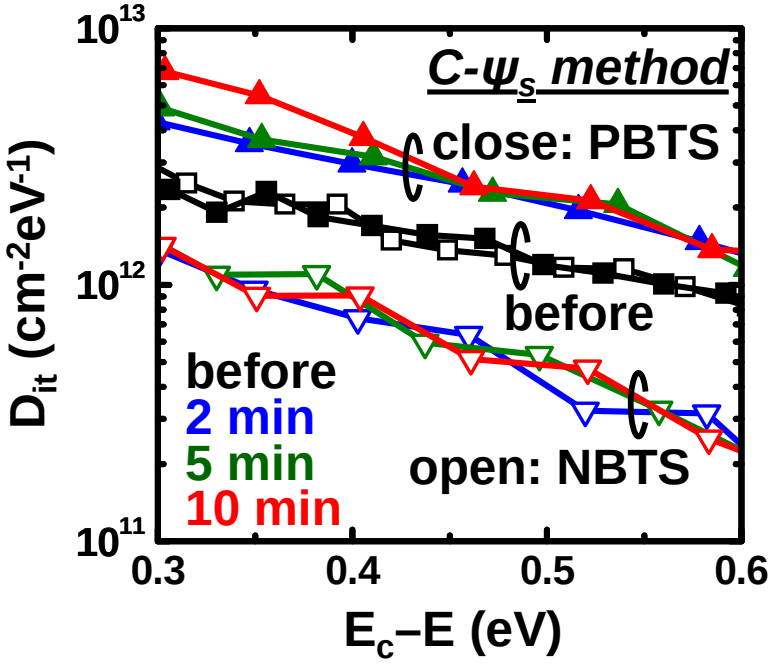

Fig. 6-13 Energy distribution of D_{it} after extended BTS experiments (see Fig. 6-9) for the SiC-MOS capacitors with AlON/20-nm-thick SiO_2. The D_{it} of PBTS-applied capacitors (close symbols) and NBTS-applied capacitors (open symbols) were estimagted by using C−ψ_s method [17,18] before (black) and after BTS for 2 min (blue), 5 min (green), and 10 min (red).

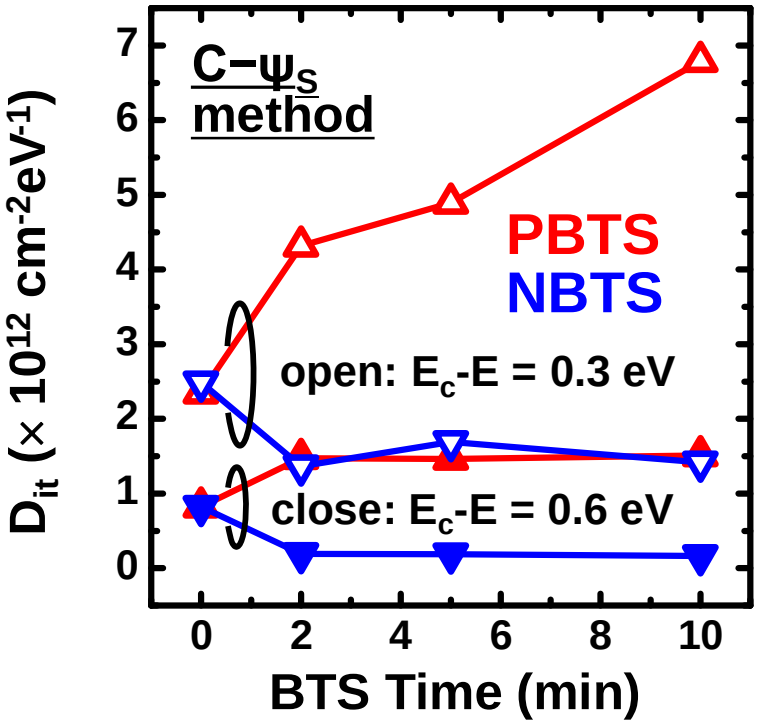

Fig. 6-14 BTS time dependence of D_{it} value for SiC-MOS capacitors with AlON/SiO_2 (20 nm) stacked gate dielectrics summarized from Fig. 6-13. Typical D_{it} values at the energy position $E_C - E$ = 0.3 (open symbols) and 0.6 eV (closed symbols) are plotted as a function of BTS time.

6-4 Summary

In summary, we investigated several gate insulators that could possibly replace conventional thermal oxides and greatly improve the BTI characteristics of SiC-MOS devices. Our systematic experiments revealed that although deposited SiO_2 insulators do not obviously improve the BTI characteristics of SiC-MOS devices, stacked gate dielectrics consisting of a high-*k* AlON film blocking the diffusion of mobile ions and a thermal SiO_2 underlayer around 8 nm thick significantly improves the long-term reliability of SiC-MOS devices.

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Chapter 7 General Conclusions

The primary purpose of this doctoral dissertation is to provide the different aspects for better understanding of bias-temperature instability (BTI) in SiC-based metal-oxide-semiconductor (MOS) devices. Later, the method to efficiently control BTI was demonstrated based on pioneering mobile ion elimination techniques proposed to improve performance and electrical stability. Lastly, high-permittivity gate dielectrics used for the advanced SiC-MOS devices were also examined. The main achievements of this study are summarized below:

In Chapter 2, the fundamental aspects of SiC oxidation were systematically described in order to clarify the physical origin of the electrical degradation of the SiO_2/SiC interface. Synchrotron radiation x-ray photoelectron spectroscopy (SR-XPS) analysis revealed a near-perfect interface dominated by Si-O bonds, and it was found that atomic scale roughness and imperfection is introduced as oxide thickness increases. These results show that a thick transition layer is ruled out as a cause of electrical degradation and that the elimination of atomistic defects just at the interface and beneath the SiC substrate must be focused on in order to obtain a guideline for future SiC-based devices. This high-resolution XPS study also examines the modulation of energy band alignment between thermally grown SiO_2 layer and 4H-SiC due to post oxidation treatments. Although the hydrogen incorporation into the SiO_2/SiC interface is effective in improving the interface property, the SR-XPS analysis showed that interface defect passivation induces a reduction of the conduction band offset.

In Chapter 3, studies on BTIs in 4H-SiC MOS capacitors revealed the unusual generation of positive mobile ions in thermal oxides that could be considered as an intrinsic phenomenon in 4H-SiC MOS devices with thermally grown oxides. Charge injection into the electrical traps at/near SiO_2/SiC interfaces causes BTI typically characterized by a clockwise hysteresis in bidirectional capacitance-voltage (C-V) curves of SiC-MOS capacitors. Forming gas annealing (FGA), POA in diluted H_2 ambient is beneficial in reducing the clockwise C-V hysteresis due to electron injection at room temperature. However, the hysteresis was changed to counter-clockwise at 200°C only for the SiC-MOS capacitors with FGA, indicating the positively charged mobile ion drift. The magnitudes of C-V hysteresis due to mobile ion drift at high-temperature were found to depend on FGA temperatures. The results were also compared with Si-MOS capacitors, but this C-V hysteresis due to mobile ions was not observed in any fabricated Si-MOS capacitor. Thus, common ion contaminations (*i.e.* Na^+, K^+) are ruled out to indicate an intrinsic problem of SiC.

In Chapter 4, in order to obtain mobile ion-free SiC-MOS capacitors, the mobile ion removal was proposed based on the negative bias-temperature stress (NBTS). Constant negative gate voltage (V_G) was applied at typical high-temperature to move all mobile ions to accumulate at the uppermost SiO_2 surface and then perform subsequent etching of a few nm-thick SiO_2 to eliminate the mobile ions. In this time, bidirectional C-V curves of the NBTS sample measured at both room and high temperatures overlap each other without hysteresis. It can be concluded that mobile ions were removed completely while maintaining the excellent interface property attributed to FGA. In addition to NBTS sample, the positive bias-temperature stress (PBTS) with negative V_G was also applied at the same temperatures to accumulate mobile ions at the bottom SiO_2/SiC interface with an areal density of several 10^{12} cm^{-2}.

In Chapter 5, the significant electrical degradation of SiC-MOS capacitors with mobile ions at the interface indicates that these ion species intensely degrade the quality of the SiO_2/SiC interface. A stretch-out of 1 MHz C-V curves was seen in the gate voltage ranging from flatband to accumulation for both samples. The stretch-out of C-V curves is considered to be due to the electron trapping into interface states near the conduction band edge which do not respond to 1 MHz. Furthermore, the marked difference between 1 MHz and ideal C-V curves for the PBTS sample means that mobile ions at the SiO_2/SiC interface may induce additional interface states. Next, the densities of slow interface state (D_{it}) were evaluated by Terman, conductance and C-ψ_s methods. Significant increases in D_{it} at both near the conduction band edge and below the Fermi level were observed for PBTS sample while NBTS sample did not show significant change in D_{it}. These experimental findings show that the interface quality of FGA-treated SiC-MOS structures gets further improvement by removing mobile ions from the SiO_2/SiC interfaces. Furthermore, a slight increase in the conduction band offset was observed for the samples containing mobile ions at SiO_2/SiC interfaces.

In Chapter 6, diffusivity of mobile ions in SiC-MOS devices was examined with deposited gate dielectrics. This study shows that the mobile ions can penetrate from thin thermally grown SiO_2 underlayer into deposited SiO_2 layer which is similar to that for single FGA-treated 40 nm-thick thermal SiO_2/SiC structures reported in the previous chapters. Nevertheless, significant improvement of BTI characteristics by high-*k* aluminum oxynitride (AlON) dielectrics deposited on thin thermal oxides was demonstrated. The C-V characteristics of AlON samples did not change much by bias stressing due to reduced gate leakage current. AlON/SiO_2 stacked dielectrics were found to be beneficial not only for reducing the leakage current but also for suppressing diffusion of mobile ions, leading to stable SiC-MOS characteristics even under strong

electric fields and high temperatures. Finally, diffusivity of the mobile ions inherent to AlON/SiO_2 structures was also investigated by conducting extended BTS experiments.

This doctoral study will further contribute to the power electronics research communities and industries in Japan and overseas for better understanding of fundamental physics in SiC-MOS (FETs). Furthermore, this study will recommend the “next stage” of innovation in modern SiC power MOS devices. The engineering of gate stacks and the designing of device architectures for SiC-MOSFETs are indispensable for realizing high-reliability and high-mobility operation. Besides, this study may present the precaution for manufacturer to perfectly fabricate SiC-MOSFETs with more concerns in reliability.

Acknowledgements

First of all, I would like to express my deepest appreciation to my supervisor, Prof. Dr. Heiji Watanabe, for his surpassing guidance, great encouragement, and kind hospitality during my study in Japan. I would like to deliver my gratefulness to Prof. Dr. Yoshizo Takai and Prof. Dr. Yasuo Kanematsu for the worthy comments and valuable guidance. I would like to phrase greatly attitudinal thankfulness to Assoc. Prof. Dr. Takayoshi Shimura and Assist. Prof. Dr. Takuji Hosoi for their extensive instructions and constructive suggestions for both educational and life experiences. I am very obliged to acknowledge all lecturers from Department of Material and Life Science, and Department of Biotechnology, Graduate School of Engineering for delivering worthy knowledge and experience during my studies. I would like to acknowledge to Dr. Takashi Nakamura, Mr. Yuki Nakano, and Mr. Shuhei Mitani from Power Electronics R&D Unit, ROHM Co., Ltd. for fruitful suggestions. The synchrotron radiation x-ray photoelectron spectroscopy (SR-XPS) (Chapters 2 and 5) were supported by Nanotechnology Platform Project (Proposal Nos. 2011B3872, 2013A3872, and 2014A3872) of the Ministry of Education, Culture, Sports, Science and Technology (MEXT), Japan, and were performed at the BL23SU of SPring-8 with the approval of Japan Atomic Energy Agency (JAEA) and the Japan Synchrotron Radiation Research Institute (JASRI). I would like to thank Prof. Dr. Yuden Teraoka and Dr. Akitaka Yoshigoe for their support in an experiment at BL23SU in SPring-8.

Secondly, I would like to express my sincere appreciation to Dr. Katsuhiro Kutsuki, Dr. Hiroaki Arimura and Dr. Tatsuya Hashimoto for valuable direction as a Ph.D. candidate, and all staffs and students at Watanabe laboratory for their tremendous contribution and warmly support my daily life while studying in Japan. I would like to note my deepest appreciation to International Program of Frontier Biotechnology, Osaka University, for allowing me to carry out the master and doctoral degree.

Lastly but not least, I would once again deeply appreciate MEXT, Japan for supporting a complete scholarship to study in the master and doctoral program at Osaka University. I would like to express my special appreciate my family for their consistent encouragement, support and understanding during my study. I would embrace my special grateful messages to Ms. Suwatana Daengsubha, my beloved friend for always encouraging. I would thank to my friends from Thailand for being together as a real family. I would like foremost to thank God for giving me strength and wisdom.

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Publication list

Original research reports: Journal papers (first author)

1. A. Chanthaphan, T. Hosoi, Y. Nakano, T. Nakamura, T. Shimura, and H. Watanabe, *Improved bias-temperature instability characteristics in SiC metal-oxide-semiconductor devices with aluminum oxynitride dielectrics*, Applied Physics Letters, Vol. 104, No.12, pp.122105, March, 2014.

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Award

"Best Presentation Award"
The International Workshop on Atomically Controlled Fabrication Technology, Osaka University, February 5-6, 2014.