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# A 1-V 120-MHz FD-SOI CMOS linear-in-dB variable gain amplifier

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**Abstract:** An intermediate frequency (IF) linear-in-dB variable gain amplifier (VGA) for a radio receiver is fabricated in 0.15-$\mu$m fully-depleted (FD) SOI CMOS technology. The complete VGA consists of two stages of the modified linearized transconductance VGA, three stages of fixed gain amplifier (FGA) and a buffer. It provides a continuous −13.6 dB to 55.8 dB gain control range, an IIP3 of −13.55 dBm and an NF of 13.3 dB at 100 MHz. The proposed VGA using FD SOI CMOS process has great advantages in power consumption and frequency response compared to the bulk CMOS VGA.

**Keywords:** variable gain amplifier, VGA, linear-in-dB, FD SOI, CMOS

**Classification:** Integrated circuits

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## 1 Introduction

Intermediate frequency (IF) variable gain amplifier (VGA) which adjusts signal level for desired output is an indispensable component in wireless communication systems. Recently, silicon-on-insulator (SOI) CMOS circuits have been developed for these applications, featuring such as high transconduc-



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tance, low body-effect and small parasitic capacitance [1, 2, 3].

The linearized transconductance VGA realizing exponential function of $\exp(2x)$ has wide gain range and moderate gain variation with control voltage [4].

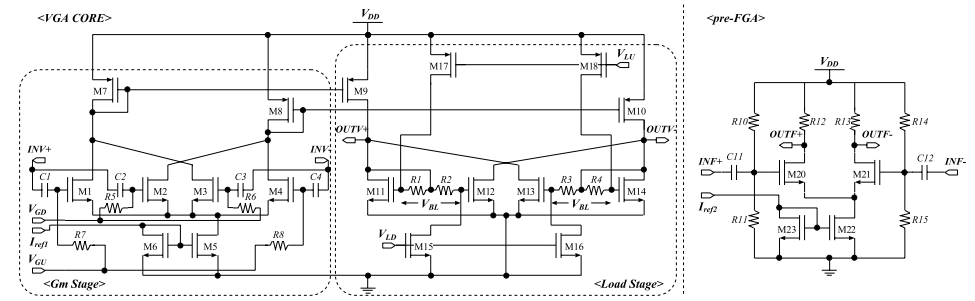
In this study, the linear-in-dB VGA using FD SOI CMOS process is described and compared with that using bulk CMOS process [5].

## 2 Circuit Configuration

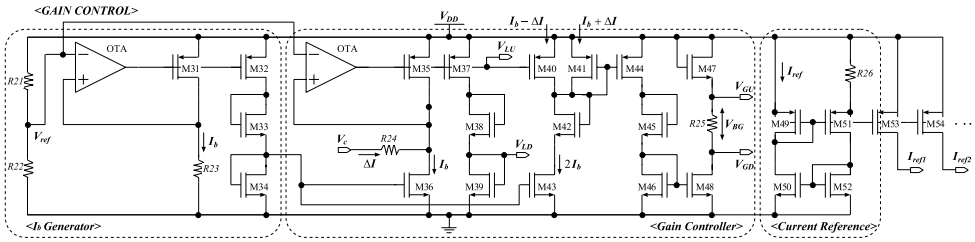
Figure 1 (a) shows the fully-differential modified linearized transconductance VGA [5] composed of $G_m$ and load stages. Gain of the VGA is given by the ratio of the transconductance of $G_m$ stage to that of load stage. Each transconductance varies linearly with DC offset voltage, $V_{BG}$ or $V_{BL}$. Bias voltages, $V_{GD}$ and $V_{GU}$ generated at the gain controller, shown in Fig 1 (b), provide the DC level of capacitively coupled input of VGA. The offset voltage source, $V_{BG}(= V_{GU} - V_{GD})$, is shared in the $G_m$ stage by using $R_5 \sim R_8$ of large resistance, while $V_{BL}$ is generated in the load stage. The offset voltages are given by

$$\begin{aligned} V_{BG} &= V_{GU} - V_{GD} = \alpha_1 R_{25}(I_b + \Delta I), \\ V_{BL} &= \alpha_2 (R_1 + R_2)(I_b - \Delta I), \end{aligned} \tag{1}$$

where $I_b$ is drain current of M36, $\Delta I$ current through $R_{24}$, $V_c$ external control voltage, and $\alpha_1$, $\alpha_2$ are constants given by the size ratio of transistors in the




(a)




(b)

**Fig. 1.** Schematics of (a) the VGA and the pre-FGA circuits and (b) the gain control circuit.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gain controller. The gain of the VGA, $G_{VGA}$, is expressed by

$$G_{VGA} = -\beta_1 \frac{V_{BG}}{V_{BL}} = -\beta_2 \frac{1+x}{1-x}, \tag{2}$$

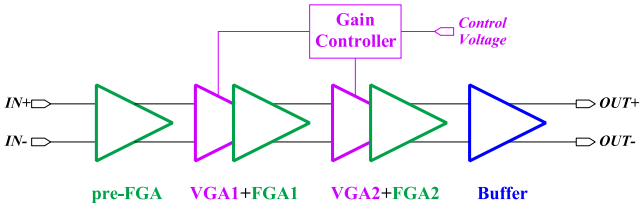
where $\beta_1$, $\beta_2$ are constants given by the size ratio of transistors in the circuits and $x = \Delta I / I_b < 1$. The VGA gain control behavior of Eq. (2) emulates exponential function of $\exp(2x)$.

For the applications of wireless communication, two VGA's have been cascaded to increase gain control range. In order to avoid the bandwidth limitation due to the cascade connection, we adopted the technique of bandwidth improvement [5] by changing output node connection from gate node of diode-connected M11(M14) to center node between two equal resistors, $R_1$ and $R_2$ ($R_3$ and $R_4$). Pole frequency, $p$, of the VGA using center-tapped load are given by

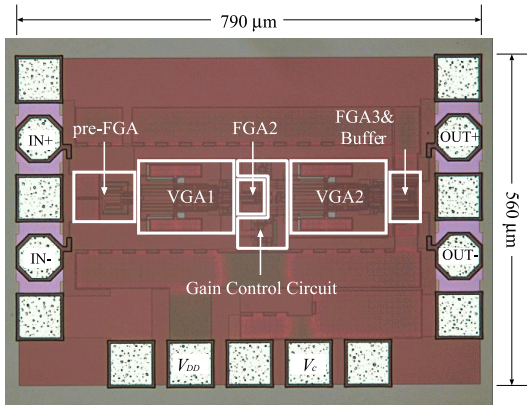
$$p = \frac{2C_A + C_{out} \pm \sqrt{(2C_A + C_{out})^2 - 4R_A C_A C_{out}\,(g_{m1} - g_{m2})}}{2R_A C_A C_{out}}, \tag{3}$$

where $C_A$ is capacitance at the gate node of M11 $\sim$ M14, $R_A$ is resistance of $R_1 \sim R_4$, and $g_{m1}$ and $g_{m2}$ are transconductances of M11 and M12, respectively. The use of SOI device with small parasitic capacitance reduces $C_A$ and $C_{out}$, leading to high pole frequency. This implies that the VGA on SOI CMOS is superior to the one on bulk CMOS in frequency characteristics.

The block diagram of the complete VGA composed of a pre-FGA (fixed gain amplifier), two VGA-FGA pairs and a buffer is shown in Fig. 2 (a). The




(a)




(b)

**Fig. 2.** (a) Block diagram and (b) photomicrograph of the fabricated VGA.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FGA used is a differential common source amplifier with resistive load to boost absolute gain of the VGA. Noise and linearity characteristics of the complete VGA have been improved by taking into account of the arrangement of the FGA's. Source follower is used as a buffer to drive a large load capacitor.

The $I_b$ generator and the beta multiplier current reference have been added to gain control circuit, as shown in Fig 1 (b), to reduce the temperature dependence of the gain of FGA as well as VGA [5]. The gain variation simulated with HSpice at $-35$°C, 27°C, and 85°C shows only $\pm 3$ dB in the whole gain range.

In order to avoid poor current mirror characteristics due to the self-heating effect [2] which reduces drain current of MOSFET on SOI process, we placed a diode-connected MOSFET which copies $I_{ref}$ from the current reference circuit, close to a mirroring MOSFET in each stage.

## 3 Circuit Implementation and Measured Results

The circuit has been implemented in 0.15-$\mu$m FD-SOI CMOS technology with poly and well resistors, and MIM capacitors.

The complete VGA shown in Fig. 2 (b) has an active area of about 0.11 mm$^2$ and consumes 7.4 mA to 8.15 mA at 1 V supply. It has a 3 dB frequency of 120 MHz at maximum gain which is the worst case of frequency characteristics. Dissipation current and bandwidth of the fabricated VGA were improved by a factor of three compared with the bulk CMOS one in the previous work [5] due to the superiority of the SOI device to the bulk counterpart in terms of small parasitic capacitance.

Figure 3 (a) shows the gain and noise figure (NF) measured as a function of the control voltage $V_c$ at a signal frequency of 100 MHz. The complete VGA has continuous linear-in-dB characteristics where its gain varies from $-13.6$ dB to 55.8 dB. NF of 13.3 dB was obtained at 55.8 dB gain.

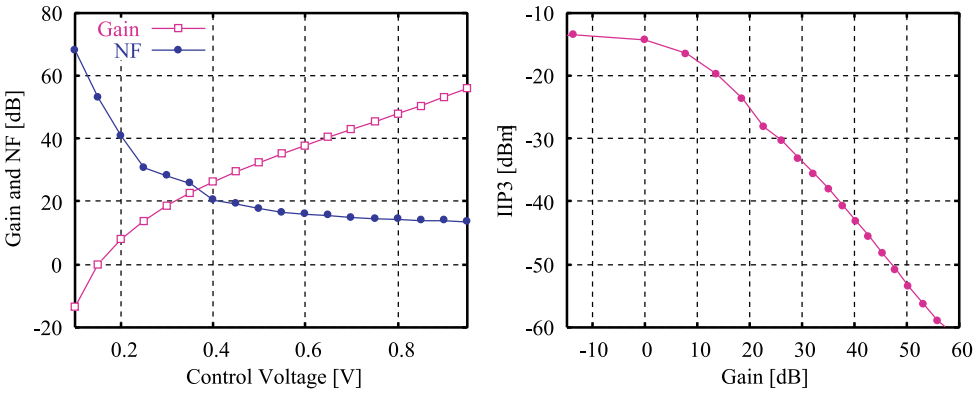


**Fig. 3.** (a) Gain and NF vs. control voltage and (b) IIP3 characteristics over the whole gain control range at 100 MHz signal frequency.


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**Table I.** Comparison of the complete VGA characteristics.

| Process | 0.15-$\mu$m FD SOI | 0.25-$\mu$m bulk [5] |
|---|---|---|
| Bandwidth (3 dB) | 8 $\sim$ 120 MHz | 4 $\sim$ 40 MHz |
| Gain Range | 69.4 ($-13.6 \sim 55.8$) dB | 66.5 (10 $\sim$ 76.5) dB |
| NF @ Gmax | 13.3 dB | 15 dB |
| IIP3 @ Gmax | $-59$ dBm | $-53$ dBm |
| IIP3 @ Gmin | $-13.55$ dBm | $-11.5$ dBm |
| Supply Voltage/Current | 1 V / 7.4 $\sim$ 8.15 mA | 3.3 V / 21 $\sim$ 22 mA |
| Active Chip Area | about 0.11 mm$^2$ | $<$ 0.4 mm$^2$ |

To investigate linearity of the complete VGA, two-tone test at 100 MHz with a 1 MHz spacing has been carried out. In Fig 3 (b), IIP3 characteristics over the whole gain range shows $-13.55$ dBm at minimum gain and $-59$ dBm at maximum gain.

Characteristics of the complete VGA using SOI CMOS and bulk CMOS process are summarized in Table I.

## 4 Conclusion

An IF linear-in-dB VGA has been composed of a pre-FGA, two modified linearized transconductance VGA-FGA pairs and a buffer, fabricated in 0.15-$\mu$m FD-SOI CMOS technology. The complete VGA showed comparable properties in gain range, IIP3, and NF to those of the bulk CMOS one in the previous work. Moreover, characteristics of the SOI CMOS VGA have been improved in terms of dissipation current and bandwidth by a factor of three compared with those fabricated in the bulk CMOS. The measured results demonstrate that the proposed VGA featuring small size and low power is suitable for SOI CMOS radio receiver.

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