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PAPER

A New Analog Correlator Circuit for DS-CDMA Wireless Applications

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SUMMARY A new analog correlator circuit is proposed for direct sequence code division multiple access (DS-CDMA) demodulator. The circuit consists of only 16 switches, 4 capacitors and 2 level shifters. Control sequence requires only three clock phases. Simulation with code length of 127 reveals that the proposed circuit has a good ability to cancel off the charge error and dissipates 3.4 mW at 128 MHz. The circuit had been designed using a 0.6 μm CMOS process. The area of 256 μm $\times$ 245 μm is estimated to be 9 times smaller compared to other reported equivalent analog correlators.

key words: *code division multiple access, analog correlator, demodulation process, switched-capacitor circuits, spread spectrum*

1. Introduction

Direct Sequence Code Division Multiple Access (DS-CDMA) has been studied as a major system for future generation mobile phones because of its high capacity and robustness against interference and noise [1], [2]. In DS-CDMA, all users share the same carrier frequency, but are assigned unique Pseudo Noise (PN) codes for spreading. The desired user's signal is separated from those of other users after performing despreading process using the same PN code as a transmitter sending the desired signal [3]. Using digital domain in recovering the information requires high-speed analog-to-digital converter (ADC) to digitize the received signal [4], [5]. This leads to high dissipation power at high-speed applications. An alternative approach would be to avoid the power consumption of a high-speed ADC and to perform the despreading in the analog domain [6]–[8]. Then, if needed a slower ADC can follow the analog correlator leading to a low power solution since the recovered signal has a lower bandwidth. A CMOS switched capacitor analog correlator has been demonstrated in [6], which describes DS-CDMA correlators operating at 128 MHz dissipates 4 mW using code length of 64 and requires more than 64 non-overlapping clocks to drive the switches. This is achieved only at the expense of chip area because a large number of capacitors and switches are used.

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This paper seeks to extend the performance of these approaches considering different circuit topology but with a small number of devices. The proposed circuit in this paper operates at 128 MHz while dissipating 3.4 mW using code length (N) of 127, but consists of only 4 capacitors, 16 switches and 2 level-shifters. The level shifter is introduced to provide good linearity. Digitizing the output of the proposed analog correlator requires sampling rate of only 1 Ms/s with a 7-bit of ADC compared to the sampling rate of 128 Ms/s with a 10-bit ADC for digital domain correlator. The remainder of the paper is organized into five sections. Section 2 gives an overview of DS-CDMA and describes how correlation is used in despreading process. Section 3 introduces the proposed circuit principle of operation. In Sect. 4 design considerations for the proposed circuit are discussed. Section 5 shows physical layout and simulation results of the proposed circuit. In Sect. 6 we summarize the main results.

2. DS-CDMA System Overview

Figure 1 depicts a simplified wireless DS-CDMA system. In the transmitter the serial data bit stream is spreaded by a PN sequence code. Because of the random nature and high frequency content of the PN code, the spectrum of spreaded data is relatively flat and much wider in bandwidth. In the receiver, despreading is accomplished by performing a correlation between the received signal and the PN code, i.e., multiplying the received signal by the PN code followed by integration. Figure 2 shows a more detailed despreading process, which is accomplished by performing a discrete-time correlation of the baseband-received

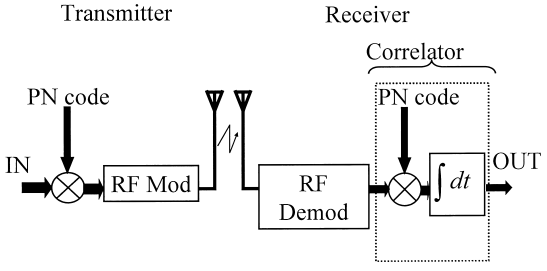

Fig. 1 Simplified wireless DS-CDMA system.

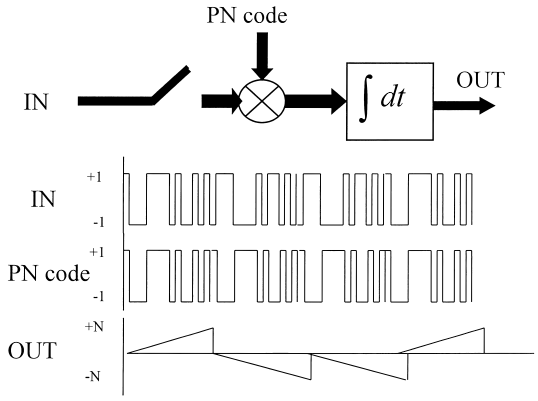

Fig. 2 DS-CDMA demodulation process using discrete time correlation.

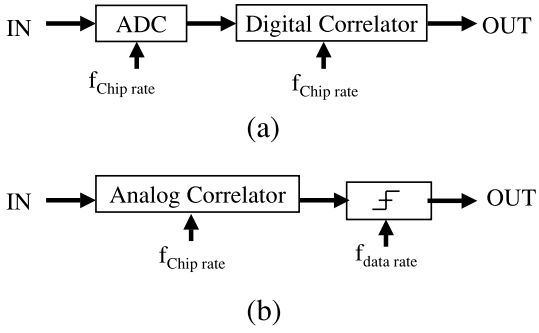

Fig. 3 (a) Digital and (b) analog correlator block diagram.

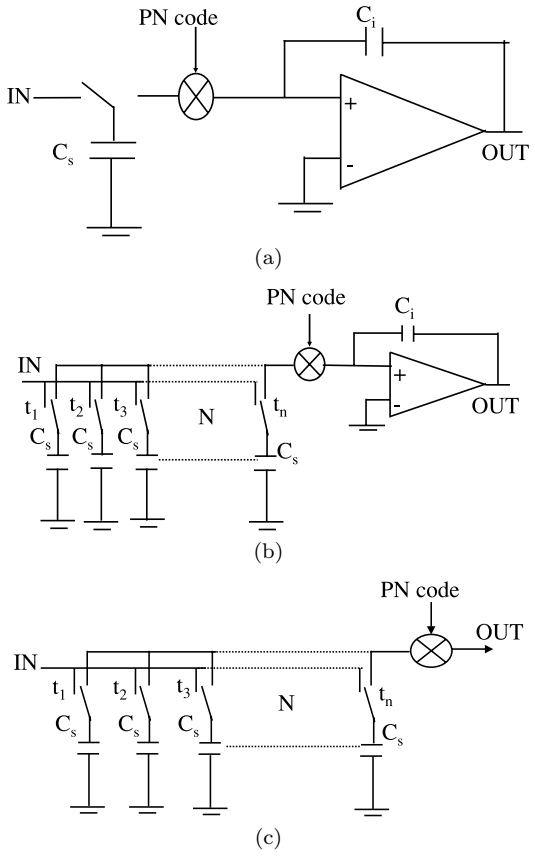

Fig. 4 (a) Active chip rate correlation, (b) active data rate correlation and (c) passive data rate correlation.

signal with the PN code using discrete-time correlation. This discrete-time correlation (C_{DT}) is defined as shown in Eq. (1)

$$C_{DT} = \sum_{i=1}^{N} S_R(i).PN(i) \tag{1}$$

where S_R(i) is the chip-rate sampled value of the received input signal, PN(i) is the N-length PN code. If the input sampled values and PN codes are normalized to 1, the output of the correlator equals +N when the two signals are in-phase and −N when they are out-of-phase. Thus, the original data bits are contained in the sign of the correlator output but not in the magnitude, permitting data recovery by employing a simple slicer.

There are two types of correlators which are used in demodulation process as shown in Fig. 3, digital correlator and analog correlator. The digital correlator consumes more power because high speed analog-to-digital converter (ADC) is needed to digitize the received signal waveform to perform despreading process operating at a high clock rate (chip rate). By using analog architecture, power consumption required for a front-end ADC sampling at the chip rate can be significantly reduced. The resolution of ADC required after analog correlator also decreases comparing to the digital counterpart one.

The first step in performing the analog correlation is multiplying the input sample with the PN code. The PN code values are ±1, so PN code multiplication is simply sign modulation of the input samples prior to integration/summation. Three possible approaches for implementing an analog correlator as shown in Fig. 4 have been reported in [6]. Figure 4(a) shows an active chip rate correlator circuit, which operates at chip rate to take a sample and integrate it. This architecture has disadvantages. Its opamp settling time must be very fast and hence opamp static power will be large. Although Fig. 4(b), which shows an active data rate correlator, modified the opamp settling time and static power dissipation by a factor of N (code length), this achieved at the expense of chip area. Figure 4(c) shows a passive data rate correlator. This architecture cancels all static power but still requires large chip area because large number of sampling capacitors and switches are used. Implementation of fully differential passive data rate correlator requires 9N switches, and 2N sampling capacitors. It was reported that the circuit operating at 128 MHz dissipates 4 mW by the use of Walsh code of length 64 together with more than 64 non-overlapping clocks to sequence the switches.

3. Circuit Principle of Operation

We proposed a new architecture to implement analog correlator, which only consists of four capacitors, (two sampling capacitors C_C, two load capacitors C_L), two level shifters V_{sh}, and sixteen switches which are implemented by transmission gates as shown in Fig. 5. The specifications of the proposed circuit are shown in Table 1.

For simplicity and clarity, a single-ended representation is used as shown in Fig. 6(a). The level shifter is introduced to decouple the output node from the correlator circuit. Theoretically, the level shifter is ideal, i.e. its gain equals unity. During the sampling phase (ϕ_1 and $\bar{\phi_3}$), electric charge is stored at the sampling capacitor, C_C as shown in Fig. 6(b). At the integrating phase (ϕ_4 and $\bar{\phi_3}$), the storage charge is then injected into the load capacitance C_L as shown in Fig. 6(c). The charge stored during sampling phase, $Q_{sampling}$ and the charge remained at the C_C during integrating phase, Q_{remain} are given by Eqs. (2) and (3) respectively.

$$Q_{sampling} = C_C\{V_{IN+} - (V_{IN-} + V_{sh})\} \tag{2}$$

$$Q_{remain} = C_C\{V_{OUT} - (V_{OUT} + V_{sh})\} \tag{3}$$

The amount of electric charge injected to the load capacitance is the difference of $Q_{sampling}$ and Q_{remain} as shown in Eq. (5).

$$Q_{CL} = Q_{sampling} - Q_{remain} \tag{4}$$

$$= C_C(V_{IN+} - V_{IN-}) \tag{5}$$

Due to the level shifter, the amount of charge is independent of the output voltage V_{OUT}. Because the level shifter shown in Fig. 7, has low output resistance, the switch $\bar{\phi_3}$ is added to protect the signal charge during zero charge cancellation phase as described in Sect. 4. Signal voltage swing ΔV for one charging cycle resulted from the charge injecting is given by

$$\Delta V = \frac{C_C(V_{IN+} - V_{IN-})}{C_L} \tag{6}$$

Discharging the same amount of charge from C_L is simple by just interchanging V_{IN+} and V_{IN-} (ϕ_2), i.e. injecting the same amount of negative charge into C_L. At the end of each cycle, the output nodes of the correlator (V_{OUT+} and V_{OUT-}) will be shorted (ϕ_{RST}) to

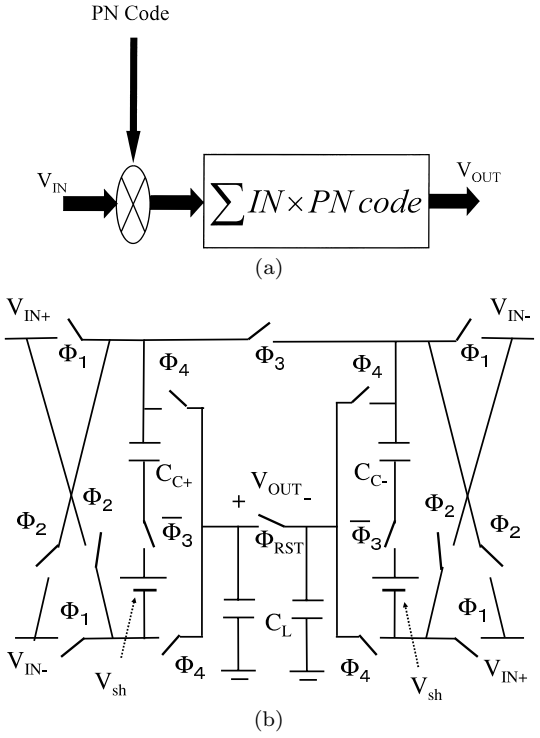

Fig. 5 Proposed analog correlator circuit.

Table 1 Analog correlator circuit specifications.

Power supply	5 V
Resolution	10 bits
PN code length	127
Maximum clock frequency	128 MHz
Output signal format	Analog
Power dissipation	3.4 mW
Process	CMOS 0.6 μm
Chip size	256 μm × 245 μm

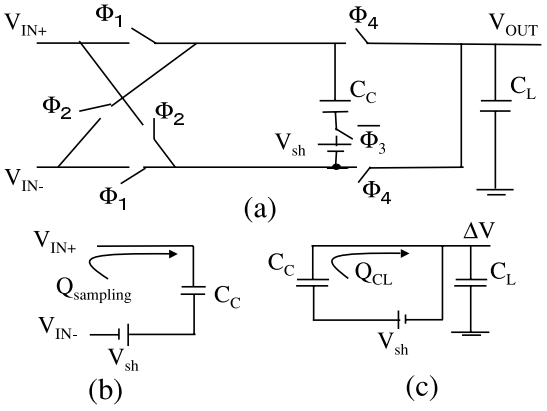

Fig. 6 (a) Single-ended analog correlator, (b) sampling phase and (c) integrating phase.

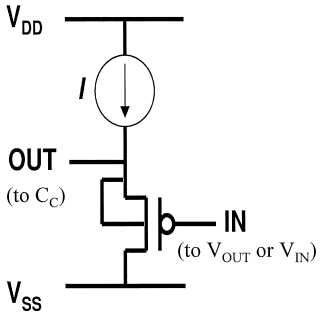

Fig. 7 Level shifter circuit.

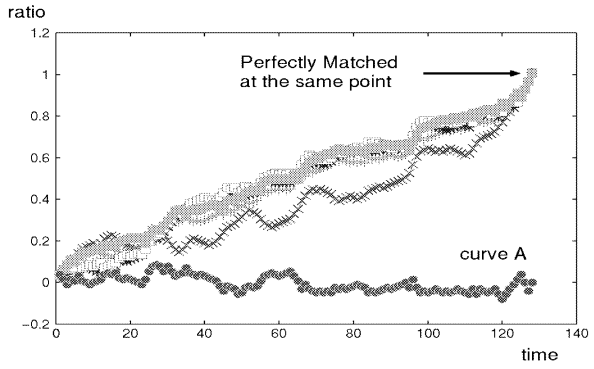

Fig. 8 Behavior of ideal correlator circuit without mismatch or parasitic capacitance. Correlated signals are summed up while non-correlated signal is rejected (curve A).

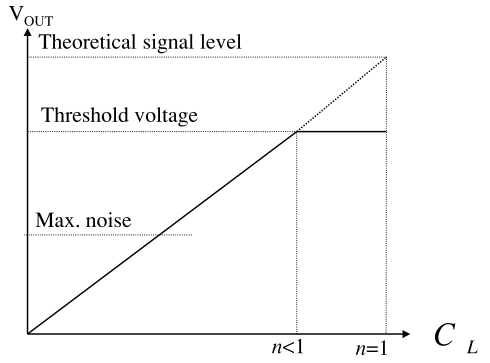

Fig. 9 An example of choosing the load capacitance value.

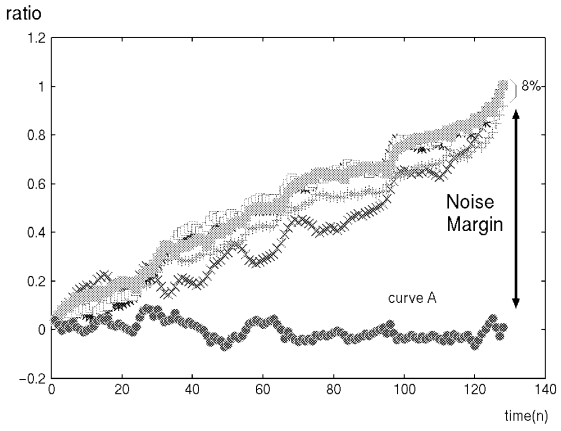

Fig. 10 Behavior of ideal correlator circuit considering the effect of channel length modulation. Noise margin remains high.

distribute electric charges and set the output nodes of the correlator back to reference point.

In addition, the proposed circuit requires only three non-overlapping clocks, which reduces the complexity of the control sequence. Eventually, this leads to less switching and low power consumption. When the PN code matched the input signal, every signal transmitted would be summed up as shown in Fig. 8, where all curves terminate at the same point except curve A. If the codes do not match, the correlator circuit gives no output because all the signals would cancel off each other as shown by curve A.

The size of charging capacitor, C_C should be related to load capacitor C_L as

$$C_L = C_C \times \frac{n \times N}{\lambda} \tag{7}$$

where n is multiplication factor between 0.7 and 1, and λ is the ratio of output voltage range to input voltage range. Although theoretically n should be one, a smaller number of n would make the output node, V_{out} saturates before the final output is obtained at the end of the clock cycles (N-th sampling for PN codes). Theoretical threshold voltage (n=1) is not required and can be chosen smaller ($n < 1$) to reduce power consumption as shown in Fig. 9. The minimum value of n is limited by the maximum of the interference level due to other channels. We have calculated the interference due to 10 channels using the same taps for $N = 127$. The value of this interference which is only 7% is acceptable for using n=0.7 to realize the correlator circuit.

In practical case, due to the level shifter channel length modulation (the level shifter's gain < 1). Equation (6) can be rewritten as follows

$$\Delta V = \frac{C_C(V_{IN+} - V_{IN-})}{C_L} + \frac{C_C(G-1)(V_{OUT} - V_{IN-})}{C_L} \tag{8}$$

where G is the level shifter's gain. Taking the channel length modulation effect into consideration using transistor size of $W/L = 16.5\,\mu$m$/0.9\,\mu$m in $0.6\,\mu$m CMOS technology, the output deviated but at a range of less than 8% although every signals swing varied at maximum 10% as shown in Fig. 10.

4. Design Considerations

Theoretically, the proposed circuit is able to charge and discharge precise amount of electronic charge. However, in reality, the circuit is not completely balanced due to charge injection of the switches, clock feedthrough, parasitic capacitance and mismatch. We will discuss these effects on the proposed analog correlator circuit.

4.1 Charge Error

Figure 11(a) shows simulation results of the proposed circuit with initial output of 2.5 V for 127 cycle of charging and discharging in alternative period. Although theoretically net charge injection is zero, the output node voltage of the circuit gradually changes. We can conclude from the simulation results that the amount of charge injection depends on the load capacitance voltage. The behavior of the load can be explained by

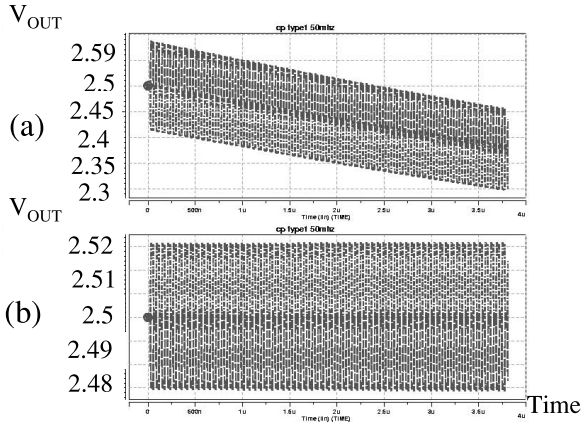

Fig. 11 Simulation with V_{in} =4 mV, λ=2, n=0.7 initial output at 2.5 V and C_L=44C_C for 127 cycles (a) without cancellation technique and (b) with cancellation technique.

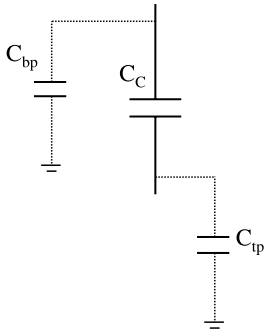

Fig. 12 Sampling capacitor with parasitic capacitance. Parasitic capacitors exist at both bottom and top plates.

taking into account the parasitic capacitance of the circuit. Actually, in a switched capacitor sampling circuit, charge errors can be caused by switch charge injection, clock feedthrough, and charge transfer on parasitic capacitance. The first two errors can be solved by using bottom-plate sampling and fully differential circuitry [9]. Figure 12 depicts the equivalent circuit when parasitic capacitance is taken into account. The value of parasitic capacitance varies depending on how the capacitor is implemented [10]. Top-plate parasitic capacitance (C_{tp}) due to interconnect at capacitor is usually small, i.e., at the order of 1/100 of C_C. The effect of (C_{tp}) is negligible small. Bottom-plate parasitic capacitance (C_{bp}) is usually larger than top-plate capacitance. The charge error gets stored on the parasitic capacitances (C_P) (bottom-plate parasitic capacitance of C_C, junction capacitances of the switching circuit, and the wiring capacitances of the metal lines).

In order to cancel off the charge transfer due to the parasitic capacitance, charge cancellation technique as shown in Fig. 13(a) is applied. The sequence of canceling the effect of parasitic capacitance is shown in Fig. 13(b).

Initially the sampling switches (ϕ_1 or ϕ_2) and $\bar{\phi_3}$

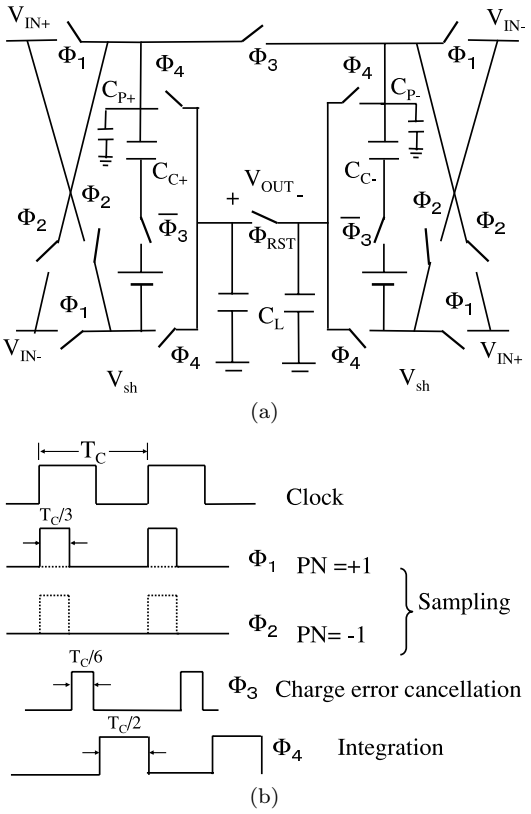

Fig. 13 (a) Fully differential correlator circuit and (b) switching sequence.

are closed for $T_C/3$ (T_C is chip period), connecting the sampling capacitance to the input [Fig. 14(a)]. Next, the charge pump capacitances are disconnected from the input by opening the (ϕ_1 or ϕ_2) and $\bar{\phi_3}$ switches. This creates charge error from the signal dependent charge injection from the (ϕ_1 or ϕ_2) switches onto C_P. To cancel off the charge error due to the bottom plate parasitic capacitance and the junction capacitance of switching circuit, the switch (ϕ_3) is momentarily closed for $T_C/6$ converting the differential charge on C_{P+} and C_{P-} to a common-mode charge effectively eliminating it [Fig. 14(b)]. Then the integration step can be done by closing switches (ϕ_4 and $\bar{\phi_3}$) for $T_C/2$ [Fig. 14(c)] (note that ϕ_4 has longer time period for integration step that is because C_L is greater than C_C). With the parasitic charge cancellation circuitry, the simulation reveals the results as shown in Fig. 11(b), indicating that parasitic capacitance effect is well taken care of.

The nonlinearity of the source and drain junction capacitances associated with the transistor switches, which are voltage dependence as follows,

$$C_P = \frac{C_{Po}}{\sqrt{1 + \frac{V_P}{\phi_o}}} \tag{9}$$

where C_{Po} is the depletion capacitance at V_P=0. These capacitance nonlinearity can introduce errors in the sampling process that generate an extra noise compo-

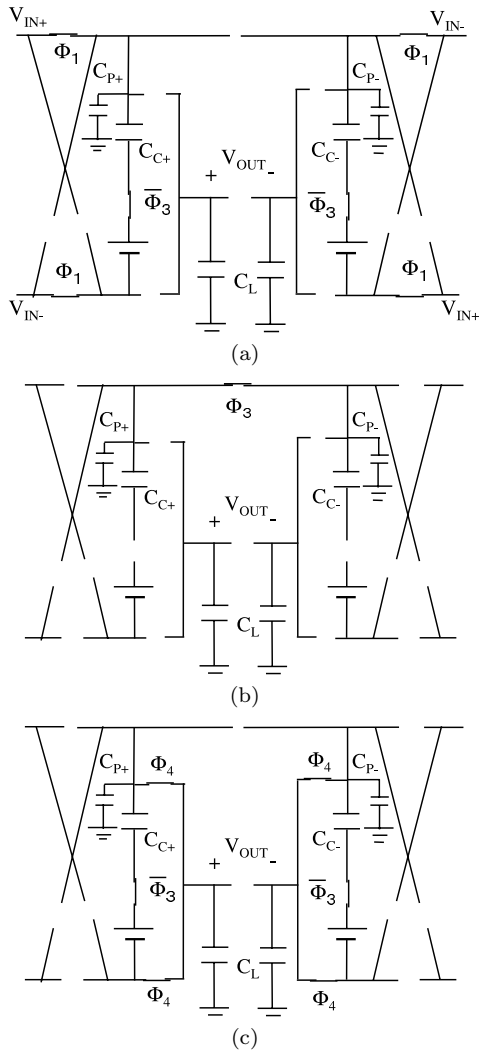

Fig. 14 The sequence of canceling the effect of parasitic capacitance, (a) sampling, (b) charge error cancellation and (c) integrating phases.

nent to the correlation process. To minimize this effect, the sampling capacitor can be increased and/or the switch sizes decreased. Doing either of these increases the settling time constant ($\tau = R_{ON} \times [C_C + C_L]$), where R_{ON} is the on-resistance of the integration switch, so there is a trade off between operating bandwidth and nonlinearity error. The switch sizes (W/L = 1.2 μm/0.6 μm) and sampling capacitors (C_C=140 fF) are used in 0.6 μm CMOS technology.

4.2 Capacitance Mismatch

As shown in Eq. (5), the charge injected into the load capacitance depends on C_C and V_{IN+}–V_{IN-}. Mismatch between C_{C+} and C_{C-} can be kept under 2% by applying layout technique such as using unit square capacitor [11]. Depending on its implementation, mismatch of (V_{IN+})–(V_{IN-}) may range from 0.2–5%. However, due to the noise rejection ability of the correlation circuit, the effect of mismatch is tolerable. This is verified through simulation result as shown in Fig. 15 in which the output of analog correlator fluctuates in less than 3% range. Due to its large noise margin, the effect due to capacitance mismatch can be easily eliminated.

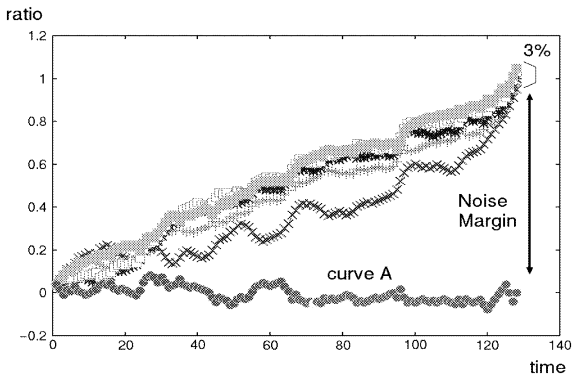

Fig. 15 Behavior of ideal correlator circuit considering the effect of capacitance mismatch. Noise margin remains large.

5. Physical Layout and Simulation

The proposed analog correlator circuit had been designed using a 0.6 μm triple-metal double polysilicon CMOS process. The designed circuit contains a clock generator for three phases (sampling, charge error cancellation, and integration). The physical layout of the correlator circuit is shown in Fig. 16. The layout size of 256 μm × 245 μm is sufficiently small. This layout has symmetry, considering wiring capacitance matching. The circuit dissipates 3.4 mW (this includes all clock power to sequence the switches and parasitic wiring capacitance) with code length of 127 at voltage supply of 5 V and operational clock frequency of 128 MHz. As the power is estimated from circuit simulations including parasitic capacitances based on the layout. The PN code used in this simulation is M-sequence with 127 code length. Figure 17 shows the simulation results of charging up the load capacitance for 127 cycles with parasitic wiring capacitance, sampling capacitor C_C=140 fF, load capacitor C_L=44C_C and input range of 4 mV. The output shows sign of saturation toward the threshold voltage because a smaller number of n (n=0.7) is used. Even though the input voltage amplitude is only 4 mV (the minimum input value which is limited by level shifer mismatch), which requires 10-bit resolution at the input, the output of the correlator becomes 35 mV, indicating that the resolution required after the analog correlator is 7 bit. In addition, the ADC after analog correlation is done with the data rate instead of chip rate. Figure 18 shows the linear behavior of the analog correlator, which is a plot of its transfer charactersitics. The maximum input range is limited by output saturation toward voltage supply of 5 V.

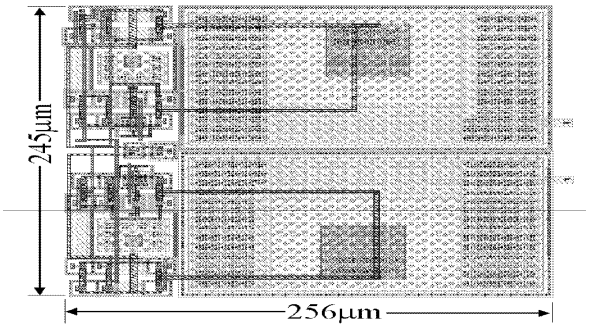

Fig. 16 Physical layout of analog correlator circuit.

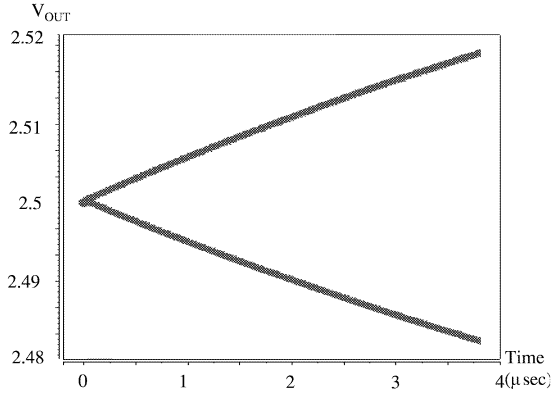

Fig. 17 Simulation results of charging up C_L with V_{in}=4 mV, λ=2, n=0.7 and C_L=44C_C for 127 cycle.

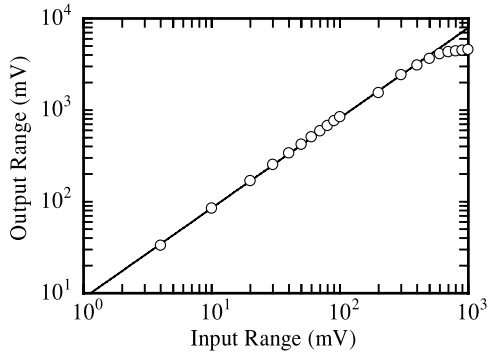

Fig. 18 Simulation results of analog correlator transfer characteristics with λ=2, n=0.7 and $C_L = 44C_C$.

6. Conclusion

An analog correlator circuit for DS-CDMA wireless communication had been proposed. The circuit consists of only sixteen switches, four capacitors and two level shifters. Control sequence for the proposed circuit is simple, as it requires only three clock phases. Simulation results verified that the charge error due to parasitic capacitance is canceled off and the integration phase can be processed in free of charge error. The proposed circuit dissipates 3.4 mW (including all clock power to sequence the switches) at 128 MHz. The output of analog correlator requires 7-bit ADC at the sampling rate of only 1 Ms/s to convert its output to digital format, which relaxes the design constraints of analog correlator circuit compared to 10-bit resolution with sampling rate of 128 Ms/s of digital correlator.

Acknowledgement

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