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Analytical design of a 0.5 V 5 GHz CMOS LC-VCO

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Abstract: A low-voltage complementary cross-coupled differential LC-VCO was investigated using simple modeling. The bias-controllability of the VCO provides a simple design for low-voltage operation. An analytical design approach realized a 5 GHz VCO under a 0.5 V supply voltage using a 90-nm digital CMOS process.

Keywords: CMOS, VCO, RF integrated circuits

Classification: Integrated circuits

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1 Introduction

The supply voltages of integrated circuits have been decreasing with the continuous scaling of CMOS technology. It has been predicted that the supply voltages of low-power digital circuits will decrease to 0.5 V in the near future, which imposes a challenge to the development of low-voltage and area-efficient RF circuits considering the integration of RF circuits with digital circuits [1]. Some VCOs that operate at 0.5 V use bonding wire inductances [2] or additional LC-tanks [3, 4], which results in deterioration of the area efficiency.

Complementary CMOS VCOs [5, 6] have been widely used, due to their low phase noise and low power performance. However, these VCOs are not presently suitable for ultra-low voltage operation (V_{DD}=0.5 V), because the common output voltage, which determines the bias voltages of the MOSFETs, is fixed at around $V_{DD}/2$ (0.25 V). In this letter, we introduce bias controllability to a complementary cross-coupled differential LC-VCO and use a simple model for design. The bias controllability of the VCO simplifies the design for low-voltage operation.

2 VCO core topology

As shown in Fig. 1 (a), the complementary cross-coupled differential LC structure is used to realize a fully integrated VCO under 0.5 V supply voltage. This structure is effective for the reduction of power required for the compensation of resonant tank loss, i.e., negative conductance. It has fully differential operation and provides complementary outputs. The resonant tank is composed of an on-chip differential symmetry spiral inductor [6], an inversion-mode PMOS varactor, and parasitic capacitances. To avoid weak inversion operation even under 0.5 V supply, the gate-source biases for MOS devices are boosted through coupling capacitances C_C and bias feeding resistors R_B, which also allow the independent control of the bias voltages for the NMOS and PMOS devices to achieve optimum transconductance for phase noise performance.

The VCO omits the conventional bias current source, which deteriorates the average resonator quality factor; however, this feature provides the following advantages [5, 6]: 1) the up-conversion of $1/f$ and thermal noise from the current source are avoided, and 2) the output swing is maximized.

It was assumed that the LC tank has a narrow passband, so that other frequency components are filtered out, except the fundamental frequency. At

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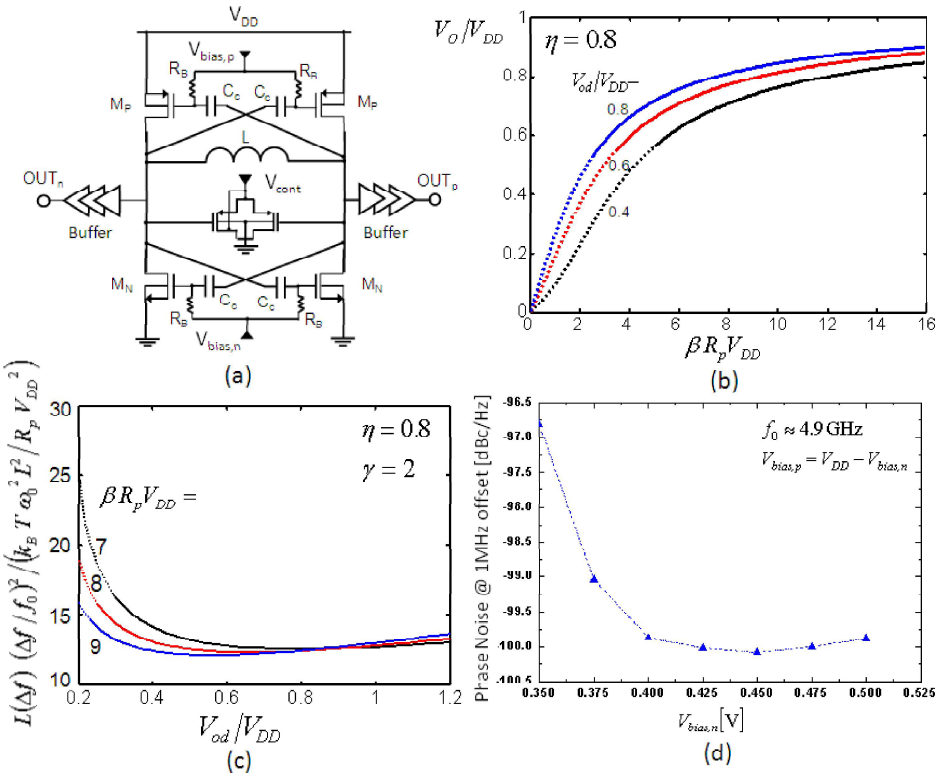

Fig. 1. (a) Schematic of a low-voltage complementary cross-coupled LC-VCO. (b) Output voltage swing and (c) phase noise calculated using a simple model as a function of $\beta R_p V_{DD}$ and V_{od}/V_{DD} (dashed lines indicate unsatisfied oscillation conditions). (d) Simulated phase noise at an offset frequency of 1 MHz as a function of the gate bias of M_N.

the resonance frequency, the impedance of the LC tank results in an equivalent parallel resistance R_p. Based on the simple analytical approach [6], the I-V restrictions in the VCO at the instance when the tank current (voltage) reaches its maximum I_O (V_O) are

$$I_O = \beta\{V_{od} + \eta V_O/2 - (1/2)(V_{DD}/2 - V_O/2)\}(V_{DD}/2 - V_O/2) \quad (1)$$

$$V_O = I_O R_p \quad (2)$$

where β and η are the transconductance parameter and the ratio of C_C to its sum with the gate-source capacitance C_{gs}, i.e. $C/(C_C + C_{gs})$, respectively, and $V_{od} = V_{bias,n} - V_{th,n} = V_{DD} - V_{bias,p} + V_{th,p}$. $V_{th,n}$ and $V_{th,p}$ are the threshold voltages of the NMOS and PMOS devices, respectively. Equation (1) assumes that the MOS devices are operating in the deep linear region and have symmetrical characteristics. The output common-mode voltage V_{CM} is assumed to be $V_{DD}/2$. Equation (1) does not neglect the squared drain-source voltage term, as in [6]. From Eqs.(1)-(2) the tank differential voltage amplitude V_O is given by

$$V_O = \frac{\kappa_2 + \sqrt{\kappa_3}}{\kappa_1} \quad (3)$$

$$\kappa_1 = (\eta + 1/2)\beta R_p \quad (4)$$

$$\kappa_2 = \beta R_p\{(\eta + 1/2)V_{DD}/2 - (V_{od} - V_{DD}/4)\} - 2 \quad (5)$$

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$$\kappa_3 = \beta^2 R_p^2\{(\eta+1/2)V_{DD}/2+(V_{od}-V_{DD}/4)\}^2 + 4[1-\beta R_p\{(\eta+1/2)V_{DD}/2-(V_{od}-V_{DD}/4)\}]. \quad (6)$$

This analytical model for the VCO provides a design methodology. Figure 1 (b) shows the calculated results for η=0.8. The value of η is set considering the occupied area limitation of C_C. V_O and V_{od} are normalized using V_{DD}. The figure reveals that the output amplitude increases with V_{od} and βR_p. However, the output amplitude tends to level off near V_{DD} when βR_p is large. The bias current of the VCO is proportional to β, and this region represents the voltage-limited region [7, 8].

The oscillation condition of the VCO is given by

$$g_{m,N}+g_{m,P} \approx 2\beta V_{od} \geq \frac{2}{R_p//(2R_{on})}, \quad (7)$$

where $g_{m,N}$, $g_{m,P}$, and $R_{on}=1/\beta V_{od}$ are the transconductances of the NMOS and PMOS devices, and the drain resistance of the MOS device in the linear region, respectively. From Eq. (7), the oscillation condition can be expressed as $\beta V_{od} R_p \geq 2$. The dashed lines in Figs. 1 (b) and 1 (c) indicate the regions that do not satisfy the oscillation condition.

3 Analysis of phase noise

The single-sideband phase noise of the VCO at the offset frequency Δf from the oscillation frequency $f_0(=\omega_0/2\pi)$, $L(\Delta f)$, is given by [9]

$$L(\Delta f) = \left(\frac{f_0}{\Delta f}\right)^2 \frac{k_B T R_{eff}}{V_O^2}(1+F_{gm}), \quad (8)$$

where k_B and T are the Boltzmann constant and temperature, respectively. R_{eff} is the effective resistance of the LC-tank, including resonator loss caused by linear-region operation of the MOS devices [7], and is given by

$$R_{eff} \approx R_{L,s}+R_{C,s}+\frac{(\omega_0 L)^2}{2R_{on}} \approx \frac{(\omega_0 L)^2}{R_p}\left(1+\frac{R_p}{2R_{on}}\right), \quad (9)$$

where $R_{L,s}$ and $R_{C,s}$ are the series resistances of the inductor and varactor, respectively. F_{gm} represents the relative contribution of MOS devices operating as a negative conductance. Based on a noise sampling model of the switching differential pairs [7], F_{gm} can be approximated by

$$F_{gm} \approx \frac{2\gamma\{(\omega_0 L)^2/R_{eff}\}I_O}{V_O} = \frac{2\gamma}{1+R_p/2R_{on}}, \quad (10)$$

where γ is the drain noise current factor. Both NMOS and PMOS devices are assumed to have the same γ value. Note that for simplification, this analytical approach does not deal with $1/f$ noise of the MOS devices. Thus, substituting Eqs. (9) and (10) into Eq. (8), the phase noise of the VCO is expressed as

$$L(\Delta f) \approx \left(\frac{f_0}{\Delta f}\right)^2 \frac{k_B T(\omega_0 L)^2}{R_p V_O^2}\left(1+2\gamma+\frac{R_p}{2R_{on}}\right). \quad (11)$$

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The three terms of Eq. (11) represent the contributions of tank resistance, the switching of the differential pair MOS devices, and the linear-region operation of the MOS devices.

Figure 1 (c) shows the calculated results for the normalized phase noise with η=0.8. The value of γ in a fabricated 90 nm NMOS device is approximately 2 [1]. As shown in Fig. 1 (c), there is an optimum V_{od} to minimize the phase noise. This is reflected by the trade-off between enhancement of the oscillation voltage amplitude and the resonant tank loss created by linear-region operation of the devices. As the oscillation frequency is around 5 GHz under 0.5 V supply voltage, the device sizes must be small to reduce their parasitic capacitance. Considering the results in Fig. 1 (c) with the gate bias less than V_{DD}, $\beta R_p V_{DD}$ around 8 and V_{od}/V_{DD} =0.5 are selected to achieve low phase noise with small device sizes. In this design the R_p of the LC tank is estimated to be around 770 Ω. Thus, the W/L sizes of the NMOS and PMOS devices of the VCO core are 4 μm × 4/100 nm and 4 μm × 16/100 nm, respectively.

Figure 1 (d) shows the gate bias dependence of the phase noise simulated using an Agilent Advanced Design System (ADS). The optimum gate biases are revealed as $V_{bias,n}$ = 0.45 V and $V_{bias,p}$ = 0.05 V, which are near V_{od}/V_{DD} =0.5. The simple optimization of the phase noise using this bias controllability is essentially similar to that used in the previous work [8].

4 Experimental results

To demonstrate the proposed complementary VCO and its design methodology, it was designed and fabricated in a 90-nm digital CMOS process without a metal-insulator-metal (MIM) capacitor process. A micrograph of the fabricated VCO is shown in Fig. 2 (a). The active chip area (without pads) of the designed VCO was 0.30×0.45 mm^2. Integrated capacitors [10] were used and their capacitance was 400 fF. The inductance and Q value of the differential symmetrical spiral inductor are 3.2 nH and approximately 10 at 5 GHz. The bias feeding resistance R_B was approximately 3 kΩ and had only a small influence on the phase noise performance. CMOS buffers with forward body biasing were used to drive the output loads. The power consumption, excluding the buffer, was 550 μW at a supply voltage of 0.5 V. Figures 2 (b) and 2 (c) show the measured output spectrum and phase noise, respectively. The VCO achieved oscillation around 5 GHz and phase noise of −98.32 dBc/Hz at 1 MHz offset. The tuning range of the VCO was 4.96 to 5.32 GHz (7%), as shown in Fig. 2 (d). A wider tuning range can be realized even under 0.5 V operation using a fully digital tuning technique [2]. Table I shows a comparison of the performance with previously reported low-voltage-operation CMOS VCOs. Figure of merit (FOM) is defined in [6]. The proposed technique achieves comparable performance in 5 GHz oscillation even with low power consumption. Compared to [6], it is expected that the complementary LC-VCO with bias controllability can be scaled while maintaining FOM, which is almost only limited by the LC tank.

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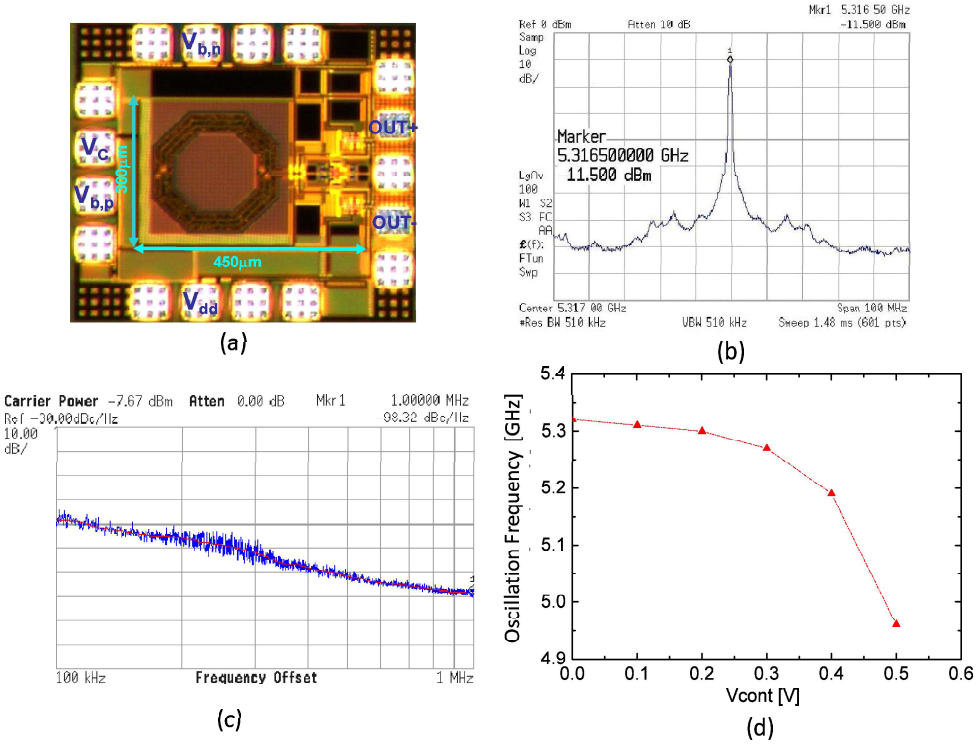

Fig. 2. (a) Micrograph, (b) output spectrum (V_{cont}=0 V), (c) phase noise characteristics (V_{cont}=0 V), and (d) tuning curve of the fabricated complementary LC-VCO ($V_{bias,n}$=0.45 V, $V_{bias,p}$=0.05 V).

Table I. Comparison of CMOS VCO performance with previous works.

	V_{DD} [V]	Center Freq. [GHz]	Phase Noise (1 MHz offset) [dB$_c$/Hz]	Power [μW]	CMOS Process [nm]	FOM [dB$_c$/Hz]
[2]	0.5	1.7	−109	186	130	−181
[3]	1.2	6.32	−118	5880	90	−186
[4](Sim.)	0.5	5.2	−117	2000	130	−188
[6]	1.8	10	−107.7	7200	180	−179
This Work	0.5	5.14	−98.3	500	90	−175

5 Conclusions

A low-voltage complementary cross-coupled differential LC-VCO was investigated using simple modeling. The VCO has bias controllability, which provides ease of design for low-voltage operation. The analytical design approach realized a 5 GHz VCO under 0.5 V supply voltage fabricated using a 90-nm digital CMOS process. It is expected that the complementary LC-VCO with bias controllability can be scaled while maintaining FOM, which is almost only limited by the LC tank.

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