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A low-power technique for pipelined ADCs with programmable gain amplification

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Abstract: A pipelined analog-to-digital converter (ADC) has been investigated, which has a programmable gain achieved by the gain control in a first-stage multiplying digital-to-analog converter (MDAC). The current consumption reduction under low gain is realized by controlling the transconductance and compensation capacitor of the MDAC circuit according to the input gain. The pipelined ADC designed using a 0.18 μm CMOS technology shows a sampling rate of 40 MSps and an input gain of 0-18 dB (6 dB-step). The maximum current consumption is 14.2 mA at the input gain of 18 dB and the minimum is 7.5 mA at 0 dB. The signal-to-noise plus distortion ratio (SNDR) is 66.1 dB for an input signal amplitude of 2 Vpp and an input gain of 0 dB, and 63.4 dB for an input signal amplitude of 250 mVpp and an input gain of 18 dB.

Keywords: pipelined A/D converter, programmable gain amplifier, controllable transconductance, low power

Classification: Integrated circuits

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1 Introduction

Pipelined ADCs are widely used as the analog front-end in systems requiring resolutions over 10-bits and sampling rates of several tens of MSps, such as communications equipment and image processing systems. A programmable gain amplifiers (PGAs) are often required as front stage of ADC in order to effectively exploit ADC resolution even with low input signal amplitudes. However, the power consumption of PGAs must be very large to drive the sampling capacitor of the ADC. A method has been proposed to eliminate the need for a PGA in the analog region, which enlarges the resolution of the ADC itself and instead uses a PGA in the digital region, thereby reducing the number of op-amps used in the analog front-end and lowering the power consumption [1]. However, when the input signal amplitude is sufficiently large and the PGA operates at low gain, the ADC resolution goes above a requirement because a required resolution becomes lower. Thus the power efficiency at low gain mode becomes lower. Another method has also been proposed that introduces programmable gain by switching between the capacitors in a cyclic ADC, thereby reducing the number of op-amps [2]. However, since the programmable gain and analog-to-digital conversion would operate in sequence, this method cannot be adapted to pipelined ADCs having rapid throughput. Furthermore, since the feedback factor is controlled in the programmable gain operation, the bandwidth and phase margin change according to the gain setting, which degrades the power efficiency during low gain operation [3].

In this letter, we propose a method for obviating PGA while maintaining the high throughput of the pipelined ADC, by embedding a programmable gain amplification in the first-stage MDAC of a pipelined ADC, and executing the programmable gain amplification simultaneously with A/D conversion. The power consumption at lower gain operation is reduced by controlling the transconductance of the input and output stages and the phase compensation capacitor of 2-stage op-amp used in the first-stage MDAC according to input gain.

2 Proposed circuit

Figure 1 (a) shows a block diagram of the proposed pipelined ADC with programmable gain amplification. The first stage consists of a 1.5 bit flash ADC and a 1.5 bit MDAC with an input gain of 6-24 dB (6 dB step). Generally, the input gain of a 1.5 bit MDAC is 6 dB, but providing a controllable range of 6-24 dB allows the pipelined ADC input gain to be controlled between 0 to 18 dB. Considering the power consumption of the flash ADC and the maximum value for the MDAC gain, an accuracy of first stage MDAC is equivalent to 4.5 bit when the input gain is 18 dB (the MDAC gain is 24 dB).

The second and third stages consist of 3.5 bit MDAC circuits with 3.5 bit flash ADCs and a gain of 18 dB. The final stage employs a 3.5 bit flash ADC, resulting in a pipelined ADC with an overall resolution of 11 bits and an input gain of 0-18 dB (6 dB step).

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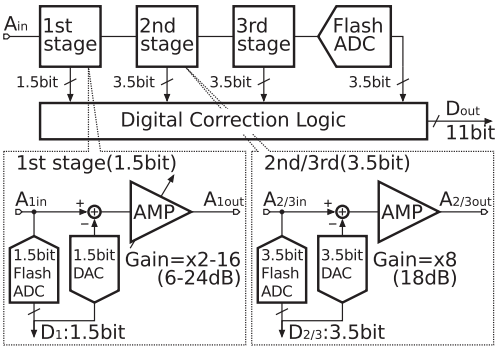
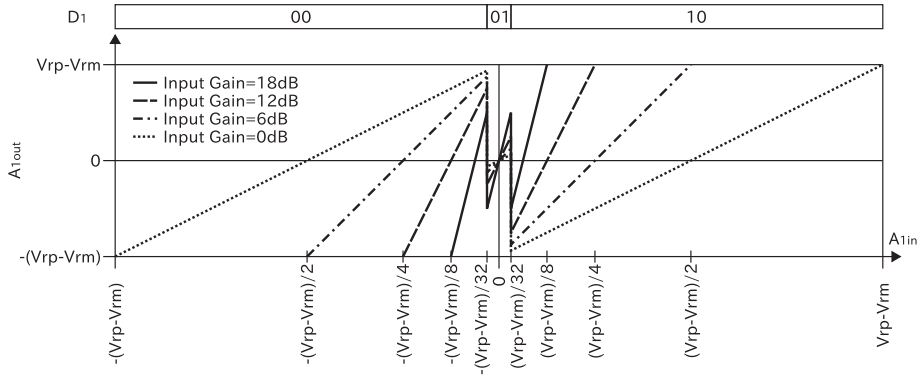


(a)

Gain [dB]	0	6	12	18
Vos,sys [V]	7/32	3/32	1/32	0
Vos,comp [mV]	31.25			
Total offset [mV]	250	125	62.5	31.25
Offset Correctable range [mV]	250	125	62.5	31.25

(c)



(b)

Fig. 1. (a) Block diagram of pipelined ADC with programmable gain amplification, (b) transfer function of the first pipelined stage, and (c) offset voltage of flash ADC at first stage ($V_{rp} - V_{rm} = 1V$).

Figure 1 (b) shows the input-output transfer function of the first-stage MDAC for each input gain. A threshold voltage of $\pm(V_{rp} - V_{rm})/32$ is employed in the flash ADC regardless of the input gain. Since the threshold voltage of the flash ADC is not controlled depending on the input gain, additional floating switches are not needed. Generally, in a 1.5 bit pipelined stage with the maximum input signal amplitude of $\pm a(V_{rp} - V_{rm})$, the threshold voltage for the flash ADC is set at $\pm a(V_{rp} - V_{rm})/4$. By keeping the input offset voltage for the comparator used in the flash ADC within $\pm a(V_{rp} - V_{rm})/4$, the influence of the comparator input offset voltage can be compensated for by a digital correction circuit [4]. In the proposed circuit, for input gains of 18, 12, 6 and 0 dB, the maximum input signal amplitudes are $\pm(V_{rp} - V_{rm})/8$, $\pm(V_{rp} - V_{rm})/4$, $\pm(V_{rp} - V_{rm})/2$ and $\pm(V_{rp} - V_{rm})$, respectively. As the threshold voltage for the flash ADC is set to the identical value of $\pm(V_{rp} - V_{rm})/32$ for all input gain modes, the transfer functions for the 12, 6 and 0 dB modes are equivalent to the cases for the comparator with systematic input offsets ($V_{os,sys}$) of $(V_{rp} - V_{rm})/32$, $3(V_{rp} - V_{rm})/32$ and $7(V_{rp} - V_{rm})/32$, respectively. As shown in Figure 1 (c), when the differential reference voltage $(V_{rp} - V_{rm})$ is 1 V, the systematic offset and the comparator offset is corrected with the digital correction circuit at all input gain by maintaining the comparator offset voltage ($V_{os,comp}$) below 31.25 mV.

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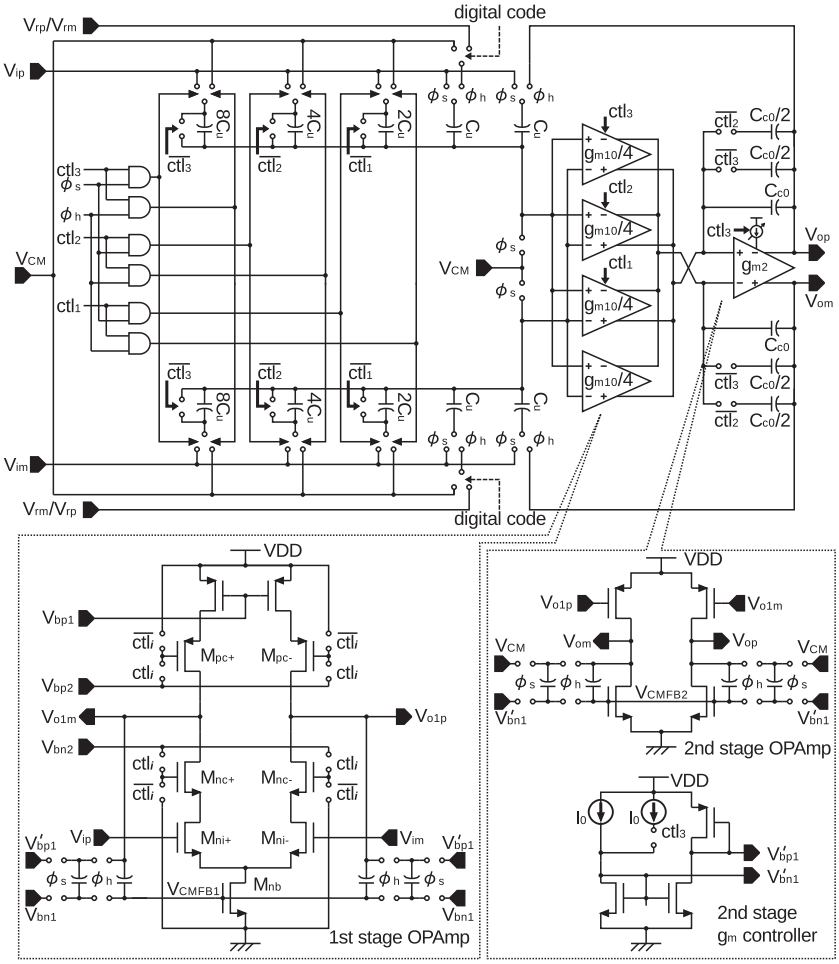

(a)

Input gain[dB]	0	6	12	18
β_F	1 / 2	1 / 4	1 / 8	1 / 16
g_{m1}	1 / 4	2 / 4	3 / 4	1
g_{m2}	0.7	0.7	0.7	1
Cc	2.0	2.0	3 / 2	1

(b)

Fig. 2. (a) MDAC circuit of the first stage with programmable gain and (b) its key parameters normalized by ones for input gain of 18 dB.

Figure 2 (a) shows the MDAC with programmable gain amplification. Programmable gain is achieved by controlling the number of sampling capacitors. In 0 dB mode, ctl_i (i = 1, 2, 3) digits are all set to "Low", the input signal is sampled by $2C_u$, and the feedback capacitor during amplification is C_u, so the gain of the MDAC is two (6 dB). In 18 dB mode, all the ctl_i digits are set to "High", the input signal is sampled by $16C_u$, and the feedback capacitor during amplification is C_u. As a result, the gain of the MDAC circuit is 16 (24 dB). In the same way, ctl_1="High", ctl_2="Low", and ctl_3="Low" are set for 6 dB mode, and ctl_1="High", ctl_2="High", and ctl_3="Low" for 12 dB mode.

In a switched capacitor circuit with a programmable gain amplification,

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the bandwidth and phase margin changes depending on input gain, causing lower power efficiency [3, 5]. Controlling the transconductance of the input and output stages and the compensation capacitor of the 2-stage op-amp appropriately according to the gain, enhances the power efficiency at low gain [5]. A reduction in power consumption at low input gains is obtained by applying this technique to the MDAC of the proposed pipelined ADC.

Bandwidth (ω_c) and phase margin (ϕ_m) of MDAC composed of 2-stage opamp with compensation capacitor are given by

$$\omega_c = \omega_2 \left[\sqrt{\frac{1}{4} + \left(\frac{\omega_1}{\omega_2}\right)^2} - \frac{1}{2} \right]^{\frac{1}{2}}, \phi_m = \tan^{-1} \left[\sqrt{\frac{1}{4} + \left(\frac{\omega_1}{\omega_2}\right)^2} - \frac{1}{2} \right]^{-\frac{1}{2}}, \quad (1)$$

$$\omega_1 = \beta_F \frac{g_{m1}}{C_C}, \quad \omega_2 = \frac{g_{m2}}{C_L + C_{p2} + C_L C_{p2}/C_C}, \quad (2)$$

where $\beta_F (= (2G)^{-1})$ is the feedback factor of MDAC, G is the input gain of ADC, g_{m1} and g_{m2} are the transconductance of input and output stages respectively, C_C, C_L and C_{p2} are the phase compensation capacitor, the load capacitor and the input parasitic capacitor of output stage respectively. The power consumption at low gain mode is reduced by suppressing the changes of ω_c and ϕ_m caused by change of β_F. Figure 2 (b) shows g_{m1}, g_{m2}, and C_C for each input gain. The value of each parameter is normalized so that it is unity in the 18 dB input gain. The g_{m1} is controlled linearly against the β_F controlled exponentially. C_C is controlled to make the ω_c constant. The change of ω_2 caused by the variation of C_C is suppressed through controlling g_{m2}. As a result, the power efficiency at low gain mode is improved without large increase in a noise and die-area [5]. In addition, the factor of 0.7 is determined considering C_{p2} and the load capacitance including the influence of the feedback capacitors to achieve over 100 MHz bandwidth [5], and it will slightly vary depending on a target specification.

The op-amps in the MDAC consist of an input stage in which ctl_i varies the number of operating parallel-connected amplifiers to control g_{m1}, an output stage which has variable g_{m2} achieved by controlling the bias voltage, and a controllable C_C.

g_{m1} is controlled by the number of operating parallel-connected amplifiers, so the current consumption I_1 in the input stage is proportional to g_{m1}. g_{m2} is controlled by varying the bias voltage V'_{bn1} and V'_{bp1} in the output stage, so the consumption current I_2 in the output stage is proportional to the square of g_{m2}. Assuming the ratio I_1/I_2 of 1/2, the current consumption in the first-stage MDAC at the 0 dB mode is achieved to be reduced by about 60% from at 18 dB mode.

Even if the PGA is still embedded in the analog front-end to achieve the required ADC resolution, the proposed technique can reduce the required gain variation in the PGA. By the adequate design, power consumption reduction in the overall analog front-end is expected even considering the increase of the required drivability of PGA due to the variation of sampling capacitance of the ADC.

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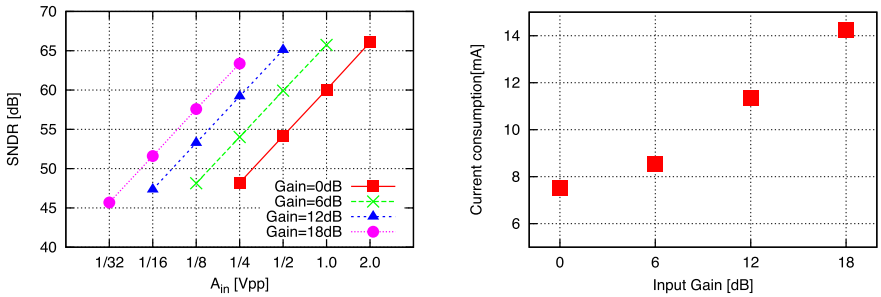

(a) (b)

Fig. 3. Simulation results of the designed pipelined ADC. (a) Input voltage gain versus SNDR and (b) input voltage gain versus current consumption.

3 Simulation results

A pipelined ADC with a programmable input gain amplitude of 0-18 dB (6 dB step) and 11-bit resolution has been designed using a 0.18 μm CMOS process with 3 V devices and metal-insulator-metal capacitors. The operating supply voltage is 3.3 V. Figure 3 (a) shows simulation result of the relationship between the differential input signal amplitude (Ain) and the signal-to-noise plus distortion ratio (SNDR) at each input gain. The SNDR is calculated by applying an 8192-point FFT to the results of *Spectre* transient noise simulation with a throughput of 40 MSps and an input signal frequency of 97.65625 kHz. Under an input signal amplitude of 250 mVpp, it is confirmed that increasing the gain of the first-stage MDAC improves the SNDR by about 6 dB per step. For an input signal amplitude of 2.0 Vpp and an input gain of 0 dB, the maximum SNDR was 66.1 dB, and for an input signal amplitude of 250 mVpp and an input gain of 18 dB, the maximum SNDR was 63.4 dB. Thus, a high SNDR is confirmed even at low signal amplitudes. The SNDR at maximum amplitude is degraded as the input gain increased because the output referred kT/C noise in the first-stage MDAC increases in proportion to the square root of the input gain.

Figure 3 (b) shows the mean current consumption during operation under each gain mode. The highest current consumption is 14.2 mA, occurring under an input gain of 18 dB. It is lowest in the 0 dB mode, at 7.5 mA. Thus, power consumption reduction of 47% is confirmed compared to the 18 dB case.

4 Conclusion

This letter has discussed low power technique for a pipelined ADC with programmable gain amplification. Programmable gains of 0-18 dB (6 dB step) are successfully implemented by controlling the number of sampling capacitors in the first-stage MDAC circuit. A simulation result confirms a SNDR value of 66.1 dB for an input signal amplitude of 2.0 Vpp and an input gain of 0 dB, and 63.4 dB for an input signal amplitude of 250 mVpp and an input gain of 18 dB. Controlling the transconductance of the input and output

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stages and the phase compensation capacitance of the 2-stage op-amp in the first-stage MDAC circuit according to the gain provides a power consumption reduction at low gain and leads to a high power efficiency. In a design using a 0.18 μm CMOS process, the maximum current consumption is 14.2 mA for an input gain of 18 dB and the lowest is 7.5 mA for an input gain of 0 dB. A 47% improvement of the power consumption at the input gain of 0 dB is achieved by using the proposed circuit techniques.

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