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# Low-power wireless on-chip microparticle manipulation with process variation compensation

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**Abstract:** A chip with which to manipulate microparticles using wireless power transfer and pulse-driven dielectrophoresis has been designed and fabricated using a 0.18- $\mu\text{m}$  CMOS process. The chip enables microparticle manipulation using a 0.35-V power supply and a 10~100 kHz clock, which are generated on the chip by means of an on-chip coil, a rectifier and a ring oscillator circuit with process variation compensation circuits. The proposed process variation compensation with effective gate-width tuning as well as body biasing can achieve stable 0.35-V operation, allowing a 87% reduction in the power consumption of digital circuits on the chip compared to previous work.

**Keywords:** dielectrophoresis, microparticle manipulation, CMOS, wireless power transfer, low-voltage operation

**Classification:** Micro- or nano-electromechanical systems

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## 1 Introduction

In recent years, sensor and control circuits have been integrated onto chips in order to make equipment more compact, inexpensive, and easy-to-use. Wireless power transfer can improve these features [1]. In addition, manipulation of particles and cells is also useful for efficient sensing [2]. Dielectrophoresis (DEP), in which particles move under the influence of a driving force generated by the gradient of the electric field intensity [3, 4], is a promising technique for this purpose.

A recent study has demonstrated wireless on-chip microparticle manipulation using pulse-driven dielectrophoresis [2]. In order to prevent the solution temperature from increasing due to the power consumption of the chip and wireless power transfer loss through the chip, the chip must be operated at a low supply voltage. It is also useful to reduce the output of the wireless power transmitter. Therefore, we investigated on-chip microparticle manipulation under a low supply voltage and frequency using process variation compensation with effective gate-width tuning [5], as well as body biasing based on previous work [6, 7, 8].

## 2 System design

Figure 1 shows the proposed wireless on-chip microparticle manipulation system. The sinusoidal AC signal received by the on-chip secondary coil, which is inductively coupled to an external primary coil, is converted to the on-chip DC supply  $V_{DD}$  using the rectifier, as in the previous circuit [2]. To produce

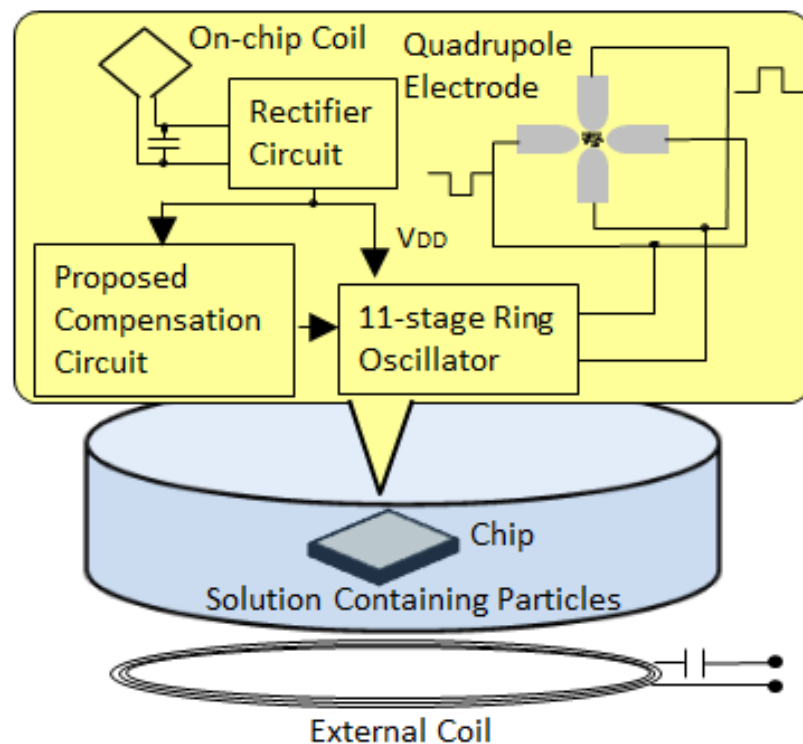


Fig. 1. Proposed wireless on-chip microparticle manipulation system.

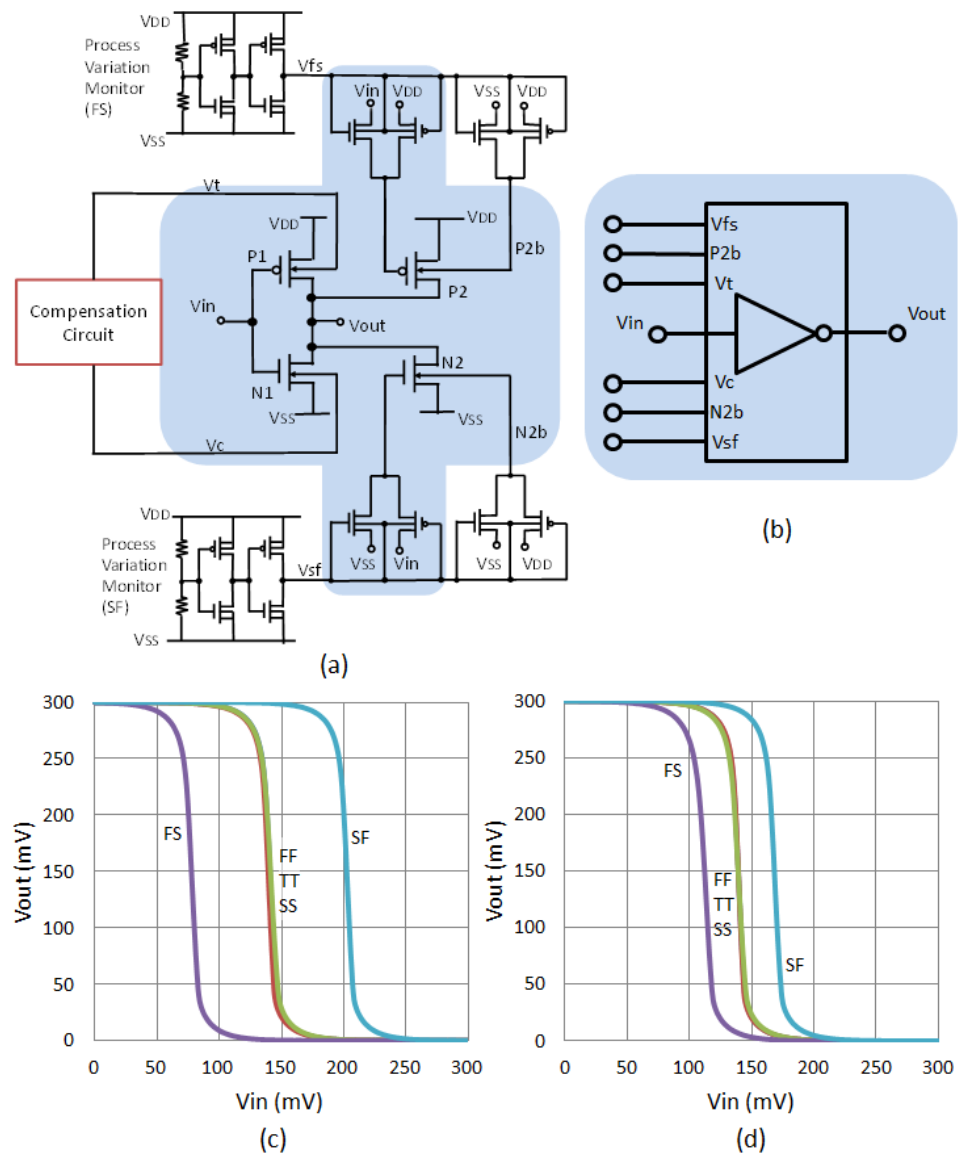
the DEP driving pulse signal, the proposed system uses an 11-stage ring oscillator instead of waveform shaping with the Schmitt trigger and frequency divider used in the previous circuit [2]. This is useful for optimizing both the sinusoidal AC signal and DEP driving pulse signal frequencies. To enhance the wireless power transfer efficiency, the AC signal can be set higher. On the other hand, to reduce the chip power consumption, the DEP driving pulse signal frequency can be set lower.

We set the on-chip supply voltage to  $V_{DD} = 0.35$  V, which is half of that used in the previous work [2]. Under a lower supply voltage, threshold voltage variation significantly influences circuit characteristics. To solve this problem, process variation compensation techniques are required. The body biasing used in previous work [6, 7, 8] is such a technique; however, at 0.35 V it cannot function sufficiently due to limited body biases. Therefore, we developed an additional process variation compensation technique with effective gate-width tuning [5].

### 3 Effective gate-width tuning

Figure 2 (a) shows an example of a CMOS inverter using the proposed technique. Note that the triple-well CMOS process is required in this technique. Although there is a little population for fast-NMOS slow-PMOS (“FS”) and slow-NMOS fast-PMOS (“SF”) due to correlation between NMOS and PMOS devices on the same die [9], their process corners are considered for more stable subthreshold circuit operation in this work. A MOSFET (P1 or N1) is connected in parallel with another MOSFET (P2 or N2) and each gate and body terminal of P2 and N2 is connected through a switch according to process variation monitoring (“FS” and “SF”). Note that the bodies of N1 and P1 are biased to compensate process variation based on previous work [6, 7]. When the gate switch of N2 is connected to a  $V_{in}$  terminal and the body terminal is applied to  $V_{DD}$  in the case of “SF”, this enhances the NMOS (N1 and N2) drive current, corresponding to N1’s extending gate width. On the other hand, when the switches are connected to the opposite terminals, NMOS N1 and N2, normal drive current flows. A similar operation is possible for the PMOS (P1 and P2) current in the case of “FS”. Figure 2 (b) shows a simplified diagram of the blue area in the CMOS inverter shown in Fig. 2 (a). The 11-stage ring oscillator circuit is composed of these CMOS inverters, which share the terminal voltages at  $V_t$ ,  $V_c$ ,  $V_{fs}$ ,  $V_{sf}$ , P2b, and N2b.

The proposed circuit was designed in a 0.18  $\mu\text{m}$  CMOS process. Note that the circuits in this work operate completely in the subthreshold region in the supply voltage range of 0.3 to 0.35 V. Table I shows the simulation conditions used for the design of the digital circuits. As shown in Fig. 2 (c), conventional CMOS inverters have large logic threshold-voltage variation. The proposed technique can reduce it by about 50%, as shown in Fig. 2 (d). The temperature dependence of the operation speed in the CMOS logic circuits can be reduced with the proposed technique, as shown in previous work [5]; however,



**Fig. 2.** (a) The proposed technique in a CMOS inverter circuit and (b) the simplified CMOS inverter circuit, and the characteristics of the CMOS inverter in each process corner (c) without the proposed technique and (d) with it.

**Table I.** Simulation condition.

$V_{DD}$	Gate-width/Gate-length of P1 and N1	Gate-width/Gate-length of P2 and N2
0.3 V	$1.0 \mu\text{m}/0.18 \mu\text{m}$	$0.22 \mu\text{m}/0.18 \mu\text{m}$

it is not so important in this work because the solution temperature is nearly constant for stable DEP operation.

#### 4 Power consumption

The power consumption of digital circuits is given by

$$P \propto f_C C_L V_{DD}^2, \quad (1)$$

where  $C_L$  is the load capacitance,  $f_C$  is the clock frequency, and  $V_{DD}$  is the DC supply voltage. This equation shows the significance of a low supply voltage. In this work, the  $V_{DD}$  is half of that used in previous work (0.7 V) [2].

In addition to a low supply voltage, we set a low-frequency operation DEP, using the 11-stage ring oscillator circuit operating under low-voltage. The frequency of the output pulse signals was about 100 kHz.

The power consumption of the Schmitt trigger circuit in the previous work [2] was  $6.77 \mu\text{W}$ , but in this investigation, the power consumption of the 11-stage ring oscillator with compensation circuits was  $0.877 \mu\text{W}$ . In other words, we achieved an 87% reduction in power consumption in spite of increase in number of devices.

#### 5 Experimental results

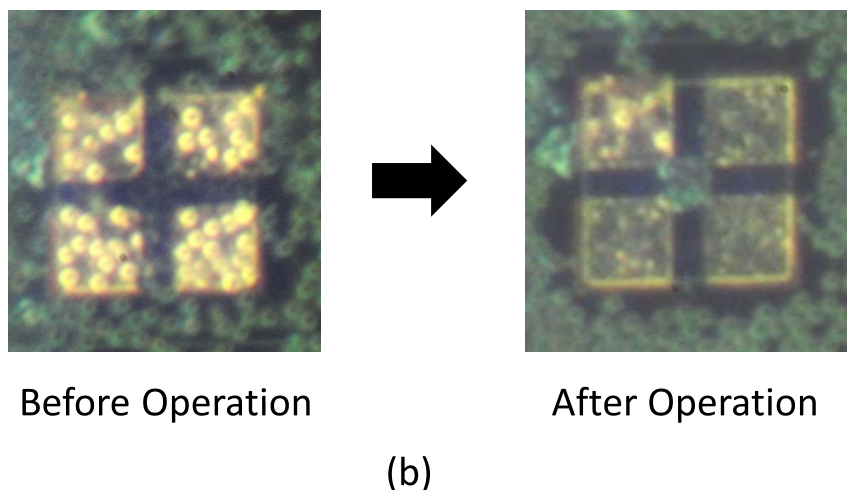
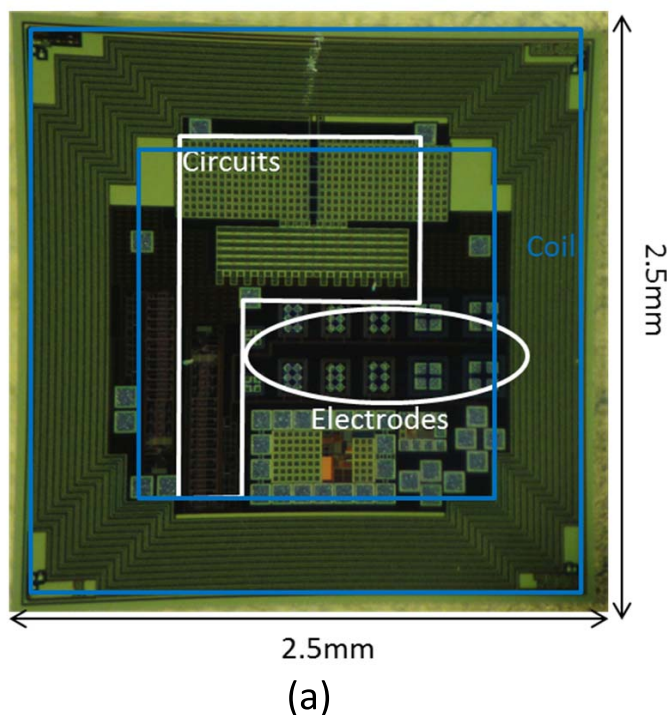
An optical microphotograph of the test chip fabricated using a  $0.18\text{-}\mu\text{m}$  triple-well CMOS process is shown in Fig. 3(a). The chip size is  $2.5\text{ mm}$  square, shown with an on-chip 11-turn coil around the edge. The external primary coil, which is the same as the previous one [2], has a magnetic sheet (ALPS HMSZS21020, permeability:  $80 - j25$  at  $13.56\text{ MHz}$ ) embedded in the bottom side.

After dropping pure water (conductivity:  $\sigma_m < 1\text{ mS/m}$ ) containing polystyrene microparticles (diameter:  $r_e = 5\text{ }\mu\text{m}$ ) onto the chip, AC power was provided to the chip through wireless power transfer to drive the electrodes for the DEP operation. The sinusoidal input of the external primary coil with the series capacitor was set to an amplitude of  $\sim 20\text{ V}$  and frequency of  $3\text{ MHz}$ , which are reduced from those used in the previous work [2].

Figure 3(b) shows microscope observations before the DEP operation (left) and 2 minutes after the start of the DEP operation (right). It can be seen that the polystyrene microparticles between the electrodes are concentrated in the center, which means negative DEP.

#### 6 Conclusion

In order to achieve low-power operation, we proposed process variation compensation with effective gate-width tuning and body biasing. Using the proposed method we achieved  $0.35\text{-V}$  operation. In addition, we selected an 11-stage ring oscillator as a circuit that produces driving signals in the electrodes for the DEP operation. As a result, we achieved an 87% reduction in the power consumption of digital circuits on the chip. Power consumption and power loss through wireless transfer on the chip increase the solution temperature during DEP operation; hence this result is useful in preventing such temperature increases.



**Fig. 3.** (a) Optical micrograph of the fabricated chip, (b) Microscope observation of negative DEP of polystyrene microparticles (diameter:  $r_e = 5 \mu\text{m}$ ) in pure water (conductivity:  $\sigma_m < 1 \text{ mS/m}$ ) on electrodes where the input voltage of the external primary coil with a series capacitor is sinusoidal (amplitude:  $\sim 20 \text{ V}$ , frequency:  $3 \text{ MHz}$ ).

Although the present study is still in its preliminary stages, we believe that it will help to facilitate the development of sensing technology and make dielectrophoresis easier to use.

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