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A Low-Voltage SOI-CMOS LC-Tank VCO with Double-Tuning Technique Using Lateral P-N Junction Variable Capacitance

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SUMMARY For wireless communication, a low-voltage monolithic LC-tank CMOS voltage-controlled-oscillator (VCO) is developed with 0.2-μm fully-depleted silicon-on-insulator (SOI) CMOS process technology. The VCO features a double-tuning technique to achieve a wide tuning range with lateral p-n junction varactors. The VCO has the following features at the supply voltage of 1.5 V: (1) Output frequency range from 1.07 GHz to 1.36 GHz, (2) Third-harmonic below −37 dBc, and (3) Phase noise of −120 dBc/Hz at 1 MHz offset frequency.

key words: *voltage-controlled oscillator, wireless communication, CMOS, SOI, double-tuning*

1. Introduction

The rapid growth in digital wireless communications has brought an increasing demand for high-performance radio frequency (RF) circuits in low-cost technologies. A major challenge is to realize CMOS single chip tranceivers. One of the most critical circuit blocks is the voltage-controlled-oscillator (VCO) because the phase noise of the VCO determines the quality and reliability of the data transmission. LC-tank VCOs are the most promising technique to achieve low phase noise [1], [2]. Thus, CMOS LC-tank VCOs with on-chip spiral inductor have been intensively studied to improve the phase-noise performance [2]. Although a CMOS LC-tank oscillator shows better noise performance, the integrated LC-tank VCO generally has a narrow tuning range. To achieve a wide tuning range, switched tuning techniques have been proposed [3], [4]. However, the switched tuning techniques increase circuit complexity.

The tuning range of the integrated LC-tank VCO is mainly limited by parasitic capacitance, C_{par}, between LC-tank and Si substrate, which is given by

$$tuning\ range\left(\frac{f_{max}-f_{min}}{f_{average}}\right) \approx \frac{C_{V,max}-C_{V,min}}{C_{V,max}+C_{V,min}+C_{par}} \quad (1)$$

where $C_{V,max}$ and $C_{V,min}$ are maximum and minimum capacitances of the varactors used. Equation (1) means that large parasitic capacitance results in narrow tuning range.

The use of Silicon-On-Insulator (SOI) reduces parasitic capacitance [5], in particular, the drain junction capacitance of SOI-MOSFETs because SOI devices are isolated from Si substrate with buried oxide as shown in Fig. 1. The buried oxide thickness of 100–200 nm is comparable to a half of field oxide thickness in bulk-CMOS (200–400 nm). Also, the use of high-resistive SOI substrates achieves high-quality on-chip spiral inductors [6] for RF CMOS circuits [6], [7], and leads to low substrate crosstalk [8]. The reduction of crosstalk has an advantage over bulk-CMOS when analog and digital circuit blocks are integrated together on an identical chip. However, the operation voltage of SOI-MOS devices has been kept low for their long term reliability, which makes it difficult to design VCOs with a wide frequency tuning range.

Fully-depleted SOI-CMOS technology allows the threshold voltage low due to its good subthreshold characteristics, resulting in the high performance of low

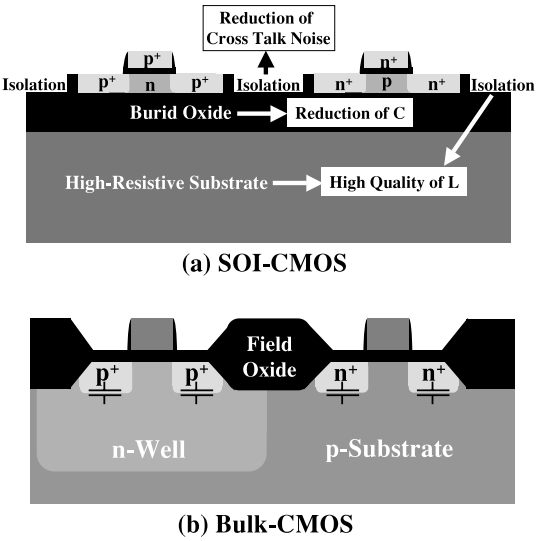

Fig. 1 Cross-section of CMOS transistors fabricated in (a) SOI-CMOS and (b) Bulk-CMOS.

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voltage digital circuits. This is a significant merit in developing one-chip phase-locked-loop frequency synthesizer.

In this paper, we propose a double-tuning LC-tank VCO with lateral p-n junction diodes using fully-depleted SOI-CMOS technology. In Sect. 2, circuit design concept will be shown. The paper will also present some measured results of the LC-tank VCO fabricated in 0.2-μm fully-depleted SOI-CMOS process technology in Sect. 3.

2. Circuit Design

2.1 VCO Circuit

Figure 2 shows a schematic of the VCO with two control voltages, V_{cnt1} and V_{cnt2}, which is referred to a double tuning technique. The n-channel SOI-MOSFET M_s, a source follower controlled by V_{cnt2}, has no body effect and acts as an ideal level shifter, providing a virtual supply voltage. H-gate SOI-MOSFET with P^+ diffusion contact underneath a part of the gate as shown in Fig. 3 [5] is used to keep the source voltage of M_s constant. The body of H-gate SOI-MOSFET M_s is tied to the source with large gate-source capacitance, resulting in stable body voltage. These features keep the source voltage of M_s constant during circuit operation. On the other hand, M_p and M_n in Fig. 2, are designed with floating-body SOI-MOSFETs for RF operation.

Using the drain DC current of M_s, I_{bias}, the equations including the source DC level of M_s, V_{CM}, are given by

$$V_{cnt2} - V_{CM} - V_{thn} = \sqrt{2I_{bias}/\beta_{Ms}}, \quad (2)$$

$$V_{CM} - V_{thn} = \sqrt{I_{bias}/\beta_{Mn}}, \quad (3)$$

where V_{thn} is the threshold voltage of n-channel SOI-MOSFETs, β_{Ms} and β_{Mn} are transconductance parameters (β's) of M_s and M_n (M_p), respectively. From these equations, V_{CM} and I_{bias} are given by

$$V_{CM} = \frac{V_{cnt2} - V_{thn}(1 - \sqrt{2\beta_{Mn}/\beta_{Ms}})}{1 + \sqrt{2\beta_{Mn}/\beta_{Ms}}}, \quad (4)$$

$$I_{bias} = \frac{\beta_{Mn}}{(1 + \sqrt{2\beta_{Mn}/\beta_{Ms}})^2}(V_{cnt2} - 2V_{thn})^2. \quad (5)$$

In this design, $\beta_{Mn}/\beta_{Ms} = 1/2$ is used to reduce the effect of V_{thn} fluctuation on the virtual supply voltage V_{CM}. Substituting $\beta_{Mn}/\beta_{Ms} = 1/2$ to Eq. (5),

$$I_{bias} = \frac{\beta_{Mn}}{4}(V_{cnt2} - 2V_{thn})^2. \quad (6)$$

There are two operation modes for a typical LC oscillator [9]; *current-* and *voltage-limited regimes*. In the current-limited regime, the tank amplitude linearly grows with the bias current until the oscillator enters the voltage-limited regime. In the voltage-limited regime, however, the amplitude is limited to V_{CM}. For SOI-VCOs operating in the current-limited regime, the amplitude of differential signals, $A = |V_p - V_n|_{max}/2$, is expressed as,

$$A = 2R_{eq}I_{bias}/\pi, \quad (7)$$

$$R_{eq} = \omega_0 L Q_{tank}, \quad (8)$$

where $\omega_0 = 1/\sqrt{LC}$, R_{eq} and Q_{tank} are the equivalent parallel resistance and Q value of the LC-tank, respectively.

2.2 Design of LC-Tank

The resonant frequency of the LC-tank with on-chip spiral inductors and varactors is expressed as $1/2\pi\sqrt{LC}$ which can be tuned by changing their capacitance. A variable capacitance is one of the critical components in the design of RF VCO. Among several structures of variable capacitor [10], [11], MOS varactors have significant nonlinearity and traditional areal bulk p-n junction diodes have parasitic resistance. To solve their

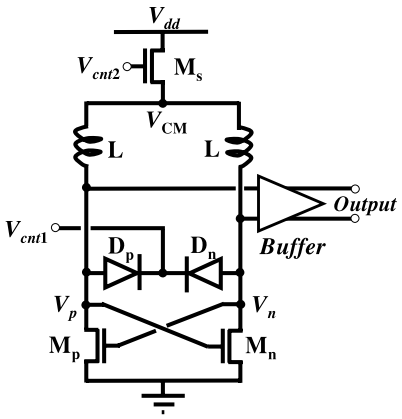


Fig. 2 Schematic of the LC-tank SOI-CMOS VCO using double-tuning technique with lateral p-n junction diodes.

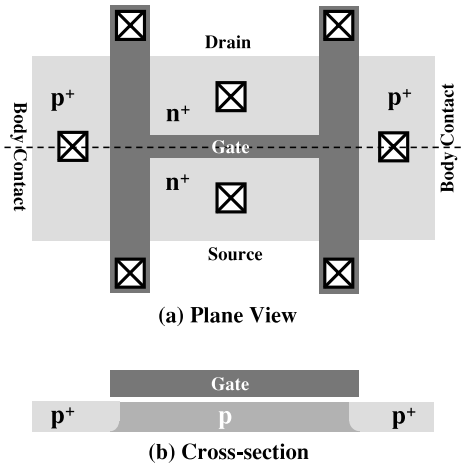


Fig. 3 H-gate SOI n-channel MOSFET with body contacts: (a) plane view and (b) cross-section.

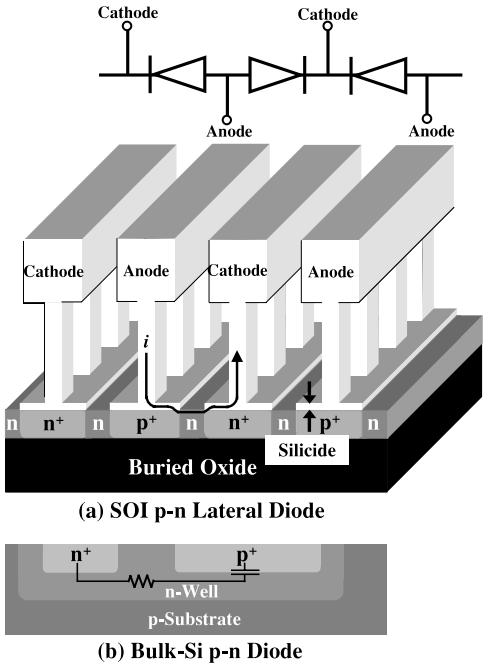


Fig. 4 Structure of the lateral p-n junction diodes. Silicided n-doped and p-doped layers are interdigitated to reduce parasitic resistance.

problems, we used lateral p-n junction diodes shown in Fig. 4(a) as the varactor whose nonlinearity is much smaller than MOS varactors. The anodes and cathodes are silicided to reduce their parasitic resistance. The area penalty of the lateral p-n junction diodes is tolerable in RF circuit blocks with spiral inductors because it occupies the area comparable to that of the spiral inductor. For higher oscillation frequencies, the occupied area of the lateral p-n junction diodes can be made smaller.

In a first order of approximation, the losses of the varactor and inductor depend only on the series resistance:

$$R_{eq} \approx \frac{1}{\omega_0 C}\left(\frac{1}{Q_{var}} + \frac{1}{Q_{ind}}\right)^{-1} \tag{9}$$

$$= \left(\frac{L^2}{R_{Svar} + R_{Sind}}\right)\omega_0^2, \tag{10}$$

$$Q_{var} = \frac{1}{\omega_0 C R_{Svar}}, \tag{11}$$

$$Q_{ind} = \frac{\omega_0 L}{R_{Sind}}, \tag{12}$$

where R_{Svar} and R_{Sind} are series resistances of the varactor and inductor [12]. In Eq. (10), for a given L, R_{eq} is inversely proportional to $R_{Svar} + R_{Sind}$.

In the lateral p-n junction diodes, as described in the preceding, the anodes and cathodes are silicided to reduce their parasitic resistance R_{Svar} so that the silicided lateral p-n junction diode has much lower parasitic resistance compared to the bulk p-n junction diode shown in Fig. 4(b). From Eqs. (7), (8), (9), (10) and (11), it is found that the lateral p-n junction diode realizes both a high quality factor and a large signal amplitude due to high R_{eq}.

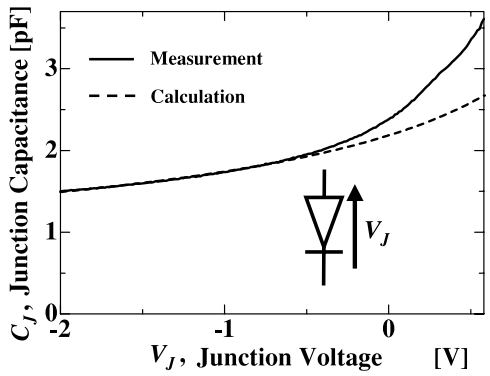


Fig. 5 Solid curve: capacitance of the p-n junction varactor as a function of the applied reverse-bias voltage. Dashed curve: calculated capacitance derived from Eq. (13).

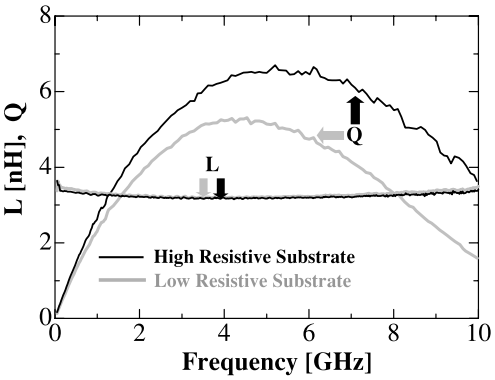


Fig. 6 Measured inductance and Q_{ind} of the on-chip spiral inductors fabricated on high and low resistivity SOI substrates.

Figure 5 shows the lateral p-n junction capacitance versus the applied reverse-bias voltage. Assuming the abrupt profile of dopant concentration (p^+-n), the capacitance C_J of the p-n junction diode shown in Fig. 4(a) is expressed as [13],

$$C_J = C_0(V_{bi} - V_J)^{-1/2}, \tag{13}$$

$$C_0 = \sqrt{qN_D\epsilon_S/2}\, S, \tag{14}$$

N_D is the dopant concentration in n-region, ϵ_S dielectric constant of silicon, S the diode area and V_{bi} a built-in potential. Figure 5 shows that the capacitance near $V_J = 0$ is larger than that calculated from Eq. (13) because of diffusion capacitance induced by injected excess minority carriers. The large diffusion capacitance and forward diode current in the LC-tank prevent the VCO from oscillating.

Figure 6 shows the measured inductance and Q_{ind} of the spiral inductors fabricated on the high resistivity and low resistivity SOI substrates. The resistivity of high- and low-resistive substrate are about 1 kΩ·cm and 20–30 Ω·cm, respectively. The measured inductance is

nearly constant in the frequency range measured. The inductance on a high-resistive SOI substrate has higher Q_{ind} than that on a low resistivity one due to small eddy current. Thus, high-resistive SOI substrate realizes a high quality factor of the inductor together with a large signal amplitude. At the operation frequency around 1GHz, the VCO has little difference in characteristic due to the small change in quality factor between high- and low-resistive substrates. High-resistive SOI substrate is, however, expected to give remarkable advantages over low-resistive one especially for future higher oscillation frequency.

2.3 Double Tuning Method

The VCO has two control voltages, the main control voltage, V_{cnt1}, and the auxiliary control voltage, V_{cnt2}, as shown in Fig. 2. For a given V_{cnt2}, V_{cnt1} is used to tune a desired oscillation frequency.

Figure 7 shows the available range of V_{cnt1}. The voltage across the diode, V_J, is given by

$$V_J = V_{CM} - V_{cnt1} \tag{15}$$
$$\approx V_{cnt2}/2 - V_{cnt1}. \tag{16}$$

The junction voltage V_J should be kept negative during oscillation, from which the following form can be derived.

$$V_{cnt2}/2 + A - V_{bi} < V_{cnt1} < V_{dd}. \tag{17}$$

From Eqs. (7), (10), (13) and (16),

$$A = \frac{2\beta_{Mn}L}{\pi(R_{Svar}+R_{Sind})C_0}(V_{cnt2}/2 - V_{thn})^2 \times\sqrt{V_{cnt1} - V_{cnt2}/2 + V_{bi}}. \tag{18}$$

The amplitude of differential signals A strongly depends on V_{cnt2} so that large V_{cnt2}, meaning a large swing of A, induces the harmonic distortion. Nonetheless the average value of the capacitance is still a function of V_J, providing a specific tuning range. The circuit suffers from a trade-off between the amplitude of differential signals and the harmonic level. So, within an acceptable harmonic level, we can control the amplitude using V_{cnt2}, for which, tuning to a required oscillation frequency is achieved by controlling V_{cnt1}.

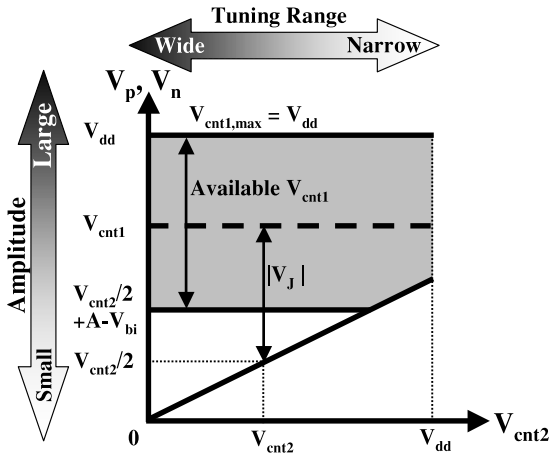


Fig. 7 Schematic explanation of the double-tuning technique with p-n junction varactors. There is trade-off between the range of junction voltage and the amplitude of oscillation. The shaded region represents the available range of V_{cnt1} for the LC-tank VCO.

3. Experimental Results

Figure 8 shows a micro-photograph of the VCO (core) fabricated in 0.2-μm fully-depleted SOI-CMOS process technology, which occupies $1 \times 1\,\mathrm{mm}^2$. The characteristics of the VCO are summarized in Table 1.

3.1 Fundamental Characteristics

Figure 9 shows the frequency spectrum of the VCO measured with a spectrum analyzer (Agilent 8562EC), which exhibits the oscillation frequency of about 1.3 GHz. Since the second-harmonic could be removed by using a balun in the following stage, we focus on the third-harmonic. Figure 10 shows the dependence of the third-harmonic on two control voltages, V_{cnt1} and V_{cnt2}. The third-harmonic level is below -37 dBc. The third-harmonic sharply increases with V_{cnt2} because the signal amplitude depends on V_{cnt2} as shown in Eq. (18). The large amplitude induces electron mobility degradation on the gate voltage in M_p and M_n in

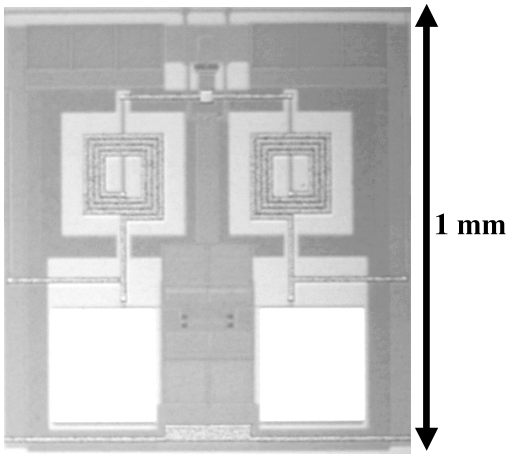


Fig. 8 Micro-photograph of the VCO (core) fabricated in 0.2-μm SOI-CMOS process technology.

Table 1 Summary of the VCO characteristics.

Supply Voltage	1.5 V
Tuning Range	1.07–1.36 GHz
Third-Harmonic	below -37 dBc
Phase Noise @ 1 MHz offset	-120 dBc/Hz
Output Level	-12 dBm
Dissipation Current (VCO core)	3.8–8.5 mA

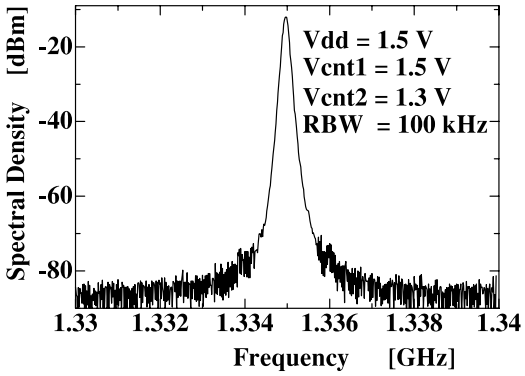


Fig. 9 Frequency spectrum of the VCO measured with a spectrum analyzer (Agilent 8562EC), which exhibits the oscillation frequency of about 1.3 GHz.

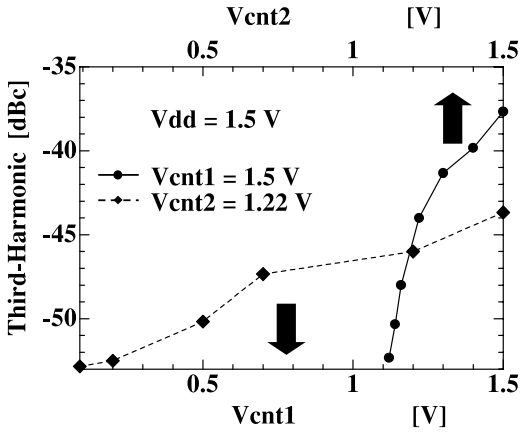


Fig. 10 Dependence of the third-harmonic on two control voltages, V_{cnt1} and V_{cnt2}. The increase of third-harmonic with V_{cnt1} is moderate compared to V_{cnt2}.

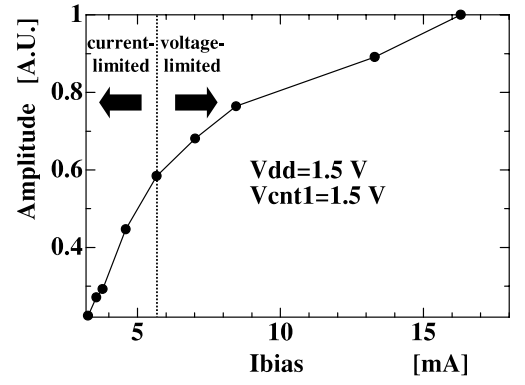
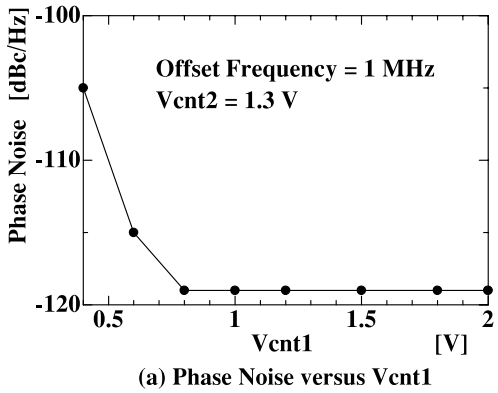


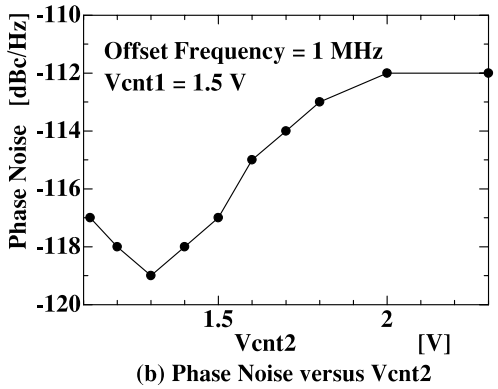
Fig. 11 Amplitude of the VCO versus I_{bias}.

their linear-region operation, and leads to non-linearity in capacitance of the varactors.

Figure 11 depicts the amplitude of VCO as a function of I_{bias} consisting of two operation modes; *current-* and *voltage-limited regimes*. In the current-limited regime, the tank amplitude linearly grows with the bias current until the oscillator enters the voltage-limited regime, in which the amplitude is limited to V_{CM}.



(a) Phase Noise versus Vcnt1



(b) Phase Noise versus Vcnt2

Fig. 12 Phase noise versus control voltages V_{cnt1} and V_{cnt2}.

3.2 Phase Noise

According to [9], the phase noise $\mathcal{L}\{f_{off}\}$ at offset frequency f_{off} is expressed as

$$\mathcal{L}\{f_{off}\} \propto \begin{cases} L^2/I_{bias}R_{Sind}^2 & (I-limited) \quad (19) \\ L^2 I_{bias}/V_{CM}^2 & (V-limited). \quad (20) \end{cases}$$

Figure 12 shows phase noise versus V_{cnt1} and V_{cnt2} measured with a VCO/PLL signal analyzer (Agilent 4352B). In Fig. 12(a), phase noise decreases with V_{cnt1} below 0.5 V and then levels off because for low V_{cnt1} the diode diffusion current reduces the current provided to M_p and M_n from I_{bias}, resulting in degradation of phase noise as expected from Eq. (19). Figure 12(b) shows that the increase of I_{bias} reduces phase noise in the current-limited regime while it induces the growth of phase noise in the voltage-limited regime and then saturate in high V_{cnt2} region as expected from Eqs. (19) and (20). This is an advantage of using SOI-MOSFET source follower as current source in Fig. 2. Figure 13 shows phase noise at V_{cnt1} of 1.5 V and V_{cnt2} of 1.3 V, which corresponds to the minimum phase noise condition in Fig. 12.

As measures of oscillator performance, D. Ham et al. defined two figures of merit [9], PFN and PFTN. One of them, *power-frequency-normalized* (PFN) is given by

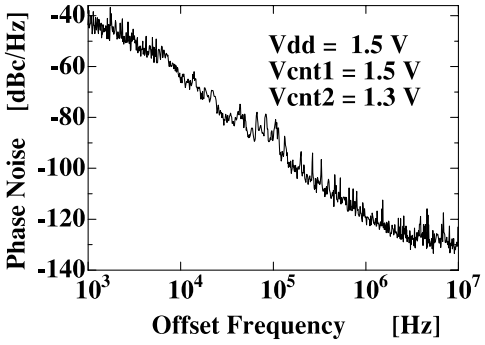


Fig. 13 Phase noise versus offset frequency.

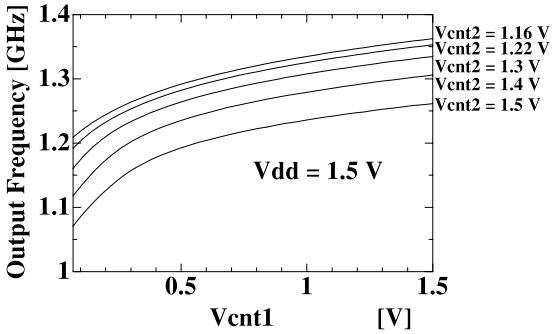


Fig. 14 Output frequency versus the main control voltage V_{cnt1} for different auxiliary control voltages V_{cnt2}, which exhibits the tuning range from 1.07 to 1.36 GHz.

$$PFN = 10\log\left[\frac{kT}{P_{sup}}\cdot\left(\frac{f_0}{f_{off}}\right)^2\right] - \mathcal{L}\{f_{0ff}\}, \quad (21)$$

where P_{sup} is the supplied power, f_0 is the oscillation frequency, $\mathcal{L}\{f_{off}\}$ is the phase noise in dBc/Hz at offset frequency f_{off}, T and k are absolute temperature and the Boltzman constant. The derived PFN of the fabricated VCO is around 0 dB, which is comparable to the reported values [2], [9], [14]–[32].

3.3 Tuning Range

Figure 14 shows the output frequency as a function of the main control voltage V_{cnt1} for different auxiliary control voltages, V_{cnt2}. V_{cnt1} is used as the main control voltage because of its small dependence of third-harmonic and phase noise, as described in Sects. 3.1 and 3.2. At $V_{cnt2} = 1.5$ V, the output frequency varies widely from 1.07 to 1.26 GHz. As seen in Fig. 14, the tuning range is almost constant (about 200 MHz) regardless of V_{cnt2}. The simultaneous use of V_{cnt1} and V_{cnt2} increases the effective tuning range from 1.07 to 1.36 GHz.

The second figure of merit *power-frequency-tuning-normalized* (PFTN) is given by

$$PFTN = 10\log\left[\frac{kT}{P_{sup}}\cdot\left(\frac{f_{tune}}{f_{off}}\right)^2\right] - \mathcal{L}\{f_{0ff}\}, \quad (22)$$

where $f_{tune} = f_{max} - f_{min}$. The derived PFTN of the fabricated VCO is −13 dB, which is also comparable to the reported data [2], [9], [14]–[32].

4. Conclusion

The double tuning technique in a low-voltage monolithic LC-tank SOI VCO is proposed. The VCO achieves a wide tuning range by using a double-tuning technique with lateral p-n junction varactors. The VCO was fabricated in the high-resistive substrate 0.2 μm fully-depleted SOI process technology. At the supply voltage of 1.5 V, the dissipation current of the VCO core is 4–8 mA, third-harmonic has small dependence on V_{cnt1} and below −37 dBc. The phase noise is −120 dBc/Hz at 1 MHz offset frequency, which is generally moderate for wireless communication in comparison with published VCOs [1]. The wide tuning range from 1.07 to 1.36 GHz is achieved by using the double-tuning technique. Two figures of merit, PFN and PFTN of the fabricated VCO are 0 dB and −13 dB, which are typical among recently reported results [2], [9], [14]–[32].

The fabricated LC-tank SOI-CMOS VCO using the double-tuning technique of the lateral p-n junction varactors has the following features: (1) wide tuning range, (2) low phase noise, (3) low harmonics and (4) low power consumption.

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