PAPER

A Wide Dynamic Range Variable Gain Amplifier with Enhanced IP1 dB and Temperature Compensation

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SUMMARY This paper presents the design consideration of a four-stage variable gain amplifier (VGA) with a wide dynamic range for receivers. The VGA uses parallel amplifiers for the first and second amplifiers in order to improve the input third-order intercept point (IIP3) in the low gain region. To investigate the behavior of the VGA, the gain and linearity analyses are newly derived for the parallel amplifiers, and are compared with the measured results. In addition, the principle of the temperature compensation is described. The gain control range of 110 dB, the IP1 dB of −11 dBm, and noise figure (NF) of 5.1 dB were measured using a 0.5 μm 26 GHz f_T BiCMOS process.

key words: *VGA, 1 dB compression point, noise figure, wireless, transceiver, IIP3*

1. Introduction

Variable gain amplifiers (VGAs) are indispensable building blocks for wireless transceivers in order to maximize the dynamic range of the overall systems. The VGAs for receivers are typically used in an automatic gain control loop in wireless systems, and adjust the received signal amplitude so as not to overflow the input dynamic range of A/D converters. For many wireless applications, such as Wideband Code Division Multiple Access (WCDMA), the receivers have to handle unpredictable receiver power which has an 80 to 100 dB range [1]–[3]. Therefore, the VGAs have to satisfy both high linearity at low gain and low noise at high gain. In addition, to achieve precise gain control and avoid signal phase discontinuity during gain settling, analog VGAs with monotonic gain control characteristics are preferred.

The basic concept of an analog VGA with linear-in-dB gain characteristics is introduced in Ref. [4]. A vast amount of the VGAs reported so far are based on this circuit topology. Figure 1 shows a conventional variable gain amplifier (Type 1) using a bipolar quad. The output current of the lower differential pair is controlled by current steering with the upper differential pair. The current transfer of the upper differential pair can be written as

$$\frac{I_{c1}}{I_e} = \frac{1}{1+\exp(-V_{cnt}/V_T)} \cong \exp(V_{cnt}/V_T)\,(-V_{cnt}/V_T \gg 1), \quad (1)$$

where V_T (=kT/q) is the thermal voltage, and V_{cnt}, I_{c1} and I_e are the control voltage to the upper differential pair, one side of the collector current of the upper differential pair, and the emitter current or the output current of the lower differential pair, respectively. As shown in Eq. (1), it is easy to make linear-in-dB characteristics using the bipolar quad, and it can cover 20 to 30 dB of gain variation. That is why this circuit topology is widely used.

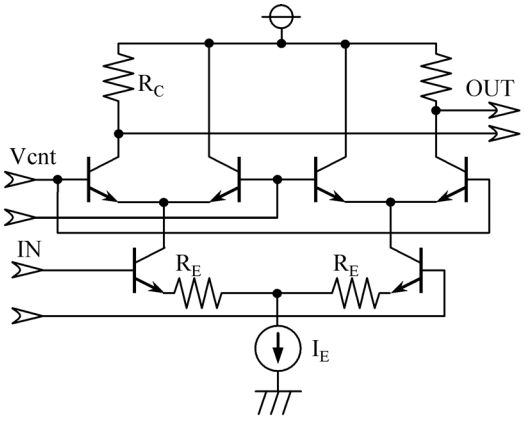

Fig. 1 Conventional VGA (type 1).

On the other hand, the conventional VGA can not avoid the substantial problem of noise and linearity tradeoff because input linearity, such as the input third-order intercept point (IIP3), and NF, are mainly defined and fixed by the emitter degeneration resistor R_E. Both a small NF for a small input signal and a high IIP3 for a large input signal are required for wireless applications.

One solution for this problem has been proposed in Ref. [3]. Since it did not show the design consideration for linearity, we will discuss an analysis of the gain and linearity of the VGA in detail in this paper. In addition, temperature compensation will be described.

In the following section, we introduce the wide dynamic range VGA with parallel amplifiers proposed in Ref. [3] again. Then the voltage gain and linearity of the VGA are discussed using simple circuit analysis. The principle of the temperature compensation is also described. In Sect. 3, the measurement results of the VGA and a comparison between the calculated and simulated results are presented. The conclusion is given in the final section.

Manuscript received December 8, 2010.
Manuscript revised April 1, 2011.

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DOI: 10.1587/transele.E94.C.1311

2. VGA Design

2.1 VGA Circuit

One effective solution to overcome the noise and linearity tradeoff problem mentioned in the introduction is to use two amplifiers, which have different characteristics to each other, in parallel. Figure 2 shows a simplified circuit of the parallel-amplifier VGA (Type 2). The VGA has two amplifiers, a high-gain amplifier (HGA) and a low-gain high-linear amplifier (HLA). The differential pair without an emitter degeneration resistor is the HGA, while the other pair is the HLA. The output currents of the HGA and the HLA are combined at load resistors R_C. The control voltage V_{cnt} for these amplifiers changes complementally. The gain of the HGA grows as the V_{cnt} rises, while the gain of the HLA becomes smaller. Although this circuit topology aims at a high IIP3 at low gain and low noise at high gain, the VGA has another problem. Since the HGA has a much larger gain than the HLA, the third-order distortion current generated by the HGA becomes dominant. Therefore, the total IIP3 of the VGA decreases suddenly when the total gain exceeds the minimum gain by even a little.

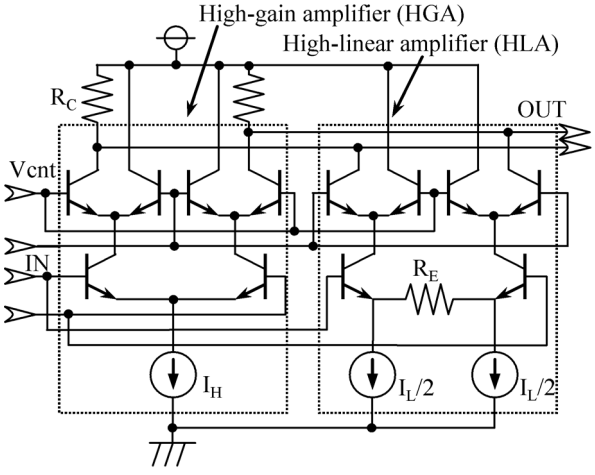

Fig. 2 Parallel-amplifier VGA (type 2).

Figure 3 shows the VGA proposed in Ref. [3] for the first and second stages. The HGA and HLA of the first stage (HGA1 and HLA1) are fully separated and paralleled, and have a common input and different outputs. Since HGA1 and HLA1 have their own load resistors (R_{C1H} and R_{C1L}), the gain and linearity of each amplifier can be designed and optimized independently. The gain control is done by the variable current sources I_{1H} and I_{1L} instead of the upper differential pair. The I_{1H} and I_{1L} are complementary, and generated by a differential amplifier, which will be described in Sect. 2.4. This configuration has the advantages of large voltage headroom, or high linearity, and small current consumption at low gain. The tail current of HGA1 is large for low noise, and is reduced at low gain. The second stage HGA and HLA (HGA2 and HLA2) follow HGA1 and HLA1, respectively. The second stage is a Type 2 VGA. The output currents of the HGA2 and the HLA2 are summed at the output load resistors R_{C2}.

Figure 4 shows a block diagram of the 4-stage VGA, where the first and second stages are Type 3 VGA. Conventional Type 1 VGAs are used for the third and fourth stages because the noise and linearity requirements are more relaxed at the input of the third stage. Note that the control voltage V_{cnt} for the high-gain path and the low-gain path is complementary to obtain high linearity at low gain. Each stage of the four stages is connected by capacitor coupling to avoid saturation of the amplifiers due to DC offset.

The advantages of this configuration are as follows.

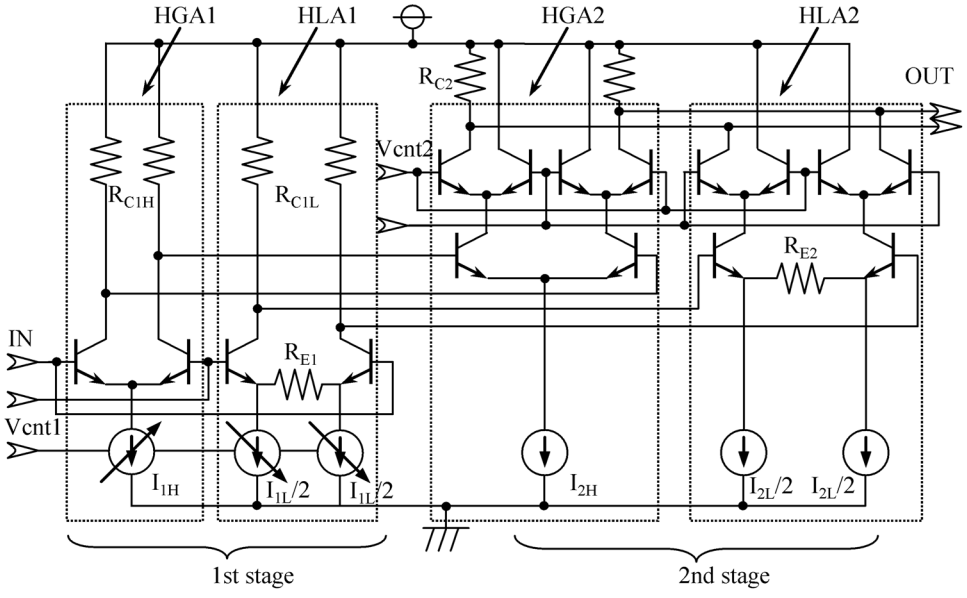

Fig. 3 Fully parallel-amplifier VGA (type 3).

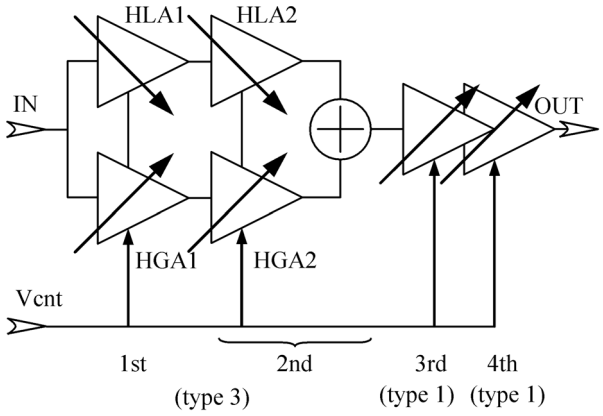

Fig. 4 Block diagram of the 4-stage VGA.

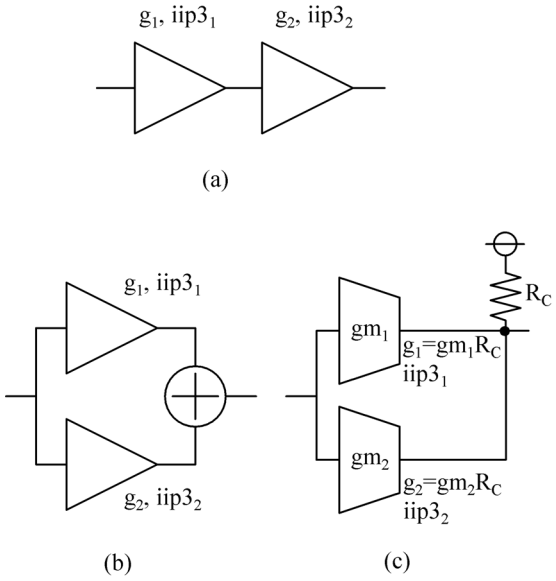

Fig. 5 (a) Cascaded amplifter, (b) parallel amplifter, (c) simplified circuit of the parallel amplifter.

First, the noise, linearity, and current consumption of the first stage can be optimized. Second, the distortion current of the HGA1 at low gain and the noise current of the HLA1 at high gain are suppressed at the second stage.

2.2 IIP3 of Parallel Amplifiers

The Type 3 VGA uses parallel amplifiers for the first and second stages, and thus the allotment of gain and linearity for the HGA and HLA has to be considered. To optimize the circuit parameters, we analyzed and calculated the gain and the IIP3 of the VGA.

The overall IIP3 of a cascaded amplifier, shown in Fig. 5(a), has been derived in Ref. [5].

$$\frac{1}{iip3_{Cas}^2} = \frac{1}{iip3_1^2} + \frac{g_1^2}{iip3_2^2} \tag{2}$$

$$iip3_{Cas} = \sqrt{\frac{1}{\frac{1}{iip3_1^2} + \frac{g_1^2}{iip3_2^2}}}, \tag{3}$$

where $iip3_{Cas}$, $iip3_1$, and $iip3_2$ are the IIP3 of the cascaded amplifier, the first stage, and the second stage in voltage domain, respectively, and g_1 and g_2 represent the voltage gains of the first and second stages, respectively.

On the other hand, there is no literature about the IIP3 of a parallel amplifier, as shown in Fig. 5(b). To derive the overall IIP3 of the parallel amplifier, consider two transconductors gm_1 and gm_2 connected in parallel and a common load resistor R_C, as shown in Fig. 5(c). In general, the IIP3 [dBm] is expressed as follows,

$$IIP3 = \frac{Pi + G - IM3}{2} + Pi, \tag{4}$$

where Pi [dBm] and G [dB] are the input power and power gain of the amplifier, respectively. Therefore, we have the third intermodulation IM3 [dBm]

$$IM3 = 3Pi + G - 2IIP3. \tag{5}$$

Considering the first amplifier has power gain G_1 [dB] and $IIP3_1$ [dBm], and the second one has G_2 [dB] and $IIP3_2$ [dBm], we have

$$IM3_1 = 3Pi + G_1 - 2IIP3_1 \tag{6}$$

and

$$IM3_2 = 3Pi + G_2 - 2IIP3_2. \tag{7}$$

The total $IM3$ [dBm] is obtained by the sum of both $IM3_1$ and $IM3_2$ in antilogarithms.

$$\begin{aligned} IM3_{tot} &= 10\log\left(10^{\frac{3Pi+G_1-2IIP3_1}{10}} + 10^{\frac{3Pi+G_2-2IIP3_2}{10}}\right). \\ &= 10\log\left(\frac{g_1^2}{iip3_1^4} + \frac{g_2^2}{iip3_2^4}\right) + 3Pi. \end{aligned} \tag{8}$$

The total power gain G_{tot} is

$$\begin{aligned} G_{tot} &= 20\log\{R_C\,(gm_1 + gm_2)\} \\ &= 10\log(g_1 + g_2)^2\,. \end{aligned} \tag{9}$$

Note that g_1, g_2, $iip3_1$, and $iip3_2$ are voltage quantities rather than power quantities.

The overall IIP3 of the parallel amplifier $IIP3_{para}$ is obtained by substituting Eqs. (8) and (9) for Eq. (4).

$$\begin{aligned} IIP3_{para} &= \frac{Pi + 10\log(g_1 + g_2)^2}{2} \\ &\quad - \frac{10\log\left(\frac{g_1^2}{iip3_1^4} + \frac{g_2^2}{iip3_2^4}\right) + 3Pi}{2} + Pi \\ &= 10\log\frac{g_1 + g_2}{\sqrt{\frac{g_1^2}{iip3_1^4} + \frac{g_2^2}{iip3_2^4}}} \end{aligned} \tag{10}$$

For the IIP3 in voltage domain, as shown in Eq. (3), we conclude that the overall IIP3 of the parallel amplifier is represented by

$$iip3_{para}^2 = \frac{g_1 + g_2}{\sqrt{\dfrac{g_1^2}{iip3_1^4} + \dfrac{g_2^2}{iip3_2^4}}}. \tag{11}$$

In general, the IIP3 of n parallel amplifiers is expressed as

$$iip3_{para}^2 = \frac{\sum_{i=1}^{n} g_i}{\sqrt{\sum_{i=1}^{n} \dfrac{g_i^2}{iip3_i{}^4}}}. \tag{12}$$

2.3 Analysis of VGA Gain and IIP3

The gain and the IIP3 of a bipolar differential amplifier with and without degeneration resistors shown in Figs. 6(a) and 6(b) have been discussed in Refs. [6]–[8]. To calculate the gain and the IIP3 of the VGA in Fig. 3, we modified the equations in these works for the differential amplifier with a common emitter-degeneration resistor shown in Fig. 6(c), and used the equations discussed in Sect. 2.2.

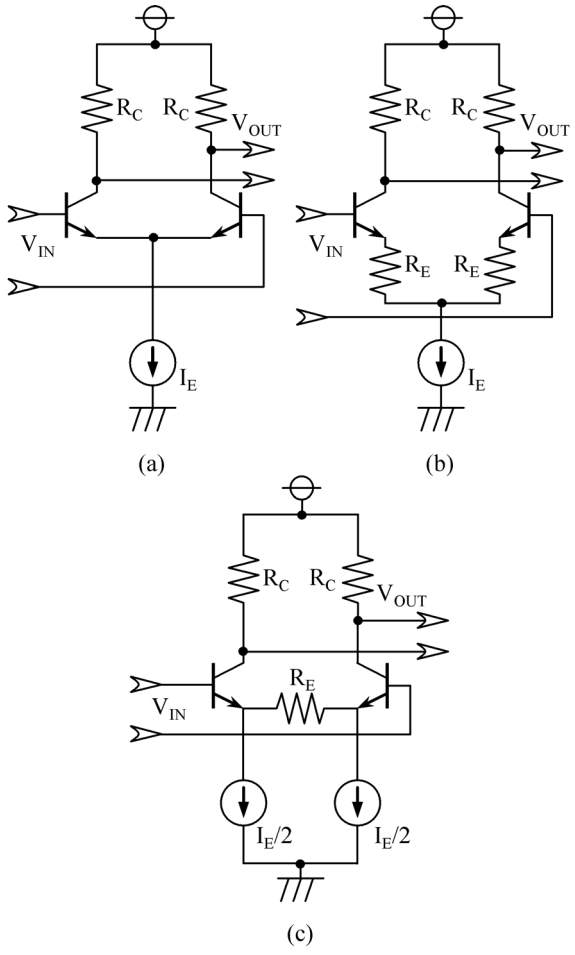

Fig. 6 (a) Simple differential amplifier, (b) emitter-degeneration differential amplifier, (c) simplified circuit of the parallel amplifier.

For the simple differential amplifier without the degeneration resistor, the HGA, the voltage gain and the IIP3 are given by

$$g_H = g_m R_C = \frac{I_E R_C}{2V_T} \tag{13}$$

$$iip3_H = 4V_T, \tag{14}$$

where I_E, R_C, and V_T are the tail current, the load resistor, and the thermal voltage, respectively. Note that iip3 is a zero-peak voltage. For the common emitter-degeneration differential amplifier shown in Fig. 6(c), the HLA, the gain and IIP3 are expressed as

$$g_L = g_m R_C = \frac{I_E R_C}{2V_T + \dfrac{I_E R_E}{2}} \tag{15}$$

$$iip3_L = 4V_T \left(1 + \frac{I_E R_E}{4V_T}\right)^{\frac{3}{2}}, \tag{16}$$

where R_E is the common emitter-degeneration resistor. The coefficients in Eqs. (15) and (16) are modified from the equations in Ref. [8].

Despite the fact that these formulas are available only for small input signals, they are effective in analyzing the VGA because the VGA operates in a linear region, and the IIP3 is defined at a small input signal.

The gain of the fully parallel-amplifier VGA (Type 3) is given by

$$\begin{aligned} g_{type3} &= g_{HGA1} g_{HGA2} + g_{HLA1} g_{HLA2} \\ &= \frac{I_{1H} R_{C1H}}{2V_T} \frac{I_{2H} R_{C2}}{2V_T} \frac{1}{1 + \exp(-V_{cnt2}/V_T)} \\ &\quad + \frac{I_{1L} R_{C1L}}{2V_T + \frac{I_{1L} R_{E1}}{2}} \frac{I_{2L} R_{C2}}{2V_T + \frac{I_{2L} R_{E2}}{2}} \frac{1}{1 + \exp(V_{cnt2}/V_T)}, \end{aligned} \tag{17}$$

where I_{1H}, I_{1L}, I_{2H}, and I_{2L} are the tail currents of the first and second stages, respectively, and I_{2H} and I_{2L} are constant currents. Here, I_{1H} and I_{1L} are variable currents expressed as

$$I_{1H} = \frac{I_{1H0}}{1 + \exp(-V_{cnt1}/V_T)} \tag{18}$$

$$I_{1L} = \frac{I_{1L0}}{1 + \exp(V_{cnt1}/V_T)}. \tag{19}$$

The control voltages V_{cnt1} and V_{cnt2} are converted from control voltage V_{cont} using a control voltage generator, which will be discussed in the following section.

The IIP3 of the Type 3 VGA can be obtained as follows. First, derive the IIP3 of the high gain path (HGP) which consists of HGA1 and HGA2, and of the high linear path (HLP) which is composed of HLA1 and HLA2. Then, calculate the total IIP3 using Eq. (11) because the Type 3 VGA is regarded as a parallel amplifier to HGP and HLP. The IIP3s of

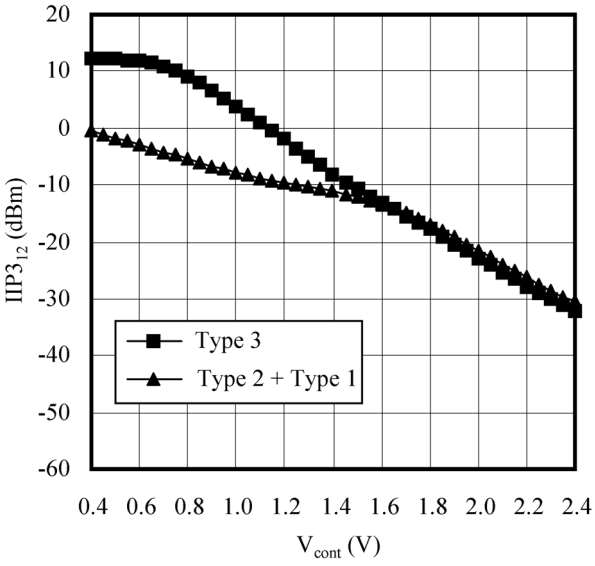

Fig. 7 IIP3 of the 1st-2nd stage versus Vcont.

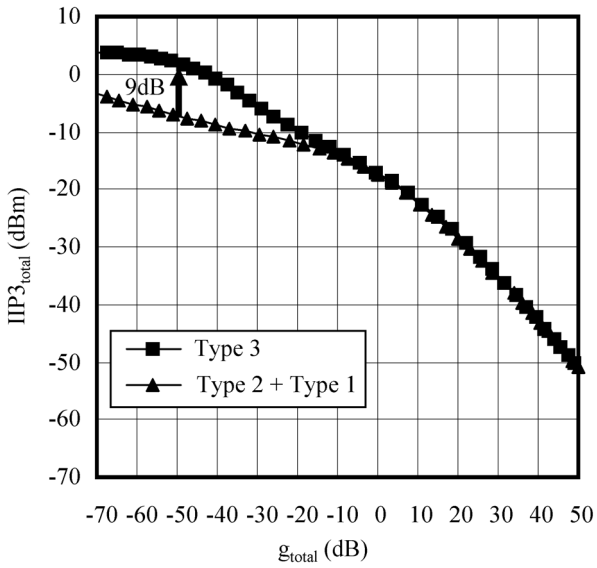

Fig. 8 Total IIP3 versus total gain of 4-stage VGA.

HGP and HLP are given by

$$iip3_{HGP} = \sqrt{\frac{1}{\frac{1}{iip3^2_{HGA1}} + \frac{g^2_{HGA1}}{iip3^2_{HGA2}}}} = \frac{4V_T}{\sqrt{1+\left(\frac{I_{1H}R_{C1H}}{2V_T}\right)^2}} \tag{20}$$

$$iip3_{HLP} = \sqrt{\frac{1}{\frac{1}{iip3^2_{HLA1}} + \frac{g^2_{HLA1}}{iip3^2_{HLA2}}}} = \frac{4V_T}{\sqrt{\frac{1}{\left(1+\frac{I_{1L}R_{E1}}{4V_T}\right)^3} + \frac{\left(\frac{I_{1L}R_{C1L}}{2V_T+\frac{I_{1L}R_{E1}}{2}}\right)^2}{\left(1+\frac{I_{2L}R_{E2}}{4V_T}\right)^3}}}. \tag{21}$$

Finally, the overall IIP3 of the Type 3 VGA is obtained by substituting Eqs. (20) and (21) for Eq. (11).

$$iip3^2_{type3} = \frac{g_{HGA1}g_{HGA2} + g_{HLA1}g_{HLA2}}{\sqrt{\frac{(g_{HGA1}g_{HGA2})^2}{iip3^4_{HGP}} + \frac{(g_{HLA1}g_{HLA2})^2}{iip3^4_{HLP}}}} \tag{22}$$

In the same way, we can calculate the total gain and the IIP3 of the four-stage VGA.

Figure 7 shows an example of the IIP3 comparison between the Type 3 VGA and a conventional VGA (Type 2 + Type 1) under the conditions that the gain variation range is 40 dB, and $iip3_{HGA1}$, and $iip3_{HLA1}$ are 0.104 V_{0-p} and 2.05 V_{0-p}, respectively. In spite of having the same IIP3 as the first stage of the Type 3 VGA, the total IIP3 of the conventional VGA is much lower than that of the Type 3 VGA at the low control voltage region. This is because the third-order distortion current generated by the HGA becomes dominant, as described in Sect. 2.1. Figure 8 shows a comparison of the total IIP3 for the 4-stage VGA. The Type 1 VGAs are used for the third and fourth stages. The total IIP3 of the Type 3 VGA is improved by 9 dB at the total gain of −50 dB. In the high gain region over −10 dB, both IIP3s show the same characteristics because the non-linearity of the high gain amplifiers becomes dominant. In this region, the degradation of the IIP3 does not have a harmful influence on the circuit because the input signal swing is much smaller than the IIP3.

2.4 Temperature Compensation

Since the transmission and the reception are done alternately in the Time Division Duplex (TDD), the calibration can be performed before the period of the switch of the transmission and the reception. On the other hand the communication is continuous in the Frequency Division Duplex (FDD). Therefore, a continuous temperature compensation is required to correspond to the temperature change during the communication. Figure 9 shows a control voltage generator to compensate for the temperature dependence of the VGA. First, with the V-I converter which is composed of a voltage follower and a resistor R_{VI}, the gain control voltage V_{cont} is converted to the current I_{VI} proportional to V_{cont}. The output current I_{VI} is expressed as

$$I_{VI} = k_{VI}\frac{V_{cont}}{R_{VI}} \tag{23}$$

where k_{VI} is a constant coefficient. Second, the current converter outputs the currents I_{cnt} and I_{cntb} in proportion to both T and V_{cont}. The I_{cnt} and I_{cntb} are connected to HLA2, HGA2, HGA3, and HGA4 through current mirror circuits, and make the control voltage V_{cnt} and V_{cnt2} in Figs. 1 and 3 with resistors R_{cnt} and R_{cnt2}, which are not shown in the figure. Finally, the current is converted as proportional to T times the exponential of TV_{cont} over V_T by the exponential converter. The output current I_{ecnt} and I_{ecntb} supply the

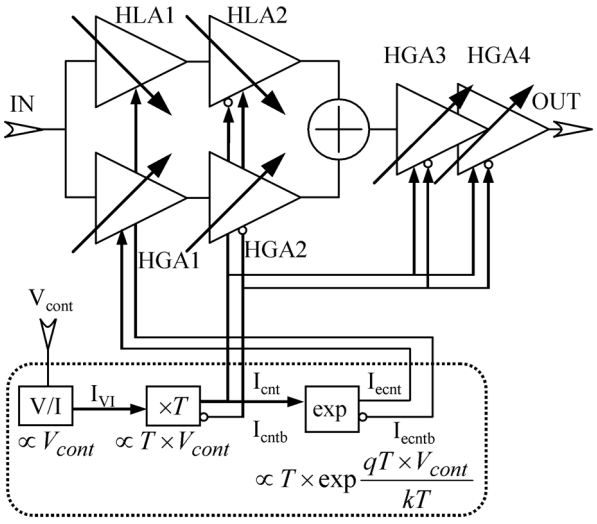

Fig. 9 Control voltage generator.

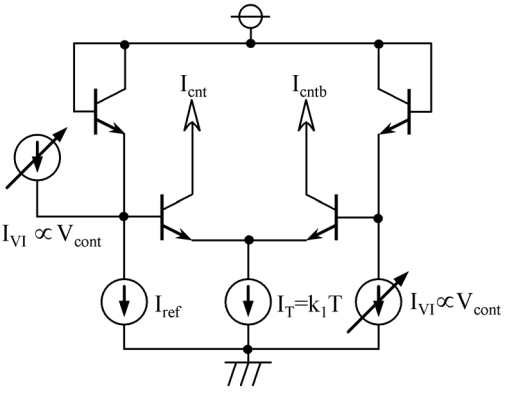

Fig. 10 Current converter to temperature proportional current.

tail current for HGA1 and HLA1 through current mirror circuits, respectively.

Figure 10 depicts a simplified circuit of the current converter based on a current multiplier [9]. The I_{cnt} and I_{cntb} are the output current, I_{VI} is the output current of the V-I converter, and I_{ref} is the constant current. The I_T is the tail current for the differential pair, and is in proportion to T. Both I_{ref} and I_T are made by a bandgap reference circuit, current mirrors, and resistors. The relations between each current are expressed in the following equations.

$$I_{cnt} : I_{cntb} = I_{VI} : \left(I_{ref} - I_{VI}\right) \tag{24}$$

$$I_{cntb} = I_T - I_{cnt}. \tag{25}$$

From Eqs. (24) and (25), one of the output current I_{cnt} is given by

$$I_{cnt} = \frac{I_T}{I_{ref}} I_{VI} = \frac{k_1 T}{I_{ref}} \frac{k_{VI} V_{cont}}{R_{VI}}, \tag{26}$$

where I_{ref} is constant, and I_T and I_{VI} are proportional to T and V_{cont}, respectively, and k_1 is a constant coefficient. Thus, I_{cnt} is proportional to both T and V_{cont}.

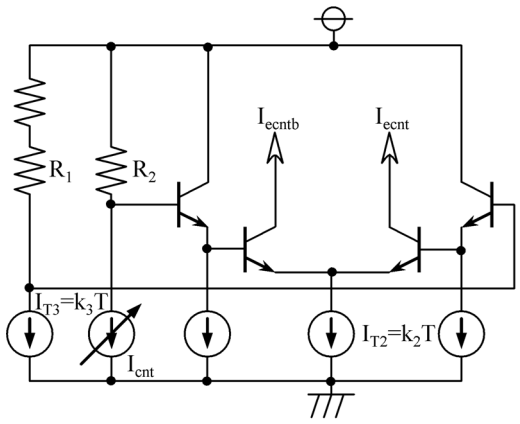

Fig. 11 Exponential converter.

The control voltage V_{cnt} and V_{cnt2} are given by

$$\begin{aligned} V_{cnt(cnt2)} &= R_{cnt(cnt2)} \left(I_{cnt} - I_{cntb}\right) \\ &= R_{cnt(cnt2)} \left(2I_{cnt} - I_T\right) \\ &= R_{cnt(cnt2)} k_1 T \left(\frac{2}{I_{ref}} \frac{k_{VI} V_{cont}}{R_{VI}} - 1\right) \end{aligned} \tag{27}$$

where R_{cnt} and R_{cnt2} are the resistors which define the control voltage. From Eq. (1), the current transfer is expressed as

$$\begin{aligned} \frac{I_{c1}}{I_e} &\cong \exp\left(\frac{R_{cnt\ (cnt2)} k_1 T \left(\frac{2}{I_{ref}} \frac{k_{VI} V_{cont}}{R_{VI}} - 1\right)}{V_T}\right) \\ &= \frac{\exp\left(R_{cnt\ (cnt2)} k_1 \frac{q}{k} \frac{2}{I_{ref}} \frac{k_{VI} V_{cont}}{R_{VI}}\right)}{\exp\left(R_{cnt(cnt2)} k_1 \frac{q}{k}\right)}. \end{aligned} \tag{28}$$

Equation (28) shows that the current transfer, or the gain of the second, third, and fourth, is proportional to $\exp(V_{cont})$ and has no temperature dependence.

Figure 11 shows a simplified circuit of the exponential converter, which consists of a differential pair with the tail current I_{T2} proportional to T. One of the output current I_{ecnt} is given by

$$\begin{aligned} I_{ecnt} &\cong I_{T2} \exp\left(\frac{I_{cnt} R_2 - I_{T3} R_1}{V_T}\right) \\ &= k_2 T \exp\left(\frac{k_{VI} k_1 R_2 q}{I_{ref} R_{VI} k} V_{cont} - \frac{k_3 R_1 q}{k}\right) \end{aligned} \tag{29}$$

where I_{T3} is bias current proportional to T, and k_2 and k_3 are constant coefficients for I_{T2} and I_{T3}, respectively. Equation (29) indicates that I_{ecnt} is proportional to T times the exponential of V_{cont}. The current I_{ecntb} is the difference between I_{T2} and I_{ecnt}.

The output current I_{ecnt} and I_{ecntb} are mirrored to the tail current of the first stage amplifiers I_{1H} and I_{1L} in Fig. 3, respectively. Using Eqs. (13) and (15), the gain of HGA1 and HLA1 is given by

$$g_{HGA1} = \frac{q I_{1H} R_{C1H}}{2kT} = a \frac{q k_2 R_{C1H}}{2k} \exp \frac{bq V_{cont}}{k}, \tag{30}$$

$$g_{HLA1} = \frac{I_{1L}R_{C1L}}{\frac{2kT}{q} + \frac{I_{1L}R_{E1}}{2}} = \frac{R_{C1L}}{\frac{2k}{cqk_2 \exp\left(-\frac{bqV_{cont}}{k}\right)} + \frac{R_{E1}}{2}} \quad (31)$$

where a, b, and c are constant coefficients which are design parameters. Since both g_{HGA1} and g_{HLA1} do not include the term T, a temperature independent gain is obtained.

In fact, each bias current, I_{ref}, I_T, I_{T2}, and I_{T3}, is determined by a resistor. Therefore, I_{ref}, k_1, k_2 and k_3 are proportional to the reciprocal of the resistor value which has temperature dependence. However, $R_{cnt(cnt2)}k_1$ and $I_{ref}R_{VI}$ in Eq. (28), k_2R_{C1H} in Eq. (30), and k_2R_{C1L} in Eq. (31) become constant because the temperature coefficient of each resistor is canceled.

3. Experimental Results and Comparisons

The VGA was fabricated using a 0.5 μm Bi-CMOS process that has 26 GHz f_T npn transistors, lateral pnp transistors, and CMOS transistors. A die photograph is shown in Fig. 12. The chip consists of a pair of 4-stage VGAs and a demodulator, PLLs, and a transmitter, which comprise an IFIC for WCDMA [3]. The chip occupies $4 \times 4\,\text{mm}^2$. To improve the noise and linearity performance, circuit parameters, such as degeneration resistors, decoupling capacitors for bias circuits and resistors of the control voltage generator, were slightly changed from those of Ref. [3].

Figure 13 shows the relation between the measured total voltage gain and the control voltage V_{cont} at 190 MHz input. The total voltage gain includes the VGA gain, the demodulator gain of 40 dB, and the 8 dB matching gain of an external matching circuit for measurement. A variable range of more than 110 dB (−28 to 83 dB) was obtained. The gain variation for temperature is shown in Fig. 14. The gain variation from −30° to 85°C was found to be within 1.7 dB, which means that temperature variation was less than 0.014 dB/°C over the entire dynamic range.

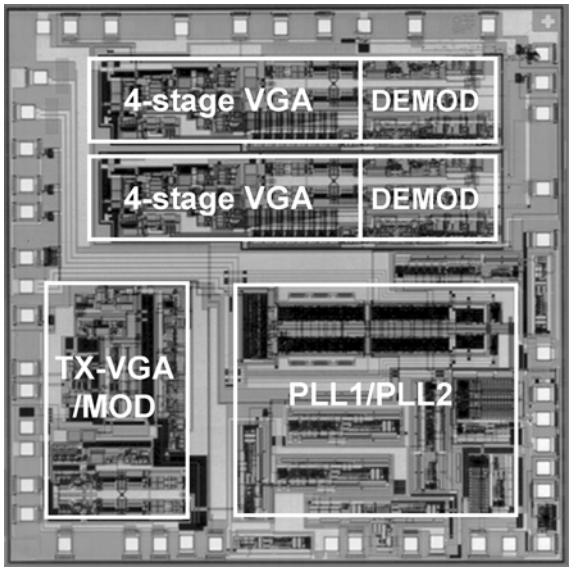

Fig. 12 Die photograph of the VGA.

The noise figure versus the voltage gain is shown in Fig. 15. The NF at 80 dB gain is 5.1 dB (5.3 dB in Ref. [3]) at room temperature. This varies ± 0.2 dB at −30°C and 85°C.

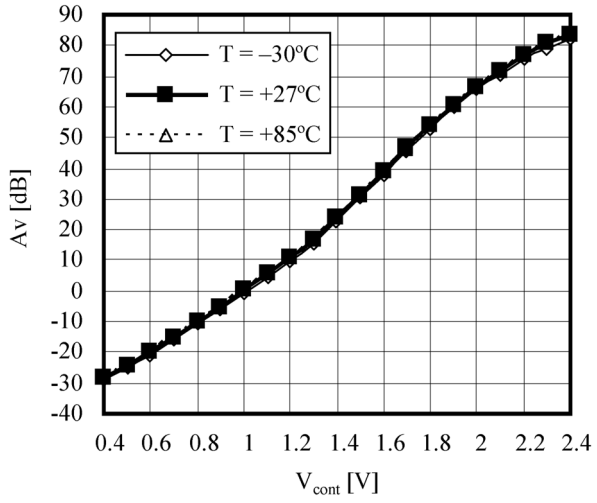

Fig. 13 Measured voltage gain versus control voltage (f = 190 MHz, Vcc = 3.0 V).

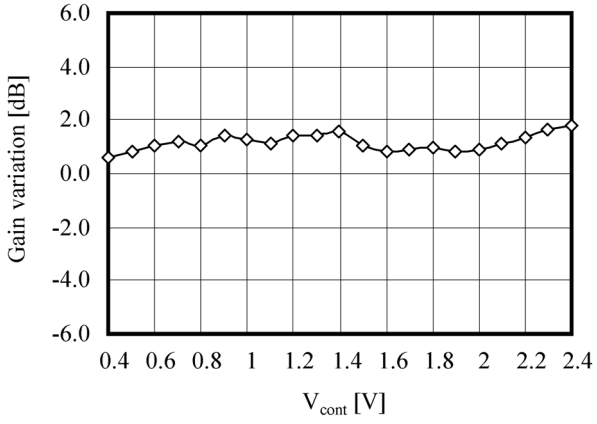

Fig. 14 Gain variation from −30°C to +80°C.

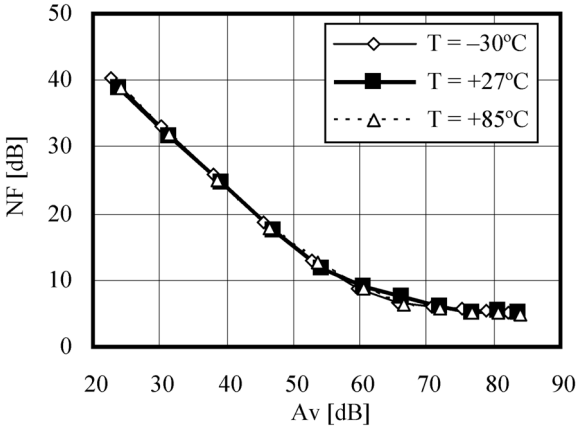

Fig. 15 Measured NF versus voltage gain (f = 190 MHz, Vcc = 3.0 V).

Table 1 Performance summary and comparison of VGAs.

	This work	2000[10]	2003[11]	2003[12]	2002[13]	2007[14]
Technology	0.5μm BiCMOS	BiCMOS	0.5μm BiCMOS	0.18μm CMOS	0.25μm CMOS	0.18μm CMOS
Frequency [MHz]	<600	<500	50	380	380	<900
Gain range [dB]	111	78	98	73	80	94
NF @Gmax [dB]	5.1	5	4.9	5	11	6.8
IP1dB [dBm]	-11	(IIP3 = -8)	-15	-18.6	-	-11
Current [mA]	4.4-6.6	12	13	6	25.3	11.4

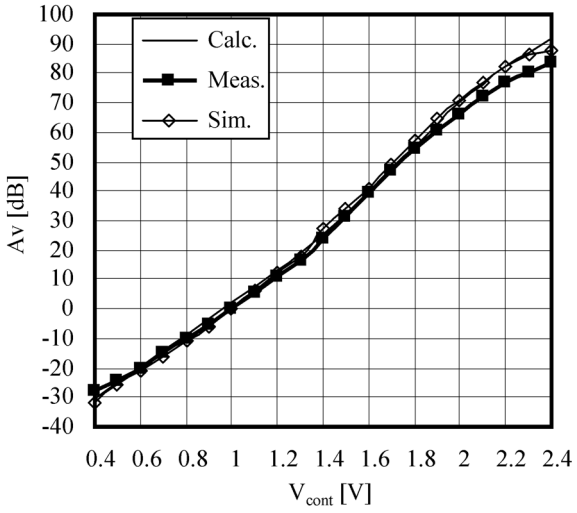

Fig. 16 Voltage gain versus control voltage (f = 190 MHz, Vcc = 3.0 V, T = 27°C).

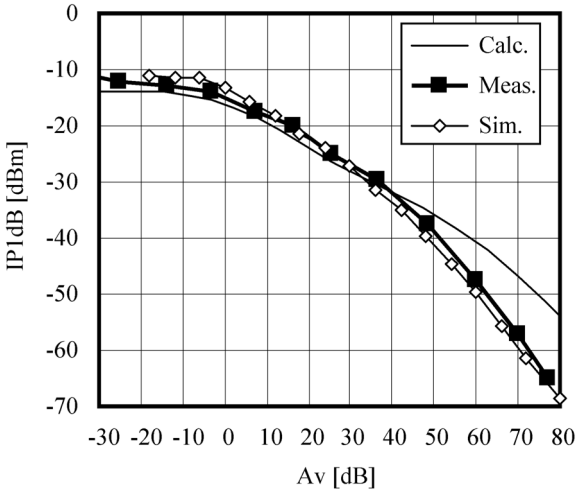

Fig. 17 Input P1 dB variation versus voltage gain (f = 190 MHz, Vcc = 3.0 V, T = 27°C).

To confirm the circuit analysis, calculations using the equations were compared with the measurement and circuit simulation results. Figure 16 shows the total voltage gain versus V_{cont} of calculation, measurement, and simulation. The demodulator gain of 40 dB and the matching gain of 8 dB are simply added to the calculation. Close agreement was found between the calculated, measured, and simulated results. Although the circuit analysis is simply a small signal DC analysis, it is effective in estimating the characteristics of the VGAs at an operating frequency below the 3 dB bandwidth of 600 MHz.

The same comparison for input 1 dB compression point IP1 dB versus voltage gain is shown in Fig. 17. The calculated IP1 dB is obtained by simply subtracting the matching gain of 8 dB and 9.6 dB from the calculated IIP3 [5]. The calculated result shows a good fit with the simulated and measured results. The difference between the calculated results and others at the high gain region of more than 50 dB is due to the non-linearity of the emitter followers of the fourth stage, which is not taken into account in the calculation. As mentioned in Sect. 2.3, the degradation of IP1 dB in this region does not have a harmful influence on the circuit. The circuit parameters, such as degeneration resistors and bias resistors of the control voltage generator, were redesigned using the linearity analysis and circuit simulation. The measured maximum input P1 dB was −11 dBm (−15 dBm in Ref. [3]) at minimum gain.

With a 3 V power supply, the current consumption of the VGA varies from 4.4 mA (minimum gain) to 6.6 mA (maximum gain) including the control voltage generator and bias circuits. Table 1 summarizes the measurement results of the VGA and comparison with previous studies.

4. Conclusions

A wide-dynamic-range four-stage VGA with temperature compensation and an analysis of the gain and linearity of the VGA have been presented. The VGA using parallel amplifiers for the first and second amplifiers achieves a low NF in the high gain region and a high linearity in the low gain region. The input P1 dB at minimum gain is improved by 9 dB compared with a conventional VGA. The VGA has a 111 dB gain control range with a maximum current of 6.6 mA. In addition, the analysis of gain and linearity using the newly derived IIP3 for parallel amplifiers shows close agreement with measured and simulated results.

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