Summary
A demodulator for short-range wireless interconnect using ASK/CDMA technique has been developed with 0.25 μm CMOS technology. The fabricated demodulator demonstrates the demodulation of 7.35 Mbps bit rate with 31 spread spectrum code length at 10 GHz carrier frequency.

Key words: CMOS, CDMA, ASK, wireless interconnect

1. Introduction

Traditional interconnect technique has been projected to be limited in their ability to meet the performance needs of high speed system LSIs at the future process technology nodes. This limitation is due to the global interconnect delay becoming significantly larger than the gate delay. To overcome this limitation revolutionarily, inter-chip and intra-chip wireless interconnection using integrated antenna at microwave frequency are being investigated [1], [2]. Although detail technological study of wireless interconnect in CMOS system LSIs is still in its infancy, wireless interconnect systems have some merits; (1) feasible integration onto CMOS system LSIs, especially compared with optical interconnections, and (2) significant reduction of wiring complexity. Although wireless interconnects can be used for both data and clock signals, wireless clock distribution is being evaluated now as a natural first step, because a modulation scheme for wireless data transmission is required [1].

This letter provides a modulation scheme for broadcast-type wireless data transmission using both Amplitude-Shift-Keying (ASK) modulation and Code-division-multiple-access (CDMA) technique, which can achieve both a modulator and a demodulator in small area. As we focus on the modulation/demodulation scheme, this letter demonstrates only a CMOS demodulator as its first prototype using 0.25 μm CMOS technology. The details on the modulator is mentioned in [3].

2. Principle of ASK/CDMA Technique

We applied the ASK modulation and CDMA technique for short-range wireless data communication; we named this topology “ASK/CDMA” technique. As the ASK modulation/demodulation can use simple circuitries, occupied area of these circuits is significantly small. The CDMA technique realizes high tolerance for noise and interferences and efficient frequency utilization in the multiple-access.

The principle of the ASK/CDMA technique is based on the properties of M-sequence used in the CDMA technique. The correlation of a bipolar ({−1, +1}) M-sequence with a unipolar ({+1, 0}) replica also produces an autocorrelation function [4]. In the ASK/CDMA technique, the unipolar sequence is used as the pseudonoise (PN) code in the transmitters, while the bipolar one is used in the receivers. To spread transmitting data D into the modulated data Ni, the positive data, D = 1, is modulated to the original PN code and the negative data, D = 0, is modulated to the inverted one. Therefore, Ni is given by

\[ N_i = \frac{1 + (-1)^{D-1}M_i}{2}, \]

where \( M_i \) is the bipolar M-sequence. The following ASK modulation stage generates carrier signal according to \( N_i \) which is the unipolar code.

In the demodulator, the received signal is despread using a bipolar M-sequence \( M_j \) as follows.

\[ (N_i, M_j) \approx \frac{(-1)^{D-1}L}{2} \delta_{i,j}, \]

where L is the codewidth of \( M_i \) and \( \delta_{i,j} \) is 1 (\( i = j \)) or 0 (\( i \neq j \)). Thus the sign of correlation between the received signal and the biloar code \( M_i \) accords with the original data D.

Based on the modulation/demodulation scheme, the ASK/CDMA transmitter can have simple circuitry, which is composed of an oscillator, an amplifier, a digital PN-code generator and MOS switches [3]. On the other hand, the receiver has to play some roles of RF amplitude detection and correlation with the bipoar PN-code. The following section will describe how to realize these functions using CMOS technology.

In this study, carrier frequency, PN-code rate and bit rate are 10 GHz, 250 Mcps (chip per second) and 7.35 Mbps, respectively. The used PN-code is composed of a M-sequence with 31-codelength and a reset signal with three-codelength. These specifications are suitable for its circuit implementation in 0.25 μm CMOS technology.
3. Demodulator Circuitry

To detect amplitude of the received signal, the non-linearity of the MOS switch is used. The non-linearity of NMOS devices in both weak inversion and strong inversion regions can be analyzed using the approximation formula of drain current $I_D$ given by [5]

$$I_D = I_0 \ln \left[ 1 + \frac{1}{2} \cdot 10^{\frac{V_{GS}-V_{th}}{S}} \right], \quad (3)$$

where $I_0$ is constant value depending on drain voltage, $V_{th}$ is threshold voltage and $S$ is subthreshold coefficient. Based on this equation, it turns out that the NMOS switch biased near $V_{GS} = V_{th}$ can detect amplitude of the received signal, as shown in Fig. 1. When an input signal is applied at the source of the MOS switch, the average of DC current is higher than that caused by input DC current. The difference between the average and bias currents corresponds to the received signal’s strength. The amplitude detector realized by a MOS switch is also performed for despreading simultaneously by applying $V_{GS}$ according to the PN-code.

Figure 2 shows the proposed demodulation circuit. The MOS switches of S1 and S2 detect the received signal and multiply it by the PN-code. To multiply the received signal by the bipolar PN-code ($[-1, +1]$), there are two signal paths. The received signal is multiplied by the unipolar replica ($S_i$) on one path, while by the inverted code of unipolar replica ($S_i$) on another path. The size of S1 and S2 must be designed considering both signal loss and charge injection. The MOS switches of S3 and S4 keep input terminal voltages of the following integrator when either S1 or S2 turns off.

To evaluate correlation between the received signal and the bipolar PN-code, the integrator is followed by the detector, in which the difference of signals multiplied by the unipolar replica and its inverted code must be integrated. In order to cancel input offset of the operational amplifier (OPA) in the integrator, the integrator performs offset canceling as well as resetting the accumulation capacitances (C1 and C2 in Fig. 2) in the reset period. The cancelling charges for the input offset can be stored on C3 and C4. During the reset period, the MOS switches of S1 and S2 are turned off, while S3 and S4 are turned on.

4. Experimental Results

The microphotograph of the fabricated ASK/CDMA demodulator test chip using 0.25 µm CMOS technology is shown in Fig. 3. The occupied areas of core circuits (a detector and an integrator) and PN-code generator are only 0.025 mm$^2$ and 0.035 mm$^2$, respectively. To keep correlation accuracy as described in [6], the OPA obtains the DC gain over 20 dB and the unity-gain-frequency over 40 MHz. The dissipation currents of core circuits and PN-code generator are 350 µA and 1mA, respectively, at 2.5 V supply voltage. This test chip does not contain clock data recovery (CDR), which is required in practical use. To synchronize the PN-code with the received signal, the external clock, CLK, and reset signal, RST, are used.

To test a demodulation circuit, ASK/CDMA modulated signal is generated using the high frequency mixer (Mini-Circuits ZMX-10G) and the BER tester (Agilent ParBERT 81250) as well as a signal generator.

Figures 4(a) and (b) show measurement results using correlated and uncorrelated PN-codes, respectively. As shown in Fig. 4(a), the integrator output waveform shows about 60 mV of positive and negative values according to transmitting data. On the other hand, as shown in Fig. 4(b), the integrator output changes only about 10 mV regardless received signal, which is due to the integration of the peri-

![Fig. 1](image1.png) Characteristics of $I_D-V_{GS}$ for NMOS device and concept of the detection.

![Fig. 2](image2.png) Schematic of demodulation circuit.

![Fig. 3](image3.png) Microphotograph of fabricated chip.
Fig. 4  Waveforms of integrator output: (a) using correlated code and (b) using uncorrelated code. Input power is $-12$ dBm and carrier frequency is 10 GHz.

Fig. 5  Measured power transfer characteristics of the demodulator at the carrier frequency of 5 and 10 GHz.

Fig. 6  Measured BER characteristics of the demodulator at the carrier frequency of 5 and 10 GHz.

odic errors by charge injection in the integrator. Since this error has always fixed value, the BER degradation is avoidable with adjustment of the judgment threshold of the following comparator (not implemented yet).

Figure 5 shows measured power transfer characteristics of the demodulator circuit. As a reference, the measured data at the carrier frequency of 5 GHz is also shown in this figure. The slope of about two demonstrates the square-law detection of the received signal amplitude shown in Fig. 1.

Figure 6 shows the measured BER characteristics. As a reference, the measured BER at the carrier frequency of 5 GHz is also shown in this figure. The BER for 5 GHz carrier frequency is better than that of 10 GHz, which corresponds to the amplitude detection efficiency shown in Fig. 5. To achieve an extremely low BER ($< 10^{-14}$ [7]), required input power of the demodulator is expected to be over $-15$ dBm at 10 GHz carrier frequency.

5. Conclusion

The CMOS demodulator in the ASK/CDMA short-range wireless interconnection has been developed for the first time. The MOS switch amplitude detector for despreading and the integrator with offset cancelling are used. The fabricated test chip demonstrates the demodulation of 7.35 Mbps bit rate with 31 PN-code length at 10 GHz carrier frequency. As this work is the first prototype, there is much room for improvement such as data rate and BER.

Acknowledgement

The chip design in this work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design System, Inc. Additionally, this work is also supported by the Japan Society for the Promotion of Science (JSPS) as part of the Research for the Future Program.

References