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PAPER Special Section on New System Paradigms for Integrated Electronics

High Speed and Noise Tolerant Parallel Bus Interface for VLSI Systems Using Multi Bit Code Division Multiple Access

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SUMMARY An efficient data transmission interface for VLSI systems, Multi-Bit Parallel Code Division Multiple Access (MB/P-CDMA) interface, has been designed with 0.35 μm CMOS technology. The proposed interface achieves 1.12 Gb/s data rate (80 MHz, 8 bit bus) using multi-bit transmission at each clock per transmitter. The proposed CDMA interface ensures higher speed operation than conventional interface even in noisy environments. Each of the transmitters and receivers occupies the die area of $290 \times 360\,\mu m^2$ and $240 \times 280\,\mu m^2$, respectively.

key words: *parallel-CDMA interface, noise tolerance, multi-bit transmission*

1. Introduction

The recent trend to high speed computing demands a high speed interface for VLSI systems. To meet such a requirement, Parallel Code Division Multiple Access (P-CDMA) interface was proposed for System LSIs [1]. The P-CDMA is characterized by short latency time (one clock cycle), which realizes high speed communication with a multiple access technique. At a given clock frequency, the higher data rate, however, requires the use of the more bus lines. To overcome the upper limit of the data rate of the P-CDMA interface without increasing the number of bus lines, we propose Multi-Bit Parallel-CDMA (MB/P-CDMA) for higher data rate transmission.

In this paper, we first explain the principle of MB/P-CDMA technique, and then circuit blocks of the MB/P-CDMA interface. In Sect. 4, we show the measurement data and then discuss the noise robustness of the proposed interface compared to the conventional interface.

2. Principle of Data Transmission

Figure 1 shows the data transmission concept of the MB/P-CDMA interface. At the k-th transmitter ($1 \leq k \leq n-1$) of the MB/P-CDMA interface, transmitted multi-bit data "$D(k)$," are encoded into multi-values "$D_{enc}(k)$" where n is the number of bus lines. The number of multi-values is 2^m where m is the number of bits per clock.

Bit data of the k-th transmitter multiplied by the l-th chip of pseudo noise-code (PN-code) "$SS_k(l)$" are output to l-th bus line ($1 \leq l \leq n$). For the MB/P-CDMA interface,

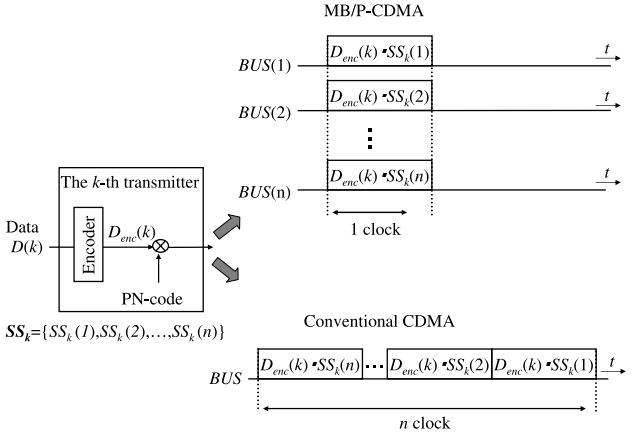

Fig. 1 Data transmission concepts of MB/P-CDMA and conventional CDMA.

the number of bus lines is the same as PN-code length. The signal of the l-th bus line "$BUS(l)$" is given by

$$BUS(l) = D_{enc}(k) \cdot SS_k(l). \tag{1}$$

The signals of the other bus lines are also generated in parallel fashion.

In the MB/P-CDMA interface, data are transferred in one clock by spreading transmitting data into the bus lines with PN-code, while the conventional CDMA interface (shown in Fig. 1) has latency because it spreads transmitting data over time span [2]–[7].

In addition, PN-codes used in this work are the M-sequence codes [8] consisting of "1" or "−1." All codes have "−1" at the end of sequence in such a way that correlation between different two PN-codes becomes zero. All transmitters have their own PN-code, so that maximum number of transmitters is limited to "$n-1$."

The use of CDMA technique in the MB/P-CDMA interface enables multiple access; all transmitters send data simultaneously to the bus lines where data are linearly added. Note that signal on each bus line is given by

$$BUS(l) = \sum_{k=1}^{n'} D_{enc}(k) \cdot SS_k(l). \tag{2}$$

where n' is the number of active transmitters. At a receiver, the received signals spread on the bus lines are multiplied by corresponding chips of the PN-code at a mixer. Then, the receiver accumulates all of the multiplied signals at an analog adder to find the correlation between the receiver and

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the transmitter to be connected. The correlation at the r-th receiver, $CORR(r)$, is given by

$$CORR(r) = \sum_{l=1}^{n} BUS(l) \cdot SS_r(l) \tag{3}$$

$$= \sum_{l=1}^{n} \sum_{k=1}^{n'} D_{enc}(k) \cdot SS_k(l) \cdot SS_r(l), \tag{4}$$

where $SS_r(l)$ is the l-th chip of PN-code used in the r-th receiver.

In what follows, 2-bit data transmission per clock at a transmitter is discussed as an example. In a transmitter, the 2-bit data "00," "01," "10" and "11" are converted into multi-values "$D_{enc}(k)$" $=-2, -1, 1, 2$, respectively.

$$CORR(r) = \begin{cases} 2\ (D(k) = \text{“11,”}\ SS(k) = SS(r)) \\ 1\ (D(k) = \text{“10,”}\ SS(k) = SS(r)) \\ 0\ (SS(k) \neq SS(r)), \\ -1\ (D(k) = \text{“01,”}\ SS(k) = SS(r)) \\ -2\ (D(k) = \text{“00,”}\ SS(k) = SS(r)), \end{cases} \tag{5}$$

because the PN-code used has the feature as follows

$$SS(x) \cdot SS(y) = \begin{cases} 1\ (SS(x) = SS(y)) \\ 0\ (SS(x) \neq SS(y)). \end{cases} \tag{6}$$

No correlation means that the bus carries no data multiplied by the PN-code used in the receiver. It is evident that from Eq. (5) the data received can be evaluated by the value of "$CORR(r)$." Thus, the data transmission rate of the MB/P-CDMA interface is doubled compared to the conventional P-CDMA for a given number of bus lines.

3. Circuit Implementation

This section describes the circuit blocks of the MB/P-CDMA interface designed. Figure 2 shows the block diagram of the MB/P-CDMA interface consisting of transmitters, receivers, a stabilizer and parallel-bus (8-bit). The parallel bus is composed of differential signal lines which ensures high common mode noise rejection. $D(k)$ is 2-bit data input to the k-th transmitter and $Enable(k)$ is the signal which activates the k-th transmitter. The k-th receiver outputs both $OUT(k)$ and $Valid(k)$. $Valid$ signal is activated when bus signals include the data modulated by the same PN-code which the k-th receiver uses.

3.1 Transmitter Circuit

Figure 3 depicts the transmitter circuit which consists of switch control circuit, capacitance coupling circuits and mixers.

The switch control circuit selects one of the voltage sources which drive capacitance C_{tr} depending on the input data, as shown in Fig. 4. The number of capacitors driven by V_{DD} is 4, 3, 1 and 0 depending on the input data such as "11," "10," "01" and "00" so that differential bus swing becomes $2\Delta V_c$, ΔV_c, $-\Delta V_c$ and $-2\Delta V_c$, respectively. The bus swing ΔV_c is given by

$$\Delta V_c = \frac{2C_{tr} \cdot (V_{DD} - V_{SS})}{C_{bus} + 4M_tC_{tr} + M_rC_{rec\_ls}}, \tag{7}$$

where C_{tr}, C_{rec_ls} and C_{bus} are capacitance of transmitter,

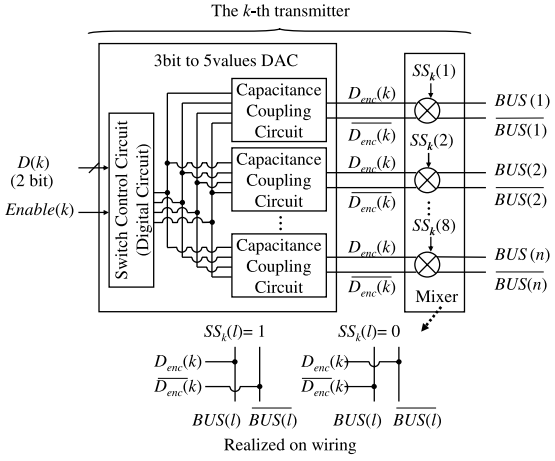

Fig. 3 Transmitter circuit.

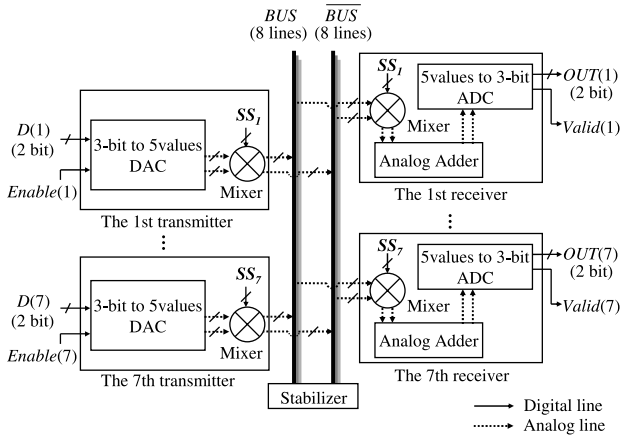

Fig. 2 Block diagram of MB/P-CDMA interface.

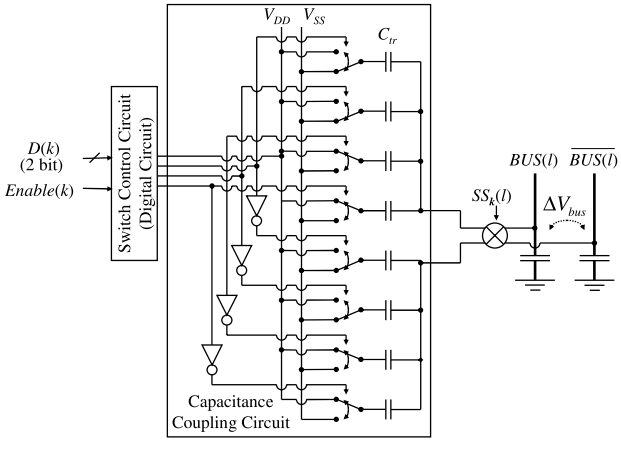

Fig. 4 Capacitance coupling circuit in a transmitter.

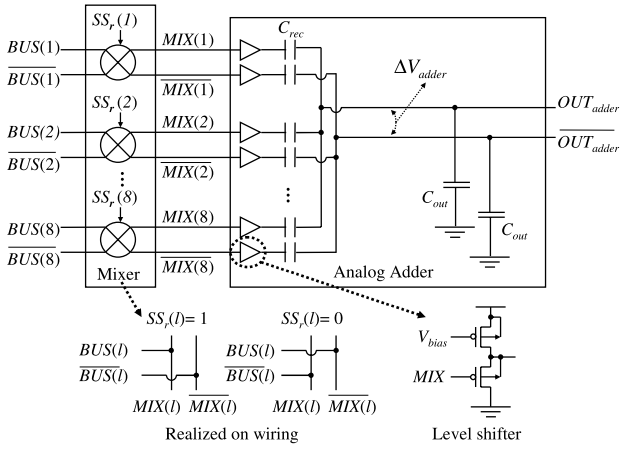

Fig. 5 Analog adder in a receiver.

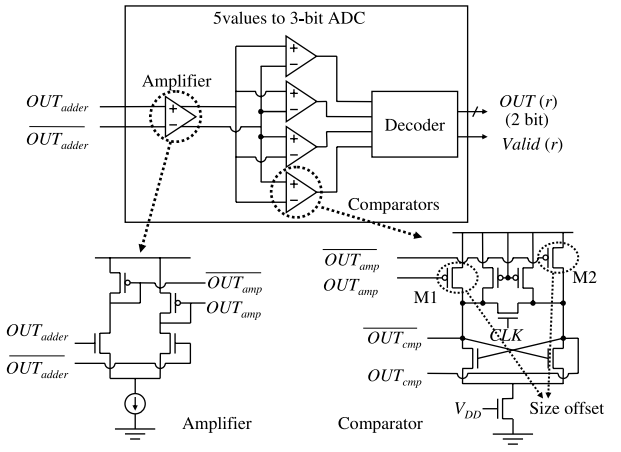

Fig. 6 3-bit AD converter in which 4 bit outputs from the comparators are converted into 2-bit data and a valid signal.

level shifter in a receiver (shown in Fig. 5) and the bus, respectively. M_t and M_r is the number of transmitters and receivers connected to the bus line.

The MB/P-CDMA transmitter drives the bus with capacitance coupling in such a way that the data from other transmitters are lineally added on the bus.

Data multiplied by a PN-code is realized by the following wiring technique. Suppose that the l-th chip of a PN-code used in the k-th transmitter is defined as $SS_k(l)$. When $SS_k(l)$ is "H," $BUS(l)$ and $\overline{BUS(l)}$ are connected to $D_{enc}(k)$ and $\overline{D_{enc}(k)}$, respectively as shown in Fig. 3. In the case of $SS_k(l)$ = "L," the connection is exchanged. This switching architecture reduces the number of logic gates and propagation delay time as well.

3.2 Receiver Circuit

As shown in Fig. 2, the receivers are composed of mixers, an analog adder, and an AD converter.

The mixer is realized by wiring similar to that used in the transmitter to reduce propagation delay. The demodulated signal will be then added by capacitance coupling in the analog adder shown in Fig. 5. The output of the analog adder OUT_{adder} is given by

$$\Delta OUT_{adder} = \frac{C_{rec} \sum_{l=1}^{n} BUS(l) \cdot SS_r(l)}{nC_{rec} + C_{out}}, \tag{8}$$

where C_{out} is parasitic capacitance of OUT_{adder}. Since the cross correlation between different PN-codes becomes zero, one of the five voltage levels is generated depending on transmitting bit data at the analog adder. OUT_{adder} and $\overline{OUT_{adder}}$ are then compared to the five reference voltage levels using the comparators in the 3-bit AD converter shown in Fig. 6. The four comparators with different input offsets induced by the different gate widths of M1 and M2 provide 4-bit output. In the decoder, the 4-bit output of comparators are converted into 2-bit data signals together with a valid signal.

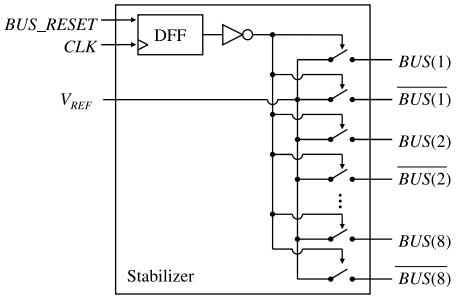

Fig. 7 Stabilizer circuit.

3.3 Stabilizer Circuit

As the bus is not biased at any specific voltage when interface is active, the initial bias of the bus must be set to avoid the drooping due to leakage current. The MB/P-CDMA interface resets the bus lines periodically as shown in Fig. 7.

4. Measurement Results

The 2-bit (four values) MB/P-CDMA interface had been designed using 0.35 μm triple-metal double-polysilicon CMOS technology. Figure 8 shows the microphotograph of the fabricated chip on which 8 bit differential parallel bus, 7 transmitters, 7 receivers and a stabilizer are integrated. Each die area occupied by a transmitter, receiver and stabilizer is $290\times360\,\mu m^2$, $240\times280\,\mu m^2$, and $60\times40\,\mu m^2$, respectively. In the transmitters and receivers, the area of capacitors dominates over those of other circuitry. Based on the occupation ratio of capacitors and other circuits, we find a transmitter's area S_t increases in proportional as

$$S_t \propto (n/8) \times 2^{m-1}, \tag{9}$$

and a receiver's S_r as

$$S_r \propto 0.9(n/8) + 0.05 \times 2^m, \tag{10}$$

where m and n are the number of multi bit and that of bus lines. At the same bus lines, 2-bit MB/P-CDMA shows higher throughput per area than any other-bit MB/P-CDMA (including the 1-bit P-CDMA) from Eqs. (9) and (10). Over 3-bit, the more the number of bit increases, the lower the throughput per area is. When the number of bus lines incleases, the throughput inclease in proportion to the area, approximately.

The chip measured demonstrated 1.12 Gb/s data transmission at 80 MHz clock frequency and 3.3 V supply voltage by using PN-code length of eight. The signal amplitude on a bus is only 80 mV per transmitted data. Figure 9 depicts input and output waveforms. In the measurement, we set *Enable*(7) ="*L*" disabling the 7-th transmitter so *Valid*(7) outputs "*L*," meaning no received data. Figure 9 demonstrates that the other transmitters and receivers established virtual direct interconnecions as expected.

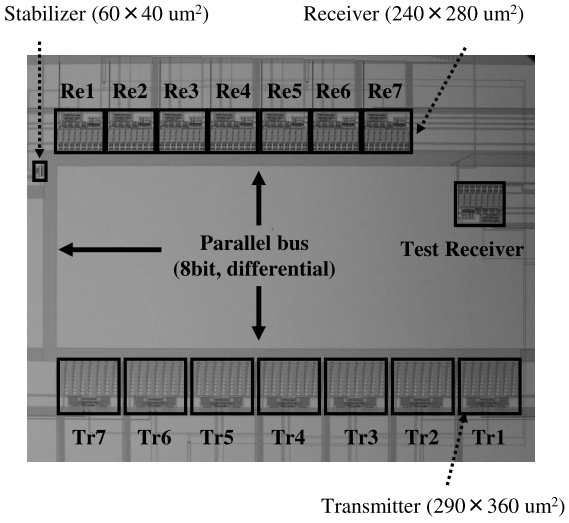

Fig. 8 Microphotograph of 2-bit MB/P-CDMA interface with 8 bit differential bus lines, 7 transmitters, 7 receivers and a stabilizer fabricated with 0.35 μm CMOS technology.

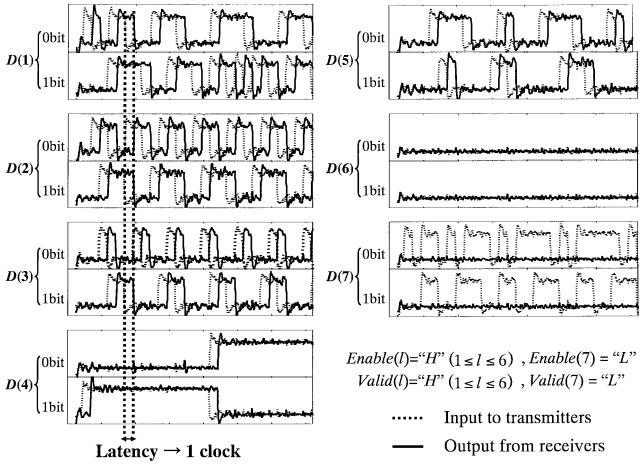

Fig. 9 Input and output signals measured.

5. Noise Tolerance and Power Consumption

In this section, the noise tolerance of the MB/P-CDMA is described.

The Bit Error Rate (BER) of the interface is strongly affected by coupling noise and clock frequency. The coupling noise from other digital lines to the bus degrades amplitude ratio of the signal to noise. Also the bus can not transfer the data if the colck frequency is much higher than the $1/\tau$ (τ: the time constant of the transmitter). The parameter mismatch of devices used in transmitters and receivers does not affect BER compared to the coupling noise and colck frequency. This is because capacitance missmatches are mere few percent and the input offset of the receiver is less than 10% of the signal amplitude.

Figure 10 shows the results of the numerical simulation. The data points demonstrate the ratio of ideal signal (τ is 0) to maximum noise imposed on a bus line vs. maximum clock frequency. The noise used in this simulation is assumed to be synchronized with the clock and normalized by the ideal signal level. The maximum frequency is defined as clock frequency at which data transmission error reaches to 0.1%. The number of the bus lines is 8. In this simulation, received OUT_{adder} data which differes more than 20% from their intended ideal values is defined as the transmission error. Time Division Multiple Access (TDMA) is considered as a conventional interface. Even in high noise environments, the MB/P-CDMA can operate faster than the conventional interface at a given BER.

2-bit MB/P-CDMA and 1-bit P-CDMA have same BER against S/N ratio, because the accuracy in device mismatch required by the ADC is the same for the same bus amplitude per bit data between 2-bit MB/P-CDMA and 1-bit P-CDMA. In this case, the 2-bit MB/P-CDMA has twice power consumption compared with 1-bit P-CDMA, because the amplitude on the bus lines and the number of comparators in the ADC are double. More than 3-bit MB/P-CDMA has lower throughput per energy.

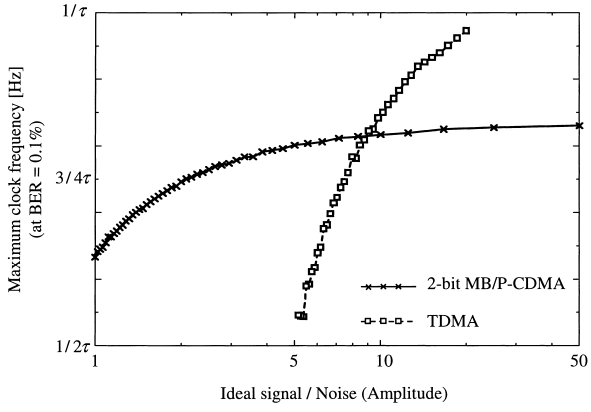

Fig. 10 Simulation results on noise tolerance of 2-bit MB/P-CDMA compared to conventional TDMA interface in low S/N (large noise) environments.

6. Conclusions

A new parallel bus interface using both P-CDMA and multi-value transferring technique has been proposed. Since the MB/P-CDMA interface can send multi-valued data from transmitters to receivers in one clock, high speed data transmission can be realized with the same bus lines as P-CDMA. The measurement results of the 2-bit MB/P-CDMA (8 bit bus lines) interface fabricated with 0.35 μm CMOS technology demonstrate 1.12 Gb/s data transmission at 80 MHz. Simulation results show noise robustness even in noisy environments. The MB/P-CDMA interface is one of the best efficient interfaces for System LSIs using future advanced CMOS process which would suffer from the coupling noise between metal lines.

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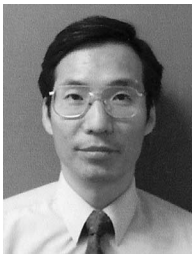

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