LETTER *Special Section on Analog Circuit and Device Technologies*

Threshold Voltage Mismatch of FD-SOI MOSFETs

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SUMMARY The threshold voltage mismatch of FD (Fully depleted) SOI (Silicon on insulator) devices have been studied. Floating body MOSFETs operating at high drain voltage show a large mismatch in the threshold voltage compared with body-tied MOSFETs. Those experimental data under different drain voltages indicate that both floating body effect and DIBL (Drain induced barrier lowering) are involved in the threshold voltage mismatch of floating body MOSFETs.

key words: *threshold voltage, FD-SOI, floating body effect, DIBL*

1. Introduction

In the analog circuit applications of FD-SOI devices, their matching characteristics are quite important issue to be clarified before actual circuit design. It is well established that the threshold voltage (V_t) mismatch of bulk MOSFETs is mainly dominated by a statistical variation of channel dopant number. However, in the case of FD-SOI devices, there would be another factor causing large V_t mismatch. In FD-SOI devices operating at high drain voltages, the generated holes by the impact ionization are accumulated in the body, which would cause statistical V_t fluctuation depending on the device structures. The aims of this paper are to investigate V_t fluctuation of FD-SOI MOSFETs operating at high drain voltages because this phenomenon has not been well studied yet in view of matching characteristics for analog circuits and to clarify the physical mechanisms behind the fluctuation.

2. Measurement

For this study, we measured the standard deviation of V_t on 0.2 μm FD-SOI CMOS technology. We use the n-channel MOSFET array structure [1], [2] to place a large number of MOSFETs in small area where gradual variations of oxide thickness and channel dopant density are negligible. This structure has 50 × 255 MOSFETs in the area of 2 mm × 4 mm, which includes 25 different gate sizes for each of two structures, floating-body and body tied with H-shaped gate, so that the mismatch of electrical properties among 255 MOSFETs can be statistically measured. The Kelvin technique is used to supply precise biases to each device whose electrical characteristics are automatically measured with an analog tester, Agilent 94000.

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3. Experimental Results and Discussions

Figure 1 shows the standard deviation of V_t ($\sigma(V_t)$) of 50 types of MOSFETs measured at V_{DS} =0.1 V and V_{DS} =1.0 V, as a function of the gate area. At V_{DS} =0.1 V, the slope of about −0.5 in the log-log plot indicates that the $\sigma(V_t)$ is inversely proportional to the square root of the gate area, meaning that the V_t mismatch originates from the statistical variation of the channel dopant number. This behavior is much the same as the bulk devices reported in Refs. [1]–[3]. However, at V_{DS} =1.0 V, the $\sigma(V_t)$ of the floating-body devices increases significantly, while that of the body-tied devices keeps their behavior unchanged. Because of their unique feature, we focus on only the floating-body devices in the following discussions.

The increase of the $\sigma(V_t)$ shown in Fig. 1 has nothing to do with the gate area at V_{DS} =1.0 V. However, the $\sigma(V_t)$ strongly depends on V_{DS} as shown in Fig. 2, where the $\sigma(V_t)$ of MOSFETs with three different channel lengths of 0.5, 0.7

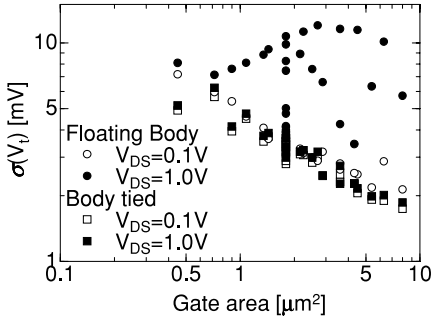

Fig. 1 $\sigma(V_t)$ of 25 types of FD-SOI MOSFETs with floating-body and body-tied as a function of gate area measured at either V_{DS} =0.1 V or 1.0 V.

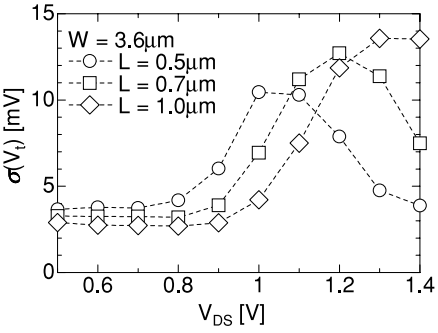

Fig. 2 $\sigma(V_t)$ of FD-SOI MOSFETs with W=3.6 μm, L=0.5, 0.7, 1.0 μm, as a function of V_{DS}.

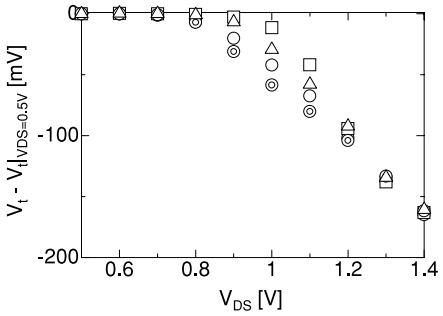

Fig. 3 Variations of V_t due to the floating body effect in four MOSFETs with a same gate size (W/L=3.6 μm/0.5 μm).

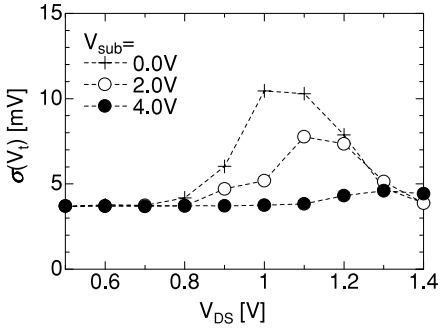

Fig. 4 Influence of the base substrate voltage (V_{sub}) on the $\sigma(V_t)$ in FD-SOI MOSFETs with W/L=3.6 μm/0.5 μm.

and 1.0 micron are plotted as a function of V_{DS}. There are two physical phenomena involved in the V_{DS} dependence of V_t mismatch; floating body effect and Drain-Induced-Barrier-Lowering (DIBL).

In FD-SOI devices operating at high drain voltage, holes generated by impact ionization are accumulated near the bottom of the body, which induces floating body effect. The amount of resulting V_t drop varies depending on the devices, which has strong sample dependence as shown in Fig. 3. Figure 2 indicates that long channel devices needs higher V_{DS} to cause impact ionization.

Figure 4 shows the $\sigma(V_t)$ as a function of drain voltage for different V_{sub}, a positive voltage bias applied to the Si substrate under the buried oxide to avoid the accumulation of generated holes near the bottom of the body. The decrease of maximum $\sigma(V_t)$ reveals the role of the floating body effect involved in the statistical fluctuation of V_t.

DIBL is another factor for the increase of $\sigma(V_t)$. In an FD-SOI MOSFET operating at high V_{DS}, the potential barrier at the body/source junction near the bottom of the body decreases with V_{DS}. This effect is enhanced for FD-SOI devices compared with partially depleted (PD) SOI devices because the potential barrier has been decreased by the gate voltage. As a result, holes generated by impact ionization flow to the source, which reduces floating body effect [4]. In DIBL regime, the $\sigma(V_t)$ is also suppressed for short channel devices at high V_{DS}, as shown in Figs. 2 and 5.

Note that the $\sigma(V_t)$ of the MOSFETs with minimum channel length of 0.2 μm has no V_{DS} dependence as shown in Fig. 5. This can be explained by enhanced DIBL. For

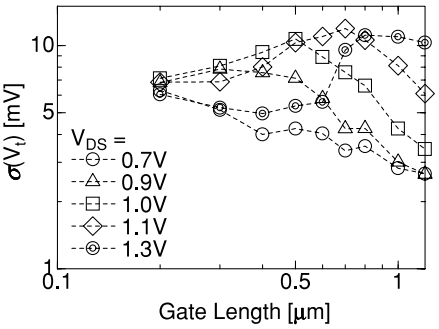

Fig. 5 $\sigma(V_t)$ of FD-SOI MOSFETs with gate width of 3.6 μm as a function of gate length for different drain voltages.

short channel devices, DIBL occurs even at lower drain voltage than the threshold voltage for impact ionization, resulting in no floating body effect.

4. Conclusion

We have investigated the V_t mismatch of FD-SOI MOSFETs. The fundamental behavior of the V_t mismatch is much the same as the bulk devices; the standard deviation of V_t is inversely proportional to the square root of the gate area. However, the V_t mismatch of the MOSFETs increases with high drain voltage because the floating body effect induces excess V_t variation. This effect is attributed to the holes accumulated in the body. Also the DIBL suppresses the increase of V_t mismatch because it decreases the body/source potential barrier accumulating holes in the body. For short channel devices where DIBL occurs at lower drain voltage, there is no noticeable excess V_t mismatch.

These behaviors are observed only in the floating-body devices and can be avoided by using the body-tied structure.

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