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# Analytical Expression Based Design of a Low-Voltage FD-SOI CMOS Low-Noise Amplifier

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**SUMMARY** We propose a design methodology of a low-voltage CMOS low-noise amplifier (LNA) consisting of a common-source and a common-gate stages. We first derive equations of power gain, noise figure (NF) and input third-order intercept point ($IIP_3$) of the two-stage LNA. A design methodology of the LNA is presented by using graphs based on analytical equations. A 1-V 5.4-GHz LNA was implemented in 0.15-$\mu$m fully-depleted silicon-on-insulator (FD-SOI) CMOS technology. Measurement results show a power gain of 23 dB, NF of 1.7 dB and $IIP_3$ of −6.1 dBm with a power consumption of 8.3 mW. These measured results are consistent with calculated results, which ensures the validity of the derived equations and the proposed design methodology.
***key words:*** *low-noise amplifier (LNA), FD-SOI CMOS, noise, linearity, low-voltage*

## 1. Introduction

Recently, the supply voltage of integrated circuits has been reduced because of MOSFET miniaturization and the increasing demand for low power consumption. It is, however, difficult to realize a radio-frequency (RF) circuit with desired performance at low supply voltage. Promising solutions are two-folds; to develop circuit topologies suitable for low supply voltage and to design circuits in a new process such as the silicon-on-insulator (SOI) process [1], [2].

The first building block of a wireless receiver is the low-noise amplifier (LNA) which amplifies small signals received by an antenna. It has to keep the internal noise as low as possible and to have sufficient high power gain. LNA also requires good linearity to reduce distortion [3], [4]. Considering both low noise and high linearity, it is difficult to design a cascode LNA [5], [6] operating below 1-V supply voltage, although the design methodology of a 2.5-V cascode LNA [7] has been reported.

We investigate the structure of a low-voltage LNA and proposes a new design methodology of the LNA taking power gain, noise and linearity into account. We implement a 1-V 5.4-GHz LNA in 0.15-$\mu$m fully-depleted SOI (FD-SOI) CMOS technology and verify both its performance and our design methodology.

This paper is organized as follows. Section 2 describes the circuit topology of a low-voltage LNA. Section 3 shows the small-signal equivalent circuit of the LNA and Sect. 4 derives equations of power gain, noise figure (NF) and input third-order intercept point ($IIP_3$) of the LNA. Section 5 presents the design methodology. Section 6 shows the measurement results of the fabricated LNA.

## 2. Two-Stage LNA

Figure 1 shows a conventional cascode LNA with inductive source degeneration [5], [6] which is widely used as a CMOS LNA. The overdrive voltage of the transistor $M_i$ is expressed as

$$V_{odi} = V_{gsi} - V_{thi} \tag{1}$$

where $V_{gsi}$ and $V_{thi}$ are the gate-source voltage and threshold voltage of $M_i$, respectively. It is difficult to use this cascode LNA at low supply voltage because the supply voltage must exceed two overdrive voltages, $V_{od1} + V_{od2}$.

In this study, we adopt a two-stage LNA consisting of a common-source and a common-gate stages [8] as shown in Fig. 2. The ac-coupling capacitor $C_c$ is placed between the input and output stages. The two internal LC tanks $L_1/C_1$ and $L_2/C_2$ are chosen to resonate at the operation frequency. The transistor $M_2$ improves reverse isolation and reduces the Miller effect. The minimum supply voltage of the LNA is only $V_{od1}$, so that the LNA operates at lower supply voltage than the conventional cascode LNA.

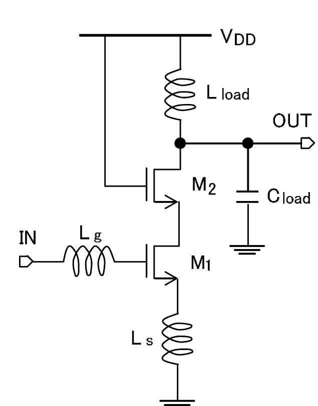


**Fig. 1** Schematic of conventional cascode LNA.

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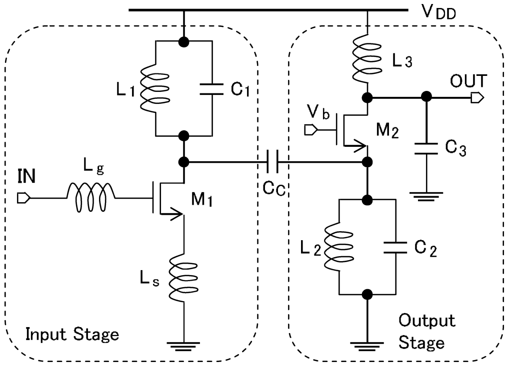


**Fig. 2** Schematic of two-stage LNA studied.

## 3. Small-Signal Equivalent Circuit of the LNA

Figure 3 shows the input stage of the two-stage LNA, where $v_s$ and $R_s$ are a signal source voltage and signal source impedance, respectively. For more precise derivations than those reported in [7], we take account of a parasitic capacitance $C_p$ originating from both the input pad capacitance and gate-drain capacitance of $M_1$, $C_{gd1}$ [4]. $R_{eq} + j\omega_0 L_{eq}$ denotes the equivalent source impedance looking into the left hand side of the reference plane 2, which is given by

$$R_{eq} = \frac{R_s}{\omega_0^2 C_p^2 R_s^2 + (1 - \omega_0^2 C_p L_g)^2}, \tag{2}$$

$$L_{eq} = \frac{L_g - C_p(\omega_0^2 L_g^2 + R_s^2)}{\omega_0^2 C_p^2 R_s^2 + (1 - \omega_0^2 C_p L_g)^2}. \tag{3}$$

Figure 4 shows the small-signal equivalent circuit of the input stage with the equivalent signal source impedance. Note that an SOI MOSFET has no body effect in the equivalent circuit. The equivalent signal source voltage $v_{s,eq}$ is given by

$$v_{s,eq} = \frac{v_s}{1 - \omega_0^2 C_p L_g + j\omega_0 C_p R_s}. \tag{4}$$

The effective gate-source capacitance of $M_1$, $C_{gs1,eff}$, effective inductance, $L_{s,eff}$, and non-quasi-static (NQS) resistance, $r_{nqs,eff}$, are expressed as follows [4]:

$$C_{gs1,eff} = (1 + M\alpha_{gd})C_{gs1}, \tag{5}$$

$$L_{s,eff} = \frac{L_s}{1 + M\alpha_{gd}}, \tag{6}$$

$$r_{nqs,eff} = \frac{r_{nqs}}{1 + M\alpha_{gd}}, \tag{7}$$

$$M = g_{m1} \times \left(\frac{1}{g_{m2}} // R_I\right) = \frac{g_{m1} R_I}{1 + g_{m2} R_I}, \tag{8}$$

$$\alpha_{gd} = \frac{C_{gd}}{C_{gs}} \tag{9}$$

where $g_{mi}$ is the transconductance of $M_i$, $M$ the Miller factor and $R_I$ the parallel resistance of $R_{L_1,p}$ and $R_{L_2,p}$. $R_{L_i,p}$ is the equivalent resistance of the internal and load LC tanks consisting $L_i$ and $C_i$ ($i$ =1, 2, 3) at a resonant frequency, which is given by

$$R_{L_i,p} \simeq \frac{\omega_0^2 L_i^2}{R_{L_i,s}} \tag{10}$$

where $R_{L_i,s}$ is the series resistance of $L_i$. From Eqs. (5)–(9), the real and imaginary parts of the input impedance looking into the right hand side of the reference plane 2 are given by

$$R_{in} = r_{nqs,eff} + \omega_{T1} L_{s,eff}, \tag{11}$$

$$X_{in} = \omega_0 L_{s,eff} - \frac{1}{\omega_0 C_{gs1,eff}} \tag{12}$$

where $\omega_{Ti} = g_{mi}/C_{gsi}$. $R'_{in}$ denotes the input impedance of the LNA looking into the right hand side of the reference plane 1, which is given by

$$R'_{in} = \frac{R_{in}(1-\omega_0^2 L_g C_p) + j(\omega_0 L_g + X_{in} - \omega_0^2 L_g C_p X_{in})}{1 - \omega_0 C_p X_{in} + j\omega_0 C_p R_{in}}. \tag{13}$$

From Fig. 4, the impedance matching condition is given by

$$R'_{in} = R_s \tag{14}$$

or

$$R_{eq} = R_{in}, \tag{15}$$

$$\omega_0 L_{eq} = -X_{in}. \tag{16}$$

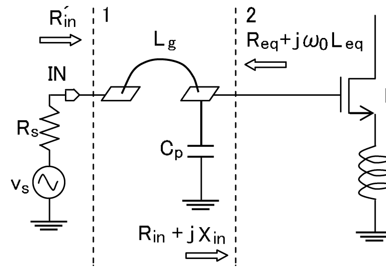


**Fig. 3** Input stage of LNA.

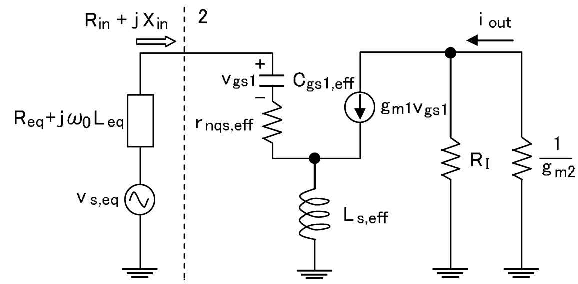


**Fig. 4** Small-signal equivalent circuit of input stage.

## 4. Power Gain, NF and IIP$_3$ of Two-Stage LNA

For our design optimization, we derive expressions of power gain, NF and IIP$_3$ of the two-stage LNA.

### 4.1 Power Gain

The output power of the LNA is given by the output load $R_{L_3,p}$ and the current injected in the load $i_{out}$ as

$$P_{out} = |i_{out}|^2 R_{L_3,p} \tag{17}$$

where $R_{L_3,p}$ is given by Eq. (10). Based on the equivalent circuit shown in Fig. 4, $|i_{out}|^2$ is given by

$$|i_{out}|^2 = \frac{4P_{av}R_{eq}}{(R_{eq}+R_{in})^2}\left(\frac{\omega_{T1}}{\omega_0}\right)^2\left(\frac{R_I}{R_I+1/g_{m2}}\right)^2 \tag{18}$$

where $P_{av}$ is the available power of the source.

$$P_{av} = \frac{|v_{s,eq}|^2}{4R_{eq}} = \frac{|v_s|^2}{4R_s}. \tag{19}$$

From Eqs. (17)–(19), the power gain of the two-stage LNA is derived as

$$G_t = \frac{4R_{eq}R_{L_3,p}}{(R_{eq}+R_{in})^2}\left(\frac{\omega_{T1}}{\omega_0}\right)^2\left(\frac{R_I}{R_I+1/g_{m2}}\right)^2. \tag{20}$$

### 4.2 NF

Figure 5 shows the noise equivalent circuit of input stage of the LNA. The noise voltage, $v_{ns,eq}$, the drain noise and the induced-gate noise currents, $i_{ndi}$ and $i_{ngi}$, of $M_i$ ($i$ = 1, 2) are expressed as

$$\overline{|v_{ns,eq}|^2} = 4k_BTR_{eq}\Delta f, \tag{21}$$

$$\overline{|i_{ndi}|^2} = 4k_BT\frac{\gamma_i}{\alpha_i}g_{mi}\Delta f, \tag{22}$$

$$\overline{|i_{ngi}|^2} = 4k_BT\delta_i\frac{(\omega C_{gsi})^2}{\kappa_i g_{d0i}}\Delta f \tag{23}$$

where $\alpha_i = g_{mi}/g_{d0i}$ and $g_{d0i}$ is the zero-bias drain conductance of $M_i$, $\gamma_i$, $\delta_i$ and $\kappa_i$ are the noise parameters of $M_i$ [5], [6].

The output noise shown in Fig. 5 is calculated from Eq. (21) as

$$\overline{|i_{o,s,eq}|^2} = \frac{4k_BTR_{eq}\omega_{T1}^2\Delta f}{\omega_0^2(1+\alpha_{gd}M)^2(R_{eq}+R_{in})^2(1+1/g_{m2}R_I)^2}. \tag{24}$$

From Eqs. (22) and (23), the equation of the output noise due to $M_1$ shown in Fig. 5 is derived as

$$\overline{|i_{o,M_1}|^2} = \frac{4k_BT\gamma_1\chi_1 g_{m1}(R_{eq}+r_{nqs,eff})^2\Delta f}{\alpha_1(R_{eq}+R_{in})^2(1+1/g_{m2}R_I)^2}, \tag{25}$$

$$\chi_1 = 1-\frac{2|c|\alpha_1R_{eq}}{(1+\alpha_{gd}M)(R_{eq}+r_{nqs,eff})}\sqrt{\frac{\delta_1}{\kappa_1\gamma_1}} + \frac{\delta_1\alpha_1^2}{\kappa_1\gamma_1}\frac{R_{eq}^2+1/\omega_0^2C_{gs1,eff}^2}{(1+\alpha_{gd}M)^2(R_{eq}+r_{nqs,eff})^2} \tag{26}$$

where $c \simeq j0.395$ is the correlation coefficient between the induced-gate and drain noise currents [5], [6]. The detailed derivations are summarized in the Appendix.

Figure 6 shows the noise equivalent circuit of the common-gate stage of the LNA. The noise current $i_{nR_{L_i}}$ originating from the internal or load LC tank is given by

$$\overline{|i_{nR_{L_i}}|^2} = \frac{4k_BT\Delta f}{R_{L_i,p}}. \tag{27}$$

The detailed derivations of the output noise due to $M_2$ are also summarized in the Appendix. The output noise originating from $M_2$ is given by

$$\overline{|i_{o,M_2}|^2} = 4k_BT\frac{\gamma_2}{\alpha_2}\chi_2 g_{m2}\Delta f, \tag{28}$$

$$\chi_2 = \frac{1}{(1+g_{m2}R_I)^2} + \frac{1}{(1+1/g_{m2}R_I)^2}\left(\frac{\omega_0}{\omega_{T2}}\right)^2\frac{\alpha_2^2\delta_2}{\kappa_2\gamma_2}. \tag{29}$$

The output noises due to the internal and load LC tanks shown in Fig. 6 are derived from Eq. (27) as

$$\overline{|i_{o,R_I}|^2} = \frac{4k_BT\Delta f}{(1+1/g_{m2}R_I)^2R_I}, \tag{30}$$

$$\overline{|i_{o,R_{L_3}}|^2} = \overline{|i_{nR_{L_3}}|^2} = \frac{4k_BT\Delta f}{R_{L_3,p}}. \tag{31}$$

Therefore, NF of the two-stage LNA results in

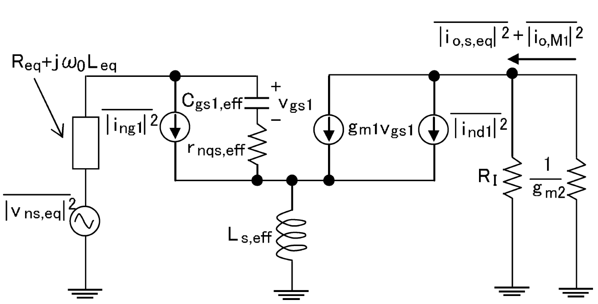


**Fig. 5** Noise equivalent circuit of input stage.

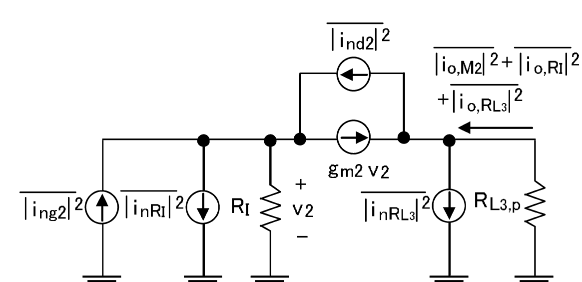


**Fig. 6** Noise quivalent circuit of common-gate stage.

$$NF = \frac{\overline{|i_{o,s,eq}|^2} + \overline{|i_{o,M_1}|^2} + \overline{|i_{o,M_2}|^2} + \overline{|i_{o,R_I}|^2} + \overline{|i_{o,R_{L_3}}|^2}}{\overline{|i_{o,s,eq}|^2}}$$
$$= 1 + \frac{\gamma_1 \chi_1}{\alpha_1}\left(\frac{\omega_0}{\omega_{T1}}\right)^2 \frac{g_{m1}(1+\alpha_{gd}M)^2(R_{eq}+r_{nqs,eff})^2}{R_{eq}}$$
$$+\left(\frac{\omega_0}{\omega_{T1}}\right)^2 \frac{(1+\alpha_{gd}M)^2(R_{eq}+R_{in})^2}{R_{eq}}\left(1+\frac{1}{g_{m2}R_I}\right)^2$$
$$\times\left[\frac{\gamma_2\chi_2 g_{m2}}{\alpha_2} + \frac{1}{(1+1/g_{m2}R_I)^2 R_I} + \frac{1}{R_{L_{3,p}}}\right]. \tag{32}$$

## 4.3 IIP$_3$

The output of a non-linear small-signal amplifier $y(t)$ is approximately expressed as

$$y(t) \approx a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \tag{33}$$

where $x(t)$ is an input signal. The IIP$_3$ of the amplifier in the expression of voltage amplitude is given by [9]

$$A_{IIP_3} = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|}. \tag{34}$$

IIP$_3$ usually expressed as the available power of signal source is given by

$$IIP_3 = \frac{A_{IIP_3}^2}{8R_s}. \tag{35}$$

The overall $A_{IIP_3}^2$ of the LNA consisting of the input and the output stages (Fig. 2) is given by [9]

$$\frac{1}{A_{LNA,IIP_3}^2} \simeq \frac{1}{A_{1,IIP_3}^2} + \frac{A_{v1}^2}{A_{2,IIP_3}^2} \tag{36}$$

where $A_{1,IIP_3}$ and $A_{2,IIP_3}$ represent the IIP$_3$ of the input and output stages in the expression of voltage amplitude, respectively. $A_{v1}$ is the voltage gain of the input stage, which is given by

$$A_{v1} = \left|\frac{g_{m1}\left(\frac{1}{g_{m2}}//R_I\right)}{j\omega_0 C_{gs1,eff}(R_{eq}+R_{in})(1-\omega_0^2 C_p L_g + j\omega_0 C_p R_s)}\right|. \tag{37}$$

The drain current of MOSFET at each stage is expressed as [10]

$$I_{di} = \frac{1}{2}\mu_0 C_{ox}\frac{W_i}{L}\frac{V_{odi}^2}{1+\Theta V_{odi}}\frac{1}{1-\lambda V_{dsi}} \tag{38}$$

where $W_i$ and $L$ are the gate width and length of $M_i$, $\lambda$ is the channel-length modulation coefficient, $\Theta = \mu_0/(2v_{sat}L) + \theta$, $v_{sat}$ the saturation velocity of the carrier, $\mu_0$ the carrier mobility under low electric field and $\theta$ the mobility reduction parameter. From Eq. (38), for a signal $v_s(t)$ applied to the LNA, the output current of each stage is derived as

$$I_{di}(t) = \frac{c_0(c_1 + c' v_i(t))^2}{c_2 + c_3 v_i(t) + c'^2 c_4 v_i^2(t)} \quad (i = 1,\ 2), \tag{39}$$
$$c' = \frac{1}{j\omega_0 C_{gs1,eff}(R_{eq}+R_{in})} \times \frac{1}{1-\omega_0^2 L_g C_p + j\omega_0 C_p R_s} \quad (i = 1), \tag{40}$$
$$-1 \quad (i = 2), \tag{41}$$
$$c_0 = \frac{1}{2}\mu_0 C_{ox}\frac{W_i}{L}, \tag{42}$$
$$c_1 = V_{odi}, \tag{43}$$
$$c_2 = (1 + \Theta V_{odi})(1 - \lambda V_{dsi}), \tag{44}$$
$$c_3 = (1 + \Theta V_{odi})\lambda A_{vi} + c'(1 - \lambda V_{dsi})\Theta, \tag{45}$$
$$c_4 = \Theta\lambda A_{vi} \tag{46}$$

where $v_1(t) = v_s(t)$ and $v_2(t) = -A_{v1}v_s(t)$. In the derivation of Eqs. (39)–(46), the channel-length modulation in $M_1$ due to the variation of the source voltage is neglected. Substituting Taylor expansion coefficients of Eq. (39), $a_1$ and $a_3$, into Eq. (34), $A_{IIP_3}^2$ of each stage can be derived as

$$A_{i,IIP_3}^2 = \frac{4}{3}\left|\frac{c_1 c_2^2(c_1 c_3 - 2c' c_2)}{(-c' c_2 + c_1 c_3)[(-c' c_2 + c_1 c_3)c_3 - 2c' c_1 c_2 c_4]}\right|. \tag{47}$$

The overall IIP$_3$ of the LNA can be given by Eqs. (35), (36) and (47).

# 5. Design of the Two-Stage LNA

The transconductance of $M_i$ is a derivative of Eq. (38), which is given by

$$g_{mi} = \frac{1}{2}\mu_0 C_{ox}\frac{W_i}{L}\frac{V_{odi}(2+\Theta V_{odi})}{(1+\Theta V_{odi})^2}\frac{1}{1-\lambda V_{dsi}}. \tag{48}$$

The power gain, NF and IIP$_3$ are expressed as a function of $V_{odi}$ by using Eq. (48) and the equations derived in the previous section. In what follows, we discuss a design methodology of the two-stage LNA with those parameters. In NF calculation, the noise paprameter, $\gamma_i$ and $\delta_i$ of a 1-V LNA in 0.15-$\mu$m FD-SOI CMOS technology based on the experimental results [11] are used.

The specifications of LNA are shown in Table 1. These are typical specifications for the LNA of a wireless local area network (WLAN) receiver.

(1) Gate lengths of $M_1$ and $M_2$

The gate length chosen is the minimum length of 0.14 $\mu$m because NF decreases with scaling the gate length [5], [6].

(2) Input impedance

The input impedance of LNA, $R'_{in}$, is designed to be lower than $R_s$ in such a way that both the power gain and NF improve [4]. For simplicity, $R'_{in}$ is set to $R_s$.

(3) Bias currents of $M_1$ and $M_2$

**Table 1** Specifications of LNA.

| | |
|---|---|
| Operation frequency | 5.4 GHz |
| $S_{11}$ | $< -10$ dB |
| Power Gain | $> 20$ dB |
| NF | $< 2.0$ dB |
| Current Consumption | 8.0 mA |
| Supply Voltage | 1.0 V |

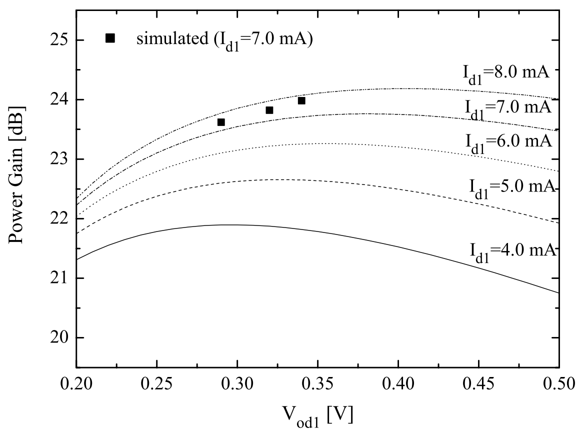


**Fig. 7** Calculated and simulated power gain versus $V_{od1}$.

Equation (20) shows that the common-gate stage has a small influence on the overall power gain. Therefore, the bais current of $M_1$, $I_{d1}$, is chosen to satisfy the power gain specification.

Figure 7 shows the calculated power gain versus $V_{od1}$ as a parameter of $I_{d1}$. Note that $g_{m2}$ is set to infinity in Eq. (20). For comparison, simulated results ($I_{d1} = 7.0$ mA) are also plotted in the figure. This and the following simulations of the LNA are carried out using the small-signal and noise FD-SOI MOS device model [11]. The calculated results are comparable to the simulated ones. The given specification is satisfied in the range of 4.0–8.0 mA. Taking account of process and temperature variations, we choose $I_{d1}$ to be 7.0 mA for a power gain of 23 dB including a 3 dB margin and $I_{d2} = 1.0$ mA from the power specification.

(4) Overdrive of $M_1$

For NF and IIP3 of the input stage, $\overline{|i_{o,M_2}|^2}$ and $g_{m2}$ are set to 0 and infinity in Eq. (32), respectively, and $A^2_{2,IIP_3}$ to infinity in Eq. (36). Figure 8 shows the calculated and simulated NF and IIP$_3$ versus $V_{od1}$ at $I_{d1} = 7.0$ mA. Again, the calculated results are comparable to the simulated ones.

From the figure, the increase of $V_{od1}$ results in better noise performance of the LNA, but poor linearity. The degradation of linearity can be explained as follows: Under the impedance matching condition, the constant current $i_{in} = v_s/2R_s$ injects in the LNA. The small-signal voltage of gate-source of $M_1$ is given by

$$v_{gs1} \simeq \frac{i_{in}}{j\omega_0 C_{gs1}}. \tag{49}$$

The gate-source capacitance of $M_1$, $C_{gs1}$, decreases with increasing $V_{od1}$ under constant $I_{d1}$, resulting in the increase of $v_{gs1}$. Although the MOSFET generally has higher linearity with increasing $V_{od1}$, in the range of 0.20–0.50 V, the degradation of linearity due to the increase in $v_{gs1}$ becomes significant, causing poor linearity. Therefore, a smaller $V_{od1}$ results in an LNA with higher linearity. Taking account of an additional noise of the output stage, we choose $V_{od1} = 0.32$ V, resulting in $W_1 = 120\,\mu$m.

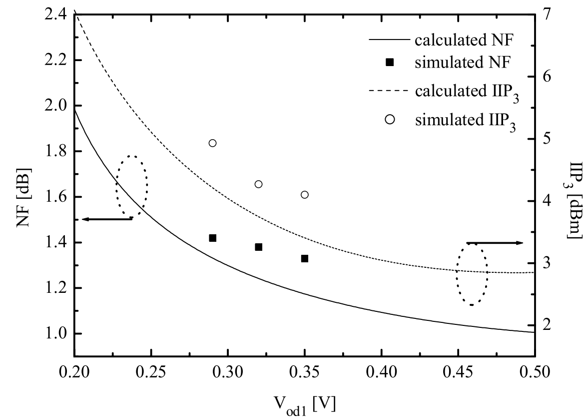


**Fig. 8** Calculated and simulated NF and IIP$_3$ versus $V_{od1}$.

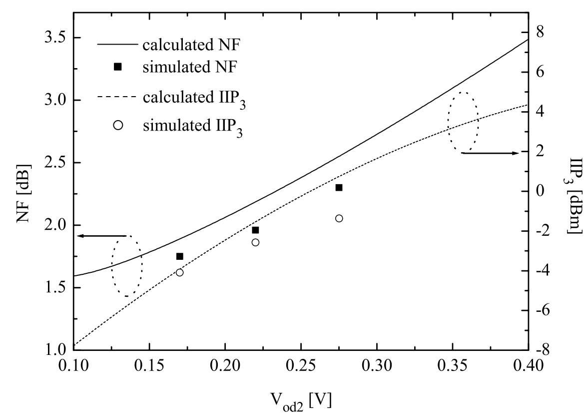


**Fig. 9** Calculated and simulated NF and IIP$_3$ versus $V_{od2}$.

(5) Overdrive of $M_2$

Figure 9 shows the calculated and simulated NF and IIP$_3$ versus $V_{od2}$ at $I_{d1} = 7.0$ mA, $V_{od1} = 0.32$ V and $I_{d2} = 1.0$ mA. The differences between the simulated and calculated results at a higher $V_{od2}$ originate form the simplified noise equivalent circuit including the Miller effect (Fig. 5) and the IIP$_3$ approximation of two non-linear stages in cascade (Eq. (36)).

Although the increase of $V_{od1}$ results in better noise performance and poor linearity as shown in Fig. 8, the increase of $V_{od2}$ leads to the opposite results: Better linearity and poor noise performance. This is because decreasing $g_{m2}$ increases the Miller factor $M$, resulting in a higher NF. Therefore, an LNA with both the given noise performance and high linearity can be achieved by choosing the highest $V_{od2}$, that is, 0.17 V satisfying the NF specification, resulting in $W_2 = 50\,\mu$m.

(6) Inductors and capacitors

Substituting the determined parameters into the equation of $L_g$ derived from Eqs. (2), (3), (11), (15) and (16), $L_g = 3.3$ nH is derived and then $L_s = 1.0$ nH from Eqs. (3) and (16).

Finally, the resonance condition gives inductors $L_i$ of 3.1 nH and capacitors $C_i$ of 120 fF ($i$ =1, 2, 3). We used the ac-coupling capacitor $C_c$ of 3.3 pF which is large enough not to affect RF signals.

From the above consideration, the following performances are expected: The power gain of 23 dB, NF 1.8 dB, $\text{IIP}_3$ −4.1 dBm and power consumption 8 mW.

## 6. Experimental Results

A two-stage LNA is implemented in a 0.15-$\mu$m FD-SOI CMOS process with five metal layers and metal-insulator-metal (MIM) capacitors. The cut-off frequency of a 0.15 $\mu$m NMOS consisting of 48 fingers with a unit of 5 $\mu$m width is about 54 GHz at $V_{ds} = 1$ V and $I_d = 7$ mA [1]. The microphotograph of the fabricated LNA is shown in Fig. 10. All the pads are not ESD protected. A quality factor of on-chip inductors is about 11 at 5.4 GHz. The chip area is 0.78 mm × 0.73 mm. For the measurement, a buffer with a voltage gain of around 0 dB is implemented. The buffer has a small influence on the input reflection and noise performance of the LNA because the LNA has high reverse isolation and high gain. The current consumption of the LNA without the buffer is 8.3 mA at a 1-V supply voltage.

$S$-parameters, NF and $\text{IIP}_3$ of the LNA are measured using on-wafer RF probes. The above characteristics of the LNA with an ideal inductor $L_g$ in series to the gate are calculated based on the measured data [11]. This avoids instrumental error originating from bonding wires.

Figure 11 shows measured and simulated $S_{11}$ and $S_{21}$, i.e., power gain of the LNA. The impedance matching is achieved ($S_{11} < -10$ dB) around 5.4 GHz where the power gain is 23 dB. Figure 12 shows measured and simulated NF versus frequency. An NF of 1.7 dB is obtained at 5.4 GHz. The measured results agree well with those simulated by the the small-signal and noise model [11].

Figure 13 shows the measured output power of fundamental tone and third-order intermodulation (IM3) products for two tones (5.4 and 5.41 GHz). The measured $\text{IIP}_3$ is about −18.0 dBm. This result includes the nonlinearity of the buffer, which can be eliminated by using the follow equation:

$$\frac{1}{A^2_{LNA,IIP_3}} \simeq \frac{1}{A^2_{LNA+Buf,IIP_3}} - \frac{A^2_{v,LNA}}{A^2_{Buf,IIP_3}} \tag{50}$$

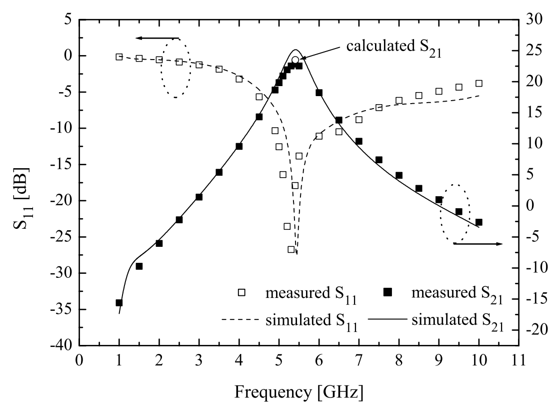


**Fig. 11** Measured and simulated $S_{11}$ and $S_{21}$ of LNA.

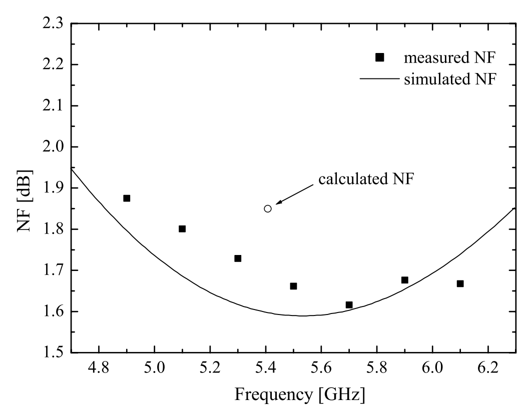


**Fig. 12** Measured and simulated NF of LNA.

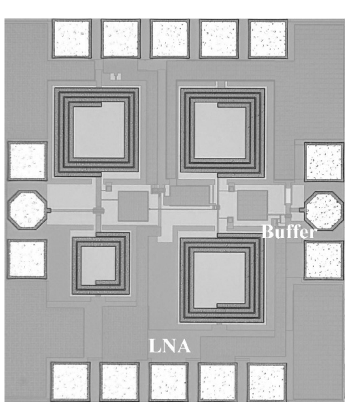


**Fig. 10** Microphotograph of LNA.

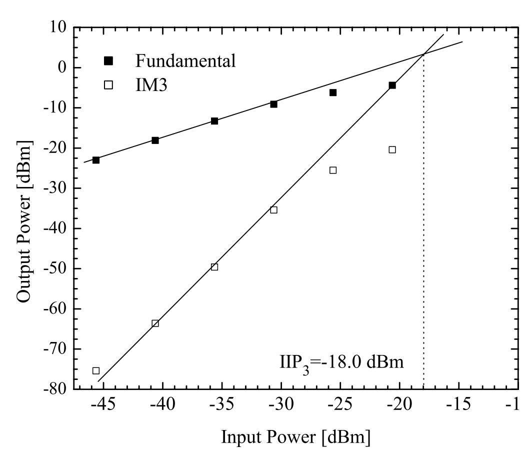


**Fig. 13** Measured $\text{IIP}_3$ of LNA including buffer.

**Table 2** Comparison of performances of LNA.

| | Specification | Measurement | Calculation | Simulation |
|---|---|---|---|---|
| Power Gain @ 5.4 GHz | 20 dB | 23 dB | 23 dB | 25 dB |
| NF @ 5.4 GHz | 2.0 dB | 1.7 dB | 1.8 dB | 1.6 dB |
| $IIP_3$ | N/A | −6.1 dBm | −4.1 dBm | −3.0 dBm |

**Table 3** Measured performance of two LNAs.

| | $L_s$=1.0 nH | $L_s$=0.8 nH |
|---|---|---|
| $S_{11}$ | $< -10$ dB | |
| Power Gain @ 5.4 GHz | 23 dB | 26 dB |
| NF @ 5.4 GHz | 1.7 dB | 1.4 dB |
| $IIP_3$ | −6.1 dBm | −7.0 dBm |
| Current Consumption | 8.3 mA | |
| Supply Voltage | 1.0 V | |

where $A_{v,LNA}$ is the voltage gain of the LNA, $A_{LNA,IIP_3}$, $A_{Buf,IIP_3}$ and $A_{LNA+Buf,IIP_3}$ represent the $IIP_3$ of the LNA, buffer and LNA including the buffer in the expression of voltage amplitude, respectively. Substituting measured $IIP_{3,LNA+Buf} = -18.0$ dBm, $IIP_{3,Buf} = 10.8$ dBm and $A_{v,LNA} = 22.5$ dB into Eq. (50), the $IIP_3$ of the LNA is achieved about $-6.1$ dBm.

Among other characteristics, $S_{12}$ and $S_{22}$ are below $-42$ dB and $-10$ dB, respectively.

Table 2 shows a comparison of performances of the LNA. The simulated and calculated power gain and NF are consistent with the measured results and the fabricated LNA, thus satisfying the specifications. The calculated $IIP_3$ agrees with the simulated one, but these results are slightly different from the measured $IIP_3$. The difference is due to inaccurate FD-SOI MOS device parameters used in the simulation and calculation.

Table 3 shows a performance summary of the above LNA ($L_s = 1.0$ nH) and other fabricated LNA with $L_s = 0.8$ nH. The table suggests that power gain and noise performance of the LNA can be improved by lowering $L_s$.

## 7. Conclusion

We investigated high frequency characteristics of a low-voltage two-stage CMOS LNA. Based on the derived equations of power gain, NF and $IIP_3$, we proposed a new design methodology of the LNA. By using the overdrive voltages of the MOSFETs as adjustable parameters, we demonstrated systematic design of an LNA under given specifications. A 1-V 5.4-GHz LNA was realized in 0.15-$\mu$m FD-SOI CMOS technology. The LNA achieved a power gain of 23 dB, NF of 1.7 dB and $IIP_3$ of $-6.1$ dBm with a power consumption of 8.3 mW. The results are consistent with the calculated results obtained from the derived equations. This ensures the validity of the equations and proposed design methodology.

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## Appendix: Derivations of Output Noise Originating from $M_1$ and $M_2$

The induced-gate noise correlates to the drain noise. Considering the correlation between the gate and drain noises, the induced-gate noise is expressed as the sum of correlated and uncorrelated components:

$$\begin{aligned}\overline{|i_{ng}|^2} &= \overline{|i_{ngc}|^2} + \overline{|i_{ngu}|^2} \\ &= \overline{|i_{ng}|^2}|c|^2 + \overline{|i_{ng}|^2}(1-|c|^2) \end{aligned} \qquad \text{(A· 1)}$$

where $i_{ng}$ is given by Eq. (23). The correlation coefficient, $c$, between the induced-gate and drain noise currents is given by [5], [6]

$$c = \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{|i_{ng}|^2}}\sqrt{\overline{|i_{nd}|^2}}}. \tag{A·2}$$

From the correlation shown above, the output noise due to $M_i$ is expressed as

$$\begin{aligned}\overline{|i_{o,M_i}|^2} &= \overline{|i_{o,ndi} + i_{o,ngi}|^2} \\ &= \overline{|i_{o,ndi} + i_{o,ngci}|^2} + \overline{|i_{o,ngui}|^2} \\ &= \overline{|i_{o,ndi}|^2} + \overline{i_{o,ngci} \cdot i_{o,ndi}^*} + \overline{i_{o,ndi} \cdot i_{o,ngci}^*} \\ &\quad + \overline{|i_{o,ngci}|^2} + \overline{|i_{o,ngui}|^2},\end{aligned} \tag{A·3}$$

where $i_{o,ndi}$, $i_{o,ngci}$ and $i_{o,ngui}$ are the output noise currents originating from $i_{ndi}$, $i_{ngci}$ and $i_{ngui}$, respectively.

From Fig. 5, the transfer function from the drain noise current $i_{nd1}$ to the output $i_{o,nd1}$ is given by

$$H_{nd1}(j\omega_0) = \frac{R_{eq} + r_{nqs,eff}}{(R_{eq} + R_{in})(1+1/g_{m2}R_I)}. \tag{A·4}$$

The transfer function from the induced-gate noise current $i_{ng1}$ to the output $i_{o,ng1}$ is also given by

$$H_{ng1}(j\omega_0) = \frac{\omega_{T1}\left(R_{eq} + j/\omega_0 C_{gs1,eff}\right)}{j\omega_0(1+\alpha_{gd}M)(R_{eq}+R_{in})(1+1/g_{m2}R_I)}. \tag{A·5}$$

Using Eqs. (22), (23), (A· 4) and (A· 5), we have

$$\begin{aligned}\overline{|i_{o,nd1}|^2} &= |H_{nd1}(j\omega_0)|^2\,\overline{|i_{nd1}|^2} \\ &= \frac{4k_B T\gamma_1 g_{m1}(R_{eq}+r_{nqs,eff})^2\Delta f}{\alpha_1(R_{eq} + R_{in})^2(1+1/g_{m2}R_I)^2},\end{aligned} \tag{A·6}$$

$$\begin{aligned}&\overline{i_{o,ngc1} \cdot i_{o,nd1}^*} + \overline{i_{o,nd1} \cdot i_{o,ngc1}^*} \\ &= H_{ngc1}(j\omega_0) i_{ngc1} \cdot H_{nd1}^*(j\omega_0) i_{nd1}^* \\ &\quad + H_{nd1}(j\omega_0) i_{nd1} \cdot H_{ngc1}^*(j\omega_0) i_{ngc1}^* \\ &= -2|c|\sqrt{\frac{\delta_1}{\kappa_1\gamma_1}}\frac{4k_B T\gamma_1 g_{m1} R_{eq}(R_{eq}+r_{nqs,eff})\Delta f}{(1+\alpha_{gd}M)(R_{eq}+R_{in})^2(1+1/g_{m2}R_I)^2},\end{aligned} \tag{A·7}$$

$$\begin{aligned}&\overline{|i_{o,ngc1}|^2} + \overline{|i_{o,ngu1}|^2} \\ &= \left|H_{ng1}(j\omega_0)\right|^2\overline{|i_{ng1}|^2} \\ &= \frac{4k_B T\alpha_1\delta_1 g_{m1}(R_{eq}^2 + 1/\omega_0^2 C_{gs1,eff}^2)\Delta f}{\kappa_1(1+\alpha_{gd}M)^2(R_{eq}+R_n)^2(1+1/g_{m2}R_I)^2}.\end{aligned} \tag{A·8}$$

Substituting Eqs. (A· 6)–(A· 8) into Eq. (A· 3), Eq. (25) can be derived.

In the same way, the output noise originating from $M_2$ is also derived. From Fig. 6, the transfer functions from the drain and induced-gate noise currents to the output are derived as

$$H_{nd2}(j\omega_0) = \frac{1}{1 + g_{m2}R_I}, \tag{A·9}$$

$$H_{ng2}(j\omega_0) = \frac{1}{1 + 1/g_{m2}R_I}. \tag{A·10}$$

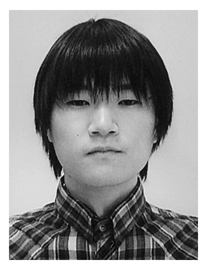
From Eqs. (22), (23), (A· 9) and (A· 10), we have

$$\overline{|i_{o,nd2}|^2} = \frac{4k_B T\gamma_2 g_{m2}}{\alpha_2(1 + g_{m2}R_I)^2}, \tag{A·11}$$

$$\overline{i_{o,ngc2} \cdot i_{o,nd1}^*} + \overline{i_{o,nd2} \cdot i_{o,ngc2}^*} = 0, \tag{A·12}$$

$$\overline{|i_{o,ngc2}|^2} + \overline{|i_{o,ngu2}|^2} = \frac{4k_B T\delta_2\alpha_2(\omega_0 C_{gs2})^2}{\kappa_2 g_{m2}(1+1/g_{m2}R_I)^2}. \tag{A·13}$$

Substituting Eqs. (A· 11)–(A· 13) into Eq. (A· 3), Eq. (28) can be derived.



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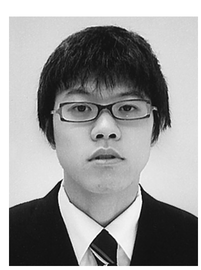

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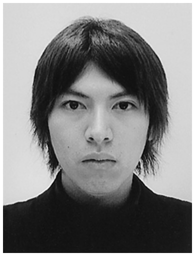

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