IEICE Electronics Express, Vol.1, No.16, 518–522

Drain current response delay of FD-SOI MOSFETs in RF operation

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Abstract: We investigated the frequency dependences of Y_{22} of FD-SOI MOSFETs, in which the drain current response delay is observed for the first time. Short channel FD-SOI devices operating in linear region show significant drain current response delay. It is confirmed that FD-SOI MOSFET's RF behavior can be well reproduced with the proposed model including the drain current response delay.

Keywords: FD-SOI, MOSFET, RF, modeling, drain current response delay

Classification: Electron devices

References

[1] F. Ichikawa, Y. Nagatomo, Y. Katakura, M. Itoh, S. Itoh, H. Matsuhashi, T. Ichimori, N. Hirashita, and S. Baba, "Fully depleted SOI process and technology for digital and RF applications," *Solid-State Electron.*, vol. 48, pp. 999–1006, 2004.

[2] A. O. Adan, T. Yoshimatsu, S. Shitara, N. Tanba, and M. Fukumi, "Linearity and Low-Noise Performance of SOI MOSFETs for RF Applications," *IEEE Trans. Electron Devices*, vol. 49, no. 5, pp. 881–888, May 2002.

[3] Ickjin Kwon, Minkyu Je, Kwyro Lee, and Hyungcheol Shin, "New RF MOSFET Small Signal SPICE Model Part 1," *J. Circuit Sim. SPICE Model. Eng.*, ed. Silvaco, vol. 11, no. 4, April 2000.

[4] I. Kwon, M. Je, K. Lee, and H. Shin, "A New Small Signal Modeling of RF MOSFETs including Charge Conservation Capacitances," *Proc. European Solid-State Circuits Conference*, pp. 296–299, Sept. 2000.

[5] Y. Tsividis, "High-Frequency Small-Signal Models," *Oper. Model. MOS Transist.*, 2nd ed., pp. 440–512, McGraw-Hill, 1999.

DOI: 10.1587/elex.1.518
Received October 22, 2004
Accepted November 08, 2004
Published November 25, 2004

1 Introduction

On a Radio-frequency (RF) CMOS circuit design, a deep understanding of the frequency behavior of MOSFETs is very important. Silicon-on-insulator (SOI) MOSFETs are suitable devices for high-frequency circuits because of their much smaller substrate capacitance than bulk MOSFETs [1, 2]. The feature, however, induces a unique characteristic in the frequency behavior of SOI MOSFETs due to the delay of drain current response. This behavior is clearly observed in short channel SOI MOSFETs, where drain parasitic capacitances is relatively small. For long channel or bulk devices, the existence of large drain parasitic capacitances significantly suppresses the frequency dependence originating from the delay of drain current response.

The aim of this paper are twofold: (1) to present a unique frequency behavior of Fully-depleted SOI (FD-SOI) MOSFETs, and (2) to clarify its physical mechanism.

2 Measurement and Evaluation

In this study, Y-parameters are extracted from the measured two-port S-parameters of MOSFETs fabricated in 0.15 μm FD-SOI process, where the source and substrate terminals are grounded while the body terminal open. The wafer-level two-port S-parameters in the range from 0.2 GHz to 20 GHz

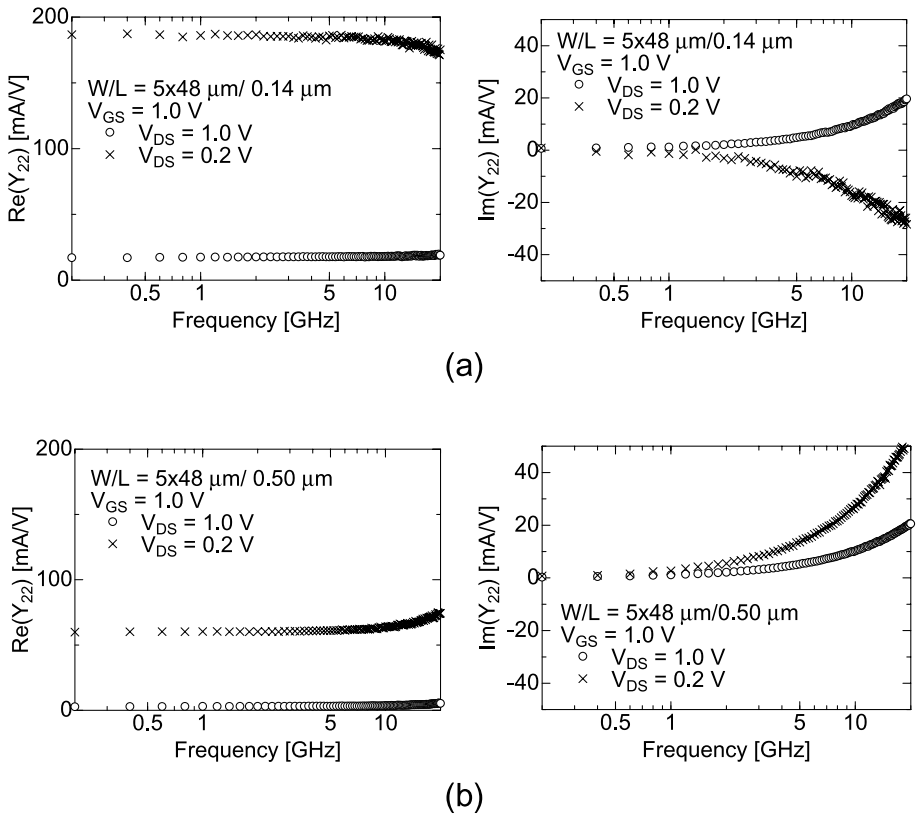

Fig. 1. Y-parameters (Y_{22}) of FD-SOI MOSFETs measured at V_{GS}=1.0V and either V_{DS}=1.0V (in saturation region) or 0.2V (in linear region) with W=5×48 μm, (a) L=0.14 μm and (b) L=0.50 μm.

DOI: 10.1587/elex.1.518
Received October 22, 2004
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Published November 25, 2004

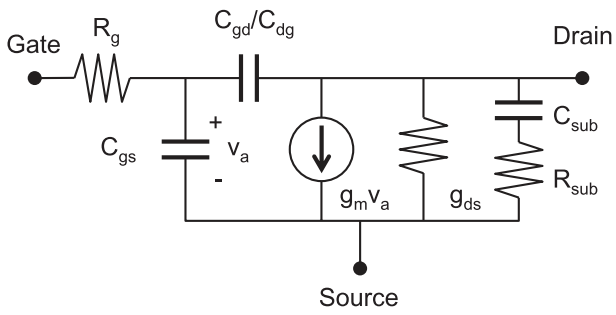

Fig. 2. A conventional small-signal equivalent circuit of a RF MOSFET.

are measured with a network analyzer, Agilent 8722ES. The measurements of open- and short-pad patterns [3] are performed to eliminate the influence of pad and on-chip wirings.

Figure 1 (a) shows the measured Y_{22} data of a FD-SOI MOSFET with W=5×48 μm and L=0.14 μm in linear (V_{GS}=1.0V, V_{DS}=0.2V) and saturation (V_{GS}=1.0V, V_{DS}=1.0V) regions.

To analyze the measured results, a conventional small-signal equivalent circuit of a RF MOSFET shown in Fig. 2 [4] has been widely used. Based on the equivalent circuit, one can derive Y_{22} given by

$$\begin{aligned} Re(Y_{22}) &= g_{ds} + \frac{\omega^2 C_{sub}^2 R_{sub}}{1+\omega^2 C_{sub}^2 R_{sub}^2} \\ &+ \frac{\omega^2 C_{gd}\{C_{dg} + g_m(C_{gs}+C_{gd})R_g\}R_g}{1+\omega^2(C_{gs}+C_{gd})^2 R_g^2} \end{aligned} \tag{1}$$

$$\begin{aligned} Im(Y_{22}) &= \omega\left[C_{dg} + \frac{C_{sub}}{1+\omega^2 C_{sub}^2 R_{sub}^2}\right. \\ &+ \left.\frac{C_{gd}\{g_m - \omega^2 C_{dg}(C_{gs}+C_{gd})R_g\}R_g}{1+\omega^2(C_{gs}+C_{gd})^2 R_g^2}\right]. \end{aligned} \tag{2}$$

Eqs. (1) and (2) show that both Re(Y_{22}) and Im(Y_{22}) increase with frequency. However, as shown in Fig. 1 (a), the short channel SOI-MOSFETs measured at V_{DS}=0.2V exhibits small decrease in Re(Y_{22}) over 5 GHz, and noticeable decrease with frequency in Im(Y_{22}). The differences between the measured results and analytical frequency dependence are attributed to the delay of drain current response, that is, non-quasi static effect: the speed of the channel charge is limited by the finite channel conductance produced by every infinitesimal gate-channel capacitor along the channel [5]. This effect can be simulated by introducing the frequency dependence of g_{ds} given by

$$g_{ds} = \frac{g_{ds0}}{1+j\omega\tau_{ds}}, \tag{3}$$

where g_{ds0} is low frequency drain conductance and τ_{ds} is the drain current response time. The real part of Eq. (3) decreases at high frequency, and the imaginary part with negative sign decreases with frequency, which explains the measured frequency dependence of Y_{22} shown in Fig. 1 (a).

DOI: 10.1587/elex.1.518
Received October 22, 2004
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3 Model Modification

Substituting Eq. (3) into Eqs. (1) and (2), we can derive the new formula including the frequency dependence of the drain conductance.

$$\begin{aligned} Re(Y_{22}) &= \frac{g_{ds0}}{1+\omega^2\tau_{ds}^2} + \frac{\omega^2 C_{sub}^2 R_{sub}}{1+\omega^2 C_{sub}^2 R_{sub}^2} \\ &+ \frac{\omega^2 C_{gd}\{C_{dg} + g_m(C_{gs}+C_{gd})R_g\}R_g}{1+\omega^2(C_{gs}+C_{gd})^2 R_g^2} \end{aligned} \tag{4}$$

$$\begin{aligned} Im(Y_{22}) &= \omega\left[-\frac{\tau_{ds} g_{ds0}}{1+\omega^2\tau_{ds}^2} + C_{dg} + \frac{C_{sub}}{1+\omega^2 C_{sub}^2 R_{sub}^2}\right. \\ &+ \left.\frac{C_{gd}\{g_m - \omega^2 C_{dg}(C_{gs}+C_{gd})R_g\}R_g}{1+\omega^2(C_{gs}+C_{gd})^2 R_g^2}\right] \end{aligned} \tag{5}$$

Note that the frequency dependence of Y_{22} becomes significant for short channel MOSFETs with large g_{ds0}, especially operating in linear region (V_{DS} = 0.2V), as shown in Fig. 1 (a). For long channel devices, their large gate capacitance and small g_{ds} even in linear region overwhelm the delay of drain current response so that the frequency dependence follows the conventional model predictions, as shown in Fig. 1 (b).

In order to study the validity of Eqs. (4) and (5), Y_{22} calculated from

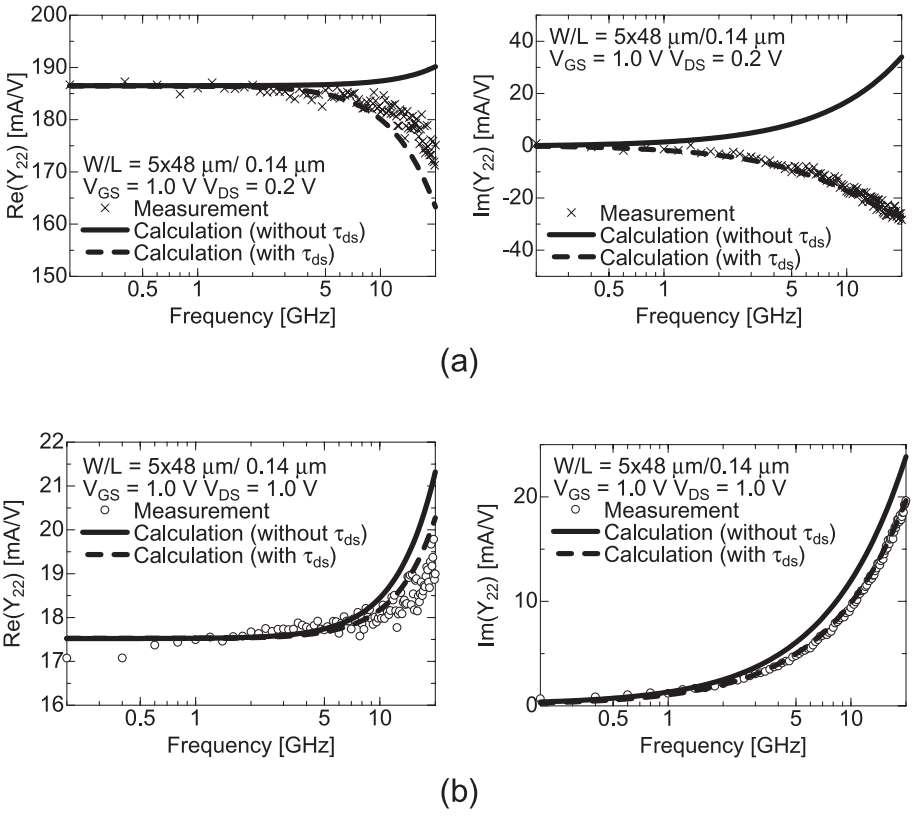

Fig. 3. The calculated Y-parameters (Y_{22}) of FD-SOI MOSFETs, which include with and without the influence of drain current delay. (a) linear region (V_{GS}=1.0V, V_{DS}=0.2V) and (b) saturation region (V_{GS}=1.0V, V_{DS}=1.0V).

DOI: 10.1587/elex.1.518
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the new equivalent circuit model is compared with measured results where several MOS parameters in Y_{22} are numerically derived from Y_{11}, Y_{21} and Y_{12} as follow.

$$R_g = Re(Y_{11})/(Im(Y_{11}))^2 \quad (6)$$
$$C_{gd} = -Im(Y_{12})/\omega \quad (7)$$
$$C_{gs} = (Im(Y_{11}) + Im(Y_{12}))/\omega \quad (8)$$
$$C_{dg} = -Im(Y_{21})/\omega - g_m R_g(C_{gs} + C_{gd}) \quad (9)$$

Figure 3 shows the measured Y_{22} and their calculated values by using these parameters with and without the drain current delay. C_{sub} is assumed to be negligibly small because of their SOI structure. g_{ds0} and τ_{ds} are treated as fitting parameters. As shown in Fig. 3 (a), the calculations based on the new model well reproduce the frequency behaviors of Y_{22} measured at V_{DS}=0.2V. The new model also demonstrates better agreement even in the saturation region than a conventional model as shown in Fig. 3 (b), which proves the existence of drain current delay even in saturation region. In these calculations, τ_{ds} used is about a few pico seconds.

For bulk devices, the effect of drain current delay has not been ever observed because bulk devices have extremely larger C_{sub} than SOI devices. Note that the second term of Eq. (4) and the third term of Eq. (5) are much larger than each of the first terms of their equations for bulk MOSFETs.

4 Conclusion

Experimental frequency dependences of Y_{22} of FD-SOI MOSFETs have been presented. The drain current response delay for drain voltage is observed for the first time. This behavior can be explained with non-quasi-static effect in g_{ds}. Short channel FD-SOI devices show significant drain current response delay in linear region due to their large g_{ds}. Y_{22} calculated with the proposed model including the delay demonstrates that short channel FD-SOI devices have drain current response delay even in saturation region. Large C_{sub} in bulk MOSFET prevents us from observing drain current response delay since the observation of drain current response delay requires small parasitic capacitances in drain terminal.

Acknowledgments

This work is supported by Semiconductor Technology Academic Research Center (STARC).

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