A 0.5 V Area-Efficient Transformer Folded-Cascode CMOS Low-Noise Amplifier

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SUMMARY A 0.5 V transformer folded-cascode CMOS low-noise amplifier (LNA) is presented. The chip area of the LNA was reduced by coupling the internal inductor with the load inductor, and the effects of the magnetic coupling between these inductors were analyzed. The magnetic coupling reduces the resonance frequency of the input matching network, the peak frequency and magnitude of the gain, and the noise contributions from the common-gate stage to the LNA. A partially-coupled transformer with low magnetic coupling has a small effect on the LNA performance. The LNA with this transformer, fabricated in a 90 nm digital CMOS process, achieved an $S_{11}$ of $-14$ dB, NF of 3.9 dB, and voltage gain of 16.8 dB at 4.7 GHz with a power consumption of 1.0 mW at a 0.5 V supply. The chip area of the proposed LNA was 25% smaller than that of the conventional folded-cascode LNA.

key words: CMOS, low-noise amplifier (LNA), low voltage, transformer

1. Introduction

Although the continuous scaling of CMOS technologies has improved the high-frequency performance of MOSFETs, it has imposed two challenges on CMOS radio-frequency integrated circuits (RFICs): low-voltage operation and a small chip area. The International Technology Roadmap for Semiconductors (ITRS) [1] predicts that the supply voltages of low-power digital circuits will decrease to 0.5 V in the near future. Reference [2] shows that a 45 nm (state-of-the-art) CMOS process costs approximately 10 times as much as a 0.13 μm (most widely used) CMOS process. Considering the integration of RF circuits with digital circuits (i.e., system-on-a-chip), we need to develop low-voltage and small-area (low-cost) RF circuits.

Low-noise amplifiers (LNAs) have difficulty in operating at low voltages with a small chip area. Cascode LNAs with inductive source degeneration [3] have been widely used for narrow band receivers, due to low-noise performance and good input impedance matching. However, this LNA is not suitable for low-voltage operation, because it requires a supply voltage of more than two drain-source saturation voltages ($V_{DD} > 2V_{DS,sat}$) to operate the cascode transistor. Although folded-cascode LNAs [4], [5] are more suitable for low voltage operation ($V_{DD} > V_{DS,sat}$), they require more inductors, which lead to an increase in the chip area. Other reported low-voltage LNAs [6], [7] consume much larger chip area than the folded-cascode LNAs, due to many inductors.

We propose a 0.5 V, 5 GHz transformer folded-cascode CMOS LNA [8], which has a smaller chip area than the conventional folded-cascode LNA. The transformer that consists of the internal and load inductors reduces the chip area of the LNA, while affecting the LNA performance. This paper is organized as follows. Section 2 describes the circuit topology of the proposed LNA. The effects of the transformer on the LNA performance are analyzed in Sect. 3. Section 4 describes the design of the LNA and transformer. Section 5 presents the measurements of the LNA implemented in a 90 nm digital CMOS technology, and Sect. 6 concludes the paper.

2. Circuit Topology

Figure 1 shows a schematic of the proposed LNA based on the conventional folded-cascode LNA with inductive source degeneration. The gate and source inductors, $L_L$ and $L_S$, provide input impedance matching at an operating frequency [3]. The PMOS transistor $M_2$ reduces the Miller effect of the gate-drain capacitor of the input transistor $M_1$, and improves the reverse isolation performance of the LNA. The internal inductor $L_L$, resonating with the parasitic capacitance $C_L$ at node I, provides a high impedance, thereby the signal current amplified by $M_1$ flows into $M_2$. The load inductor $L_L$ also resonates with the parasitic capacitance $C_L$, resulting in a high impedance. These inductors, $L_I$ and $L_L$, are magnetically coupled to form a transformer in such a way as to have a positive magnetic coupling with retaining the LNA.
performance.

The positive magnetic coupling of $L_I$ and $L_s$ is the most effective way to reduce the chip area of the folded-cascode LNA. Increasing the magnetic coupling leads to a smaller $L_I$ and $L_s$ (smaller chip area), as will be shown in the next section. On the contrary, the negative magnetic coupling requires a larger $L_I$ and $L_s$ (larger chip area). The coupling of $L_g$ or $L_I$ and $L_s$ or $L_L$ is also not beneficial for the following reasons:

1. $L_g$ is often implemented with a bonding wire.
2. $L_s$ is usually small (< 1.0 nH) for input impedance matching.
3. The coupling makes the LNA unstable.

3. Effect of Magnetic Coupling

The magnetic coupling between $L_I$ and $L_s$ affects the LNA performance in terms of input impedance, gain, and noise. In this section, the effects of the magnetic coupling are analyzed, and the stability of the LNA is also discussed.

3.1 Input Impedance

The magnetic coupling changes the frequency response of the LNA input impedance $Z_{in}$ through the gate-drain capacitance of $M_1$, $C_{gd1}$. The small-signal equivalent circuit of the input stage, shown in Fig. 2, yields $Z_{in}$, given by

$$Z_{in} \approx sL_g + \frac{1}{\omega_{r1} L_I + sL_s + \frac{1}{\alpha_M}},$$

(1)

$$\alpha_M = 1 + \frac{\omega_{r1} g_{m1}}{\alpha_{gd1}} Y_I,$$

(2)

where $\omega_{r1} = g_{m1}/C_{gd1}$ is the unity current gain frequency of $M_1$; $\alpha_{gd1} = C_{gd1}/C_{gd1}$ is the ratio between $C_{gd1}$ and $C_{gd1}$. The input admittance of the common-gate stage, shown in Fig. 3, is given by

$$Y_I = \frac{i_i}{v_i} \approx g_{m2} + sC_I + \frac{1}{sL_I + R_I} - \frac{nk(g_{m2} - nkC_L) + \omega^2 L_s C_L + sR_s C_L}{1 + s^2(1 - k^2)L_s C_L + sR_s C_L},$$

(3)

where $g_{m2}$ is the transconductance of $M_2$; $R_I$ and $R_s$ are the parasitic resistances of $L_I$ and $L_s$, respectively; $k$ and $n = \sqrt{L_s/L_I}$ are the coupling factor and turns ratio of the transformer, respectively. The frequency responses of $Y_I$ and $1/Y_I$ are described in Appendix A. The calculated real and imaginary parts of $\alpha_M$ and $\omega_0$ are shown in Figs. 4(a) and (b), respectively. Using $\text{Re}[\alpha_M]$ and $\text{Im}[\alpha_M]$, we can approximate $Z_{in}$ as

$$\text{Re}[Z_{in}] \approx \frac{\omega_{r1} L_I \text{Re}[\alpha_M] - \text{Im}[\alpha_M]}{|\alpha_M|^2},$$

(4)

$$\text{Im}[Z_{in}] \approx \omega_{r1} L_I \text{Re}[\alpha_M] + \text{Re}[\alpha_M]$$

(5)

where $\omega_{r1}$ is ignored against $1/\omega_{r1} g_{gd1}$. As shown in Fig. 4(a), $\text{Re}[\alpha_M]$ increases and $\text{Im}[\alpha_M]$ decreases at low frequencies, which results in an increase of $\text{Re}[Z_{in}]$. For a low $k$ (<0.6), $\text{Re}[Z_{in}]$ becomes a maximum around the frequency at which $\text{Im}[\alpha_M]$ becomes a minimum. Meanwhile, $\text{Im}[Z_{in}]$ with $k$ reaches zero faster than $\text{Im}[Z_{in}]$ without $k (k = 0)$, due to the increase in $\text{Re}[\alpha_M]$ at low frequencies.

The magnetic coupling shifts the input impedance matching region (an $S_{11}$ of less than $-10$ dB) toward lower frequencies. Due to good reverse isolation of the folded-cascode topology ($S_{12} < 0$), the $S_{11}$ of the LNA can be approximated as [9]

$$S_{11} \approx \frac{Z_{in} - R_i}{Z_{in} + R_i},$$

(6)

where $R_i$ is the signal source impedance. For input impedance matching at the frequency of $\omega_0$, the following conditions must be satisfied:

$$\text{Re}[Z_{in}] = R_s,$$

(7)

$$\text{Im}[Z_{in}] = 0,$$

(8)

$$\text{Im}[\alpha_M] = 0,$$

(9)

which give the following conditions:

$$\frac{\omega_{r1} L_I}{\text{Re}[\alpha_M(\text{j}\omega_0,\omega_0)]} \approx R_s,$$

(10)

$$\omega_0 \approx \frac{1}{\sqrt{L_s C_{gs1} \text{Re}[\alpha_M(\text{j}\omega_0,\omega_0)]}}$$

(11)

$$\omega_0,\omega_0 \approx \frac{1}{\sqrt{L_I(C_L + n^2k^2C_L)}},$$

(12)
respectively, where \( \text{Re}[\alpha_M(j\omega_{0,\alpha_M})] \) is approximated as
\[
\text{Re}[\alpha_M(j\omega_{0,\alpha_M})] \approx 1 + \frac{\alpha_{g1l}g_{m1}}{(1-nk)g_{m2}}. \tag{13}
\]
Equations (10)–(13) show that the resonance frequencies of \( Z_{in} \) and \( \alpha_M \) decrease and \( \text{Re}[\alpha_M] \) increases as \( k \) increases. Figure 4(c) shows the calculated \( S_{11} \) with \( k \) as a parameter. Input impedance matching is achieved around \( \omega_0 \), which decreases with increasing \( k \).

3.2 Gain

The magnetic coupling reduces the peak frequency and magnitude of the LNA gain. The common-gate stage acts as a transimpedance, which converts the input signal current \( i_i \) to the output voltage \( v_{out} \), as shown in Fig. 3. The input current \( i_i \) amplified by the first stage is derived from Fig. 2:
\[
i_i \approx \frac{g_{m1}}{j\omega_0 C_{gs1}R_s \cdot \text{Re}[\alpha_M]} v_{in}, \tag{14}
\]
where input impedance matching is assumed (i.e., \( Z_{in} = R_2 \)) and \( v_{in} \) represents the input voltage of the LNA as shown in Fig. 2. The transimpedance from node I to the output is given by
\[
Z_T = \frac{v_{out}}{i_i} = \frac{v_{out}}{v_{in}} \frac{v_i}{\omega_0 C_{gs1}R_s \cdot \text{Re}[\alpha_M]}.
\tag{15}
\]

Equations (10)–(13) show that the resonance frequencies of \( Z_{in} \) and \( \alpha_M \) decrease and \( \text{Re}[\alpha_M] \) increases as \( k \) increases. Figure 5 shows the calculated \( A_{v,LNA} \) with \( k \) as a parameter. The increase of \( k \) shifts the gain peak toward a lower frequency and reduces the gain magnitude. The peak frequency in Fig. 5 corresponds well to that calculated from Eq. (19).

The LNA with the magnetic coupling sacrifices a maximum voltage gain to achieve the target peak frequency, \( \omega_{p,1} \).
the parallel impedances of the internal and load LC tanks at and $LL$

Equation (19) gives the following condition:

$$L_L = L_I = \frac{1}{\omega_{ps} (1 + k)C_L} \quad \text{for } n = 1. \quad (20)$$

A turns ratio of one provides the smallest chip area of the transformer, because $L_L$ and $L_I$ simultaneously decrease with increasing $k$. Equation (20) shows that a smaller $L_I$ and $L_L$ are required to achieve $\omega_{ps}$ as $k$ increases. Reducing $L_I$ and $L_L$ leads to a smaller chip area, but to a decrease in the parallel impedances of the internal and load LC tanks at the resonance frequencies ($Z_p = (\omega_0 L_I L_L) / R_{L}$), causing a lower voltage gain. Figure 6 shows the calculated voltage gain for $f_{ps} = 5.0 \, \text{GHz}$ where $L_L$ and $L_I$ satisfy Eq. (20). A peak frequency of approximately $5.0 \, \text{GHz}$ can be achieved even for a large $k$, while the maximum gain decreases with increasing $k$. A small coupling factor such as 0.2, however, is acceptable for the LNA, due to a small gain reduction of 3 dB.

3.3 Noise

The transformer reduces the output noise originating from the common-gate transistor and the parasitic resistance of $L_L$, thereby improving the noise performance. This transformer noise reduction scheme has been reported in [10]. Figure 7 conceptually illustrates how the transformer reduces the drain noise current of $M_2$, represented by $i_{nd2}$. The primary (internal) inductor $L_I$ detects $i_{nd2}$ and then induces a noise voltage to the secondary (load) inductor $L_L$. The induced noise voltage is correlated and anti-phase to the output noise voltage produced by $i_{nd2}$ flowing through $L_L$, reducing the output noise caused by $M_2$. The other output noise originating from $L_L$ is also reduced by the transformer in the same way.

The magnetic coupling affects the noise contributions from $M_2$, $L_I$, and $L_L$ to the LNA ($F_{M_2}$, $F_{L_I}$, and $F_{L_L}$, respectively), but not that from $M_1$ ($F_{M_1}$). The LNA noise factor is given by

$$F = 1 + F_{M_1} + F_{M_2} + F_{L_I} + F_{L_L} + F_{L_L} + F_{L_L}$$

$$F_{M_2} = \gamma_1 \frac{\gamma_1}{\alpha_1} g_{m1} R_i \left( \frac{\omega_0}{\alpha_2 R_i} \right)^2 \left( \frac{\alpha_1 \delta_1}{k_1 g_{m1} \mu s} \right)$$

$$\chi_1 = (1 + \alpha_{gds})^2 - 2 \epsilon |\alpha_1| \left( \frac{\delta_1}{k_1 \gamma_1} \right) (1 + \alpha_{gds}) + \frac{\alpha_2^2 \delta_1}{k_1 \gamma_1}$$

$$F_{L_2} \approx \frac{Y_{L_2}}{Y_{0} + Y_{L_2}} \left( \frac{\omega_0}{\alpha_2 R_i} \right)^2 \left| \alpha_M \right|^2 \left( \frac{\omega_0}{\alpha_2 R_i} \right)^2 \left( 1 - k \right) \left( 1 - j \frac{Y_0 + Y_{L_2}}{\omega_0 C_L} \right)$$

$$\times \left( \frac{\omega_0}{\alpha_2 R_i} \right)^2 \left( 1 - k \right) \left( 1 - j \frac{Y_0 + Y_{L_2}}{\omega_0 C_L} \right)$$

where $\alpha_i = g_{mi} / g_{dss}$ and $g_{dss}$ is the zero bias drain conduc-
tance of $M_i$ ($i = 1, 2$); $\gamma_i$ and $\delta_i$ are the drain noise current factor and the induced gate noise current factor, respectively, and $c$ is the correlation coefficient between these noise currents ($=0.395$ [11]); $k_i$ is the Elmore constant ($=5$ [12]); $L_L = L_L = 1/\omega_0^2(1 + k)C_L$; $Y_0$ represents the output admittance of the input stage at node I and is approximated as $j\omega C_{gdd}$; $Y_{LI C1} = j\omega C_f + 1/(j\omega L_f + R_f)$. The detailed derivations are summarized in Appendix B. Equations (22)–(26) show that $F_M$, is independent of $k$ while $F_{LL}$, $F_{LI}$, and $F_{Lg}$ are functions of $k$. Figure 8 shows the calculated $F_M$, $F_{LL}$, and $F_{LI}$ versus $k$. As Eq. (24) shows, $F_M$, approaches zero with increasing $k$. Meanwhile, $F_{LL}$ increases and $F_{Lg}$ slightly decreases. This difference originates from the different numerators in Eqs. (25) and (26), i.e., $-k(Y_0 + j\omega C_f)$ and $Y_0 + Y_{LI C1}$.

The noise improvement by the transformer is limited in the folded-cascode topology. The calculated noise figure (NF, defined by 10 log $F$) versus $k$ are shown in Fig. 9, where 90 nm CMOS process parameters were used. The NF simulated using Agilent Advanced Design System (ADS) are also plotted. Figure 9 shows that the calculated NF is comparable to the simulated NF, and the magnetic coupling reduces the NF by up to 0.08 dB (calculated) or 0.12 dB (simulated) for $g_{m2} = 15$ mS. The amount of noise reduction is relatively small, because the noise of $M_1$ is the dominant noise source in the LNA ($F_M \cong 1.20$ and 1.05 in the calculations and simulations, respectively).

![Fig. 8 Calculated $F_M, F_{LL}$, and $F_{LI}$ versus $k$.](image)

![Fig. 9 Calculated and simulated NFs versus $k$.](image)

$$\text{Re}[Z_m] = \frac{\omega \gamma_1 \left[L_f(1+\alpha g_{d1})-L_f \alpha g_{d1}\right]}{(1+\alpha g_{d1})^2 + \omega^2 L_f^2 \alpha_{g1}^2 g_{m1}}.$$ (28)

Substituting Eq. (28) in Eq. (27), we have

$$L_L < L_f \left(1 + \frac{1}{\alpha g_{d1}}\right),$$ (29)

which shows that a smaller $L_L$ ensures the stability. Using Eq. (20), we can rewrite the above condition as

$$C_L > \frac{1}{2\omega^2 L_f^2 \left(1 + \frac{1}{\alpha g_{d1}}\right)}.$$ (30)

For example, $C_L > 160 \text{ fF}$ is calculated from $f_{in} = 5 \text{ GHz}$, $L_s = 0.6 \text{ nH}$, and $\alpha g_{d1} = 0.2$. This capacitance value can be satisfied with the parasitic capacitances of $L_L$ and the input capacitance of the following stage.

### 4. Design

The input transistor $M_1$ is designed to achieve a minimum NF at 5 GHz with a bias current $I_{d1}$ of 1.0 mA at a supply voltage of 0.5 V. Equations (22) and (23) provide an optimum (for noise performance) gate width for $M_1$ of $4 \times 40 \mu\text{m}$ (40 gate fingers, each with a unit of 4 $\mu\text{m}$ width) and a minimum gate length of 100 nm. Although the calculated minimum NF is 3.6 dB for $I_{d1} = 1.0$ mA, increasing $I_{d1}$ leads to a lower NF (i.e., 2.2 dB for $I_{d1} = 2.0$ mA).

The size of the common-gate transistor $M_2$ is selected as a compromise between noise and linearity performance. For a fixed bias current of 1.0 mA, a small gate width of $M_2$ provides high linearity [13], but leads to a lower $g_{m2}$, which results in the increase of $F_M$, $F_{LL}$, and $F_{Lg}$ as shown in Eqs. (24)–(26). Figure 9 shows less NF degradation for $g_{m2} > 15$ mS than for $g_{m2} < 15$ mS at a low $k$. Thus, $g_{m2}$ is selected to be approximately 15 mS, which results in a gate width of $4 \times 40 \mu\text{m}$ and gate length of 100 nm.

A partially-coupled transformer, shown in Fig. 10(a), allows us to simultaneously achieve a small chip area (0.314 $\times$ 0.200 mm$^2$) and reduce the magnetic coupling ($k \cong \frac{\alpha g_{d1}}{\alpha g_{d1}}$).
0.1). On the other hand, a stacked transformer, shown in Fig. 10(b), provides a smaller chip area (0.210×0.200 mm²), thereby reducing the cost. However, a large k of the stacked transformer (k ≃ 0.9) leads to poor gain, and does not significantly reduce the LNA NF as shown in Sect. 3. Figure 11 shows the ADS simulated voltage gain and NFs of the LNAs employing the transformers shown in Fig. 10(a) and (b). The transformers were designed using a 3-D electromagnetic simulator (Ansoft HFSS), and the inductors of the transformer are designed to resonate at a frequency of approximately 5 GHz. The outer diameter of each inductor is 200 μm, the metal width 7 μm, and the metal spacing 2 μm. Electromagnetic simulations resulted in $L_t = L_L = 3.6$ nH and quality factors (Q) of 6.7 at 5 GHz.

The inductances of $L_t$ and $L_g$ are determined by the input impedance matching conditions, derived from Eqs. (7)–(9): $L_t = 0.8$ nH and $L_g = 4.3$ nH. The outer diameter of $L_g$ is 200 μm, the metal width 5 μm, and metal spacing 2 μm. The simulated Q of $L_g$ was 7.5 at 5 GHz.

5. Experimental Results

The designed LNA with the partially-coupled transformer was fabricated in a 90 nm digital CMOS process without metal-insulator-metal (MIM) capacitors. For comparison, a conventional folded-cascode LNA was also fabricated on the same chip. A micrograph of the fabricated LNAs is shown in Fig. 12. The active chip areas (without the pads) of the proposed and conventional LNAs were 0.39 × 0.55 mm² and 0.52 × 0.55 mm², respectively. The input and output pads were not electrostatic-discharge (ESD) protected. For the measurements, a unity-gain common-source amplifier with a 50 Ω output resistor was used as a buffer. The S-
parameters, NFs, and linearity of the LNAs were measured using on-wafer RF probes. The power consumption of each LNA and the buffer were 1.0 mW and 1.8 mW at a supply voltage of 0.5 V, respectively.

Figures 13 and 14 show the measured and simulated $S_{11}$ and $S_{21}$ of the LNAs, respectively. The proposed LNA obtained an $S_{11}$ of −14 dB and a maximum $S_{21}$ of 16.8 dB at 4.7 GHz. The magnetic coupling in the proposed LNA had a small impact on the $S_{11}$ performance, while the measured peak of $S_{21}$ was shifted to a lower frequency than the simulated one, due to the increased magnetic coupling of the fabricated transformer ($k \approx 0.2$). This frequency shift can be reduced by using a smaller $L_1$ and $L_2$ (3.4 nH).

The discrepancy between the measured and simulated $S_{21}$ is mainly attributed to insufficient accuracy in the simulation of the inductors used. The electromagnetic simulator has difficulty in simulating substrate losses in conductive silicon at high frequencies, and the simulated inductors include no metal fills in order to solve convergence problems. These factors led to the decrease in the quality factors of the inductors, resulting in a lower voltage gain.

Figure 15 shows the measured and simulated $S_{12}$ of the LNAs with the buffers. The stand-alone buffer achieved an $S_{12}$ of −30 dB around 5.0 GHz (not shown). Thus, the $S_{12}$ of the proposed LNA without the buffer was approximately −17 dB. Figure 15 also shows that the inductor coupling deteriorates the reverse isolation by a factor of 12 dB at 5 GHz, compared to the conventional LNA. This deterioration is not problematic, because the proposed LNA still has good isolation, due to the folded-cascode topology. Measurements (not shown) also showed that both the LNAs achieved an $S_{22}$ of less than −10 dB around 5.0 GHz.

Figure 16 shows the measured and simulated NFs of the LNAs. The proposed LNA obtained a minimum NF of 3.9 dB at 4.7 GHz, while the conventional LNA achieved a minimum NF of 4.1 dB at 4.7 GHz. The difference between the measured minimum NFs can be attributed to more input-referred noise of the buffer in the conventional LNA than that in the proposed LNA. The LNAs had different values of $S_{21}$ at 4.7 GHz, which resulted in different input-referred noise of the buffer.

Figure 17 shows the measured output power of the fundamental tone and third-order intermodulation (IM3) products for two tones (4.999 GHz and 5.000 GHz). The measured IIP3 of the proposed LNA with the buffer was −18.5 dBm, and that of the stand-alone buffer was
Table 1  Measured performance and comparison of low-voltage CMOS LNAs.

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$\text{FoM}[\text{mW}^{-1}] = \frac{\text{Gain[lin]}}{\text{Power[mW] \cdot (NF[lin] - 1)}}$. (31)

Among the reported low-voltage CMOS LNAs, the proposed LNA obtained the best FoM (4.8 mW⁻¹) with the smallest chip area.

6. Conclusion

We have demonstrated a transformer folded-cascode CMOS LNA, in which the internal and load inductors have been magnetically coupled to reduce the chip area. Circuit analysis showed that the magnetic coupling between these inductors decreases the resonance frequency of the input matching network, the peak frequency and magnitude of the gain, and the noise figure. The partially-coupled transformer reduced the chip area, while having a small impact on the LNA performance. The LNA, implemented with a 90 nm CMOS technology, occupied 0.21 mm², and achieved an $S_{11}$ of −14 dB, NF of 3.9 dB, and voltage gain of 16.8 dB at 4.7 GHz with a power consumption of 1.0 mW from a 0.5 V supply. It has been demonstrated that the proposed LNA can replace conventional low-voltage CMOS LNAs.

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References

Appendix A: Frequency Responses of $Y_I$ and $1/Y_I$

A.1 $Y_I$

The frequency response of $Y_I$ is shown in Fig. A.1(a). At low frequencies, Eq. (3) can be approximated as

$$\text{Re}[Y_I] \approx g_{m2}(1 - nk),$$  \hspace{1cm} (A-1) \\
$$\text{Im}[Y_I] \approx \omega (C_I + n^2 k^2 C_L) - \frac{1}{\omega L_I},$$  \hspace{1cm} (A-2) \\

which shows that $\text{Im}[Y_I]$ becomes zero around

$$\omega_{0,Y_I} = \frac{1}{\sqrt{L_I (C_I + n^2 k^2 C_L)}}. \hspace{1cm} (A-3)$$

At $\omega_{1,Y_I} = 1/\sqrt{(1-k^2)L/L_C}$, $\text{Re}[Y_I]$ exceeds $g_{m2}$ and $\text{Im}[Y_I]$ becomes a maximum:

$$\text{Re}[Y_I] \approx g_{m2} + \frac{n^2 k^2}{R_L}, \hspace{1cm} (A-4) \\
\text{Im}[Y_I] \approx \omega_{1,Y_I} C_I - \frac{1}{\omega_{1,Y_I} L_I} + \frac{n^2 k g_{m2}}{\omega_{1,Y_I} R_L C_L}, \hspace{1cm} (A-5)$$

respectively. Above $\omega_{1,Y_I}$, $\text{Re}[Y_I]$ and $\text{Im}[Y_I]$ approach gradually $g_{m2}$ and $\omega C_I - 1/\omega L_I$, respectively.

A.2 $1/Y_I$

The reverse of $Y_I$ is expressed as

$$\frac{1}{Y_I} = \frac{\frac{1}{\omega L_I}}{s C_L + \frac{1}{\omega (1-k^2)L + R_L}}, \hspace{1cm} (A-6)$$

where $D$ is given by Eq. (16). Figure A.1(b) shows the calculated frequency response of $1/Y_I$ with $k$ as a parameter. At low frequencies, $1/Y_I$ is approximated as

$$\text{Re} \left[ \frac{1}{Y_I} \right] \approx \frac{R_L}{1 + R_L g_{m2}(1 - nk)}, \hspace{1cm} (A-7) \\
\text{Im} \left[ \frac{1}{Y_I} \right] \approx 0. \hspace{1cm} (A-8)$$

Equation (16) indicates that $\text{Re}[1/Y_I]$ and $\text{Im}[1/Y_I]$ have peaks around $\omega_p$, given by Eq. (19). Above $\omega_p$, $\text{Re}[1/Y_I]$ and $\text{Im}[1/Y_I]$ approach gradually $1/g_{m2}$ and $1/\omega C_I - 1/\omega L_I$, respectively.

Appendix B: NF Derivation

The noise of $M_1$, $M_2$, $R_I$, and $R_L$ contribute to the overall LNA noise. The LNA noise factor is given by

$$F = \frac{|v_{o,R}|^2 + |v_{o,M_1}|^2 + |v_{o,M_2}|^2 + |v_{o,R,R}|^2}{|v_{o,R,R}|^2},$$

$$= 1 + F_{M_1} + F_{M_2} + F_L + F_{L_R}. \hspace{1cm} (A-9)$$

Fig. A.1  Calculated (a) $Y_I$ and (b) $1/Y_I$ with $k$ as a parameter.
where $v_{o,Rx}$, $v_{o,Mx}$, $v_{o,My}$, $v_{o,Ry}$, and $v_{o,Rz}$ are the output noise voltages originating from $R_x$, $M_1$, $M_2$, $R_I$, and $R_L$, respectively.

The output noise voltage originating from $R_x$, $v_{o,Rx}$, can be derived from the noise equivalent circuit of the input stage, shown in Fig. A.2. The signal source noise current is expressed as

$$|i_{n,Rx}|^2 = \frac{4k_BT \Delta f}{R_x},$$

(10)

where $k_B$ is Boltzmann’s constant, $T$ the absolute temperature, and $\Delta f$ the noise bandwidth. The transfer function from $i_{n,Rx}$ to the noise current at node $I$, $i_{I,Rx}$, is given by

$$H_{n,I}(j\omega) = \frac{g_{m1}R_s}{j\omega_0\alpha_M C_{gs1}(R_s + \omega_LT_s/\alpha_M)},$$

(11)

where $\text{Im}[Z_{o1}(j\omega_0)]=0$ and $\alpha_M$ is approximated as $\text{Re}[\alpha_M]$ for input impedance matching as shown in Section 3.1. Using Eq. (11), we have

$$|i_{n,Rx}|^2 = |H_{n,I}(j\omega_0)|^2 |i_{n,Rx}|^2 = \frac{4k_BT R_s \omega_0^2 \Delta f}{\omega_0^2 \alpha_M^2 (R_s + \omega_LT_s/\alpha_M)}.$$

(12)

The common-gate stage converts $i_{I,Rx}$ to the output voltage:

$$|v_{o,Rx}|^2 = |Z_T|^2 |i_{I,Rx}|^2,$$

(13)

where $Z_T$ is the transimpedance of the common-gate stage and is given by Eq. (15).

B.1 $F_{M_1}$

The noise current of $M_1$ is also converted by the common-gate stage. The noise current from $M_1$ can be expressed as

$$F_{M_1} = \frac{|v_{o,Mx}|^2}{|v_{o,Rx}|^2} = \frac{|Z_T|^2 |i_{M_1}|^2}{|Z_T|^2 |i_{R}|^2} = \frac{|i_{M_1}|^2}{|i_{R}|^2},$$

(14)

where $i_{I,M_1}$ is the noise current at node $I$ as shown in Fig. A.2.

The main noise sources in a MOSFET are the drain noise current $i_{ad}$ and induced-gate noise current $i_{ng}$, which are expressed as

$$|i_{ad}|^2 = 4k_BT \gamma g_{m1} \Delta f,$$

(15)

$$|i_{ng}|^2 = 4k_BT \delta \omega C_{gs} \Delta f,$$

(16)

respectively. The induced-gate noise current correlates to the drain noise current, and the correlation coefficient is given by [11]

$$c = \frac{\text{Im}[i_{ad}] \cdot \text{Im}[i_{ng}]}{\sqrt{|i_{ad}|^2 \sqrt{|i_{ng}|^2}},$$

(17)

Using this coefficient, we can express the induced-gate noise as

$$|i_{ng}|^2 = |i_{ad}|^2 + |i_{ngu}|^2$$

$$= |i_{ad}|^2 |c|^2 + |i_{ngu}|^2(1-|c|^2),$$

(18)

where $i_{ad}$ and $i_{ng}u$ are the correlated and uncorrelated components, respectively. The induced-gate noise current due to $M_1$ at node $I$ is therefore expressed as

$$|i_{I,M_1}|^2 = |i_{ad}|^2 + |i_{ngu}|^2$$

$$= |i_{ad}|^2 + i_{ng1}^2 + i_{ng1}^2 + i_{n1}^2 + i_{n1}^2$$

$$= |i_{ng1}|^2 + |i_{n1}|^2,$$

(19)

where $i_{n1}$, $i_{ng1}$, and $i_{n1}$ are the noise currents originating from $i_{ad}$, $i_{ng1}$, and $i_{n1}$ at node $I$, respectively. From Fig. A.2, the transfer function from $i_{ad}$ to $i_{n1}$ is approximated as

$$H_{n1}(j\omega_0) = \frac{R_s (1 + \alpha_{adj})}{\alpha_M (R_s + \omega_T L_s/\alpha_M)}.$$  

(20)

The transfer function from $i_{ng}$ to $i_{n1}$ is also approximated as

$$H_{n1}(j\omega_0) = -\frac{g_{m1} (R_s + \omega_T C_{gs})}{j\omega_0 \alpha_M C_{gs1} (R_s + \omega_T L_s/\alpha_M)},$$

(21)

Using Eqs. (15), (16), (20), and (21), we have

$$|i_{I,M_1}|^2 = |H_{n1}(j\omega_0)|^2 |i_{ad}|^2$$

$$= \frac{4k_BT \gamma g_{m1} R_s (1 + \alpha_{adj}) \Delta f}{\alpha_M |\alpha_M|^2 (R_s + \omega_T L_s/\alpha_M)^2},$$

(22)

$$|i_{n1}|^2 = H_{n1}(j\omega_0) i_{n1} = i_{n1} H_{n1}(j\omega_0)$$

$$= -2|c| \frac{\delta g_{m1} \Delta f}{\kappa_1 \gamma_1} \frac{|\alpha_M|^2 (R_s + \omega_T L_s/\alpha_M)^2}{|\alpha_M|^2 (R_s + \omega_T L_s/\alpha_M)^2}.$$  

(23)
where $M$ represents the output admittance of the input stage at node 1, and $Y_{L, C_I} = sC_I + 1/(sL_I + R_I)$, as shown in Section 3.3. Rewriting Eq. (A·13) in terms of $Y_0 + Y_I$, we have

$$\begin{align*}
|v_{o,RL}|^2 &= \left| \frac{N_{ns}}{Y_0 + Y_I} \right|^2 \frac{|Y_0 + Y_I|^2}{|H_{nm}(j\omega)|^2}, \\
N_{ns} &= \frac{sM}{sL_I + R_I} + g_{m2} \left( sL_I + R_I - \frac{s^2M^2}{sL_I + R_I} \right) \\
&\approx nk + g_{m2} \cdot sn^2(1 - k^2)L_I.
\end{align*}$$

(A·30)

Dividing Eq. (A·27) by Eq. (A·29) with $L_I = 1/\omega_0^2(1 + k)C_L$ and $n = 1$, we obtain $F_{M_2}$ (Eq. (24)).

B.3 $F_{L_I}$ and $F_{L_L}$

The noise voltages of the parasitic resistances of $L_I$ and $L_L$ are given by

$$\begin{align*}
|v_{nR_I}|^2 &= 4\pi R_I \Delta f, \\
|v_{nR_L}|^2 &= 4\pi R_L \Delta f,
\end{align*}$$

(A·31) (A·32)

respectively. The output noise voltages due to $v_{nR_I}$ and $v_{nR_L}$ can be expressed from Fig. A·3:

$$\begin{align*}
|v_{o,R_I}|^2 &= \left| \frac{N_{ns}}{Y_0 + Y_I} \right|^2 |v_{nR_I}|^2, \\
N_{ns} &= g_{m2} \left( 1 - \frac{sM}{sL_I + R_I} \right) + Y_0 + Y_{L, C_I} \\
&\approx g_{m2}(1 - nk) + Y_0 + Y_{L, C_I},
\end{align*}$$

(A·33) (A·34)

and

$$\begin{align*}
|v_{o,R_L}|^2 &= \left| \frac{N_{ns}}{Y_0 + Y_I} \right|^2 |v_{nR_L}|^2, \\
N_{ns} &= g_{m2} \left( \frac{sL_I + R_L}{sL_I + R_I} \frac{sM}{sL_I + R_I} \right) - \left( \frac{sM}{sL_I + R_I} \right) \frac{sM}{sL_I + R_I} \\
&\approx n(n - 1)g_{m2} - nk(Y_0 + sC_I),
\end{align*}$$

(A·35) (A·36)

respectively. Dividing Eqs. (A·33) and (A·35) by Eq. (A·29) with $L_I = 1/\omega_0^2(1 + k)C_L$ and $n = 1$, we derive $F_{L_I}$ (Eq. (25)) and $F_{L_L}$ (Eq. (26)), respectively.

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