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PAPER

A 0.5 V Area-Efficient Transformer Folded-Cascode CMOS Low-Noise Amplifier

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SUMMARY A 0.5 V transformer folded-cascode CMOS low-noise amplifier (LNA) is presented. The chip area of the LNA was reduced by coupling the internal inductor with the load inductor, and the effects of the magnetic coupling between these inductors were analyzed. The magnetic coupling reduces the resonance frequency of the input matching network, the peak frequency and magnitude of the gain, and the noise contributions from the common-gate stage to the LNA. A partially-coupled transformer with low magnetic coupling has a small effect on the LNA performance. The LNA with this transformer, fabricated in a 90 nm digital CMOS process, achieved an S_{11} of −14 dB, NF of 3.9 dB, and voltage gain of 16.8 dB at 4.7 GHz with a power consumption of 1.0 mW at a 0.5 V supply. The chip area of the proposed LNA was 25% smaller than that of the conventional folded-cascode LNA.

key words: *CMOS, low-noise amplifier (LNA), low voltage, transformer*

1. Introduction

Although the continuous scaling of CMOS technologies has improved the high-frequency performance of MOSFETs, it has imposed two challenges on CMOS radio-frequency integrated circuits (RFICs): low-voltage operation and a small chip area. The International Technology Roadmap for Semiconductors (ITRS) [1] predicts that the supply voltages of low-power digital circuits will decrease to 0.5 V in the near future. Reference [2] shows that a 45 nm (state-of-the-art) CMOS process costs approximately 10 times as much as a 0.13 μm (most widely used) CMOS process. Considering the integration of RF circuits with digital circuits (i.e., system-on-a-chip), we need to develop low-voltage and small-area (low-cost) RF circuits.

Low-noise amplifiers (LNAs) have difficulty in operating at low voltages with a small chip area. Cascode LNAs with inductive source degeneration [3] have been widely used for narrow band receivers, due to low-noise performance and good input impedance matching. However, this LNA is not suitable for low-voltage operation, because it requires a supply voltage of more than two drain-source saturation voltages ($V_{DD} > 2V_{DS,sat}$) to operate the cascode transistor. Although folded-cascode LNAs [4], [5] are more suitable for low voltage operation ($V_{DD} > V_{DS,sat}$), they require more inductors, which lead to an increase in the chip area. Other reported low-voltage LNAs [6], [7] consume much larger chip area than the folded-cascode LNAs, due to many inductors.

We propose a 0.5 V, 5 GHz transformer folded-cascode CMOS LNA [8], which has a smaller chip area than the conventional folded-cascode LNA. The transformer that consists of the internal and load inductors reduces the chip area of the LNA, while affecting the LNA performance. This paper is organized as follows. Section 2 describes the circuit topology of the proposed LNA. The effects of the transformer on the LNA performance are analyzed in Sect. 3. Section 4 describes the design of the LNA and transformer. Section 5 presents the measurements of the LNA implemented in a 90 nm digital CMOS technology, and Sect. 6 concludes the paper.

2. Circuit Topology

Figure 1 shows a schematic of the proposed LNA based on the conventional folded-cascode LNA with inductive source degeneration. The gate and source inductors, L_g and L_s, provide input impedance matching at an operating frequency [3]. The PMOS transistor M_2 reduces the Miller effect of the gate-drain capacitor of the input transistor M_1, and improves the reverse isolation performance of the LNA. The internal inductor L_I, resonating with the parasitic capacitance C_I at node I, provides a high impedance, thereby the signal current amplified by M_1 flows into M_2. The load inductor L_L also resonates with the parasitic capacitance C_L, resulting in a high impedance. These inductors, L_I and L_L, are magnetically coupled to form a transformer in such a way as to have a positive magnetic coupling with retaining the LNA

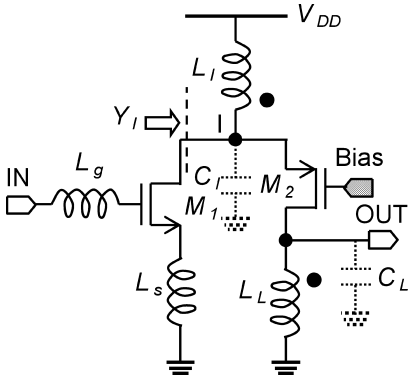

Fig. 1 Schematic of the proposed LNA.

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performance.

The positive magnetic coupling of L_I and L_L is the most effective way to reduce the chip area of the folded-cascode LNA. Increasing the magnetic coupling leads to a smaller L_I and L_L (smaller chip area), as will be shown in the next section. On the contrary, the negative magnetic coupling requires a larger L_I and L_L (larger chip area). The coupling of L_g or L_s and L_I or L_L is also not beneficial for the following reasons:

1. L_g is often implemented with a bonding wire.
2. L_s is usually small (< 1.0 nH) for input impedance matching.
3. The coupling makes the LNA unstable.

3. Effect of Magnetic Coupling

The magnetic coupling between L_I and L_L affects the LNA performance in terms of input impedance, gain, and noise. In this section, the effects of the magnetic coupling are analyzed, and the stability of the LNA is also discussed.

3.1 Input Impedance

The magnetic coupling changes the frequency response of the LNA input impedance Z_{in} through the gate-drain capacitance of M_1, C_{gd1}. The small-signal equivalent circuit of the input stage, shown in Fig. 2, yields Z_{in}, given by

$$Z_{in} \approx sL_g + \frac{\omega_{T1}L_s + sL_s + \frac{1}{sC_{gs1}}}{\alpha_M}, \tag{1}$$

$$\alpha_M = 1 + \alpha_{gd1} + \frac{\alpha_{gd1} g_{m1}}{Y_I}, \tag{2}$$

where $\omega_{T_1} = g_{m1}/C_{gs1}$ is the unity current gain frequency of M_1; $\alpha_{gd1} = C_{gd1}/C_{gs1}$ is the ratio between C_{gd1} and C_{gs1}. The input admittance of the common-gate stage, shown in Fig. 3, is given by

$$Y_I = \frac{i_i}{v_i} \approx g_{m2} + sC_I + \frac{1}{sL_I + R_I} - \frac{nk\,(g_{m2} - snkC_L)}{1 + s^2(1-k^2)L_LC_L + sR_LC_L}, \tag{3}$$

where g_{m2} is the transconductance of M_2; R_I and R_L are the parasitic resistances of L_I and L_L, respectively; k and $n = \sqrt{L_L/L_I}$ are the coupling factor and turns ratio of the transformer, respectively. The frequency responses of Y_I and $1/Y_I$ are described in Appendix A. The calculated real and imaginary parts of α_M and Z_{in} are shown in Figs. 4(a) and (b), respectively. Using $\mathrm{Re}[\alpha_M]$ and $\mathrm{Im}[\alpha_M]$, we can approximate Z_{in} as

$$\mathrm{Re}[Z_{in}] \approx \frac{\omega_{T1}L_s \cdot \mathrm{Re}[\alpha_M] - \frac{\mathrm{Im}[\alpha_M]}{\omega C_{gs1}}}{|\alpha_M|^2}, \tag{4}$$

$$\mathrm{Im}[Z_{in}] \approx \omega L_g - \frac{\omega_{T1}L_s \cdot \mathrm{Im}[\alpha_M] + \frac{\mathrm{Re}[\alpha_M]}{\omega C_{gs1}}}{|\alpha_M|^2}, \tag{5}$$

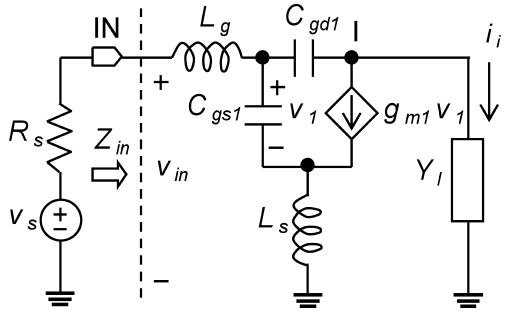

Fig. 2 Small-signal equivalent circuit of the input stage.

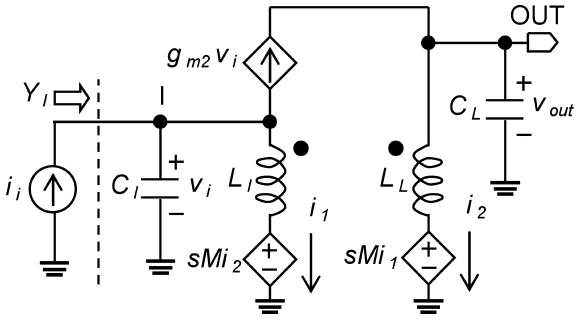

Fig. 3 Small-signal equivalent circuit of the common-gate stage.

where ωL_s is ignored against $1/\omega C_{gs1}$. As shown in Fig. 4(a), $\mathrm{Re}[\alpha_M]$ increases and $\mathrm{Im}[\alpha_M]$ decreases at low frequencies, which results in an increase of $\mathrm{Re}[Z_{in}]$. For a low k (<0.6), $\mathrm{Re}[Z_{in}]$ becomes a maximum around the frequency at which $\mathrm{Im}[\alpha_M]$ becomes a minimum. Meanwhile, $\mathrm{Im}[Z_{in}]$ with k reaches zero faster than $\mathrm{Im}[Z_{in}]$ without k ($k = 0$), due to the increase in $\mathrm{Re}[\alpha_M]$ at low frequencies.

The magnetic coupling shifts the input impedance matching region (an S_{11} of less than -10 dB) toward lower frequencies. Due to good reverse isolation of the folded-cascode topology ($S_{12} \simeq 0$), the S_{11} of the LNA can be approximated as [9]

$$S_{11} \approx \frac{Z_{in} - R_s}{Z_{in} + R_s}, \tag{6}$$

where R_s is the signal source impedance. For input impedance matching at the frequency of ω_0, the following conditions must be satisfied:

$$\mathrm{Re}[Z_{in}] \simeq R_s, \tag{7}$$

$$\mathrm{Im}[Z_{in}] \simeq 0, \tag{8}$$

$$\mathrm{Im}[\alpha_M] \simeq 0, \tag{9}$$

which give the following conditions:

$$\frac{\omega_{T1}L_s}{\mathrm{Re}[\alpha_M(j\omega_{0,\alpha_M})]} \simeq R_s, \tag{10}$$

$$\omega_0 \approx \frac{1}{\sqrt{L_gC_{gs1} \cdot \mathrm{Re}[\alpha_M(j\omega_{0,\alpha_M})]}}, \tag{11}$$

$$\omega_{0,\alpha_M} \approx \frac{1}{\sqrt{L_I(C_I + n^2k^2C_L)}}, \tag{12}$$

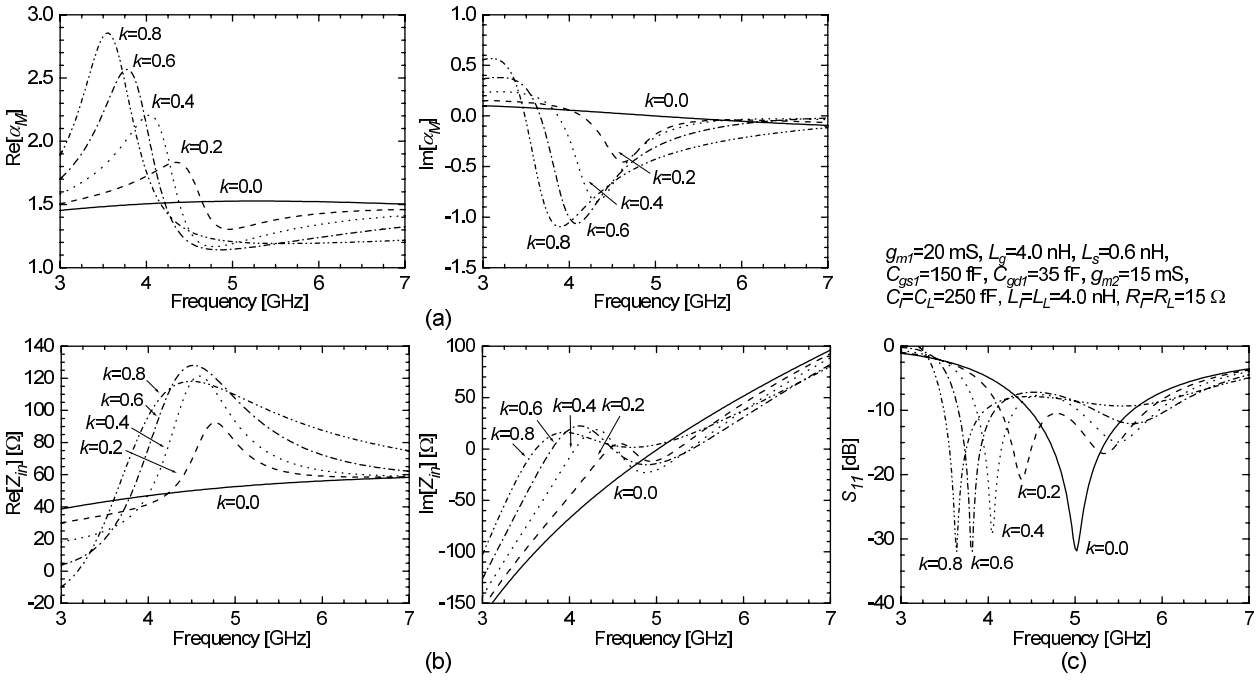

Fig. 4 Calculated (a) α_M, (b) Z_{in}, and (c) S_{11} with k as a parameter.

respectively, where $\mathrm{Re}[\alpha_M(j\omega_{0,\alpha_M})]$ is approximated as

$$\mathrm{Re}[\alpha_M(j\omega_{0,\alpha_M})] \approx 1 + \alpha_{gd1} + \frac{\alpha_{gd1} g_{m1}}{(1-nk)g_{m2}}. \tag{13}$$

Equations (10)–(13) show that the resonance frequencies of Z_{in} and α_M decrease and $\mathrm{Re}[\alpha_M]$ increases as k increases. Figure 4(c) shows the calculated S_{11} with k as a parameter. Input impedance matching is achieved around ω_0, which decreases with increasing k.

3.2 Gain

The magnetic coupling reduces the peak frequency and magnitude of the LNA gain. The common-gate stage acts as a transimpedance, which converts the input signal current i_i to the output voltage v_{out}, as shown in Fig. 3. The input current i_i amplified by the first stage is derived from Fig. 2:

$$i_i \approx -\frac{g_{m1}}{j\omega_0 C_{gs1} R_s \cdot \mathrm{Re}[\alpha_M]} v_{in}, \tag{14}$$

where input impedance matching is assumed (i.e., $Z_{in} = R_s$) and v_{in} represents the input voltage of the LNA as shown in Fig. 2. The transimpedance from node I to the output is given by

$$\begin{aligned} Z_T &= \frac{v_{out}}{i_i} = \frac{v_{out}}{v_i}\frac{v_i}{i_i} \\ &= \frac{nk + g_{m2}[R_L + s(1-k^2)L_L]}{1 + sC_L[R_L + s(1-k^2)L_L]} \cdot \frac{1}{Y_I} \\ &= \frac{\frac{nk}{R_L + s(1-k^2)L_L} + g_{m2}}{D}, \\ D &= \left(sC_I + \frac{1}{sL_I + R_I}\right)\left(sC_L + \frac{1}{s(1-k^2)L_L + R_L}\right) \\ &\quad + g_{m2}\left(sC_L + \frac{1-nk}{s(1-k^2)L_L + R_L}\right) \\ &\quad + \frac{sn^2k^2C_L}{s(1-k^2)L_L + R_L}. \end{aligned} \tag{15, 16}$$

Around $\omega = 1/\sqrt{L_I C_I} = 1/\sqrt{L_L C_L}$, the first term in Eq. (16) is approximated by zero:

$$D \approx g_{m2}\left(j\omega C_L + \frac{1-nk}{j\omega(1-k^2)L_L}\right) + \frac{n^2k^2C_L}{(1-k^2)L_L}, \tag{17}$$

where R_I and R_L are ignored for simplicity. The magnitude of Z_T becomes a maximum when the first term in Eq. (17) equals zero. The voltage gain of the LNA and its peak frequency can be therefore expressed as

$$\begin{aligned} A_{v,LNA} &= \left|\frac{v_{out}}{v_{in}}\right| \\ &= \left|\frac{i_i Z_T}{v_{in}}\right| = \left|\frac{g_{m1} Z_T}{j\omega_0 C_{gs1} R_s \cdot \mathrm{Re}[\alpha_M]}\right|, \end{aligned} \tag{18}$$

$$\omega_p \approx \frac{1}{\sqrt{\frac{1-k^2}{1-nk} L_L C_L}}, \tag{19}$$

respectively. Equations (18) and (19) show that the magnitude and peak frequency of the voltage gain decrease with increasing k. Figure 5 shows the calculated $A_{v,LNA}$ with k as a parameter. The increase of k shifts the gain peak toward a lower frequency and reduces the gain magnitude. The peak frequency in Fig. 5 corresponds well to that calculated from Eq. (19).

The LNA with the magnetic coupling sacrifices a maximum voltage gain to achieve the target peak frequency, $\omega_{p,t}$.

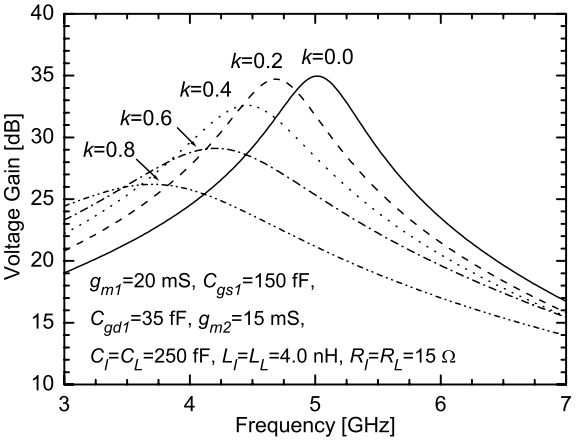

Fig. 5 Calculated voltage gain with k as a parameter.

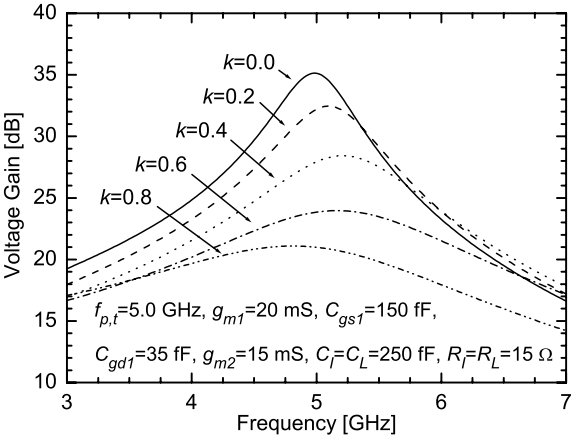

Fig. 6 Calculated voltage gain with k as a parameter for $L_L = L_I = 1/\omega_{p,t}^2(1+k)C_L$.

Equation (19) gives the following condition:

$$L_L = L_I = \frac{1}{\omega_{p,t}^2(1+k)C_L} \quad (\text{for } n = 1). \tag{20}$$

A turns ratio of one provides the smallest chip area of the transformer, because L_L and L_I simultaneously decrease with increasing k. Equation (20) shows that a smaller L_I and L_L are required to achieve $\omega_{p,t}$ as k increases. Reducing L_I and L_L leads to a smaller chip area, but to a decrease in the parallel impedances of the internal and load LC tanks at the resonance frequencies ($Z_p \approx (\omega_0 L_{I,L})^2/R_{I,L}$), causing a lower voltage gain. Figure 6 shows the calculated voltage gain for $f_{p,t} = 5.0$ GHz where L_L and L_I satisfy Eq. (20). A peak frequency of approximately 5.0 GHz can be achieved even for a large k, while the maximum gain decreases with increasing k. A small coupling factor such as 0.2, however, is acceptable for the LNA, due to a small gain reduction of 3 dB.

3.3 Noise

The transformer reduces the output noise originating from the common-gate transistor and the parasitic resistance of L_L, thereby improving the noise performance. This transformer noise reduction scheme has been reported in [10]. Figure 7 conceptually illustrates how the transformer reduces the drain noise current of M_2, represented by i_{nd2}. The primary (internal) inductor L_I detects i_{nd2}, and then induces a noise voltage to the secondary (load) inductor L_L. The induced noise voltage is correlated and anti-phase to the output noise voltage produced by i_{nd2} flowing through L_L, reducing the output noise caused by M_2. The other output noise originating from L_L is also reduced by the transformer in the same way.

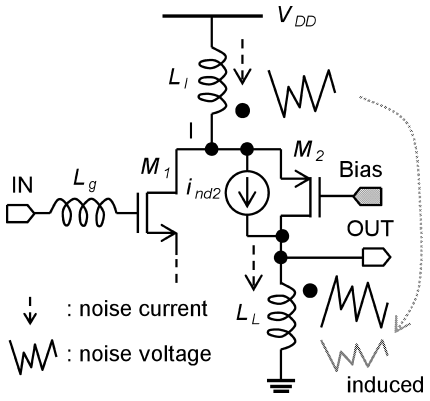

Fig. 7 Mechanisms for noise reduction of i_{nd2}.

The magnetic coupling affects the noise contributions from M_2, L_I, and L_L to the LNA (F_{M_2}, F_{L_I}, and F_{L_L}, respectively), but not that from M_1 (F_{M_1}). The LNA noise factor is given by

$$F = 1 + F_{M_1} + F_{M_2} + F_{L_I} + F_{L_L}, \tag{21}$$

$$F_{M_1} \approx \frac{\gamma_1\chi_1}{\alpha_1} g_{m1} R_s \left(\frac{\omega_0}{\omega_{T_1}}\right)^2 + \frac{\alpha_1\delta_1}{\kappa_1 g_{m1} R_s}, \tag{22}$$

$$\chi_1 = (1+\alpha_{gd1})^2 - 2|c|\alpha_1\sqrt{\frac{\delta_1}{\kappa_1\gamma_1}}(1+\alpha_{gd1}) + \frac{\alpha_1^2\delta_1}{\kappa_1\gamma_1}, \tag{23}$$

$$F_{M_2} \approx 4\left|\frac{Y_I}{Y_0+Y_I}\right|^2 \frac{\gamma_2}{\alpha_2} g_{m2} R_s \left(\frac{\omega_0}{\omega_{T_1}}\right)^2 |\alpha_M|^2 \times \left|\frac{(1-k)\left(1 - j\frac{Y_0+Y_{L_I}C_L}{\omega_0 C_L}\right)}{k + j\frac{g_{m2}(1-k)}{\omega_0 C_L}}\right|^2, \tag{24}$$

$$F_{L_I} \approx 4\left|\frac{Y_I}{Y_0+Y_I}\right|^2 R_I R_s \left(\frac{\omega_0}{\omega_{T_1}}\right)^2 |\alpha_M|^2 \times \left|\frac{(1-k)g_{m2} - k(Y_0 + j\omega_0 C_I)}{k + j\frac{g_{m2}(1-k)}{\omega_0 C_L}}\right|^2, \tag{25}$$

$$F_{L_L} \approx 4\left|\frac{Y_I}{Y_0+Y_I}\right|^2 R_L R_s \left(\frac{\omega_0}{\omega_{T_1}}\right)^2 |\alpha_M|^2 \times \left|\frac{(1-k)g_{m2} + Y_0 + Y_{L_I C_I}}{k + j\frac{g_{m2}(1-k)}{\omega_0 C_L}}\right|^2, \tag{26}$$

where $\alpha_i = g_{mi}/g_{d0i}$ and g_{d0i} is the zero bias drain conduc-

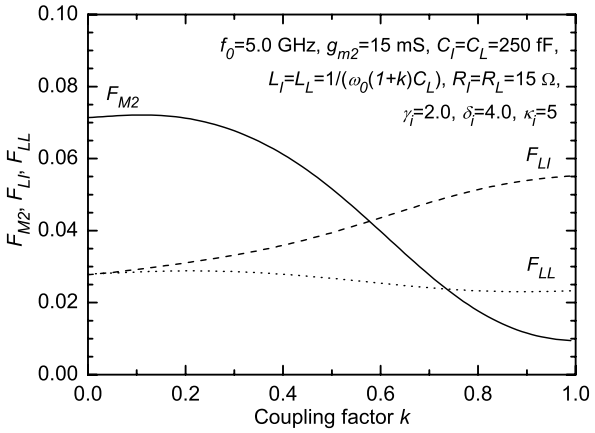

Fig. 8 Calculated F_{M_2}, F_{R_I}, and F_{R_L} versus k.

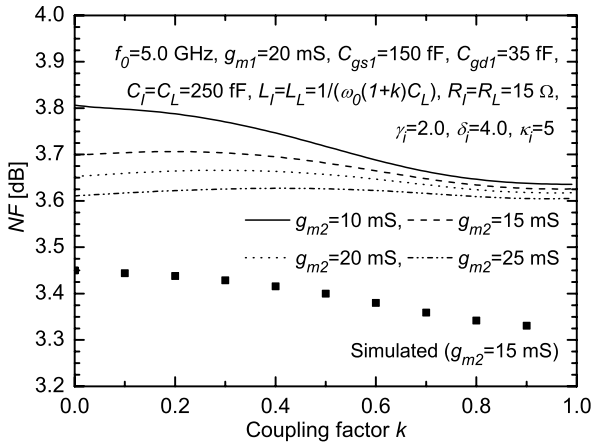

Fig. 9 Calculated and simulated NFs versus k.

tance of M_i ($i = 1, 2$); γ_i and δ_i are the drain noise current factor and the induced gate noise current factor, respectively, and c is the correlation coefficient between these noise currents ($\simeq j0.395$ [11]); κ_i is the Elmore constant (= 5 [12]); $L_I = L_L = 1/\omega_0^2(1 + k)C_L$; Y_0 represents the output admittance of the input stage at node I and is approximated as $j\omega C_{gd1}$; $Y_{L_IC_I} = j\omega C_I + 1/(j\omega L_I + R_I)$. The detailed derivations are summarized in Appendix B. Equations (22)–(26) show that F_{M_1} is independent of k while F_{M_2}, F_{L_I}, and F_{L_L} are functions of k. Figure 8 shows the calculated F_{M_2}, F_{L_I}, and F_{L_L} versus k. As Eq. (24) shows, F_{M_2} approaches zero with increasing k. Meanwhile, F_{L_I} increases and F_{L_L} slightly decreases. This difference originates from the different numerators in Eqs. (25) and (26), i.e., $-k\,(Y_0 + j\omega_0 C_I)$ and $Y_0 + Y_{L_IC_I}$.

The noise improvement by the transformer is limited in the folded-cascode topology. The calculated noise figure (NF, defined by $10 \log F$) versus k are shown in Fig. 9, where 90 nm CMOS process parameters were used. The NF simulated using Agilent Advanced Design System (ADS) are also plotted. Figure 9 shows that the calculated NF is comparable to the simulated NF, and the magnetic coupling reduces the NF by up to 0.08 dB (calculated) or 0.12 dB (simulated) for $g_{m2} = 15$ mS. The amount of noise reduction is relatively small, because the noise of M_1 is the dominant noise source in the LNA ($F_{M_1} \simeq 1.20$ and 1.05 in the calculations and simulations, respectively).

3.4 Stability

A small L_I or large C_L ensures the stability of the LNA. The proposed LNA becomes potentially unstable, because the transformer provides a positive feedback from the output to node I, as shown in Fig. 1. For stability, the LNA must satisfy the following condition [9]:

$$\mathrm{Re}[Z_{in}] > 0. \tag{27}$$

For $k = 1$ and low frequencies (the worst case), $\mathrm{Re}[Z_{in}]$ is approximated as

$$\mathrm{Re}[Z_{in}] \approx \frac{\omega_{T1}[L_s(1+\alpha_{gd1}) - L_I\alpha_{gd1}]}{(1+\alpha_{gd1})^2 + \omega^2 L_I^2 \alpha_{gd1}^2 g_{m1}^2}. \tag{28}$$

Substituting Eq. (28) in Eq. (27), we have

$$L_I < L_s\left(1 + \frac{1}{\alpha_{gd1}}\right), \tag{29}$$

which shows that a smaller L_I ensures the stability. Using Eq. (20), we can rewrite the above condition as

$$C_L > \frac{1}{2\omega_{p,t}^2 L_s\left(1 + \frac{1}{\alpha_{gd1}}\right)}. \tag{30}$$

For example, $C_L > 160$ fF is calculated from $f_{p,t} = 5$ GHz, $L_s = 0.6$ nH, and $\alpha_{gd1} = 0.2$. This capacitance value can be satisfied with the parasitic capacitances of L_L and the input capacitance of the following stage.

4. Design

The input transistor M_1 is designed to achieve a minimum NF at 5 GHz with a bias current I_{d1} of 1.0 mA at a supply voltage of 0.5 V. Equations (22) and (23) provide an optimum (for noise performance) gate width for M_1 of $4 \times 40\,\mu$m (40 gate fingers, each with a unit of $4\,\mu$m width) and a minimum gate length of 100 nm. Although the calculated minimum NF is 3.6 dB for I_{d1} =1.0 mA, increasing I_{d1} leads to a lower NF (i.e., 2.2 dB for I_{d1} =2.0 mA).

The size of the common-gate transistor M_2 is selected as a compromise between noise and linearity performance. For a fixed bias current of 1.0 mA, a small gate width of M_2 provides high linearity [13], but leads to a lower g_{m2}, which results in the increase of F_{M_2}, F_{L_I}, and F_{L_L} as shown in Eqs. (24)–(26). Figure 9 shows less NF degradation for $g_{m2} > 15$ mS than for $g_{m2} < 15$ mS at a low k. Thus, g_{m2} is selected to be approximately 15 mS, which results in a gate width of $4 \times 40\,\mu$m and gate length of 100 nm.

A partially-coupled transformer, shown in Fig. 10(a), allows us to simultaneously achieve a small chip area (0.314×0.200 mm^2) and reduce the magnetic coupling ($k \simeq$

0.1). On the other hand, a stacked transformer, shown in Fig. 10(b), provides a smaller chip area ($0.210\times0.200\,\mathrm{mm}^2$), thereby reducing the cost. However, a large k of the stacked transformer ($k \simeq 0.9$) leads to poor gain, and does not significantly reduce the LNA NF as shown in Sect. 3. Figure 11 shows the ADS simulated voltage gain and NFs of the LNAs employing the transformers shown in Fig. 10(a) and (b). The transformers were designed using a 3-D electromagnetic simulator (Ansoft HFSS), and L_s and L_g in both the LNAs were adjusted to achieve an S_{11} of less than $-10\,\mathrm{dB}$ at 5 GHz. The LNA with the stacked transformer had 13 dB lower gain than the LNA with the partially-coupled transformer at 5 GHz. This leads to an increase in the overall NF of the receiver. A larger k also leads to an increase in the voltage swing at node I (Fig. 1), causing poor reverse isolation. Simulations (not shown) showed degradation of approximately 10 dB in the reverse isolation performance (S_{12}) of the LNA with the stacked transformer.

The inductors of the transformer are designed to resonate at a frequency of approximately 5 GHz. The outer diameter of each inductor is $200\,\mu$m, the metal width $7\,\mu$m, and the metal spacing $2\,\mu$m. Electromagnetic simulations resulted in $L_I = L_L = 3.6$ nH and quality factors (Q) of 6.7 at 5 GHz.

The inductances of L_s and L_g are determined by the input impedance matching conditions, derived from Eqs. (7)–(9): $L_s \simeq 0.8$ nH and $L_g \simeq 4.3$ nH. The outer diameter of L_g is $200\,\mu$m, the metal width $5\,\mu$m, and metal spacing $2\,\mu$m. The simulated Q of L_g was 7.5 at 5 GHz.

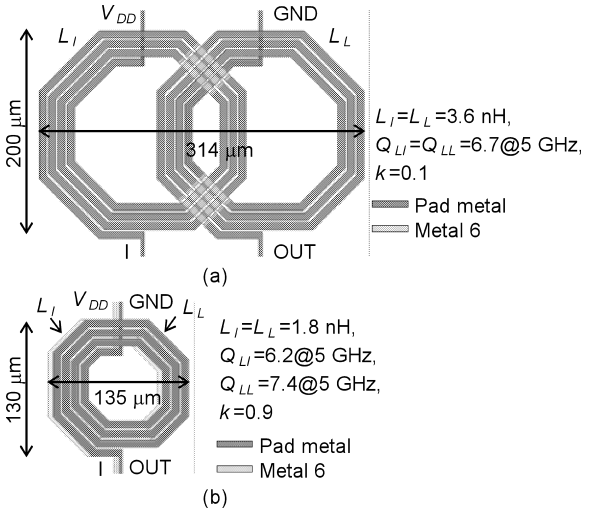

Fig. 10 Layout of (a) a partially-coupled transformer and (b) a stacked transformer.

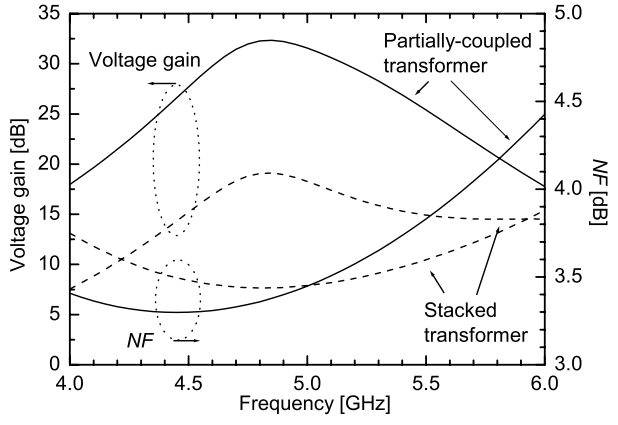

Fig. 11 Simulated voltage gain and NFs of LNAs employing the partially-coupled transformer (solid line) and stacked transformer (dashed line).

5. Experimental Results

The designed LNA with the partially-coupled transformer was fabricated in a 90 nm digital CMOS process without metal-insulator-metal (MIM) capacitors. For comparison, a conventional folded-cascode LNA was also fabricated on the same chip. A micrograph of the fabricated LNAs is shown in Fig. 12. The active chip areas (without the pads) of the proposed and conventional LNAs were $0.39\times0.55\,\mathrm{mm}^2$ and $0.52\times0.55\,\mathrm{mm}^2$, respectively. The input and output pads were not electrostatic-discharge (ESD) protected. For the measurements, a unity-gain common-source amplifier with a $50\,\Omega$ output resistor was used as a buffer. The S-

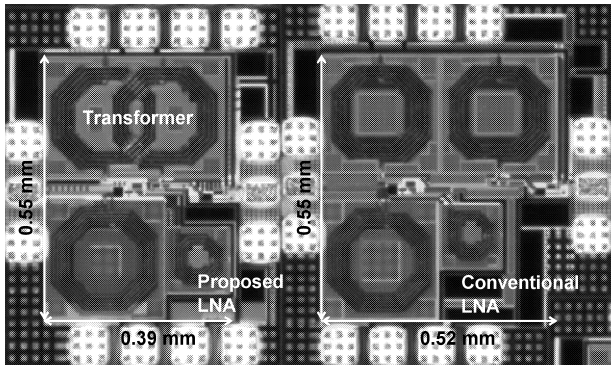

Fig. 12 Micrograph of the proposed LNA (left) and conventional folded-cascode LNA (right).

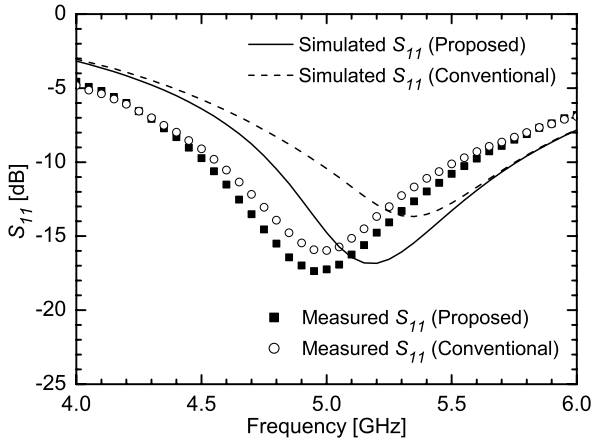

Fig. 13 Measured and simulated S_{11} of the LNAs.

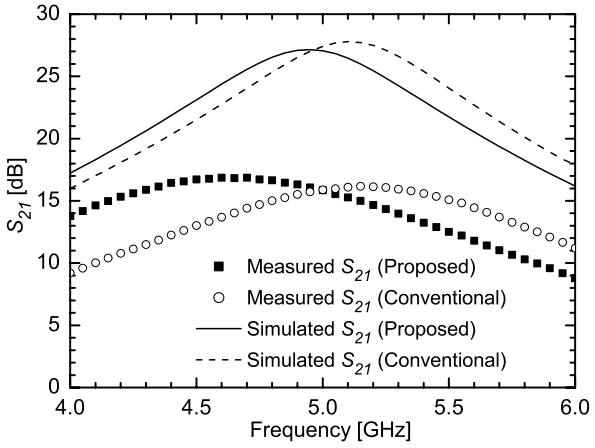

Fig. 14 Measured and simulated S_{21} of the LNAs.

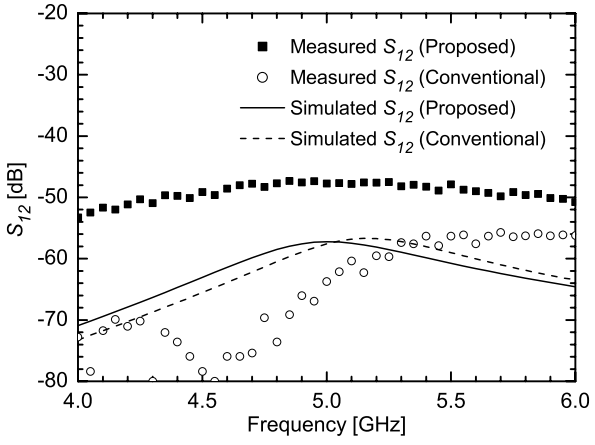

Fig. 15 Measured and simulated S_{12} of the LNAs.

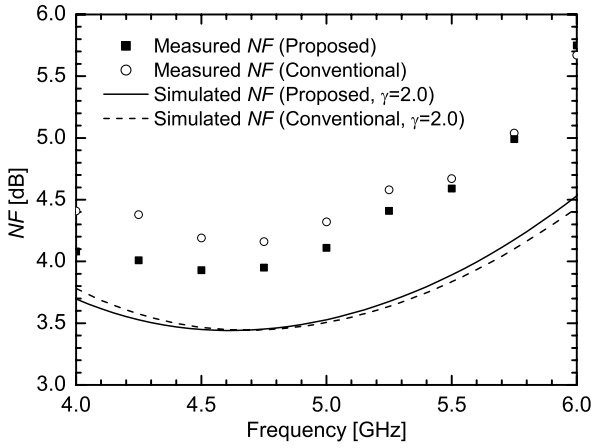

Fig. 16 Measured and simulated NFs of the LNAs.

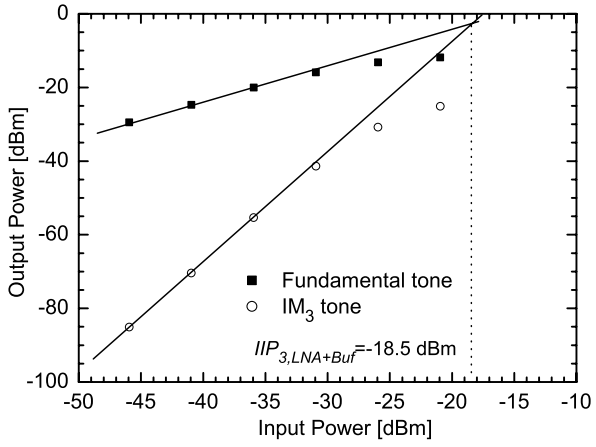

Fig. 17 Measured IIP_3 of the proposed LNA with the buffer.

parameters, NFs, and linearity of the LNAs were measured using on-wafer RF probes. The power consumption of each LNA and the buffer were 1.0 mW and 1.8 mW at a supply voltage of 0.5 V, respectively.

Figures 13 and 14 show the measured and simulated S_{11} and S_{21} of the LNAs, respectively. The proposed LNA obtained an S_{11} of -14 dB and a maximum S_{21} of 16.8 dB at 4.7 GHz. The magnetic coupling in the proposed LNA had a small impact on the S_{11} performance, while the measured peak of S_{21} was shifted to a lower frequency than the simulated one, due to the increased magnetic coupling of the fabricated transformer ($k \simeq 0.2$). This frequency shift can be reduced by using a smaller L_I and L_L (3.4 nH).

The discrepancy between the measured and simulated S_{21} is mainly attributed to insufficient accuracy in the simulation of the inductors used. The electromagnetic simulator has difficulty in simulating substrate losses in conductive silicon at high frequencies, and the simulated inductors include no metal fills in order to solve convergence problems. These factors led to the decrease in the quality factors of the inductors, resulting in a lower voltage gain.

Figure 15 shows the measured and simulated S_{12} of the LNAs with the buffers. The stand-alone buffer achieved an S_{12} of -30 dB around 5.0 GHz (not shown). Thus, the S_{12} of the proposed LNA without the buffer was approximately -17 dB. Figure 15 also shows that the inductor coupling deteriorates the reverse isolation by a factor of 12 dB at 5 GHz, compared to the conventional LNA. This deterioration is not problematic, because the proposed LNA still has good isolation, due to the folded-cascode topology. Measurements (not shown) also showed that both the LNAs achieved an S_{22} of less than -10 dB around 5.0 GHz.

Figure 16 shows the measured and simulated NFs of the LNAs. The proposed LNA obtained a minimum NF of 3.9 dB at 4.7 GHz, while the conventional LNA achieved a minimum NF of 4.1 dB at 4.7 GHz. The difference between the measured minimum NFs can be attributed to more input-referred noise of the buffer in the conventional LNA than that in the proposed LNA. The LNAs had different values of S_{21} at 4.7 GHz, which resulted in different input-referred noise of the buffer.

Figure 17 shows the measured output power of the fundamental tone and third-order intermodulation (IM_3) products for two tones (4.999 GHz and 5.000 GHz). The measured IIP_3 of the proposed LNA with the buffer was -18.5 dBm, and that of the stand-alone buffer was

Table 1 Measured performance and comparison of low-voltage CMOS LNAs.

Reference	CMOS Technology	Frequency [GHz]	NF [dB]	Gain [dB]	IIP_3 [dBm]	$P_{in\text{-}1\,dB}$ [dBm]	Supply [V]	Power [mW]	Area [mm^2]	FoM [mW^{-1}]
This work	90 nm	4.7	3.9	16.8	−14.8	−27	0.5	1.0	0.21	4.8
Folded-cascode LNA	90 nm	5.0	4.1	16.1	−14.8	−27	0.5	1.0	0.29	4.1
[4]	90 nm	5.5	3.6	9.2	−7.25	−15.8	0.6	1.0	0.30	2.2
[5]	180 nm	5.8	2.9	7.0	N/A	−9	0.7	12.5	0.40	0.2
[6]	130 nm	5.1	5.3	10.3	N/A	−22	0.4	1.0	0.75	1.4
[7]	180 nm	5.0	4.5	9.2	−16	−27	0.6	0.9	0.54	1.8
[14]	180 nm	5.0	3.65	14.1	−17.1	−25	0.6	1.68	0.46	2.3

−0.25 dBm. Following the de-embedding procedure shown in [13], we can calculate the IIP_3 of the LNA without the buffer as −14.8 dBm. The IIP_3 of the conventional LNA was also −14.8 dBm.

Table 1 shows a summary of the LNA performance and a comparison with previously reported low-voltage (approximately 0.6 V) CMOS LNAs for 5 GHz applications. The proposed LNA achieved performance comparable to the conventional folded-cascode LNA, while consuming three fourths of the chip area of the conventional LNA. The figure of merit (FoM) for the LNAs, included in Table 1, is defined as [4]

$$FoM[\mathrm{mW}^{-1}] = \frac{Gain[\mathrm{lin}]}{Power[\mathrm{mW}]\cdot(NF[\mathrm{lin}]-1)}. \quad (31)$$

Among the reported low-voltage CMOS LNAs, the proposed LNA obtained the best FoM ($4.8\,\mathrm{mW}^{-1}$) with the smallest chip area

6. Conclusion

We have demonstrated a transformer folded-cascode CMOS LNA, in which the internal and load inductors have been magnetically coupled to reduce the chip area. Circuit analysis showed that the magnetic coupling between these inductors decreases the resonance frequency of the input matching network, the peak frequency and magnitude of the gain, and the noise figure. The partially-coupled transformer reduced the chip area, while having a small impact on the LNA performance. The LNA, implemented with a 90 nm CMOS technology, occupied 0.21 mm^2, and achieved an S_{11} of −14 dB, NF of 3.9 dB, and voltage gain of 16.8 dB at 4.7 GHz with a power consumption of 1.0 mW from a 0.5 V supply. It has been demonstrated that the proposed LNA can replace conventional low-voltage CMOS LNAs.

Acknowledgments

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Appendix A: Frequency Responses of Y_I and $1/Y_I$

A.1 Y_I

The frequency response of Y_I is shown in Fig. A· 1(a). At low frequencies, Eq. (3) can be approximated as

$$\mathrm{Re}[Y_I] \approx g_{m2}(1 - nk), \tag{A· 1}$$

$$\mathrm{Im}[Y_I] \approx \omega\left(C_I + n^2k^2C_L\right) - \frac{1}{\omega L_I}, \tag{A· 2}$$

which shows that $\mathrm{Im}[Y_I]$ becomes zero around

$$w_{0,Y_I} = \frac{1}{\sqrt{L_I\left(C_I + n^2k^2C_L\right)}}. \tag{A· 3}$$

At $\omega_{1,Y_I} = 1/\sqrt{(1-k^2)L_LC_L}$, $\mathrm{Re}[Y_I]$ exceeds g_{m2} and $\mathrm{Im}[Y_I]$ becomes a maximum:

$$\mathrm{Re}[Y_I] \approx g_{m2} + \frac{n^2k^2}{R_L}, \tag{A· 4}$$

$$\mathrm{Im}[Y_I] \approx \omega_{1,Y_I}C_I - \frac{1}{\omega_{1,Y_I}L_I} + \frac{nkg_{m2}}{\omega_{1,Y_I}R_LC_L}, \tag{A· 5}$$

respectively. Above ω_{1,Y_I}, $\mathrm{Re}[Y_I]$ and $\mathrm{Im}[Y_I]$ approach gradually g_{m2} and $\omega C_I - 1/\omega L_I$, respectively.

A.2 $1/Y_I$

The reverse of Y_I is expressed as

$$\frac{1}{Y_I} = \frac{sC_L + \frac{1}{s(1-k^2)L_L + R_L}}{D}, \tag{A· 6}$$

where D is given by Eq. (16). Figure A· 1(b) shows the calculated frequency response of $1/Y_I$ with k as a parameter. At low frequencies, $1/Y_I$ is approximated as

$$\mathrm{Re}\left[\frac{1}{Y_I}\right] \approx \frac{R_I}{1 + R_Ig_{m2}(1 - nk)}, \tag{A· 7}$$

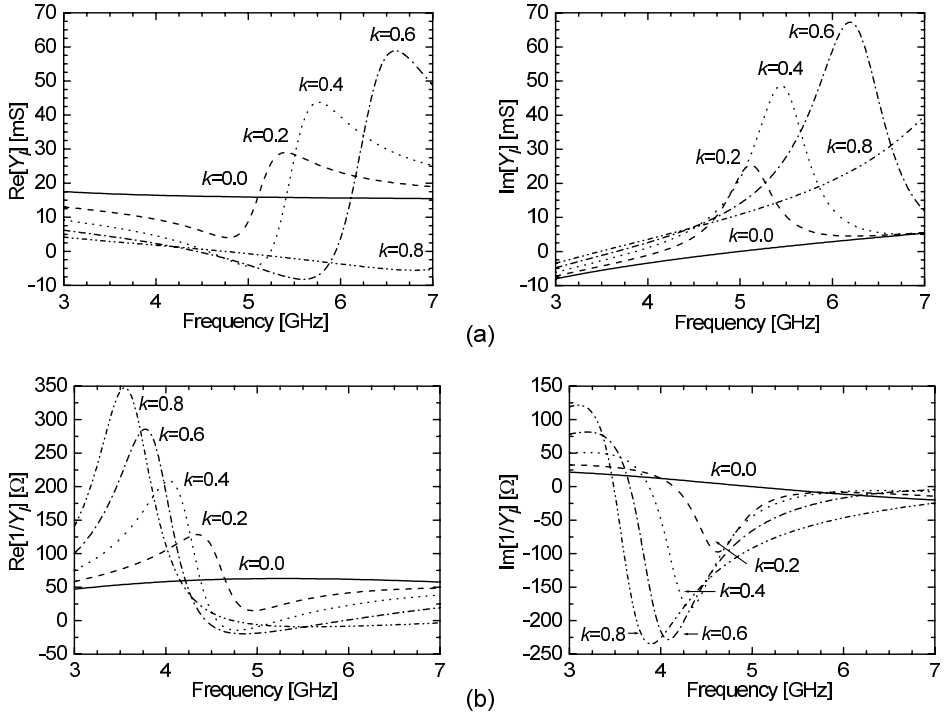
$$\mathrm{Im}\left[\frac{1}{Y_I}\right] \approx 0. \tag{A· 8}$$

Equation (16) indicates that $\mathrm{Re}[1/Y_I]$ and $\mathrm{Im}[1/Y_I]$ have peaks around ω_p, given by Eq. (19). Above ω_p, $\mathrm{Re}[1/Y_I]$ and $\mathrm{Im}[1/Y_I]$ approach gradually $1/g_{m2}$ and $1/(\omega C_I - 1/\omega L_I)$, respectively.

Appendix B: NF Derivation

The noise of M_1, M_2, R_I, and R_L contribute to the overall LNA noise. The LNA noise factor is given by

$$F = \frac{\overline{|v_{o,R_s}|^2} + \overline{|v_{o,M_1}|^2} + \overline{|v_{o,M_2}|^2} + \overline{|v_{o,R_I}|^2} + \overline{|v_{o,R_L}|^2}}{\overline{|v_{o,R_s}|^2}},$$
$$= 1 + F_{M_1} + F_{M_2} + F_{L_I} + F_{L_L}, \tag{A· 9}$$



g_{m1}=20 mS, L_g=4.0 nH, L_s=0.6 nH, C_{gs1}=150 fF, C_{gd1}=35 fF, g_{m2}=15 mS, C_I=C_L=250 fF, L_I=L_L=4.0 nH, R_I=R_L=15 Ω

Fig. A· 1 Calculated (a) Y_I and (b) $1/Y_I$ with k as a parameter.

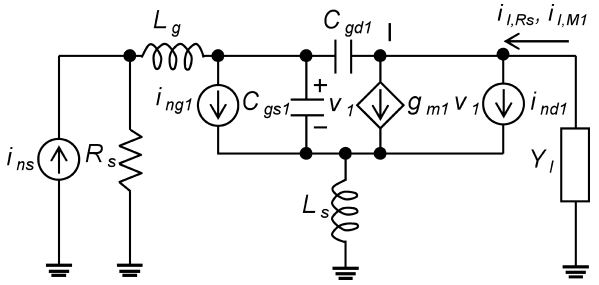


Fig. A· 2 Noise equivalent circuit of the input stage.

where v_{o,R_s}, v_{o,M_1}, v_{o,M_2}, v_{o,R_I}, and v_{o,R_L} are the output noise voltages originating from R_s, M_1, M_2, R_I, and R_L, respectively.

The output noise voltage originating from R_s, v_{o,R_s}, can be derived from the noise equivalent circuit of the input stage, shown in Fig. A· 2. The signal source noise current is expressed as

$$\overline{|i_{ns}|^2} = \frac{4k_BT\Delta f}{R_s}, \tag{A· 10}$$

where k_B is Boltzmann's constant, T the absolute temperature, and Δf the noise bandwidth. The transfer function from i_{ns} to the noise current at node I, $i_{I,Rs}$, is given by

$$H_{ns}(j\omega_0) = \frac{g_{m1}R_s}{j\omega_0\alpha_M C_{gs1}\,(R_s+\omega_T L_s/\alpha_M)}, \tag{A· 11}$$

where $\mathrm{Im}[Z_{in}(j\omega_0)]=0$ and α_M is approximated as $\mathrm{Re}[\alpha_M]$ for input impedance matching as shown in Section 3.1. Using Eq. (A· 11), we have

$$\begin{aligned}\overline{|i_{I,Rs}|^2} &= |H_{ns}(j\omega_0)|^2\,\overline{|i_{ns}|^2}\\ &= \frac{4k_BTR_s\omega_{T1}^2\Delta f}{\omega_0^2|\alpha_M|^2(R_s+\omega_T L_s/|\alpha_M|)^2}.\end{aligned} \tag{A· 12}$$

The common-gate stage converts $i_{I,Rs}$ to the output voltage:

$$\overline{|v_{o,Rs}|^2} = |Z_T|^2\,\overline{|i_{I,Rs}|^2}, \tag{A· 13}$$

where Z_T is the transimpedance of the common-gate stage and is given by Eq. (15).

B.1 F_{M_1}

The noise current of M_1 is also converted by the common-gate stage. The noise contribution from M_1 can be expressed as

$$F_{M_1} = \frac{\overline{|v_{o,M_1}|^2}}{\overline{|v_{o,R_s}|^2}} = \frac{|Z_T|^2\overline{|i_{I,M_1}|^2}}{|Z_T|^2\overline{|i_{I,R_s}|^2}} = \frac{\overline{|i_{I,M_1}|^2}}{\overline{|i_{I,R_s}|^2}}, \tag{A· 14}$$

where i_{I,M_1} is the noise current at node I as shown in Fig. A· 2.

The main noise sources in a MOSFET are the drain noise current i_{nd} and induced-gate noise current i_{ng}, which are expressed as

$$\overline{|i_{nd}|^2} = 4k_BT\gamma g_{d0}\Delta f, \tag{A· 15}$$

$$\overline{|i_{ng}|^2} = 4k_BT\delta\frac{(\omega C_{gs})^2}{\kappa g_{d0}}\Delta f, \tag{A· 16}$$

respectively. The induced-gate noise current correlates to the drain noise current, and the correlation coefficient is given by [11]

$$c = \frac{\overline{i_{ng}\cdot i_{nd}^*}}{\sqrt{\overline{|i_{ng}|^2}}\sqrt{\overline{|i_{nd}|^2}}}. \tag{A· 17}$$

Using this coefficient, we can express the induced-gate noise as

$$\begin{aligned}\overline{|i_{ng}|^2} &= \overline{|i_{ngc}|^2} + \overline{|i_{ngu}|^2}\\ &= \overline{|i_{ng}|^2}|c|^2 + \overline{|i_{ng}|^2}(1-|c|^2),\end{aligned} \tag{A· 18}$$

where i_{ngc} and i_{ngu} are the correlated and uncorrelated components, respectively. The noise current due to M_1 at node I is therefore expressed as

$$\begin{aligned}\overline{|i_{I,M_1}|^2} &= \overline{|i_{I,nd1}+i_{I,ng1}|^2}\\ &= \overline{|i_{I,nd1}+i_{I,ngc1}|^2} + \overline{|i_{I,ngu1}|^2}\\ &= \overline{|i_{I,nd1}|^2} + \overline{i_{I,ngc1}\cdot i_{I,nd1}^*} + \overline{i_{I,nd1}\cdot i_{I,ngc1}^*}\\ &\quad + \overline{|i_{I,ngc1}|^2} + \overline{|i_{I,ngu1}|^2},\end{aligned} \tag{A· 19}$$

where $i_{I,nd1}$, $i_{I,ngc1}$, and $i_{I,ngu1}$ are the noise currents originating from i_{nd1}, i_{ngc1}, and i_{ngu1} at node I, respectively. From Fig. A· 2, the transfer function from i_{nd1} to $i_{I,nd1}$ is approximated as

$$H_{nd1}(j\omega_0) \approx \frac{R_s\left(1+\alpha_{gd1}\right)}{\alpha_M\,(R_s+\omega_{T1}L_s/\alpha_M)}. \tag{A· 20}$$

The transfer function from i_{ng1} to $i_{I,ng1}$ is also approximated as

$$H_{ng1}(j\omega_0) \approx -\frac{g_{m1}\left(R_s+\frac{j}{\omega_0 C_{gs1}}\right)}{j\omega_0\alpha_M C_{gs1}\,(R_s+\omega_{T1}L_s/\alpha_M)}. \tag{A· 21}$$

Using Eqs. (A· 15), (A· 16), (A· 20), and (A· 21), we have

$$\begin{aligned}\overline{|i_{I,nd1}|^2} &= |H_{nd1}(j\omega_0)|^2\,\overline{|i_{nd1}|^2}\\ &= \frac{4k_BT\gamma_1 g_{m1}R_s^2\left(1+\alpha_{gd1}\right)^2\Delta f}{\alpha_1|\alpha_M|^2(R_s+\omega_{T1}L_s/|\alpha_M|)^2},\end{aligned} \tag{A· 22}$$

$$\begin{aligned}&\overline{i_{I,ngc1}\cdot i_{I,nd1}^*} + \overline{i_{I,nd1}\cdot i_{I,ngc1}^*}\\ &= H_{ngc1}(j\omega_0)i_{ngc1}\cdot H_{nd1}^*(j\omega_0)i_{nd1}^*\\ &\quad + H_{nd1}(j\omega_0)i_{nd1}\cdot H_{ngc1}^*(j\omega_0)i_{ngc1}^*\\ &= -2|c|\sqrt{\frac{\delta_1}{\kappa_1\gamma_1}}\frac{4k_BT\gamma_1 g_{m1}R_s^2\left(1+\alpha_{gd1}\right)\Delta f}{|\alpha_M|^2(R_s+\omega_{T1}L_s/|\alpha_M|)^2},\end{aligned} \tag{A· 23}$$

$$\overline{|i_{I,ngc1}|^2} + \overline{|i_{I,ngu1}|^2}$$

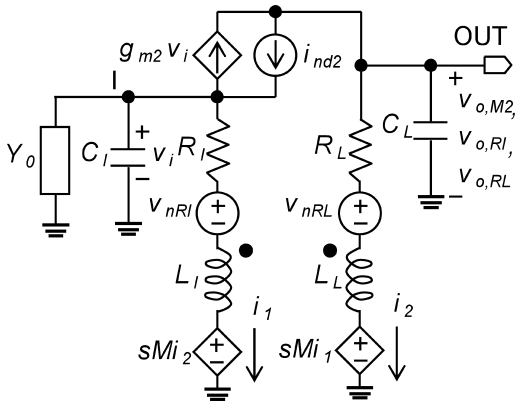


Fig. A·3 Noise equivalent circuit of the common-gate stage.

$$= \left|H_{ng1}(j\omega_0)\right|^2 \overline{|i_{ng1}|^2}$$
$$= \frac{4k_BT\alpha_1\delta_1 g_{m1}\left(R_s^2 + \frac{1}{\omega_0^2 C_{gs1}^2}\right)\Delta f}{\kappa_1|\alpha_M|^2(R_s + \omega_{T1}L_s/|\alpha_M|)^2}. \quad (A\cdot 24)$$

Substituting Eqs. (A· 22)–(A· 24) into Eq. (A· 19) gives the noise current of M_1 at node I:

$$\overline{|i_{I,M_1}|^2} = \frac{4k_BTR_s\Delta f}{|\alpha_M|^2(R_s + \omega_{T1}L_s/|\alpha_M|)^2} \times\left(\frac{\gamma_1\chi_1}{\alpha_1}g_{m1}R_s + \frac{\alpha_1\delta_1 g_{m1}}{\kappa_1\omega_0^2 C_{gs1}^2 R_s}\right), \quad (A\cdot 25)$$

where χ_1 is given by Eq. (23). Substituting Eqs. (A· 12) and (A· 25) into Eq. (A· 14) gives F_{M_1} (Eq. (22)).

B.2 F_{M_2}

In a common-gate topology, the gate-induced noise current of the MOSFET can be ignored against the drain noise current:

$$\overline{|v_{o,M_2}|^2} \approx \overline{|v_{o,nd2}|^2}, \quad (A\cdot 26)$$

where $v_{o,nd2}$ is the output voltage originating from the drain noise current of M_2, i_{nd2}, and is derived from the noise equivalent circuit of the common-gate stage, shown in Fig. A· 3:

$$\overline{|v_{o,nd2}|^2} = \left|\frac{N_{nd2}}{Y_0 + Y_I}\right|^2 \overline{|i_{nd2}|^2}$$
$$= \left|\frac{N_{nd2}}{Y_0 + Y_I}\right|^2 \cdot 4k_BT\frac{\gamma_2}{\alpha_2}g_{m2}\Delta f, \quad (A\cdot 27)$$
$$N_{nd2} = -\left(sL_L + R_L - \frac{s^2M^2}{sL_I + R_I}\right)(Y_0 + Y_{L_IC_I}) + \frac{sM}{sL_I + R_I}\left(1 - \frac{sM}{sL_I + R_I}\right)$$
$$\approx -sn^2(1-k^2)L_I\cdot(Y_0 + Y_{L_IC_I}) + nk(1-nk), \quad (A\cdot 28)$$

where M is the mutual inductance between L_I and L_L, Y_0 represents the output admittance of the input stage at node I, and $Y_{L_IC_I} = sC_I + 1/(sL_I + R_I)$, as shown in Section 3.3. Rewriting Eq. (A· 13) in terms of $Y_0 + Y_I$, we have

$$\overline{|v_{o,Rs}|^2} = \left|\frac{N_{ns}}{Y_0 + Y_I}\right|^2 \left|\frac{Y_0 + Y_I}{Y_I}\right|^2 \overline{|i_{I,Rs}|^2}, \quad (A\cdot 29)$$
$$N_{ns} = \frac{sM}{sL_I + R_I} + g_{m2}\left(sL_L + R_L - \frac{s^2M^2}{sL_I + R_I}\right) \approx nk + g_{m2}\cdot sn^2(1-k^2)L_I. \quad (A\cdot 30)$$

Dividing Eq. (A· 27) by Eq. (A· 29) with $L_I = 1/\omega_0^2(1+k)C_L$ and $n = 1$, we obtain F_{M_2} (Eq. (24)).

B.3 F_{L_I} and F_{L_L}

The noise voltages of the parasitic resistances of L_I and L_L are given by

$$\overline{|v_{nR_I}|^2} = 4k_BTR_I\Delta f, \quad (A\cdot 31)$$
$$\overline{|v_{nR_L}|^2} = 4k_BTR_L\Delta f, \quad (A\cdot 32)$$

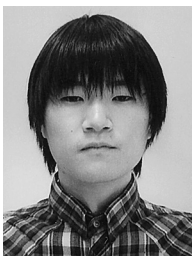
respectively. The output noise voltages due to v_{nR_I} and v_{nR_L} can be expressed from Fig. A· 3:

$$\overline{|v_{o,R_L}|^2} = \left|\frac{N_{nR_L}}{Y_0 + Y_I}\right|^2 \overline{|v_{nR_L}|^2}, \quad (A\cdot 33)$$
$$N_{nR_L} = g_{m2}\left(1 - \frac{sM}{sL_I + R_I}\right) + Y_0 + Y_{L_IC_I} \approx g_{m2}(1-nk) + Y_0 + Y_{L_IC_I} \quad (A\cdot 34)$$

and

$$\overline{|v_{o,R_I}|^2} = \left|\frac{N_{nR_I}}{Y_0 + Y_I}\right|^2 \overline{|v_{nR_I}|^2} \quad (A\cdot 35)$$
$$N_{nR_I} = g_{m2}\left(\frac{sL_L + R_L}{sL_I + R_I} - \frac{sM}{sL_I + R_I}\right) - \frac{sM}{sL_I + R_I}(Y_0 + sC_I) \approx n(n-k)g_{m2} - nk(Y_0 + sC_I), \quad (A\cdot 36)$$

respectively. Dividing Eqs. (A· 33) and (A· 35) by Eq. (A· 29) with $L_I = 1/\omega_0^2(1+k)C_L$ and $n = 1$, we derive F_{L_I} (Eq. (25)) and F_{L_L} (Eq. (26)), respectively.



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