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# Watch-Dog Circuit for Quality Guarantee with Subthreshold MOSFET Current

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**SUMMARY** We propose an ultra low power watch-dog circuit with the use of MOSFET's operation under subthreshold characteristics. The circuit monitors the amount of the product degradation because the subthreshold current of MOSFET emulates the rate of the general chemical reaction. Its operation was verified with both SPICE simulation and the measurement of the prototype chip. The new circuit embedded in a tag attached to any product could dynamically monitor the degradation regardless of storage conditions.

**key words:** CMOS, subthreshold current, ultra-low-power, temperature dependence

## 1. Introduction

We developed a new electronic circuit to monitor the expiration date of consumer products such as medical goods, farm products, foods, beverages, and so on. In general, the expiration date is carefully specified to guarantee their quality before shipping. However, it is not appropriate to fix the expiration date in advance without knowing their preservation conditions. Degradation of any consumer product should be monitored with an ultra-low-power circuit directly attached to the consumer product. The idea of the expiration date checker originates from the fact that the rate of material degradation is expressed with a rate equation regardless of their mechanisms such as chemical reaction and biological proliferation. The circuitry attached to each product can monitor its real quality by emulating the amount of degradation based on the activation energy even if its preservation condition dynamically changes.

## 2. Overview

Materials are degraded based on the thermal chemical reaction [1]; materials  $A$  and  $B$  react, and then unwanted material  $C$  generates. This reaction is expressed as the following equation.



According to this reaction, a rate equation can be given by

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$$\frac{d[C]}{dt} = k[A][B] = [A][B]k_0 \exp\left(-\frac{\Delta E_a}{k_B T(t)}\right) \quad (2)$$

where  $[A]$  and  $[B]$  are the concentrations of the reactants, and  $[C]$  is that of the produced unwanted material. The rate constant,  $k$ , is given by the pre-exponential factor,  $k_0$ , and the activation energy,  $\Delta E_a$  for the reaction.  $k_B$  is the Boltzmann constant and  $T$  the absolute temperature. Integrating the equation from  $t = 0$  to  $t = t_1$ , one can derive the concentration of the unwanted product  $[C]$  as

$$[C] = [A]_0[B]_0 k_0 \int_0^{t_1} \exp\left(-\frac{\Delta E_a}{k_B T(t)}\right) dt \quad (3)$$

where the  $[A]_0$  and  $[B]_0$  are the initial concentrations of the materials,  $A$  and  $B$ . Among many parameters only temperature ( $T(t)$ ) is a function of time so that the amount of degradation is greatly affected by its thermal history.

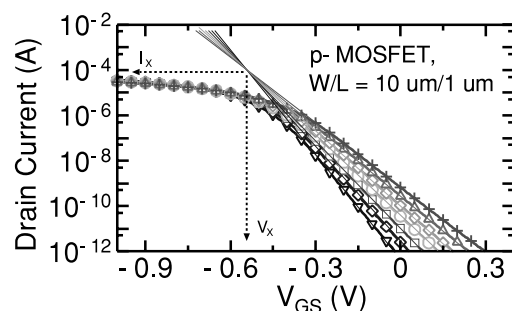
### 2.1 Principle of Circuit Operation

We developed a circuit which emulates the degradation of materials by integrating the subthreshold leakage current of MOSFET whose activation energy is exactly the same as that of the products to be monitored.

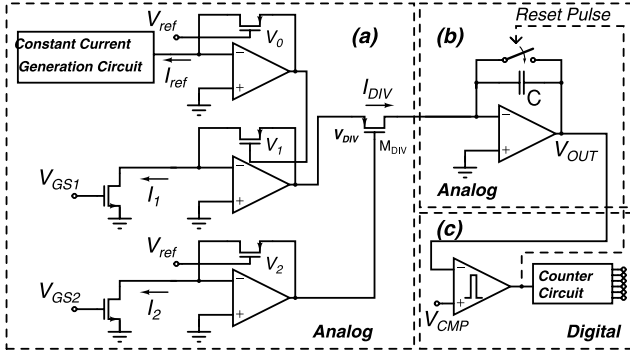
Figure 1 shows the measurement result of the  $V_{GS}$ - $I_D$  characteristics. The subthreshold drain current of MOSFET is expressed as

$$I_D = I_X \exp\left(\frac{e(V_{GS} - V_X)}{\eta k_B T}\right) \quad (4)$$

where  $I_X$  and  $V_X$  are temperature-independent but process-dependent parameters, and  $\eta$  the subthreshold slope factor.



**Fig. 1** Measurement results of p-MOSFET  $V_{GS}$ - $I_D$  characteristics at different temperatures from  $-20^\circ\text{C}$  to  $100^\circ\text{C}$ .  $W/L = 10\mu\text{m}/1\mu\text{m}$ ,  $V_{DS} = 100\text{mV}$ .  $V_X$  and  $I_X$  are independent parameter on temperature.



**Fig. 2** Block diagram of the circuit. (a) The current divider, (b) the integrator, and (c) the comparator and digital counter circuit.

The ratio of two subthreshold currents,  $I_{D1}$ , and  $I_{D2}$  can mimic the activation energy as

$$\frac{I_{D1}}{I_{D2}} = \exp\left(-\frac{e(V_{GS,2} - V_{GS,1})}{\eta k_B T}\right) = \exp\left(-\frac{\Delta E}{k_B T}\right) \quad (5)$$

$$\Delta E = \frac{e(V_{GS,2} - V_{GS,1})}{\eta} \quad (6)$$

where  $V_{GS,1}$  and  $V_{GS,2}$  are the input gate-source voltages of the subthreshold currents  $I_{D1}$  and  $I_{D2}$ , respectively, and  $\Delta E$  is the emulated activation energy. Integrating the equation with time, one obtains the following equation.

$$\int_0^{t_1} \left(\frac{I_{D1}}{I_{D2}}\right) dt = \int_0^{t_1} \exp\left(-\frac{\Delta E}{k_B T(t)}\right) dt \quad (7)$$

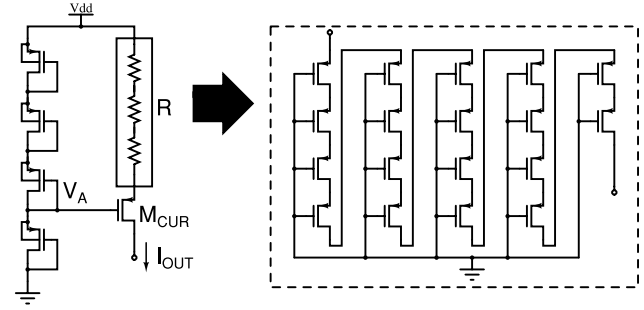
which is proportional to the right-hand side of Eq. (3). At given voltages  $V_{GS,1}$  and  $V_{GS,2}$ , the temperature  $T$  is the only variable with time. The degradation rate of the material can be monitored from the integrated value.

In order to achieve high portability, we adopt the use of a button type battery with the nominal voltage of 1.5 V. Figure 2 shows the whole circuitry consisting of the bias circuit, current dividers, integrator, comparator and digital counter. The whole analog elements work at subthreshold region to achieve ultra low power consumption.

## 2.2 Constant Current Generation Circuit

In the ultra low power circuit, the bias current should be kept constant even in wide temperature change. Figure 3 shows the reference circuit designed. The reference voltage is generated from the four diode connected p-MOSFETs placed in four separate n-wells with their bodies connected to the sources. The circuit generates the reference voltage,  $V_A$ , with very little temperature dependence. A p-channel MOS transistor  $M_{CUR}$  with a large source resistance biased at the voltage  $V_A$  yields the reference current,  $I_{OUT}$ , given by

$$I_{OUT} = I_X \exp\left(\frac{e(V_{DD} - I_D R - V_A - V_X)}{\eta k_B T}\right) \quad (8)$$



**Fig. 3** Constant current generation circuit consisting of four-diode connected p-MOSFETs, a p-MOSFET  $M_{CUR}$ , and the 18 p-MOSFETs. Each 18 p-MOSFETs operate in deep triode region.

**Table 1** Simulation result of the constant current generation circuit shown in Fig. 3.

| Temperature (°C) | -25  | 0    | 25   | 50   | 75   |
|------------------|------|------|------|------|------|
| $I_{OUT}$ (nA)   | 8.27 | 8.26 | 8.26 | 8.26 | 8.28 |

The large resistor degenerates the source-gate voltage  $V_{SG}$  ( $= V_{DD} - I_D R - V_A$ ) of the transistor  $M_{CUR}$ . As the current increases with temperature, the source-gate voltage  $V_{SG}$  decreases, resulting in current suppression, and vice versa. The large resistor consists of 18 p-MOSFETs operating in deep triode region in series connection as shown in Figure 3. The simulation of the bias circuit reveals that the change of the output reference current is suppressed within 1% variation in the temperature range of  $-25^\circ\text{C}$  to  $75^\circ\text{C}$  as shown in Table 1. The power dissipation in operational amplifier biased with this circuit is from 244.4 [nW] to 246.2 [nW] in the temperature range from  $-25^\circ\text{C}$  to  $75^\circ\text{C}$ .

## 2.3 Elements of the Circuitry

Figure 2(a) shows the subthreshold current divider with logarithm voltage converters consisting of operational amplifiers, feedback transistors, and an anti-log converter transistor [2]. The source-gate voltages of respective feedback transistors,  $V_0$ ,  $V_1$ , and  $V_2$  are the function of the current given as

$$V_0 = V_X + \frac{\eta k_B T}{e} \ln\left(\frac{I_0}{I_X}\right) \quad (9)$$

$$V_1 = V_X + \frac{\eta k_B T}{e} \ln\left(\frac{I_1}{I_X}\right) \quad (10)$$

$$V_2 = V_X + \frac{\eta k_B T}{e} \ln\left(\frac{I_2}{I_X}\right) \quad (11)$$

Taking account of the source-gate voltage of a anti-log converter,  $V_{SG,DIV} = V_0 + V_1 - V_2$ , the output current  $I_{DIV}$  is given by

$$\begin{aligned} I_{DIV} &= I_X \exp\left(\frac{e(V_0 + V_1 - V_2 - V_X)}{\eta k_B T}\right) \\ &= I_0 \frac{I_1}{I_2} = I_{ref} \exp\left(\frac{e(V_{GS,1} - V_{GS,2})}{\eta k_B T}\right) \end{aligned}$$

$$= I_{ref} \exp\left(-\frac{\Delta E}{k_B T}\right) \quad (12)$$

which emulates the degradation rate with the activation energy of the products. Note that the current  $I_{ref}$  make this circuitry stable. Without the reference current, the output current  $I_{DIV}$  sometimes results in too low to be detected, because the transistor's junction leakage current overwhelms the emulated current.

As shown in Fig. 2(b), the capacitor  $C$  together with the operational amplifier integrates the current  $I_{DIV}$  to generate  $V_{OUT}$  given by

$$\begin{aligned} V_{OUT} &= V_{CM} - \frac{1}{C} \int_0^{t_1} I_{DIV} dt \\ &= V_{CM} - \frac{I_{ref}}{C} \int_0^{t_1} \exp\left(-\frac{\Delta E}{k_B T}\right) dt \end{aligned} \quad (13)$$

A long time current integration demands the use of a large capacitor, resulting in a large chip size. This can be, however, avoided by introducing iterative integration technique with a small size capacitor. Once the output voltage  $V_{OUT}$  surpasses the comparator's reference voltage  $V_{CMP}$ , the comparator generates a reset pulse to discharge the capacitor so that the total number of the reset pulses is effectively equal to a long time integration of the current.

The system repeating above operations provides the information on the degree of degraded products.

Since the prefactor of Eq. (3) ( $[A]_0$ ,  $[B]_0$ , and  $k_0$ ) and those of Eq. (13) ( $I_{ref}$ , and  $C$ ) are constant when the target materials are specified, the proportionality factor ( $[A]_0[B]_0k_0/\frac{I_{ref}}{C}$ ) can be fixed before shipping, that is, the allowable maximum number of reset pulses can be preset. The counter circuit monitoring the reset pulses consists of D flip flop (DFF) circuits with small occupation area. In the case of materials with small activation energy, the number of the DFFs has to be increased because the allowable maximum number of reset pulses increases for the materials.

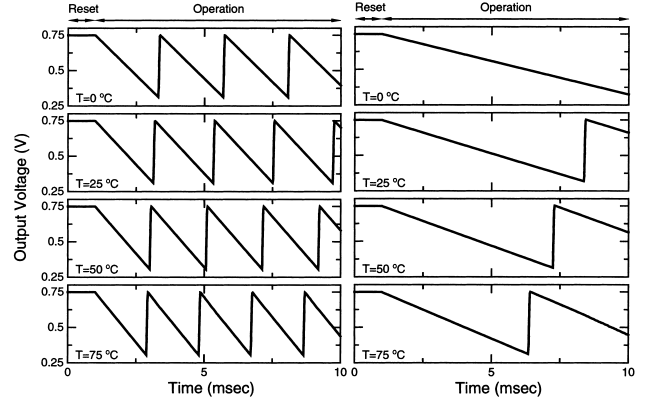
## 2.4 Simulation Results

Figure 4 shows the simulated output voltage of the integrator at different temperatures from 0°C to 75°C. At a given temperature, the output voltage, the integration of the emulated current, linearly decreases with operation period and the slope of the output voltage increase with the operation temperature, both of which are the natural consequences of its operation principle.

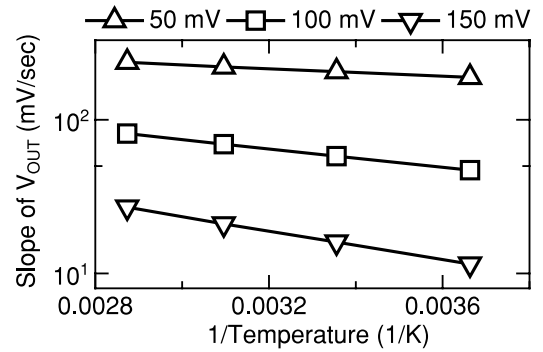
Equation (13) suggests that the slope of the output voltage with time can be expressed as

$$\left|\frac{dV_{OUT}}{dt}\right| = \frac{I_{ref}}{C} \exp\left(-\frac{\Delta E}{k_B T}\right) \quad (14)$$

Eq. (14) indicates that the slope,  $dV_{OUT}/dt$  is a linear function of  $1/T$  in a semi-log plot. This can be shown in Fig. 5 for the cases of different activation energies  $\Delta E$ , representing Arrhenius-type relationship.



**Fig. 4** Simulated output voltage of the integrator at the different temperatures from  $T = 0^\circ\text{C}$  to  $T = 75^\circ\text{C}$ . The left of  $V_{GS2} - V_{GS1}$  is set at 50 mV, and the right 100 mV.



**Fig. 5** The slope of the output voltage of the integrator for different  $V_{GS,2} - V_{GS,1}$  from 50 mV to 150 mV. The horizontal axis shows the reciprocal of temperature, and the vertical axis shows the slope of the output voltage. According to the Eq. (13), the output voltage of the integrator is on the straight line with the reciprocal of temperature.

**Table 2** Performance summary.

|           |  |
|-----------|--|
| Process   | 0.25 $\mu\text{m}$ 1-poly 5-metal CMOS               |
| $V_{DD}$  | 1.5 V  |
| Power     | 1.37 $\mu\text{W}$ ( $T = 75^\circ\text{C}$ )        |
| Chip Area | 510 ( $\mu\text{m}$ ) $\times$ 425 ( $\mu\text{m}$ ) |

The system performance is summarized in Table 2. The simulated power consumption of the circuit is only 1.37  $\mu\text{W}$  at 75°C. A button type battery with 35 mAh ensures that the circuit works for 35 mAh/0.91  $\mu\text{A}$ —4.4 year operation.

## 3. Circuit Implementation

The circuit configuration described in Fig. 2 is difficult to emulate large activation energy because of the reference subthreshold current  $I_{ref}$  being very small value. In order to deal with large activation energy, we implemented the circuit as shown in Fig. 6. A MOSFET generate a  $I_0$  current instead of constant current generation circuit. In this circuit, the output current  $I_{DIV}$  is given by

$$I_{DIV} = I_0 \frac{I_1}{I_2}$$



sured output voltage. This figure shows that both of them are on the straight line, and the same slope with the reciprocal of the temperature, representing Arrhenius-type relationship.

In this paper, we applied the input bias voltages ( $V_{GS,0}$ ,  $V_{GS,1}$ , and  $V_{GS,2}$ ) externally. However, in practical application, these voltages can be generated internally from a multiple diode-connected transistor string with three taps.

#### 4. Conclusion

We proposed a watch-dog circuit for the product quality guarantee which dynamically monitors the subthreshold current of MOSFET. Its operation principle is verified with both SPICE simulation and measurement of the prototype chip designed with a  $0.25\mu\text{m}$  single-poly and 5-metal CMOS process. The new circuitry could be implemented in a tag chip to monitor the degree of degradation for each product upon sale.

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