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# Accurate Small-Signal Modeling of FD-SOI MOSFETs

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**SUMMARY** A new small-signal model for fully depleted silicon-on-insulator (FD-SOI) MOSFETs operating at RF frequencies is presented. The model accounts for the non-quasi-static effect by determining model parameters using a curve fitting procedure to reproduce the frequency response of FD-SOI MOSFETs. The accuracy of the model is validated by comparison of  $S$  parameters with measured results in the range from 0.2 GHz to 20 GHz.

**key words:** FD-SOI, MOSFET, RF, modeling, non-quasi-static

## 1. Introduction

MOSFETs with a fully depleted silicon-on-insulator (FD-SOI) structure have lower substrate capacitance compared to bulk MOSFETs and as such are advantageous for high-frequency circuits [1], [2]. However, short-channel FD-SOI devices operating in the linear region exhibit a relatively long delay in drain conductance as a non-quasi static (NQS) effect [3], [4]. Although the parameters of conventional quasi-static models are usually determined from the measured  $S$  parameters using several direct methods, such methods are not applicable for NQS models due to the large number of unknown parameters. In this paper, a new FD-SOI MOSFET model is proposed in which the parameters are accurately determined for RF operation by curve fitting to experimental results in such a way as to reduce the uncertainty of the model parameters, including NQS channel resistances ( $R_{gsi}$  and  $R_{gdi}$ ) and drain current response times ( $\tau_{gds}$  and  $\tau_{gm}$ ).

## 2. Experimental Results and Discussion

$n$ -MOSFETs with multiple  $n^+$  poly-gate fingers ( $0.14\mu\text{m}$  length by  $5\mu\text{m}$  width per finger) were fabricated on high-resistivity SOI wafers using a  $0.15\mu\text{m}$  FD-SOI CMOS process. A both-side gate connection structure was used in order to reduce gate resistance. The  $S$  parameters were measured with the source and substrate terminals grounded and the body terminal open. Pad and interconnection parasitics were removed from the measured  $S$  parameters by applying a de-embedding procedure using open and short test patterns. Figure 1 shows a widely used small-signal equivalent

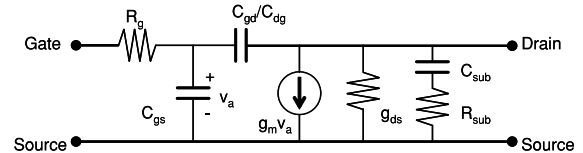


Fig. 1 Conventional small-signal equivalent circuit for an RF MOSFET.

circuit for an RF MOSFET [5]. The measured  $Y$  parameters for an FD-SOI MOSFET with  $W = 5 \times 48\mu\text{m}$  and  $L = 0.14\mu\text{m}$  ( $V_{GS} = 1.0\text{ V}$ ,  $V_{DS} = 0.2\text{ V}$ ) are shown in Fig. 2.

To illustrate the drawbacks of the conventional model,  $Y$  parameters determined by the conventional are compared with those for the new models and measured results in Fig. 2.  $\text{Re}(Y_{11})$  and  $\text{Re}(Y_{21})$  given by the conventional model deviate substantially from the measured results at frequencies higher than 5 GHz. This discrepancy is attributable to the NQS effect, by which the speed of channel charge is limited due to the finite channel conductance produced by every infinitesimal gate-channel capacitor along the channel [4]. As shown in Fig. 3, this effect can be explained by the NQS channel resistances ( $R_{gsi}$  and  $R_{gdi}$ ) coupled to the gate-source, gate-drain capacitances, and resulting delay of  $g_m$ , as described by

$$g_m = \frac{g_{m0}}{1 + j\omega\tau_{gm}} \quad (1)$$

where  $g_{m0}$  is the low-frequency transconductance and  $\tau_{gm}$  is the drain current response time for  $v_{gs}$ . Similar modeling has been investigated in other FETs [6]. The delay of  $g_m$  also contributes transcapacitance ( $C_m$ ) [4].

In addition,  $Y_{22}$  derived by the conventional equivalent circuit increases with frequency in both  $\text{Re}(Y_{22})$  and  $\text{Im}(Y_{22})$ . However, as shown in Fig. 2, the short-channel SOI-MOSFETs measured at  $V_{DS} = 0.2\text{ V}$  exhibit a small decrease in  $\text{Re}(Y_{22})$  over 5 GHz, and a noticeable decrease with frequency in  $\text{Im}(Y_{22})$ . The differences between the measured results and the conventional analytical frequency dependence originate from the delay of the drain current response. For bulk devices, the existence of large drain parasitic capacitances causes appreciable suppression of the frequency dependence caused by the delay of the drain current response. The intrinsic delay of  $g_{ds}$  can be simulated by introducing the frequency dependence of  $g_{ds}$ , as given by [3]

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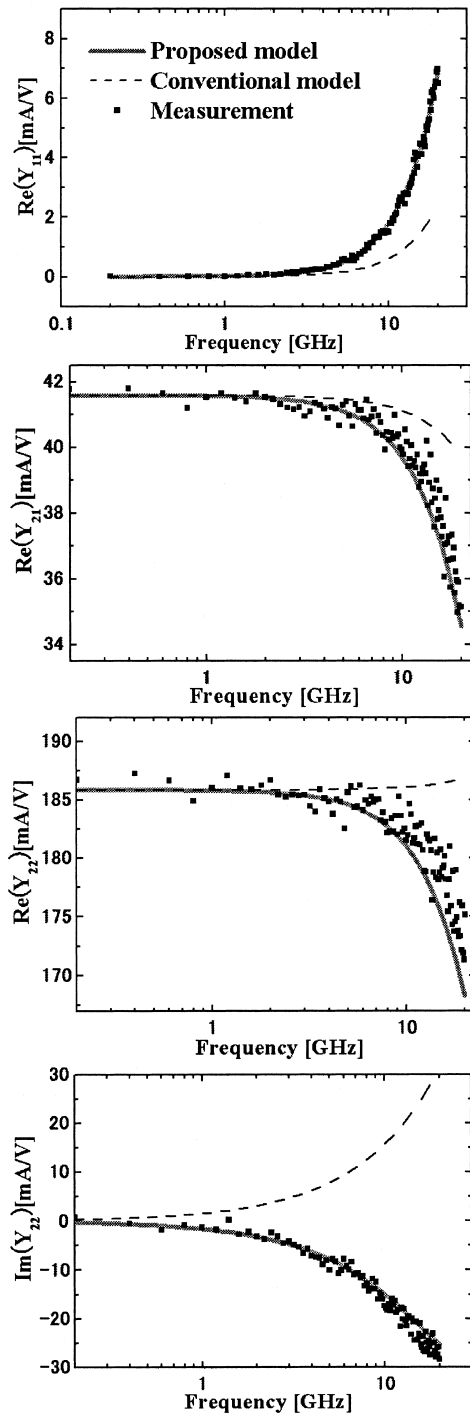


Fig. 2 Comparison of Y parameters for FD-SOI MOSFETs. ( $W = 5 \times 48 \mu\text{m}$ ,  $L = 0.14 \mu\text{m}$ ,  $V_{GS} = 1.0 \text{ V}$ ,  $V_{DS} = 0.2 \text{ V}$ )

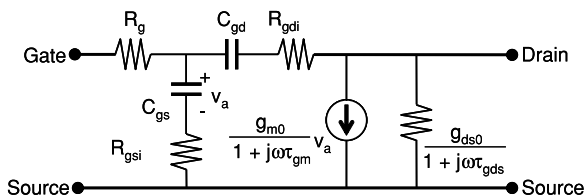


Fig. 3 Proposed RF small-signal equivalent circuit for FD-SOI MOSFETs.

$$g_{ds} = \frac{g_{ds0}}{1 + j\omega\tau_{gds}} \quad (2)$$

where  $g_{ds0}$  is the low-frequency drain conductance and  $\tau_{gds}$  is the drain current response time. The real part of Eq. (2) decreases at high frequency, and the imaginary part with negative sign decreases with increasing frequency, which explains the frequency dependence of the proposed model including the delay of  $g_{ds}$ , as seen in  $Y_{22}$  (Fig. 2).

Although some parts of Fig. 3 may not be modeled with sufficient accuracy by the compact models used in current circuit simulators, those parts may be readily implemented as external components to be added to the compact MOS model in macro or subcircuit model techniques [7].

### 3. Model Parameter Extraction

The values of  $Y_{22}$  calculated by the proposed model, which accounts for the delay, indicate that short-channel FD-SOI devices exhibit drain current response delay, even in the saturation region [3]. Accurate model parameters that are capable of reproducing the small-signal response of FD-SOI MOSFETs in both the linear and saturation regions are therefore necessary. Figure 3 shows the proposed small-signal model for FD-SOI MOSFETs including the NQS effect. The proposed model parameters are determined separately on the input and output sides. The poly-gate resistance ( $R_g$ ) and NQS channel resistances ( $R_{gsi}$  and  $R_{gdi}$ ) must be determined separately due to the irregular geometry and bias dependence of the effective gate resistance resulting from the combined distributed effects in both the gate and channel at high frequency [8].

In the first step, the input-side parameters for the proposed model ( $C_{gs}$ ,  $C_{gd}$ ,  $R_g$ ,  $R_{gsi}$ ,  $R_{gdi}$ ) are determined.  $C_{gs}$  and  $C_{gd}$  can be obtained from the measured results as follows.

$$C_{gd} = -\text{Im}(Y_{12})/\omega \quad (3)$$

$$C_{gs} = (\text{Im}(Y_{11}) + \text{Im}(Y_{12}))/\omega \quad (4)$$

$R_g$  can be found by reducing the fitting parameter, i.e.,

$$R_g = \frac{1}{12} R_{sg} \frac{W_f}{L_f} \frac{1}{N_f} \quad (5)$$

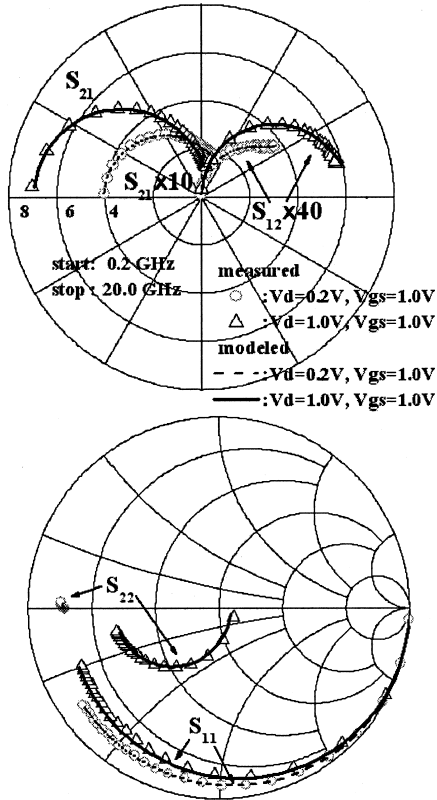
where  $R_{sg}$  is the sheet resistance of gate polysilicon,  $W_f$  is the gate width per finger,  $L_f$  is the gate length, and  $N_f$  is the number of gate fingers.  $R_{gsi}$  and  $R_{gdi}$  are determined by curve fitting.

In the second step, the output-side parameters for the proposed model ( $g_{m0}$ ,  $g_{ds0}$ ,  $\tau_{gds}$ ,  $\tau_{gm}$ ) are determined. Here,  $g_{m0}$  and  $g_{ds0}$  are also derived from the measured results, as follows.

$$g_{m0} = \text{Re}(Y_{21}) \quad (6)$$

$$g_{ds0} = \text{Re}(Y_{22}) \quad (7)$$

Similarly,  $\tau_{gds}$  and  $\tau_{gm}$  are determined by curve fitting. In this study,  $C_{sub}$  and  $R_{sub}$  in Fig. 3 are neglected, due to low



**Fig. 4** Measured and modeled  $S$  parameters with  $W = 5 \times 48 \mu\text{m}$  and  $L = 0.14 \mu\text{m}$  in the linear and saturation regions.

**Table 1** Extracted parameters for a  $5 \times 48 \mu\text{m}/0.14 \mu\text{m}$  MOS device under various bias conditions.

	$V_{GS}=1.0 \text{ V}$ $V_{DS}=1.0 \text{ V}$	$V_{GS}=1.0 \text{ V}$ $V_{DS}=0.2 \text{ V}$
$g_{m0}$ (mS)	130.6	41.6
$g_{ds0}$ (mS)	17.0	185.6
$C_{gd}$ (fF)	123.6	240.8
$C_{gs}$ (fF)	230.3	183.8
$R_g$ ( $\Omega$ )	0.83	0.83
$R_{gsi}$ ( $\Omega$ )	7.1	8.4
$R_{gdi}$ ( $\Omega$ )	2.0	0.3
$\tau_{gds}$ (ps)	0	3.5
$\tau_{gm}$ (ps)	2.0	2.75

drain-source and drain-body capacitances. Figure 4 shows the measured  $S$  parameters and the results obtained by the proposed small-signal model with the parameters listed in

Table 1. This figure demonstrates good agreement between the measured and modeled  $S$  parameter up to 20 GHz.

#### 4. Conclusion

Short-channel FD-SOI MOS devices operating in the linear region exhibit substantial drain current response delay due to the small parasitic capacitance in such devices. To explain this phenomenon, an accurate small-signal model for FD-SOI MOSFETs operating at high frequency was presented. The model parameters attributed to the NQS effect are accurately determined by curve fitting. The validity of the proposed model was demonstrated by comparison of  $S$  parameters with measured results at up to 20 GHz.

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#### References

- [1] F. Ichikawa, Y. Nagatomo, Y. Katakura, M. Itoh, S. Itoh, H. Matsushashi, T. Ichimori, N. Hirashita, and S. Baba, "Fully depleted SOI process and technology for digital and RF applications," *Solid-State Electron.*, vol.48, pp.999–1006, 2004.
- [2] A.O. Adan, T. Yoshimatsu, S. Shitara, N. Tanba, and M. Fukumi, "Linearity and low-noise performance of SOI MOSFETs for RF applications," *IEEE Trans. Electron Devices*, vol.49, no.5, pp.881–888, May 2002.
- [3] Y. Shimizu, G. Kim, B. Murakami, K. Ueda, Y. Utsurogi, S. Cha, T. Matsuoka, and K. Taniguchi, "Drain current response delay of FD-SOI MOSFETs in RF operation," *IEICE Electronics Express*, vol.1, no.16, pp.518–522, Nov. 2004.
- [4] Y. Tividis, "High-frequency small-signal models," in *Operation and Modeling of the MOS Transistor*, 2nd ed., pp.440–512, McGraw-Hill, 1999.
- [5] I. Kwon, M. Je, K. Lee, and H. Shin, "A new small signal modeling of RF MOSFETs including charge conservation capacitances," *Proc. European Solid-State Circuits Conference*, pp.296–299, Sept. 2000.
- [6] W.R. Curtice, "The performance of submicrometer gate length GaAs MESFET's," *IEEE Trans. Electron Devices*, vol.30, no.12, pp.1693–1699, Dec. 1983.
- [7] C.C. Enz and Y. Cheng, "MOS transistor modeling for RF IC," *IEEE J. Solid-State Circuits*, vol.35, no.2, pp.186–201, Feb. 2000.
- [8] Y. Cheng and M. Matloubian, "High frequency characterization of gate resistance in RF MOSFETs," *IEEE Electron Device Lett.*, vol.22, no.2, pp.98–100, Feb. 2001.